

VSCLIB v1.0 User Manual

Naohiko Shimizu

February 25, 2025

Contents

I Vsclib 1.0 library concepts	4
1 Vsclib from Graham Petley	4
2 My modification to the vsclib	4
2.1 To be DRC clean against Skywater 130 and IHP sg13g2	4
2.2 Solve the Cell to Cell DRC problems	5
2.3 Functional Verification with Hitas and Alliance	5
2.4 make '.lib' file for synthesis	5
II Implementation	6
3 Individual cells	6
3.1 an2v0x05	7
3.2 an2v0x1	9
3.3 an2v0x4	11
3.4 an2v0x8	13
3.5 an3v0x05	15
3.6 an3v0x1	17
3.7 an3v0x2	19
3.8 an3v6x05	21
3.9 an4v0x05	23
3.10 aoi112v0x05	25
3.11 aoi211v0x05	27
3.12 aoi211v0x1	29
3.13 aoi211v0x2	31
3.14 aoi211v5x05	33
3.15 aoi21a2bv0x05	35
3.16 aoi21a2bv5x05	37
3.17 aoi21a2v0x05	39
3.18 aoi21bv0x05	41
3.19 aoi21v0x05	43
3.20 aoi22v0x05	45
3.21 aoi22v0x1	47
3.22 aoi22v5x05	49

3.23 aoi31v0x05	51
3.24 aoi31v0x1	53
3.25 aoi31v0x2	55
3.26 aon21bv0x05	57
3.27 aon21bv0x1	59
3.28 aon21bv0x2	61
3.29 aon21v0x05	63
3.30 bf1v0x05	65
3.31 bf1v0x12	67
3.32 bf1v0x1	69
3.33 bf1v0x2	71
3.34 bf1v0x4	73
3.35 bf1v0x8	75
3.36 bf1v5x05	77
3.37 dfnt1v0x2	79
3.38 dly1v0x05	81
3.39 dly2v0x05	83
3.40 iv1v0x05	85
3.41 iv1v1x05	87
3.42 lant1v0x05	89
3.43 mx12v0x05	91
3.44 mx12v0x2	93
3.45 mxn2v0x05	95
3.46 nd2abv0x05	97
3.47 nd2av0x05	99
3.48 nd2av0x1	101
3.49 nd2av0x2	103
3.50 nd2av0x4	105
3.51 nd2v0x05	107
3.52 nd2v0x1	109
3.53 nd2v0x2	111
3.54 nd2v0x4	113
3.55 nd2v3x05	115
3.56 nd2v5x05	117
3.57 nd3abv0x05	119
3.58 nd3av0x05	121
3.59 nd3v0x05	123
3.60 nd3v0x1	125
3.61 nd4v0x05	127
3.62 nd4v0x1	129
3.63 nd4v0x2	131
3.64 nr2av0x1	133
3.65 nr2av0x2	135
3.66 nr2av0x4	137
3.67 nr2av1x05	139
3.68 nr2v0x05	141
3.69 nr2v0x1	143
3.70 nr2v0x4	145
3.71 nr2v1x05	147
3.72 nr3abv0x05	149

3.73 nr3av0x05	151
3.74 nr3v0x05	153
3.75 nr3v0x1	155
3.76 nr3v0x2	157
3.77 nr3v0x4	159
3.78 nr3v1x05	161
3.79 nr4v0x1	163
3.80 nr4v0x2	165
3.81 nr4v1x05	167
3.82 oai211v0x05	169
3.83 oai21a2bv0x05	171
3.84 oai21a2v0x05	173
3.85 oai21bv0x05	175
3.86 oai21v0x05	177
3.87 oai21v0x1	179
3.88 oai21v0x4	181
3.89 oai22v0x05	183
3.90 oai23av0x05	185
3.91 oai31v0x05	187
3.92 oai31v0x1	189
3.93 oan21bv0x05	191
3.94 oan21v0x05	193
3.95 or2v0x05	195
3.96 or2v0x1	197
3.97 or3v0x05	199
3.98 or3v0x1	201
3.99 or3v0x2	203
3.100or3v4x05	205
3.101or4v0x05	207
3.102or4v4x05	209
3.103rowend_x0	211
3.104tie_x0	213
3.105vddtie	215
3.106vsstie	217
3.107xaon21v0x05	219
3.108xnr2v8x05	221
3.109xnr3v1x05	223
3.110xoon21v0x05	225
3.111xor2v0x05	227
3.112xor2v1x05	229
3.113xor2v2x05	231
3.114xor2v8x05	233
3.115xor3v1x05	235

Part I

Vsclib 1.0 library concepts

1 Vsclib from Graham Petley

Graham Petley's web page <https://www.vlsitechnology.org/index.html> VLSI and ASIC Technology Standard Cell Library Design provides several cell libraries which are compatible to Alliance. Among the libraries, the smallest foot print one is the vsclib which has 72 lambda cell height and 8 lambda wiring pitch. Graham Petley may generate the similar libraries from some scripts. Then the library had bad designed cells to use, and some of them did not work. Also he has too many same functional cells with almost the same drivability that seems to be redundant. Therefore, I manually modified most of them and remove redundant cells.

I hope that with the small footprint of the cell may help to reduce the total chip area. But unfortunately, until now, the objective was not achieved yet.

2 My modification to the vsclib

I made the modifications on the vsclib with the following views.

1. To be DRC clean against Skywater 130 and IHP sg13g2.
 2. Correct functionality of the cells.
 3. Solve the Cell to Cell DRC problems
 4. STA compatible description.

2.1 To be DRC clean against Skywater 130 and IHP sg13g2

I wrote RDS conversion table and check the generated GDS against PDK DRC rules. Both Skywater 130 and IHP sg13g2 have similar physical appearance but each has different constraints.

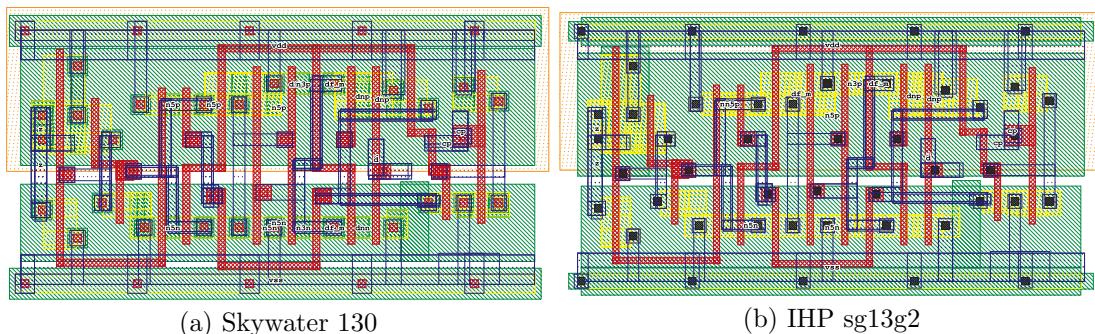


Figure 1: The flip flop cell adapted to Skywater 130 and IHP sg13g2

2.2 Solve the Cell to Cell DRC problems

Even if each cell passes the DRC, when they are in the layout, some constraints between cell will cause DRC errors. There were a lot of errors but biggest problem was iron implants separations. Because, the original vsclib did not have enough enclosure and/or separation of the implants. Also active to active separation between cell caused problems. Therefore, I decided to modify them manually, and I made the required implants from the n-well position.

In addition to the errors, to stabilize the well potential, I added the tie area and the body contacts on the top and bottom edge of the cells.

2.3 Functional Verification with Hitas and Alliance

Hitas extracts the behavior of the cells from the Spice net list. After then, we can use 'proof' in Alliance to verify the behavior in functional method. There are some problems around memory cells (FF and Latch) for Hitas to detect the behavior functionality. Therefore, I modified the behavior description on the Vsclib to meet the restriction of the Hitas.

2.4 make '.lib' file for synthesis

After the functional verification, we can proceed to make '.lib' file from the layout. We will evaluate the gate delay, gate capacitance, etc.

Part II

Implementation

In this section, we will see the cells in nsxlib. We will show the cell behavior VHDL and layout.

3 Individual cells

The implemented cells to be available for the Skywater 130 and IHP sg13g2 are 115 cells. We will see each of them in the following sheets. The functionality and the symbolic layout will be shown.

3.1 an2v0x05

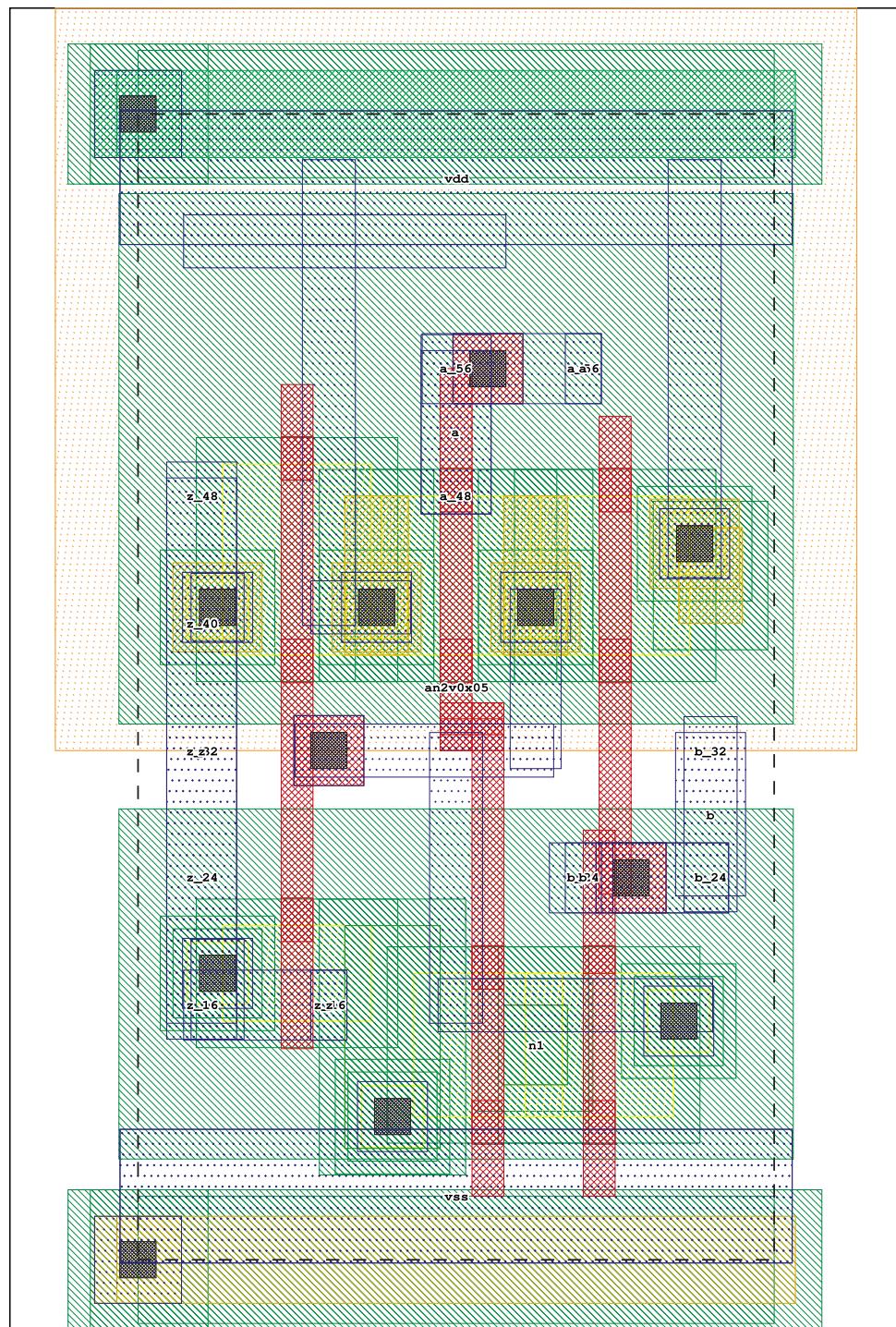
```

ENTITY an2v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT cin_a          : NATURAL := 3;
    CONSTANT rdown_b_z      : NATURAL := 3860;
    CONSTANT rdown_a_z      : NATURAL := 3870;
    CONSTANT rup_b_z        : NATURAL := 4960;
    CONSTANT rup_a_z        : NATURAL := 4960;
    CONSTANT tphh_a_z       : NATURAL := 69;
    CONSTANT tphh_b_z       : NATURAL := 70;
    CONSTANT tp11_b_z       : NATURAL := 90;
    CONSTANT tp11_a_z       : NATURAL := 99;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END an2v0x05;

ARCHITECTURE behaviour_data_flow OF an2v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an2v0x05"
    SEVERITY WARNING;
    z <= (b and a) after 192 ps;
END;

```



3.2 an2v0x1

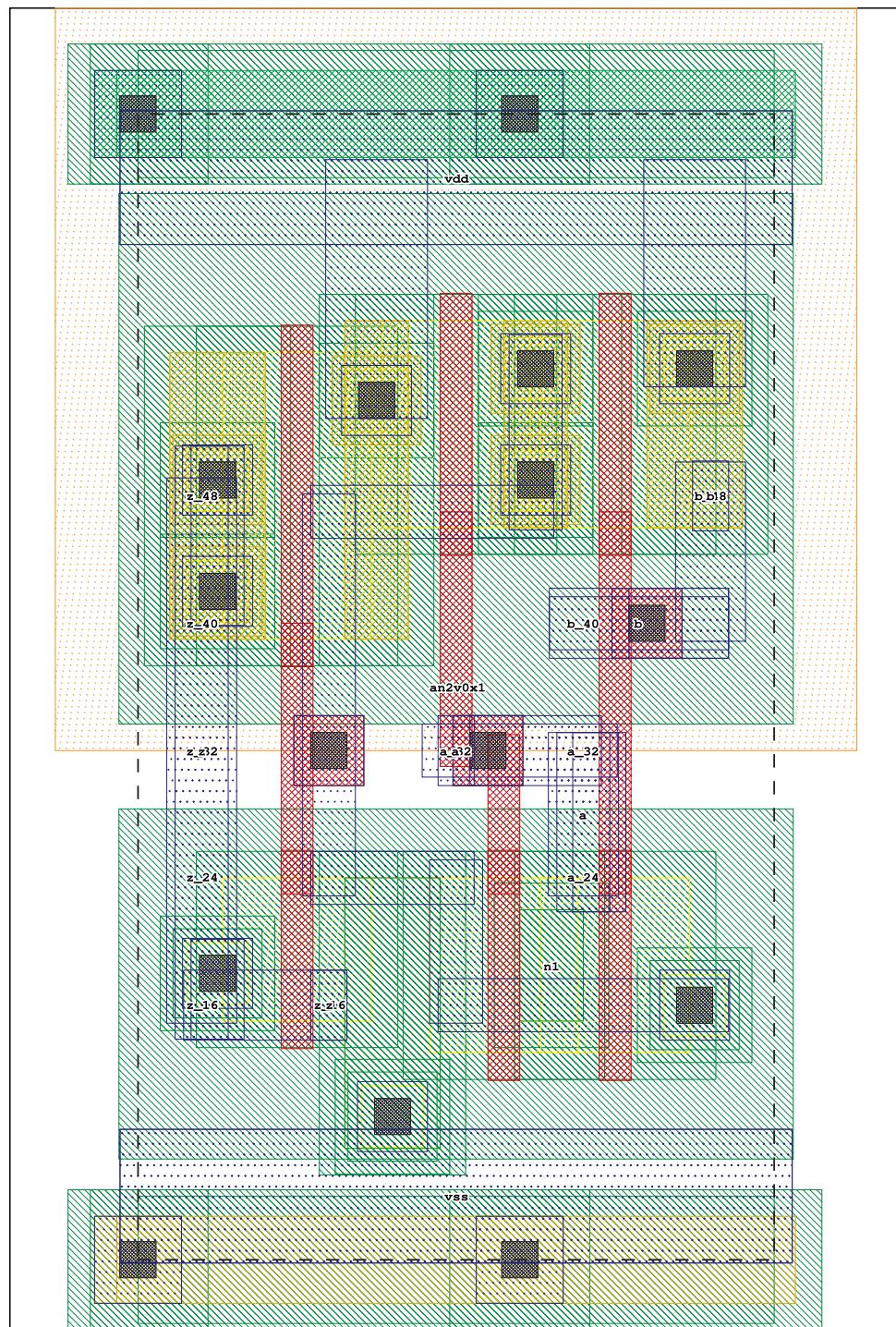
```

ENTITY an2v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT rdown_b_z     : NATURAL := 2570;
    CONSTANT rdown_a_z     : NATURAL := 2580;
    CONSTANT rup_b_z       : NATURAL := 3310;
    CONSTANT rup_a_z       : NATURAL := 3310;
    CONSTANT tphh_a_z      : NATURAL := 73;
    CONSTANT tphh_b_z      : NATURAL := 73;
    CONSTANT tp11_b_z      : NATURAL := 91;
    CONSTANT tp11_a_z      : NATURAL := 101;
    CONSTANT transistors   : NATURAL := 6
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END an2v0x1;

ARCHITECTURE behaviour_data_flow OF an2v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an2v0x1"
    SEVERITY WARNING;
    z <= (b and a) after 158 ps;
END;

```



3.3 an2v0x4

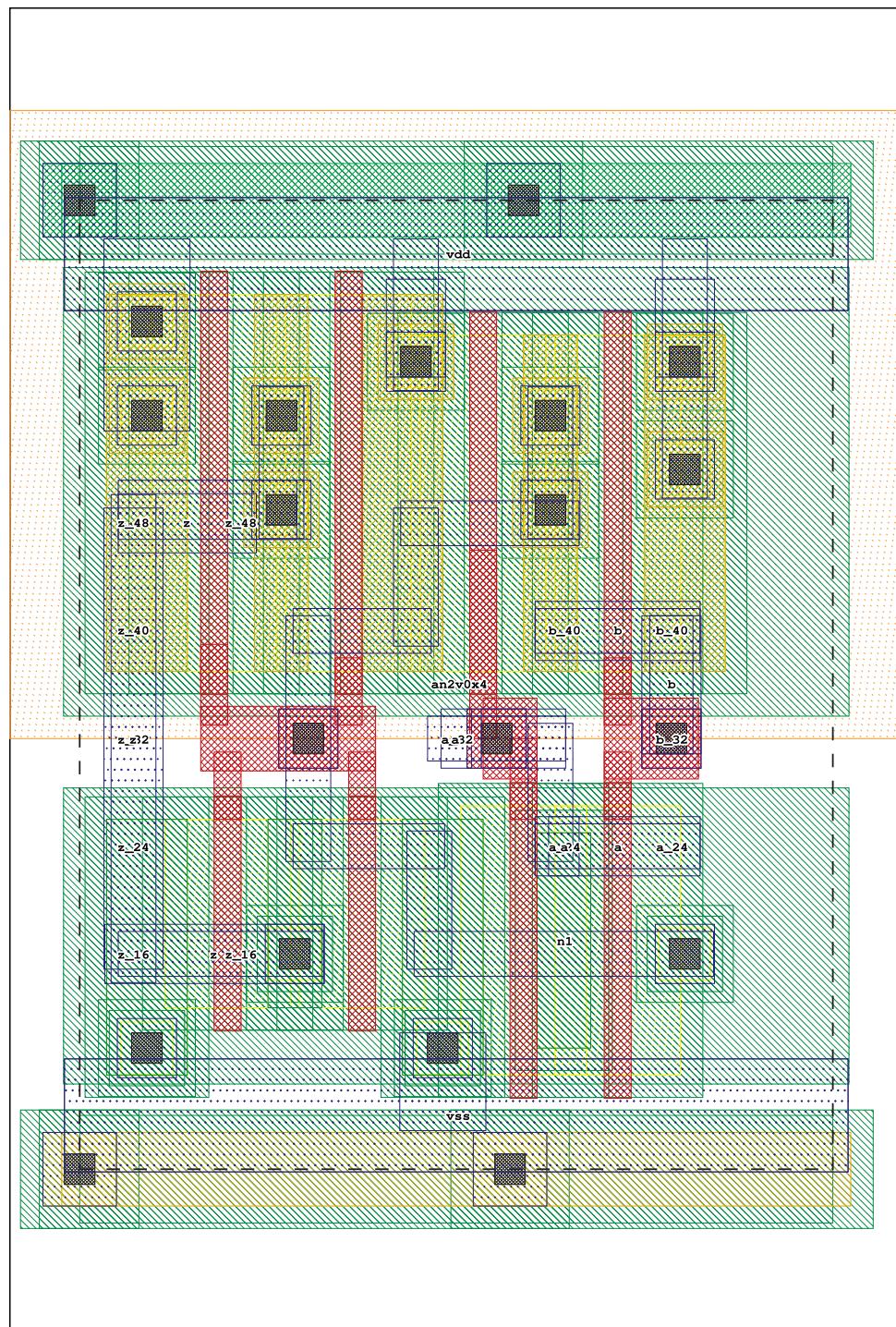
```

ENTITY an2v0x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b         : NATURAL := 6;
    CONSTANT cin_a         : NATURAL := 6;
    CONSTANT rdown_b_z     : NATURAL := 830;
    CONSTANT rdown_a_z     : NATURAL := 840;
    CONSTANT rup_b_z       : NATURAL := 1070;
    CONSTANT rup_a_z       : NATURAL := 1070;
    CONSTANT tphh_a_z      : NATURAL := 74;
    CONSTANT tphh_b_z      : NATURAL := 75;
    CONSTANT tp11_b_z       : NATURAL := 92;
    CONSTANT tp11_a_z       : NATURAL := 100;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END an2v0x4;

ARCHITECTURE behaviour_data_flow OF an2v0x4 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an2v0x4"
    SEVERITY WARNING;
    z <= (b and a) after 109 ps;
END;

```



3.4 an2v0x8

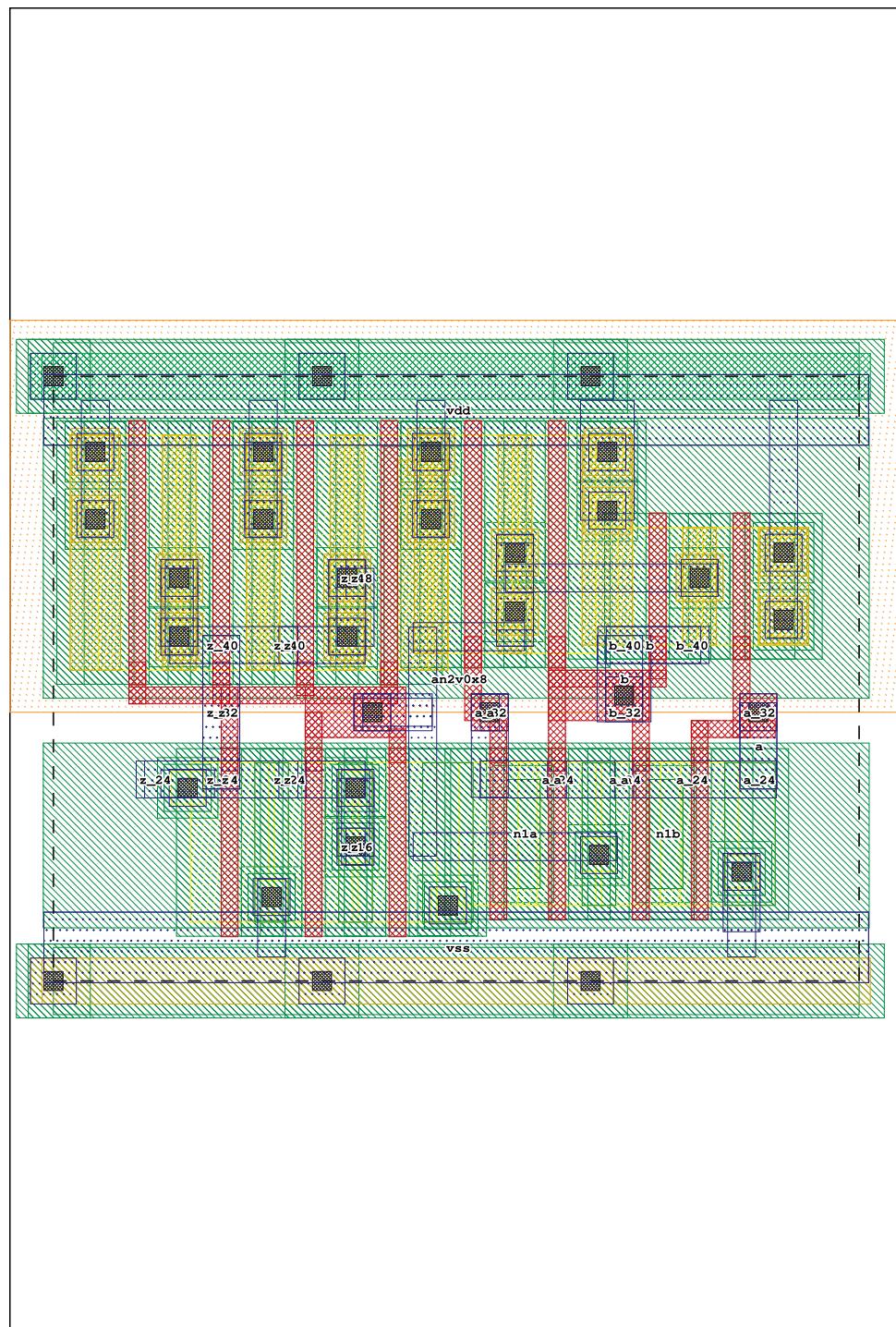
```

ENTITY an2v0x8 IS
GENERIC (
    CONSTANT area          : NATURAL := 6912;
    CONSTANT cin_b         : NATURAL := 9;
    CONSTANT cin_a         : NATURAL := 10;
    CONSTANT rdown_b_z     : NATURAL := 410;
    CONSTANT rdown_a_z     : NATURAL := 410;
    CONSTANT rup_b_z       : NATURAL := 530;
    CONSTANT rup_a_z       : NATURAL := 530;
    CONSTANT tphh_a_z      : NATURAL := 76;
    CONSTANT tphh_b_z      : NATURAL := 77;
    CONSTANT tp11_b_z       : NATURAL := 97;
    CONSTANT tp11_a_z       : NATURAL := 106;
    CONSTANT transistors   : NATURAL := 16
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END an2v0x8;

ARCHITECTURE behaviour_data_flow OF an2v0x8 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an2v0x8"
    SEVERITY WARNING;
    z <= (b and a) after 101 ps;
END;

```



3.5 an3v0x05

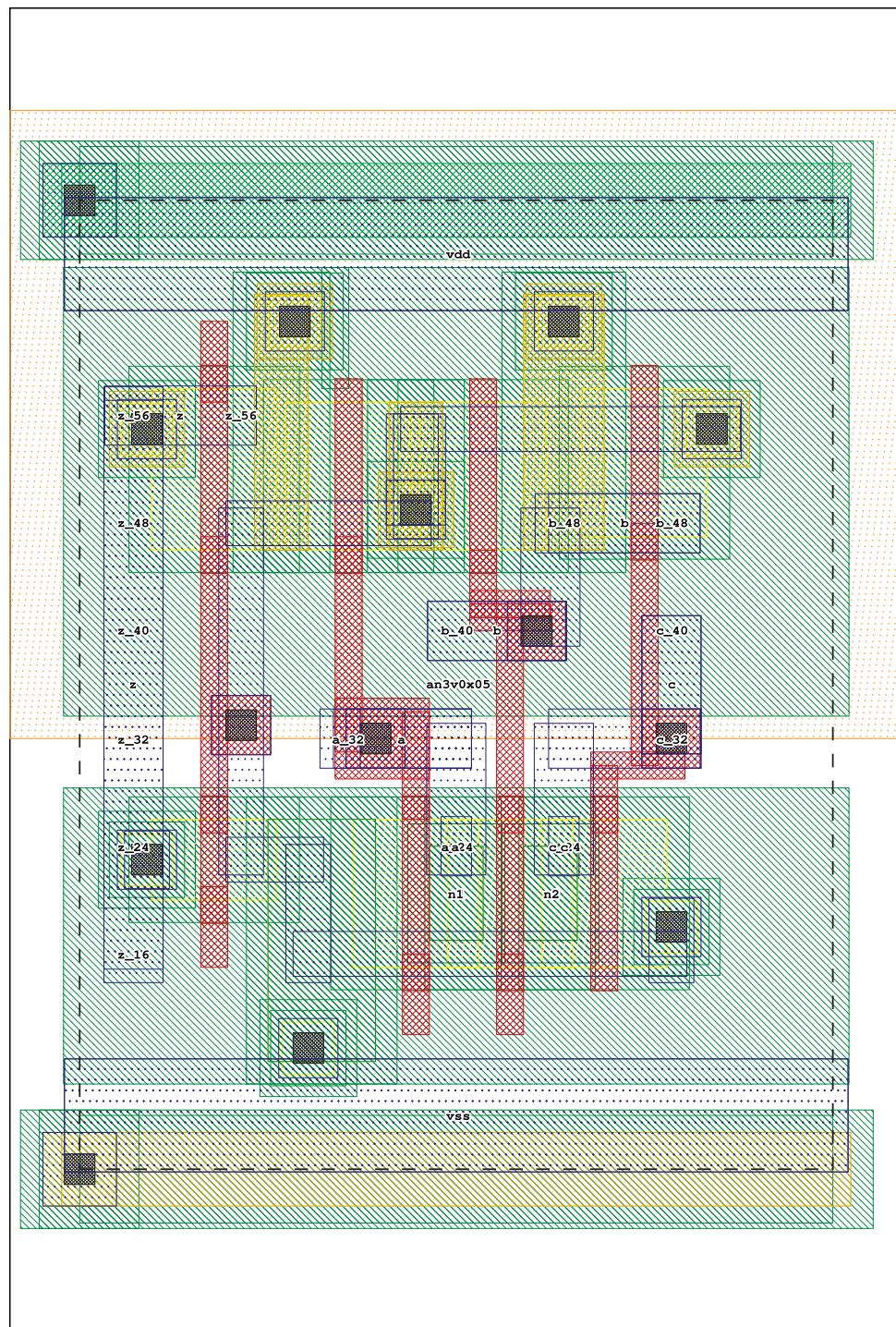
```

ENTITY an3v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 3950;
    CONSTANT rdown_b_z     : NATURAL := 3910;
    CONSTANT rdown_c_z     : NATURAL := 3890;
    CONSTANT rup_a_z       : NATURAL := 5010;
    CONSTANT rup_b_z       : NATURAL := 5010;
    CONSTANT rup_c_z       : NATURAL := 5010;
    CONSTANT tphh_c_z      : NATURAL := 88;
    CONSTANT tphh_b_z      : NATURAL := 93;
    CONSTANT tphh_a_z      : NATURAL := 94;
    CONSTANT tp11_a_z       : NATURAL := 120;
    CONSTANT tp11_b_z       : NATURAL := 111;
    CONSTANT tp11_c_z       : NATURAL := 100;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END an3v0x05;

ARCHITECTURE behaviour_data_flow OF an3v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an3v0x05"
    SEVERITY WARNING;
    z <= ((a and b) and c) after 213 ps;
END;

```



3.6 an3v0x1

```

ENTITY an3v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 4;
    CONSTANT rdown_a_z     : NATURAL := 2610;
    CONSTANT rdown_b_z     : NATURAL := 2600;
    CONSTANT rdown_c_z     : NATURAL := 2580;
    CONSTANT rup_a_z       : NATURAL := 3330;
    CONSTANT rup_b_z       : NATURAL := 3330;
    CONSTANT rup_c_z       : NATURAL := 3330;
    CONSTANT tphh_c_z      : NATURAL := 89;
    CONSTANT tphh_b_z      : NATURAL := 93;
    CONSTANT tphh_a_z      : NATURAL := 94;
    CONSTANT tp11_a_z       : NATURAL := 121;
    CONSTANT tp11_b_z       : NATURAL := 112;
    CONSTANT tp11_c_z       : NATURAL := 101;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END an3v0x1;

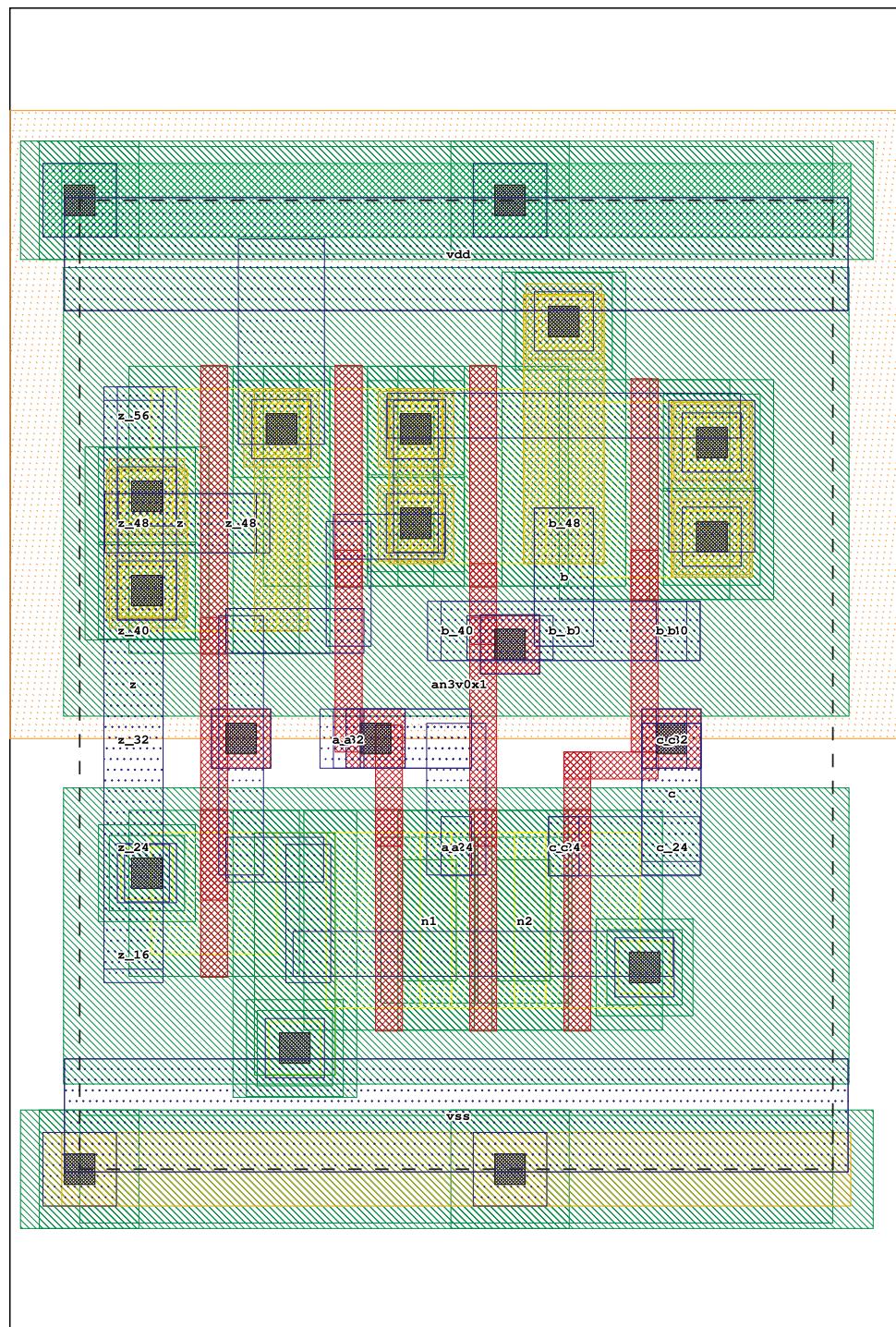
```

```

ARCHITECTURE behaviour_data_flow OF an3v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an3v0x1"
    SEVERITY WARNING;
    z <= ((a and b) and c) after 176 ps;
END;

```



3.7 an3v0x2

```

ENTITY an3v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 5;
    CONSTANT cin_b         : NATURAL := 5;
    CONSTANT cin_c         : NATURAL := 5;
    CONSTANT rdown_a_z     : NATURAL := 1700;
    CONSTANT rdown_b_z     : NATURAL := 1680;
    CONSTANT rdown_c_z     : NATURAL := 1670;
    CONSTANT rup_a_z       : NATURAL := 2150;
    CONSTANT rup_b_z       : NATURAL := 2150;
    CONSTANT rup_c_z       : NATURAL := 2150;
    CONSTANT tphh_c_z      : NATURAL := 86;
    CONSTANT tphh_b_z      : NATURAL := 89;
    CONSTANT tphh_a_z      : NATURAL := 91;
    CONSTANT tp11_a_z       : NATURAL := 118;
    CONSTANT tp11_b_z       : NATURAL := 109;
    CONSTANT tp11_c_z       : NATURAL := 98;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END an3v0x2;

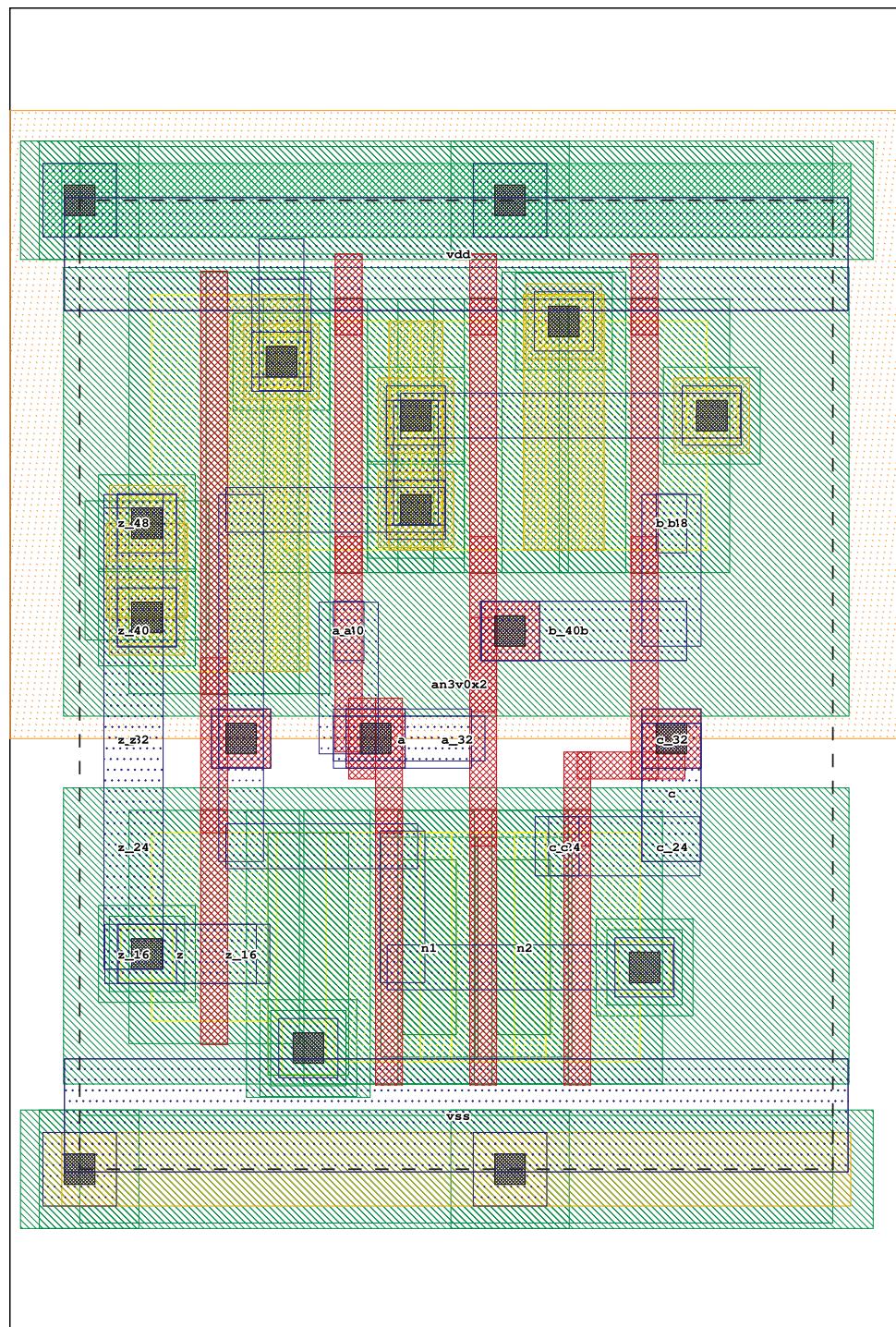
```

```

ARCHITECTURE behaviour_data_flow OF an3v0x2 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an3v0x2"
    SEVERITY WARNING;
    z <= ((a and b) and c) after 146 ps;
END;

```



3.8 an3v6x05

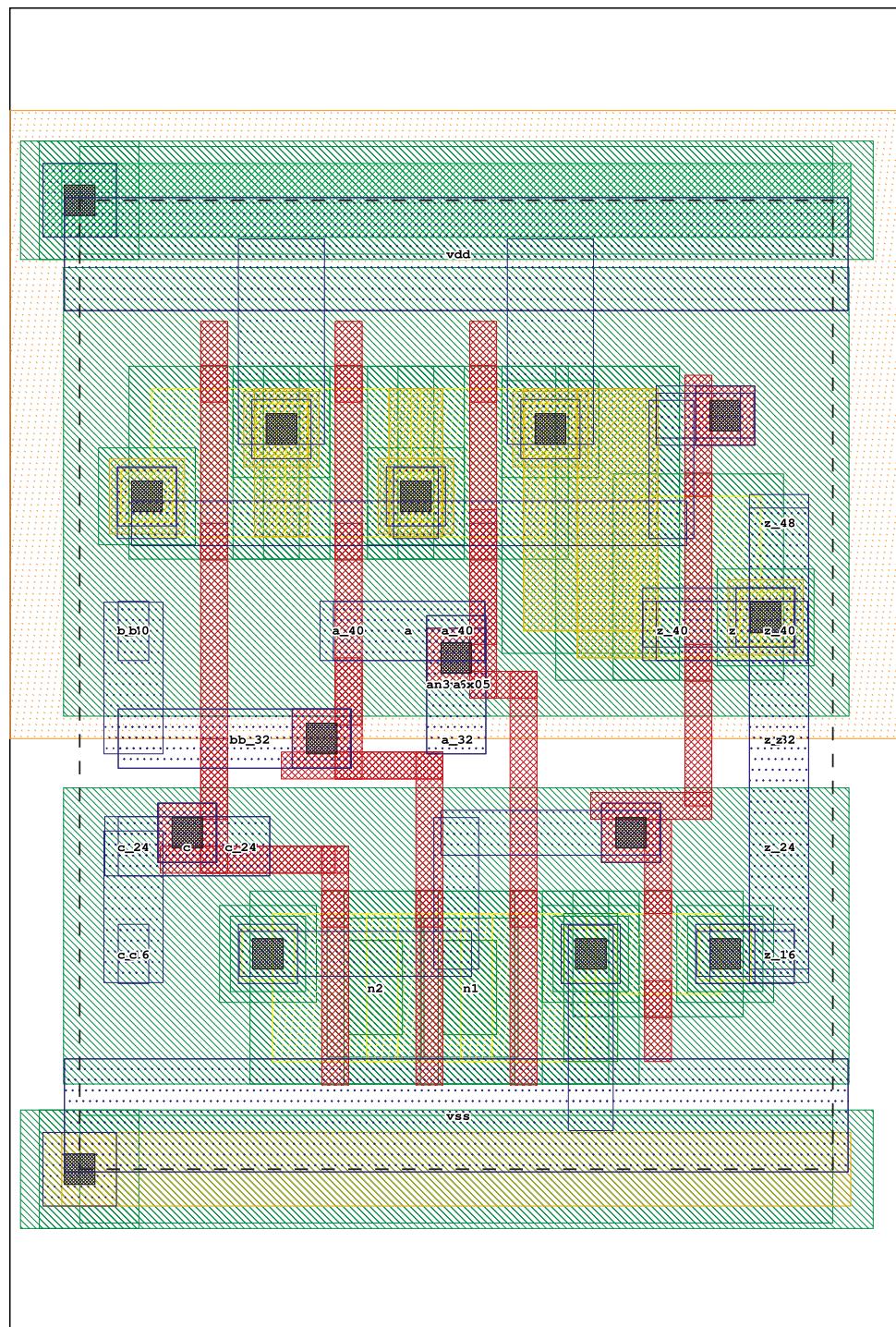
```

ENTITY an3v6x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 3930;
    CONSTANT rdown_b_z     : NATURAL := 3910;
    CONSTANT rdown_c_z     : NATURAL := 3880;
    CONSTANT rup_a_z       : NATURAL := 4990;
    CONSTANT rup_b_z       : NATURAL := 5000;
    CONSTANT rup_c_z       : NATURAL := 5000;
    CONSTANT tphh_c_z      : NATURAL := 86;
    CONSTANT tphh_b_z      : NATURAL := 90;
    CONSTANT tphh_a_z      : NATURAL := 91;
    CONSTANT tp11_a_z      : NATURAL := 117;
    CONSTANT tp11_b_z      : NATURAL := 109;
    CONSTANT tp11_c_z      : NATURAL := 98;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END an3v6x05;

ARCHITECTURE behaviour_data_flow OF an3v6x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an3v6x05"
    SEVERITY WARNING;
    z <= ((a and b) and c) after 210 ps;
END;

```



3.9 an4v0x05

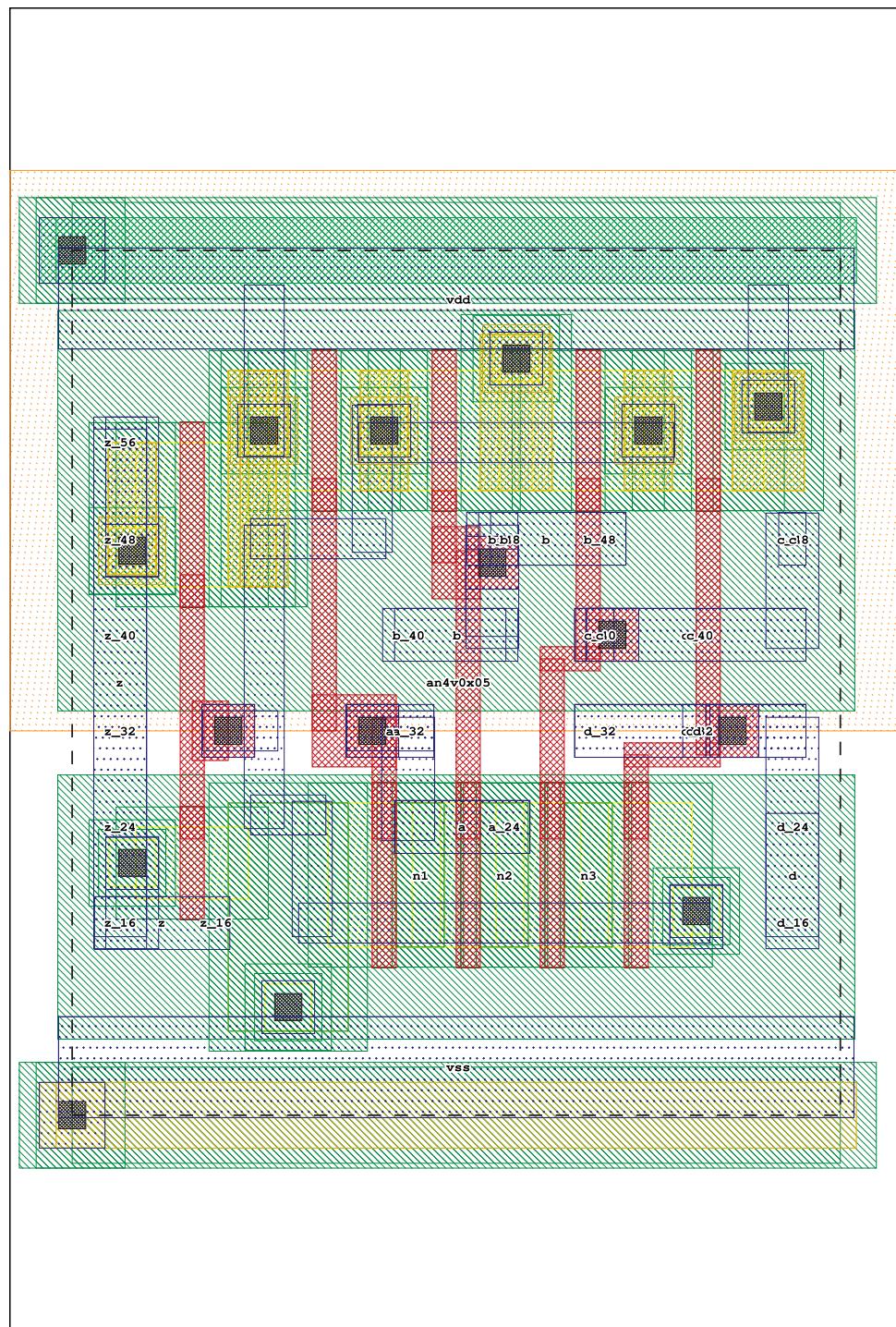
```

ENTITY an4v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT cin_c          : NATURAL := 3;
    CONSTANT cin_d          : NATURAL := 3;
    CONSTANT rdown_a_z      : NATURAL := 4040;
    CONSTANT rdown_b_z      : NATURAL := 3990;
    CONSTANT rdown_c_z      : NATURAL := 3950;
    CONSTANT rdown_d_z      : NATURAL := 3920;
    CONSTANT rup_a_z         : NATURAL := 5060;
    CONSTANT rup_b_z         : NATURAL := 5060;
    CONSTANT rup_c_z         : NATURAL := 5060;
    CONSTANT rup_d_z         : NATURAL := 5060;
    CONSTANT tphh_a_z        : NATURAL := 114;
    CONSTANT tphh_b_z        : NATURAL := 110;
    CONSTANT tpll_d_z        : NATURAL := 107;
    CONSTANT tphh_c_z        : NATURAL := 104;
    CONSTANT tpll_c_z        : NATURAL := 119;
    CONSTANT tphh_d_z        : NATURAL := 97;
    CONSTANT tpll_b_z        : NATURAL := 131;
    CONSTANT tpll_a_z        : NATURAL := 140;
    CONSTANT transistors     : NATURAL := 10
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    d      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END an4v0x05;

ARCHITECTURE behaviour_data_flow OF an4v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an4v0x05"
    SEVERITY WARNING;
    z <= (((a and b) and c) and d) after 228 ps;
END;

```



3.10 aoi112v0x05

```

ENTITY aoi112v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 3456;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT cin_c1         : NATURAL := 5;
    CONSTANT cin_c2         : NATURAL := 5;
    CONSTANT rdown_a_z      : NATURAL := 4010;
    CONSTANT rdown_b_z      : NATURAL := 3920;
    CONSTANT rdown_c1_z     : NATURAL := 4160;
    CONSTANT rdown_c2_z     : NATURAL := 4140;
    CONSTANT rup_a_z        : NATURAL := 5970;
    CONSTANT rup_b_z        : NATURAL := 5960;
    CONSTANT rup_c1_z       : NATURAL := 6240;
    CONSTANT rup_c2_z       : NATURAL := 6270;
    CONSTANT tphl_a_z       : NATURAL := 84;
    CONSTANT tphl_b_z       : NATURAL := 77;
    CONSTANT tphl_c2_z      : NATURAL := 58;
    CONSTANT tphl_c1_z      : NATURAL := 53;
    CONSTANT tphl_b_z       : NATURAL := 95;
    CONSTANT tphl_c1_z      : NATURAL := 64;
    CONSTANT tphl_a_z       : NATURAL := 103;
    CONSTANT tphl_c2_z      : NATURAL := 55;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c1    : in  BIT;
    c2    : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END aoi112v0x05;

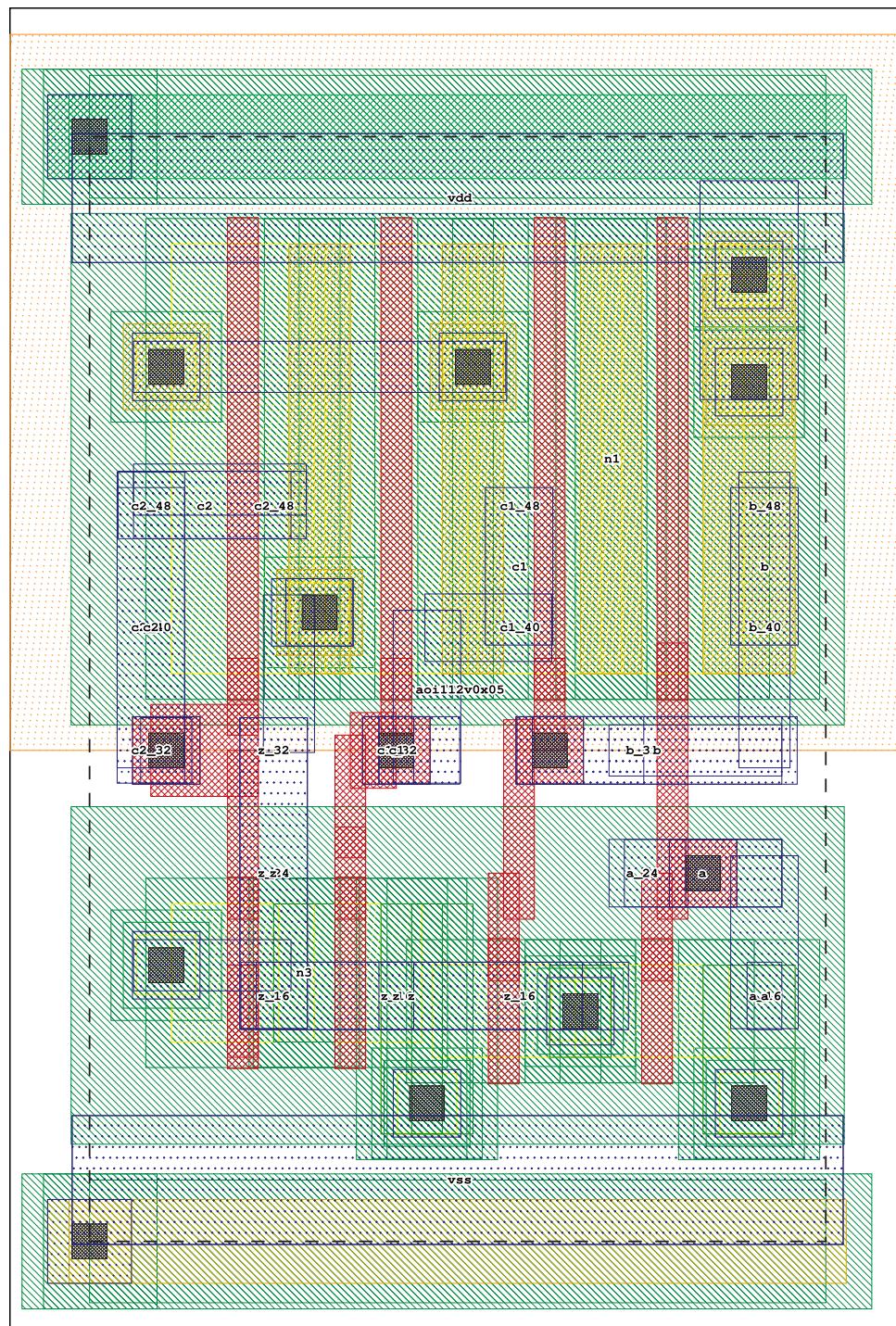
```

ARCHITECTURE behaviour_data_flow OF aoi112v0x05 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi112v0x05"
    SEVERITY WARNING;
    z <= not ((a or b) or (c1 and c2)) after 201 ps;
END;

```



3.11 aoi211v0x05

```

ENTITY aoi211v0x05 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3456;
    CONSTANT cin_b         : NATURAL := 5;
    CONSTANT cin_c         : NATURAL := 5;
    CONSTANT cin_a1        : NATURAL := 5;
    CONSTANT cin_a2        : NATURAL := 5;
    CONSTANT rdown_b_z     : NATURAL := 3900;
    CONSTANT rdown_c_z     : NATURAL := 3910;
    CONSTANT rdown_a1_z    : NATURAL := 4430;
    CONSTANT rdown_a2_z    : NATURAL := 4420;
    CONSTANT rup_b_z       : NATURAL := 5920;
    CONSTANT rup_c_z       : NATURAL := 5890;
    CONSTANT rup_a1_z      : NATURAL := 6280;
    CONSTANT rup_a2_z      : NATURAL := 6310;
    CONSTANT tphl_b_z      : NATURAL := 65;
    CONSTANT tphl_c_z      : NATURAL := 52;
    CONSTANT tplh_a2_z     : NATURAL := 96;
    CONSTANT tphl_a1_z     : NATURAL := 74;
    CONSTANT tplh_c_z      : NATURAL := 57;
    CONSTANT tplh_a1_z     : NATURAL := 104;
    CONSTANT tpls_b_z       : NATURAL := 76;
    CONSTANT tpls_a2_z     : NATURAL := 76;
    CONSTANT transistors   : NATURAL := 8
  );
  PORT (
    b      : in  BIT;
    c      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END aoi211v0x05;

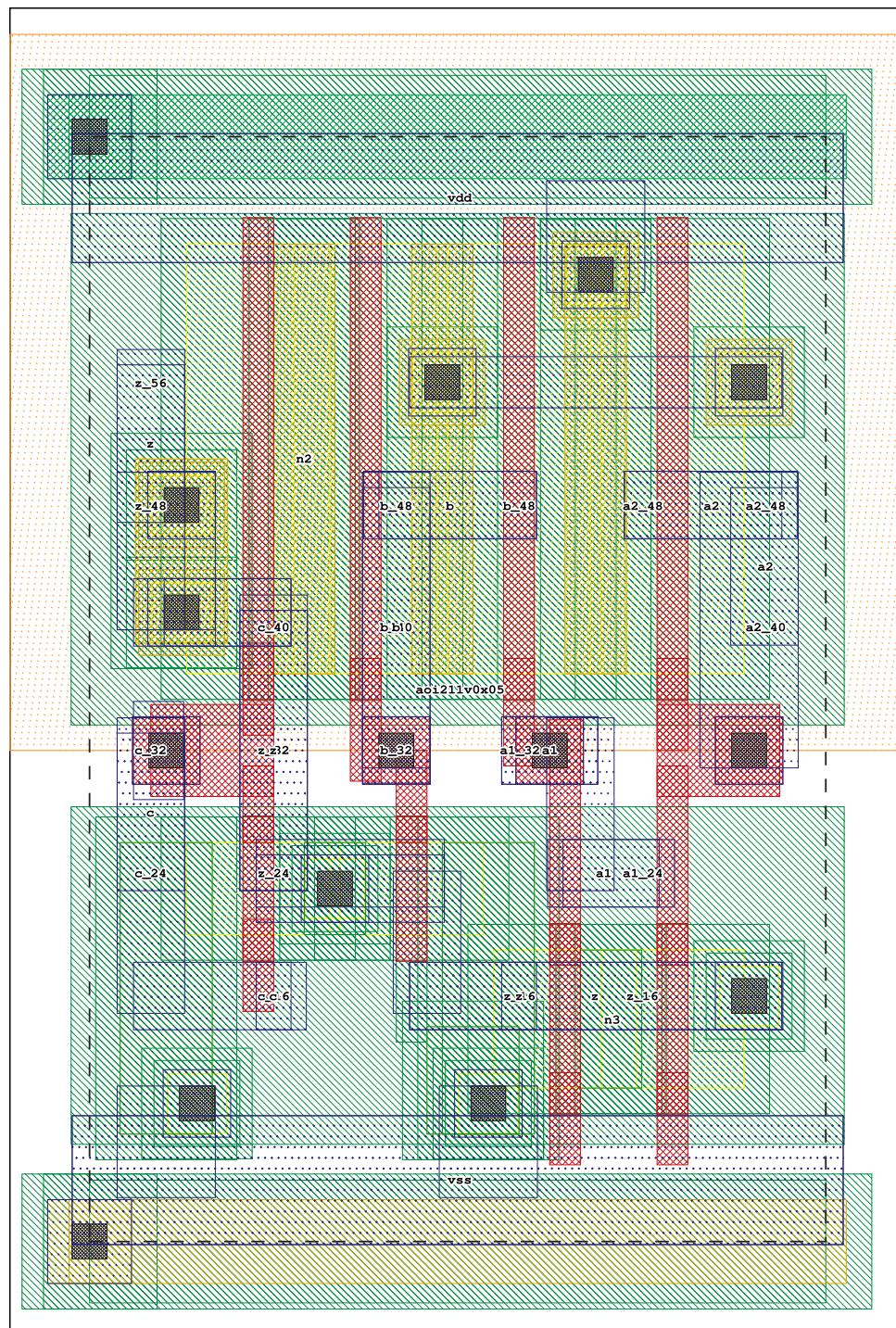
```

ARCHITECTURE behaviour_data_flow OF aoi211v0x05 IS

```

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on aoi211v0x05"
  SEVERITY WARNING;
  z <= not((b or c) or (a1 and a2)) after 203 ps;
END;

```



3.12 aoi211v0x1

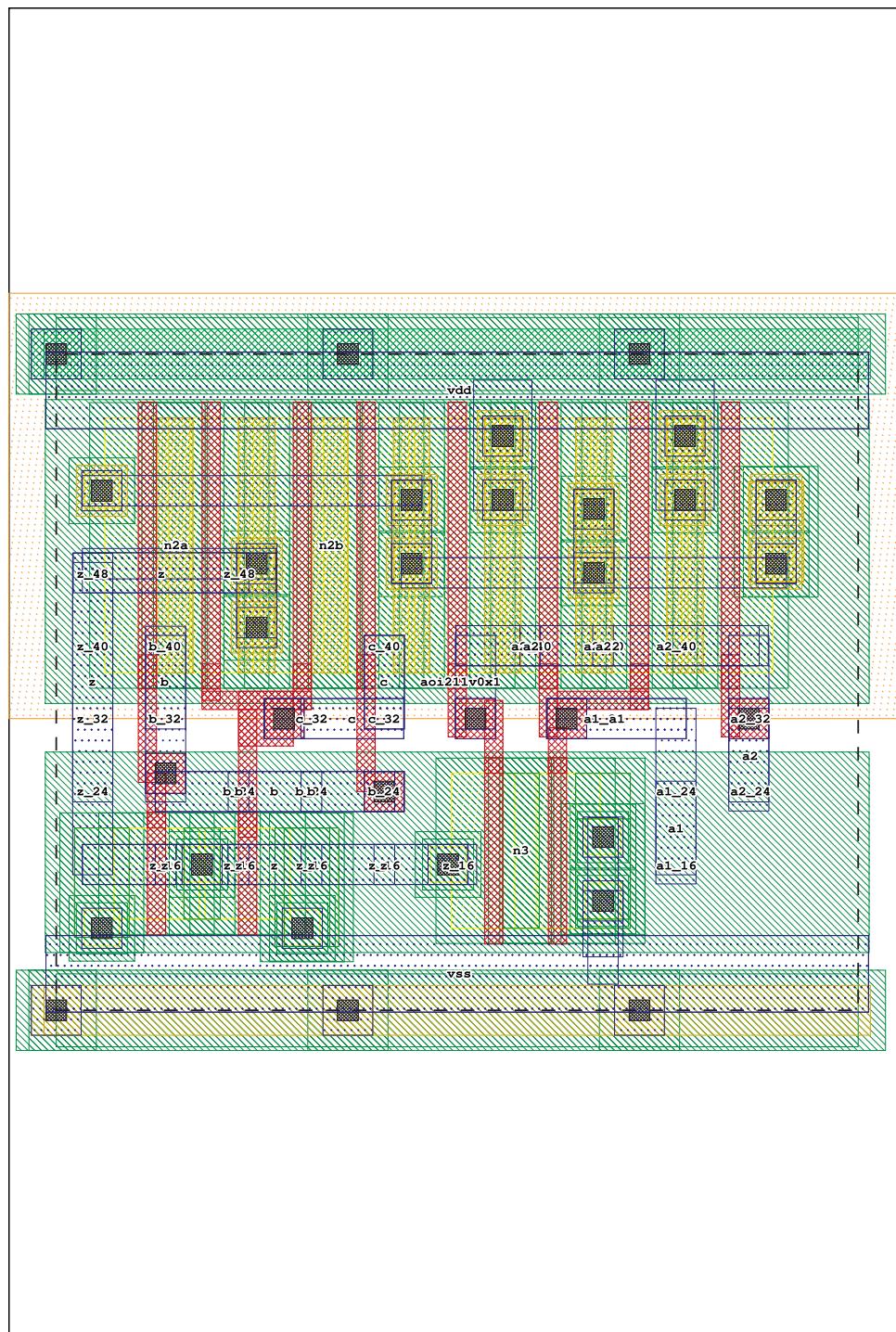
```

ENTITY aoi211v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 6336;
    CONSTANT cin_b         : NATURAL := 8;
    CONSTANT cin_c         : NATURAL := 8;
    CONSTANT cin_a1        : NATURAL := 9;
    CONSTANT cin_a2        : NATURAL := 9;
    CONSTANT rdown_b_z     : NATURAL := 2330;
    CONSTANT rdown_c_z     : NATURAL := 2330;
    CONSTANT rdown_a1_z    : NATURAL := 2320;
    CONSTANT rdown_a2_z    : NATURAL := 2320;
    CONSTANT rup_b_z       : NATURAL := 2960;
    CONSTANT rup_c_z       : NATURAL := 2940;
    CONSTANT rup_a1_z      : NATURAL := 3130;
    CONSTANT rup_a2_z      : NATURAL := 3140;
    CONSTANT tphl_b_z      : NATURAL := 67;
    CONSTANT tphl_c_z      : NATURAL := 50;
    CONSTANT tplh_a2_z     : NATURAL := 88;
    CONSTANT tphl_a1_z     : NATURAL := 71;
    CONSTANT tplh_c_z      : NATURAL := 48;
    CONSTANT tplh_a1_z     : NATURAL := 95;
    CONSTANT tphl_b_z      : NATURAL := 68;
    CONSTANT tphl_a2_z     : NATURAL := 73;
    CONSTANT transistors   : NATURAL := 12
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END aoi211v0x1;

ARCHITECTURE behaviour_data_flow OF aoi211v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi211v0x1"
    SEVERITY WARNING;
    z <= not((b or c) or (a1 and a2)) after 137 ps;
END;

```



3.13 aoi211v0x2

```

ENTITY aoi211v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 12096;
    CONSTANT cin_b         : NATURAL := 15;
    CONSTANT cin_c         : NATURAL := 15;
    CONSTANT cin_a1        : NATURAL := 17;
    CONSTANT cin_a2        : NATURAL := 16;
    CONSTANT rdown_b_z     : NATURAL := 1160;
    CONSTANT rdown_c_z     : NATURAL := 1160;
    CONSTANT rdown_a1_z    : NATURAL := 1160;
    CONSTANT rdown_a2_z    : NATURAL := 1160;
    CONSTANT rup_b_z       : NATURAL := 1480;
    CONSTANT rup_c_z       : NATURAL := 1470;
    CONSTANT rup_a1_z      : NATURAL := 1560;
    CONSTANT rup_a2_z      : NATURAL := 1570;
    CONSTANT tphl_b_z      : NATURAL := 66;
    CONSTANT tphl_c_z      : NATURAL := 50;
    CONSTANT tplh_a2_z     : NATURAL := 85;
    CONSTANT tphl_a1_z     : NATURAL := 70;
    CONSTANT tplh_c_z      : NATURAL := 48;
    CONSTANT tplh_a1_z     : NATURAL := 93;
    CONSTANT tphl_b_z      : NATURAL := 67;
    CONSTANT tphl_a2_z     : NATURAL := 72;
    CONSTANT transistors   : NATURAL := 22
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END aoi211v0x2;

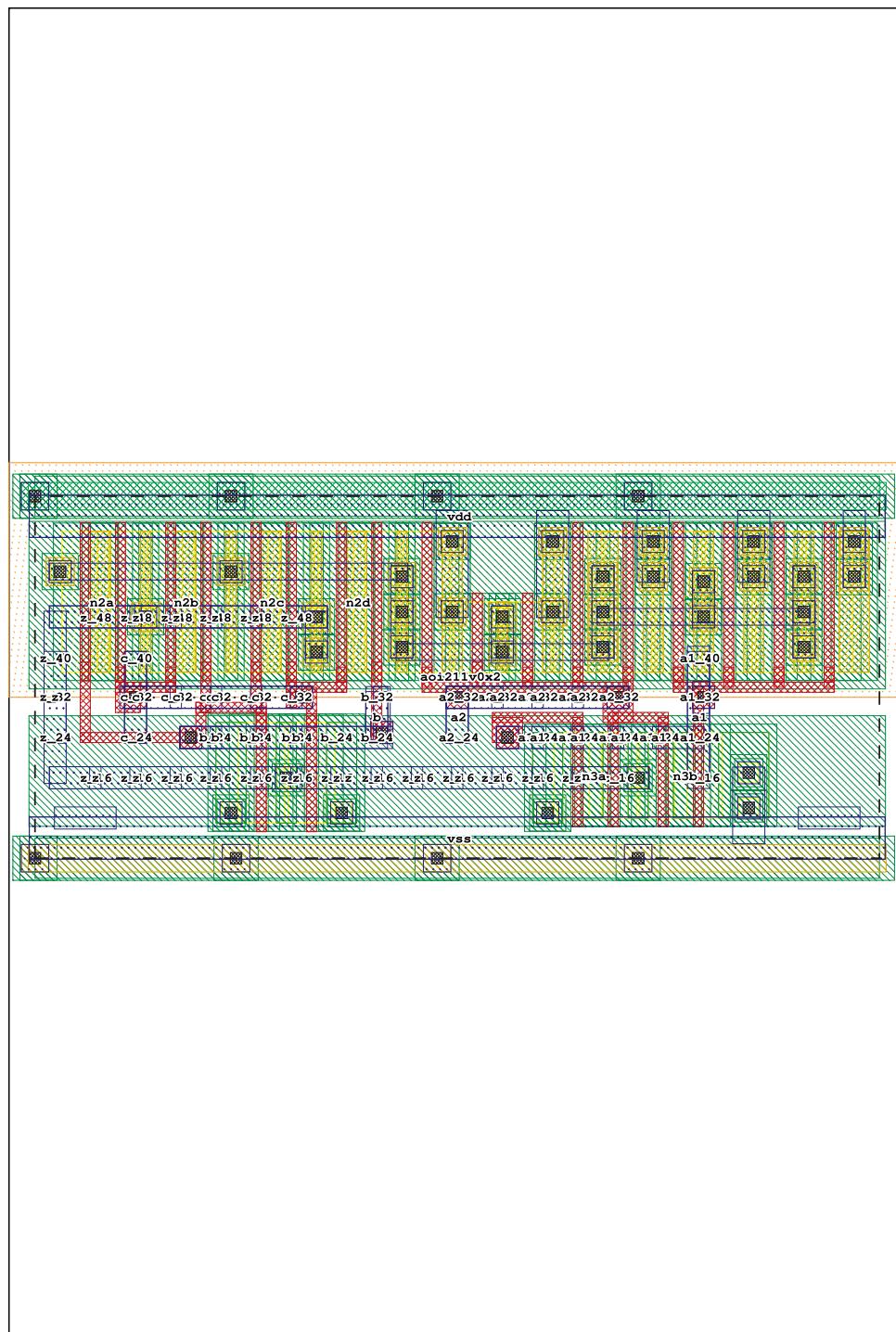
```

ARCHITECTURE behaviour_data_flow OF aoi211v0x2 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi211v0x2"
    SEVERITY WARNING;
    z <= not((b or c) or (a1 and a2)) after 102 ps;
END;

```



3.14 aoi211v5x05

```

ENTITY aoi211v5x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 4;
    CONSTANT cin_a1        : NATURAL := 5;
    CONSTANT cin_a2        : NATURAL := 5;
    CONSTANT rdown_b_z     : NATURAL := 3870;
    CONSTANT rdown_c_z     : NATURAL := 3880;
    CONSTANT rdown_a1_z    : NATURAL := 4370;
    CONSTANT rdown_a2_z    : NATURAL := 4360;
    CONSTANT rup_b_z       : NATURAL := 6120;
    CONSTANT rup_c_z       : NATURAL := 6110;
    CONSTANT rup_a1_z      : NATURAL := 6500;
    CONSTANT rup_a2_z      : NATURAL := 6520;
    CONSTANT tphl_b_z      : NATURAL := 63;
    CONSTANT tphl_c_z      : NATURAL := 52;
    CONSTANT tplh_a2_z     : NATURAL := 97;
    CONSTANT tphl_a1_z     : NATURAL := 73;
    CONSTANT tplh_c_z      : NATURAL := 58;
    CONSTANT tplh_a1_z     : NATURAL := 106;
    CONSTANT tpls_b_z       : NATURAL := 76;
    CONSTANT tpls_a2_z      : NATURAL := 75;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END aoi211v5x05;

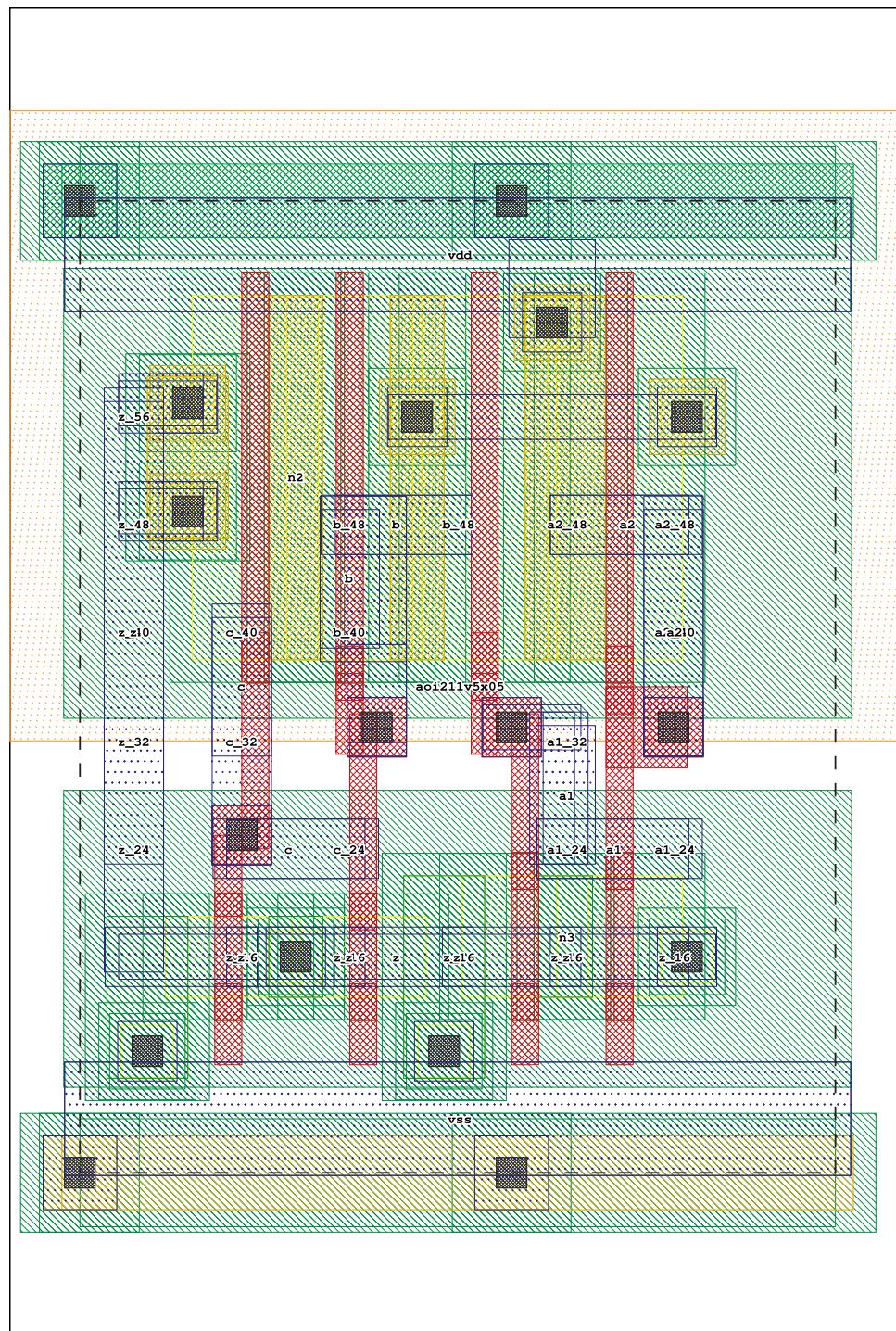
```

ARCHITECTURE behaviour_data_flow OF aoi211v5x05 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi211v5x05"
    SEVERITY WARNING;
    z <= not((b or c) or (a1 and a2)) after 205 ps;
END;

```



3.15 aoi21a2bv0x05

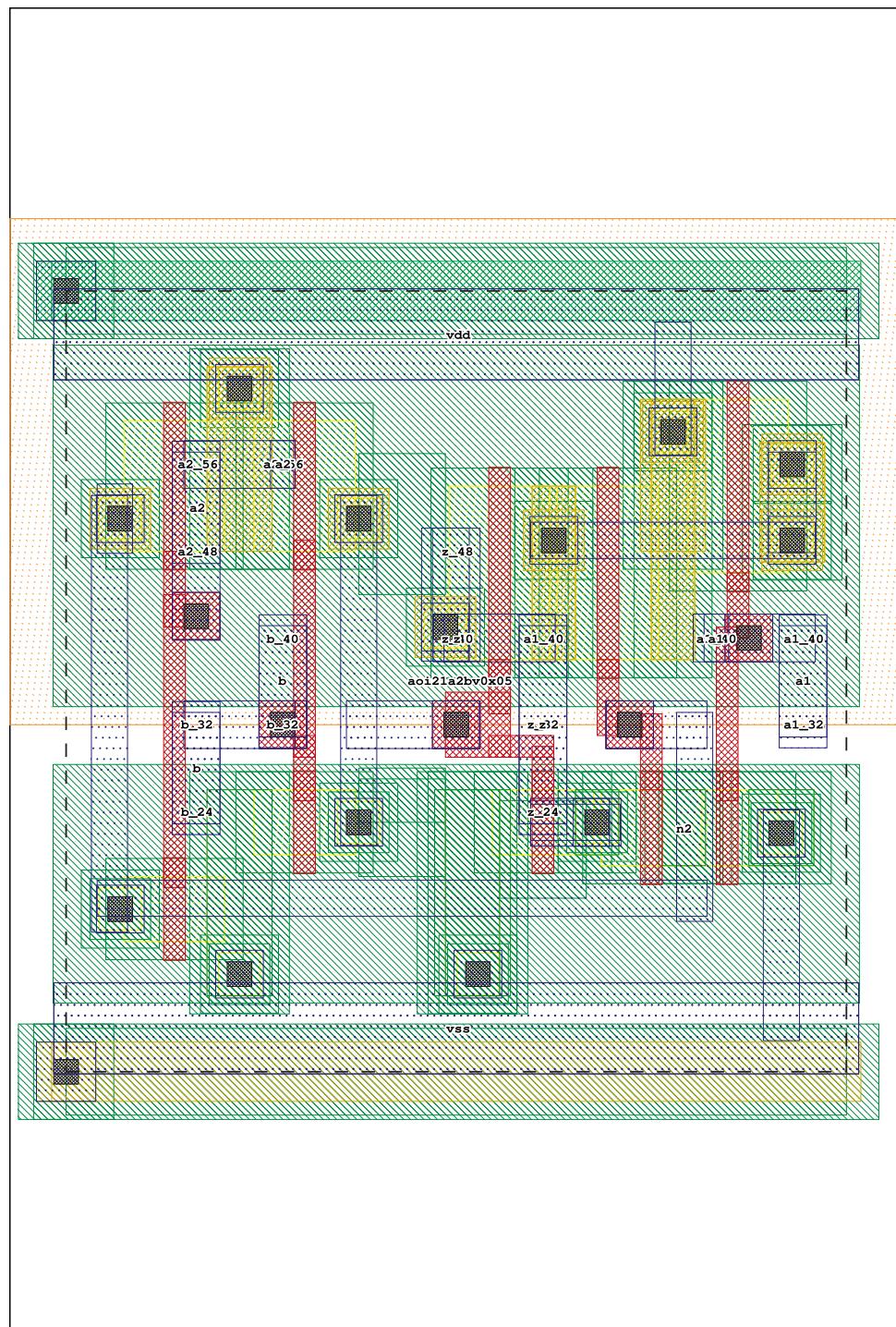
```

ENTITY aoi21a2bv0x05 IS
  GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5400;
    CONSTANT rdown_a2_z     : NATURAL := 5400;
    CONSTANT rdown_b_z      : NATURAL := 3890;
    CONSTANT rup_a1_z       : NATURAL := 7300;
    CONSTANT rup_a2_z       : NATURAL := 7330;
    CONSTANT rup_b_z        : NATURAL := 6690;
    CONSTANT tphl_a1_z      : NATURAL := 58;
    CONSTANT tpll_a2_z      : NATURAL := 110;
    CONSTANT tpll_b_z       : NATURAL := 85;
    CONSTANT tphh_b_z       : NATURAL := 76;
    CONSTANT tphh_a2_z      : NATURAL := 105;
    CONSTANT tplh_a1_z      : NATURAL := 78;
    CONSTANT transistors    : NATURAL := 10
  );
  PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END aoi21a2bv0x05;

ARCHITECTURE behaviour_data_flow OF aoi21a2bv0x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on aoi21a2bv0x05"
  SEVERITY WARNING;
  z <= (not a1 or a2) and b after 235 ps;
END;

```



3.16 aoi21a2bv5x05

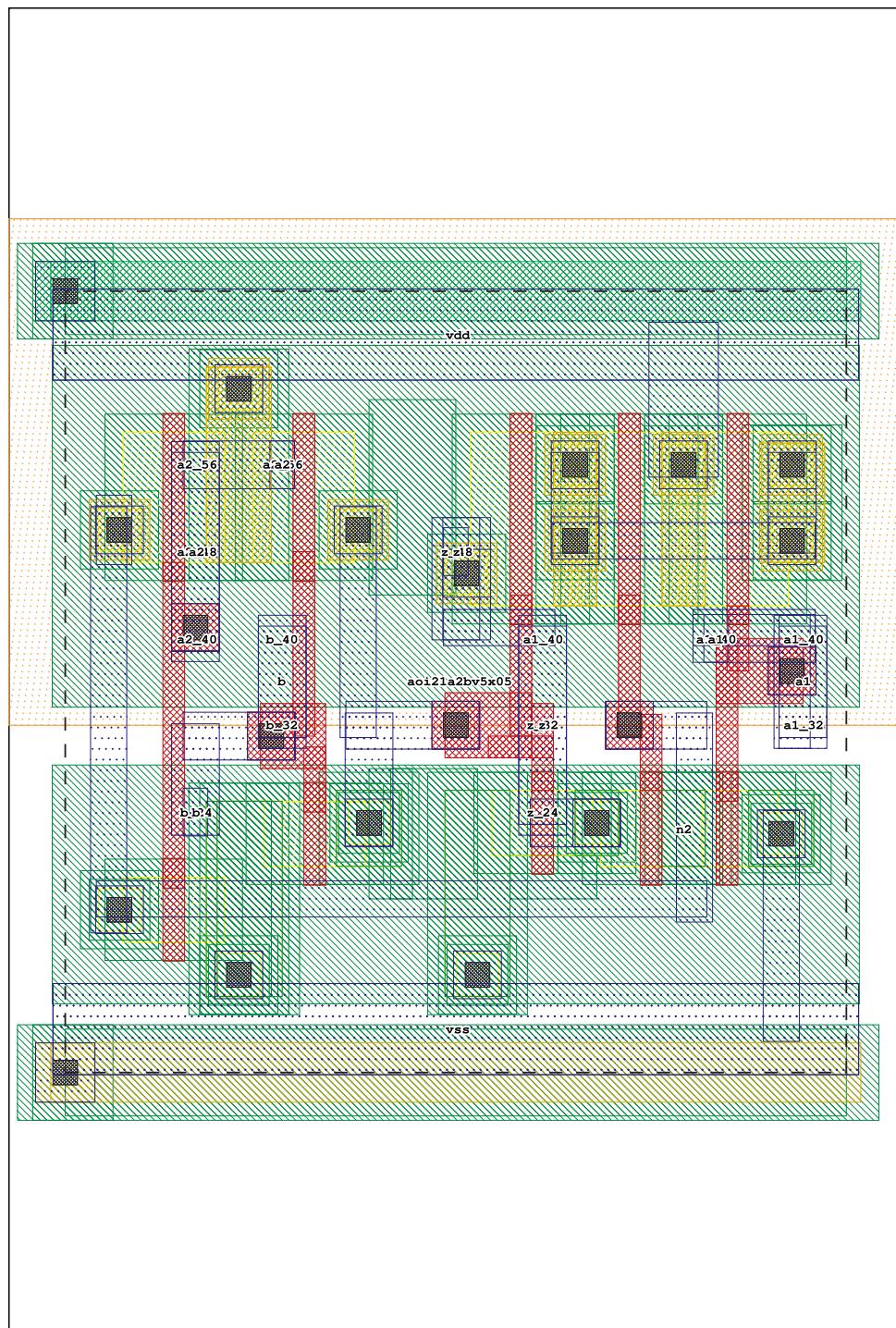
```

ENTITY aoi21a2bv5x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5410;
    CONSTANT rdown_a2_z     : NATURAL := 5400;
    CONSTANT rdown_b_z      : NATURAL := 3900;
    CONSTANT rup_a1_z       : NATURAL := 7300;
    CONSTANT rup_a2_z       : NATURAL := 7330;
    CONSTANT rup_b_z        : NATURAL := 6690;
    CONSTANT tphl_a1_z      : NATURAL := 59;
    CONSTANT tpll_a2_z      : NATURAL := 113;
    CONSTANT tpll_b_z       : NATURAL := 86;
    CONSTANT tphh_b_z       : NATURAL := 78;
    CONSTANT tphh_a2_z      : NATURAL := 108;
    CONSTANT tplh_a1_z      : NATURAL := 79;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aoi21a2bv5x05;

ARCHITECTURE behaviour_data_flow OF aoi21a2bv5x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi21a2bv5x05"
    SEVERITY WARNING;
    z <= (not a1 or a2) and b after 237 ps;
END;

```



3.17 aoi21a2v0x05

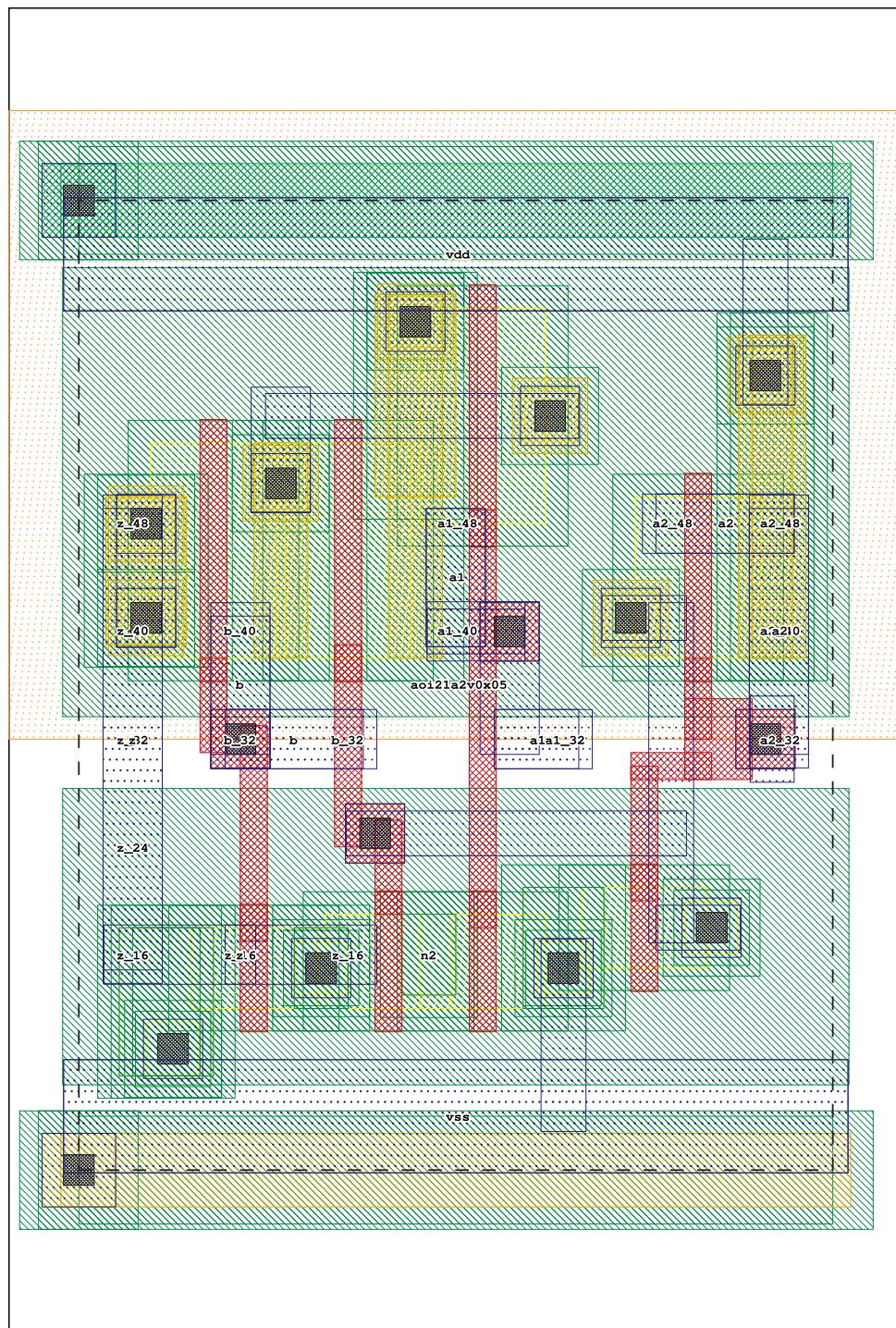
```

ENTITY aoi21a2v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5390;
    CONSTANT rdown_a2_z     : NATURAL := 5380;
    CONSTANT rdown_b_z      : NATURAL := 3880;
    CONSTANT rup_a1_z       : NATURAL := 7290;
    CONSTANT rup_a2_z       : NATURAL := 7310;
    CONSTANT rup_b_z        : NATURAL := 6650;
    CONSTANT tphl_a1_z      : NATURAL := 57;
    CONSTANT tpll_a2_z      : NATURAL := 104;
    CONSTANT tphl_b_z       : NATURAL := 39;
    CONSTANT tplh_b_z       : NATURAL := 48;
    CONSTANT tphh_a2_z      : NATURAL := 98;
    CONSTANT tplh_a1_z      : NATURAL := 74;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aoi21a2v0x05;

ARCHITECTURE behaviour_data_flow OF aoi21a2v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi21a2v0x05"
    SEVERITY WARNING;
    z <= not ((a1 and not a2) or b) after 220 ps;
END;

```



3.18 aoi21bv0x05

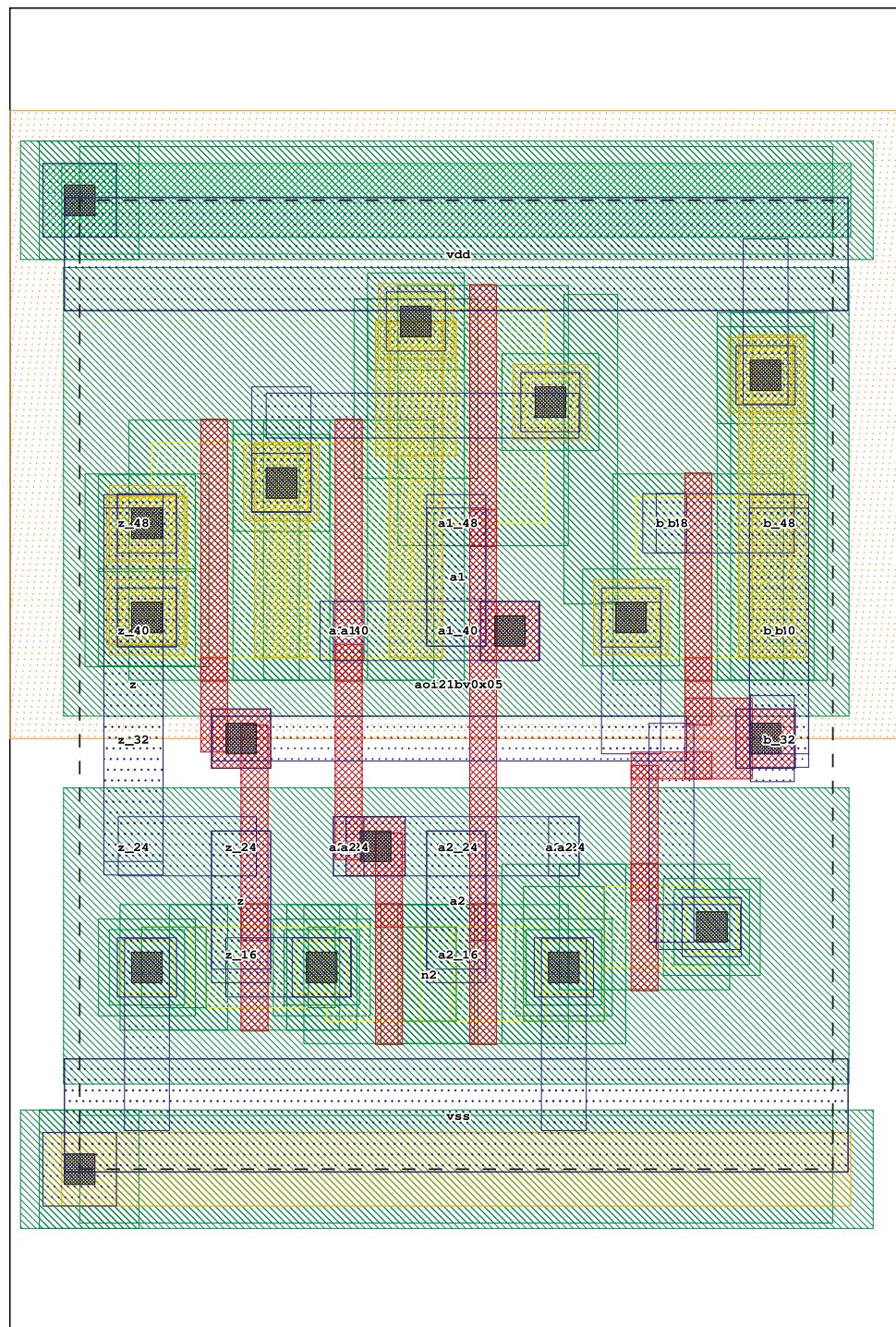
```

ENTITY aoi21bv0x05 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a1         : NATURAL := 4;
    CONSTANT cin_a2         : NATURAL := 4;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5380;
    CONSTANT rdown_a2_z     : NATURAL := 5370;
    CONSTANT rdown_b_z      : NATURAL := 3900;
    CONSTANT rup_a1_z       : NATURAL := 7290;
    CONSTANT rup_a2_z       : NATURAL := 7330;
    CONSTANT rup_b_z        : NATURAL := 6680;
    CONSTANT tphl_a1_z      : NATURAL := 57;
    CONSTANT tphl_a2_z      : NATURAL := 59;
    CONSTANT tpll_b_z       : NATURAL := 88;
    CONSTANT tphh_b_z       : NATURAL := 79;
    CONSTANT tplh_a2_z      : NATURAL := 70;
    CONSTANT tplh_a1_z      : NATURAL := 78;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END aoi21bv0x05;

ARCHITECTURE behaviour_data_flow OF aoi21bv0x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on aoi21bv0x05"
  SEVERITY WARNING;
  z <= not ((a1 and a2) or not b) after 222 ps;
END;

```



3.19 aoi21v0x05

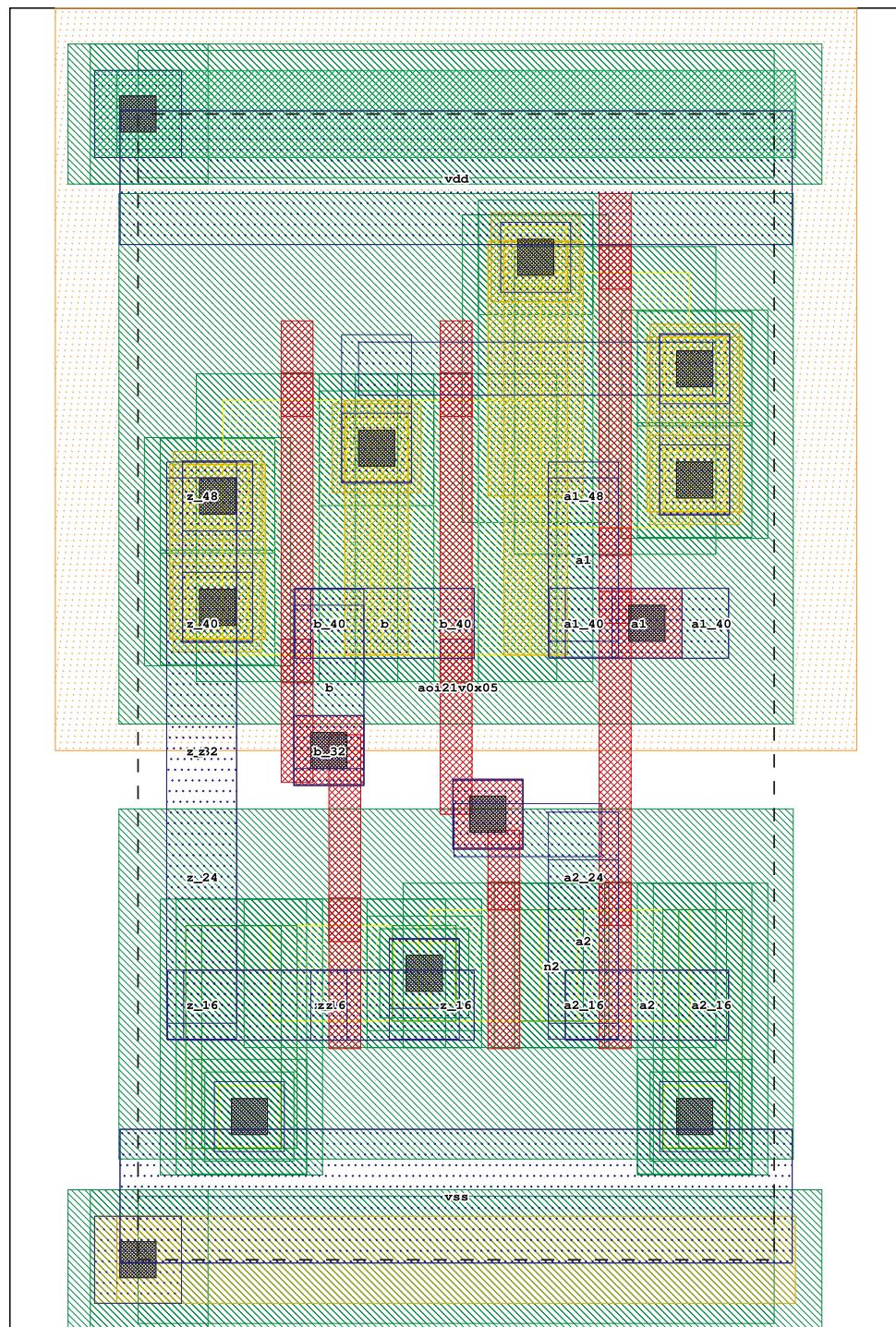
```

ENTITY aoi21v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5380;
    CONSTANT rdown_a2_z     : NATURAL := 5370;
    CONSTANT rdown_b_z      : NATURAL := 3880;
    CONSTANT rup_a1_z       : NATURAL := 7280;
    CONSTANT rup_a2_z       : NATURAL := 7320;
    CONSTANT rup_b_z        : NATURAL := 6640;
    CONSTANT tphl_a1_z      : NATURAL := 57;
    CONSTANT tphl_a2_z      : NATURAL := 58;
    CONSTANT tphl_b_z       : NATURAL := 39;
    CONSTANT tplh_b_z       : NATURAL := 49;
    CONSTANT tplh_a2_z      : NATURAL := 69;
    CONSTANT tplh_a1_z      : NATURAL := 76;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END aoi21v0x05;

ARCHITECTURE behaviour_data_flow OF aoi21v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi21v0x05"
    SEVERITY WARNING;
    z <= not (((a1 and a2) or b)) after 207 ps;
END;

```



3.20 aoi22v0x05

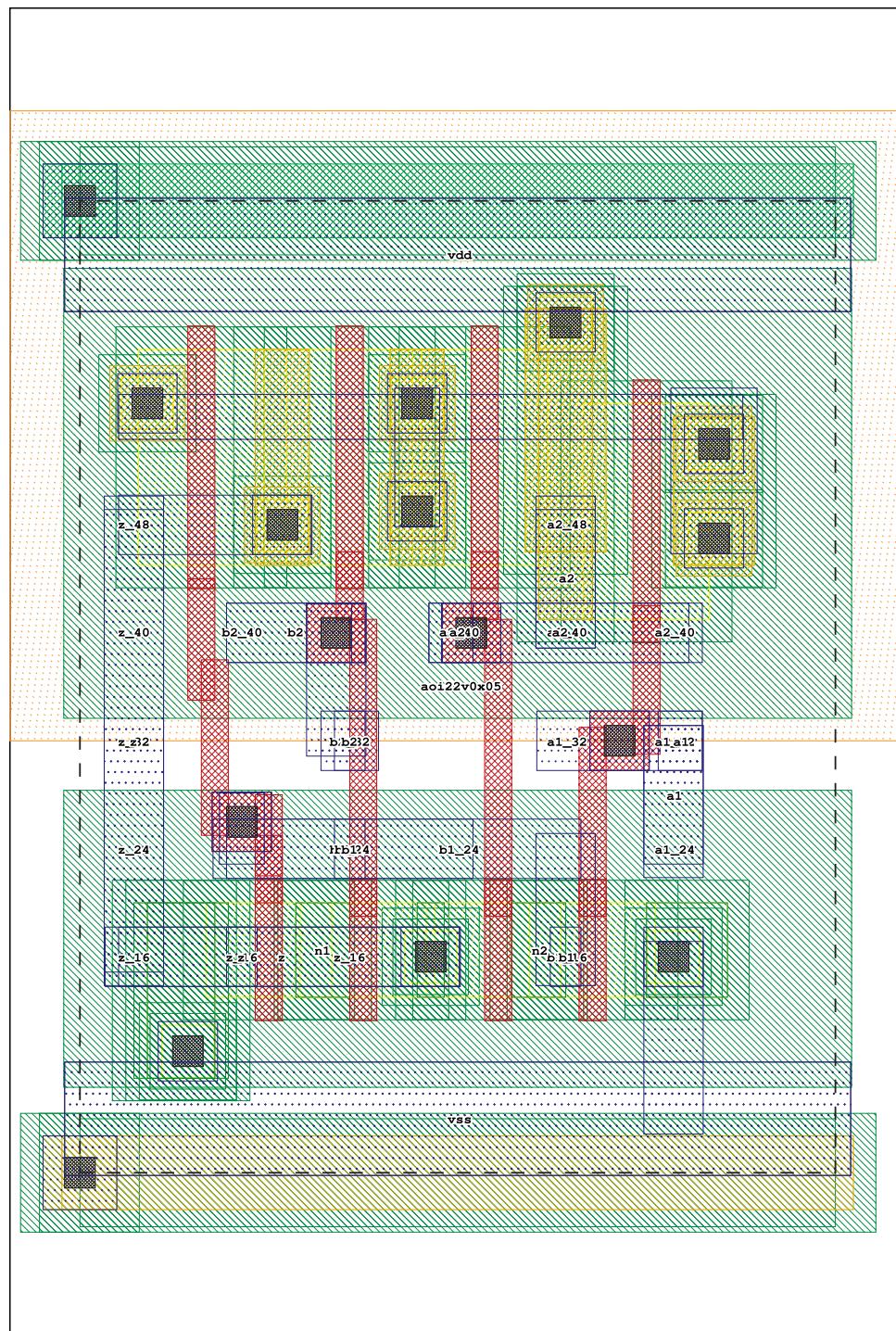
```

ENTITY aoi22v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b1         : NATURAL := 4;
    CONSTANT cin_b2         : NATURAL := 3;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT rdown_b1_z     : NATURAL := 5320;
    CONSTANT rdown_b2_z     : NATURAL := 5290;
    CONSTANT rdown_a1_z     : NATURAL := 5410;
    CONSTANT rdown_a2_z     : NATURAL := 5400;
    CONSTANT rup_b1_z       : NATURAL := 6650;
    CONSTANT rup_b2_z       : NATURAL := 6660;
    CONSTANT rup_a1_z       : NATURAL := 6740;
    CONSTANT rup_a2_z       : NATURAL := 6760;
    CONSTANT tphl_b1_z      : NATURAL := 48;
    CONSTANT tphl_b2_z      : NATURAL := 49;
    CONSTANT tplh_a2_z      : NATURAL := 82;
    CONSTANT tphl_a1_z      : NATURAL := 69;
    CONSTANT tplh_b2_z      : NATURAL := 55;
    CONSTANT tplh_a1_z      : NATURAL := 88;
    CONSTANT tphl_b1_z      : NATURAL := 62;
    CONSTANT tphl_a2_z      : NATURAL := 71;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    b1      : in  BIT;
    b2      : in  BIT;
    a1      : in  BIT;
    a2      : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aoi22v0x05;

ARCHITECTURE behaviour_data_flow OF aoi22v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on aoi22v0x05"
        SEVERITY WARNING;
    z <= not (((b1 and b2) or (a1 and a2))) after 216 ps;
END;

```



3.21 aoi22v0x1

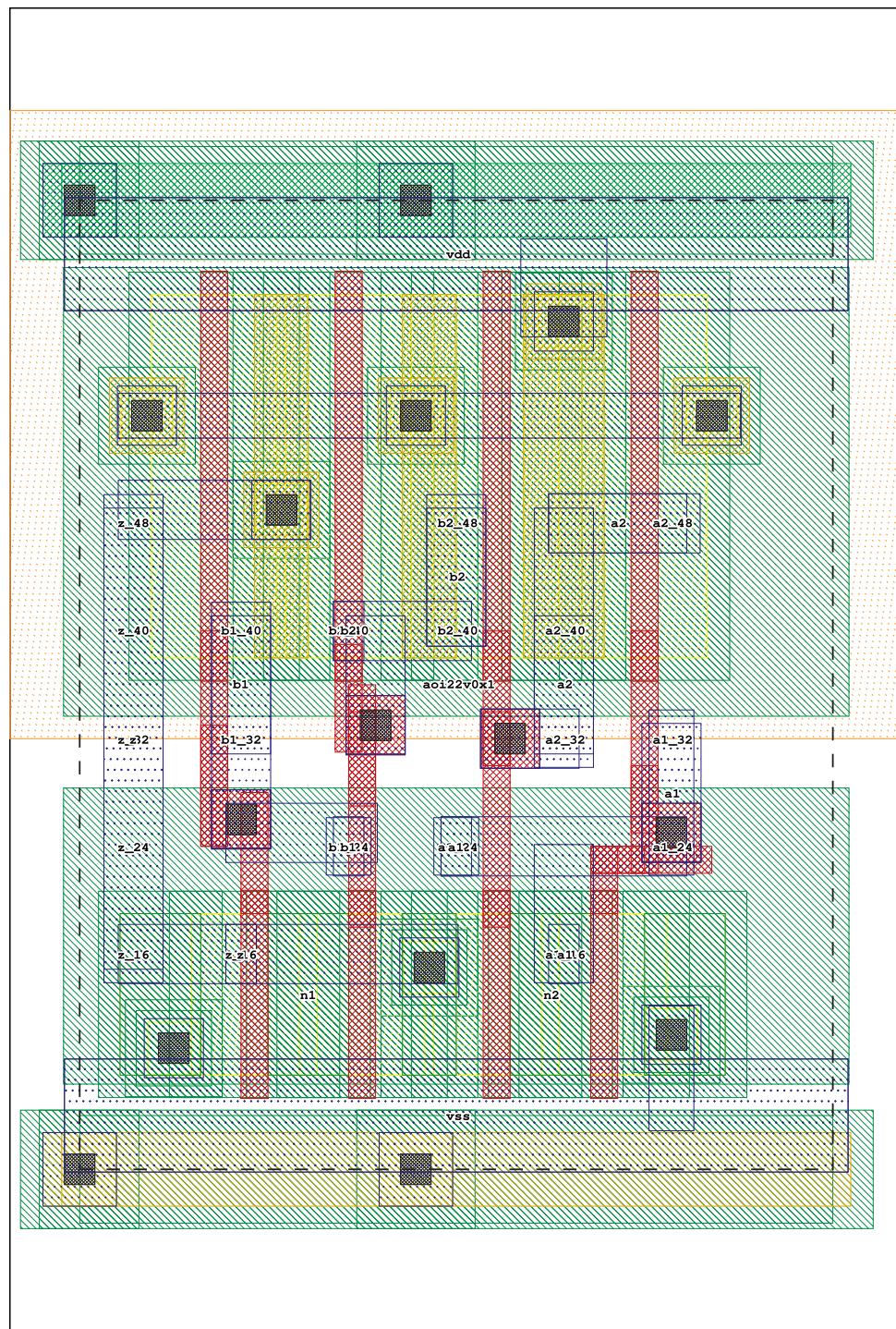
```

ENTITY aoi22v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b1         : NATURAL := 5;
    CONSTANT cin_b2         : NATURAL := 5;
    CONSTANT cin_a1         : NATURAL := 5;
    CONSTANT cin_a2         : NATURAL := 5;
    CONSTANT rdown_b1_z     : NATURAL := 3110;
    CONSTANT rdown_b2_z     : NATURAL := 3090;
    CONSTANT rdown_a1_z     : NATURAL := 3150;
    CONSTANT rdown_a2_z     : NATURAL := 3150;
    CONSTANT rup_b1_z       : NATURAL := 3940;
    CONSTANT rup_b2_z       : NATURAL := 3940;
    CONSTANT rup_a1_z       : NATURAL := 4000;
    CONSTANT rup_a2_z       : NATURAL := 4010;
    CONSTANT tphl_b1_z      : NATURAL := 45;
    CONSTANT tphl_b2_z      : NATURAL := 46;
    CONSTANT tplh_a2_z      : NATURAL := 77;
    CONSTANT tphl_a1_z      : NATURAL := 65;
    CONSTANT tplh_b2_z      : NATURAL := 52;
    CONSTANT tplh_a1_z      : NATURAL := 84;
    CONSTANT tplh_b1_z      : NATURAL := 59;
    CONSTANT tphl_a2_z      : NATURAL := 66;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    b1      : in  BIT;
    b2      : in  BIT;
    a1      : in  BIT;
    a2      : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aoi22v0x1;

ARCHITECTURE behaviour_data_flow OF aoi22v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on aoi22v0x1"
        SEVERITY WARNING;
    z <= not (((b1 and b2) or (a1 and a2))) after 150 ps;
END;

```



3.22 aoi22v5x05

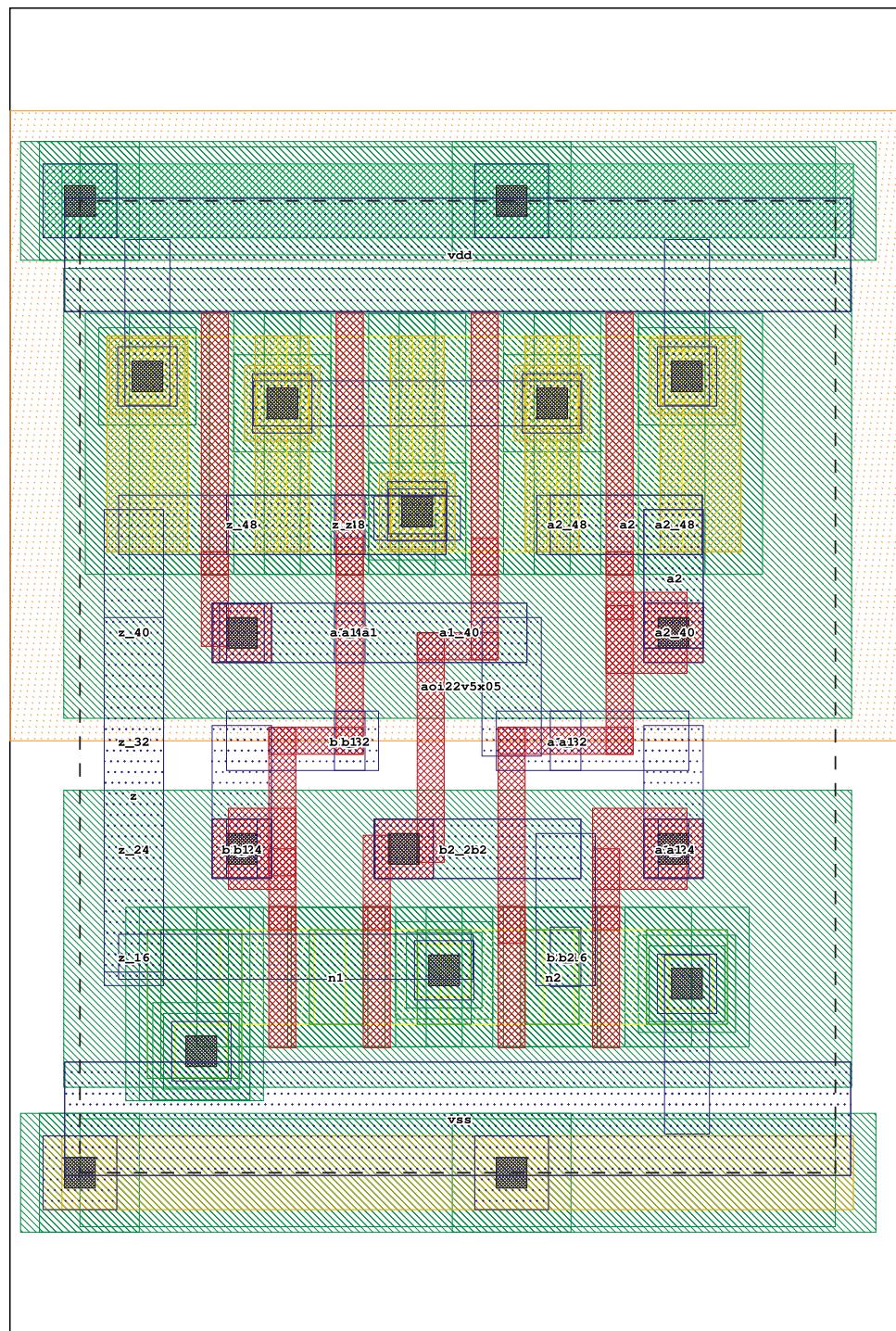
```

ENTITY aoi22v5x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b1         : NATURAL := 4;
    CONSTANT cin_b2         : NATURAL := 3;
    CONSTANT cin_a1         : NATURAL := 4;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT rdown_b1_z     : NATURAL := 5310;
    CONSTANT rdown_b2_z     : NATURAL := 5290;
    CONSTANT rdown_a1_z     : NATURAL := 5380;
    CONSTANT rdown_a2_z     : NATURAL := 5360;
    CONSTANT rup_b1_z       : NATURAL := 6640;
    CONSTANT rup_b2_z       : NATURAL := 6650;
    CONSTANT rup_a1_z       : NATURAL := 6750;
    CONSTANT rup_a2_z       : NATURAL := 6760;
    CONSTANT tphl_b1_z      : NATURAL := 49;
    CONSTANT tphl_b2_z      : NATURAL := 50;
    CONSTANT tplh_a2_z      : NATURAL := 78;
    CONSTANT tphl_a1_z      : NATURAL := 69;
    CONSTANT tplh_b2_z      : NATURAL := 56;
    CONSTANT tplh_a1_z      : NATURAL := 87;
    CONSTANT tplh_b1_z      : NATURAL := 63;
    CONSTANT tphl_a2_z      : NATURAL := 68;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    b1      : in  BIT;
    b2      : in  BIT;
    a1      : in  BIT;
    a2      : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aoi22v5x05;

ARCHITECTURE behaviour_data_flow OF aoi22v5x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on aoi22v5x05"
        SEVERITY WARNING;
    z <= not (((b1 and b2) or (a1 and a2))) after 215 ps;
END;

```



3.23 aoi31v0x05

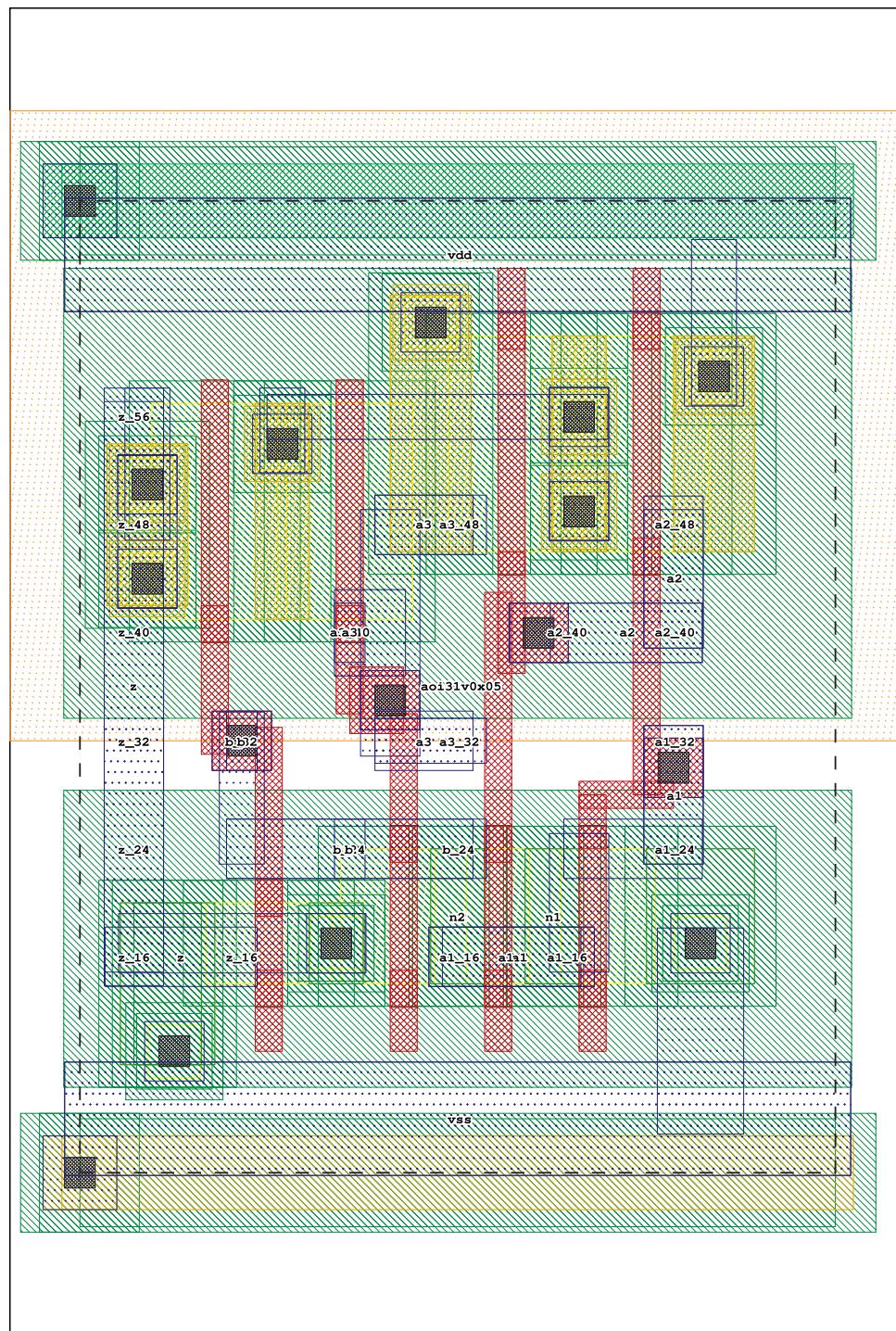
```

ENTITY aoi31v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT cin_a1        : NATURAL := 4;
    CONSTANT cin_a2        : NATURAL := 4;
    CONSTANT cin_a3        : NATURAL := 4;
    CONSTANT rdown_b_z     : NATURAL := 3890;
    CONSTANT rdown_a1_z    : NATURAL := 5240;
    CONSTANT rdown_a2_z    : NATURAL := 5230;
    CONSTANT rdown_a3_z    : NATURAL := 5230;
    CONSTANT rup_b_z       : NATURAL := 6120;
    CONSTANT rup_a1_z      : NATURAL := 7320;
    CONSTANT rup_a2_z      : NATURAL := 7320;
    CONSTANT rup_a3_z      : NATURAL := 7350;
    CONSTANT tphl_b_z      : NATURAL := 41;
    CONSTANT tphl_a1_z     : NATURAL := 62;
    CONSTANT tphl_a3_z     : NATURAL := 75;
    CONSTANT tphl_a2_z     : NATURAL := 60;
    CONSTANT tplh_a1_z     : NATURAL := 94;
    CONSTANT tplh_a2_z     : NATURAL := 85;
    CONSTANT tplh_b_z      : NATURAL := 53;
    CONSTANT tphl_a3_z     : NATURAL := 58;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    b      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    a3     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END aoi31v0x05;

ARCHITECTURE behaviour_data_flow OF aoi31v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aoi31v0x05"
    SEVERITY WARNING;
    z <= not(b or ((a1 and a2) and a3)) after 215 ps;
END;

```



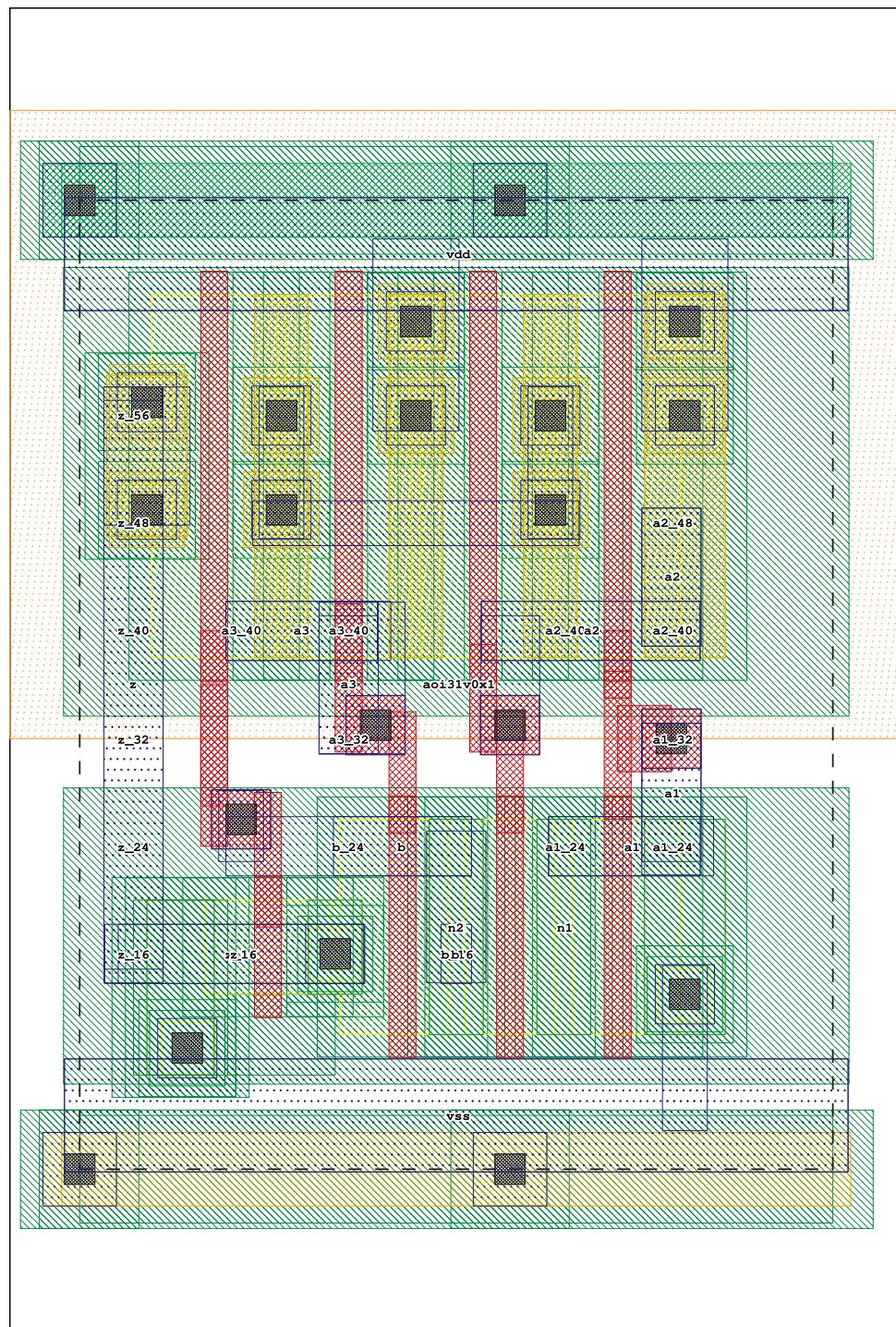
3.24 aoi31v0x1

```

ENTITY aoi31v0x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b          : NATURAL := 5;
    CONSTANT cin_a1         : NATURAL := 5;
    CONSTANT cin_a2         : NATURAL := 5;
    CONSTANT cin_a3         : NATURAL := 5;
    CONSTANT rdown_b_z      : NATURAL := 3310;
    CONSTANT rdown_a1_z     : NATURAL := 3270;
    CONSTANT rdown_a2_z     : NATURAL := 3270;
    CONSTANT rdown_a3_z     : NATURAL := 3270;
    CONSTANT rup_b_z        : NATURAL := 3630;
    CONSTANT rup_a1_z       : NATURAL := 4340;
    CONSTANT rup_a2_z       : NATURAL := 4340;
    CONSTANT rup_a3_z       : NATURAL := 4360;
    CONSTANT tphl_b_z       : NATURAL := 47;
    CONSTANT tphl_a1_z      : NATURAL := 60;
    CONSTANT tphl_a3_z      : NATURAL := 70;
    CONSTANT tphl_a2_z      : NATURAL := 60;
    CONSTANT tplh_a1_z      : NATURAL := 88;
    CONSTANT tplh_a2_z      : NATURAL := 80;
    CONSTANT tplh_b_z       : NATURAL := 49;
    CONSTANT tphl_a3_z      : NATURAL := 57;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    b      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    a3     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END aoi31v0x1;

ARCHITECTURE behaviour_data_flow OF aoi31v0x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on aoi31v0x1"
  SEVERITY WARNING;
  z <= not(b or ((a1 and a2) and a3)) after 157 ps;
END;

```



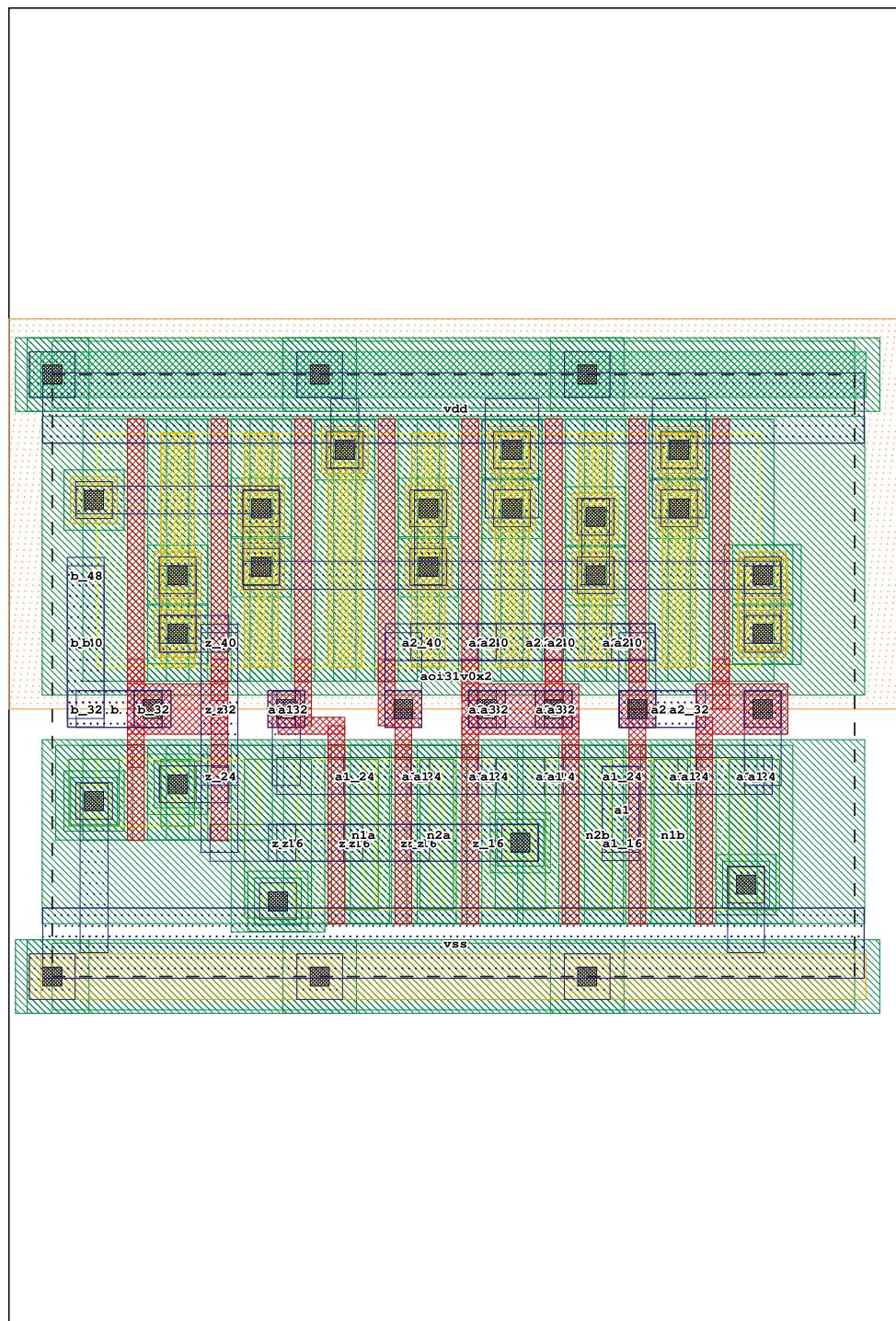
3.25 aoi31v0x2

```

ENTITY aoi31v0x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 6912;
    CONSTANT cin_b          : NATURAL := 8;
    CONSTANT cin_a1         : NATURAL := 12;
    CONSTANT cin_a2         : NATURAL := 11;
    CONSTANT cin_a3         : NATURAL := 10;
    CONSTANT rdown_b_z      : NATURAL := 1450;
    CONSTANT rdown_a1_z     : NATURAL := 1470;
    CONSTANT rdown_a2_z     : NATURAL := 1460;
    CONSTANT rdown_a3_z     : NATURAL := 1460;
    CONSTANT rup_b_z        : NATURAL := 1750;
    CONSTANT rup_a1_z       : NATURAL := 2100;
    CONSTANT rup_a2_z       : NATURAL := 2090;
    CONSTANT rup_a3_z       : NATURAL := 2110;
    CONSTANT tphl_b_z       : NATURAL := 42;
    CONSTANT tphl_a1_z      : NATURAL := 57;
    CONSTANT tphl_a3_z      : NATURAL := 69;
    CONSTANT tphl_a2_z      : NATURAL := 55;
    CONSTANT tplh_a1_z      : NATURAL := 90;
    CONSTANT tplh_a2_z      : NATURAL := 80;
    CONSTANT tplh_b_z       : NATURAL := 47;
    CONSTANT tphl_a3_z      : NATURAL := 52;
    CONSTANT transistors    : NATURAL := 16
  );
  PORT (
    b      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    a3     : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
  );
END aoi31v0x2;

ARCHITECTURE behaviour_data_flow OF aoi31v0x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on aoi31v0x2"
  SEVERITY WARNING;
  z <= not(b or ((a1 and a2) and a3)) after 105 ps;
END;

```



3.26 aon21bv0x05

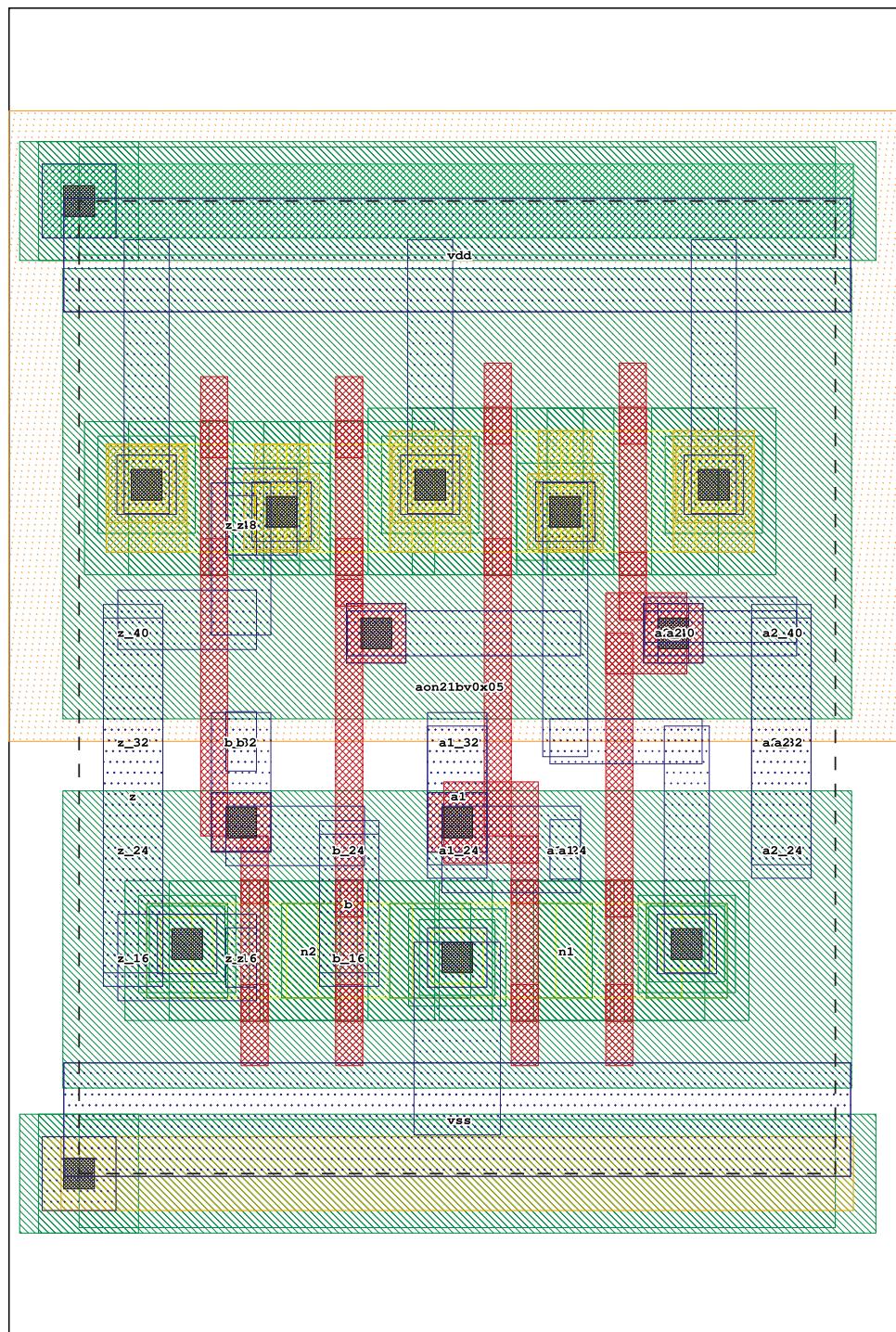
```

ENTITY aon21bv0x05 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a2_z     : NATURAL := 5280;
    CONSTANT rdown_a1_z     : NATURAL := 5290;
    CONSTANT rdown_b_z      : NATURAL := 5290;
    CONSTANT rup_a2_z       : NATURAL := 7430;
    CONSTANT rup_a1_z       : NATURAL := 7430;
    CONSTANT rup_b_z        : NATURAL := 7430;
    CONSTANT tphh_a2_z      : NATURAL := 91;
    CONSTANT tphl_b_z       : NATURAL := 38;
    CONSTANT tplh_b_z       : NATURAL := 50;
    CONSTANT tphh_a1_z      : NATURAL := 91;
    CONSTANT tpll_a1_z      : NATURAL := 100;
    CONSTANT tpll_a2_z      : NATURAL := 92;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    a2      : in  BIT;
    a1      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END aon21bv0x05;

ARCHITECTURE behaviour_data_flow OF aon21bv0x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on aon21bv0x05"
  SEVERITY WARNING;
  z <= not b or (a1 and a2) after 236 ps;
END;

```



3.27 aon21bv0x1

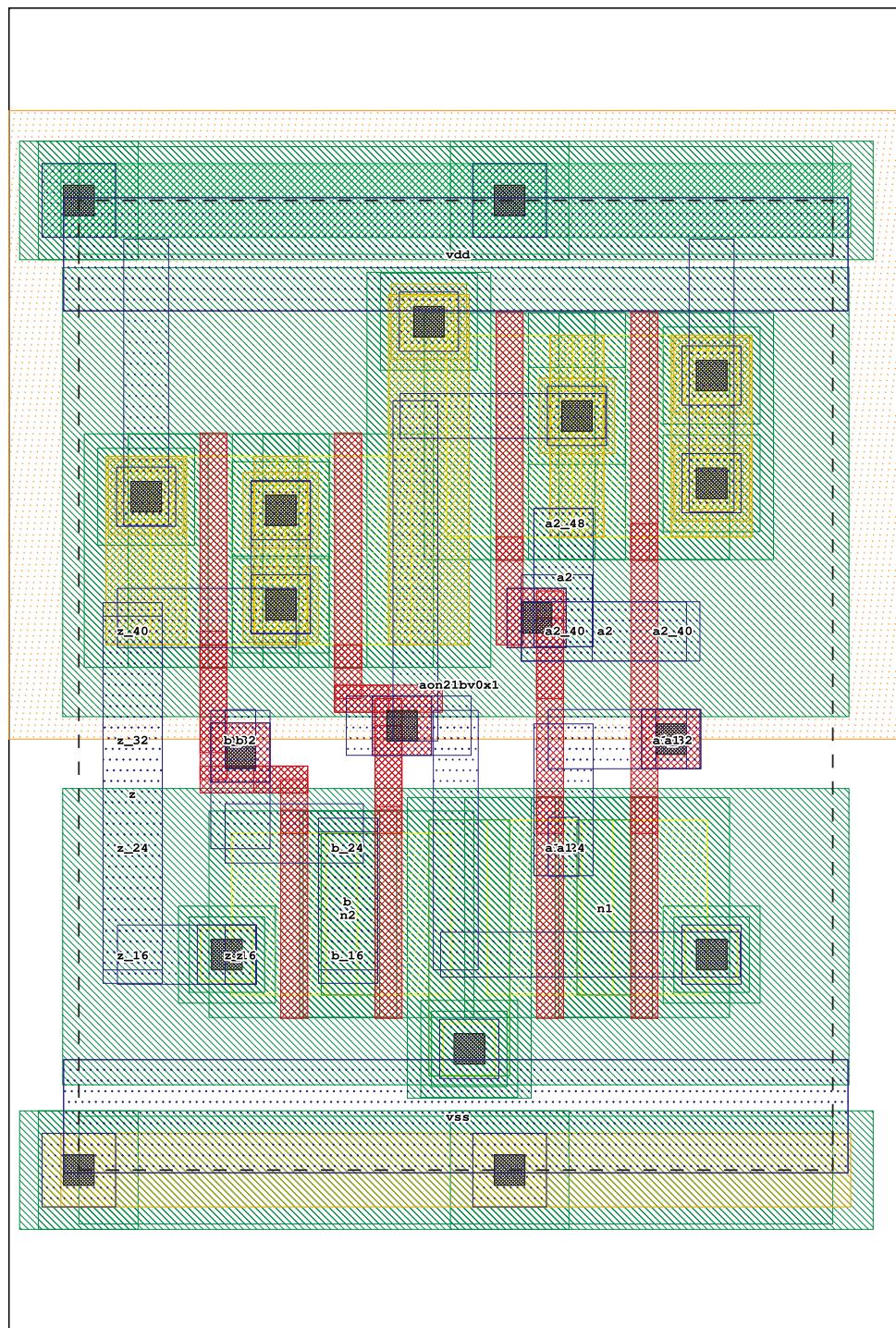
```

ENTITY aon21bv0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a2         : NATURAL := 4;
    CONSTANT cin_a1         : NATURAL := 4;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT rdown_a2_z     : NATURAL := 3090;
    CONSTANT rdown_a1_z     : NATURAL := 3080;
    CONSTANT rdown_b_z      : NATURAL := 3100;
    CONSTANT rup_a2_z       : NATURAL := 4250;
    CONSTANT rup_a1_z       : NATURAL := 4250;
    CONSTANT rup_b_z        : NATURAL := 4240;
    CONSTANT tphh_a2_z      : NATURAL := 79;
    CONSTANT tphl_b_z       : NATURAL := 35;
    CONSTANT tplh_b_z       : NATURAL := 46;
    CONSTANT tphh_a1_z      : NATURAL := 80;
    CONSTANT tpll_a1_z      : NATURAL := 86;
    CONSTANT tpll_a2_z      : NATURAL := 95;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a2      : in  BIT;
    a1      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aon21bv0x1;

ARCHITECTURE behaviour_data_flow OF aon21bv0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aon21bv0x1"
    SEVERITY WARNING;
    z <= not b or (a1 and a2) after 162 ps;
END;

```



3.28 aon21bv0x2

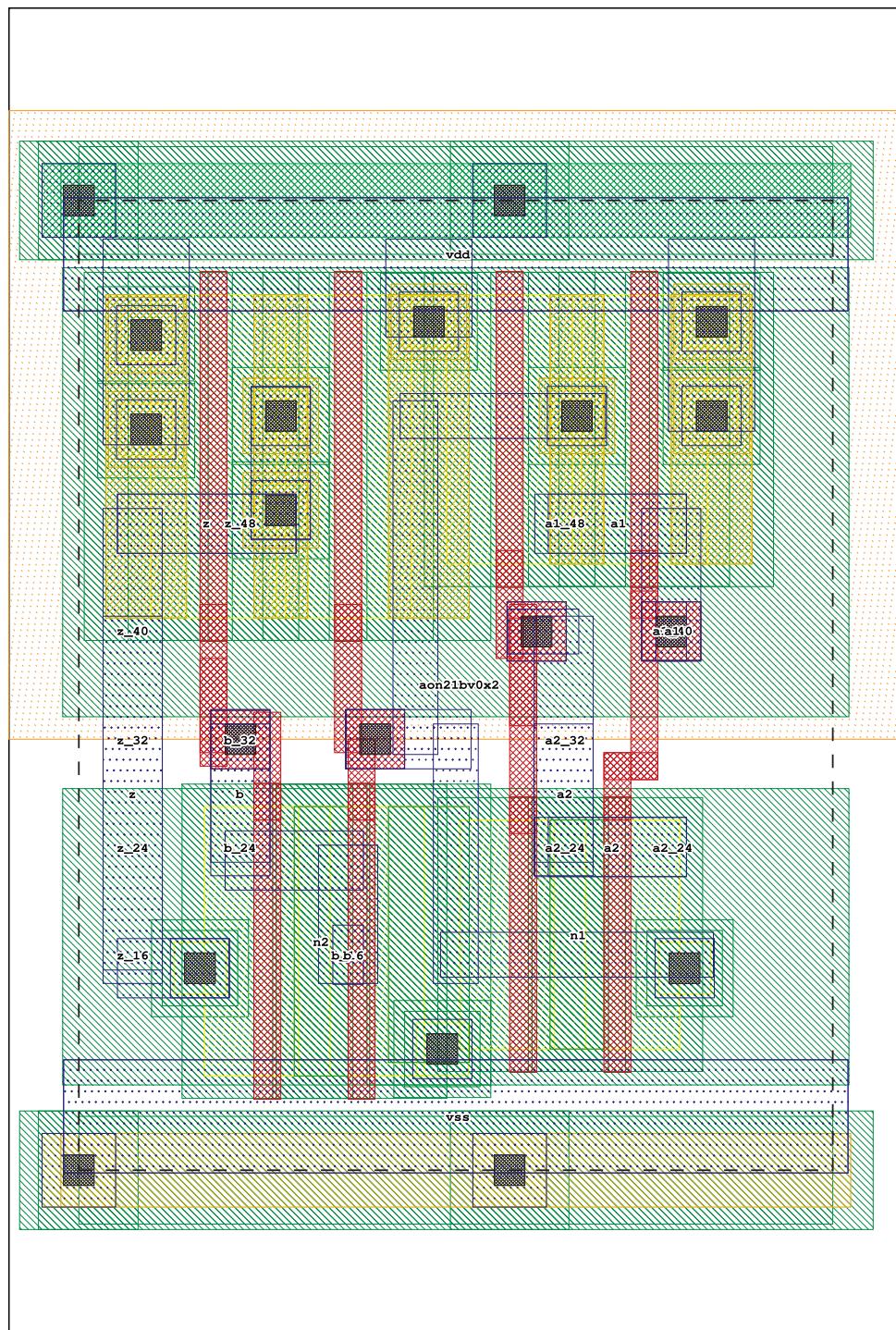
```

ENTITY aon21bv0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a2         : NATURAL := 5;
    CONSTANT cin_a1         : NATURAL := 5;
    CONSTANT cin_b          : NATURAL := 6;
    CONSTANT rdown_a2_z     : NATURAL := 1850;
    CONSTANT rdown_a1_z     : NATURAL := 1850;
    CONSTANT rdown_b_z      : NATURAL := 1850;
    CONSTANT rup_a2_z       : NATURAL := 2470;
    CONSTANT rup_a1_z       : NATURAL := 2470;
    CONSTANT rup_b_z        : NATURAL := 2470;
    CONSTANT tphh_a2_z      : NATURAL := 80;
    CONSTANT tphl_b_z       : NATURAL := 34;
    CONSTANT tplh_b_z       : NATURAL := 44;
    CONSTANT tphh_a1_z      : NATURAL := 80;
    CONSTANT tpll_a1_z      : NATURAL := 87;
    CONSTANT tpll_a2_z      : NATURAL := 96;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a2      : in  BIT;
    a1      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aon21bv0x2;

ARCHITECTURE behaviour_data_flow OF aon21bv0x2 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aon21bv0x2"
    SEVERITY WARNING;
    z <= not b or (a1 and a2) after 124 ps;
END;

```



3.29 aon21v0x05

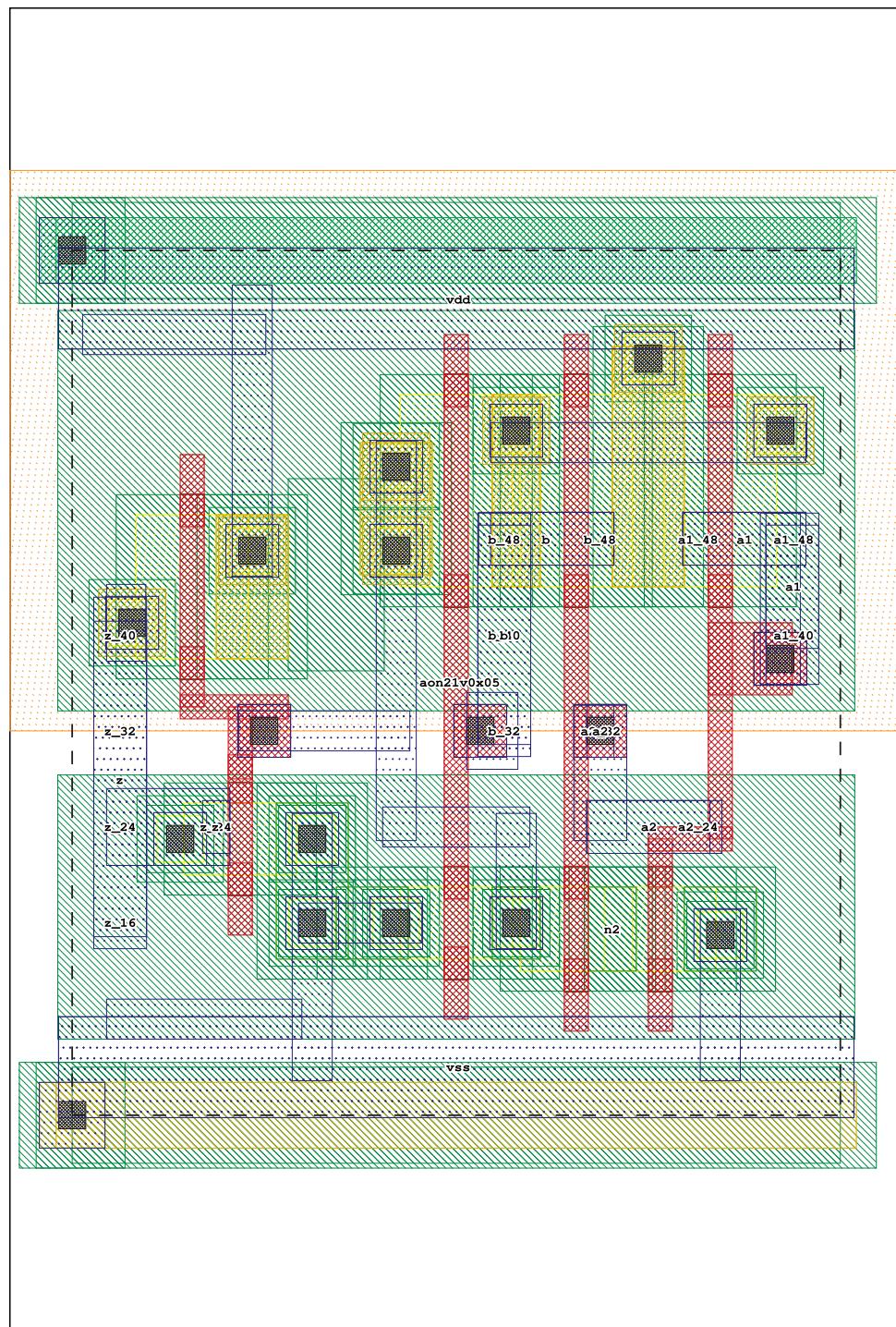
```

ENTITY aon21v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT rdown_a1_z     : NATURAL := 4090;
    CONSTANT rdown_a2_z     : NATURAL := 4060;
    CONSTANT rdown_b_z      : NATURAL := 4030;
    CONSTANT rup_a1_z       : NATURAL := 5090;
    CONSTANT rup_a2_z       : NATURAL := 5090;
    CONSTANT rup_b_z        : NATURAL := 4970;
    CONSTANT tphh_a1_z      : NATURAL := 101;
    CONSTANT tphh_b_z       : NATURAL := 72;
    CONSTANT tpll_b_z       : NATURAL := 95;
    CONSTANT tphh_a2_z      : NATURAL := 102;
    CONSTANT tpll_a2_z      : NATURAL := 116;
    CONSTANT tpll_a1_z      : NATURAL := 125;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END aon21v0x05;

ARCHITECTURE behaviour_data_flow OF aon21v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on aon21v0x05"
    SEVERITY WARNING;
    z <= (a1 and a2) or b after 216 ps;
END;

```



3.30 bf1v0x05

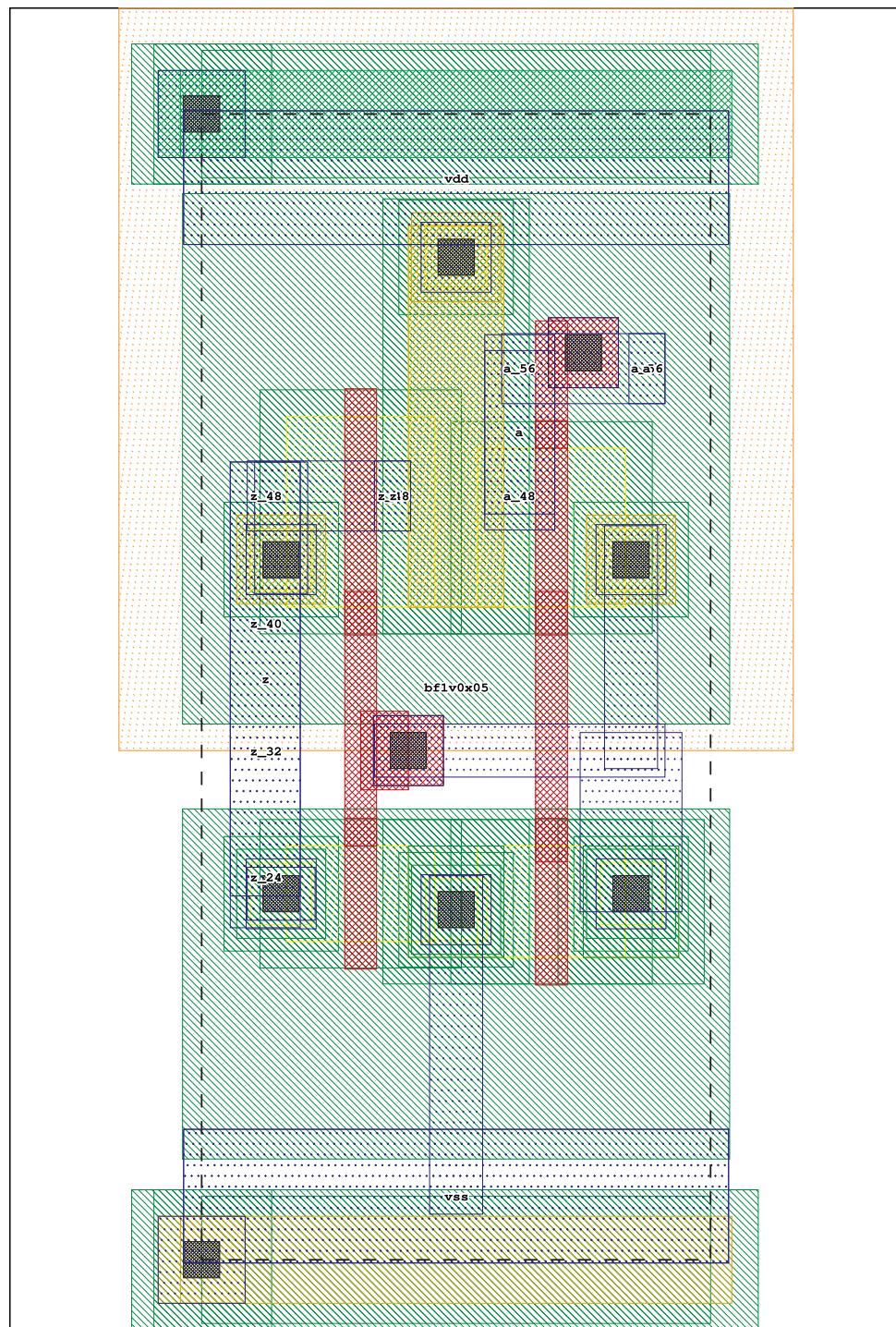
```

ENTITY bf1v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 3830;
    CONSTANT rup_a_z       : NATURAL := 4940;
    CONSTANT tp11_a_z      : NATURAL := 78;
    CONSTANT tphh_a_z      : NATURAL := 54;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END bf1v0x05;

ARCHITECTURE behaviour_data_flow OF bf1v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on bf1v0x05"
        SEVERITY WARNING;
    z <= a after 176 ps;
END;

```



3.31 bf1v0x12

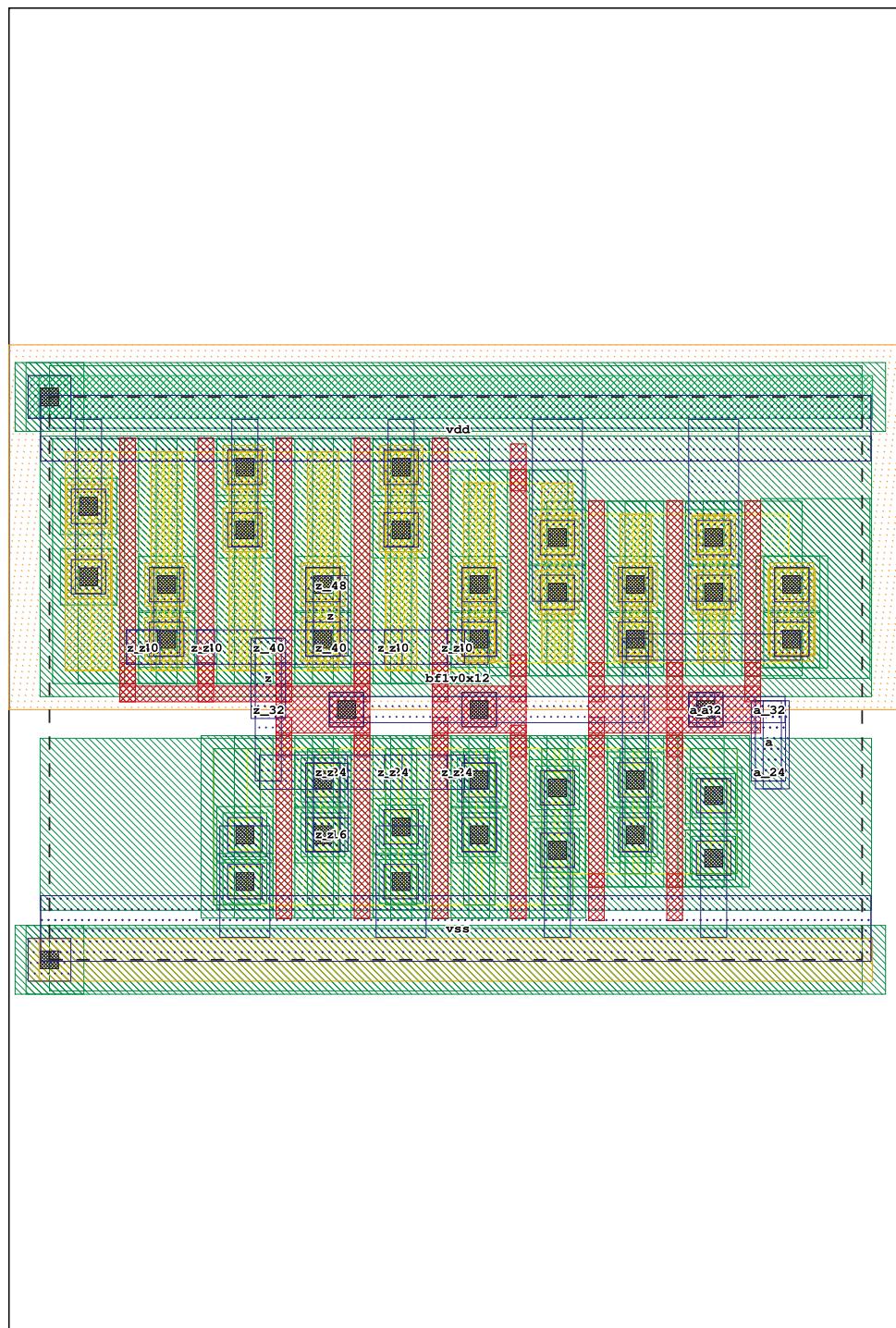
```

ENTITY bf1v0x12 IS
GENERIC (
  CONSTANT area          : NATURAL := 7488;
  CONSTANT cin_a         : NATURAL := 11;
  CONSTANT rdown_a_z    : NATURAL := 290;
  CONSTANT rup_a_z       : NATURAL := 360;
  CONSTANT tpll_a_z     : NATURAL := 91;
  CONSTANT tphh_a_z     : NATURAL := 70;
  CONSTANT transistors   : NATURAL := 15
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END bf1v0x12;

ARCHITECTURE behaviour_data_flow OF bf1v0x12 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on bf1v0x12"
  SEVERITY WARNING;
  z <= a after 89 ps;
END;

```



3.32 bf1v0x1

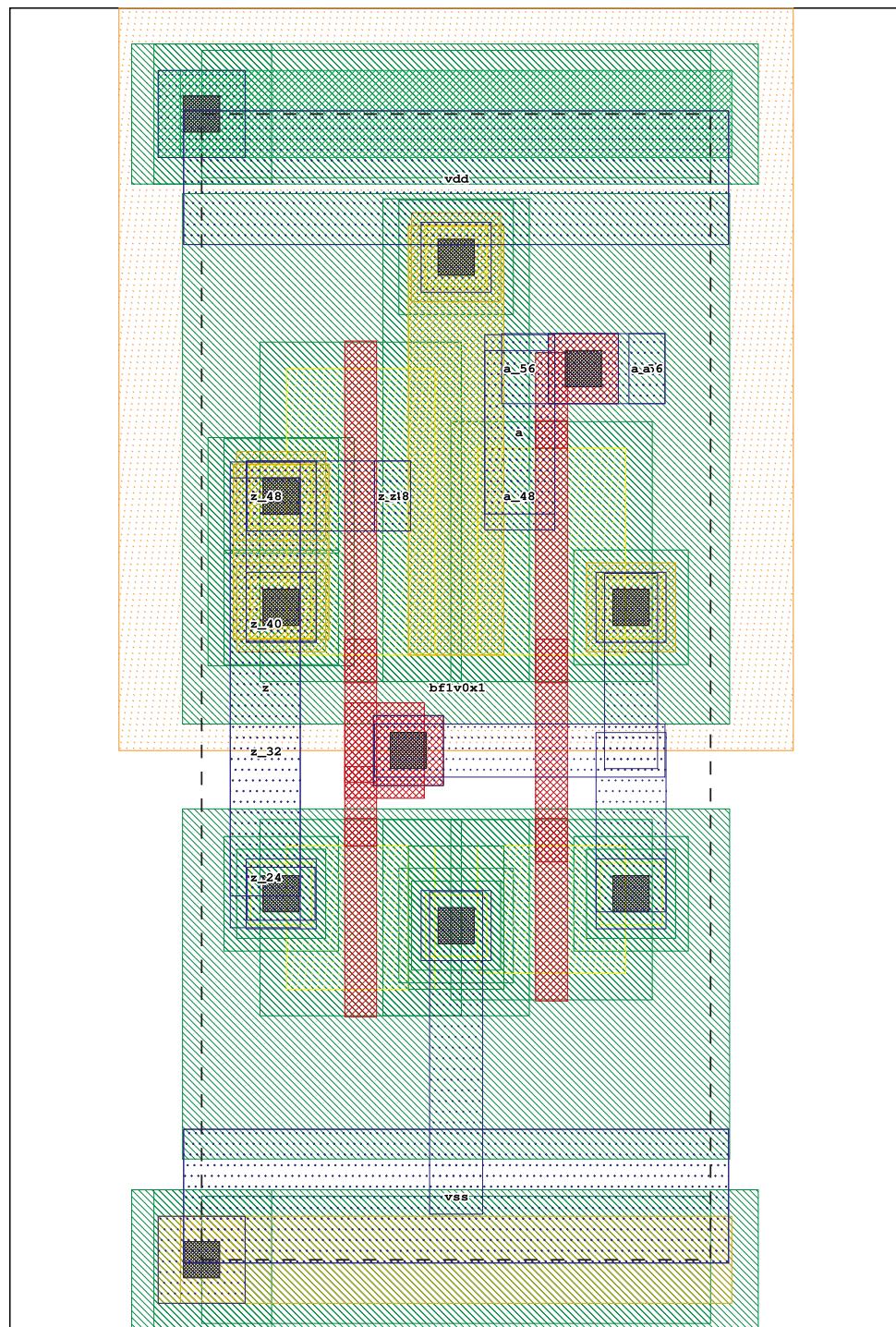
```

ENTITY bf1v0x1 IS
GENERIC (
  CONSTANT area          : NATURAL := 2304;
  CONSTANT cin_a         : NATURAL := 3;
  CONSTANT rdown_a_z    : NATURAL := 2550;
  CONSTANT rup_a_z      : NATURAL := 3290;
  CONSTANT tpll_a_z     : NATURAL := 77;
  CONSTANT tphh_a_z     : NATURAL := 56;
  CONSTANT transistors   : NATURAL := 4
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END bf1v0x1;

ARCHITECTURE behaviour_data_flow OF bf1v0x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on bf1v0x1"
  SEVERITY WARNING;
  z <= a after 140 ps;
END;

```



3.33 bf1v0x2

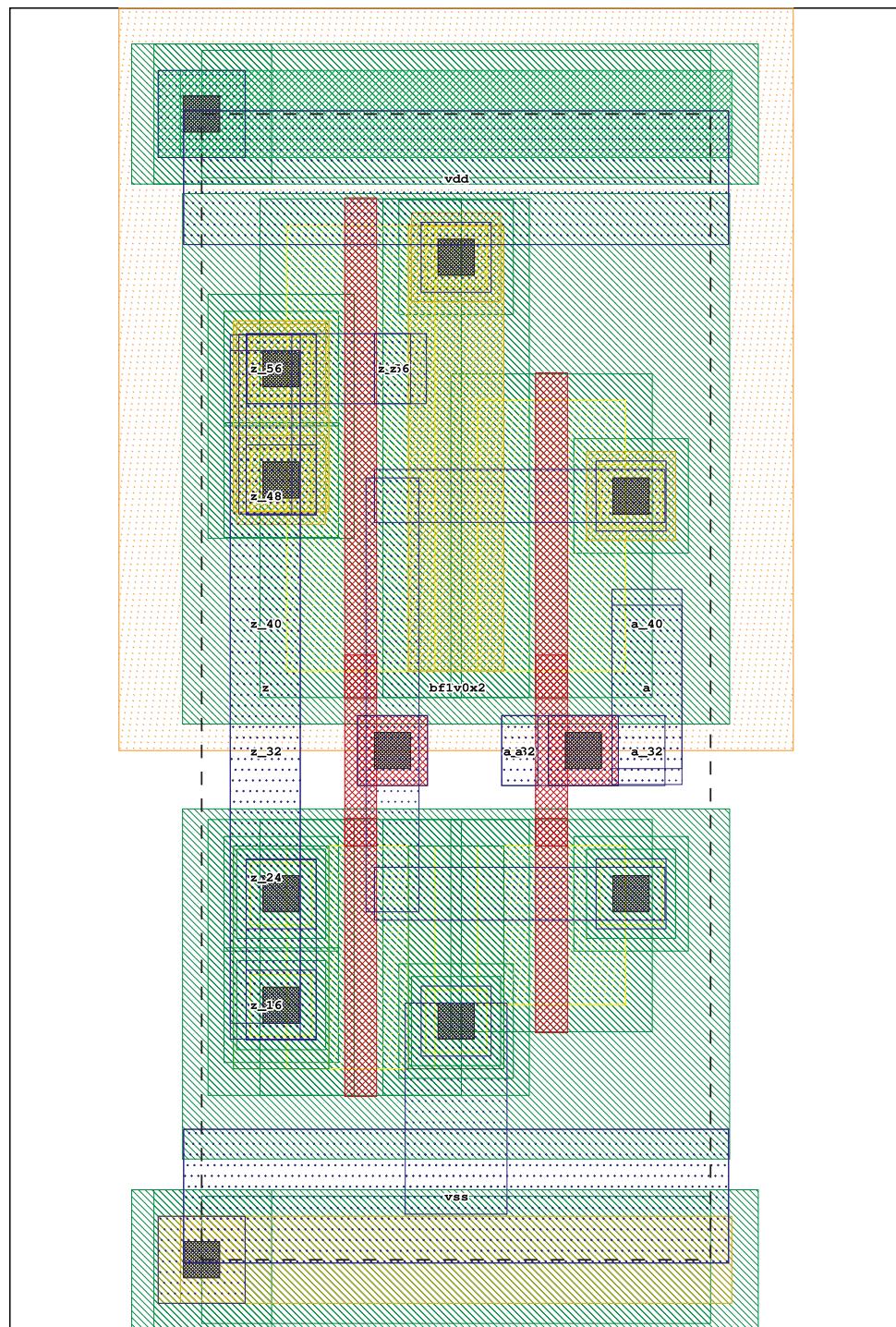
```

ENTITY bf1v0x2 IS
GENERIC (
  CONSTANT area          : NATURAL := 2304;
  CONSTANT cin_a         : NATURAL := 4;
  CONSTANT rdown_a_z    : NATURAL := 1650;
  CONSTANT rup_a_z      : NATURAL := 2120;
  CONSTANT tpll_a_z     : NATURAL := 82;
  CONSTANT tphh_a_z     : NATURAL := 62;
  CONSTANT transistors   : NATURAL := 4
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END bf1v0x2;

ARCHITECTURE behaviour_data_flow OF bf1v0x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on bf1v0x2"
  SEVERITY WARNING;
  z <= a after 119 ps;
END;

```



3.34 bf1v0x4

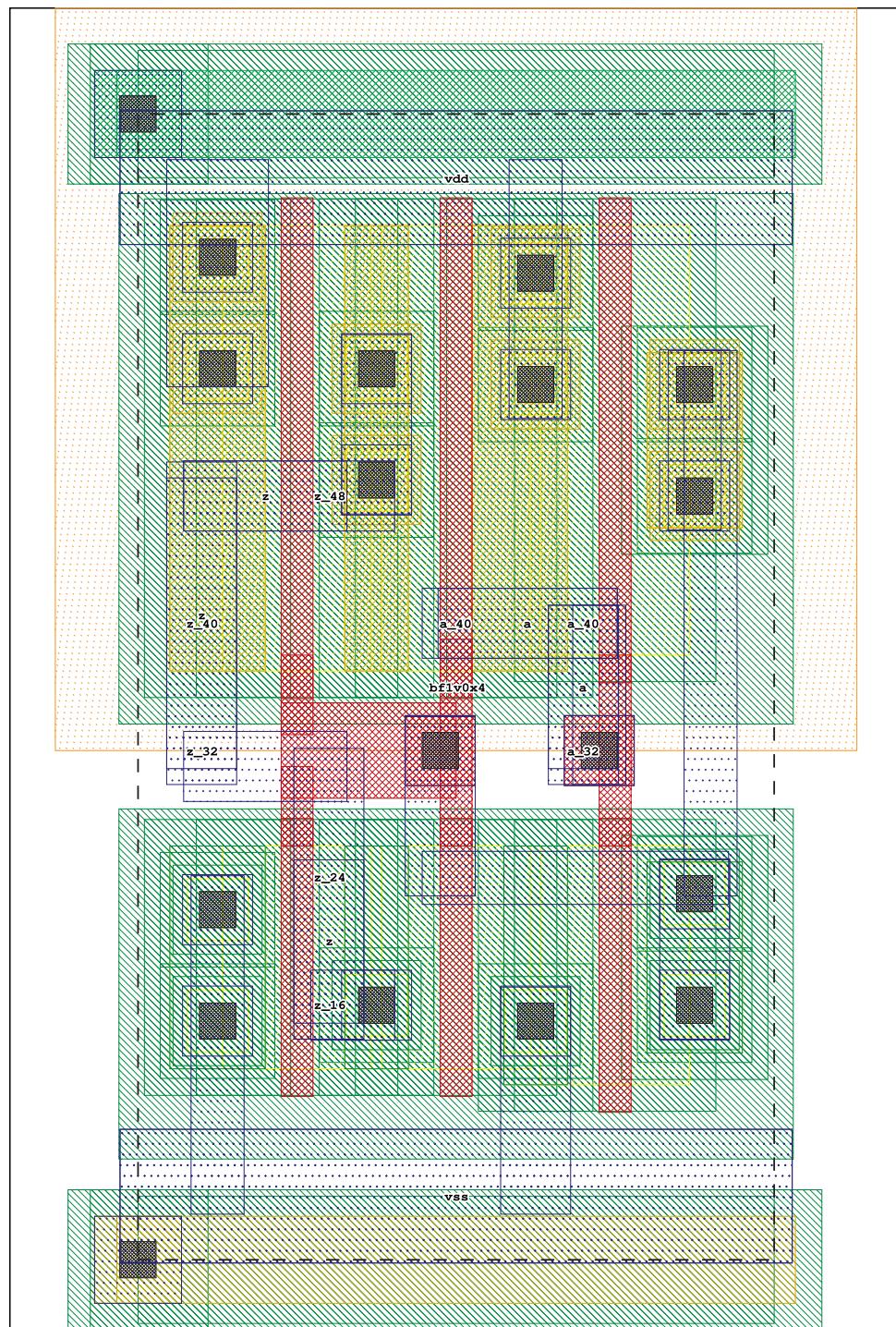
```

ENTITY bf1v0x4 IS
GENERIC (
  CONSTANT area          : NATURAL := 2880;
  CONSTANT cin_a         : NATURAL := 6;
  CONSTANT rdown_a_z    : NATURAL := 830;
  CONSTANT rup_a_z      : NATURAL := 1060;
  CONSTANT tpll_a_z     : NATURAL := 84;
  CONSTANT tphh_a_z     : NATURAL := 65;
  CONSTANT transistors   : NATURAL := 6
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END bf1v0x4;

ARCHITECTURE behaviour_data_flow OF bf1v0x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on bf1v0x4"
  SEVERITY WARNING;
  z <= a after 98 ps;
END;

```



3.35 bf1v0x8

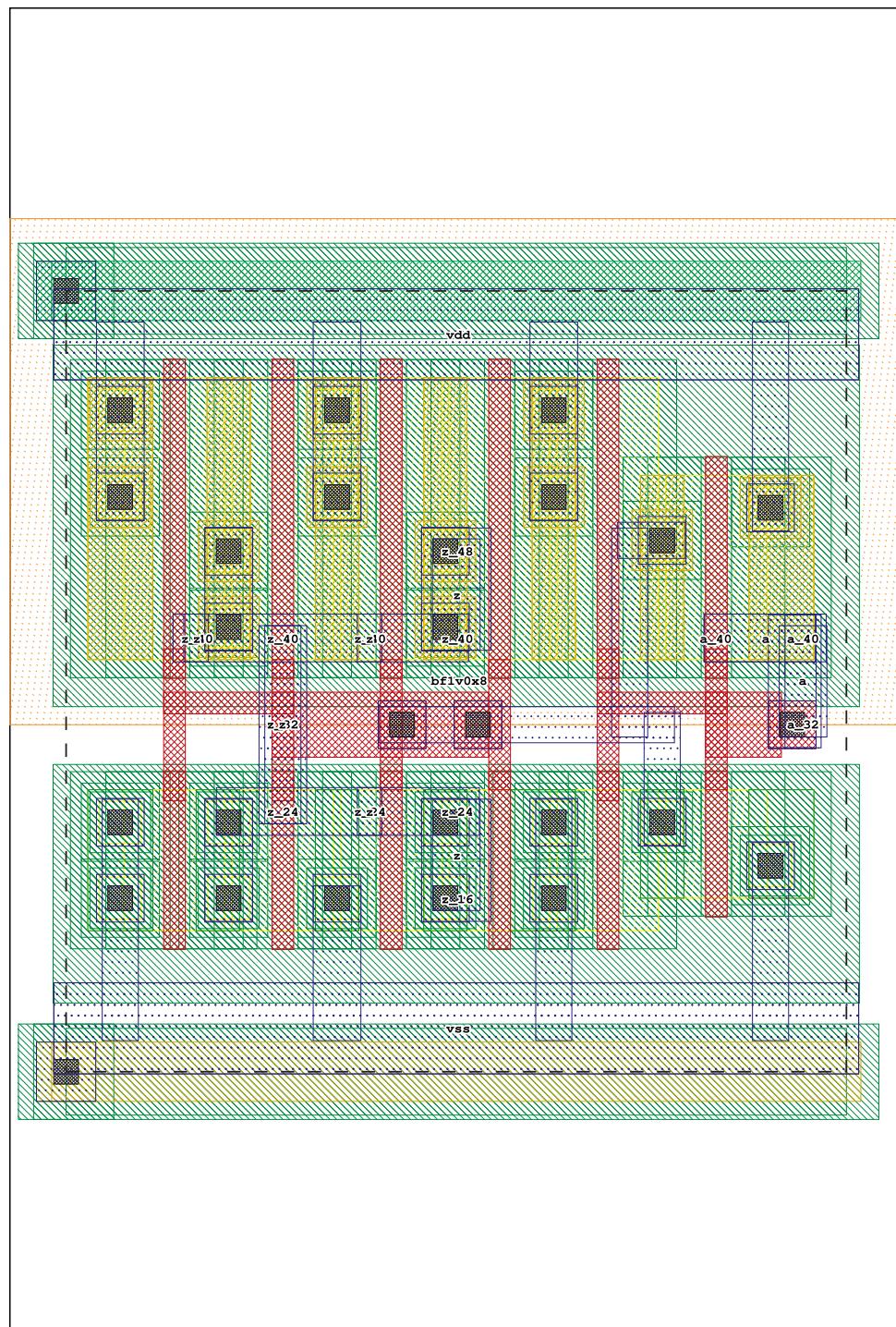
```

ENTITY bf1v0x8 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_a         : NATURAL := 8;
    CONSTANT rdown_a_z     : NATURAL := 450;
    CONSTANT rup_a_z       : NATURAL := 570;
    CONSTANT tpll_a_z      : NATURAL := 85;
    CONSTANT tphh_a_z      : NATURAL := 67;
    CONSTANT transistors   : NATURAL := 12
);
PORT (
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END bf1v0x8;

ARCHITECTURE behaviour_data_flow OF bf1v0x8 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on bf1v0x8"
        SEVERITY WARNING;
    z <= a after 89 ps;
END;

```



3.36 bf1v5x05

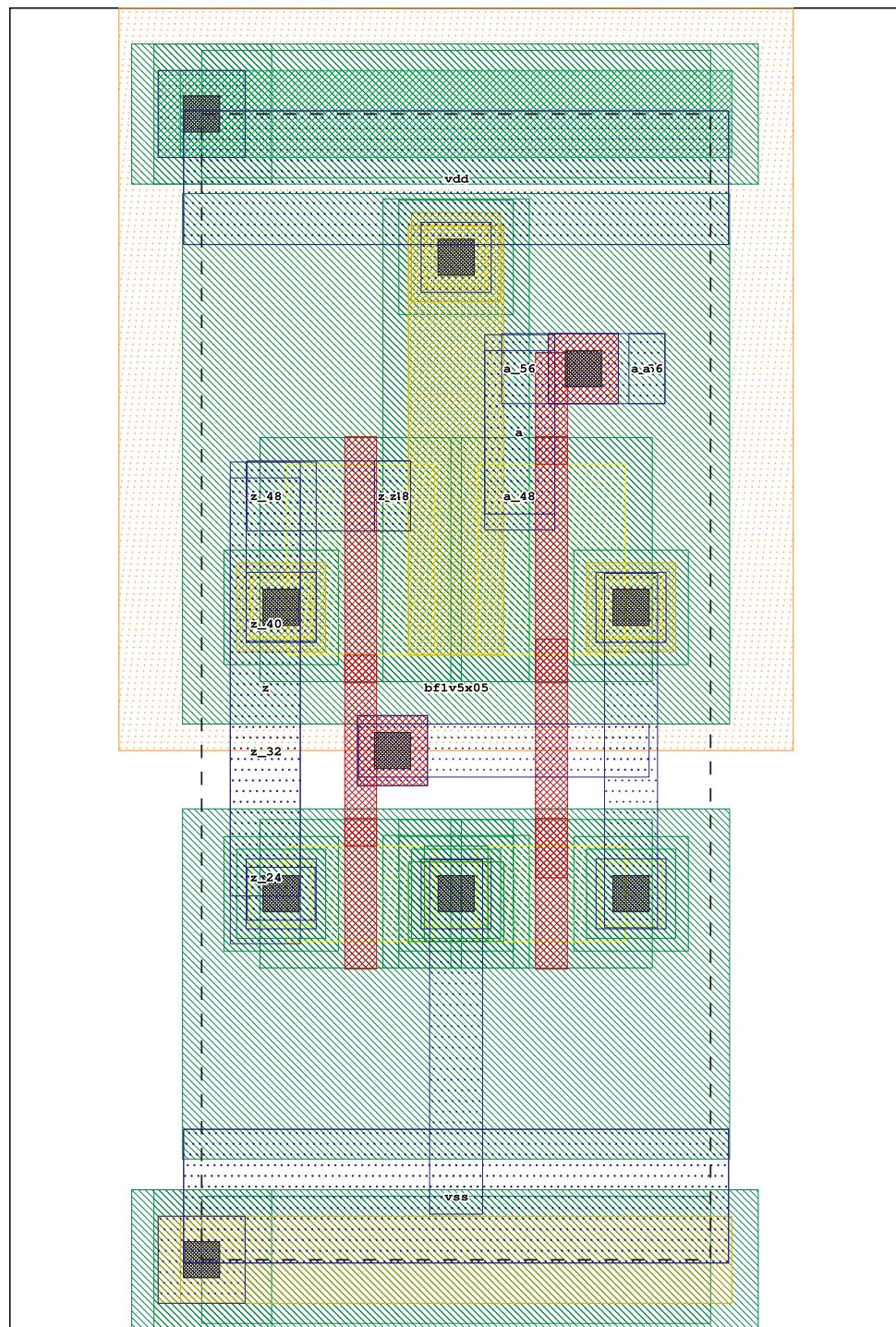
```

ENTITY bf1v5x05 IS
GENERIC (
  CONSTANT area          : NATURAL := 2304;
  CONSTANT cin_a         : NATURAL := 3;
  CONSTANT rdown_a_z    : NATURAL := 3820;
  CONSTANT rup_a_z      : NATURAL := 4940;
  CONSTANT tpll_a_z     : NATURAL := 71;
  CONSTANT tphh_a_z     : NATURAL := 59;
  CONSTANT transistors   : NATURAL := 4
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END bf1v5x05;

ARCHITECTURE behaviour_data_flow OF bf1v5x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on bf1v5x05"
  SEVERITY WARNING;
  z <= a after 175 ps;
END;

```



3.37 dfnt1v0x2

```

ENTITY dfnt1v0x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 10368;
    CONSTANT cin_cp        : NATURAL := 3;
    CONSTANT cin_d         : NATURAL := 3;
    CONSTANT rdown_cp_z   : NATURAL := 1670;
    CONSTANT rup_cp_z     : NATURAL := 2130;
    CONSTANT taf_cp_z     : NATURAL := 222;
    CONSTANT tar_cp_z     : NATURAL := 193;
    CONSTANT thf_d_cp     : NATURAL := 36;
    CONSTANT thr_d_cp     : NATURAL := 204;
    CONSTANT tsf_d_cp     : NATURAL := 343;
    CONSTANT tsr_d_cp     : NATURAL := 227;
    CONSTANT transistors  : NATURAL := 24
  );
  PORT (
    cp      : in  BIT;
    d       : in  BIT;
    z       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END dfnt1v0x2;

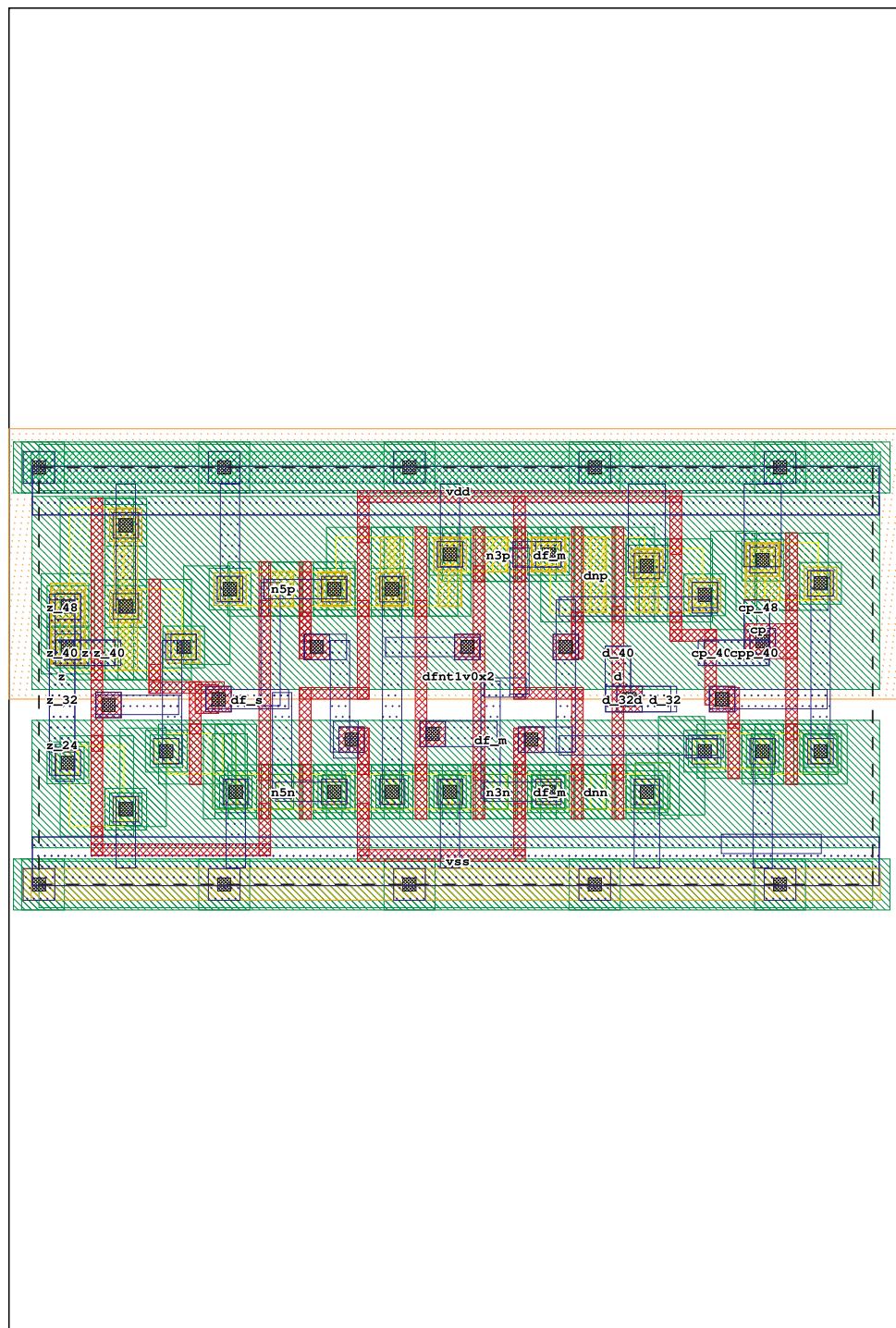
ARCHITECTURE VBE OF dfnt1v0x2 IS
  SIGNAL df_m      : REG_BIT REGISTER;

BEGIN
  ASSERT (vdd and not (vss))
  REPORT "power supply is missing on dfnt1v0x2"
  SEVERITY WARNING;

  label0 : BLOCK (cp and not cp)'STABLE)
  BEGIN
    df_m <= GUARDED not d;
  END BLOCK label0;

  z <= not df_m after 255 ps;
END;

```



3.38 dly1v0x05

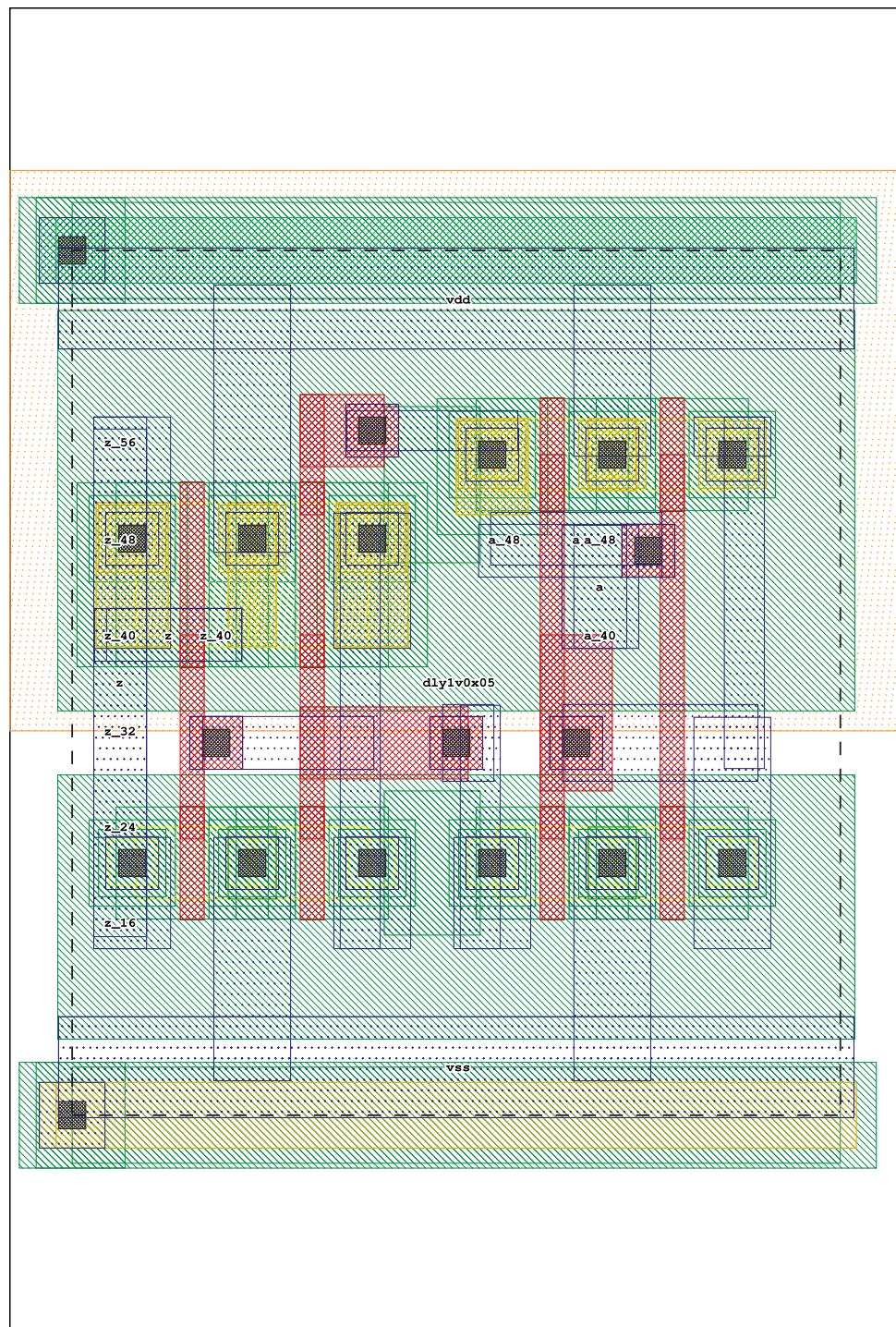
```

ENTITY dly1v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 3830;
    CONSTANT rup_a_z       : NATURAL := 4950;
    CONSTANT tpll_a_z      : NATURAL := 166;
    CONSTANT tphh_a_z      : NATURAL := 158;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END dly1v0x05;

ARCHITECTURE behaviour_data_flow OF dly1v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on dly1v0x05"
        SEVERITY WARNING;
    z <= a after 272 ps;
END;

```



3.39 dly2v0x05

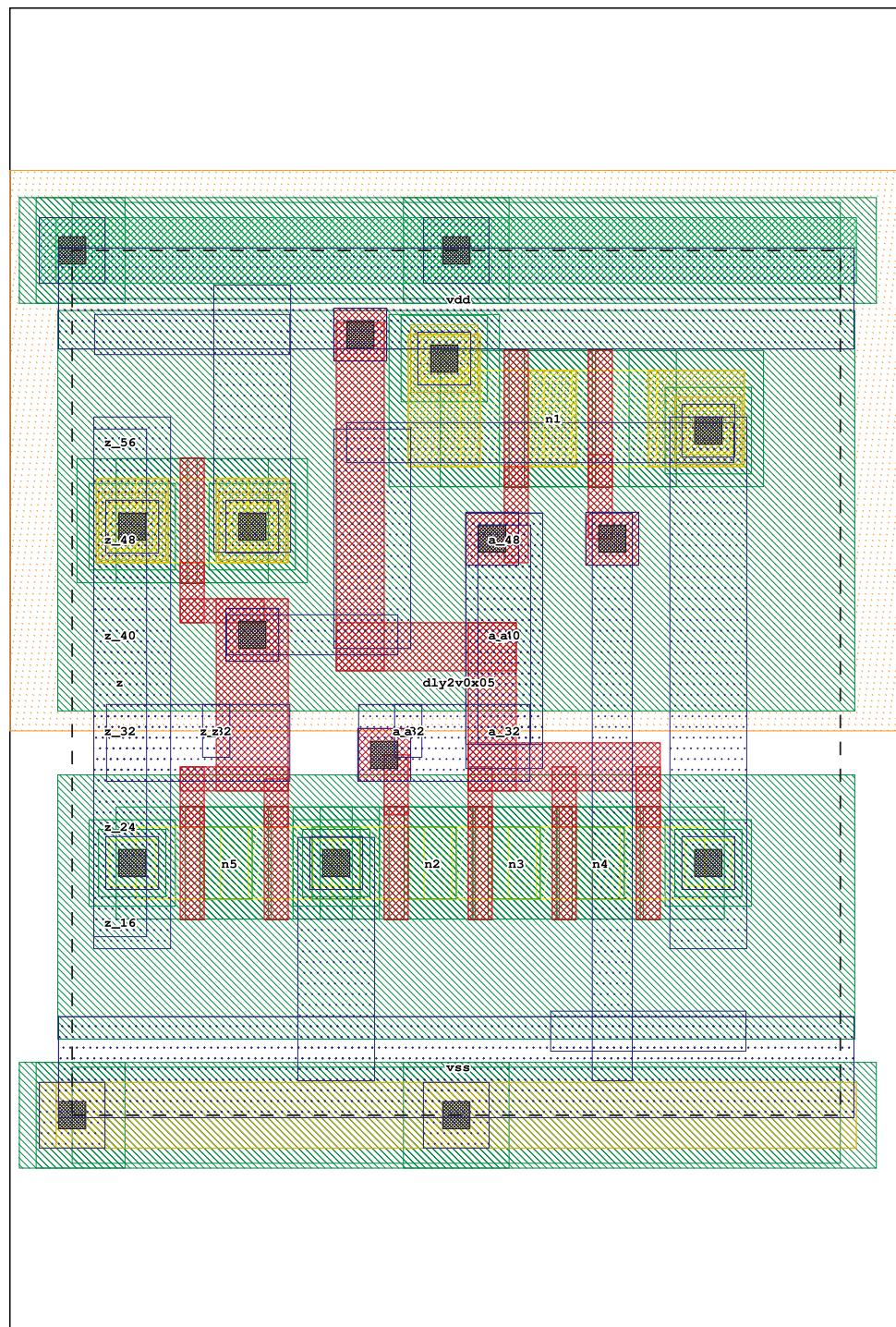
```

ENTITY dly2v0x05 IS
GENERIC (
  CONSTANT area          : NATURAL := 4608;
  CONSTANT cin_a         : NATURAL := 3;
  CONSTANT rdown_a_z     : NATURAL := 7080;
  CONSTANT rup_a_z       : NATURAL := 8860;
  CONSTANT tp1l_a_z      : NATURAL := 216;
  CONSTANT tpjh_a_z      : NATURAL := 170;
  CONSTANT transistors   : NATURAL := 9
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd    : in  BIT;
  vss    : in  BIT
);
END dly2v0x05;

ARCHITECTURE behaviour_data_flow OF dly2v0x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on dly2v0x05"
  SEVERITY WARNING;
  z <= a after 392 ps;
END;

```



3.40 iv1v0x05

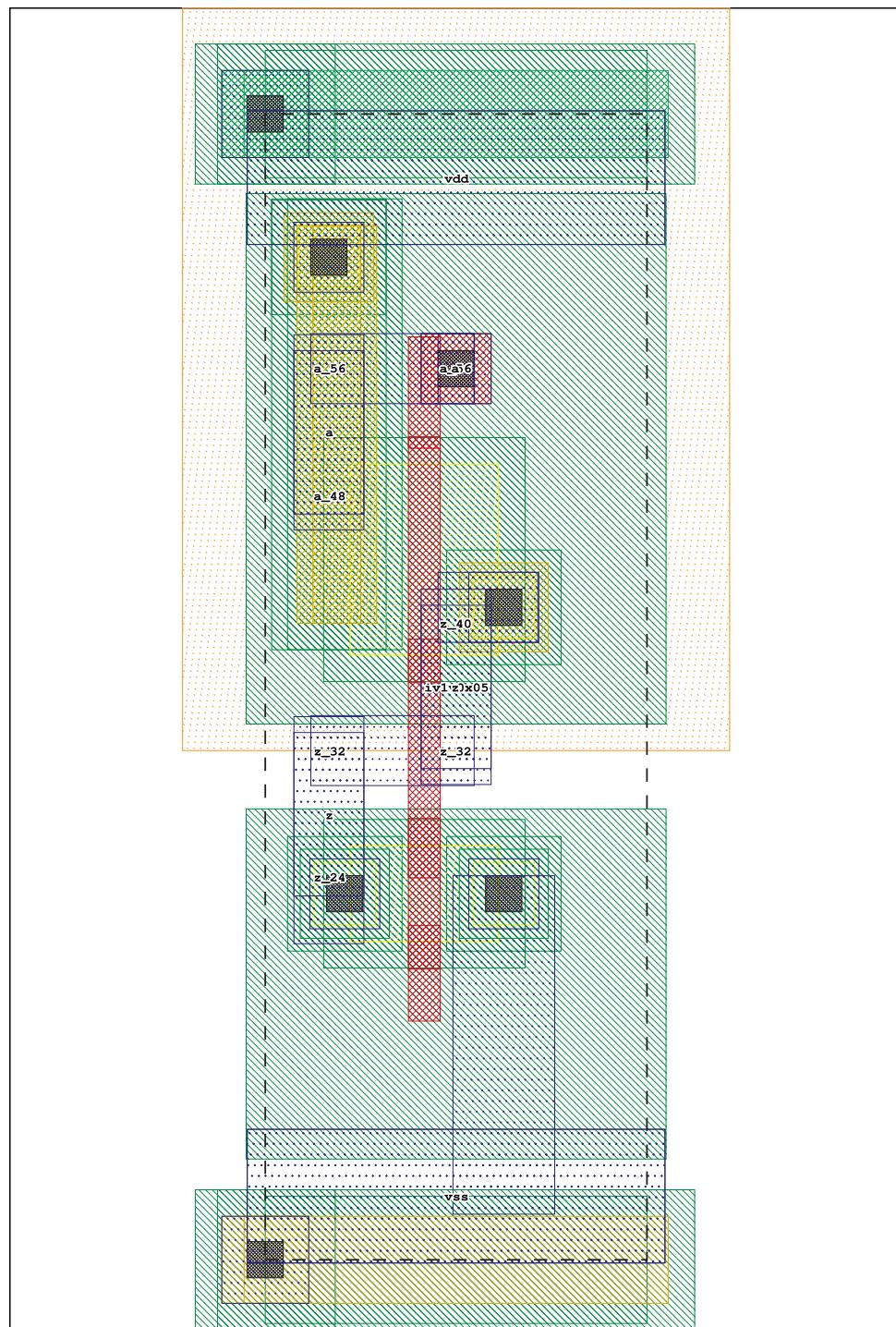
```

ENTITY iv1v0x05 IS
GENERIC (
  CONSTANT area          : NATURAL := 1728;
  CONSTANT cin_a         : NATURAL := 3;
  CONSTANT rdown_a_z    : NATURAL := 3840;
  CONSTANT rup_a_z      : NATURAL := 4930;
  CONSTANT tphl_a_z     : NATURAL := 34;
  CONSTANT tplh_a_z     : NATURAL := 39;
  CONSTANT transistors   : NATURAL := 2
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END iv1v0x05;

ARCHITECTURE behaviour_data_flow OF iv1v0x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on iv1v0x05"
  SEVERITY WARNING;
  z <= not (a) after 146 ps;
END;

```



3.41 iv1v1x05

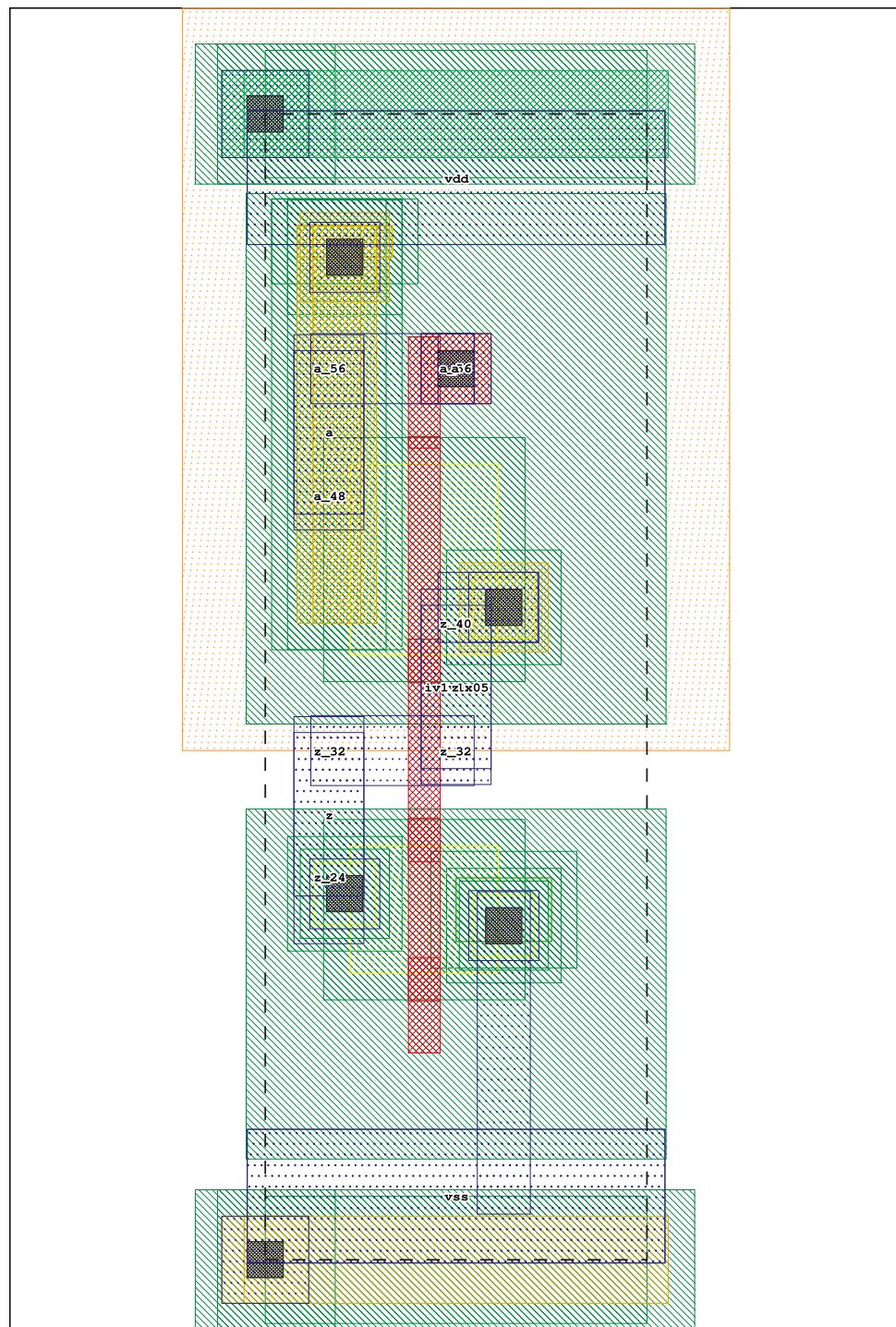
```

ENTITY iv1v1x05 IS
GENERIC (
  CONSTANT area          : NATURAL := 1728;
  CONSTANT cin_a         : NATURAL := 3;
  CONSTANT rdown_a_z    : NATURAL := 2920;
  CONSTANT rup_a_z      : NATURAL := 4930;
  CONSTANT tphl_a_z     : NATURAL := 30;
  CONSTANT tplh_a_z     : NATURAL := 40;
  CONSTANT transistors   : NATURAL := 2
);
PORT (
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END iv1v1x05;

ARCHITECTURE behaviour_data_flow OF iv1v1x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on iv1v1x05"
  SEVERITY WARNING;
  z <= not (a) after 133 ps;
END;

```



3.42 lant1v0x05

```

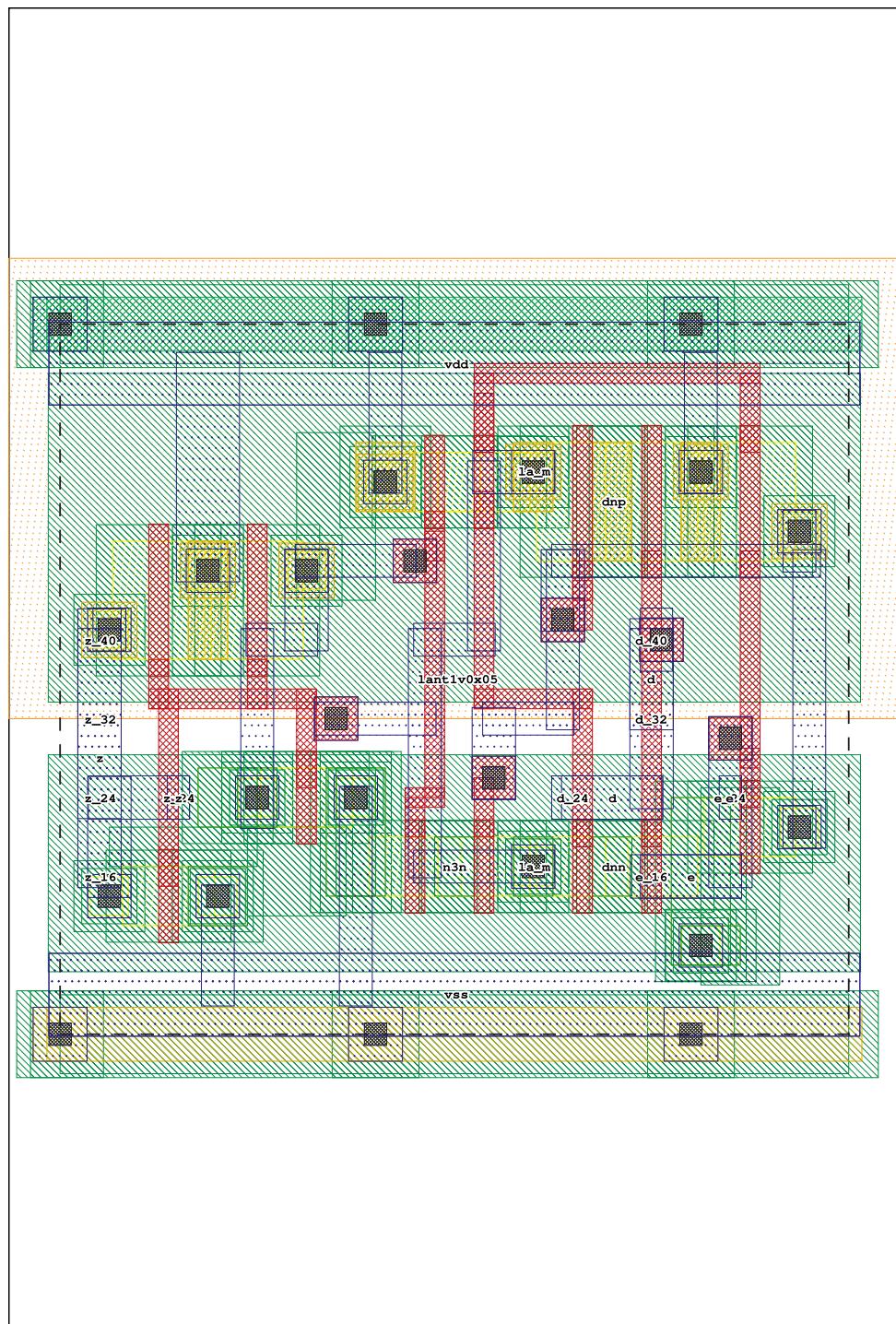
ENTITY lant1v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5760;
    CONSTANT cin_e         : NATURAL := 5;
    CONSTANT cin_d         : NATURAL := 3;
    CONSTANT rdown_e_z     : NATURAL := 4260;
    CONSTANT rdown_d_z     : NATURAL := 4450;
    CONSTANT rup_e_z       : NATURAL := 5100;
    CONSTANT rup_d_z       : NATURAL := 5170;
    CONSTANT taf_e_z       : NATURAL := 185;
    CONSTANT taf_d_z       : NATURAL := 162;
    CONSTANT tar_e_z       : NATURAL := 102;
    CONSTANT tar_d_z       : NATURAL := 117;
    CONSTANT thf_d_e       : NATURAL := 0;
    CONSTANT thr_d_e       : NATURAL := 0;
    CONSTANT tsf_d_e       : NATURAL := 365;
    CONSTANT tsr_d_e       : NATURAL := 384;
    CONSTANT transistors   : NATURAL := 14
);
PORT (
    e      : in  BIT;
    d      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END lant1v0x05;

ARCHITECTURE VBE OF lant1v0x05 IS
    SIGNAL la_m      : REG_BIT REGISTER;

BEGIN
    ASSERT (vdd and not (vss))
        REPORT "power supply is missing on lant1v0x05"
        SEVERITY WARNING;
    label0 : BLOCK (e)
    BEGIN
        la_m <= GUARDED not d;
    END BLOCK label0;

    z <= not la_m after 260 ps;
END;

```



3.43 mxi2v0x05

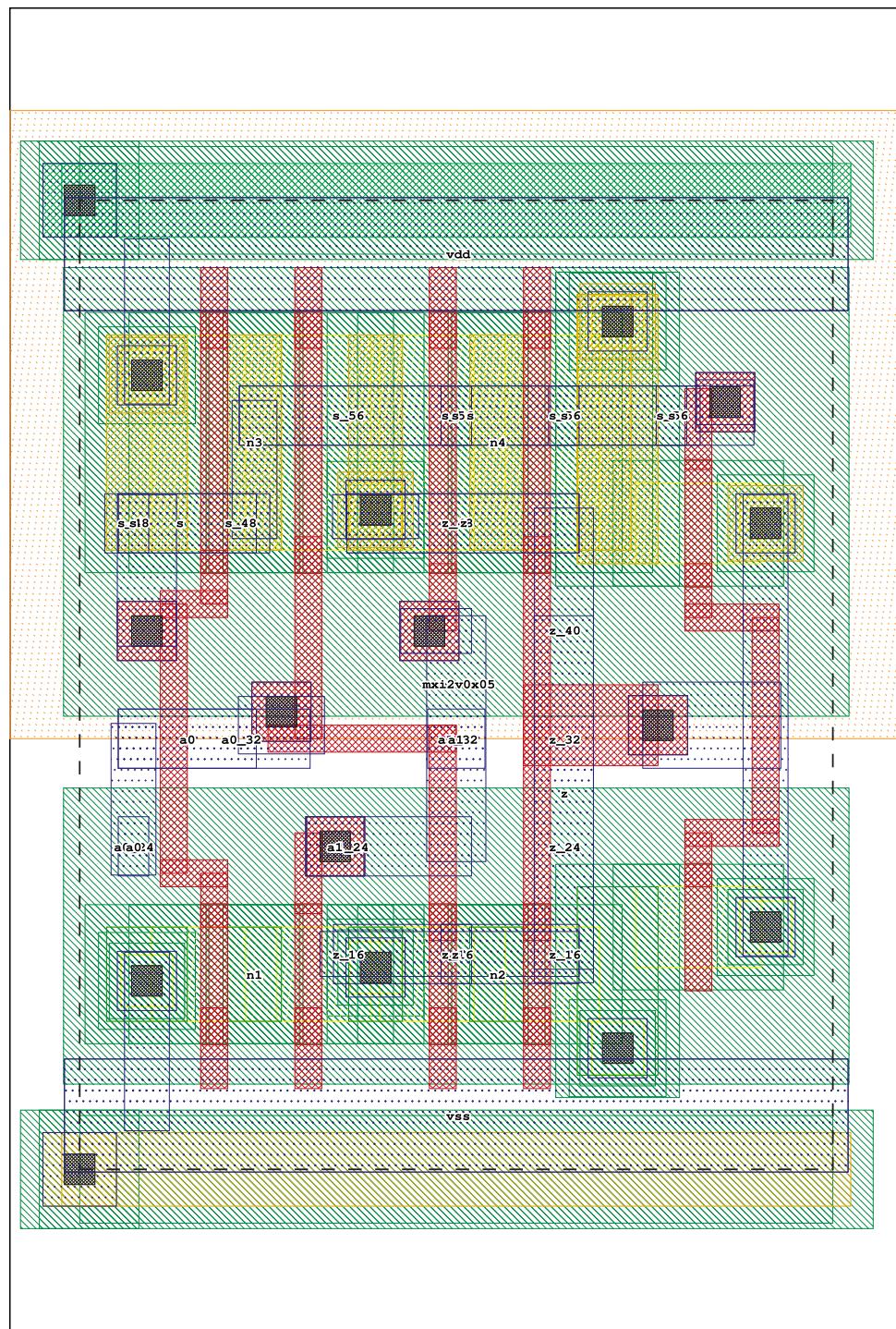
```

ENTITY mxi2v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_s         : NATURAL := 6;
    CONSTANT cin_a0        : NATURAL := 3;
    CONSTANT cin_a1        : NATURAL := 4;
    CONSTANT rdown_s_z     : NATURAL := 5310;
    CONSTANT rdown_a0_z    : NATURAL := 5310;
    CONSTANT rdown_a1_z    : NATURAL := 5320;
    CONSTANT rup_s_z       : NATURAL := 7260;
    CONSTANT rup_a0_z      : NATURAL := 7330;
    CONSTANT rup_a1_z      : NATURAL := 7360;
    CONSTANT tphl_a0_z     : NATURAL := 56;
    CONSTANT tphl_a1_z     : NATURAL := 59;
    CONSTANT tphl_s_z      : NATURAL := 57;
    CONSTANT tplh_a0_z     : NATURAL := 62;
    CONSTANT tplh_a1_z     : NATURAL := 65;
    CONSTANT tplh_s_z      : NATURAL := 73;
    CONSTANT tphh_s_z      : NATURAL := 99;
    CONSTANT tpll_s_z      : NATURAL := 132;
    CONSTANT transistors   : NATURAL := 10
);
PORT (
    s      : in  BIT;
    a0     : in  BIT;
    a1     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END mxi2v0x05;

ARCHITECTURE behaviour_data_flow OF mxi2v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on mxi2v0x05"
        SEVERITY WARNING;
    z <= (not a0 and not s) or (not a1 and s) after 233 ps;
END;

```



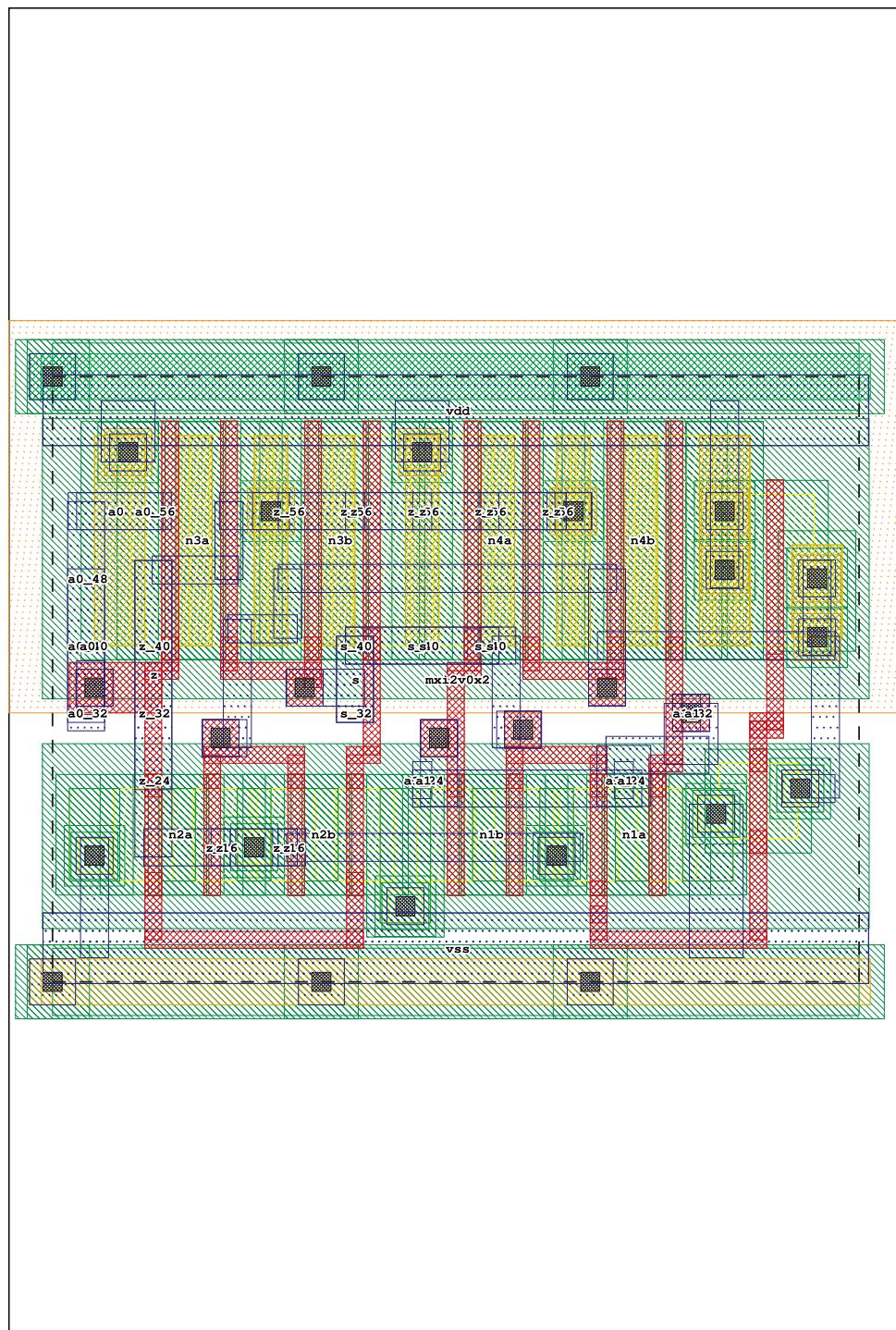
3.44 mxi2v0x2

```

ENTITY mxi2v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 6912;
    CONSTANT cin_s          : NATURAL := 12;
    CONSTANT cin_a0         : NATURAL := 9;
    CONSTANT cin_a1         : NATURAL := 9;
    CONSTANT rdown_s_z      : NATURAL := 1670;
    CONSTANT rdown_a0_z     : NATURAL := 1700;
    CONSTANT rdown_a1_z     : NATURAL := 1690;
    CONSTANT rup_s_z        : NATURAL := 2300;
    CONSTANT rup_a0_z        : NATURAL := 2340;
    CONSTANT rup_a1_z        : NATURAL := 2340;
    CONSTANT tphl_a0_z       : NATURAL := 57;
    CONSTANT tphl_a1_z       : NATURAL := 54;
    CONSTANT tphl_s_z        : NATURAL := 40;
    CONSTANT tplh_a0_z       : NATURAL := 69;
    CONSTANT tplh_a1_z       : NATURAL := 73;
    CONSTANT tplh_s_z        : NATURAL := 47;
    CONSTANT tphh_s_z        : NATURAL := 106;
    CONSTANT tpll_s_z        : NATURAL := 121;
    CONSTANT transistors     : NATURAL := 18
);
PORT (
    s      : in  BIT;
    a0     : in  BIT;
    a1     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END mxi2v0x2;

ARCHITECTURE behaviour_data_flow OF mxi2v0x2 IS
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on mxi2v0x2"
        SEVERITY WARNING;
    z <= (not a0 and not s) or (not a1 and s) after 121 ps;
END;

```



3.45 mxn2v0x05

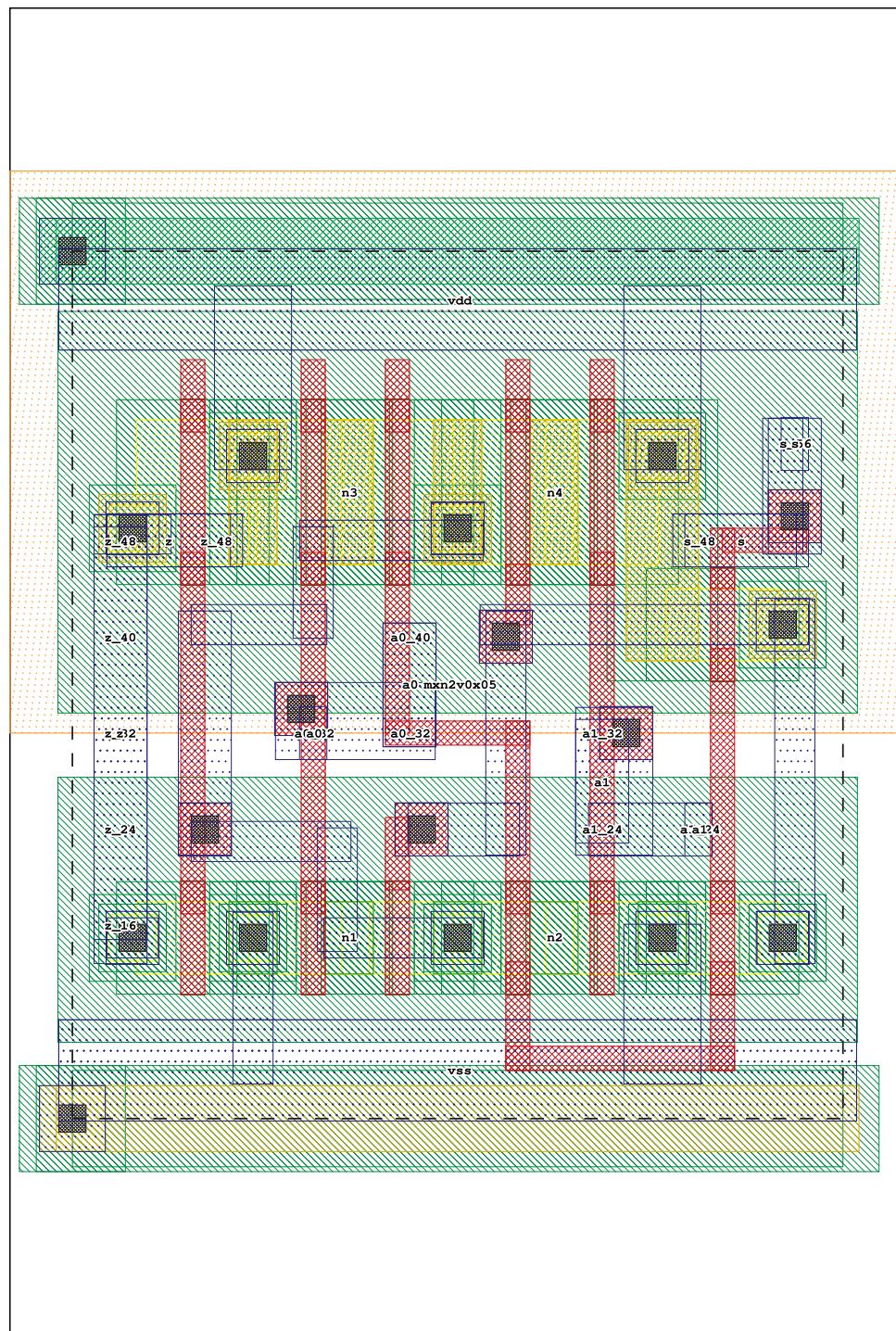
```

ENTITY mxn2v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_s         : NATURAL := 5;
    CONSTANT cin_a0        : NATURAL := 3;
    CONSTANT cin_a1        : NATURAL := 3;
    CONSTANT rdown_s_z     : NATURAL := 4070;
    CONSTANT rdown_a0_z    : NATURAL := 4080;
    CONSTANT rdown_a1_z    : NATURAL := 4080;
    CONSTANT rup_s_z       : NATURAL := 5030;
    CONSTANT rup_a0_z      : NATURAL := 5030;
    CONSTANT rup_a1_z      : NATURAL := 5030;
    CONSTANT tphh_a0_z     : NATURAL := 113;
    CONSTANT tphh_a1_z     : NATURAL := 108;
    CONSTANT tpll_a0_z     : NATURAL := 149;
    CONSTANT tpll_a1_z     : NATURAL := 147;
    CONSTANT tphh_s_z      : NATURAL := 94;
    CONSTANT tphl_s_z      : NATURAL := 159;
    CONSTANT tpll_s_z      : NATURAL := 120;
    CONSTANT tplh_s_z      : NATURAL := 185;
    CONSTANT transistors   : NATURAL := 12
);
PORT (
    s      : in  BIT;
    a0     : in  BIT;
    a1     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END mxn2v0x05;

ARCHITECTURE behaviour_data_flow OF mxn2v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on mxn2v0x05"
    SEVERITY WARNING;
    z <= (a0 and not s) or (a1 and s) after 248 ps;
END;

```



3.46 nd2abv0x05

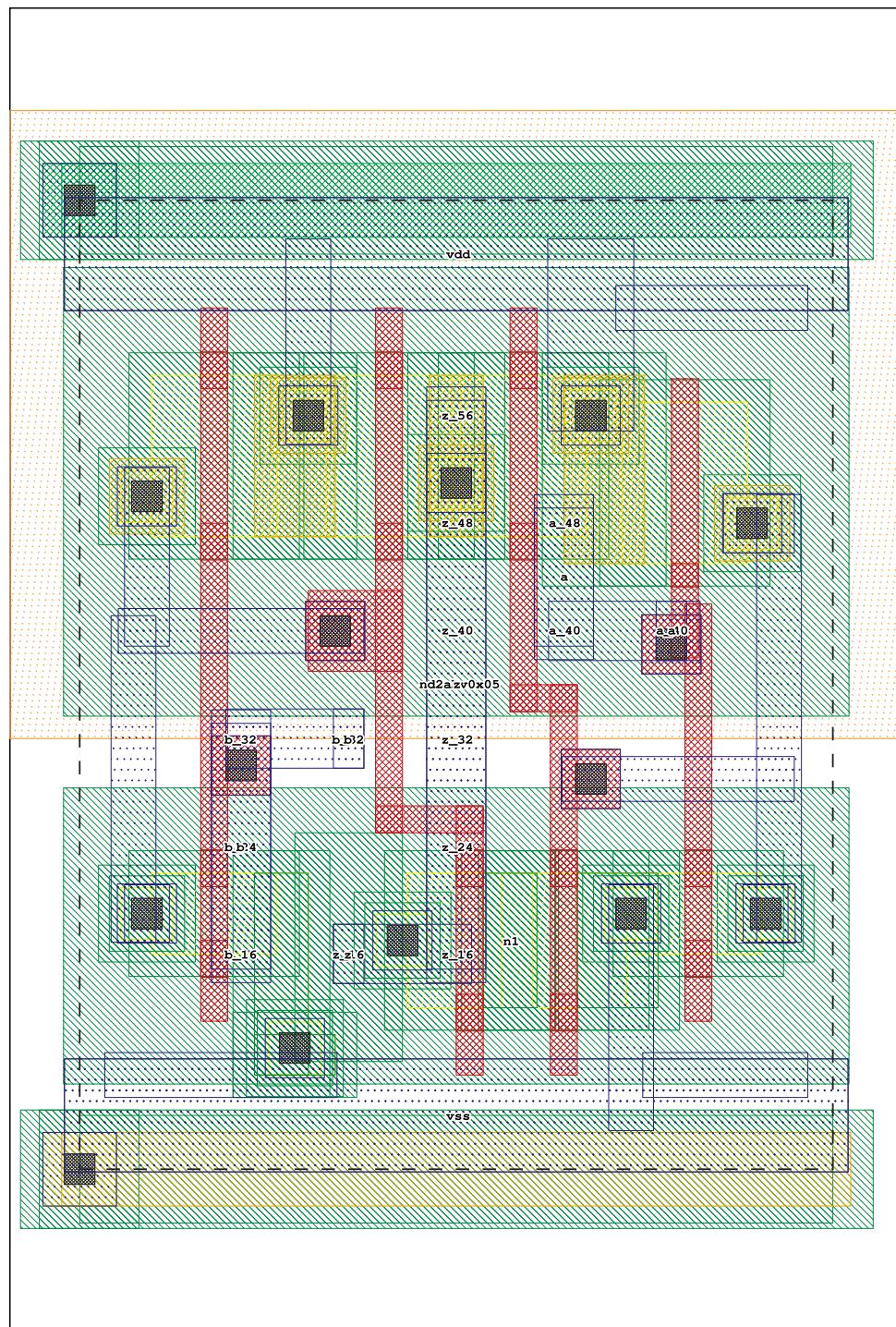
```

ENTITY nd2abv0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT rdown_a_z    : NATURAL := 3700;
    CONSTANT rdown_b_z    : NATURAL := 3700;
    CONSTANT rup_a_z      : NATURAL := 4950;
    CONSTANT rup_b_z      : NATURAL := 4960;
    CONSTANT tpll_a_z     : NATURAL := 82;
    CONSTANT tphh_b_z     : NATURAL := 73;
    CONSTANT tpll_b_z     : NATURAL := 80;
    CONSTANT tphh_a_z     : NATURAL := 78;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2abv0x05;

ARCHITECTURE behaviour_data_flow OF nd2abv0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2abv0x05"
    SEVERITY WARNING;
    z <= (a or b) after 186 ps;
END;

```



3.47 nd2av0x05

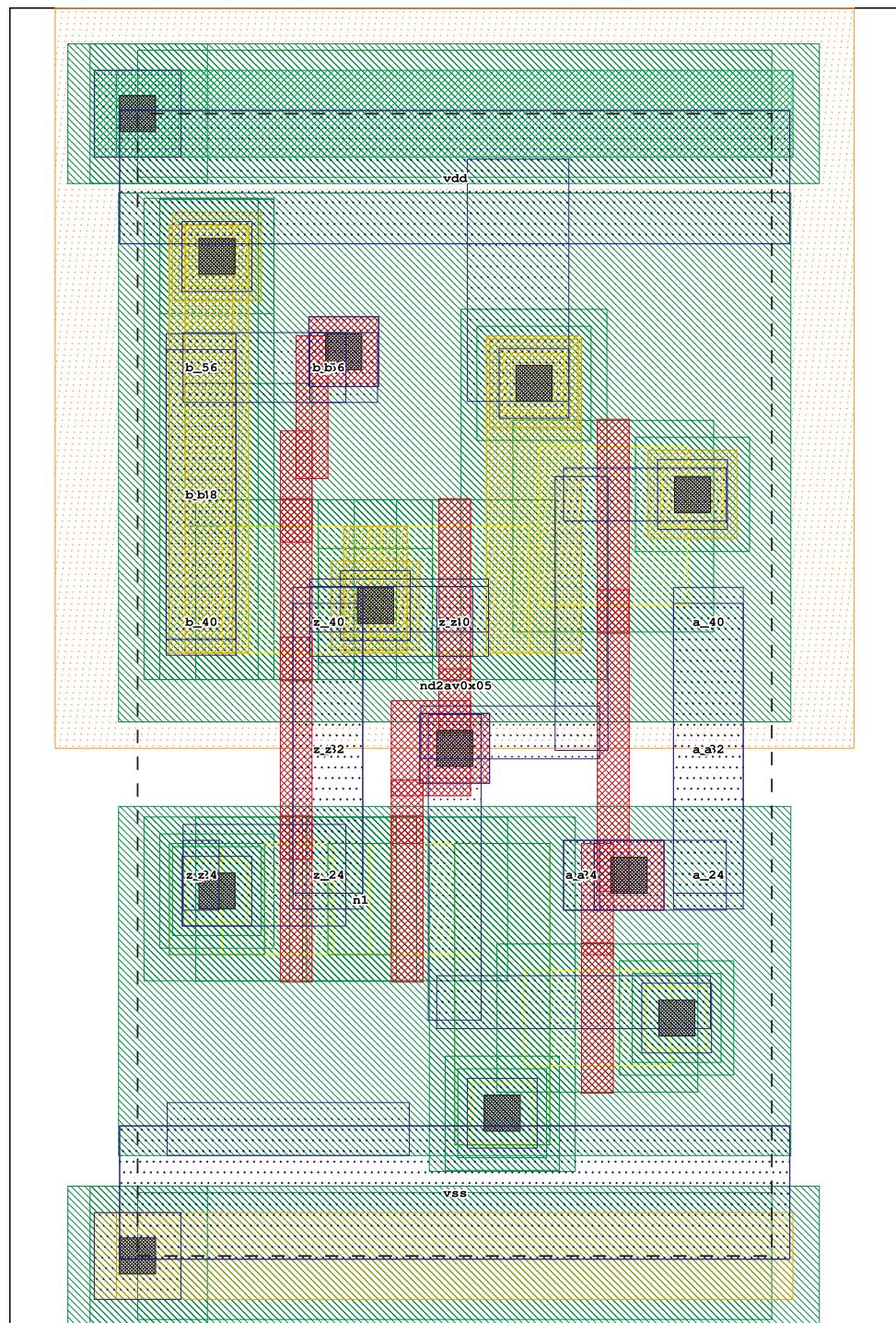
```

ENTITY nd2av0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_b         : NATURAL := 2;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT rdown_b_z    : NATURAL := 5290;
    CONSTANT rdown_a_z    : NATURAL := 5280;
    CONSTANT rup_b_z      : NATURAL := 7420;
    CONSTANT rup_a_z      : NATURAL := 7430;
    CONSTANT tphl_b_z     : NATURAL := 36;
    CONSTANT tplh_b_z     : NATURAL := 48;
    CONSTANT tp11_a_z     : NATURAL := 86;
    CONSTANT tphh_a_z     : NATURAL := 78;
    CONSTANT transistors   : NATURAL := 6
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2av0x05;

ARCHITECTURE behaviour_data_flow OF nd2av0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2av0x05"
    SEVERITY WARNING;
    z <= (not (b) or a) after 221 ps;
END;

```



3.48 nd2av0x1

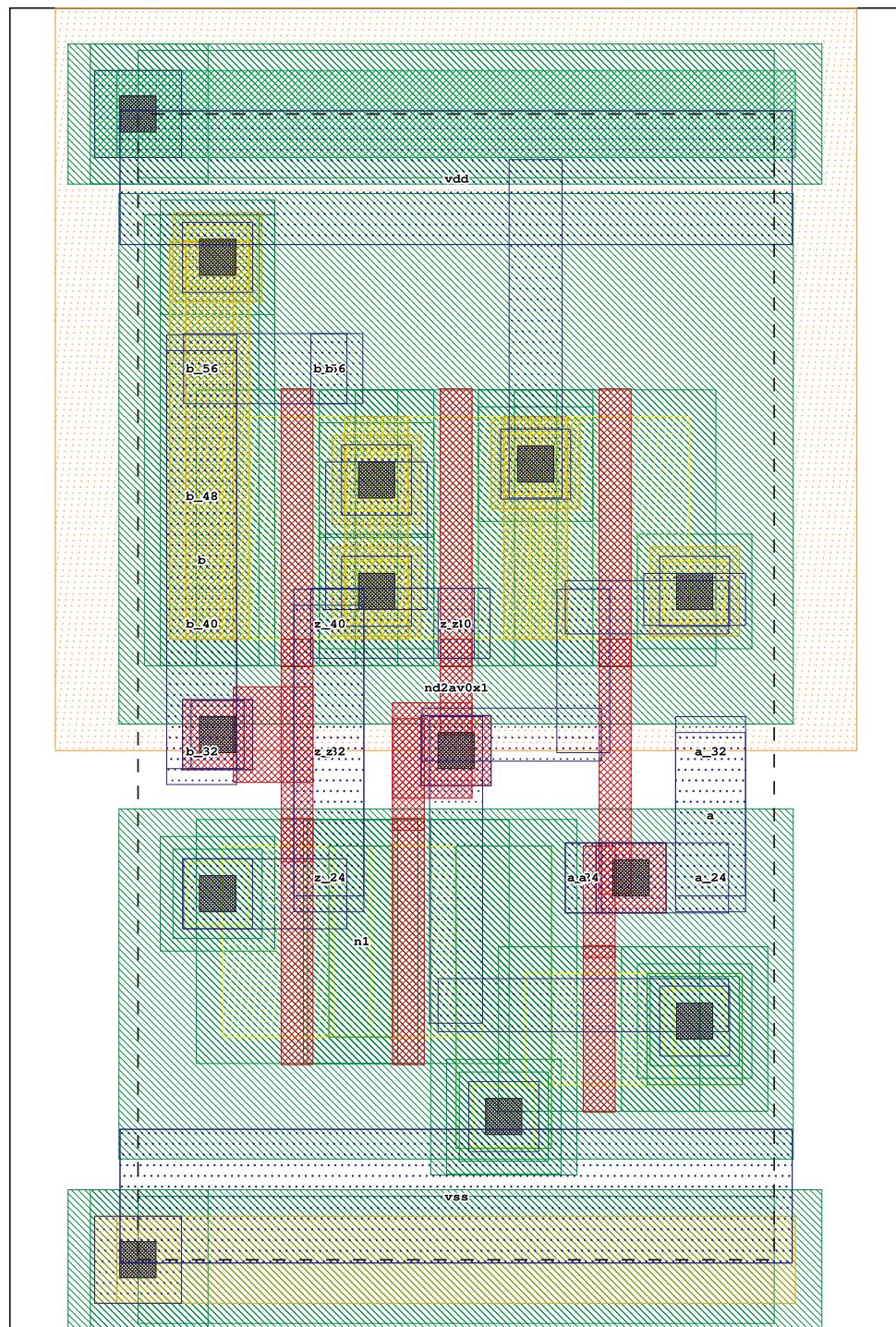
```

ENTITY nd2av0x1 IS
GENERIC (
  CONSTANT area          : NATURAL := 2880;
  CONSTANT cin_b          : NATURAL := 4;
  CONSTANT cin_a          : NATURAL := 4;
  CONSTANT rdown_b_z      : NATURAL := 3100;
  CONSTANT rdown_a_z      : NATURAL := 3080;
  CONSTANT rup_b_z        : NATURAL := 4240;
  CONSTANT rup_a_z        : NATURAL := 4250;
  CONSTANT tphl_b_z       : NATURAL := 34;
  CONSTANT tplh_b_z       : NATURAL := 46;
  CONSTANT tp11_a_z       : NATURAL := 83;
  CONSTANT tphh_a_z       : NATURAL := 81;
  CONSTANT transistors    : NATURAL := 6
);
PORT (
  b      : in  BIT;
  a      : in  BIT;
  z      : out BIT;
  vdd    : in  BIT;
  vss    : in  BIT
);
END nd2av0x1;

ARCHITECTURE behaviour_data_flow OF nd2av0x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nd2av0x1"
  SEVERITY WARNING;
  z <= (not (b) or a) after 153 ps;
END;

```



3.49 nd2av0x2

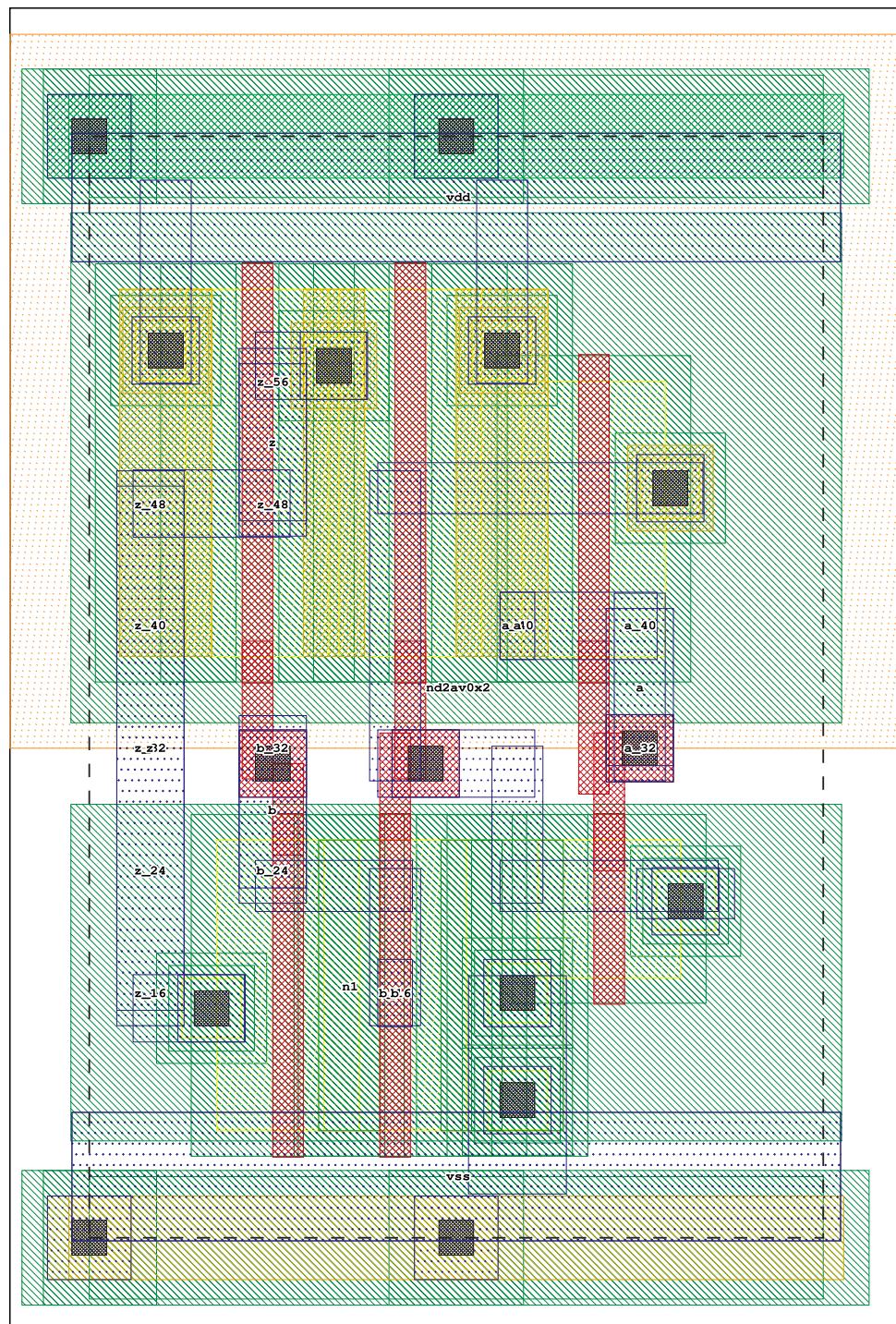
```

ENTITY nd2av0x2 IS
GENERIC (
  CONSTANT area          : NATURAL := 3456;
  CONSTANT cin_b          : NATURAL := 5;
  CONSTANT cin_a          : NATURAL := 4;
  CONSTANT rdown_b_z      : NATURAL := 1950;
  CONSTANT rdown_a_z      : NATURAL := 1940;
  CONSTANT rup_b_z        : NATURAL := 2470;
  CONSTANT rup_a_z        : NATURAL := 2470;
  CONSTANT tphl_b_z       : NATURAL := 34;
  CONSTANT tplh_b_z       : NATURAL := 44;
  CONSTANT tp11_a_z       : NATURAL := 83;
  CONSTANT tphh_a_z       : NATURAL := 79;
  CONSTANT transistors    : NATURAL := 6
);
PORT (
  b      : in  BIT;
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END nd2av0x2;

ARCHITECTURE behaviour_data_flow OF nd2av0x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nd2av0x2"
  SEVERITY WARNING;
  z <= (not (b) or a) after 115 ps;
END;

```



3.50 nd2av0x4

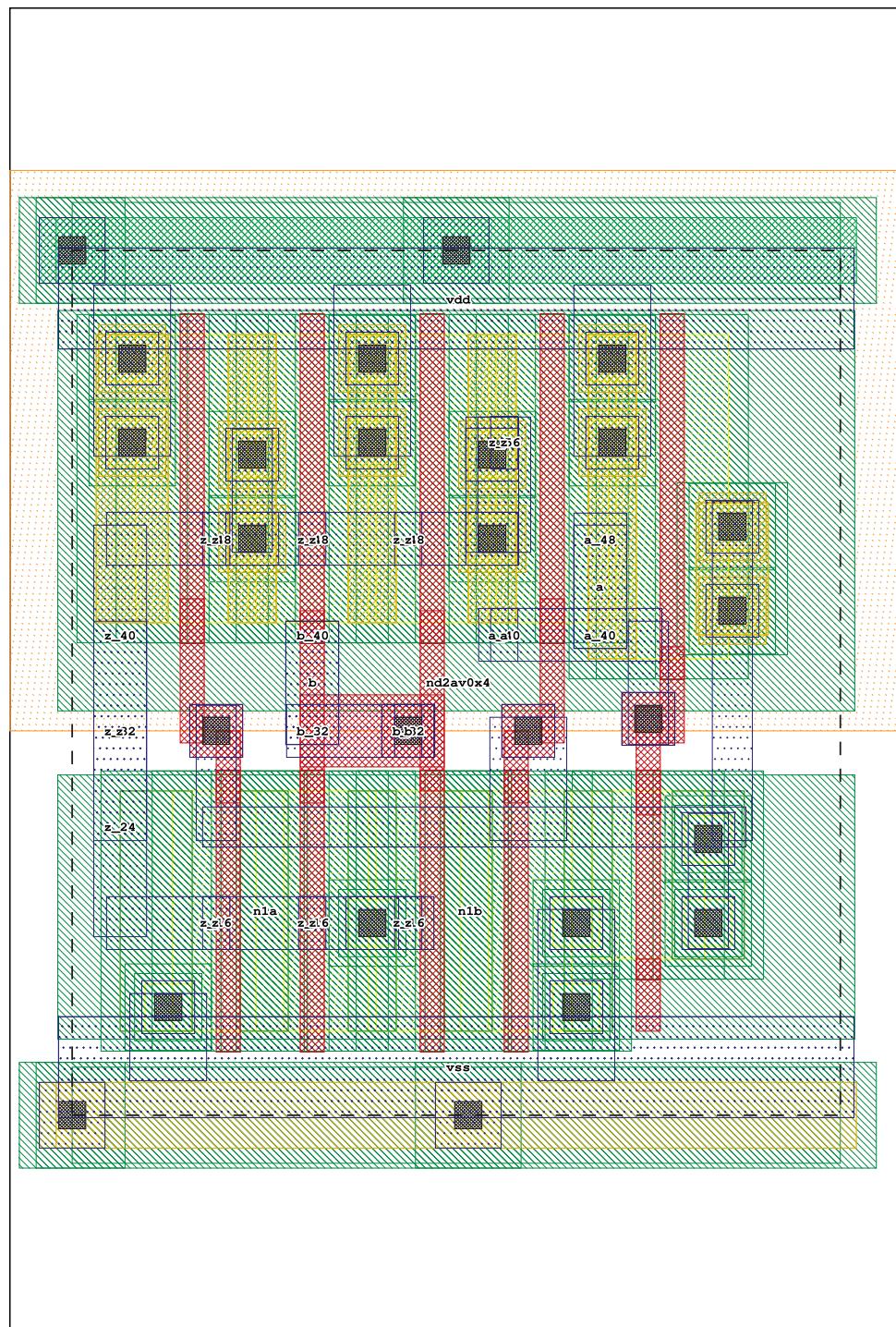
```

ENTITY nd2av0x4 IS
GENERIC (
  CONSTANT area          : NATURAL := 4608;
  CONSTANT cin_b          : NATURAL := 10;
  CONSTANT cin_a          : NATURAL := 6;
  CONSTANT rdown_b_z      : NATURAL := 930;
  CONSTANT rdown_a_z      : NATURAL := 920;
  CONSTANT rup_b_z        : NATURAL := 1230;
  CONSTANT rup_a_z        : NATURAL := 1240;
  CONSTANT tphl_b_z       : NATURAL := 33;
  CONSTANT tplh_b_z       : NATURAL := 43;
  CONSTANT tp11_a_z       : NATURAL := 89;
  CONSTANT tphh_a_z       : NATURAL := 84;
  CONSTANT transistors    : NATURAL := 10
);
PORT (
  b      : in  BIT;
  a      : in  BIT;
  z      : out BIT;
  vdd    : in  BIT;
  vss    : in  BIT
);
END nd2av0x4;

ARCHITECTURE behaviour_data_flow OF nd2av0x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nd2av0x4"
  SEVERITY WARNING;
  z <= (not (b) or a) after 89 ps;
END;

```



3.51 nd2v0x05

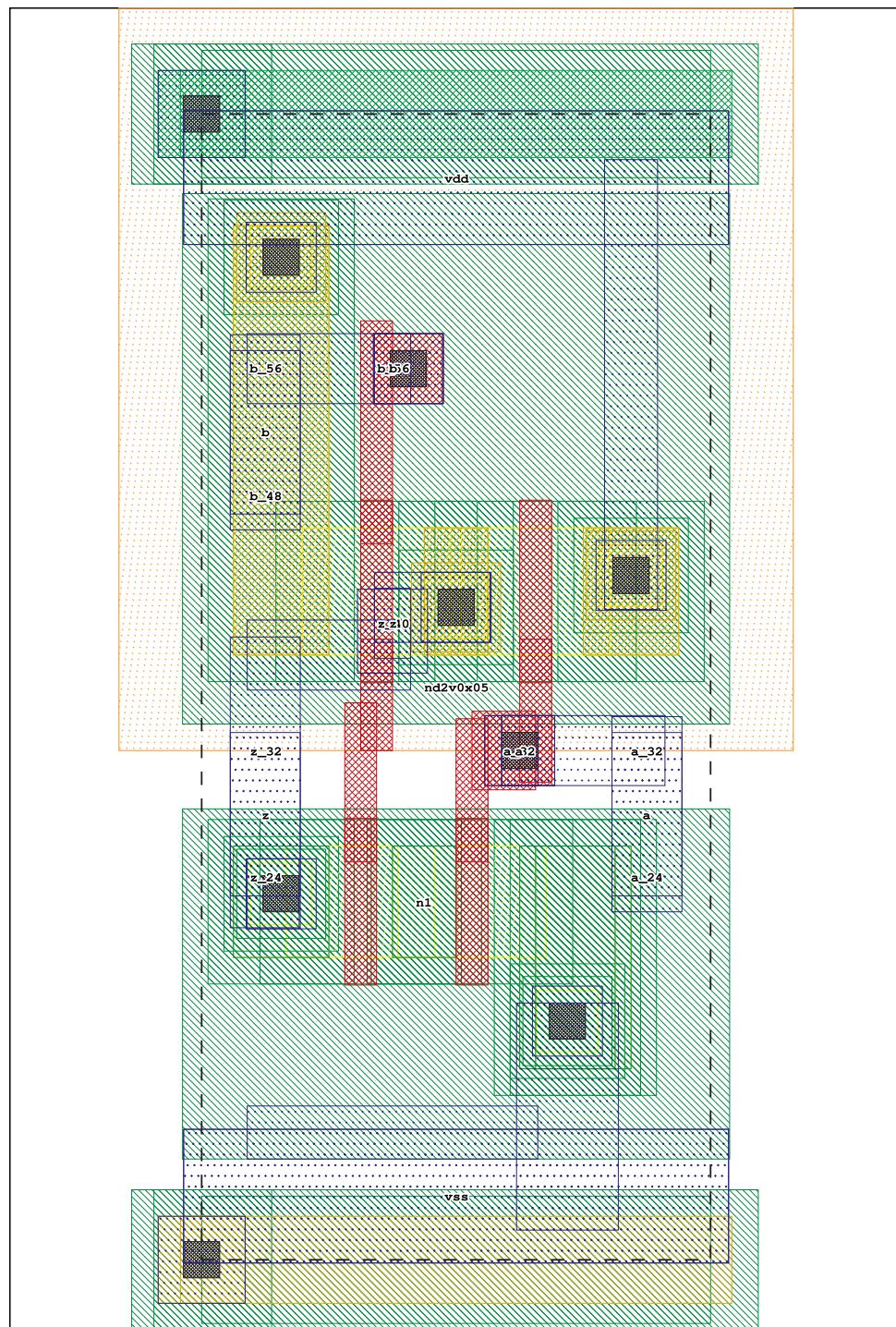
```

ENTITY nd2v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 2;
    CONSTANT cin_b         : NATURAL := 2;
    CONSTANT rdown_a_z    : NATURAL := 5290;
    CONSTANT rdown_b_z    : NATURAL := 5290;
    CONSTANT rup_a_z      : NATURAL := 7390;
    CONSTANT rup_b_z      : NATURAL := 7410;
    CONSTANT tphl_a_z     : NATURAL := 33;
    CONSTANT tphl_b_z     : NATURAL := 34;
    CONSTANT tplh_b_z     : NATURAL := 46;
    CONSTANT tplh_a_z     : NATURAL := 53;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2v0x05;

ARCHITECTURE behaviour_data_flow OF nd2v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2v0x05"
    SEVERITY WARNING;
    z <= not ((a and b)) after 200 ps;
END;

```



3.52 nd2v0x1

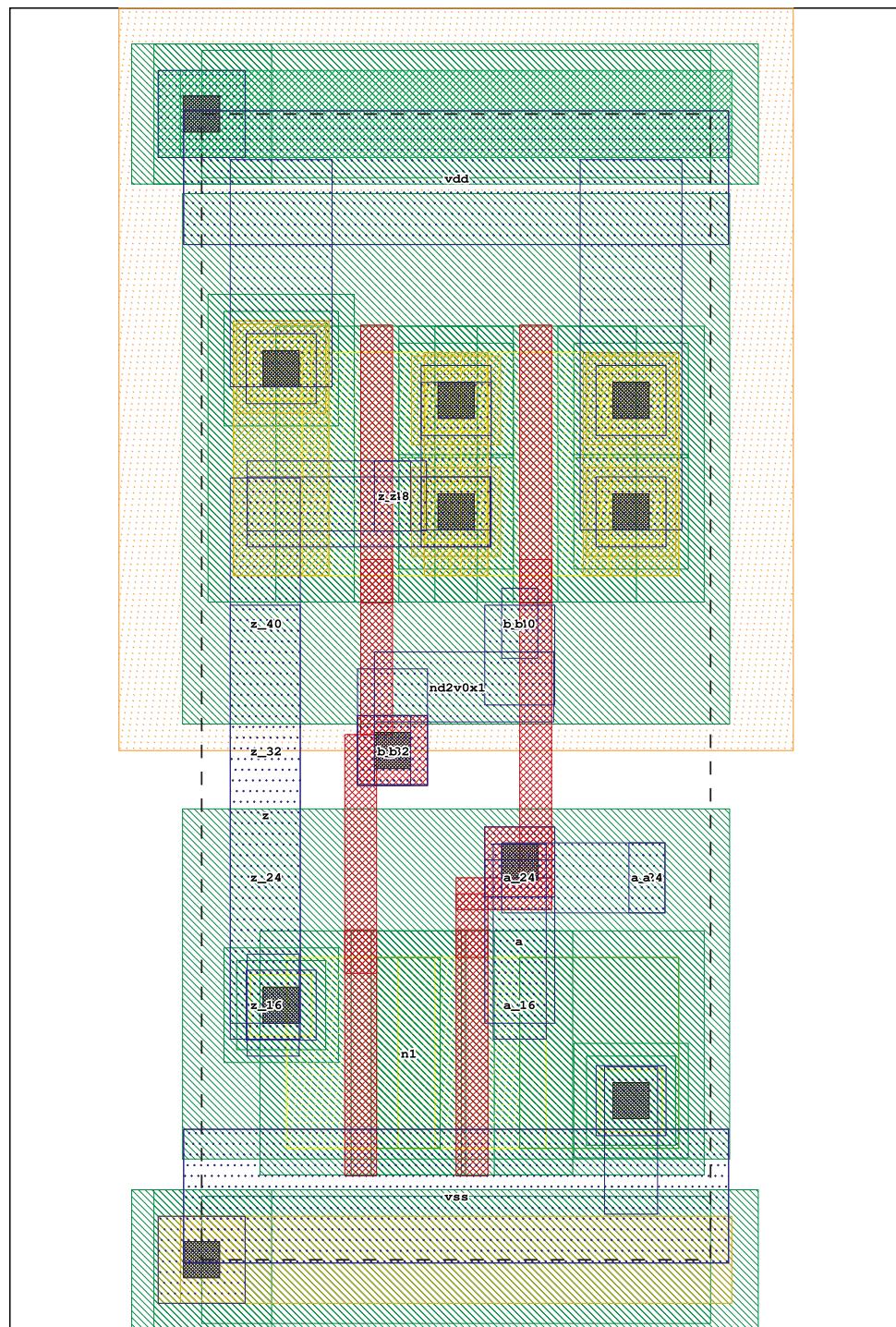
```

ENTITY nd2v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT rdown_a_z     : NATURAL := 3090;
    CONSTANT rdown_b_z     : NATURAL := 3100;
    CONSTANT rup_a_z       : NATURAL := 4220;
    CONSTANT rup_b_z       : NATURAL := 4240;
    CONSTANT tphl_a_z      : NATURAL := 33;
    CONSTANT tphl_b_z      : NATURAL := 34;
    CONSTANT tplh_b_z      : NATURAL := 45;
    CONSTANT tplh_a_z      : NATURAL := 52;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2v0x1;

ARCHITECTURE behaviour_data_flow OF nd2v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2v0x1"
    SEVERITY WARNING;
    z <= not ((a and b)) after 133 ps;
END;

```



3.53 nd2v0x2

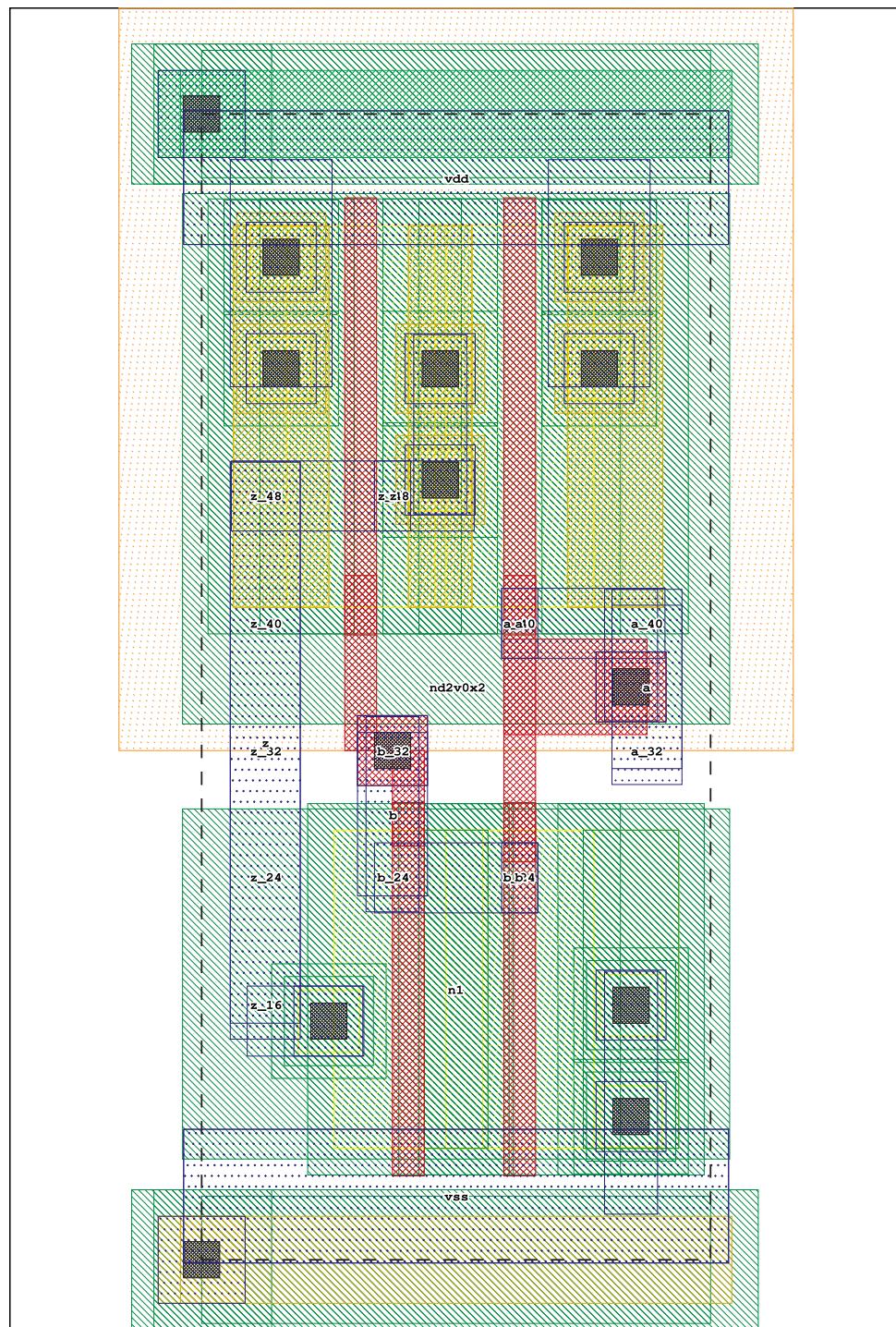
```

ENTITY nd2v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 5;
    CONSTANT cin_b         : NATURAL := 5;
    CONSTANT rdown_a_z     : NATURAL := 1850;
    CONSTANT rdown_b_z     : NATURAL := 1850;
    CONSTANT rup_a_z       : NATURAL := 2460;
    CONSTANT rup_b_z       : NATURAL := 2470;
    CONSTANT tphl_a_z      : NATURAL := 32;
    CONSTANT tphl_b_z      : NATURAL := 34;
    CONSTANT tplh_b_z      : NATURAL := 44;
    CONSTANT tplh_a_z      : NATURAL := 50;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2v0x2;

ARCHITECTURE behaviour_data_flow OF nd2v0x2 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2v0x2"
    SEVERITY WARNING;
    z <= not ((a and b)) after 94 ps;
END;

```



3.54 nd2v0x4

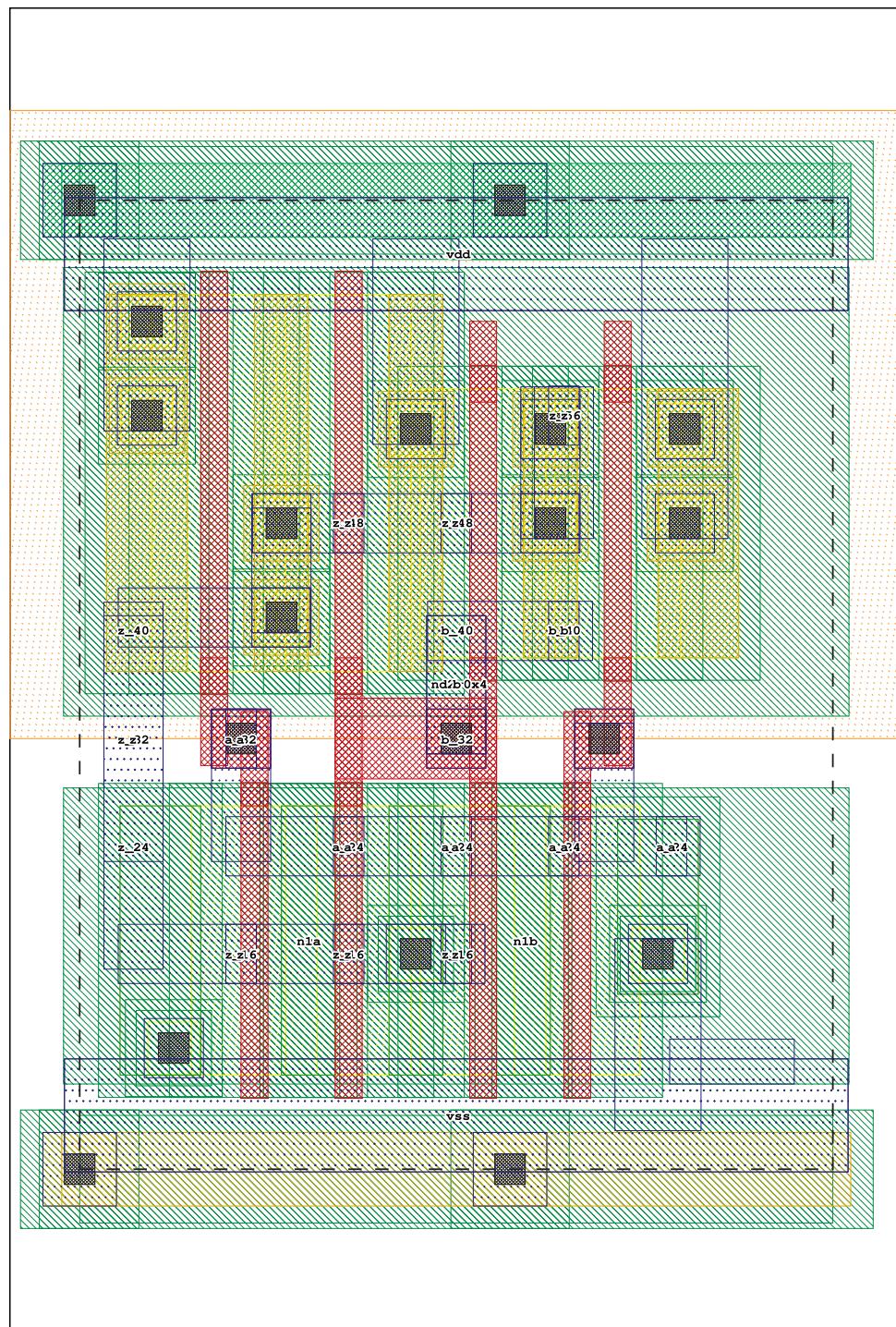
```

ENTITY nd2v0x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 11;
    CONSTANT cin_b         : NATURAL := 10;
    CONSTANT rdown_a_z    : NATURAL := 920;
    CONSTANT rdown_b_z    : NATURAL := 930;
    CONSTANT rup_a_z      : NATURAL := 1230;
    CONSTANT rup_b_z      : NATURAL := 1230;
    CONSTANT tphl_a_z     : NATURAL := 32;
    CONSTANT tphl_b_z     : NATURAL := 33;
    CONSTANT tplh_b_z     : NATURAL := 43;
    CONSTANT tplh_a_z     : NATURAL := 49;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2v0x4;

ARCHITECTURE behaviour_data_flow OF nd2v0x4 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2v0x4"
    SEVERITY WARNING;
    z <= not ((a and b)) after 66 ps;
END;

```



3.55 nd2v3x05

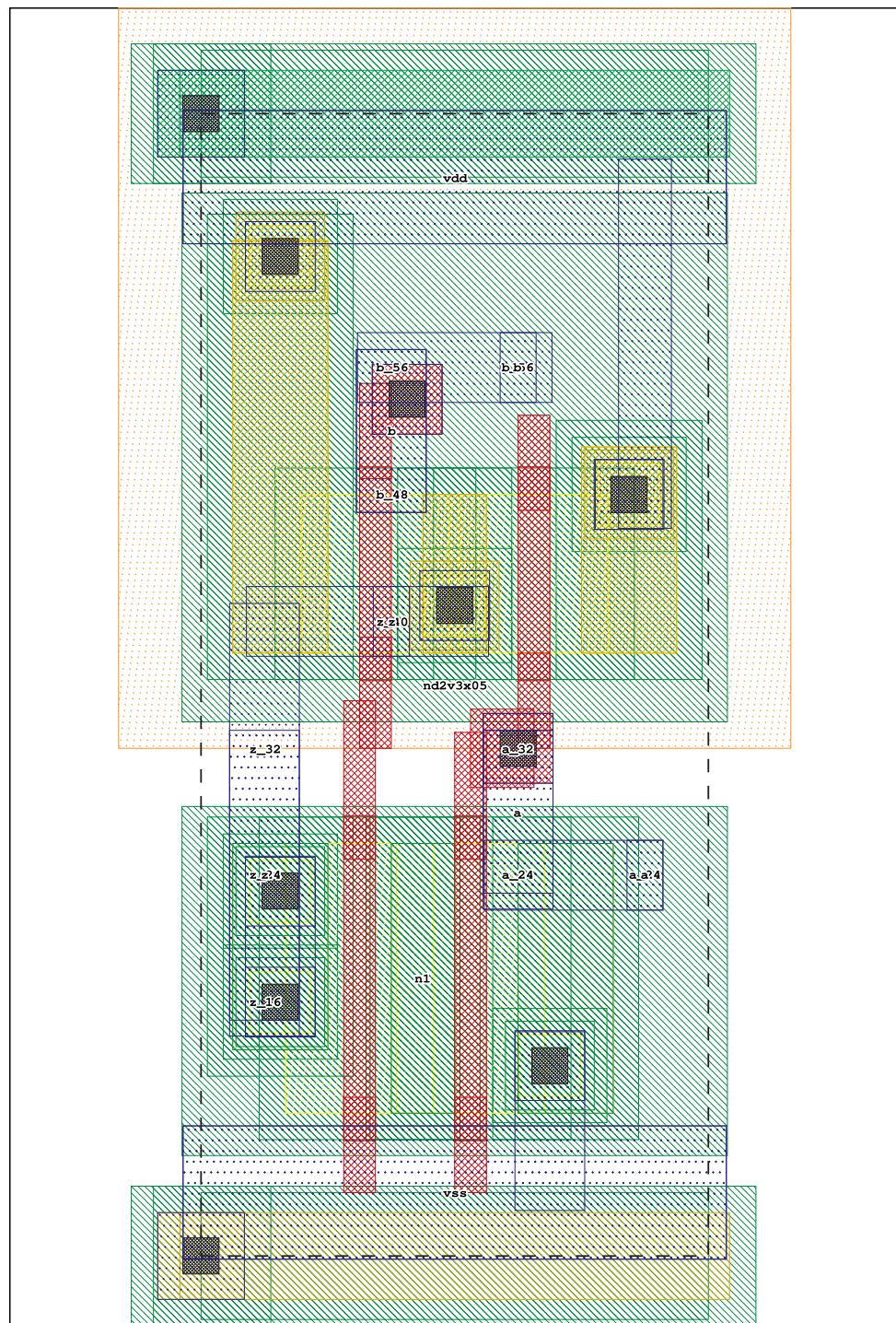
```

ENTITY nd2v3x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT rdown_a_z    : NATURAL := 2250;
    CONSTANT rdown_b_z    : NATURAL := 2310;
    CONSTANT rup_a_z      : NATURAL := 5920;
    CONSTANT rup_b_z      : NATURAL := 5950;
    CONSTANT tphl_a_z     : NATURAL := 26;
    CONSTANT tphl_b_z     : NATURAL := 25;
    CONSTANT tplh_b_z     : NATURAL := 51;
    CONSTANT tplh_a_z     : NATURAL := 65;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2v3x05;

ARCHITECTURE behaviour_data_flow OF nd2v3x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2v3x05"
    SEVERITY WARNING;
    z <= not ((a and b)) after 144 ps;
END;

```



3.56 nd2v5x05

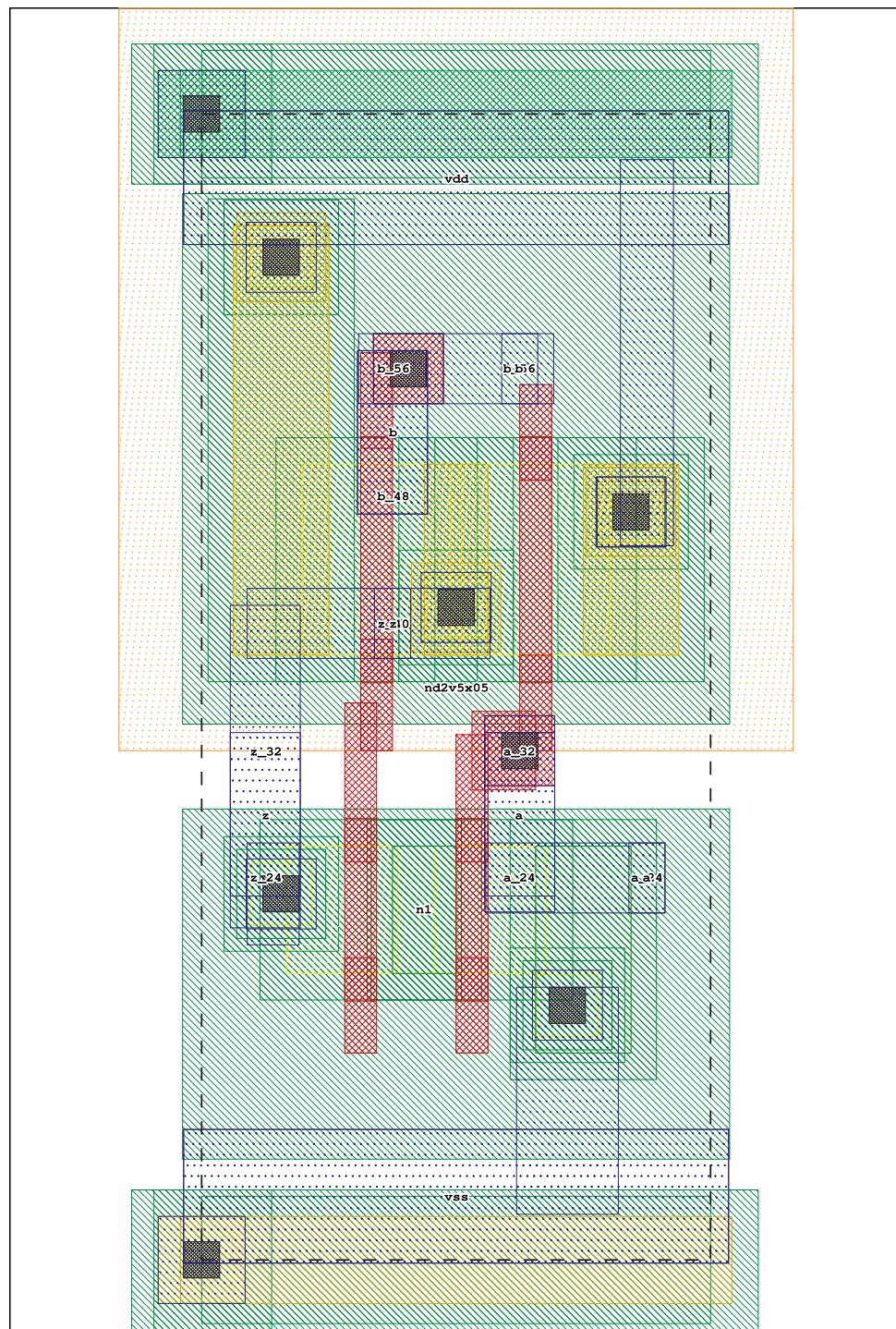
```

ENTITY nd2v5x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT rdown_a_z    : NATURAL := 4610;
    CONSTANT rdown_b_z    : NATURAL := 4610;
    CONSTANT rup_a_z      : NATURAL := 4920;
    CONSTANT rup_b_z      : NATURAL := 4940;
    CONSTANT tphl_a_z     : NATURAL := 36;
    CONSTANT tphl_b_z     : NATURAL := 37;
    CONSTANT tplh_b_z     : NATURAL := 43;
    CONSTANT tplh_a_z     : NATURAL := 48;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd2v5x05;

ARCHITECTURE behaviour_data_flow OF nd2v5x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd2v5x05"
    SEVERITY WARNING;
    z <= not ((a and b)) after 160 ps;
END;

```



3.57 nd3abv0x05

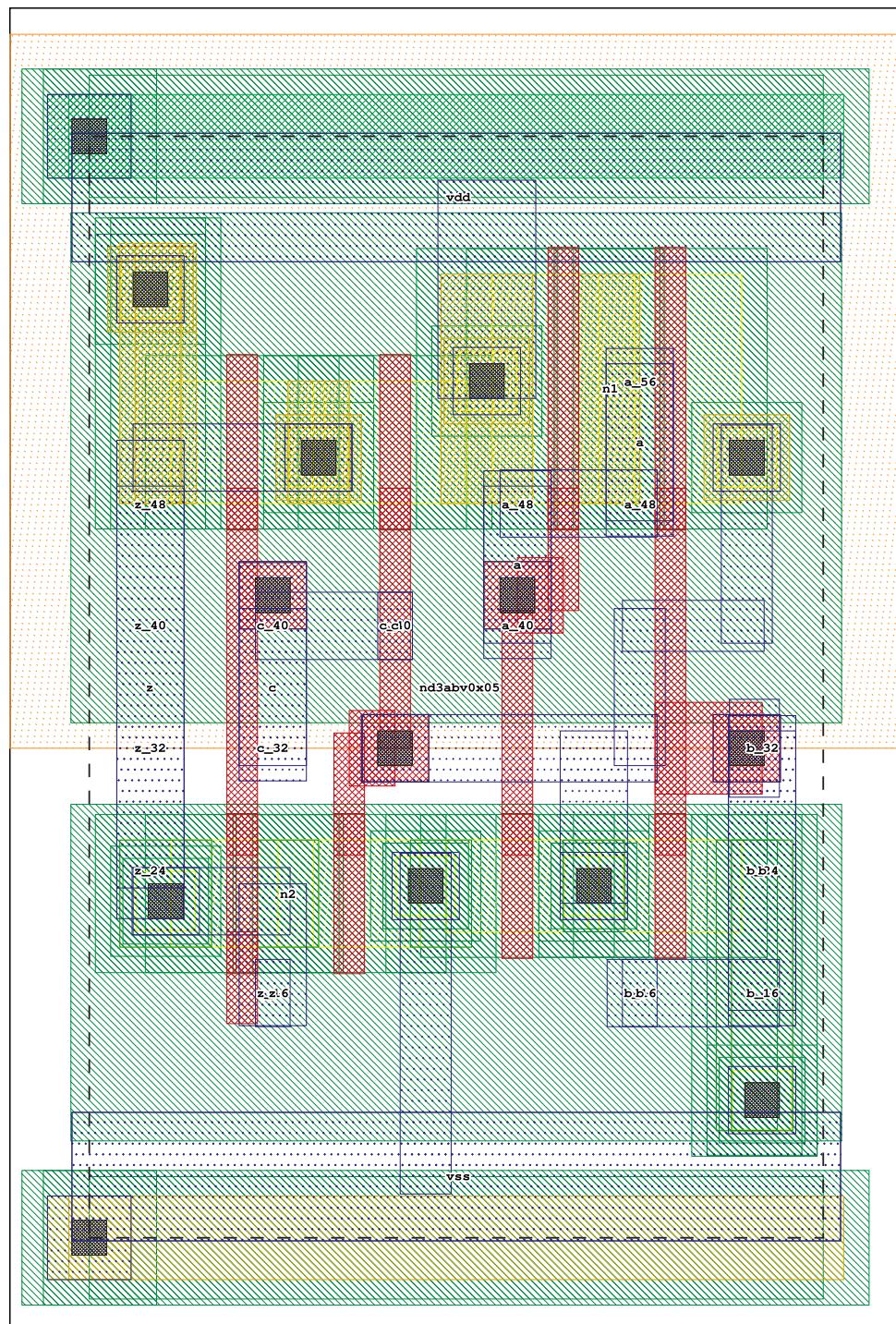
```

ENTITY nd3abv0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 3456;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT cin_c         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 5320;
    CONSTANT rdown_b_z     : NATURAL := 5320;
    CONSTANT rdown_c_z     : NATURAL := 5290;
    CONSTANT rup_a_z       : NATURAL := 7430;
    CONSTANT rup_b_z       : NATURAL := 7420;
    CONSTANT rup_c_z       : NATURAL := 7430;
    CONSTANT tpll_a_z      : NATURAL := 110;
    CONSTANT tpll_b_z      : NATURAL := 100;
    CONSTANT tphl_c_z      : NATURAL := 38;
    CONSTANT tplh_c_z      : NATURAL := 50;
    CONSTANT tphh_b_z      : NATURAL := 84;
    CONSTANT tphh_a_z      : NATURAL := 93;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nd3abv0x05;

ARCHITECTURE behaviour_data_flow OF nd3abv0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on nd3abv0x05"
        SEVERITY WARNING;
    z <= not ((not a and not b) and c) after 238 ps;
END;

```



3.58 nd3av0x05

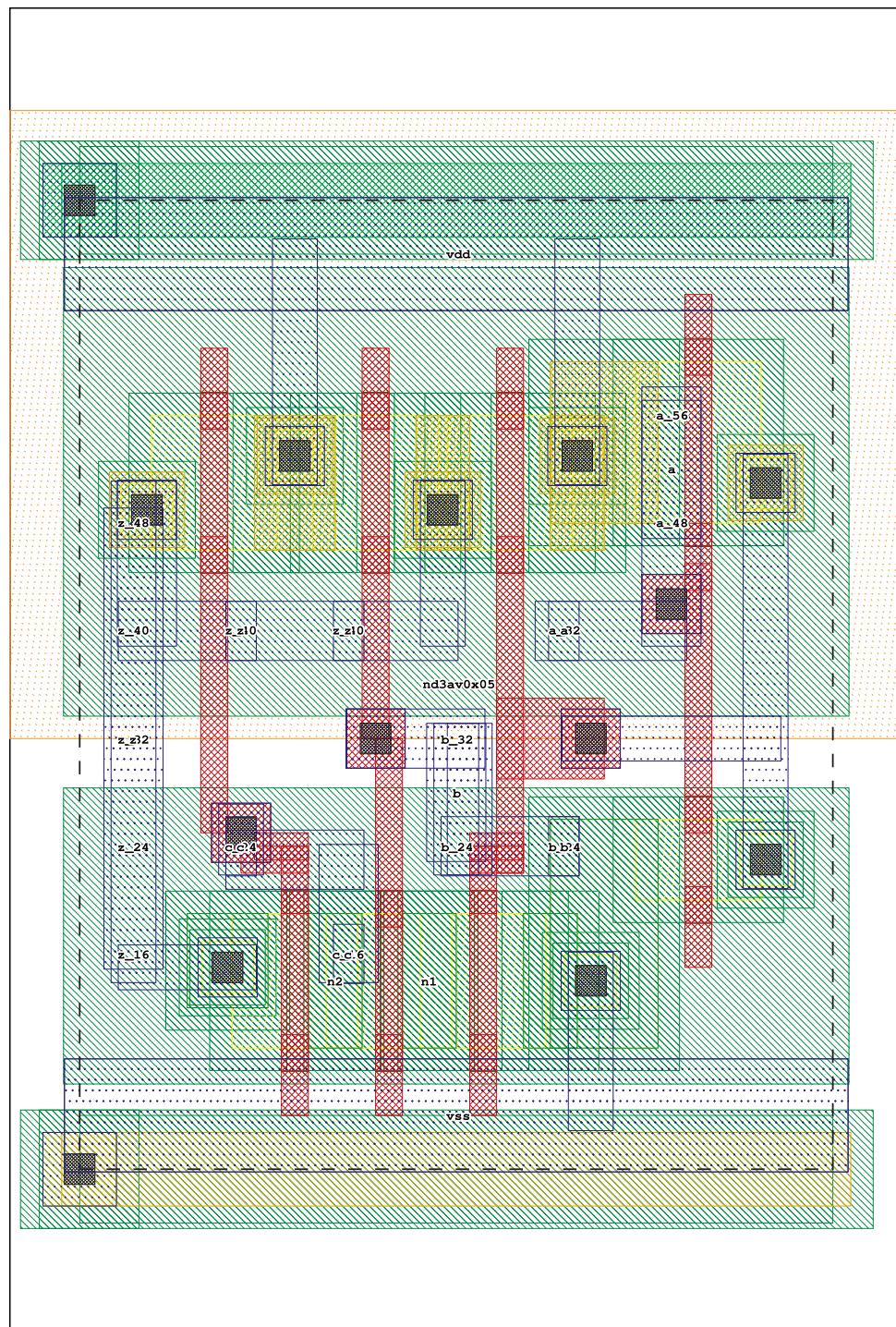
```

ENTITY nd3av0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT cin_c         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 5090;
    CONSTANT rdown_b_z     : NATURAL := 5110;
    CONSTANT rdown_c_z     : NATURAL := 5100;
    CONSTANT rup_a_z       : NATURAL := 5950;
    CONSTANT rup_b_z       : NATURAL := 5930;
    CONSTANT rup_c_z       : NATURAL := 5940;
    CONSTANT tpll_a_z      : NATURAL := 93;
    CONSTANT tphl_b_z      : NATURAL := 45;
    CONSTANT tphl_c_z      : NATURAL := 42;
    CONSTANT tplh_c_z      : NATURAL := 53;
    CONSTANT tplh_b_z      : NATURAL := 61;
    CONSTANT tphh_a_z      : NATURAL := 93;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nd3av0x05;

ARCHITECTURE behaviour_data_flow OF nd3av0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on nd3av0x05"
        SEVERITY WARNING;
    z <= not ((not a and b) and c) after 203 ps;
END;

```



3.59 nd3v0x05

```

ENTITY nd3v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT cin_c         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 5100;
    CONSTANT rdown_b_z     : NATURAL := 5100;
    CONSTANT rdown_c_z     : NATURAL := 5100;
    CONSTANT rup_a_z       : NATURAL := 5940;
    CONSTANT rup_b_z       : NATURAL := 5930;
    CONSTANT rup_c_z       : NATURAL := 5950;
    CONSTANT tphl_a_z      : NATURAL := 46;
    CONSTANT tphl_b_z      : NATURAL := 46;
    CONSTANT tphl_c_z      : NATURAL := 43;
    CONSTANT tplh_c_z      : NATURAL := 54;
    CONSTANT tplh_b_z      : NATURAL := 62;
    CONSTANT tplh_a_z      : NATURAL := 68;
    CONSTANT transistors   : NATURAL := 6
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nd3v0x05;

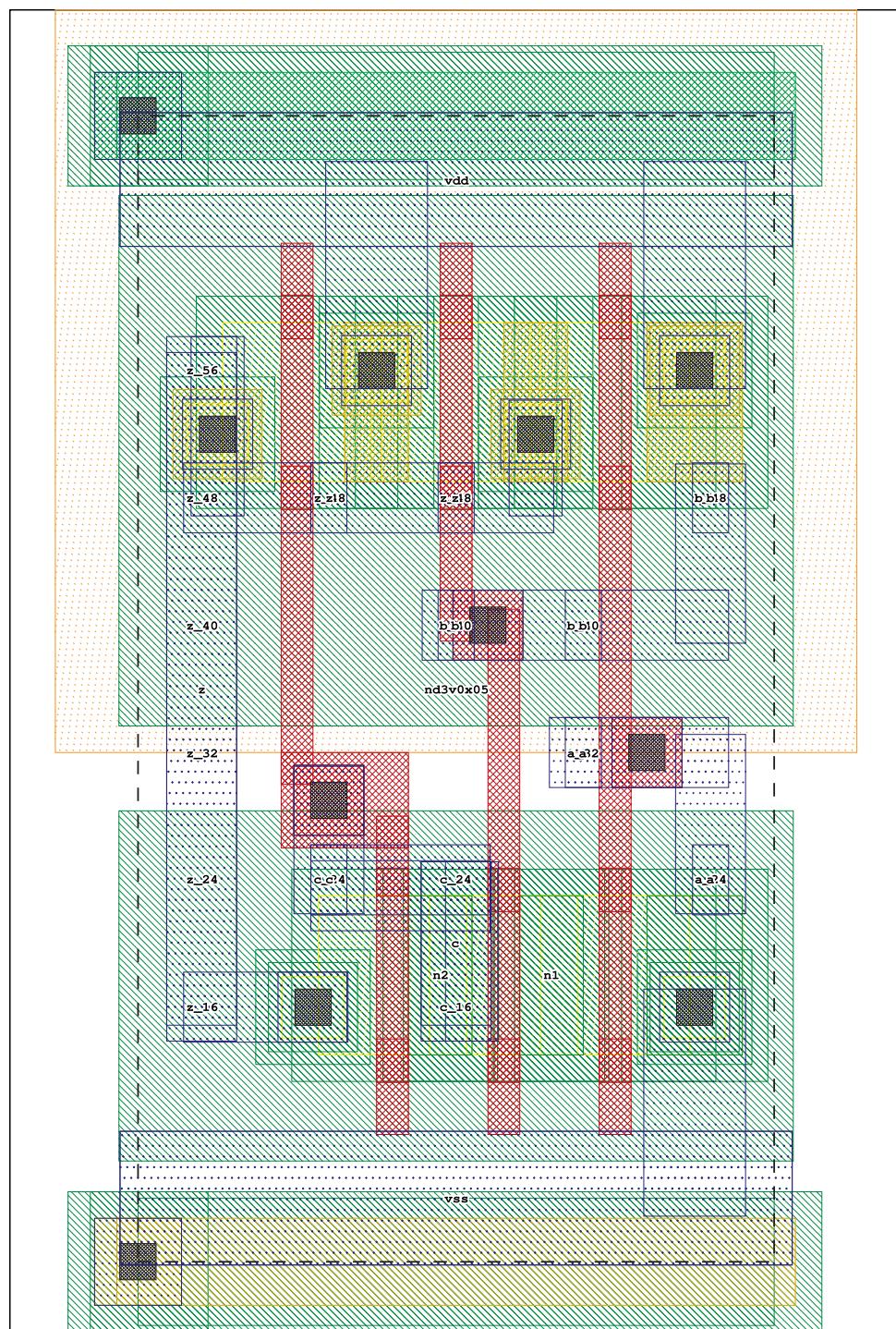
```

```

ARCHITECTURE behaviour_data_flow OF nd3v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd3v0x05"
    SEVERITY WARNING;
    z <= not (((a and b) and c)) after 191 ps;
END;

```



3.60 nd3v0x1

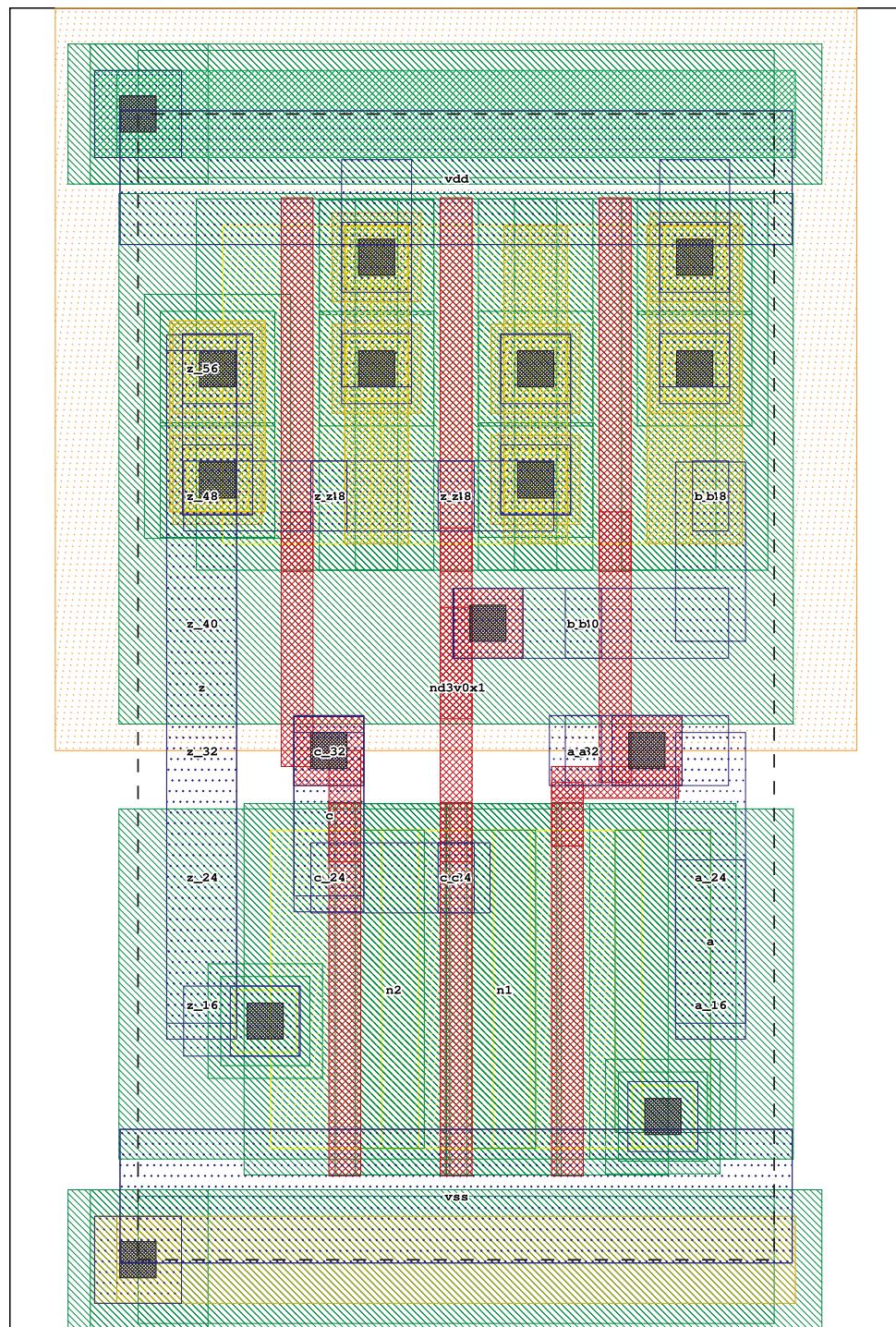
```

ENTITY nd3v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_a          : NATURAL := 5;
    CONSTANT cin_b          : NATURAL := 5;
    CONSTANT cin_c          : NATURAL := 5;
    CONSTANT rdown_a_z      : NATURAL := 2550;
    CONSTANT rdown_b_z      : NATURAL := 2550;
    CONSTANT rdown_c_z      : NATURAL := 2550;
    CONSTANT rup_a_z         : NATURAL := 2970;
    CONSTANT rup_b_z         : NATURAL := 2960;
    CONSTANT rup_c_z         : NATURAL := 2970;
    CONSTANT tphl_a_z        : NATURAL := 43;
    CONSTANT tphl_b_z        : NATURAL := 42;
    CONSTANT tphl_c_z        : NATURAL := 39;
    CONSTANT tplh_c_z        : NATURAL := 50;
    CONSTANT tplh_b_z        : NATURAL := 58;
    CONSTANT tplh_a_z        : NATURAL := 64;
    CONSTANT transistors     : NATURAL := 6
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nd3v0x1;

ARCHITECTURE behaviour_data_flow OF nd3v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd3v0x1"
    SEVERITY WARNING;
    z <= not (((a and b) and c)) after 118 ps;
END;

```



3.61 nd4v0x05

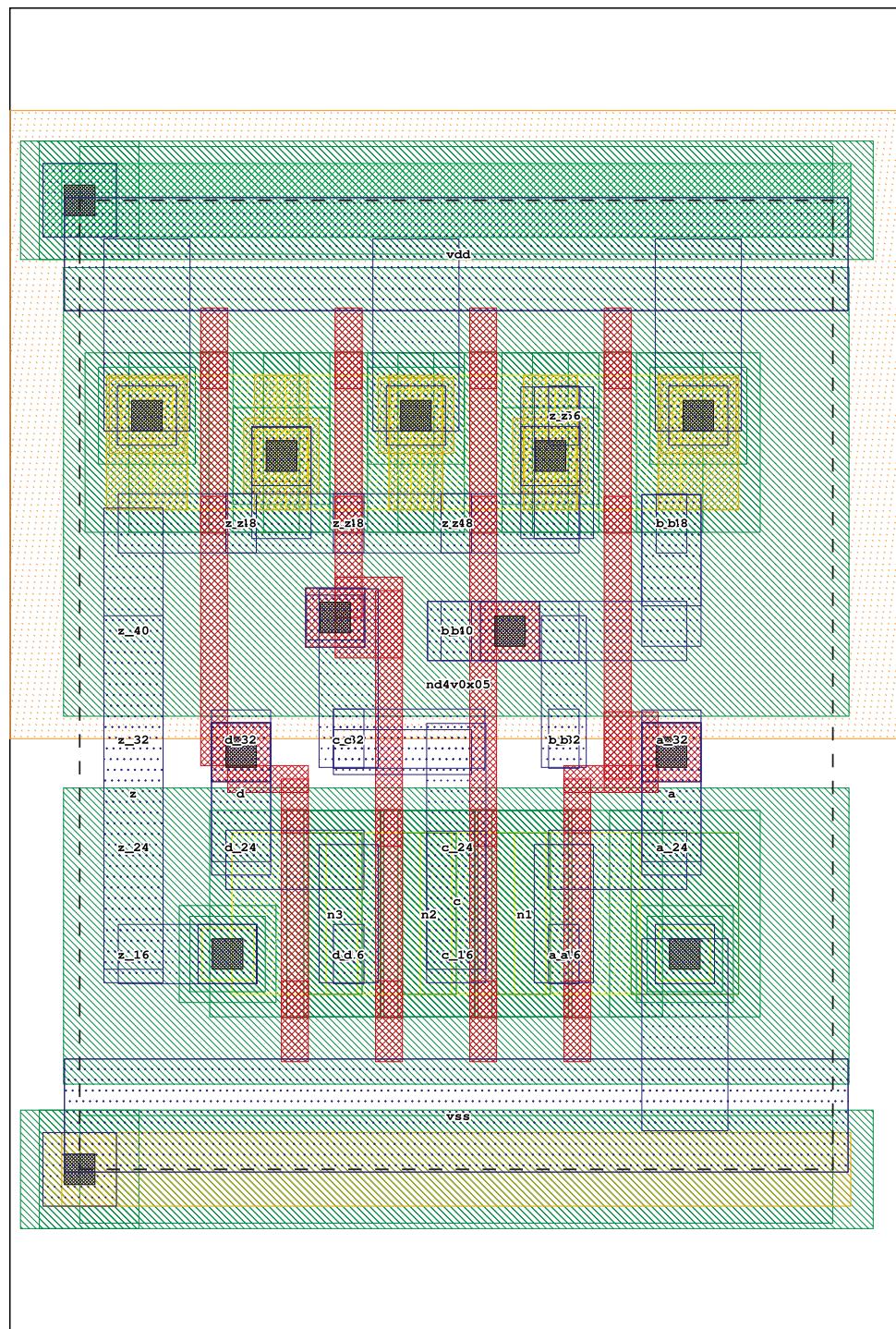
```

ENTITY nd4v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 4;
    CONSTANT cin_d         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 5440;
    CONSTANT rdown_b_z     : NATURAL := 5440;
    CONSTANT rdown_c_z     : NATURAL := 5440;
    CONSTANT rdown_d_z     : NATURAL := 5430;
    CONSTANT rup_a_z       : NATURAL := 5990;
    CONSTANT rup_b_z       : NATURAL := 5960;
    CONSTANT rup_c_z       : NATURAL := 5950;
    CONSTANT rup_d_z       : NATURAL := 5960;
    CONSTANT tphl_a_z      : NATURAL := 59;
    CONSTANT tphl_b_z      : NATURAL := 58;
    CONSTANT tphl_c_z      : NATURAL := 52;
    CONSTANT tphl_d_z      : NATURAL := 46;
    CONSTANT tplh_d_z      : NATURAL := 59;
    CONSTANT tplh_c_z      : NATURAL := 69;
    CONSTANT tplh_b_z      : NATURAL := 78;
    CONSTANT tplh_a_z      : NATURAL := 84;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    d      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd4v0x05;

ARCHITECTURE behaviour_data_flow OF nd4v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on nd4v0x05"
        SEVERITY WARNING;
    z <= not (((a and b) and c) and d)) after 206 ps;
END;

```



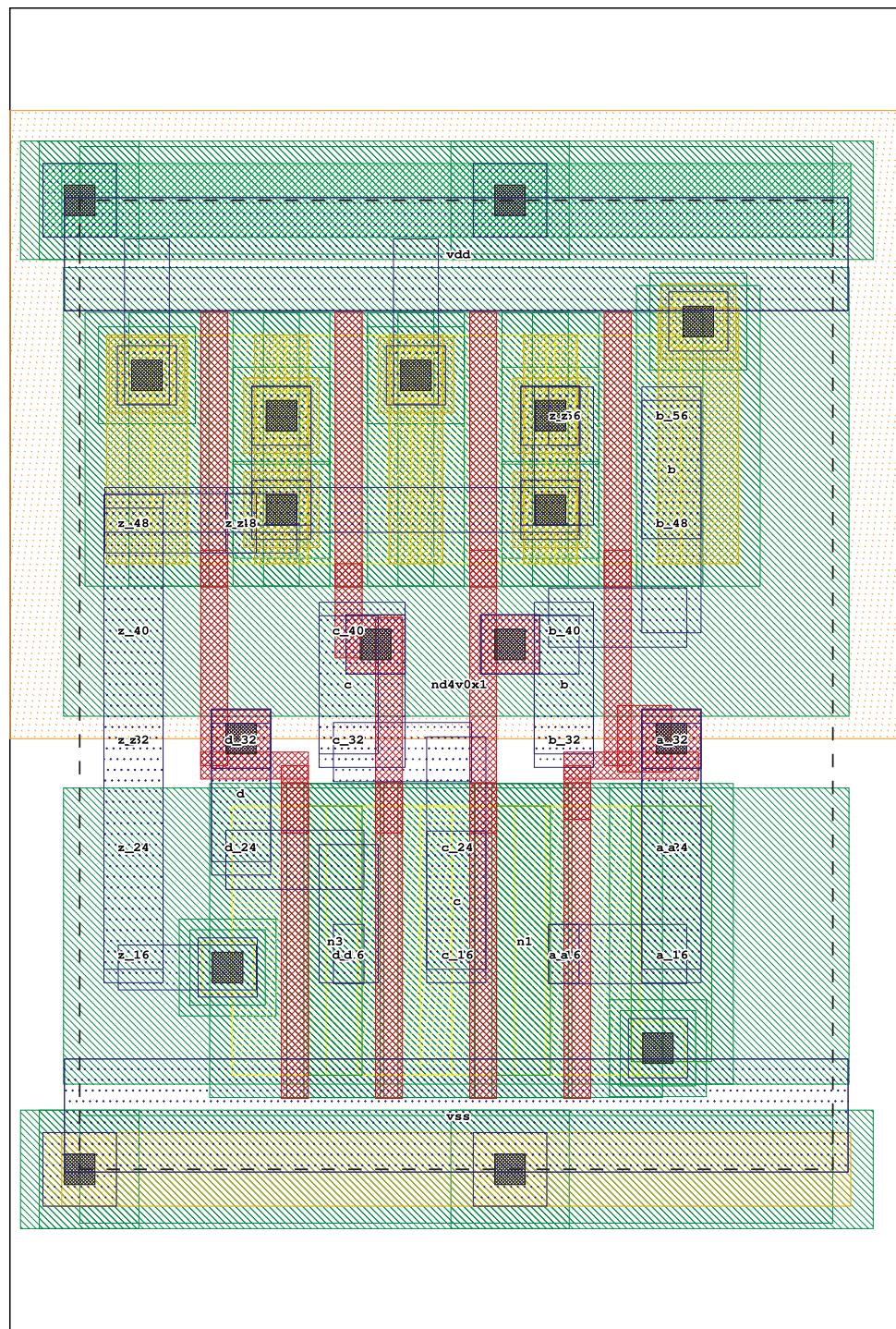
3.62 nd4v0x1

```

ENTITY nd4v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 5;
    CONSTANT cin_b         : NATURAL := 5;
    CONSTANT cin_c         : NATURAL := 5;
    CONSTANT cin_d         : NATURAL := 5;
    CONSTANT rdown_a_z     : NATURAL := 3260;
    CONSTANT rdown_b_z     : NATURAL := 3270;
    CONSTANT rdown_c_z     : NATURAL := 3270;
    CONSTANT rdown_d_z     : NATURAL := 3260;
    CONSTANT rup_a_z       : NATURAL := 3520;
    CONSTANT rup_b_z       : NATURAL := 3500;
    CONSTANT rup_c_z       : NATURAL := 3500;
    CONSTANT rup_d_z       : NATURAL := 3500;
    CONSTANT tphl_a_z      : NATURAL := 56;
    CONSTANT tphl_b_z      : NATURAL := 54;
    CONSTANT tphl_c_z      : NATURAL := 49;
    CONSTANT tphl_d_z      : NATURAL := 42;
    CONSTANT tplh_d_z      : NATURAL := 55;
    CONSTANT tplh_c_z      : NATURAL := 64;
    CONSTANT tplh_b_z      : NATURAL := 73;
    CONSTANT tplh_a_z      : NATURAL := 79;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    d      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd4v0x1;

ARCHITECTURE behaviour_data_flow OF nd4v0x1 IS
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on nd4v0x1"
        SEVERITY WARNING;
    z <= not (((a and b) and c) and d)) after 144 ps;
END;

```



3.63 nd4v0x2

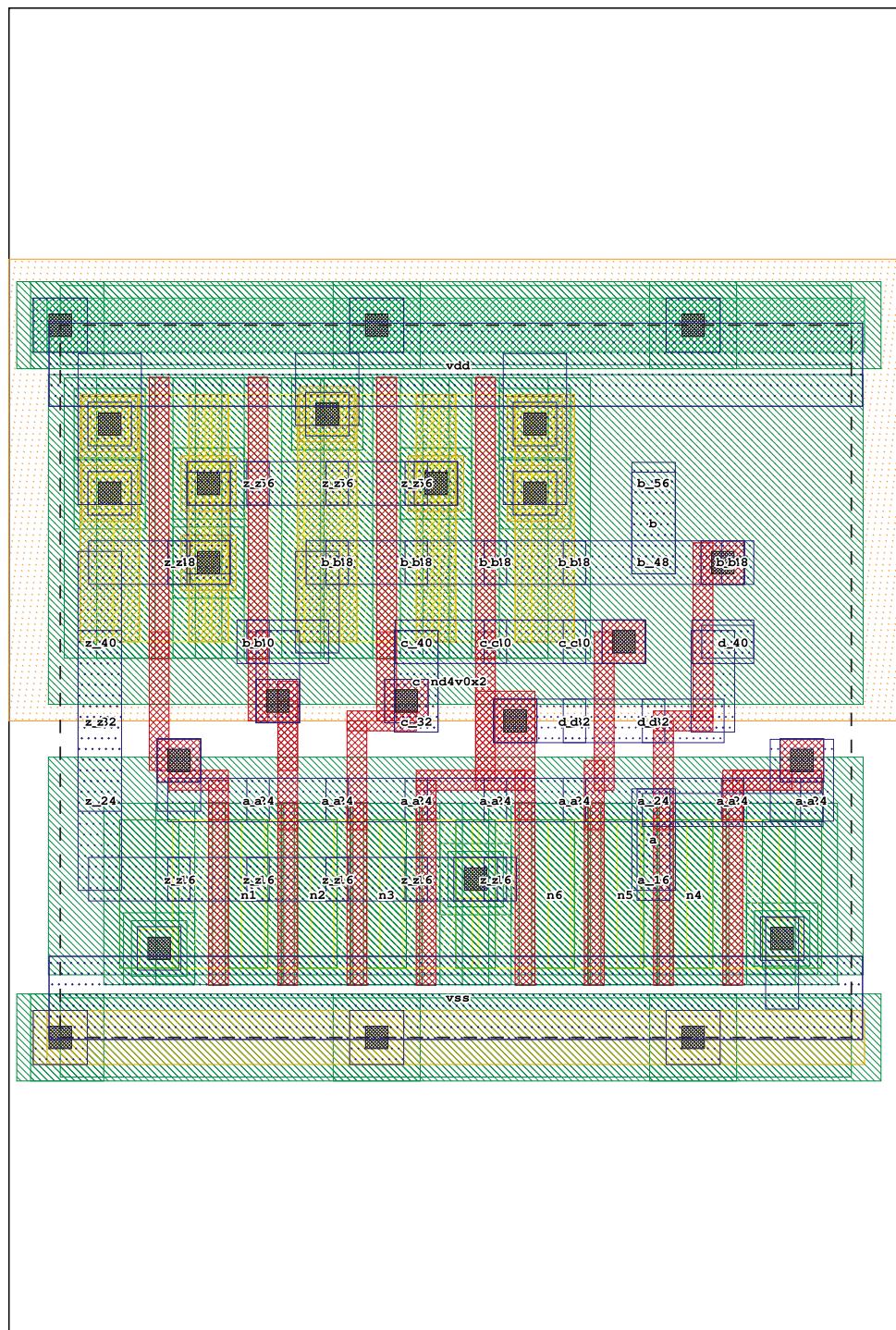
```

ENTITY nd4v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 5760;
    CONSTANT cin_a          : NATURAL := 8;
    CONSTANT cin_b          : NATURAL := 8;
    CONSTANT cin_c          : NATURAL := 7;
    CONSTANT cin_d          : NATURAL := 7;
    CONSTANT rdown_a_z      : NATURAL := 2180;
    CONSTANT rdown_b_z      : NATURAL := 2180;
    CONSTANT rdown_c_z      : NATURAL := 2180;
    CONSTANT rdown_d_z      : NATURAL := 2170;
    CONSTANT rup_a_z        : NATURAL := 2400;
    CONSTANT rup_b_z        : NATURAL := 2380;
    CONSTANT rup_c_z        : NATURAL := 2380;
    CONSTANT rup_d_z        : NATURAL := 2380;
    CONSTANT tphl_a_z       : NATURAL := 56;
    CONSTANT tphl_b_z       : NATURAL := 53;
    CONSTANT tphl_c_z       : NATURAL := 47;
    CONSTANT tphl_d_z       : NATURAL := 40;
    CONSTANT tplh_d_z       : NATURAL := 53;
    CONSTANT tplh_c_z       : NATURAL := 63;
    CONSTANT tplh_b_z       : NATURAL := 72;
    CONSTANT tplh_a_z       : NATURAL := 80;
    CONSTANT transistors    : NATURAL := 12
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    d      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nd4v0x2;

ARCHITECTURE behaviour_data_flow OF nd4v0x2 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nd4v0x2"
    SEVERITY WARNING;
    z <= not (((a and b) and c) and d)) after 115 ps;
END;

```



3.64 nr2av0x1

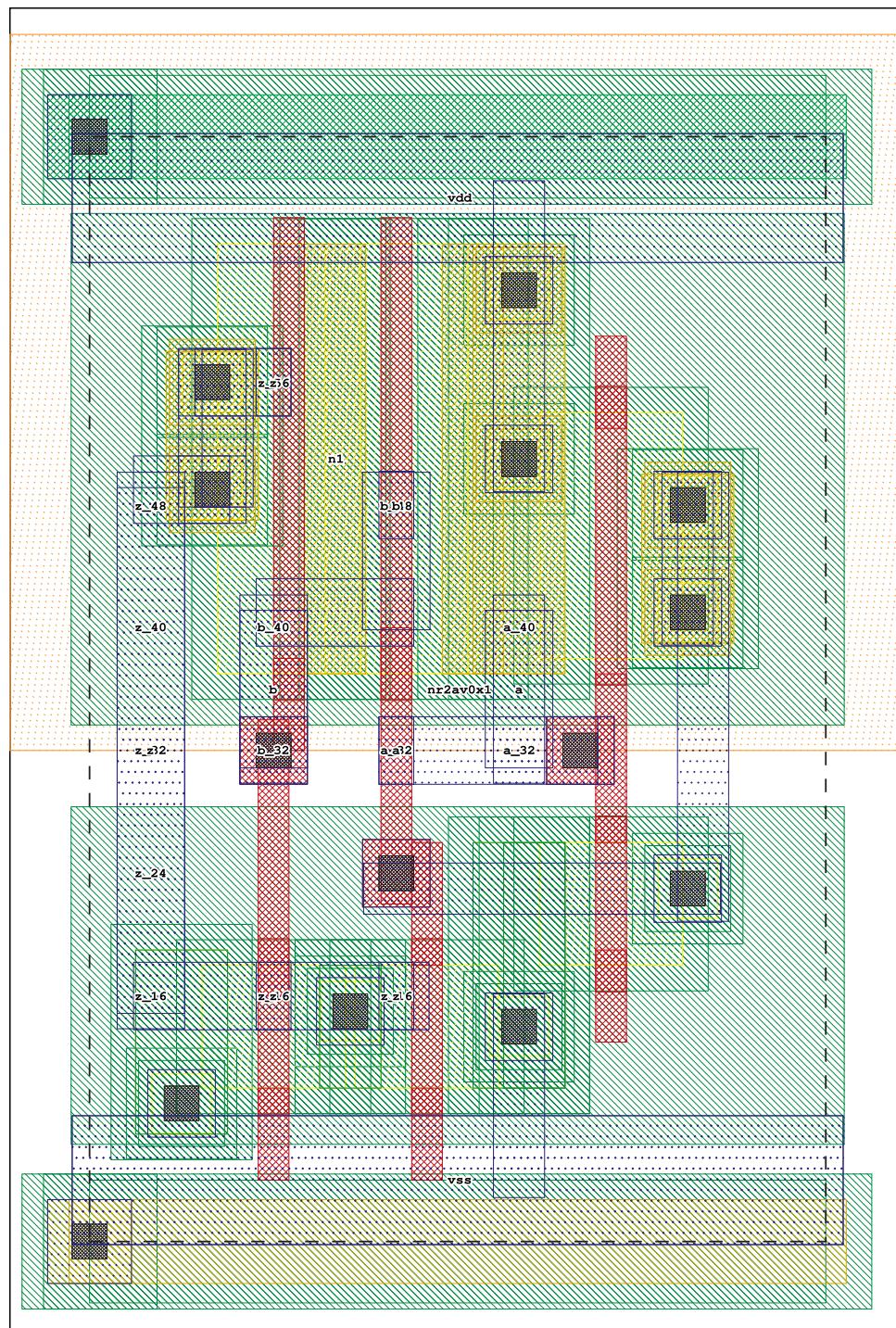
```

ENTITY nr2av0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 3456;
    CONSTANT cin_b          : NATURAL := 5;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT rdown_b_z      : NATURAL := 2890;
    CONSTANT rdown_a_z      : NATURAL := 2900;
    CONSTANT rup_b_z        : NATURAL := 4150;
    CONSTANT rup_a_z        : NATURAL := 4160;
    CONSTANT tplh_b_z       : NATURAL := 45;
    CONSTANT tphl_b_z       : NATURAL := 41;
    CONSTANT tphh_a_z       : NATURAL := 83;
    CONSTANT tpll_a_z       : NATURAL := 95;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr2av0x1;

ARCHITECTURE behaviour_data_flow OF nr2av0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr2av0x1"
    SEVERITY WARNING;
    z <= (not (b) and a) after 154 ps;
END;

```



3.65 nr2av0x2

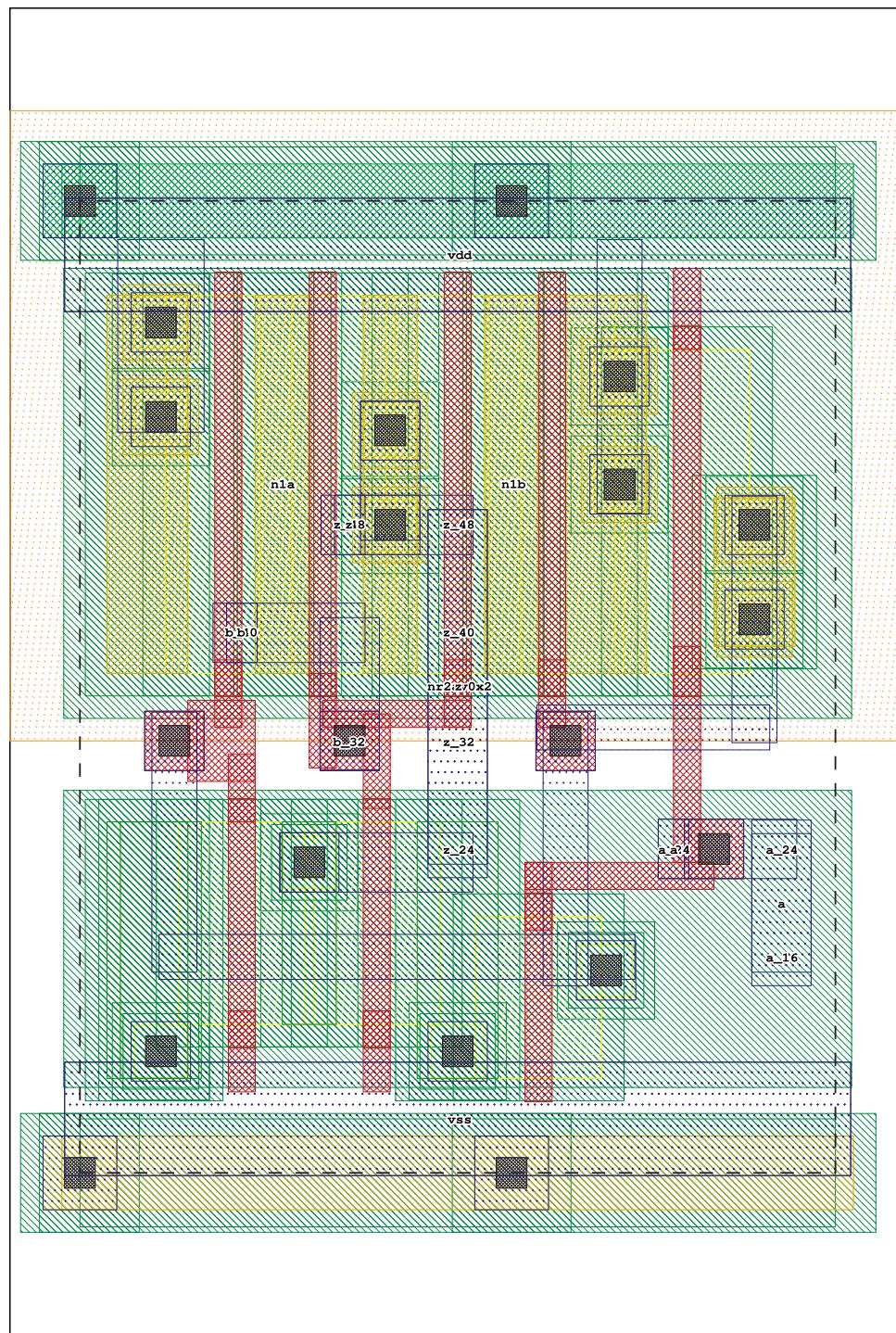
```

ENTITY nr2av0x2 IS
GENERIC (
  CONSTANT area          : NATURAL := 4032;
  CONSTANT cin_b          : NATURAL := 8;
  CONSTANT cin_a          : NATURAL := 5;
  CONSTANT rdown_b_z      : NATURAL := 1550;
  CONSTANT rdown_a_z      : NATURAL := 1550;
  CONSTANT rup_b_z        : NATURAL := 2080;
  CONSTANT rup_a_z        : NATURAL := 2080;
  CONSTANT tplh_b_z       : NATURAL := 41;
  CONSTANT tphl_b_z       : NATURAL := 39;
  CONSTANT tphh_a_z       : NATURAL := 85;
  CONSTANT tpll_a_z       : NATURAL := 101;
  CONSTANT transistors    : NATURAL := 6
);
PORT (
  b      : in  BIT;
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END nr2av0x2;

ARCHITECTURE behaviour_data_flow OF nr2av0x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nr2av0x2"
  SEVERITY WARNING;
  z <= (not (b) and a) after 112 ps;
END;

```



3.66 nr2av0x4

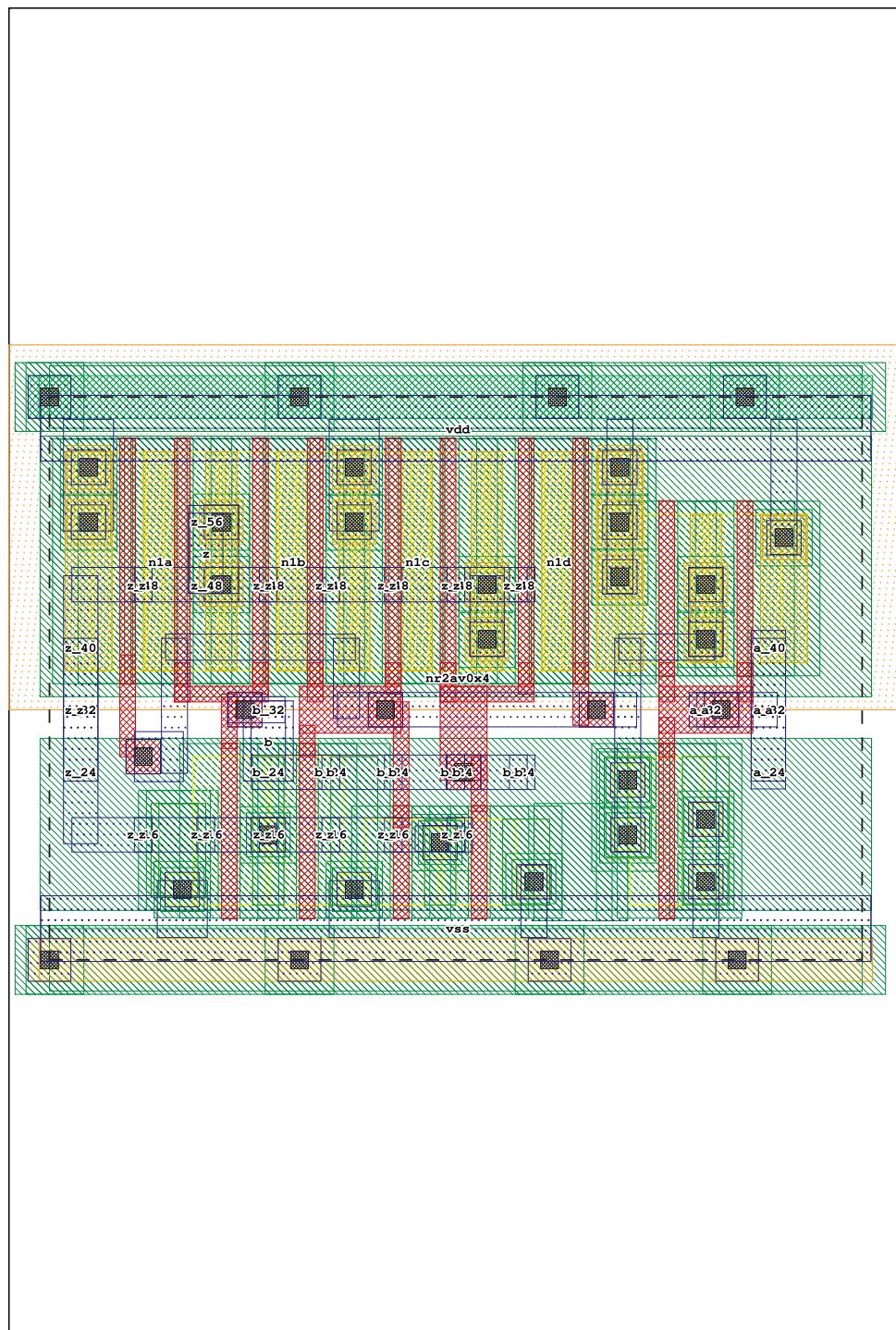
```

ENTITY nr2av0x4 IS
GENERIC (
  CONSTANT area          : NATURAL := 7488;
  CONSTANT cin_b          : NATURAL := 16;
  CONSTANT cin_a          : NATURAL := 7;
  CONSTANT rdown_b_z      : NATURAL := 770;
  CONSTANT rdown_a_z      : NATURAL := 780;
  CONSTANT rup_b_z        : NATURAL := 1040;
  CONSTANT rup_a_z        : NATURAL := 1040;
  CONSTANT tplh_b_z       : NATURAL := 41;
  CONSTANT tphl_b_z       : NATURAL := 39;
  CONSTANT tphh_a_z       : NATURAL := 89;
  CONSTANT tpll_a_z       : NATURAL := 107;
  CONSTANT transistors    : NATURAL := 15
);
PORT (
  b      : in  BIT;
  a      : in  BIT;
  z      : out BIT;
  vdd   : in  BIT;
  vss   : in  BIT
);
END nr2av0x4;

ARCHITECTURE behaviour_data_flow OF nr2av0x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nr2av0x4"
  SEVERITY WARNING;
  z <= (not (b) and a) after 92 ps;
END;

```



3.67 nr2av1x05

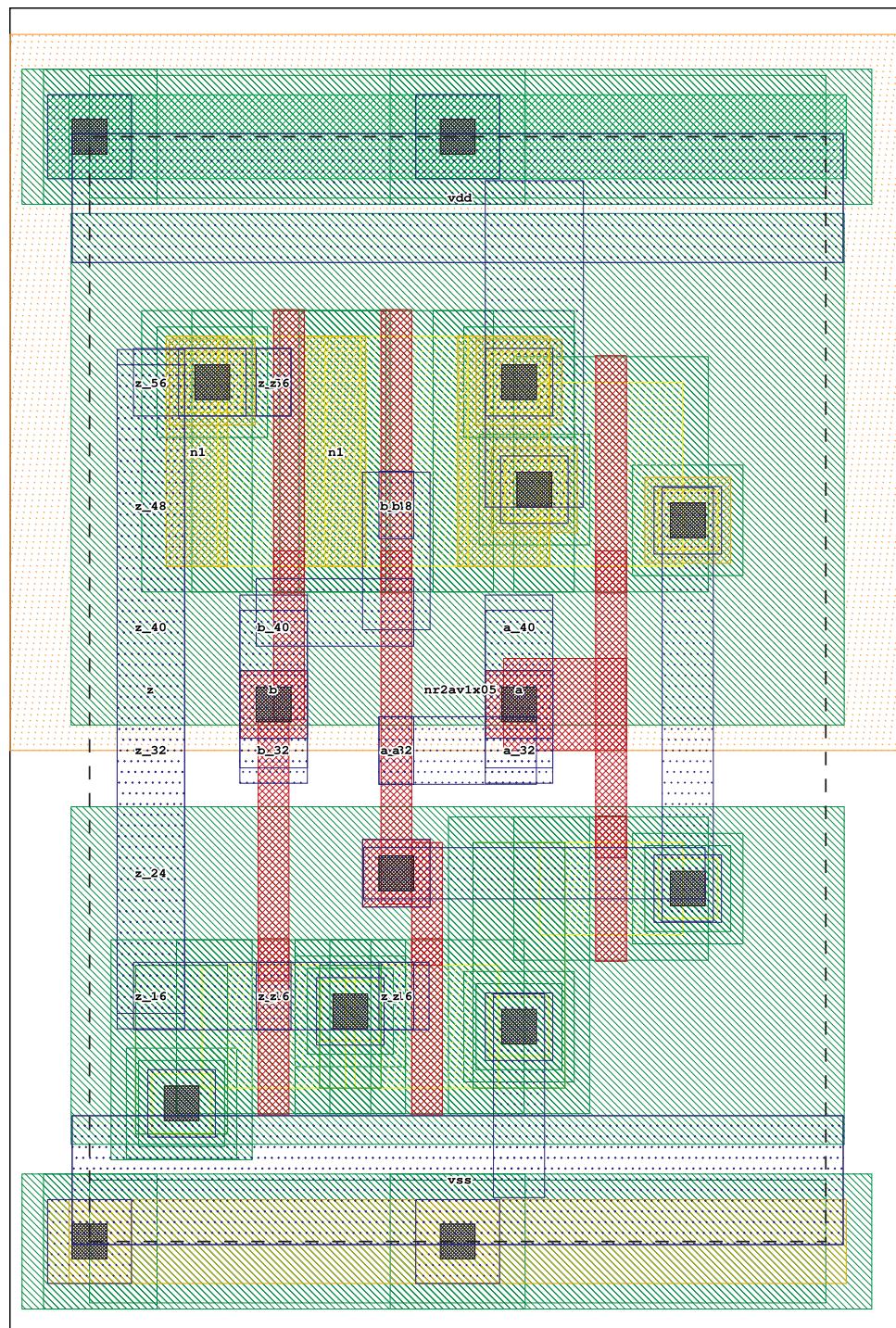
```

ENTITY nr2av1x05 IS
GENERIC (
  CONSTANT area      : NATURAL := 3456;
  CONSTANT cin_b     : NATURAL := 3;
  CONSTANT cin_a     : NATURAL := 3;
  CONSTANT rdown_b_z : NATURAL := 2970;
  CONSTANT rdown_a_z : NATURAL := 2940;
  CONSTANT rup_b_z   : NATURAL := 7760;
  CONSTANT rup_a_z   : NATURAL := 7780;
  CONSTANT tplh_b_z  : NATURAL := 53;
  CONSTANT tphl_b_z  : NATURAL := 34;
  CONSTANT tphh_a_z  : NATURAL := 90;
  CONSTANT tpll_a_z  : NATURAL := 83;
  CONSTANT transistors : NATURAL := 6
);
PORT (
  b      : in  BIT;
  a      : in  BIT;
  z      : out BIT;
  vdd    : in  BIT;
  vss    : in  BIT
);
END nr2av1x05;

ARCHITECTURE behaviour_data_flow OF nr2av1x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nr2av1x05"
  SEVERITY WARNING;
  z <= (not (b) and a) after 199 ps;
END;

```



3.68 nr2v0x05

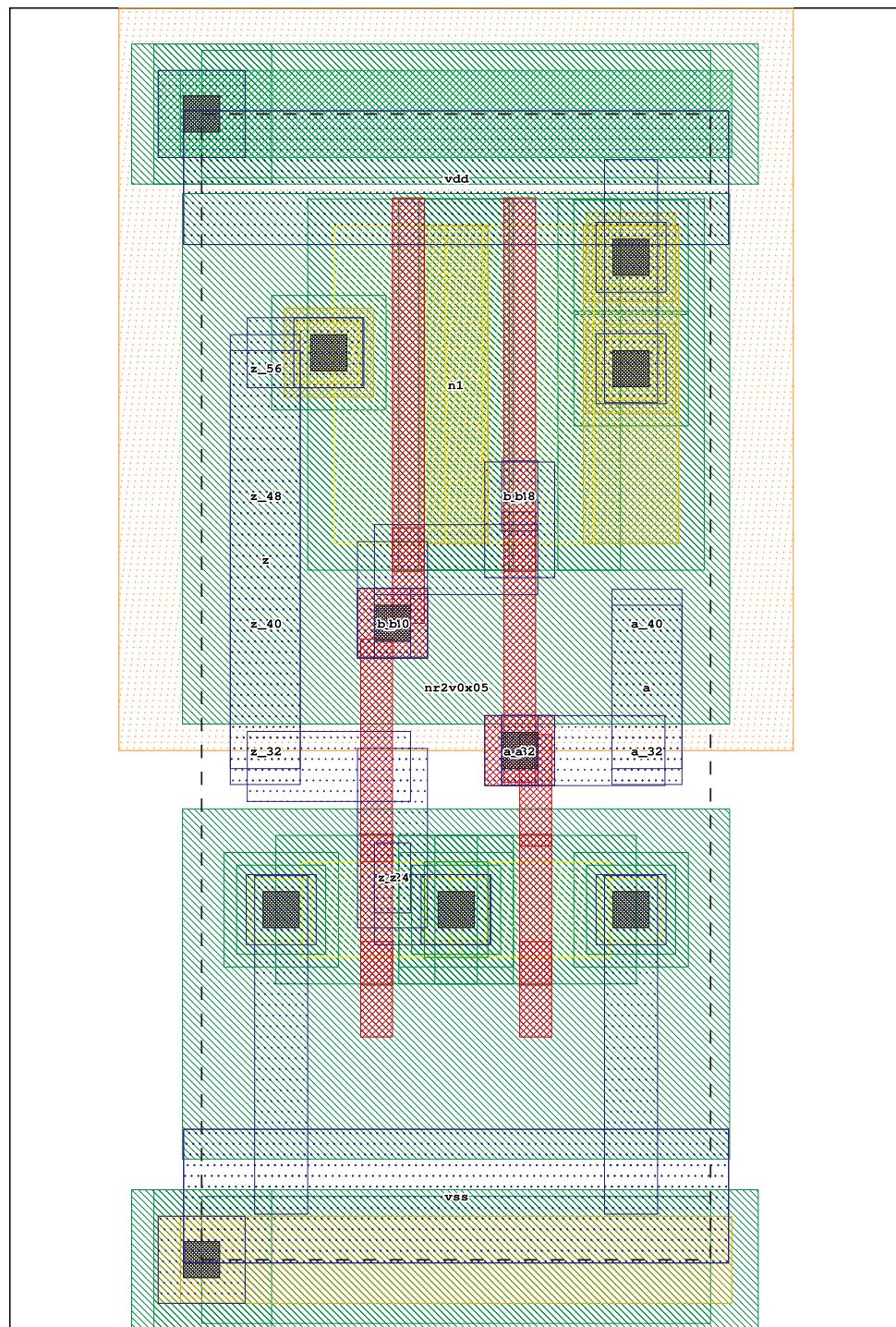
```

ENTITY nr2v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT rdown_a_z     : NATURAL := 3840;
    CONSTANT rdown_b_z     : NATURAL := 3860;
    CONSTANT rup_a_z       : NATURAL := 5820;
    CONSTANT rup_b_z       : NATURAL := 5810;
    CONSTANT tplh_a_z      : NATURAL := 54;
    CONSTANT tplh_b_z      : NATURAL := 46;
    CONSTANT tphl_b_z      : NATURAL := 41;
    CONSTANT tphl_a_z      : NATURAL := 49;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nr2v0x05;

ARCHITECTURE behaviour_data_flow OF nr2v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr2v0x05"
    SEVERITY WARNING;
    z <= not ((a or b)) after 168 ps;
END;

```



3.69 nr2v0x1

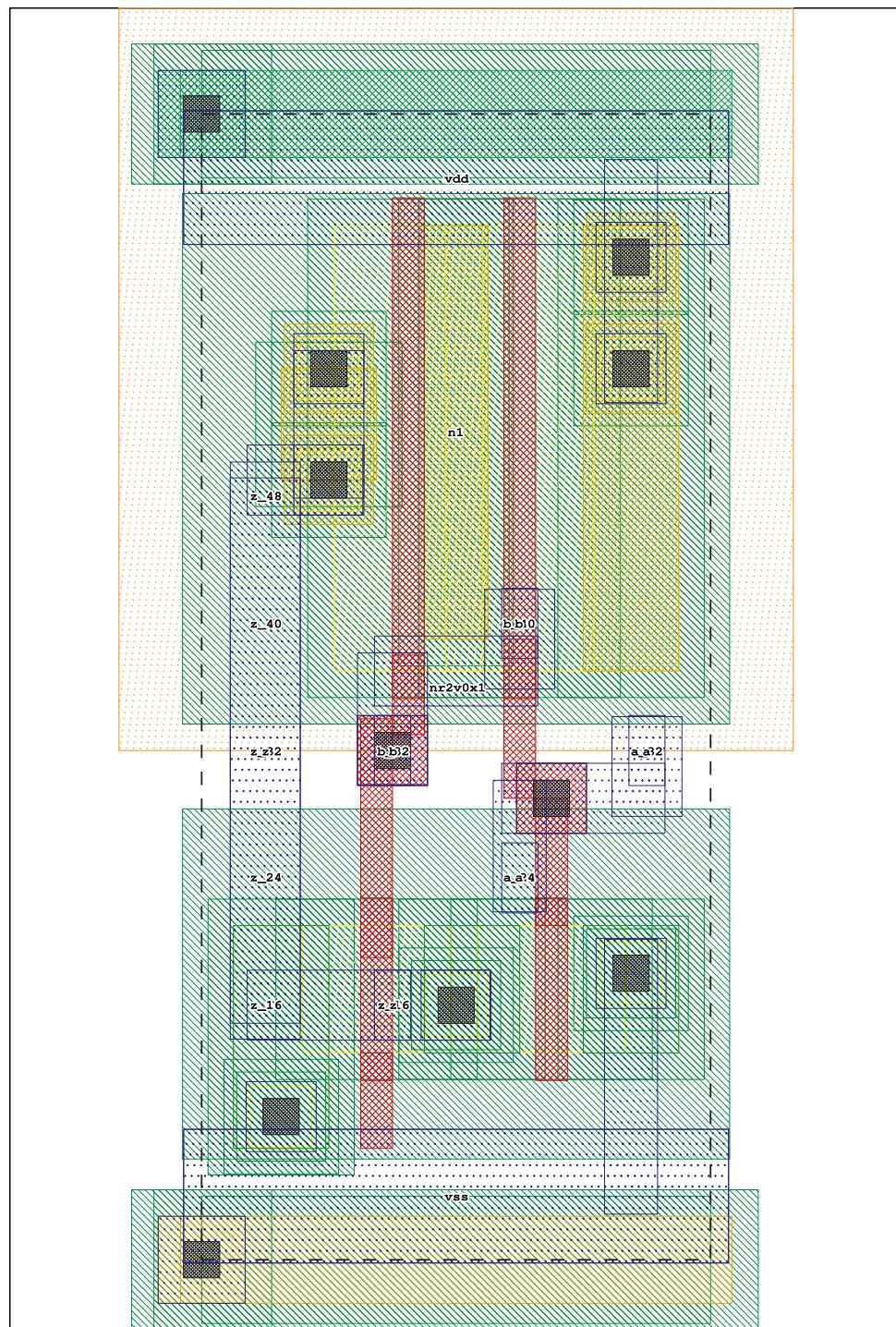
```

ENTITY nr2v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT rdown_a_z     : NATURAL := 2880;
    CONSTANT rdown_b_z     : NATURAL := 2890;
    CONSTANT rup_a_z       : NATURAL := 4160;
    CONSTANT rup_b_z       : NATURAL := 4150;
    CONSTANT tplh_a_z      : NATURAL := 53;
    CONSTANT tplh_b_z      : NATURAL := 45;
    CONSTANT tphl_b_z      : NATURAL := 41;
    CONSTANT tphl_a_z      : NATURAL := 50;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nr2v0x1;

ARCHITECTURE behaviour_data_flow OF nr2v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr2v0x1"
    SEVERITY WARNING;
    z <= not ((a or b)) after 135 ps;
END;

```



3.70 nr2v0x4

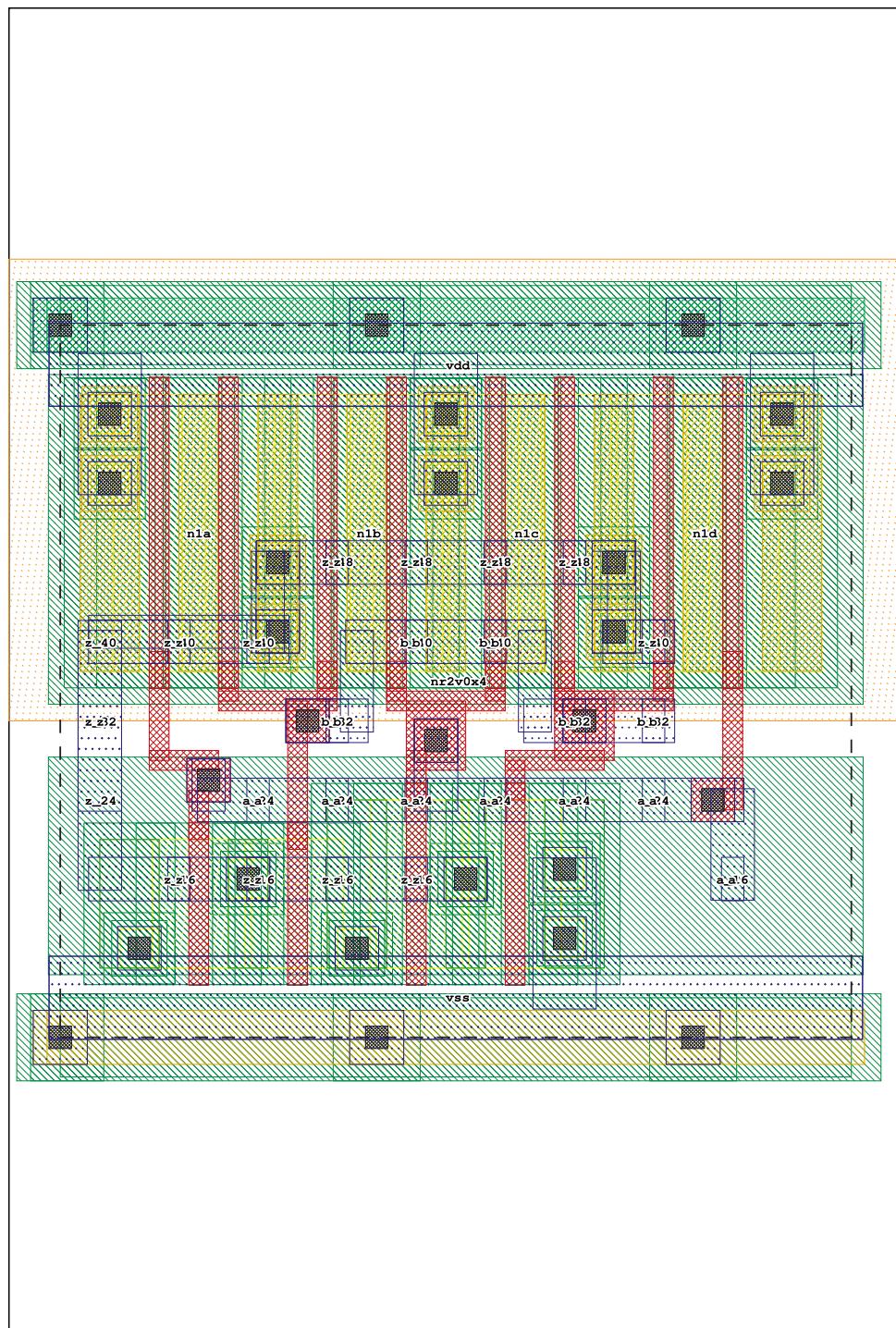
```

ENTITY nr2v0x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 5760;
    CONSTANT cin_a         : NATURAL := 17;
    CONSTANT cin_b         : NATURAL := 16;
    CONSTANT rdown_a_z     : NATURAL := 770;
    CONSTANT rdown_b_z     : NATURAL := 770;
    CONSTANT rup_a_z       : NATURAL := 1040;
    CONSTANT rup_b_z       : NATURAL := 1040;
    CONSTANT tplh_a_z      : NATURAL := 50;
    CONSTANT tplh_b_z      : NATURAL := 41;
    CONSTANT tphl_b_z      : NATURAL := 39;
    CONSTANT tphl_a_z      : NATURAL := 49;
    CONSTANT transistors   : NATURAL := 12
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nr2v0x4;

ARCHITECTURE behaviour_data_flow OF nr2v0x4 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr2v0x4"
    SEVERITY WARNING;
    z <= not ((a or b)) after 67 ps;
END;

```



3.71 nr2v1x05

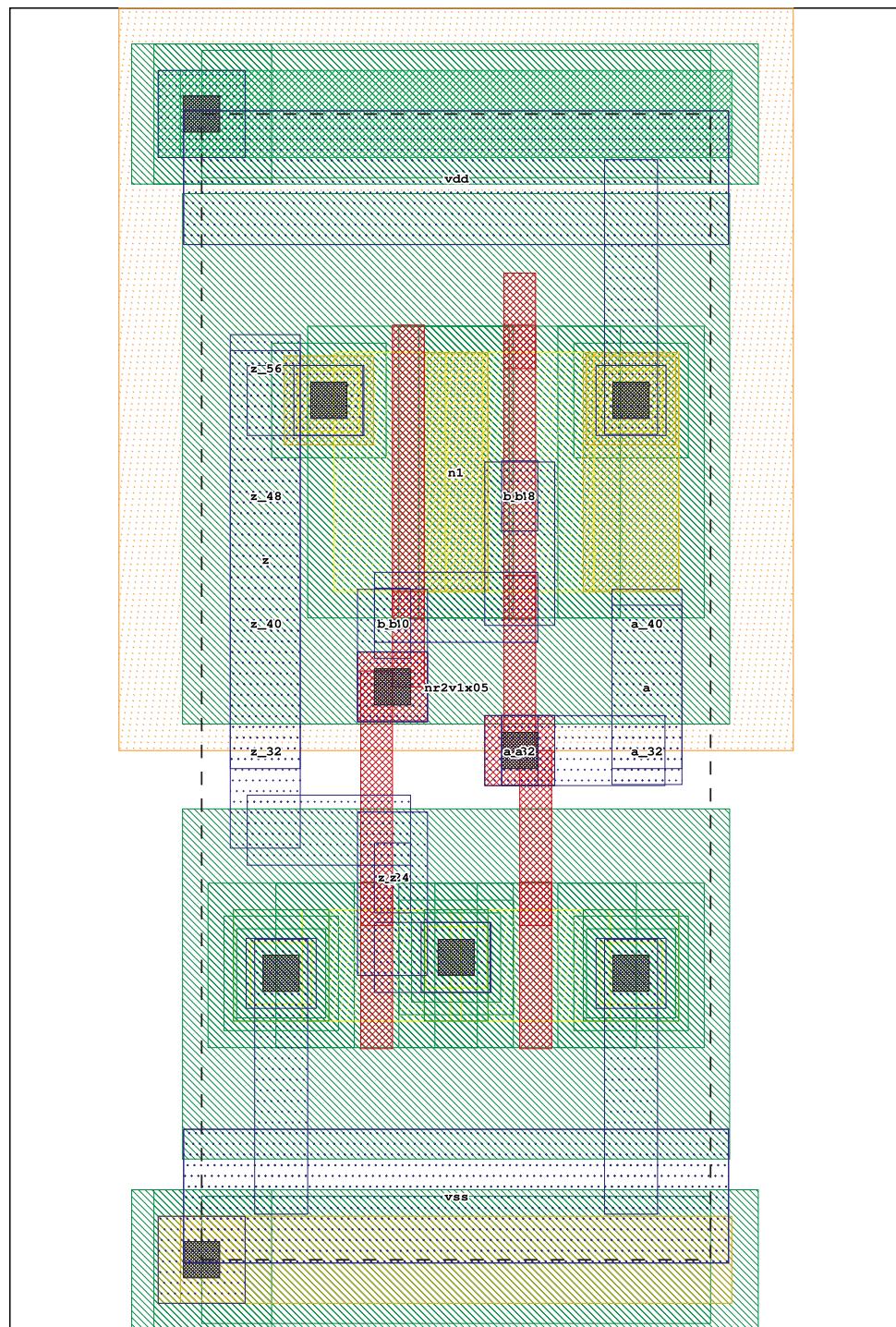
```

ENTITY nr2v1x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2304;
    CONSTANT cin_a         : NATURAL := 3;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT rdown_a_z    : NATURAL := 3330;
    CONSTANT rdown_b_z    : NATURAL := 3360;
    CONSTANT rup_a_z      : NATURAL := 7770;
    CONSTANT rup_b_z      : NATURAL := 7750;
    CONSTANT tplh_a_z     : NATURAL := 58;
    CONSTANT tplh_b_z     : NATURAL := 51;
    CONSTANT tphl_b_z     : NATURAL := 36;
    CONSTANT tphl_a_z     : NATURAL := 41;
    CONSTANT transistors   : NATURAL := 4
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nr2v1x05;

ARCHITECTURE behaviour_data_flow OF nr2v1x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr2v1x05"
    SEVERITY WARNING;
    z <= not ((a or b)) after 185 ps;
END;

```



3.72 nr3abv0x05

```

ENTITY nr3abv0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 3456;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 4;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT rdown_b_z     : NATURAL := 3880;
    CONSTANT rdown_c_z     : NATURAL := 3860;
    CONSTANT rdown_a_z     : NATURAL := 3890;
    CONSTANT rup_b_z       : NATURAL := 5830;
    CONSTANT rup_c_z       : NATURAL := 5810;
    CONSTANT rup_a_z       : NATURAL := 5830;
    CONSTANT tphh_a_z      : NATURAL := 90;
    CONSTANT tphl_c_z      : NATURAL := 42;
    CONSTANT tplh_c_z      : NATURAL := 47;
    CONSTANT tphh_b_z      : NATURAL := 90;
    CONSTANT tpll_b_z      : NATURAL := 106;
    CONSTANT tpll_a_z      : NATURAL := 115;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr3abv0x05;

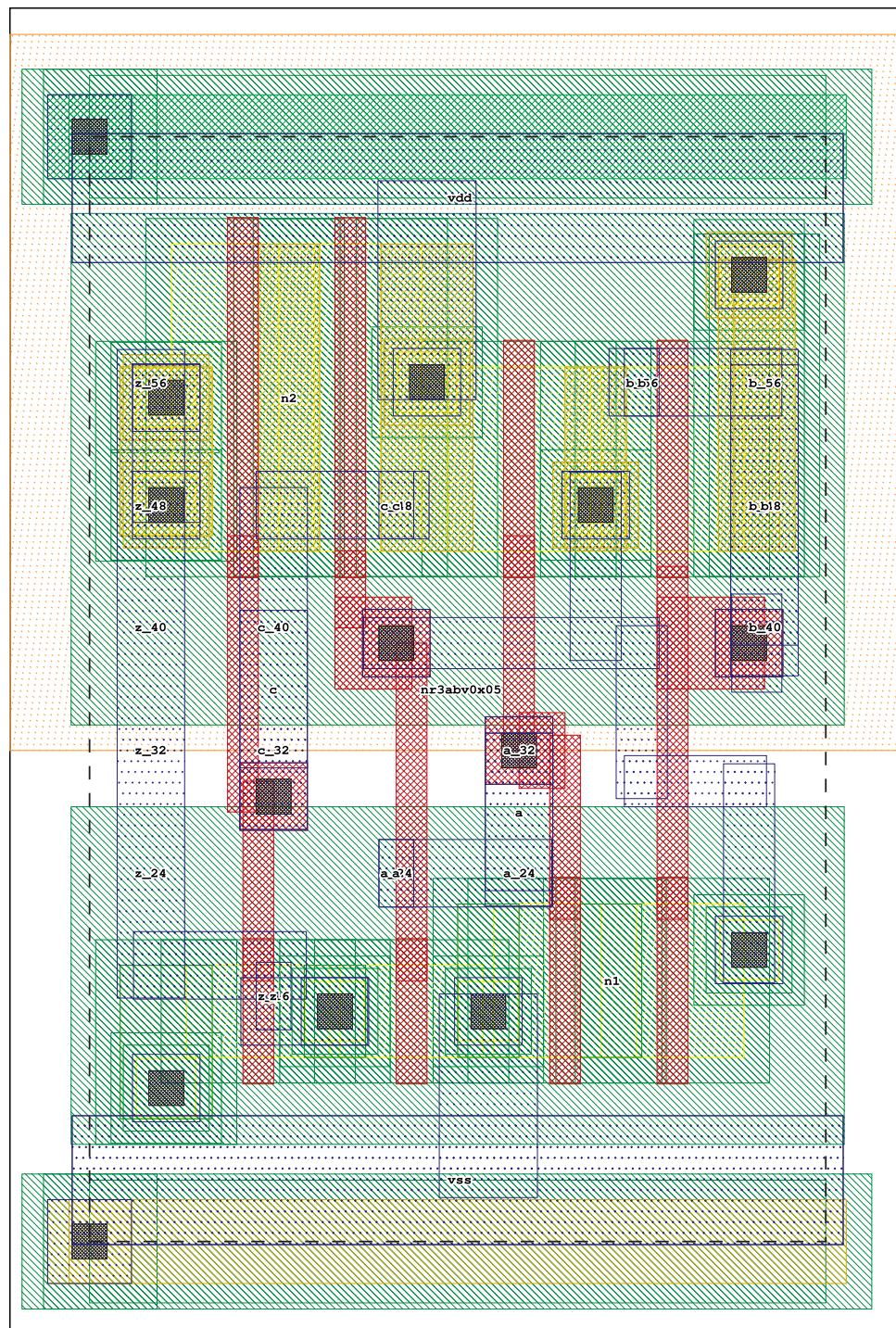
```

```

ARCHITECTURE behaviour_data_flow OF nr3abv0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr3abv0x05"
    SEVERITY WARNING;
    z <= not ((not a or not b) or c) after 203 ps;
END;

```



3.73 nr3av0x05

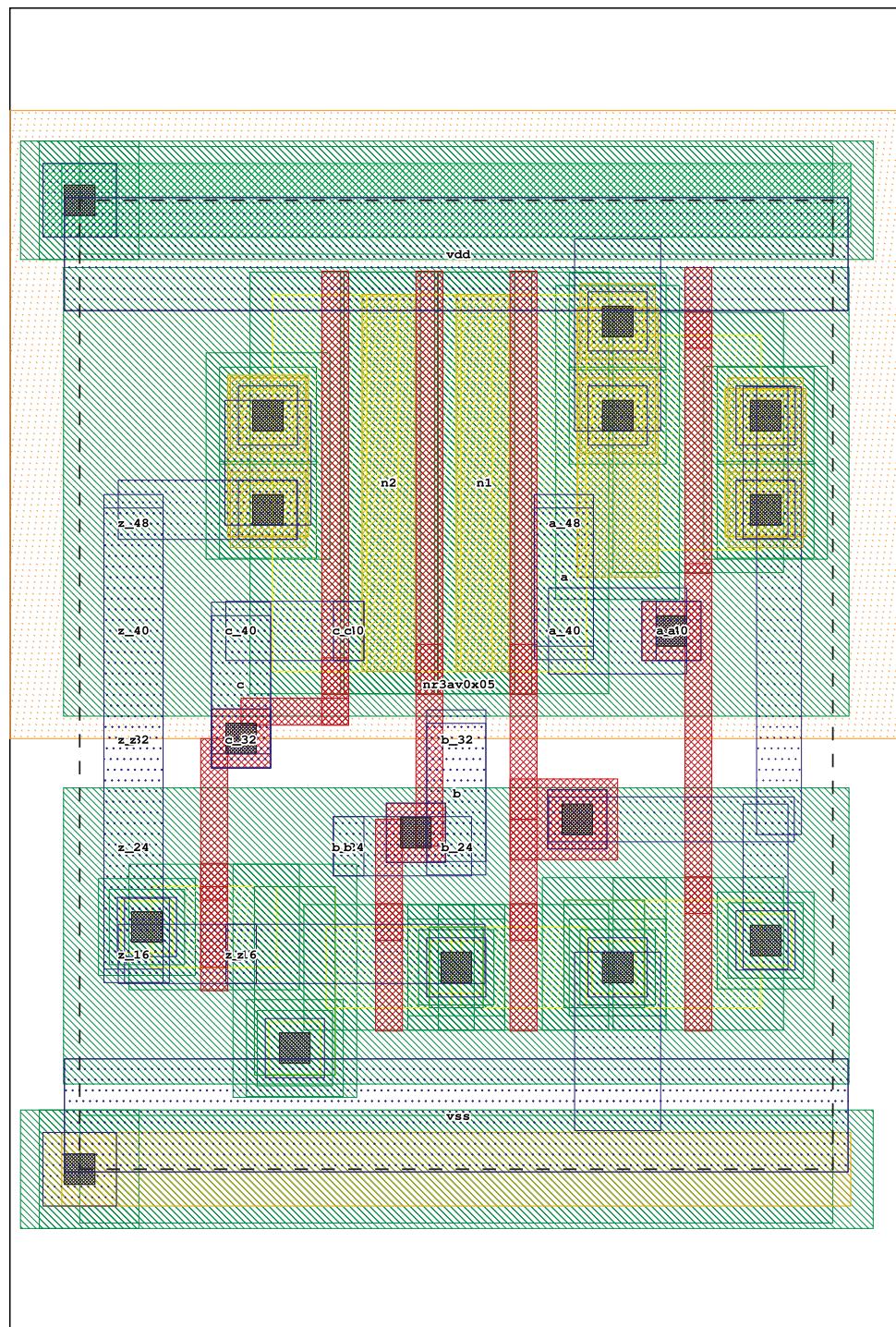
```

ENTITY nr3av0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 4;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT rdown_b_z     : NATURAL := 3880;
    CONSTANT rdown_c_z     : NATURAL := 3870;
    CONSTANT rdown_a_z     : NATURAL := 4000;
    CONSTANT rup_b_z       : NATURAL := 6260;
    CONSTANT rup_c_z       : NATURAL := 6240;
    CONSTANT rup_a_z       : NATURAL := 6250;
    CONSTANT tphh_a_z      : NATURAL := 111;
    CONSTANT tphl_c_z      : NATURAL := 50;
    CONSTANT tplh_c_z      : NATURAL := 53;
    CONSTANT tplh_b_z      : NATURAL := 74;
    CONSTANT tphl_b_z      : NATURAL := 62;
    CONSTANT tpll_a_z      : NATURAL := 112;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr3av0x05;

ARCHITECTURE behaviour_data_flow OF nr3av0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr3av0x05"
    SEVERITY WARNING;
    z <= not ((not a or b) or c) after 204 ps;
END;

```



3.74 nr3v0x05

```

ENTITY nr3v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT cin_c          : NATURAL := 4;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT rdown_b_z      : NATURAL := 3880;
    CONSTANT rdown_c_z      : NATURAL := 3880;
    CONSTANT rdown_a_z      : NATURAL := 3980;
    CONSTANT rup_b_z         : NATURAL := 6260;
    CONSTANT rup_c_z         : NATURAL := 6240;
    CONSTANT rup_a_z         : NATURAL := 6250;
    CONSTANT tplh_a_z        : NATURAL := 81;
    CONSTANT tplh_c_z        : NATURAL := 49;
    CONSTANT tplh_c_z        : NATURAL := 52;
    CONSTANT tplh_b_z        : NATURAL := 73;
    CONSTANT tplh_b_z        : NATURAL := 61;
    CONSTANT tplh_a_z        : NATURAL := 67;
    CONSTANT transistors     : NATURAL := 6
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr3v0x05;

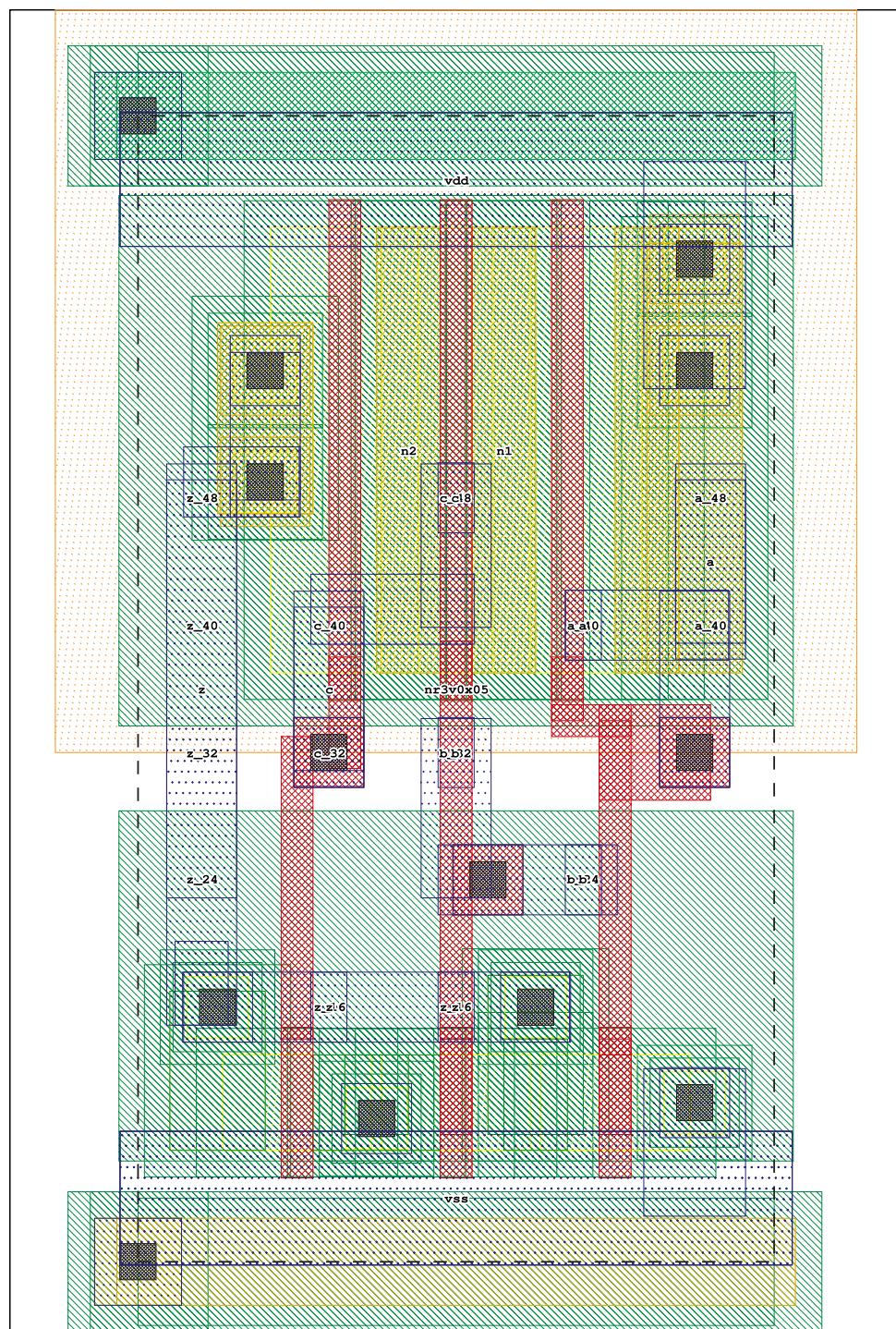
```

```

ARCHITECTURE behaviour_data_flow OF nr3v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr3v0x05"
    SEVERITY WARNING;
    z <= not (((b or c) or a)) after 191 ps;
END;

```



3.75 nr3v0x1

```

ENTITY nr3v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_b         : NATURAL := 8;
    CONSTANT cin_c         : NATURAL := 7;
    CONSTANT cin_a         : NATURAL := 9;
    CONSTANT rdown_b_z     : NATURAL := 2330;
    CONSTANT rdown_c_z     : NATURAL := 2320;
    CONSTANT rdown_a_z     : NATURAL := 2390;
    CONSTANT rup_b_z       : NATURAL := 3130;
    CONSTANT rup_c_z       : NATURAL := 3120;
    CONSTANT rup_a_z       : NATURAL := 3140;
    CONSTANT tplh_a_z      : NATURAL := 77;
    CONSTANT tplh_c_z      : NATURAL := 48;
    CONSTANT tplh_c_z      : NATURAL := 45;
    CONSTANT tplh_b_z      : NATURAL := 67;
    CONSTANT tplh_b_z      : NATURAL := 64;
    CONSTANT tplh_a_z      : NATURAL := 74;
    CONSTANT transistors   : NATURAL := 9
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr3v0x1;

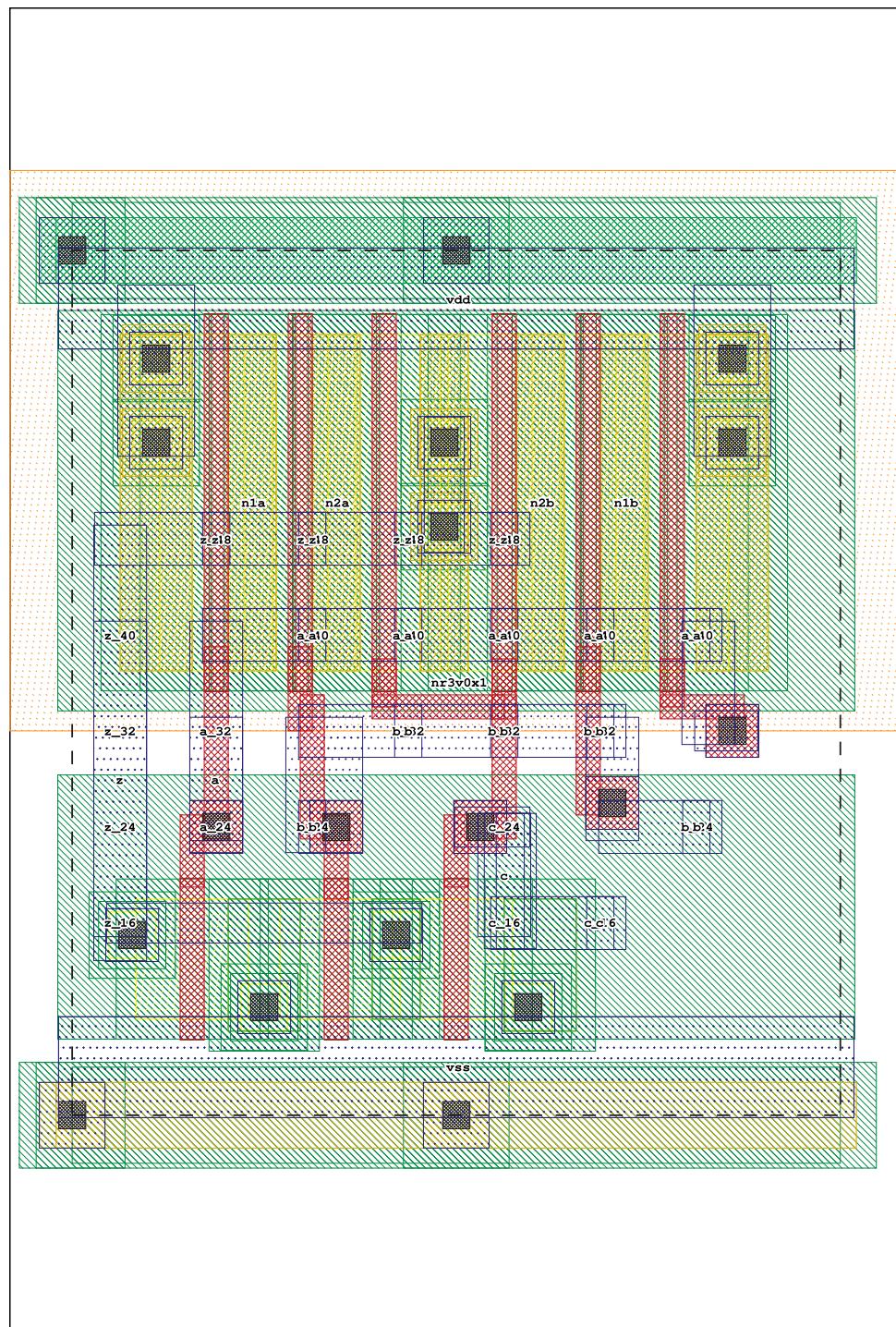
```

```

ARCHITECTURE behaviour_data_flow OF nr3v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr3v0x1"
    SEVERITY WARNING;
    z <= not (((b or c) or a)) after 131 ps;
END;

```



3.76 nr3v0x2

```

ENTITY nr3v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 6336;
    CONSTANT cin_b         : NATURAL := 11;
    CONSTANT cin_c         : NATURAL := 11;
    CONSTANT cin_a         : NATURAL := 11;
    CONSTANT rdown_b_z     : NATURAL := 1550;
    CONSTANT rdown_c_z     : NATURAL := 1550;
    CONSTANT rdown_a_z     : NATURAL := 1580;
    CONSTANT rup_b_z       : NATURAL := 2160;
    CONSTANT rup_c_z       : NATURAL := 2160;
    CONSTANT rup_a_z       : NATURAL := 2160;
    CONSTANT tplh_a_z      : NATURAL := 76;
    CONSTANT tplh_c_z      : NATURAL := 49;
    CONSTANT tplh_c_z      : NATURAL := 47;
    CONSTANT tplh_b_z      : NATURAL := 67;
    CONSTANT tplh_b_z      : NATURAL := 63;
    CONSTANT tplh_a_z      : NATURAL := 71;
    CONSTANT transistors   : NATURAL := 12
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr3v0x2;

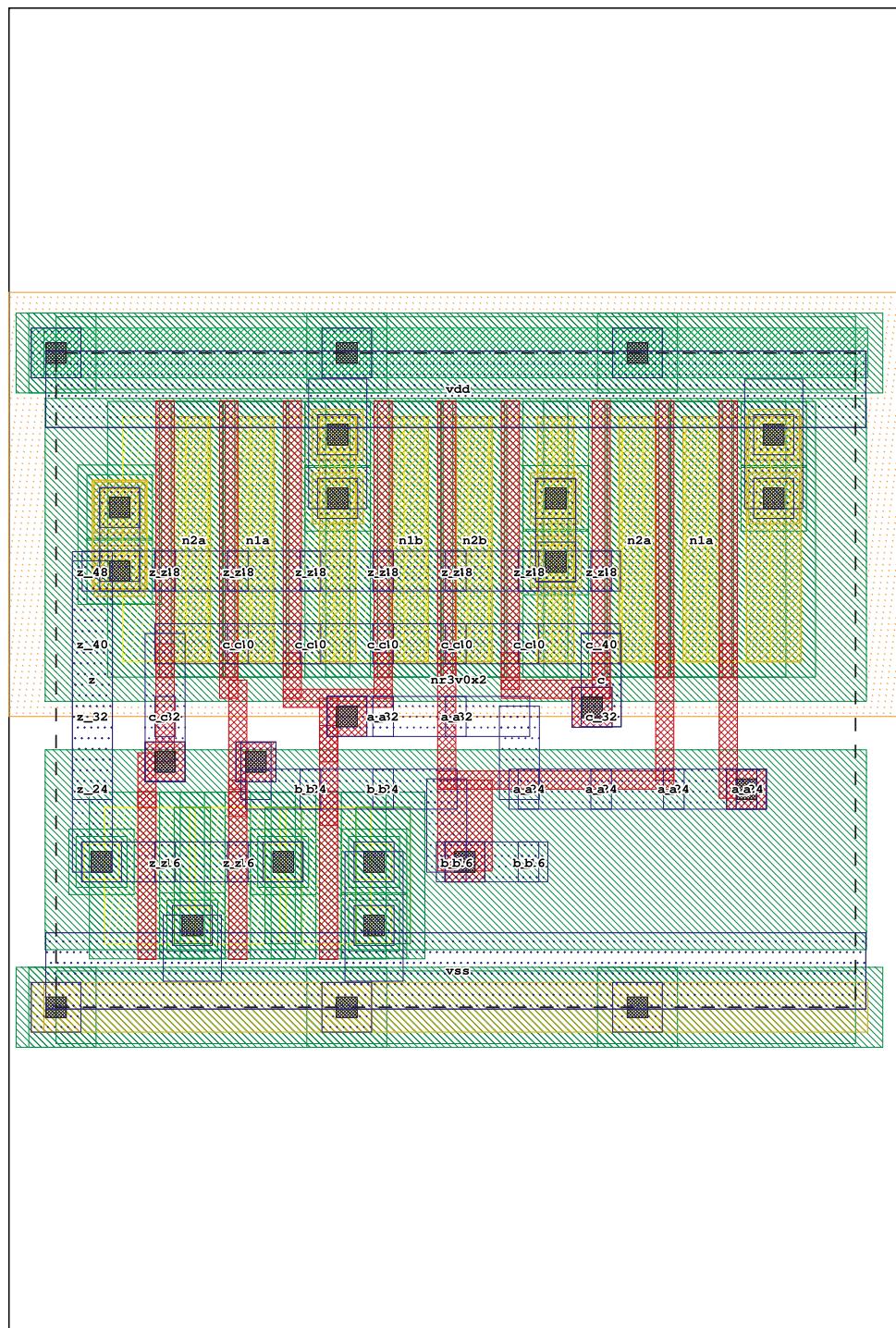
```

```

ARCHITECTURE behaviour_data_flow OF nr3v0x2 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr3v0x2"
    SEVERITY WARNING;
    z <= not (((b or c) or a)) after 109 ps;
END;

```



3.77 nr3v0x4

```

ENTITY nr3v0x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 9792;
    CONSTANT cin_b         : NATURAL := 19;
    CONSTANT cin_c         : NATURAL := 19;
    CONSTANT cin_a         : NATURAL := 19;
    CONSTANT rdown_b_z     : NATURAL := 970;
    CONSTANT rdown_c_z     : NATURAL := 970;
    CONSTANT rdown_a_z     : NATURAL := 990;
    CONSTANT rup_b_z       : NATURAL := 1330;
    CONSTANT rup_c_z       : NATURAL := 1320;
    CONSTANT rup_a_z       : NATURAL := 1330;
    CONSTANT tplh_a_z      : NATURAL := 76;
    CONSTANT tplh_c_z      : NATURAL := 49;
    CONSTANT tplh_c_z      : NATURAL := 47;
    CONSTANT tplh_b_z      : NATURAL := 67;
    CONSTANT tplh_b_z      : NATURAL := 64;
    CONSTANT tplh_a_z      : NATURAL := 72;
    CONSTANT transistors   : NATURAL := 21
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr3v0x4;

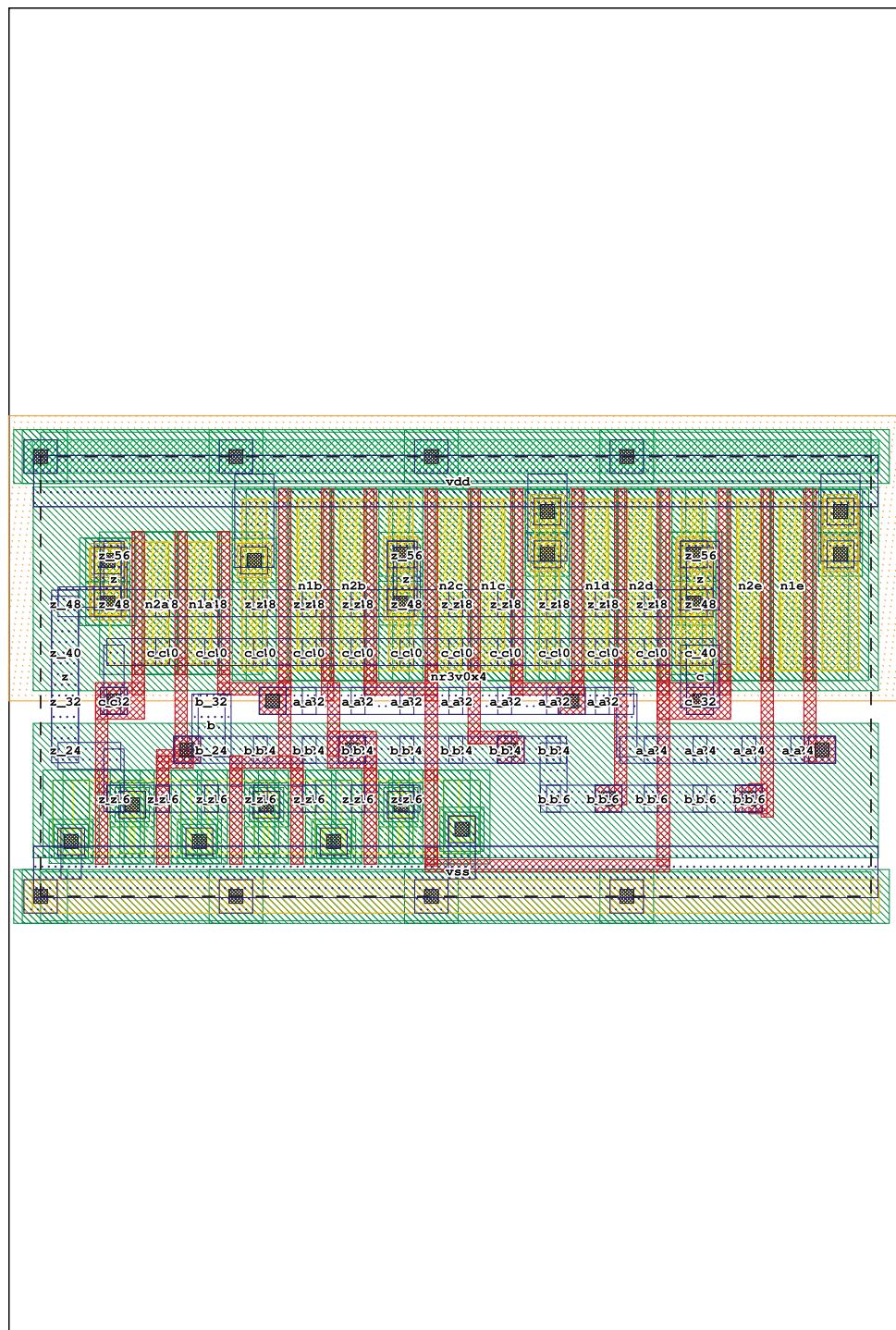
```

```

ARCHITECTURE behaviour_data_flow OF nr3v0x4 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr3v0x4"
    SEVERITY WARNING;
    z <= not (((b or c) or a)) after 91 ps;
END;

```



3.78 nr3v1x05

```

ENTITY nr3v1x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_b          : NATURAL := 5;
    CONSTANT cin_c          : NATURAL := 5;
    CONSTANT cin_a          : NATURAL := 5;
    CONSTANT rdown_b_z      : NATURAL := 2350;
    CONSTANT rdown_c_z      : NATURAL := 2390;
    CONSTANT rdown_a_z      : NATURAL := 2410;
    CONSTANT rup_b_z        : NATURAL := 6280;
    CONSTANT rup_c_z        : NATURAL := 6240;
    CONSTANT rup_a_z        : NATURAL := 6270;
    CONSTANT tplh_a_z       : NATURAL := 86;
    CONSTANT tplh_c_z       : NATURAL := 39;
    CONSTANT tplh_c_z       : NATURAL := 57;
    CONSTANT tplh_b_z       : NATURAL := 78;
    CONSTANT tplh_b_z       : NATURAL := 47;
    CONSTANT tplh_a_z       : NATURAL := 50;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END nr3v1x05;

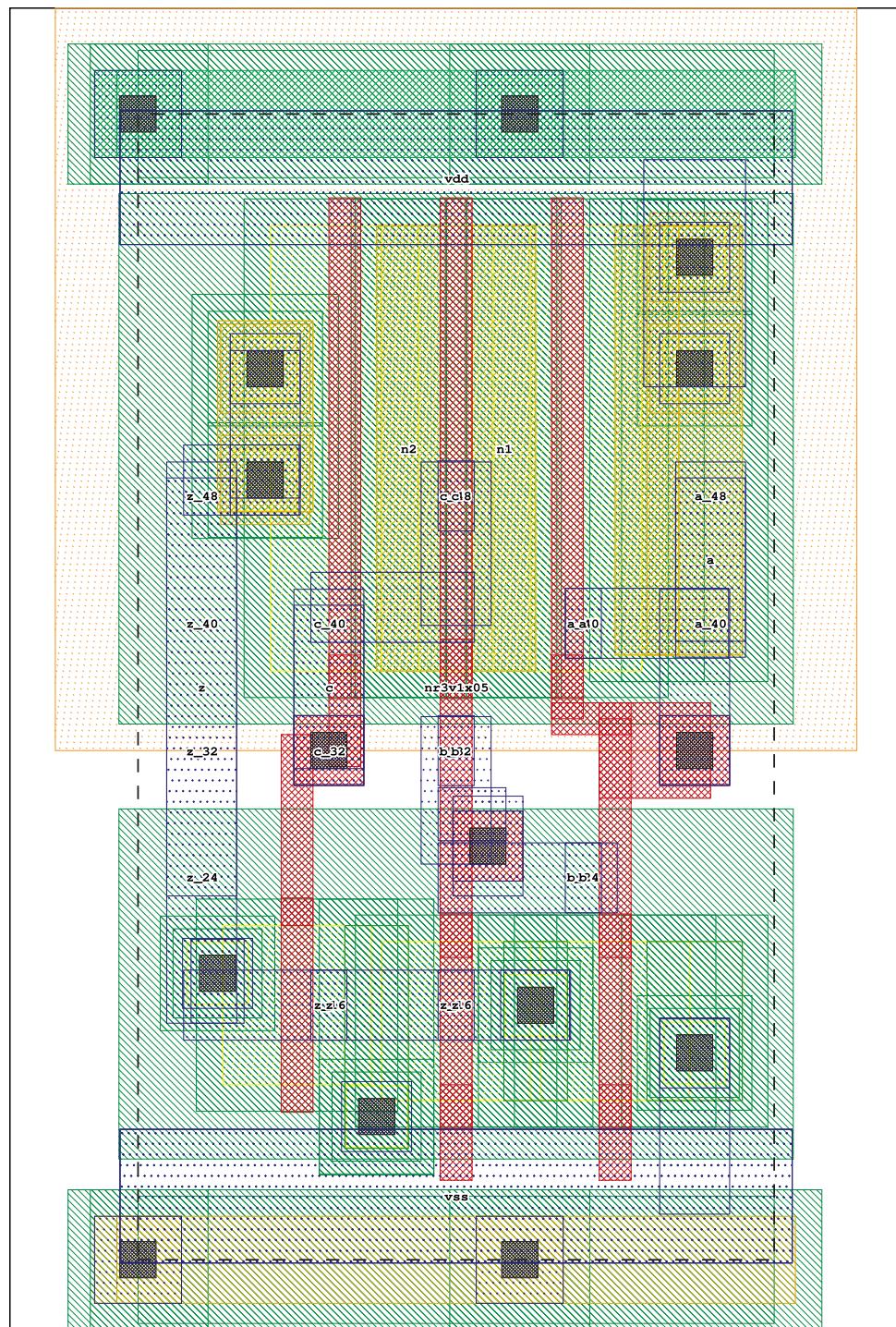
```

```

ARCHITECTURE behaviour_data_flow OF nr3v1x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr3v1x05"
    SEVERITY WARNING;
    z <= not (((b or c) or a)) after 168 ps;
END;

```



3.79 nr4v0x1

```

ENTITY nr4v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 5760;
    CONSTANT cin_c          : NATURAL := 6;
    CONSTANT cin_d          : NATURAL := 6;
    CONSTANT cin_b          : NATURAL := 7;
    CONSTANT cin_a          : NATURAL := 7;
    CONSTANT rdown_c_z      : NATURAL := 3900;
    CONSTANT rdown_d_z      : NATURAL := 3890;
    CONSTANT rdown_b_z      : NATURAL := 4000;
    CONSTANT rdown_a_z      : NATURAL := 4150;
    CONSTANT rup_c_z         : NATURAL := 5460;
    CONSTANT rup_d_z         : NATURAL := 5400;
    CONSTANT rup_b_z         : NATURAL := 5480;
    CONSTANT rup_a_z         : NATURAL := 5480;
    CONSTANT tphl_d_z        : NATURAL := 58;
    CONSTANT tphl_a_z        : NATURAL := 116;
    CONSTANT tphl_d_z        : NATURAL := 49;
    CONSTANT tphl_c_z        : NATURAL := 80;
    CONSTANT tphl_b_z        : NATURAL := 106;
    CONSTANT tphl_c_z        : NATURAL := 83;
    CONSTANT tphl_b_z        : NATURAL := 95;
    CONSTANT tphl_a_z        : NATURAL := 103;
    CONSTANT transistors     : NATURAL := 12
);
PORT (
    c      : in  BIT;
    d      : in  BIT;
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nr4v0x1;

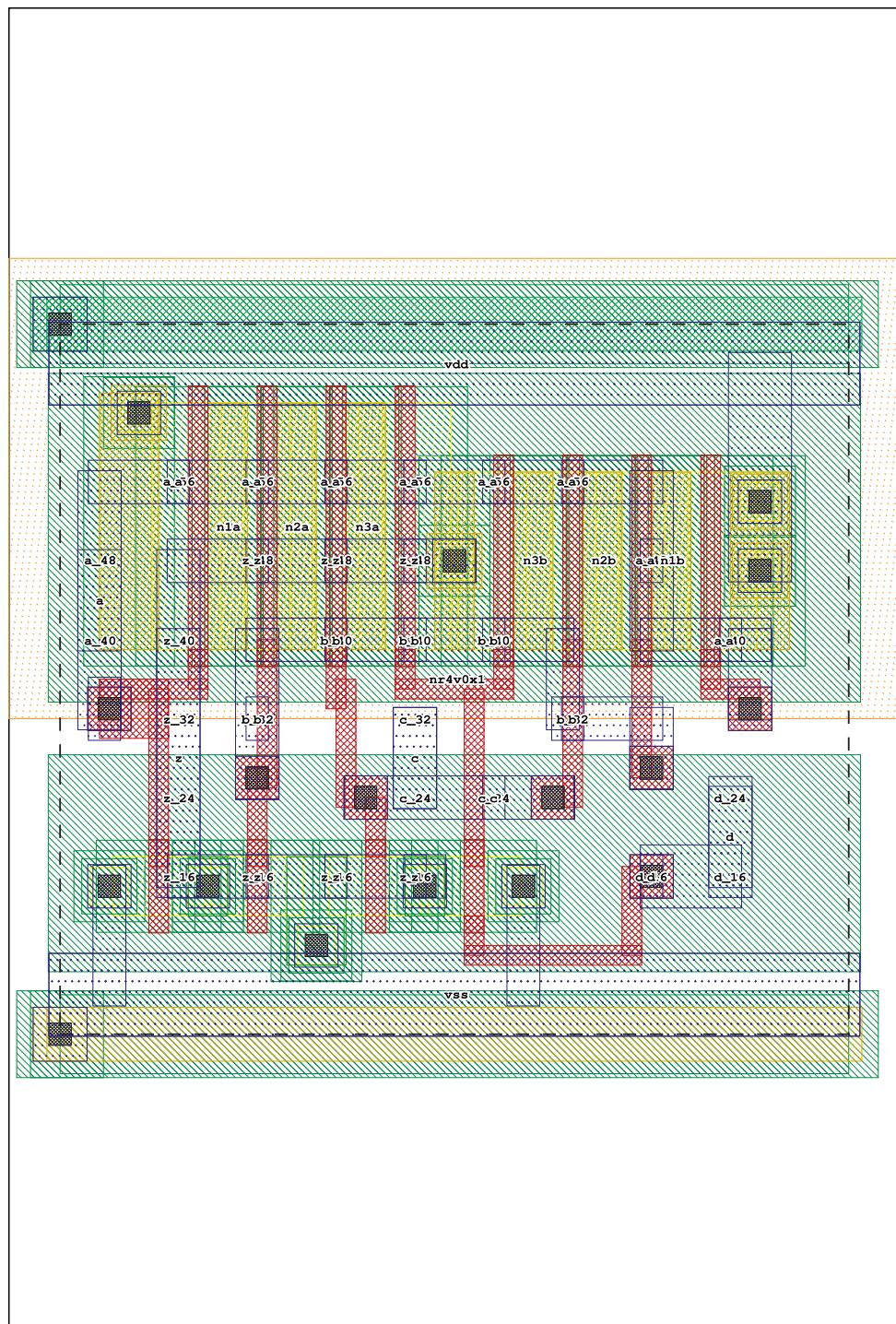
```

ARCHITECTURE behaviour_data_flow OF nr4v0x1 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr4v0x1"
    SEVERITY WARNING;
    z <= not (((((c or d) or b) or a)) after 204 ps;
END;

```



3.80 nr4v0x2

```

ENTITY nr4v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 8064;
    CONSTANT cin_c          : NATURAL := 11;
    CONSTANT cin_d          : NATURAL := 11;
    CONSTANT cin_b          : NATURAL := 11;
    CONSTANT cin_a          : NATURAL := 11;
    CONSTANT rdown_c_z      : NATURAL := 2120;
    CONSTANT rdown_d_z      : NATURAL := 2120;
    CONSTANT rdown_b_z      : NATURAL := 2170;
    CONSTANT rdown_a_z      : NATURAL := 2250;
    CONSTANT rup_c_z         : NATURAL := 2970;
    CONSTANT rup_d_z         : NATURAL := 2960;
    CONSTANT rup_b_z         : NATURAL := 2970;
    CONSTANT rup_a_z         : NATURAL := 2970;
    CONSTANT tphl_d_z        : NATURAL := 59;
    CONSTANT tphl_a_z        : NATURAL := 110;
    CONSTANT tphl_d_z        : NATURAL := 50;
    CONSTANT tphl_c_z        : NATURAL := 79;
    CONSTANT tphl_b_z        : NATURAL := 102;
    CONSTANT tphl_c_z        : NATURAL := 81;
    CONSTANT tphl_b_z        : NATURAL := 92;
    CONSTANT tphl_a_z        : NATURAL := 99;
    CONSTANT transistors     : NATURAL := 16
);
PORT (
    c      : in  BIT;
    d      : in  BIT;
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nr4v0x2;

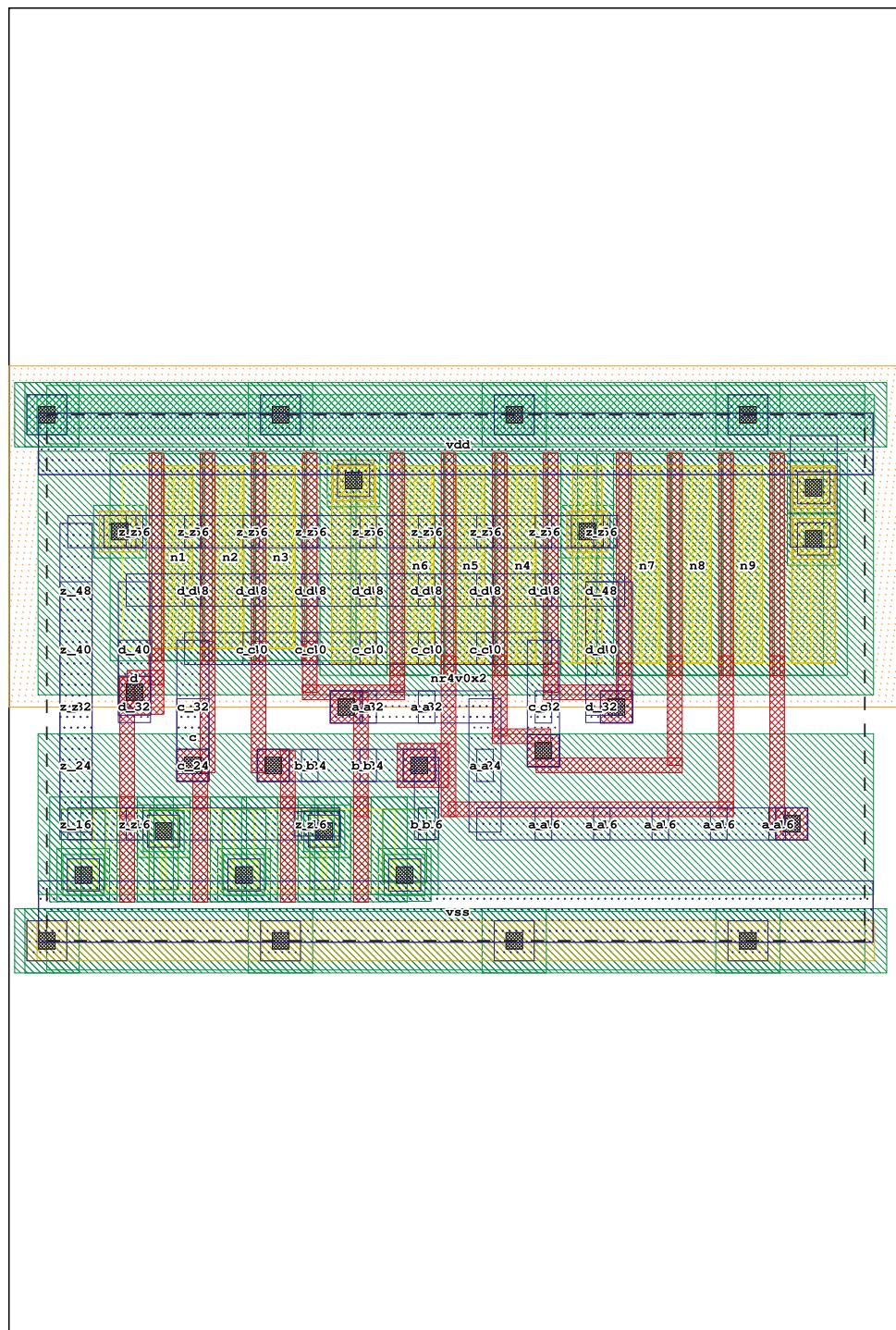
```

ARCHITECTURE behaviour_data_flow OF nr4v0x2 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr4v0x2"
    SEVERITY WARNING;
    z <= not (((((c or d) or b) or a)) after 148 ps;
END;

```



3.81 nr4v1x05

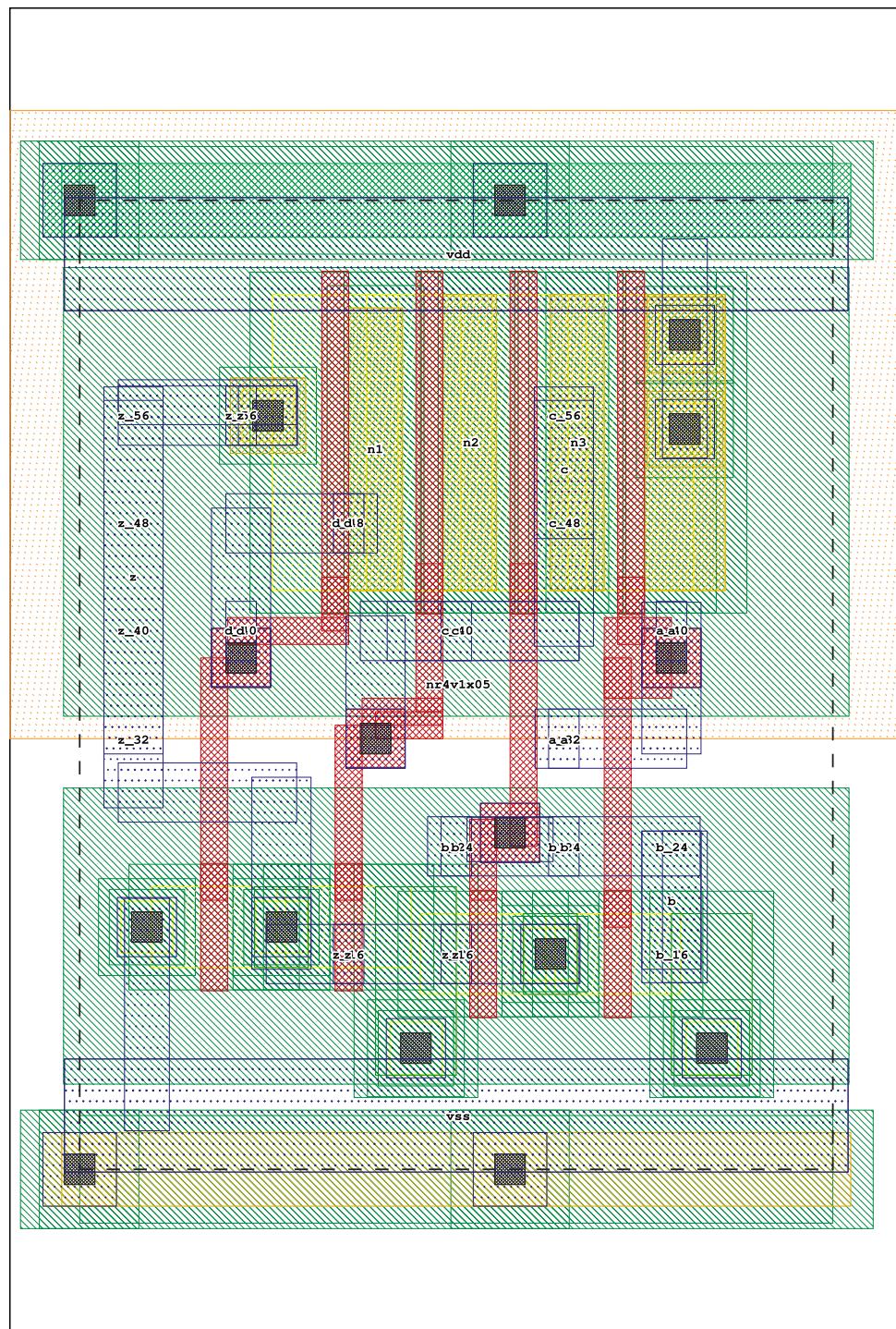
```

ENTITY nr4v1x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_c          : NATURAL := 4;
    CONSTANT cin_d          : NATURAL := 4;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT rdown_c_z      : NATURAL := 3910;
    CONSTANT rdown_d_z      : NATURAL := 3920;
    CONSTANT rdown_b_z      : NATURAL := 4050;
    CONSTANT rdown_a_z      : NATURAL := 4200;
    CONSTANT rup_c_z        : NATURAL := 10700;
    CONSTANT rup_d_z        : NATURAL := 10650;
    CONSTANT rup_b_z        : NATURAL := 10710;
    CONSTANT rup_a_z        : NATURAL := 10680;
    CONSTANT tphl_d_z       : NATURAL := 47;
    CONSTANT tphl_a_z       : NATURAL := 126;
    CONSTANT tphl_d_z       : NATURAL := 64;
    CONSTANT tphl_c_z       : NATURAL := 57;
    CONSTANT tphl_b_z       : NATURAL := 118;
    CONSTANT tphl_c_z       : NATURAL := 96;
    CONSTANT tphl_b_z       : NATURAL := 62;
    CONSTANT tphl_a_z       : NATURAL := 62;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    c      : in  BIT;
    d      : in  BIT;
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END nr4v1x05;

ARCHITECTURE behaviour_data_flow OF nr4v1x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nr4v1x05"
    SEVERITY WARNING;
    z <= not (((((c or d) or b) or a)) after 263 ps;
END;

```



3.82 oai211v0x05

```

ENTITY oai211v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 3456;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT cin_c         : NATURAL := 3;
    CONSTANT cin_a1        : NATURAL := 4;
    CONSTANT cin_a2        : NATURAL := 3;
    CONSTANT rdown_b_z     : NATURAL := 4870;
    CONSTANT rdown_c_z     : NATURAL := 4860;
    CONSTANT rdown_a1_z    : NATURAL := 5140;
    CONSTANT rdown_a2_z    : NATURAL := 5140;
    CONSTANT rup_b_z       : NATURAL := 6620;
    CONSTANT rup_c_z       : NATURAL := 6640;
    CONSTANT rup_a1_z      : NATURAL := 7350;
    CONSTANT rup_a2_z      : NATURAL := 7340;
    CONSTANT tphl_b_z      : NATURAL := 49;
    CONSTANT tphl_c_z      : NATURAL := 47;
    CONSTANT tplh_a2_z     : NATURAL := 87;
    CONSTANT tphl_a1_z     : NATURAL := 66;
    CONSTANT tplh_c_z      : NATURAL := 59;
    CONSTANT tplh_a1_z     : NATURAL := 96;
    CONSTANT tplh_b_z      : NATURAL := 68;
    CONSTANT tphl_a2_z     : NATURAL := 57;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END oai211v0x05;

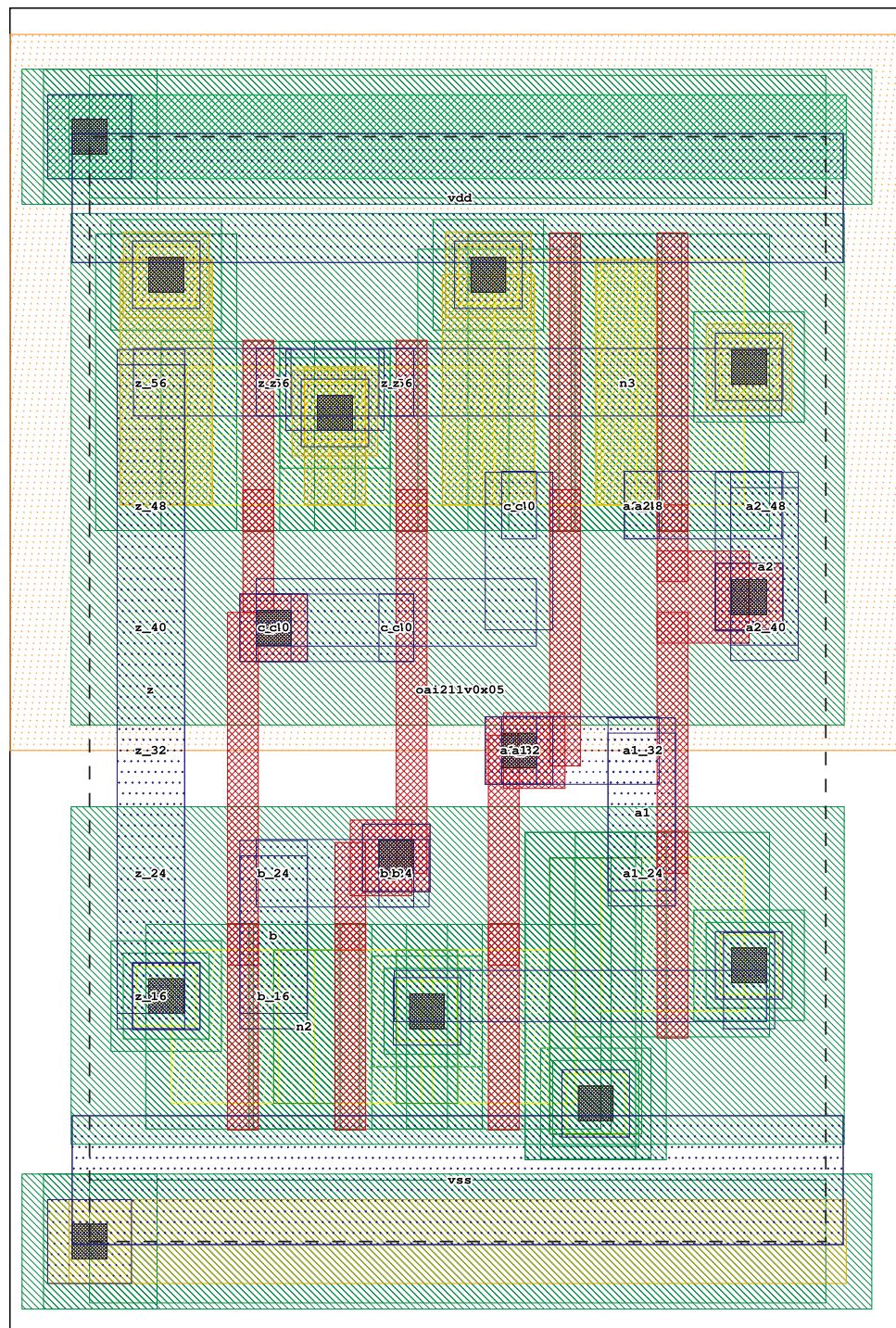
```

ARCHITECTURE behaviour_data_flow OF oai211v0x05 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai211v0x05"
    SEVERITY WARNING;
    z <= not((b and c) and (a1 or a2)) after 216 ps;
END;

```



3.83 oai21a2bv0x05

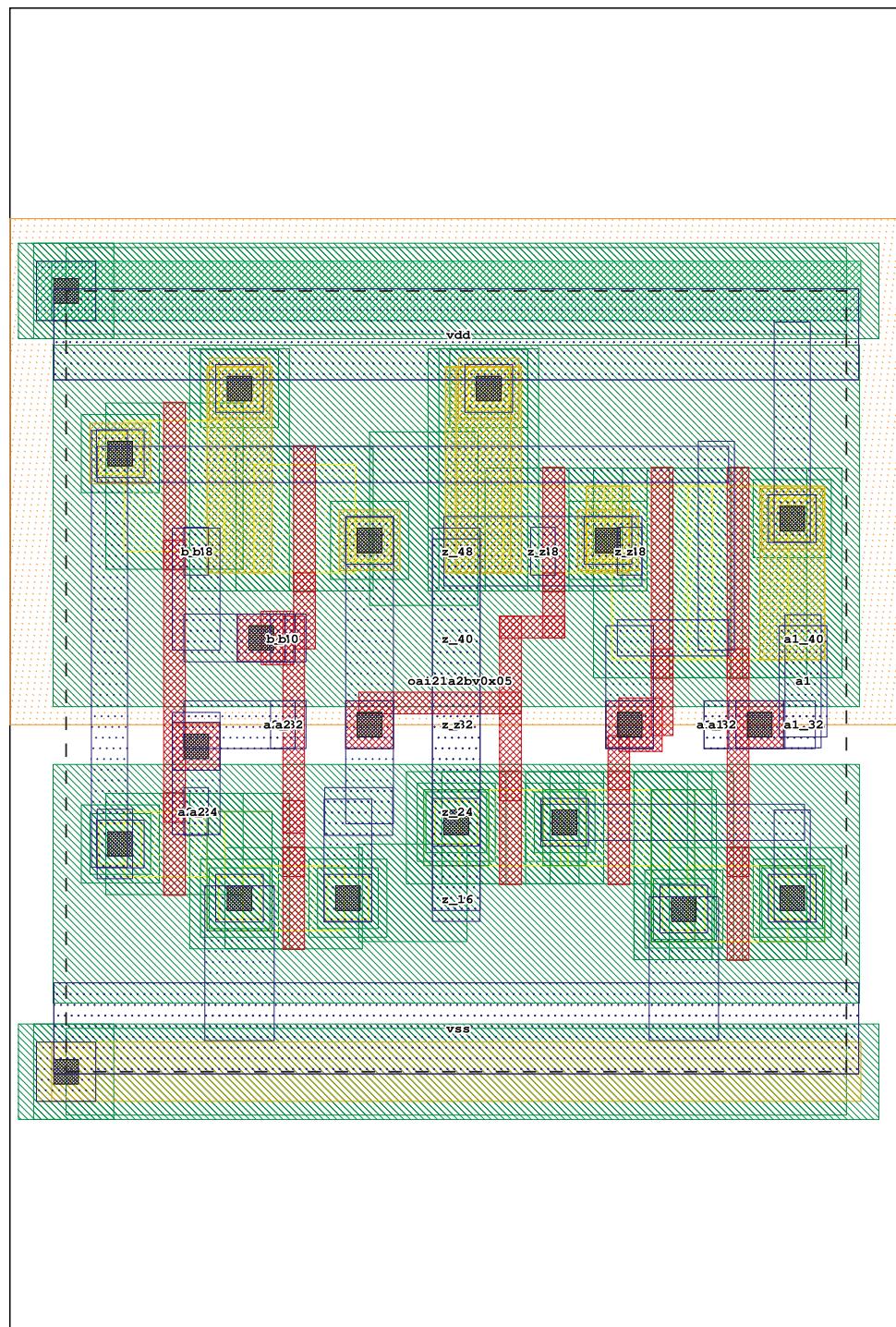
```

ENTITY oai21a2bv0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5330;
    CONSTANT rdown_a2_z     : NATURAL := 5360;
    CONSTANT rdown_b_z      : NATURAL := 4940;
    CONSTANT rup_a1_z       : NATURAL := 7320;
    CONSTANT rup_a2_z       : NATURAL := 7350;
    CONSTANT rup_b_z        : NATURAL := 7490;
    CONSTANT tpll_b_z       : NATURAL := 91;
    CONSTANT tpll_a2_z      : NATURAL := 108;
    CONSTANT tplh_a1_z      : NATURAL := 77;
    CONSTANT tphh_b_z       : NATURAL := 78;
    CONSTANT tphh_a2_z      : NATURAL := 104;
    CONSTANT tphl_a1_z      : NATURAL := 61;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END oai21a2bv0x05;

ARCHITECTURE behaviour_data_flow OF oai21a2bv0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai21a2bv0x05"
    SEVERITY WARNING;
    z <= (not a1 and a2) or b after 244 ps;
END;

```



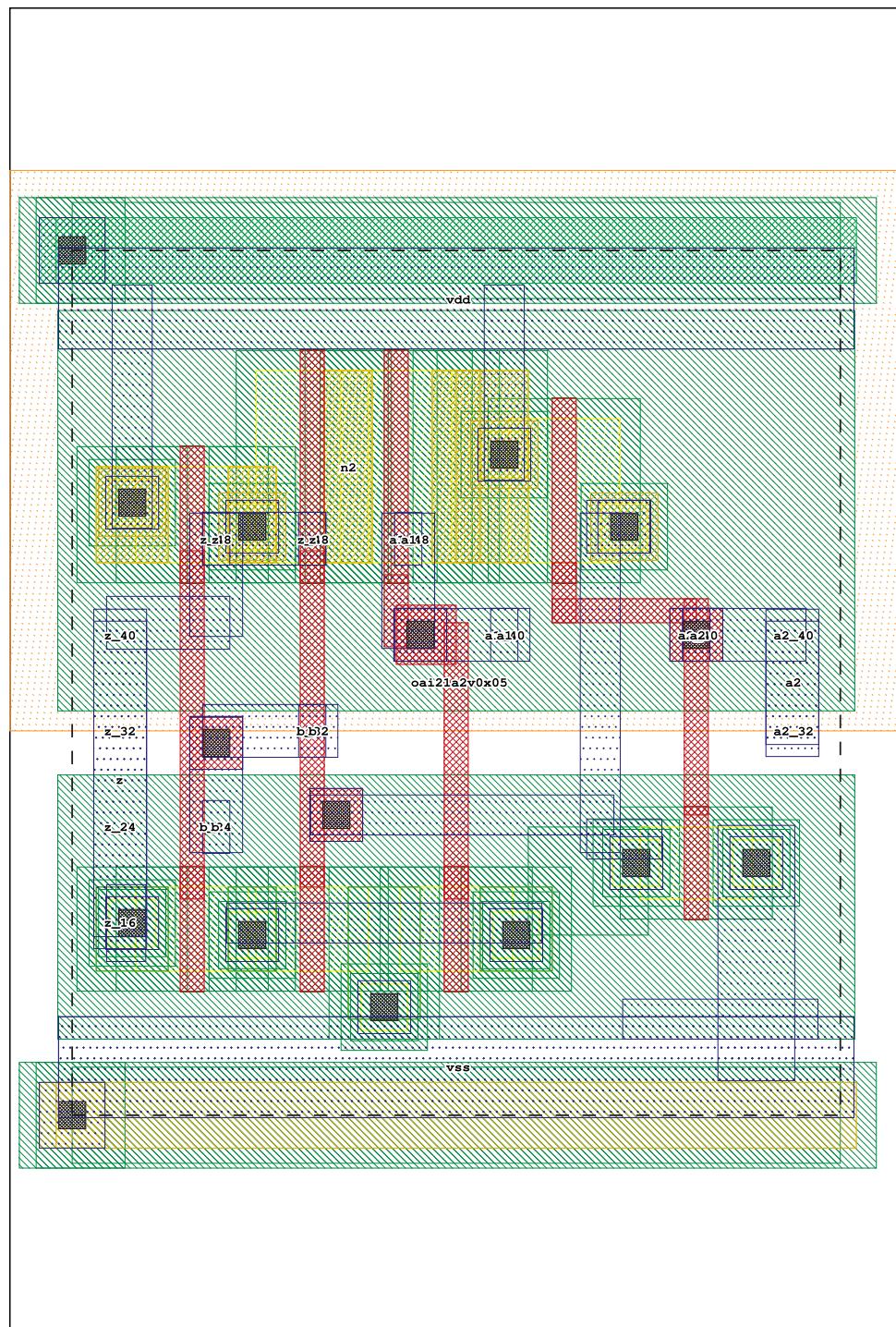
3.84 oai21a2v0x05

```

ENTITY oai21a2v0x05 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5320;
    CONSTANT rdown_a2_z     : NATURAL := 5320;
    CONSTANT rdown_b_z      : NATURAL := 4920;
    CONSTANT rup_a1_z       : NATURAL := 7310;
    CONSTANT rup_a2_z       : NATURAL := 7320;
    CONSTANT rup_b_z        : NATURAL := 7450;
    CONSTANT tphl_b_z       : NATURAL := 42;
    CONSTANT tpll_a2_z      : NATURAL := 96;
    CONSTANT tplh_a1_z      : NATURAL := 75;
    CONSTANT tplh_b_z       : NATURAL := 53;
    CONSTANT tphh_a2_z      : NATURAL := 93;
    CONSTANT tphl_a1_z      : NATURAL := 57;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oai21a2v0x05;

ARCHITECTURE behaviour_data_flow OF oai21a2v0x05 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai21a2v0x05"
    SEVERITY WARNING;
  z <= not ((a1 or not a2) and b) after 226 ps;
END;

```



3.85 oai21bv0x05

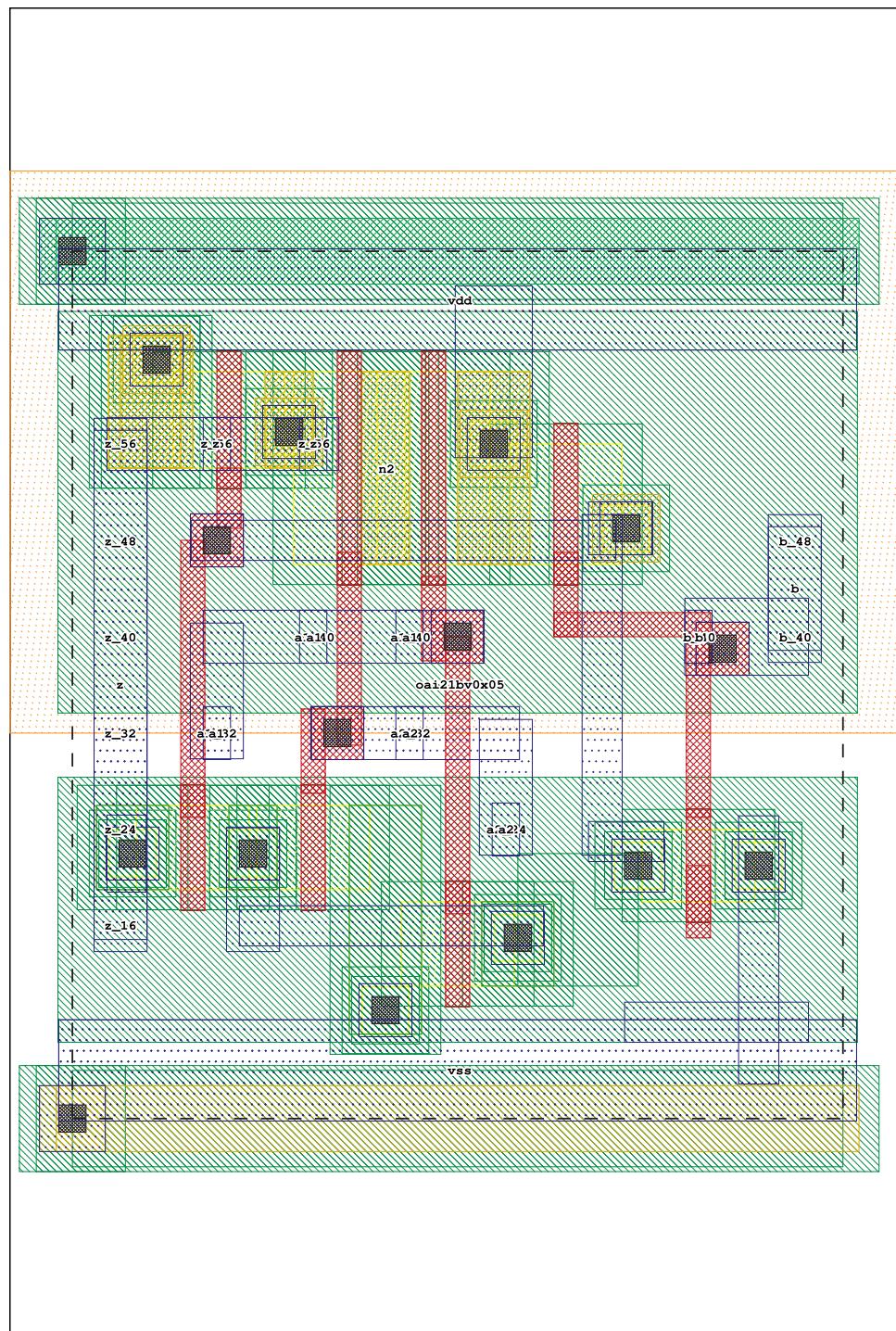
```

ENTITY oai21bv0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_a1         : NATURAL := 4;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5330;
    CONSTANT rdown_a2_z     : NATURAL := 5330;
    CONSTANT rdown_b_z      : NATURAL := 4930;
    CONSTANT rup_a1_z       : NATURAL := 7320;
    CONSTANT rup_a2_z       : NATURAL := 7300;
    CONSTANT rup_b_z        : NATURAL := 7480;
    CONSTANT tpll_b_z       : NATURAL := 90;
    CONSTANT tphl_a2_z      : NATURAL := 50;
    CONSTANT tphl_a1_z      : NATURAL := 75;
    CONSTANT tphh_b_z       : NATURAL := 77;
    CONSTANT tphl_a2_z      : NATURAL := 65;
    CONSTANT tphl_a1_z      : NATURAL := 60;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END oai21bv0x05;

ARCHITECTURE behaviour_data_flow OF oai21bv0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai21bv0x05"
    SEVERITY WARNING;
    z <= not ((a1 or a2) and not b) after 227 ps;
END;

```



3.86 oai21v0x05

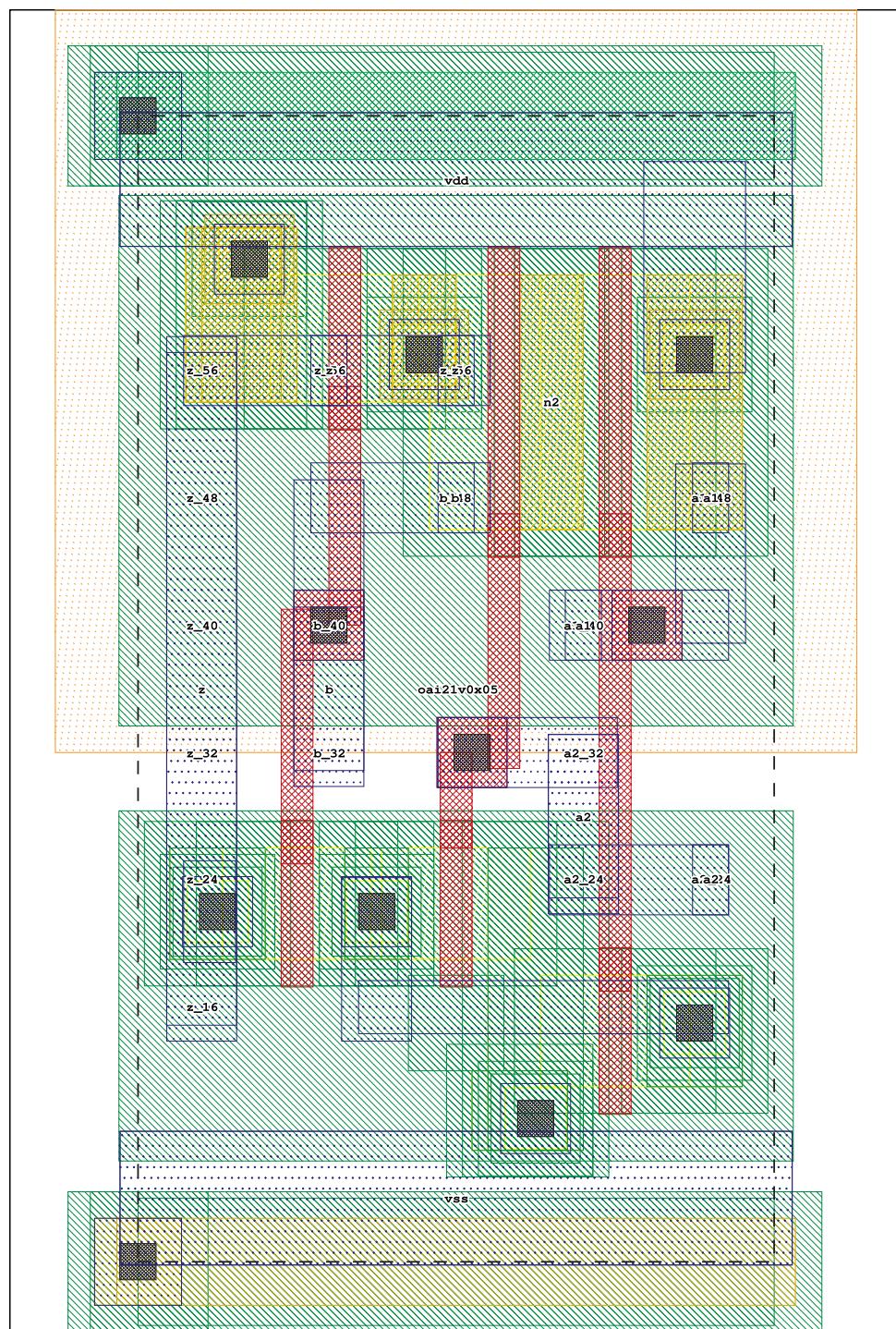
```

ENTITY oai21v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 5310;
    CONSTANT rdown_a2_z     : NATURAL := 5310;
    CONSTANT rdown_b_z      : NATURAL := 4920;
    CONSTANT rup_a1_z       : NATURAL := 7300;
    CONSTANT rup_a2_z       : NATURAL := 7290;
    CONSTANT rup_b_z        : NATURAL := 7460;
    CONSTANT tphl_b_z       : NATURAL := 44;
    CONSTANT tphl_a2_z      : NATURAL := 48;
    CONSTANT tplh_a1_z      : NATURAL := 74;
    CONSTANT tplh_b_z       : NATURAL := 54;
    CONSTANT tplh_a2_z      : NATURAL := 64;
    CONSTANT tphl_a1_z      : NATURAL := 58;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END oai21v0x05;

ARCHITECTURE behaviour_data_flow OF oai21v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai21v0x05"
    SEVERITY WARNING;
    z <= not (((a1 or a2) and b)) after 214 ps;
END;

```



3.87 oai21v0x1

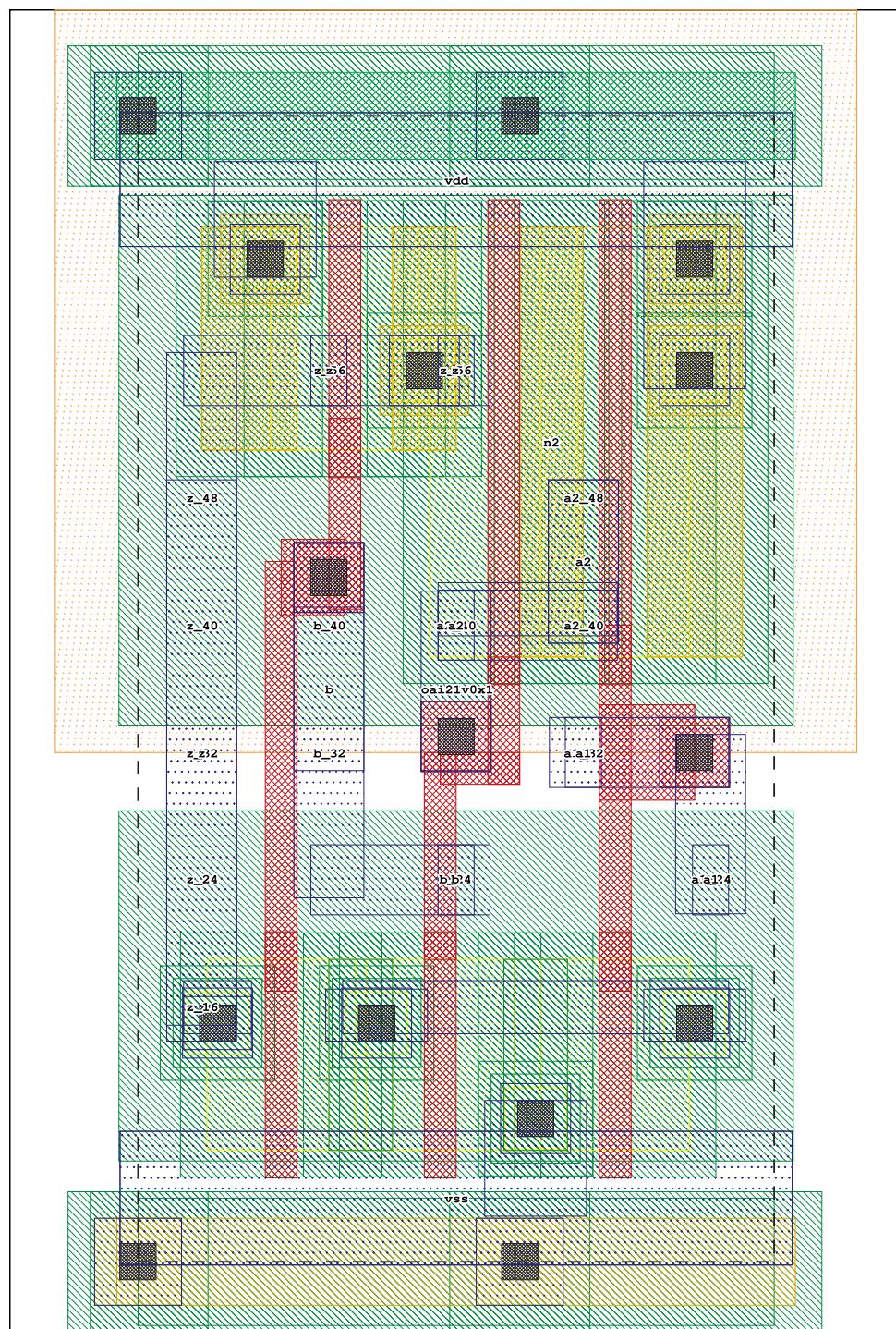
```

ENTITY oai21v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_a1         : NATURAL := 5;
    CONSTANT cin_a2         : NATURAL := 5;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT rdown_a1_z     : NATURAL := 3100;
    CONSTANT rdown_a2_z     : NATURAL := 3110;
    CONSTANT rdown_b_z      : NATURAL := 2880;
    CONSTANT rup_a1_z       : NATURAL := 4320;
    CONSTANT rup_a2_z       : NATURAL := 4320;
    CONSTANT rup_b_z        : NATURAL := 4250;
    CONSTANT tphl_b_z       : NATURAL := 40;
    CONSTANT tphl_a2_z      : NATURAL := 44;
    CONSTANT tplh_a1_z      : NATURAL := 69;
    CONSTANT tplh_b_z       : NATURAL := 50;
    CONSTANT tplh_a2_z      : NATURAL := 60;
    CONSTANT tphl_a1_z      : NATURAL := 53;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END oai21v0x1;

ARCHITECTURE behaviour_data_flow OF oai21v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai21v0x1"
    SEVERITY WARNING;
    z <= not (((a1 or a2) and b)) after 144 ps;
END;

```



3.88 oai21v0x4

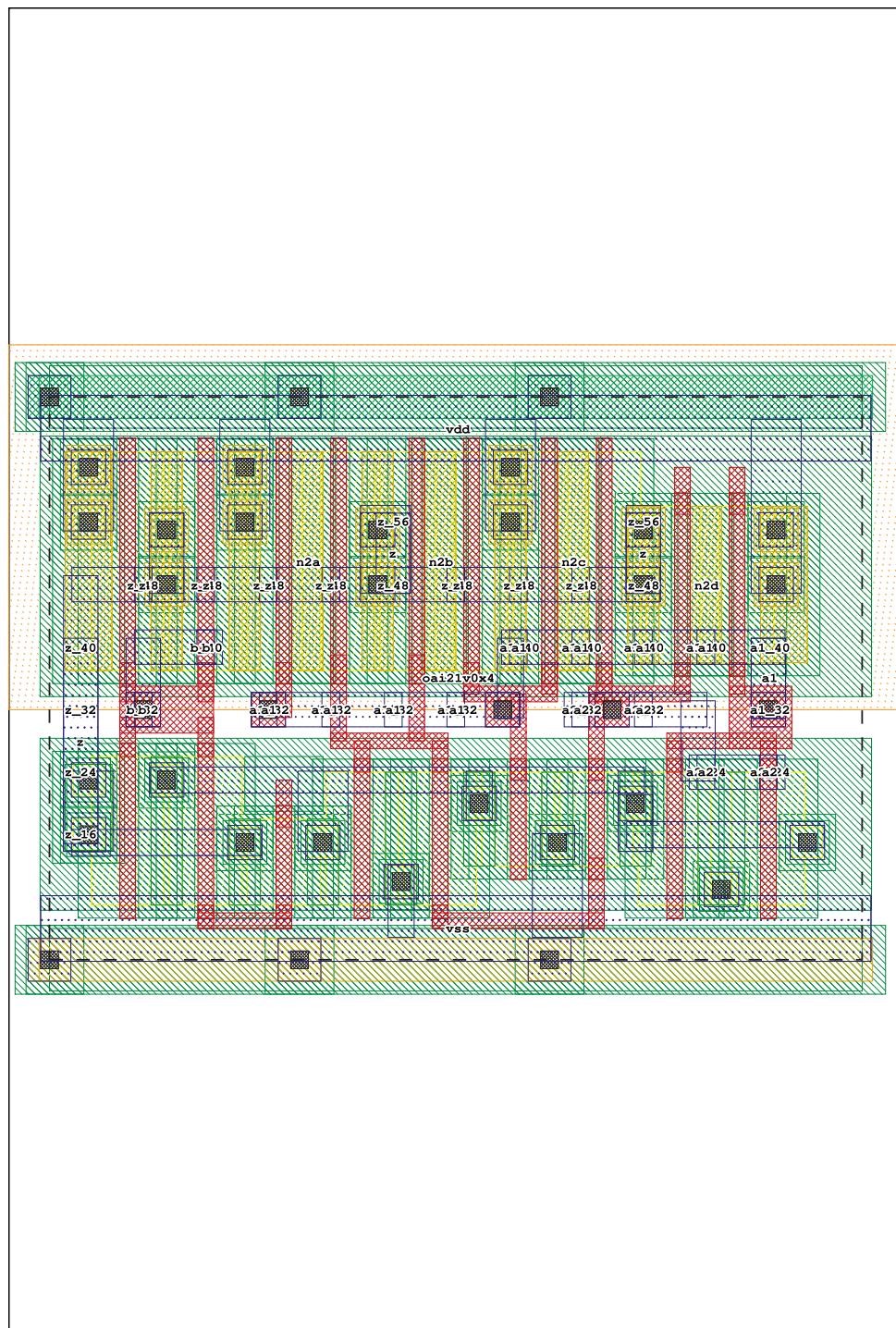
```

ENTITY oai21v0x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 7488;
    CONSTANT cin_a1         : NATURAL := 18;
    CONSTANT cin_a2         : NATURAL := 16;
    CONSTANT cin_b          : NATURAL := 12;
    CONSTANT rdown_a1_z     : NATURAL := 780;
    CONSTANT rdown_a2_z     : NATURAL := 780;
    CONSTANT rdown_b_z      : NATURAL := 720;
    CONSTANT rup_a1_z       : NATURAL := 1120;
    CONSTANT rup_a2_z       : NATURAL := 1120;
    CONSTANT rup_b_z        : NATURAL := 1060;
    CONSTANT tphl_b_z       : NATURAL := 38;
    CONSTANT tphl_a2_z      : NATURAL := 42;
    CONSTANT tplh_a1_z      : NATURAL := 67;
    CONSTANT tplh_b_z       : NATURAL := 47;
    CONSTANT tplh_a2_z      : NATURAL := 58;
    CONSTANT tphl_a1_z      : NATURAL := 51;
    CONSTANT transistors    : NATURAL := 19
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END oai21v0x4;

ARCHITECTURE behaviour_data_flow OF oai21v0x4 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai21v0x4"
    SEVERITY WARNING;
    z <= not (((a1 or a2) and b)) after 74 ps;
END;

```



3.89 oai22v0x05

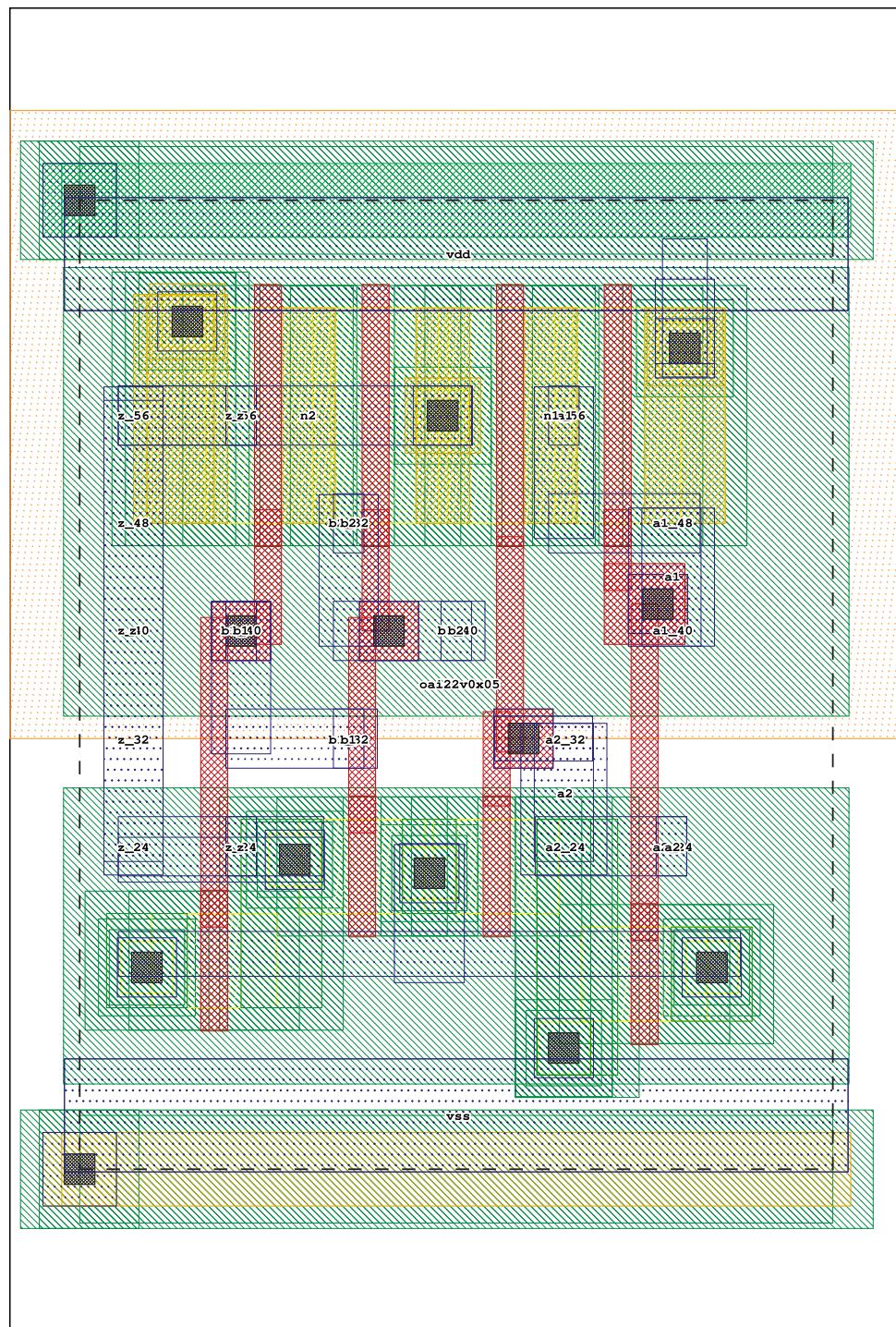
```

ENTITY oai22v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b1         : NATURAL := 3;
    CONSTANT cin_b2         : NATURAL := 3;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT rdown_b1_z     : NATURAL := 4930;
    CONSTANT rdown_b2_z     : NATURAL := 4930;
    CONSTANT rdown_a1_z     : NATURAL := 4880;
    CONSTANT rdown_a2_z     : NATURAL := 4880;
    CONSTANT rup_b1_z       : NATURAL := 7340;
    CONSTANT rup_b2_z       : NATURAL := 7310;
    CONSTANT rup_a1_z       : NATURAL := 7340;
    CONSTANT rup_a2_z       : NATURAL := 7330;
    CONSTANT tphl_a2_z      : NATURAL := 61;
    CONSTANT tphl_b2_z      : NATURAL := 51;
    CONSTANT tplh_b1_z      : NATURAL := 69;
    CONSTANT tphl_a1_z      : NATURAL := 69;
    CONSTANT tplh_b2_z      : NATURAL := 58;
    CONSTANT tphl_b1_z      : NATURAL := 60;
    CONSTANT tplh_a1_z      : NATURAL := 88;
    CONSTANT tplh_a2_z      : NATURAL := 78;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    b1      : in  BIT;
    b2      : in  BIT;
    a1      : in  BIT;
    a2      : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END oai22v0x05;

ARCHITECTURE behaviour_data_flow OF oai22v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on oai22v0x05"
        SEVERITY WARNING;
    z <= not (((b1 or b2) and (a1 or a2))) after 220 ps;
END;

```



3.90 oai23av0x05

ENTITY oai23av0x05 IS

GENERIC (

CONSTANT area	:	NATURAL := 5184;
CONSTANT cin_b1	:	NATURAL := 6;
CONSTANT cin_b2	:	NATURAL := 6;
CONSTANT cin_a2	:	NATURAL := 5;
CONSTANT rdown_b1_z	:	NATURAL := 4940;
CONSTANT rdown_b2_z	:	NATURAL := 4900;
CONSTANT rdown_a2_z	:	NATURAL := 8140;
CONSTANT rup_b1_z	:	NATURAL := 7300;
CONSTANT rup_b2_z	:	NATURAL := 7270;
CONSTANT rup_a2_z	:	NATURAL := 8030;
CONSTANT tphl_a2_z	:	NATURAL := 165;
CONSTANT tphl_b2_z	:	NATURAL := 51;
CONSTANT tp11_b2_z	:	NATURAL := 127;
CONSTANT tphh_b1_z	:	NATURAL := 65;
CONSTANT tphh_b1_z	:	NATURAL := 120;
CONSTANT tphh_a2_z	:	NATURAL := 238;
CONSTANT tphh_b2_z	:	NATURAL := 57;
CONSTANT tphh_b2_z	:	NATURAL := 119;
CONSTANT tphl_b1_z	:	NATURAL := 58;
CONSTANT tp11_b1_z	:	NATURAL := 132;
CONSTANT transistors	:	NATURAL := 12

);

PORt (

b1	:	in BIT;
b2	:	in BIT;
a2	:	in BIT;
z	:	out BIT;
vdd	:	in BIT;
vss	:	in BIT

);

END oai23av0x05;

ARCHITECTURE behaviour_data_flow OF oai23av0x05 IS

BEGIN

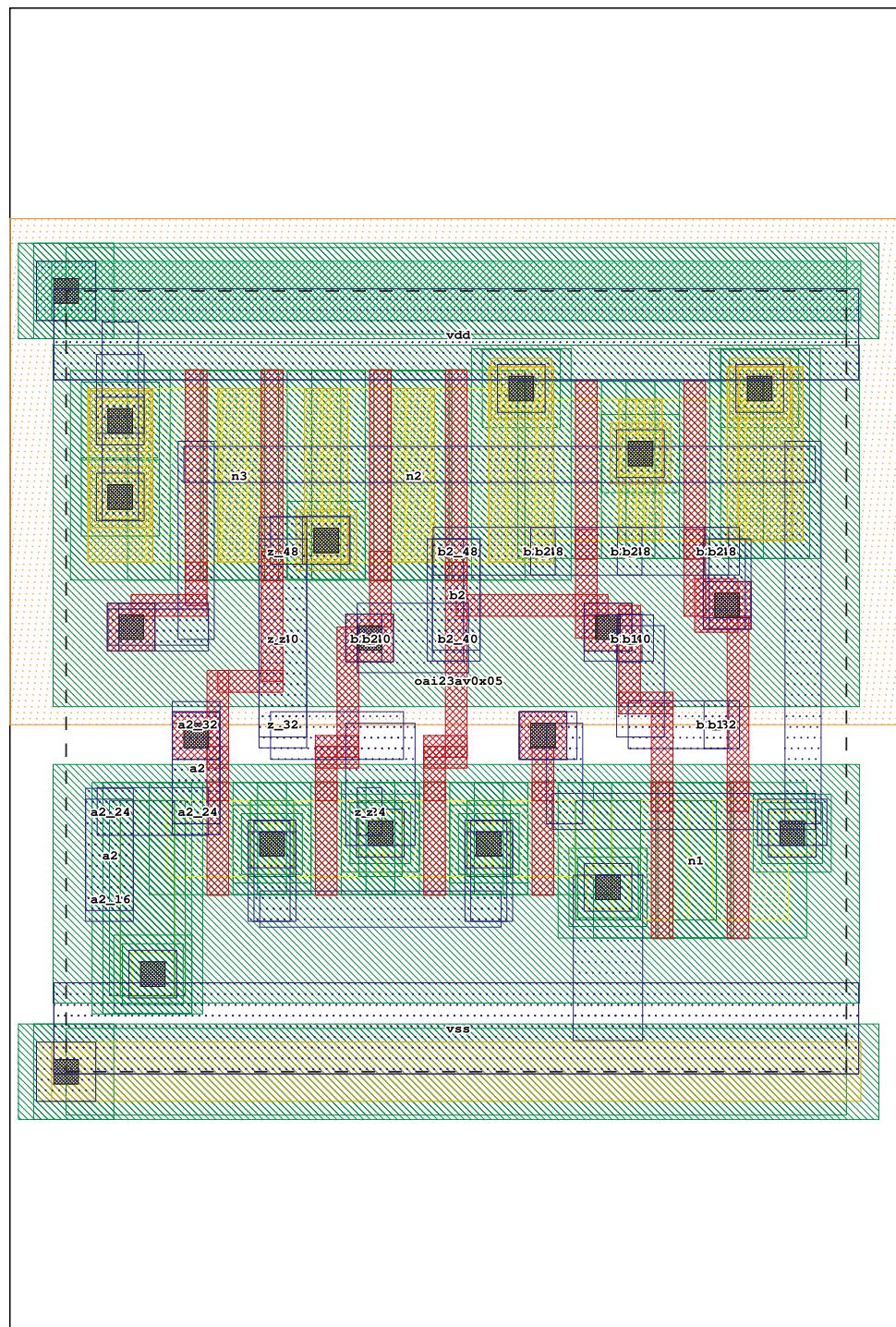
ASSERT ((vdd and not (vss)) = '1')

REPORT "power supply is missing on oai23av0x05"

SEVERITY WARNING;

z <= (not b1 and not b2) or (not a2 and (b1 and b2)) after 234 ps;

END;



3.91 oai31v0x05

```

ENTITY oai31v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_b         : NATURAL := 3;
    CONSTANT cin_a3        : NATURAL := 5;
    CONSTANT cin_a2        : NATURAL := 5;
    CONSTANT cin_a1        : NATURAL := 5;
    CONSTANT rdown_b_z     : NATURAL := 3630;
    CONSTANT rdown_a3_z    : NATURAL := 4190;
    CONSTANT rdown_a2_z    : NATURAL := 4180;
    CONSTANT rdown_a1_z    : NATURAL := 4280;
    CONSTANT rup_b_z       : NATURAL := 5430;
    CONSTANT rup_a3_z      : NATURAL := 6510;
    CONSTANT rup_a2_z      : NATURAL := 6510;
    CONSTANT rup_a1_z      : NATURAL := 6510;
    CONSTANT tphl_a1_z     : NATURAL := 71;
    CONSTANT tphl_a3_z     : NATURAL := 50;
    CONSTANT tplh_b_z      : NATURAL := 52;
    CONSTANT tphl_a2_z     : NATURAL := 64;
    CONSTANT tplh_a3_z     : NATURAL := 67;
    CONSTANT tphl_b_z      : NATURAL := 45;
    CONSTANT tplh_a2_z     : NATURAL := 89;
    CONSTANT tplh_a1_z     : NATURAL := 97;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    b      : in  BIT;
    a3     : in  BIT;
    a2     : in  BIT;
    a1     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END oai31v0x05;

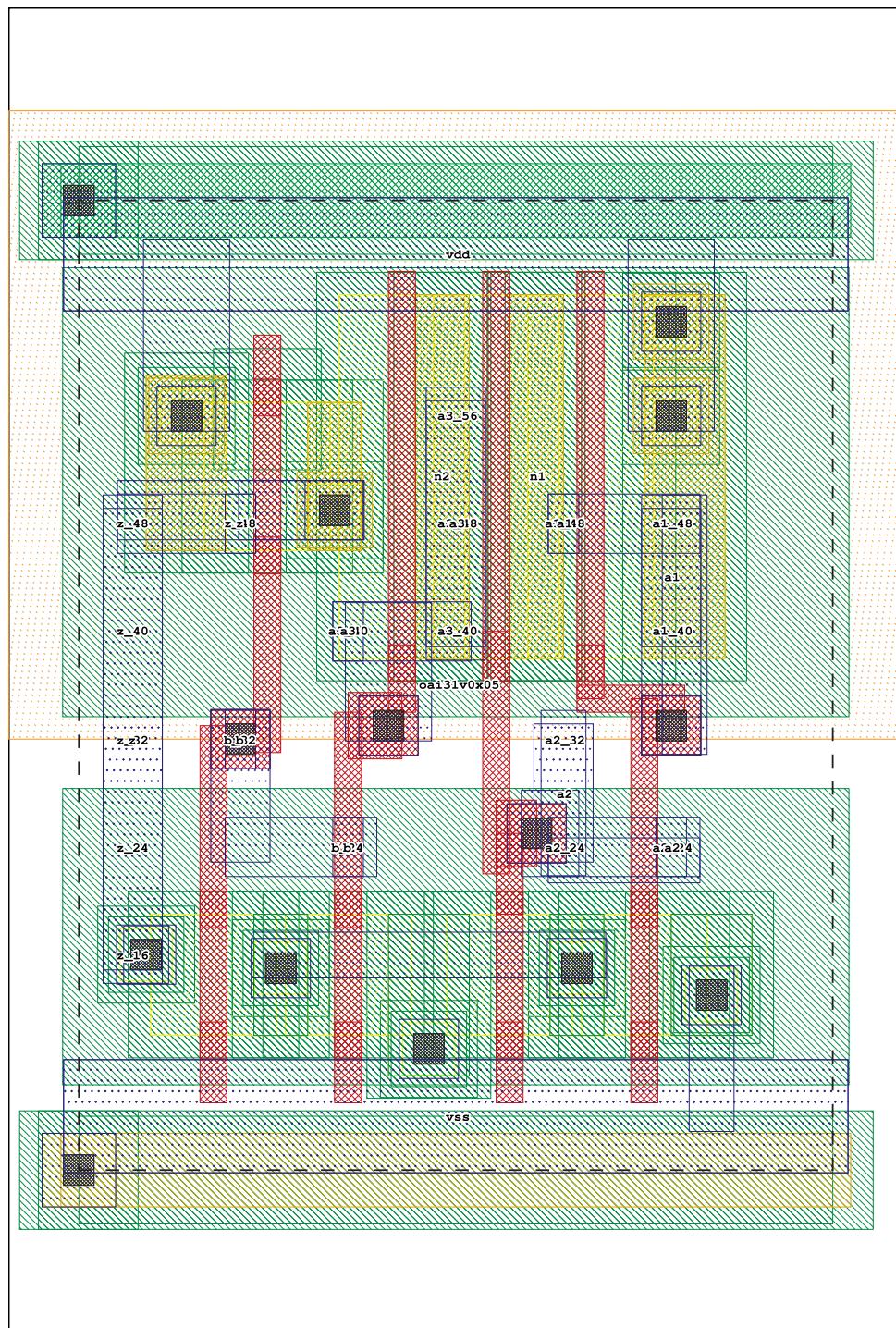
```

ARCHITECTURE behaviour_data_flow OF oai31v0x05 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai31v0x05"
    SEVERITY WARNING;
    z <= not(b and ((a1 or a2) or a3)) after 196 ps;
END;

```



3.92 oai31v0x1

```

ENTITY oai31v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_b         : NATURAL := 5;
    CONSTANT cin_a3        : NATURAL := 8;
    CONSTANT cin_a2        : NATURAL := 8;
    CONSTANT cin_a1        : NATURAL := 9;
    CONSTANT rdown_b_z     : NATURAL := 2040;
    CONSTANT rdown_a3_z    : NATURAL := 2350;
    CONSTANT rdown_a2_z    : NATURAL := 2350;
    CONSTANT rdown_a1_z    : NATURAL := 2400;
    CONSTANT rup_b_z       : NATURAL := 3150;
    CONSTANT rup_a3_z      : NATURAL := 3370;
    CONSTANT rup_a2_z      : NATURAL := 3380;
    CONSTANT rup_a1_z      : NATURAL := 3380;
    CONSTANT tphl_a1_z     : NATURAL := 74;
    CONSTANT tphl_a3_z     : NATURAL := 51;
    CONSTANT tplh_b_z      : NATURAL := 53;
    CONSTANT tphl_a2_z     : NATURAL := 66;
    CONSTANT tplh_a3_z     : NATURAL := 63;
    CONSTANT tphl_b_z      : NATURAL := 47;
    CONSTANT tplh_a2_z     : NATURAL := 85;
    CONSTANT tplh_a1_z     : NATURAL := 95;
    CONSTANT transistors   : NATURAL := 11
);
PORT (
    b      : in  BIT;
    a3     : in  BIT;
    a2     : in  BIT;
    a1     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END oai31v0x1 ;

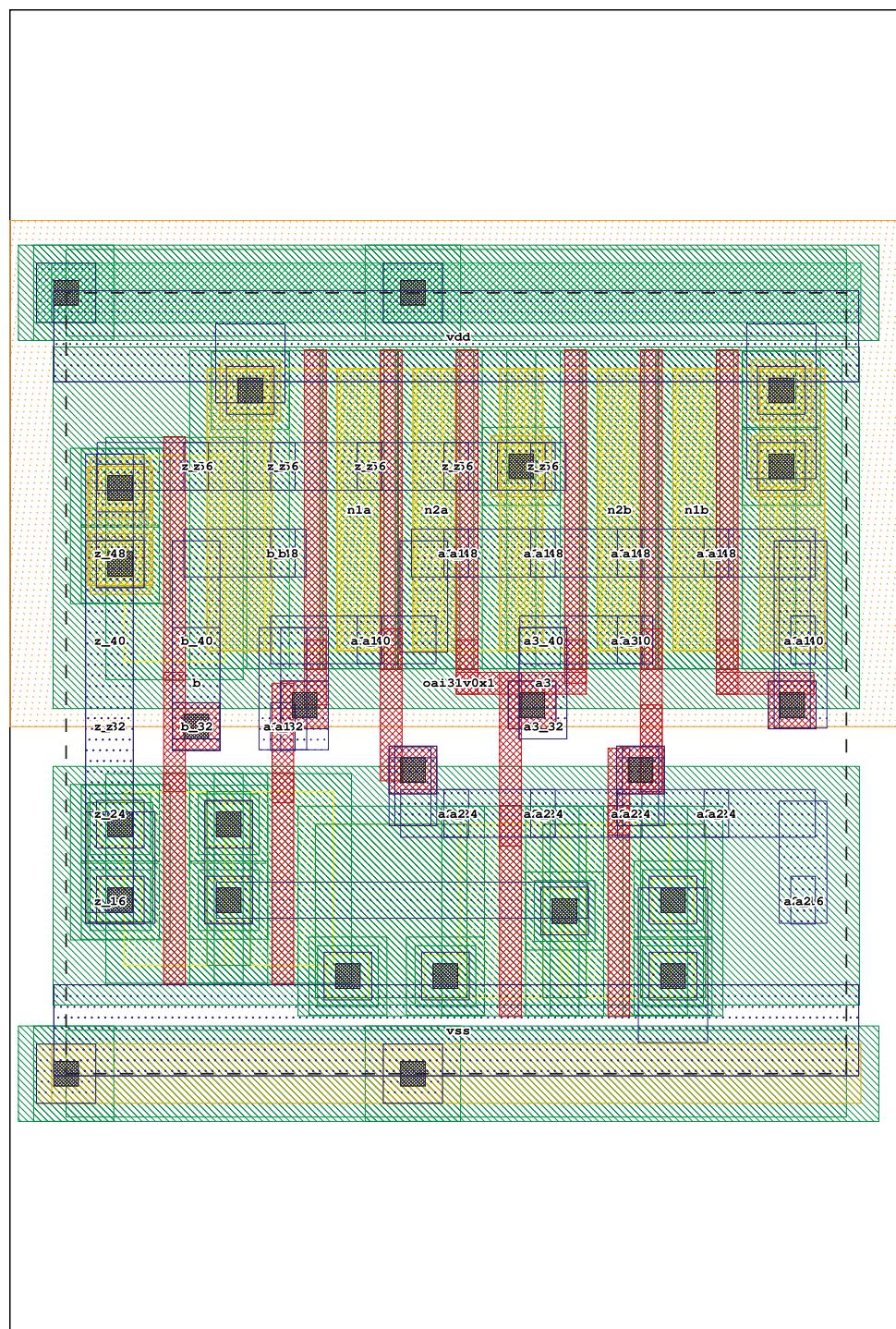
```

ARCHITECTURE behaviour_data_flow OF oai31v0x1 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oai31v0x1"
    SEVERITY WARNING;
    z <= not(b and ((a1 or a2) or a3)) after 137 ps;
END;

```



3.93 oan21bv0x05

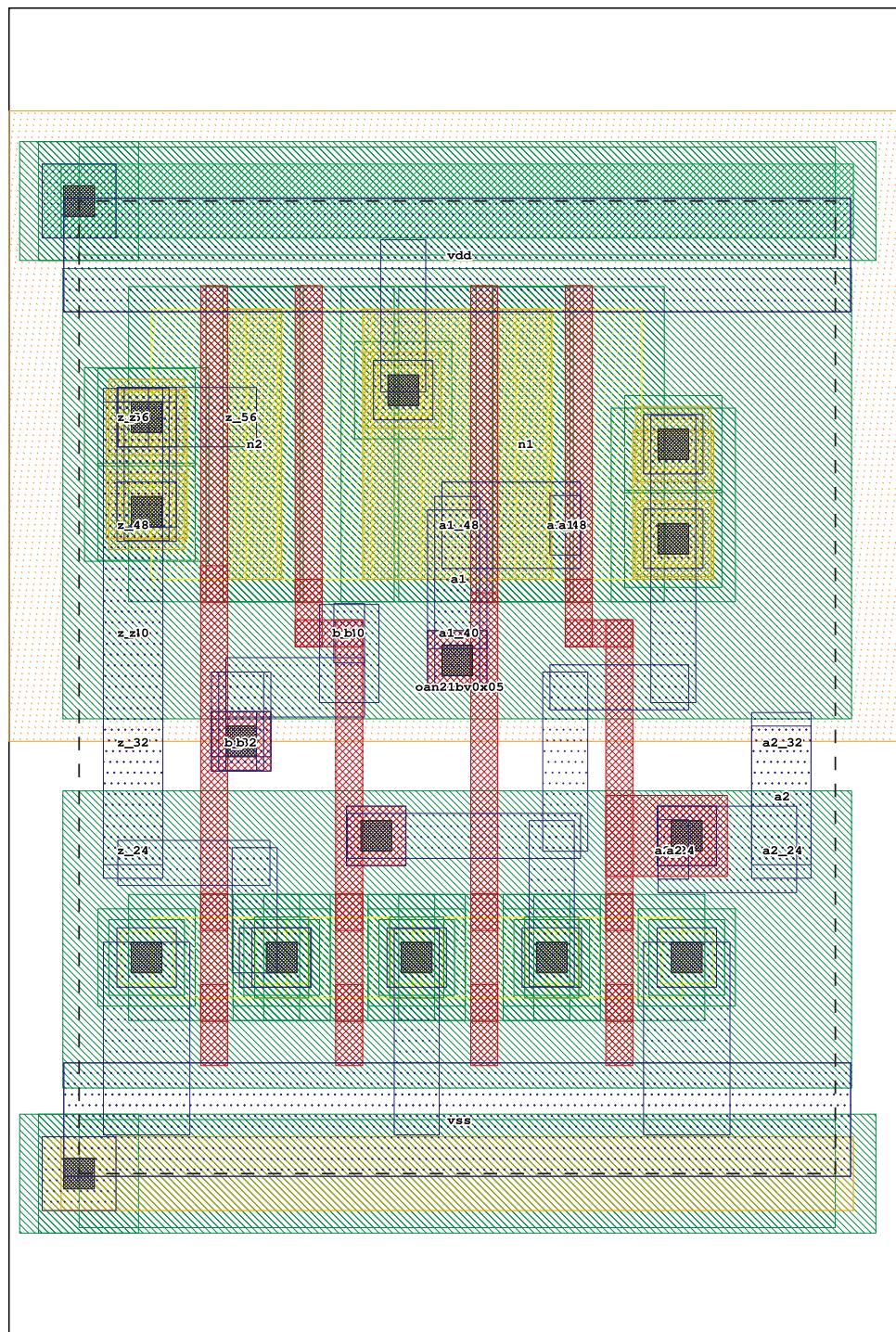
```

ENTITY oan21bv0x05 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a2         : NATURAL := 4;
    CONSTANT cin_a1         : NATURAL := 4;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT rdown_a2_z     : NATURAL := 3930;
    CONSTANT rdown_a1_z     : NATURAL := 3930;
    CONSTANT rdown_b_z      : NATURAL := 3850;
    CONSTANT rup_a2_z       : NATURAL := 5830;
    CONSTANT rup_a1_z       : NATURAL := 5830;
    CONSTANT rup_b_z        : NATURAL := 5810;
    CONSTANT tphl_b_z       : NATURAL := 42;
    CONSTANT tplh_b_z       : NATURAL := 47;
    CONSTANT tp11_a2_z      : NATURAL := 114;
    CONSTANT tp11_a1_z      : NATURAL := 108;
    CONSTANT tp11_a1_z      : NATURAL := 123;
    CONSTANT tp11_a2_z      : NATURAL := 96;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    a2      : in  BIT;
    a1      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END oan21bv0x05;

ARCHITECTURE behaviour_data_flow OF oan21bv0x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oan21bv0x05"
    SEVERITY WARNING;
  z <= not b and (a1 or a2) after 210 ps;
END;

```



3.94 oan21v0x05

```

ENTITY oan21v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_a1         : NATURAL := 3;
    CONSTANT cin_a2         : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT rdown_a1_z     : NATURAL := 3980;
    CONSTANT rdown_a2_z     : NATURAL := 3980;
    CONSTANT rdown_b_z      : NATURAL := 3940;
    CONSTANT rup_a1_z       : NATURAL := 5000;
    CONSTANT rup_a2_z       : NATURAL := 4970;
    CONSTANT rup_b_z        : NATURAL := 4970;
    CONSTANT tphh_b_z       : NATURAL := 79;
    CONSTANT tppll_b_z      : NATURAL := 102;
    CONSTANT tppll_a1_z     : NATURAL := 128;
    CONSTANT tppll_a2_z     : NATURAL := 87;
    CONSTANT tphh_a2_z      : NATURAL := 120;
    CONSTANT tphh_a1_z      : NATURAL := 98;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a1      : in  BIT;
    a2      : in  BIT;
    b       : in  BIT;
    z       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END oan21v0x05;

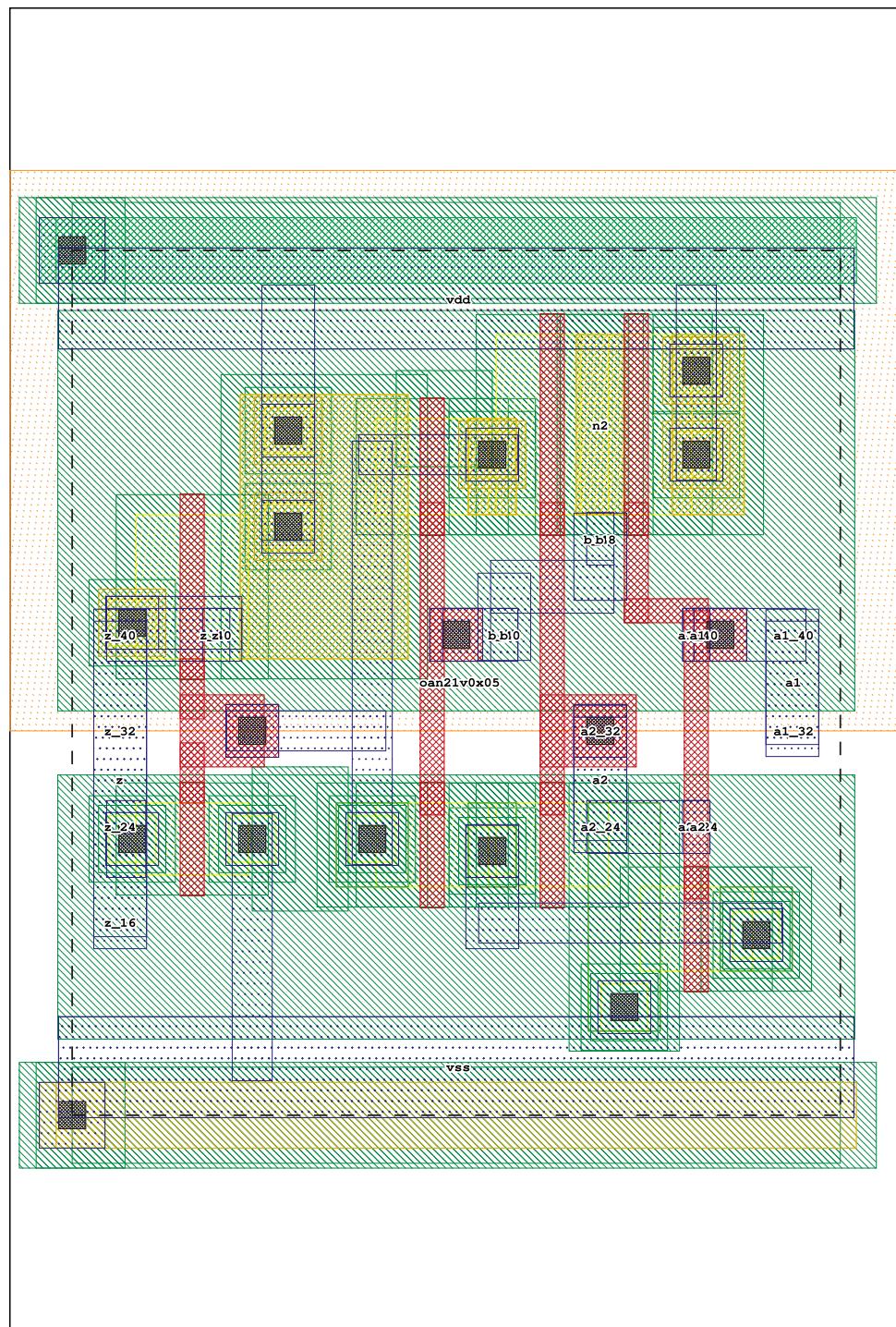
```

```

ARCHITECTURE behaviour_data_flow OF oan21v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on oan21v0x05"
    SEVERITY WARNING;
    z <= (a1 or a2) and b after 214 ps;
END;

```



3.95 or2v0x05

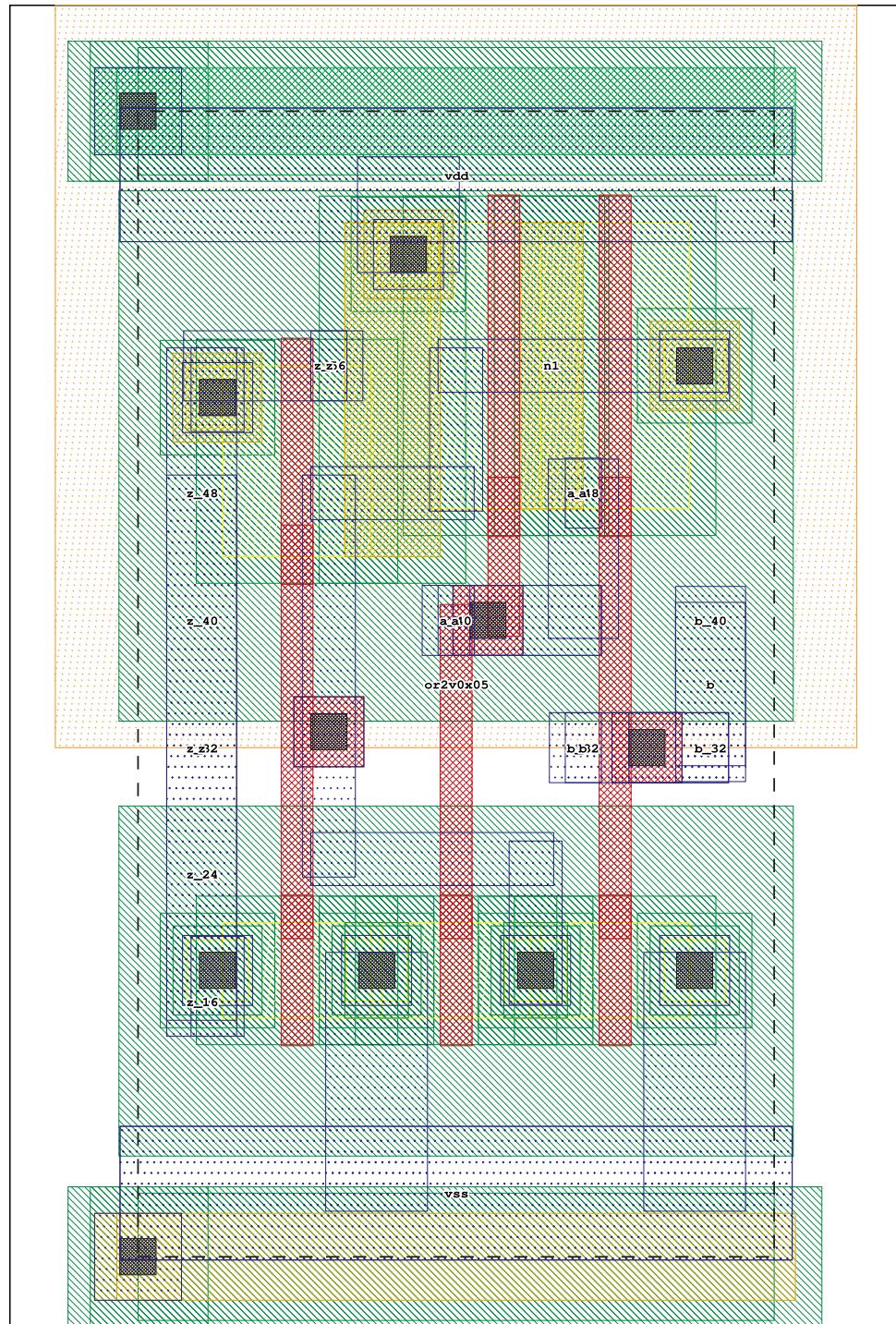
```

ENTITY or2v0x05 IS
GENERIC (
  CONSTANT area      : NATURAL := 2880;
  CONSTANT cin_a     : NATURAL := 4;
  CONSTANT cin_b     : NATURAL := 4;
  CONSTANT rdown_a_z : NATURAL := 3920;
  CONSTANT rdown_b_z : NATURAL := 3920;
  CONSTANT rup_a_z   : NATURAL := 4970;
  CONSTANT rup_b_z   : NATURAL := 4960;
  CONSTANT tpll_a_z  : NATURAL := 107;
  CONSTANT tphh_b_z  : NATURAL := 74;
  CONSTANT tpll_b_z  : NATURAL := 97;
  CONSTANT tphh_a_z  : NATURAL := 86;
  CONSTANT transistors : NATURAL := 6
);
PORT (
  a      : in  BIT;
  b      : in  BIT;
  z      : out BIT;
  vdd    : in  BIT;
  vss    : in  BIT
);
END or2v0x05;

ARCHITECTURE behaviour_data_flow OF or2v0x05 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on or2v0x05"
  SEVERITY WARNING;
  z <= (a or b) after 202 ps;
END;

```



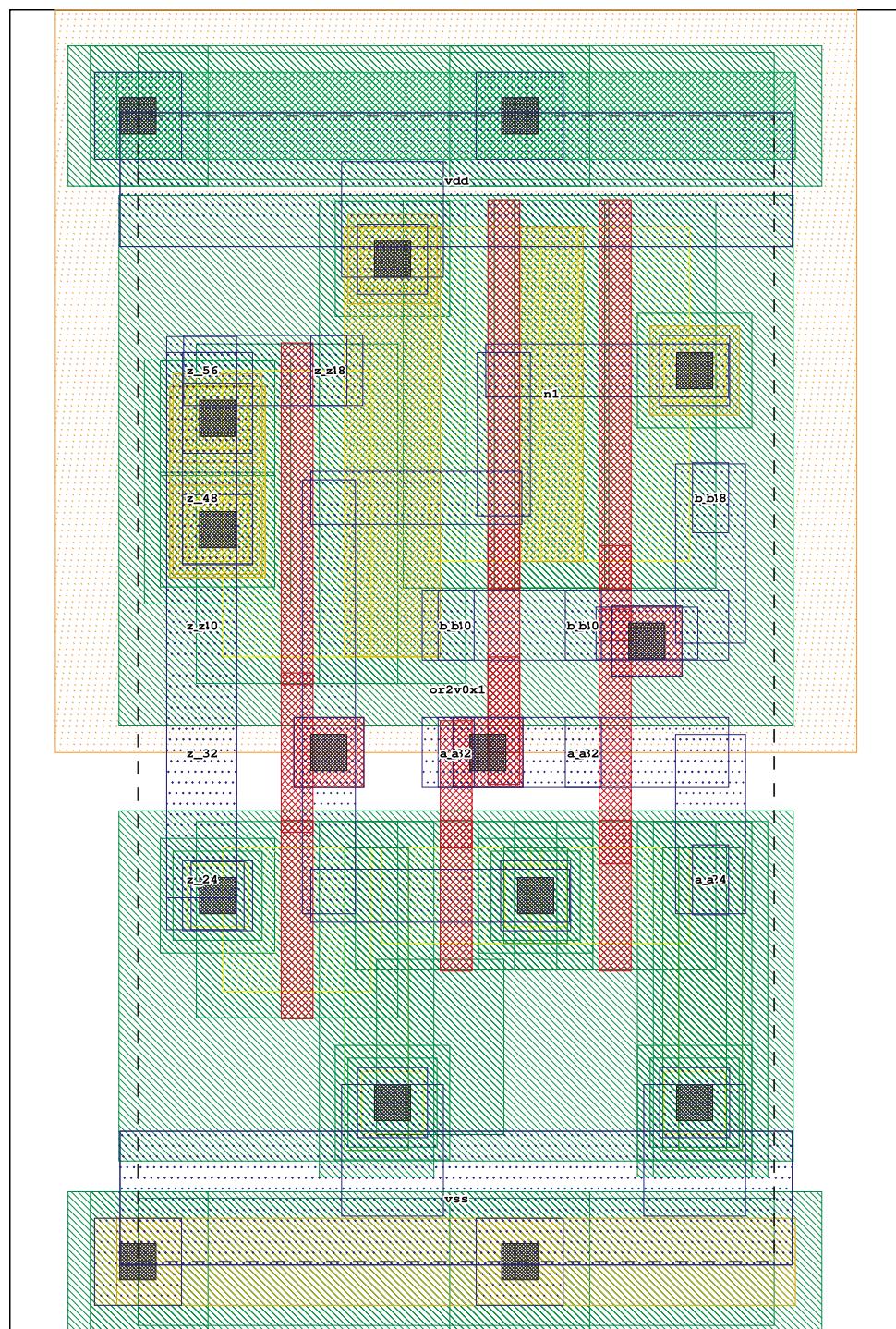
3.96 or2v0x1

```

ENTITY or2v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 2880;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT rdown_a_z      : NATURAL := 2660;
    CONSTANT rdown_b_z      : NATURAL := 2670;
    CONSTANT rup_a_z        : NATURAL := 3330;
    CONSTANT rup_b_z        : NATURAL := 3320;
    CONSTANT tpll_a_z       : NATURAL := 104;
    CONSTANT tphh_b_z       : NATURAL := 79;
    CONSTANT tpll_b_z       : NATURAL := 95;
    CONSTANT tphh_a_z       : NATURAL := 91;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END or2v0x1;

ARCHITECTURE behaviour_data_flow OF or2v0x1 IS
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on or2v0x1"
    SEVERITY WARNING;
    z <= (a or b) after 167 ps;
END;

```



3.97 or3v0x05

```

ENTITY or3v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT cin_b         : NATURAL := 4;
    CONSTANT cin_c         : NATURAL := 4;
    CONSTANT rdown_a_z     : NATURAL := 4070;
    CONSTANT rdown_b_z     : NATURAL := 4070;
    CONSTANT rdown_c_z     : NATURAL := 4070;
    CONSTANT rup_a_z       : NATURAL := 5030;
    CONSTANT rup_b_z       : NATURAL := 4980;
    CONSTANT rup_c_z       : NATURAL := 4960;
    CONSTANT tphh_c_z      : NATURAL := 85;
    CONSTANT tp_ll_a_z     : NATURAL := 143;
    CONSTANT tp_ll_b_z     : NATURAL := 100;
    CONSTANT tp_ll_b_z     : NATURAL := 134;
    CONSTANT tp_ll_a_z     : NATURAL := 109;
    CONSTANT tp_ll_c_z     : NATURAL := 113;
    CONSTANT transistors   : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END or3v0x05;

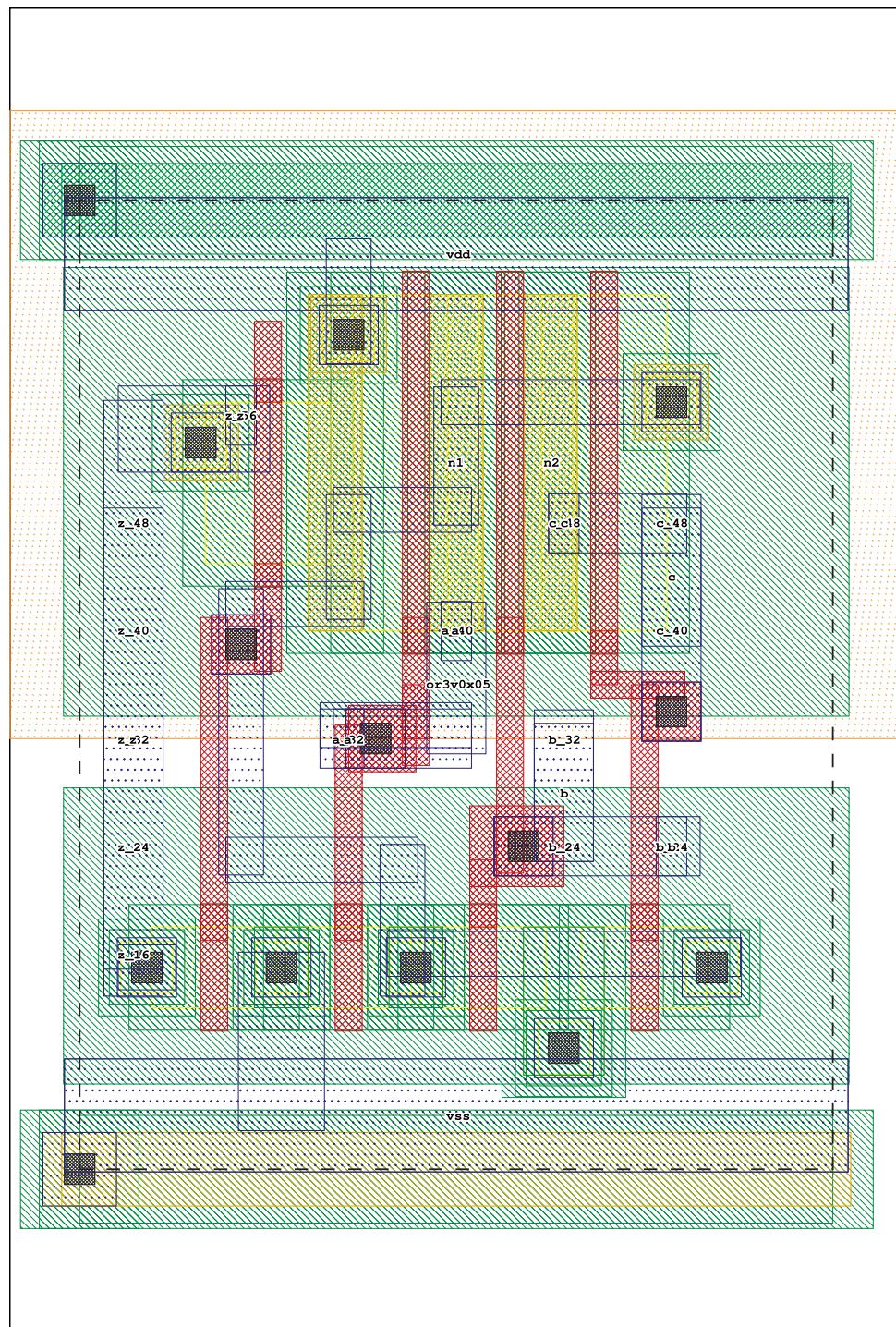
```

```

ARCHITECTURE behaviour_data_flow OF or3v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on or3v0x05"
    SEVERITY WARNING;
    z <= ((a or b) or c) after 227 ps;
END;

```



3.98 or3v0x1

```

ENTITY or3v0x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a          : NATURAL := 5;
    CONSTANT cin_b          : NATURAL := 5;
    CONSTANT cin_c          : NATURAL := 5;
    CONSTANT rdown_a_z      : NATURAL := 2690;
    CONSTANT rdown_b_z      : NATURAL := 2690;
    CONSTANT rdown_c_z      : NATURAL := 2690;
    CONSTANT rup_a_z        : NATURAL := 3170;
    CONSTANT rup_b_z        : NATURAL := 3150;
    CONSTANT rup_c_z        : NATURAL := 3130;
    CONSTANT tphh_c_z       : NATURAL := 91;
    CONSTANT tpLL_a_z       : NATURAL := 147;
    CONSTANT tphh_b_z       : NATURAL := 107;
    CONSTANT tpLL_b_z       : NATURAL := 137;
    CONSTANT tphh_a_z       : NATURAL := 118;
    CONSTANT tpLL_c_z       : NATURAL := 116;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END or3v0x1;

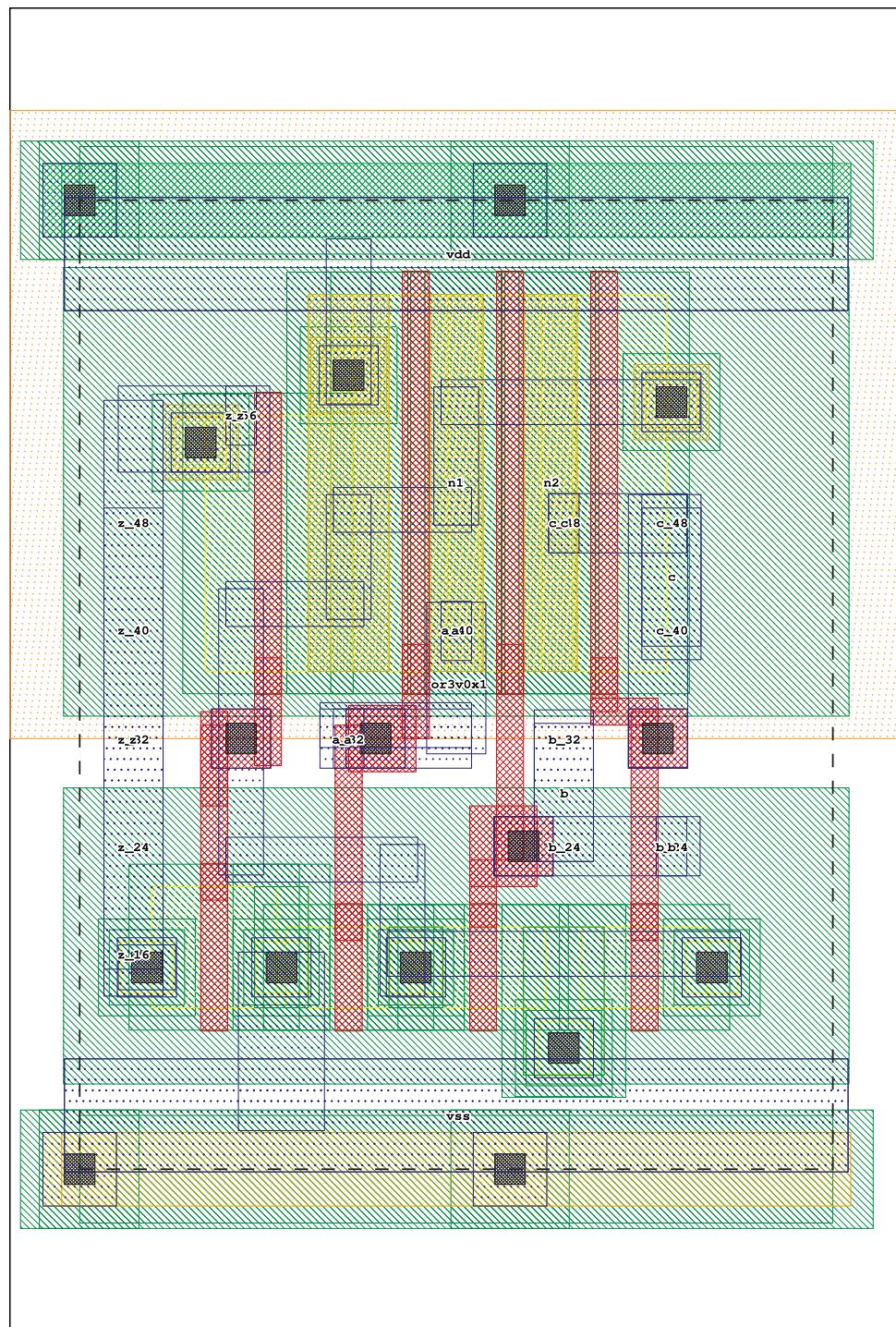
```

```

ARCHITECTURE behaviour_data_flow OF or3v0x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on or3v0x1"
    SEVERITY WARNING;
    z <= ((a or b) or c) after 192 ps;
END;

```



3.99 or3v0x2

```

ENTITY or3v0x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_a          : NATURAL := 7;
    CONSTANT cin_b          : NATURAL := 6;
    CONSTANT cin_c          : NATURAL := 6;
    CONSTANT rdown_a_z      : NATURAL := 1740;
    CONSTANT rdown_b_z      : NATURAL := 1740;
    CONSTANT rdown_c_z      : NATURAL := 1740;
    CONSTANT rup_a_z        : NATURAL := 2160;
    CONSTANT rup_b_z        : NATURAL := 2140;
    CONSTANT rup_c_z        : NATURAL := 2130;
    CONSTANT tphh_c_z       : NATURAL := 87;
    CONSTANT tp_ll_a_z      : NATURAL := 136;
    CONSTANT tp_ll_b_z      : NATURAL := 105;
    CONSTANT tp_ll_c_z      : NATURAL := 125;
    CONSTANT tp_hh_a_z      : NATURAL := 118;
    CONSTANT tp_hh_c_z      : NATURAL := 103;
    CONSTANT transistors    : NATURAL := 11
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd   : in  BIT;
    vss   : in  BIT
);
END or3v0x2;

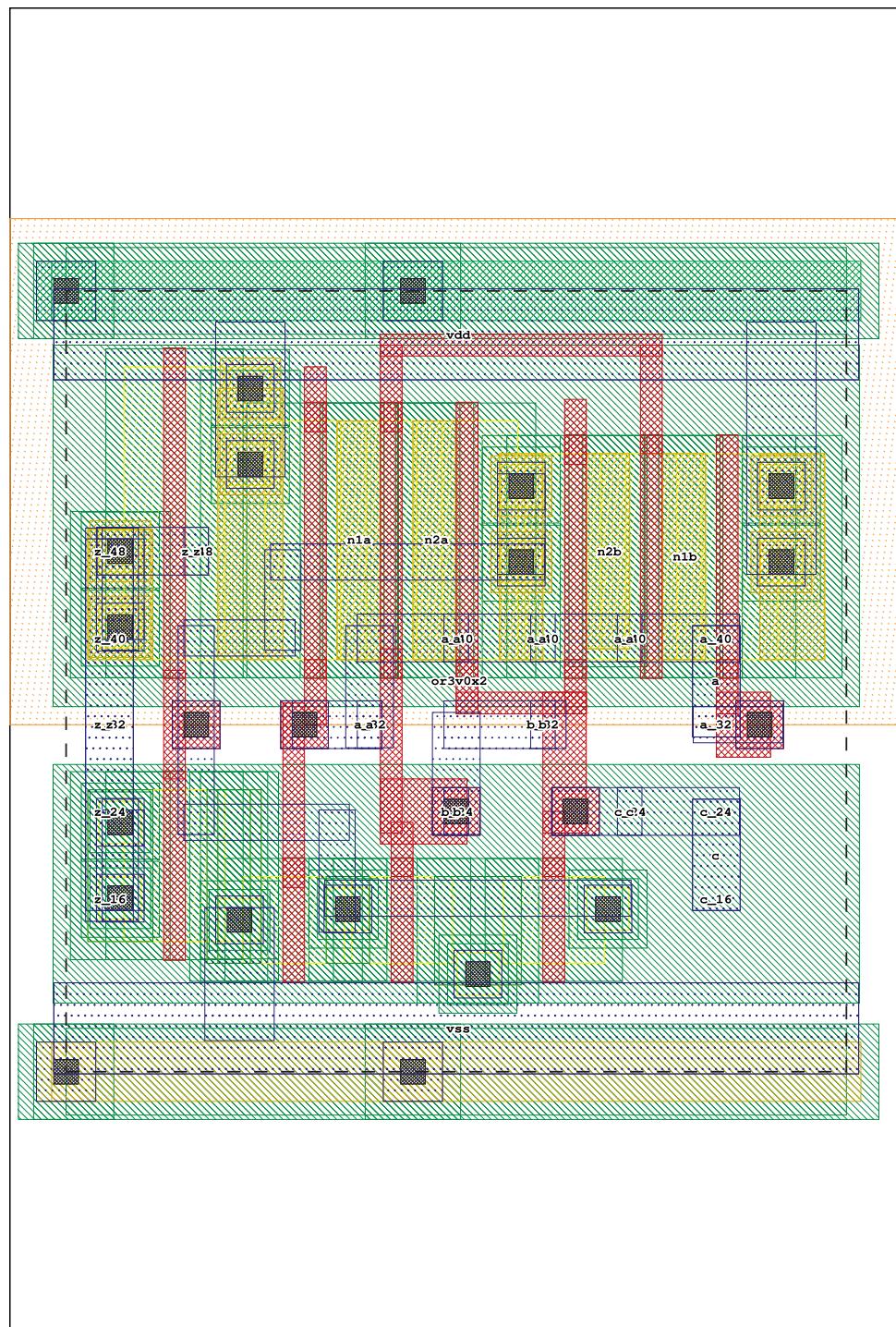
```

```

ARCHITECTURE behaviour_data_flow OF or3v0x2 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on or3v0x2"
    SEVERITY WARNING;
    z <= ((a or b) or c) after 161 ps;
END;

```



3.100 or3v4x05

```

ENTITY or3v4x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4032;
    CONSTANT cin_a          : NATURAL := 3;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT cin_c          : NATURAL := 3;
    CONSTANT rdown_a_z      : NATURAL := 4430;
    CONSTANT rdown_b_z      : NATURAL := 4440;
    CONSTANT rdown_c_z      : NATURAL := 4430;
    CONSTANT rup_a_z         : NATURAL := 4990;
    CONSTANT rup_b_z         : NATURAL := 4970;
    CONSTANT rup_c_z         : NATURAL := 4960;
    CONSTANT tphh_c_z        : NATURAL := 75;
    CONSTANT tp_ll_a_z       : NATURAL := 212;
    CONSTANT tp_ll_b_z       : NATURAL := 81;
    CONSTANT tp_ll_b_z       : NATURAL := 198;
    CONSTANT tp_ll_a_z       : NATURAL := 85;
    CONSTANT tp_ll_c_z       : NATURAL := 176;
    CONSTANT transistors     : NATURAL := 8
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END or3v4x05;

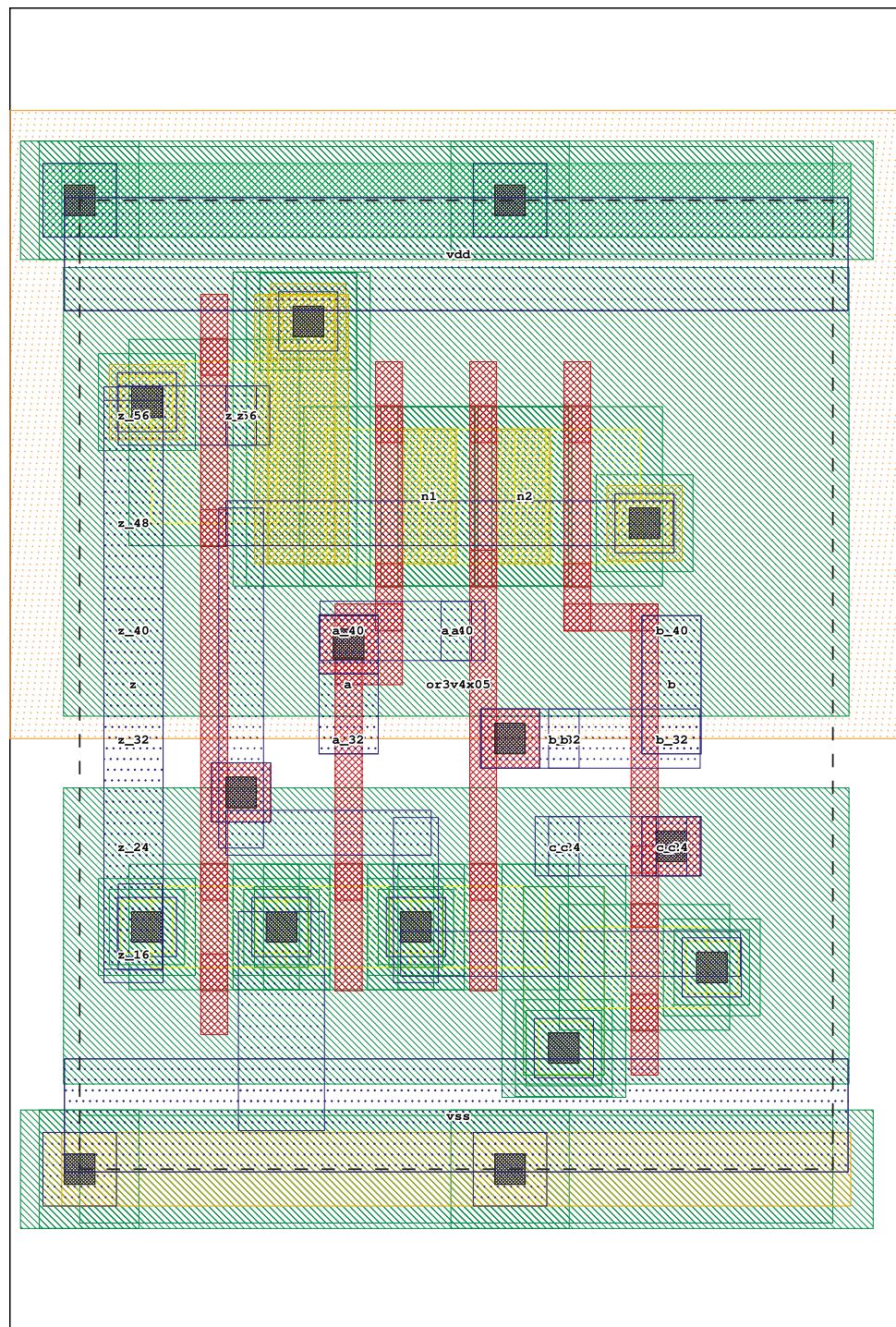
```

```

ARCHITECTURE behaviour_data_flow OF or3v4x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on or3v4x05"
    SEVERITY WARNING;
    z <= ((a or b) or c) after 255 ps;
END;

```



3.101 or4v0x05

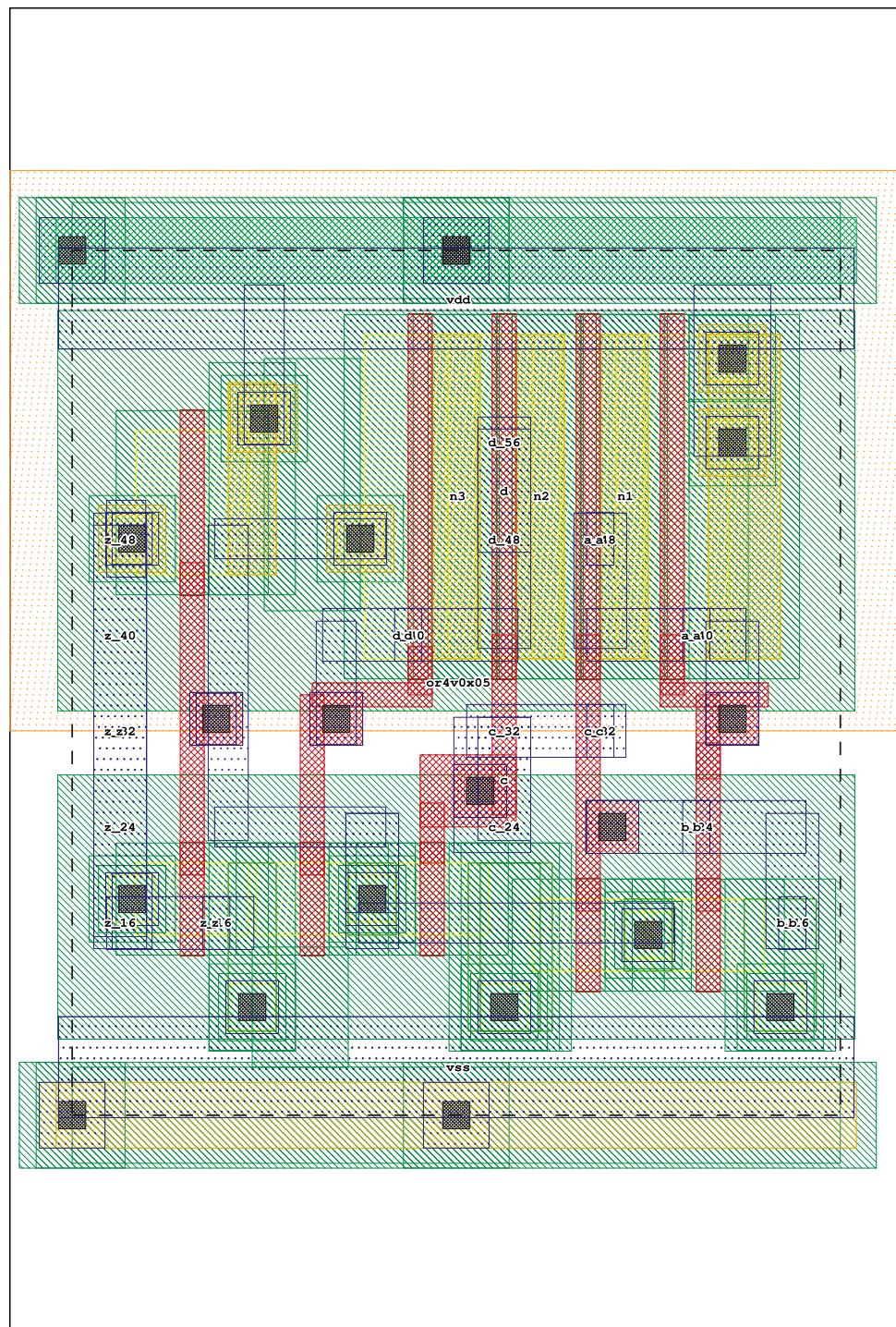
```

ENTITY or4v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT cin_c          : NATURAL := 4;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT cin_d          : NATURAL := 5;
    CONSTANT rdown_b_z      : NATURAL := 4290;
    CONSTANT rdown_c_z      : NATURAL := 4290;
    CONSTANT rdown_a_z      : NATURAL := 4290;
    CONSTANT rdown_d_z      : NATURAL := 4280;
    CONSTANT rup_b_z        : NATURAL := 5030;
    CONSTANT rup_c_z        : NATURAL := 4980;
    CONSTANT rup_a_z        : NATURAL := 5100;
    CONSTANT rup_d_z        : NATURAL := 4960;
    CONSTANT tphh_d_z       : NATURAL := 86;
    CONSTANT tphh_c_z       : NATURAL := 101;
    CONSTANT tphh_b_z       : NATURAL := 111;
    CONSTANT tp11_a_z       : NATURAL := 184;
    CONSTANT tp11_a_z       : NATURAL := 116;
    CONSTANT tp11_b_z       : NATURAL := 175;
    CONSTANT tp11_d_z       : NATURAL := 123;
    CONSTANT tp11_c_z       : NATURAL := 155;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    d      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END or4v0x05;

ARCHITECTURE behaviour_data_flow OF or4v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on or4v0x05"
    SEVERITY WARNING;
    z <= (((b or c) or a) or d) after 248 ps;
END;

```



3.102 or4v4x05

```

ENTITY or4v4x05 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_b          : NATURAL := 3;
    CONSTANT cin_c          : NATURAL := 3;
    CONSTANT cin_a          : NATURAL := 3;
    CONSTANT cin_d          : NATURAL := 3;
    CONSTANT rdown_b_z      : NATURAL := 4650;
    CONSTANT rdown_c_z      : NATURAL := 4650;
    CONSTANT rdown_a_z      : NATURAL := 4650;
    CONSTANT rdown_d_z      : NATURAL := 4650;
    CONSTANT rup_b_z        : NATURAL := 4990;
    CONSTANT rup_c_z        : NATURAL := 4970;
    CONSTANT rup_a_z        : NATURAL := 5030;
    CONSTANT rup_d_z        : NATURAL := 4960;
    CONSTANT tphh_d_z       : NATURAL := 75;
    CONSTANT tphh_c_z       : NATURAL := 82;
    CONSTANT tphh_b_z       : NATURAL := 86;
    CONSTANT tp11_a_z       : NATURAL := 246;
    CONSTANT tp11_a_z       : NATURAL := 87;
    CONSTANT tp11_b_z       : NATURAL := 237;
    CONSTANT tp11_d_z       : NATURAL := 184;
    CONSTANT tp11_c_z       : NATURAL := 216;
    CONSTANT transistors    : NATURAL := 10
  );
  PORT (
    b      : in  BIT;
    c      : in  BIT;
    a      : in  BIT;
    d      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END or4v4x05;

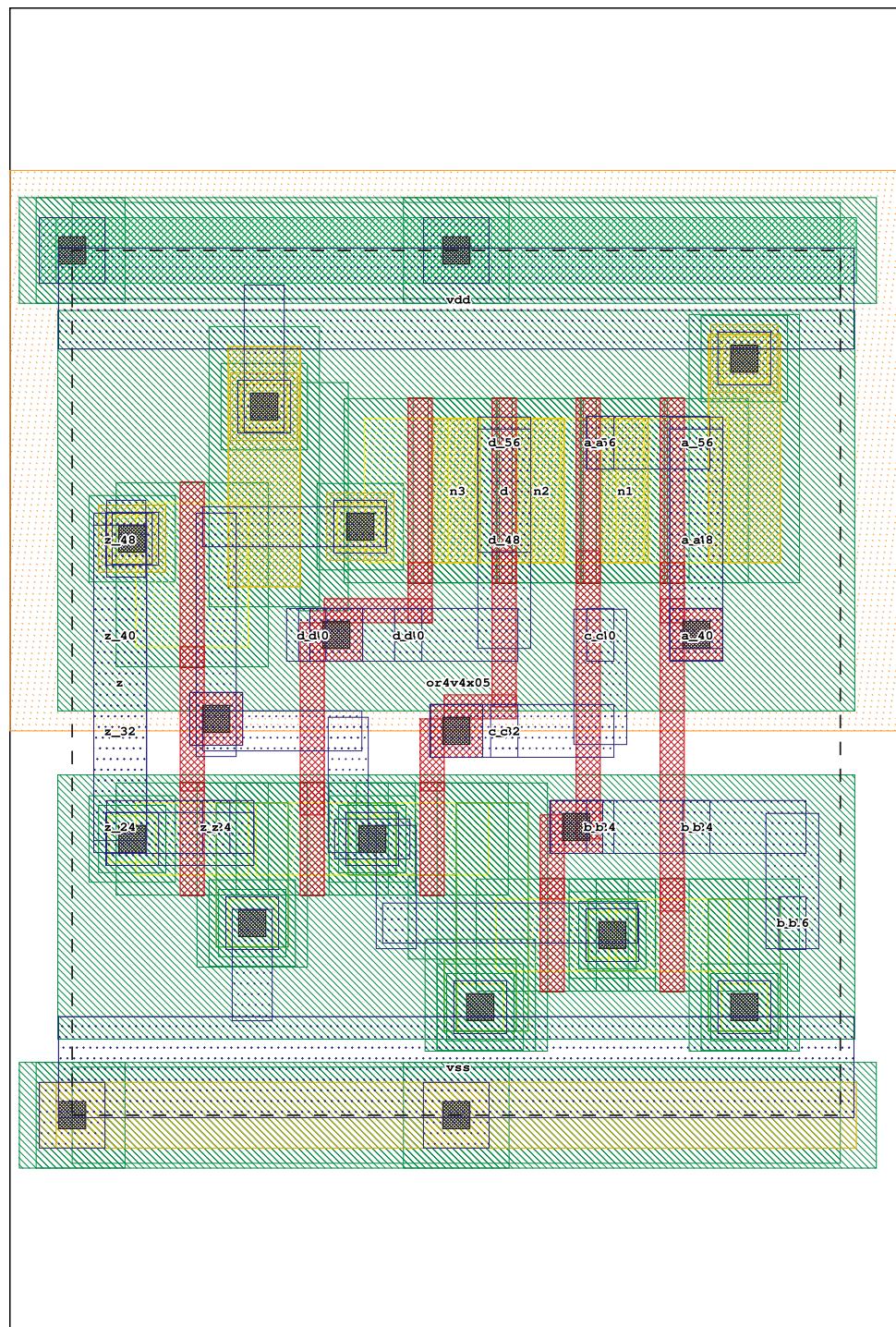
```

ARCHITECTURE behaviour_data_flow OF or4v4x05 IS

```

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on or4v4x05"
  SEVERITY WARNING;
  z <= (((b or c) or a) or d) after 272 ps;
END;

```

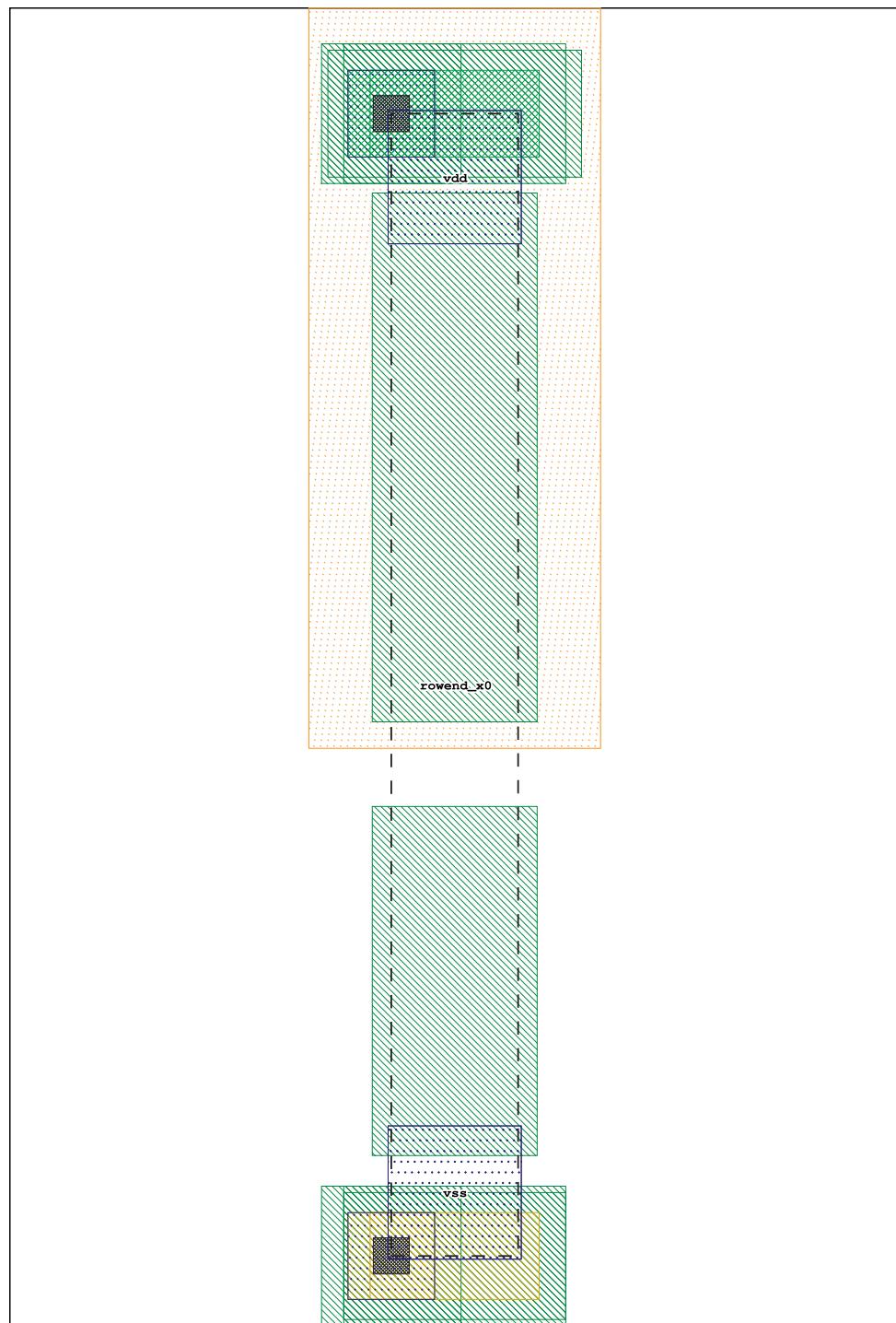


3.103 rowend_x0

```
ENTITY rowend_x0 IS
  GENERIC (
    CONSTANT area          : NATURAL := 576;
    CONSTANT transistors   : NATURAL := 0
  );
  PORT (
    vdd      : in  BIT;
    vss      : in  BIT
  );
END rowend_x0;

ARCHITECTURE behaviour_data_flow OF rowend_x0 IS

BEGIN
  ASSERT (vdd and not (vss))
    REPORT "power supply is missing on rowend_x0"
    SEVERITY WARNING;
END;
```

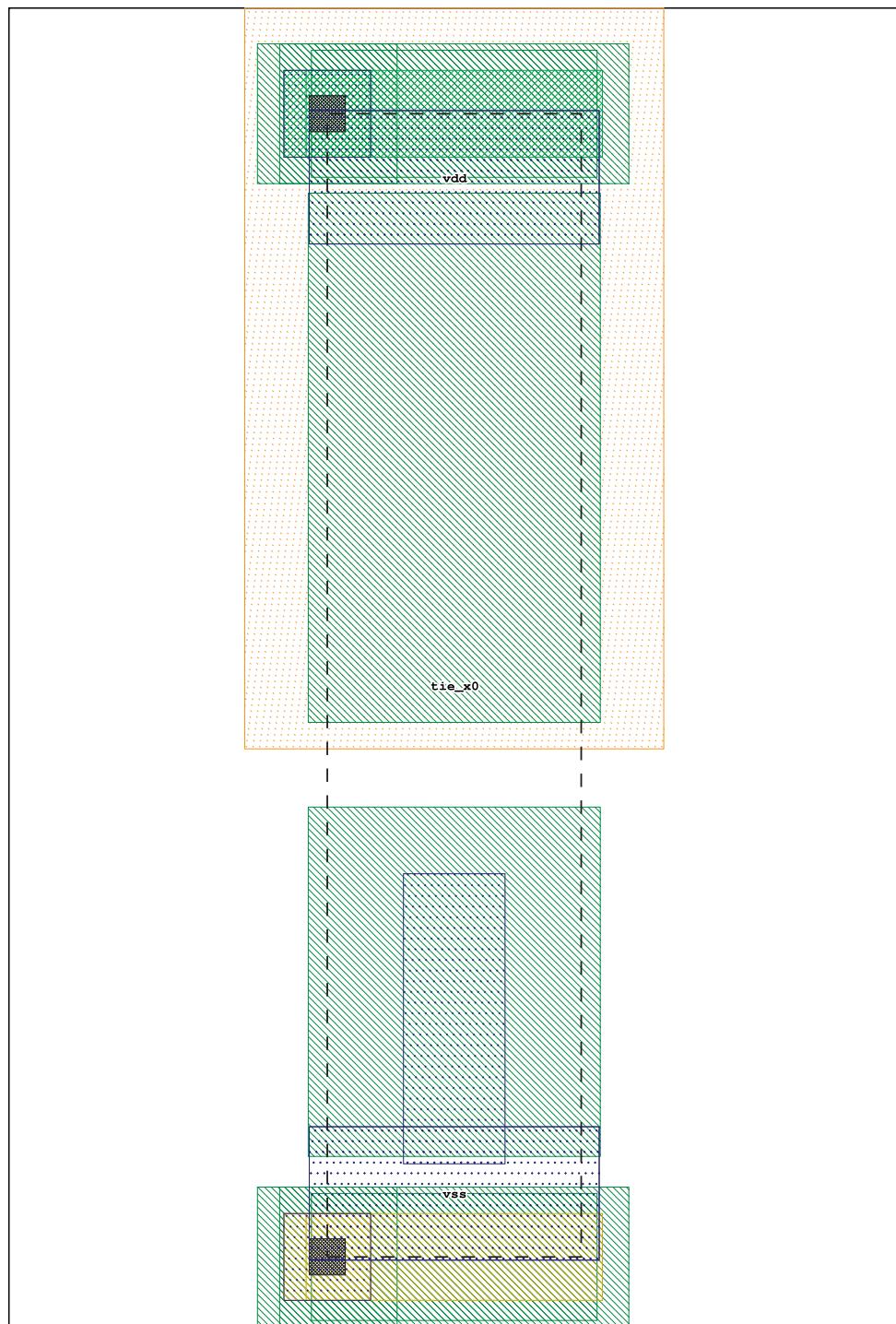


```
3.104 tie_x0

ENTITY tie_x0 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1152;
    CONSTANT transistors   : NATURAL := 0
  );
  PORT (
    vdd      : in  BIT;
    vss      : in  BIT
  );
END tie_x0;

ARCHITECTURE behaviour_data_flow OF tie_x0 IS

BEGIN
  ASSERT (vdd and not (vss))
    REPORT "power supply is missing on tie_x0"
    SEVERITY WARNING;
END;
```

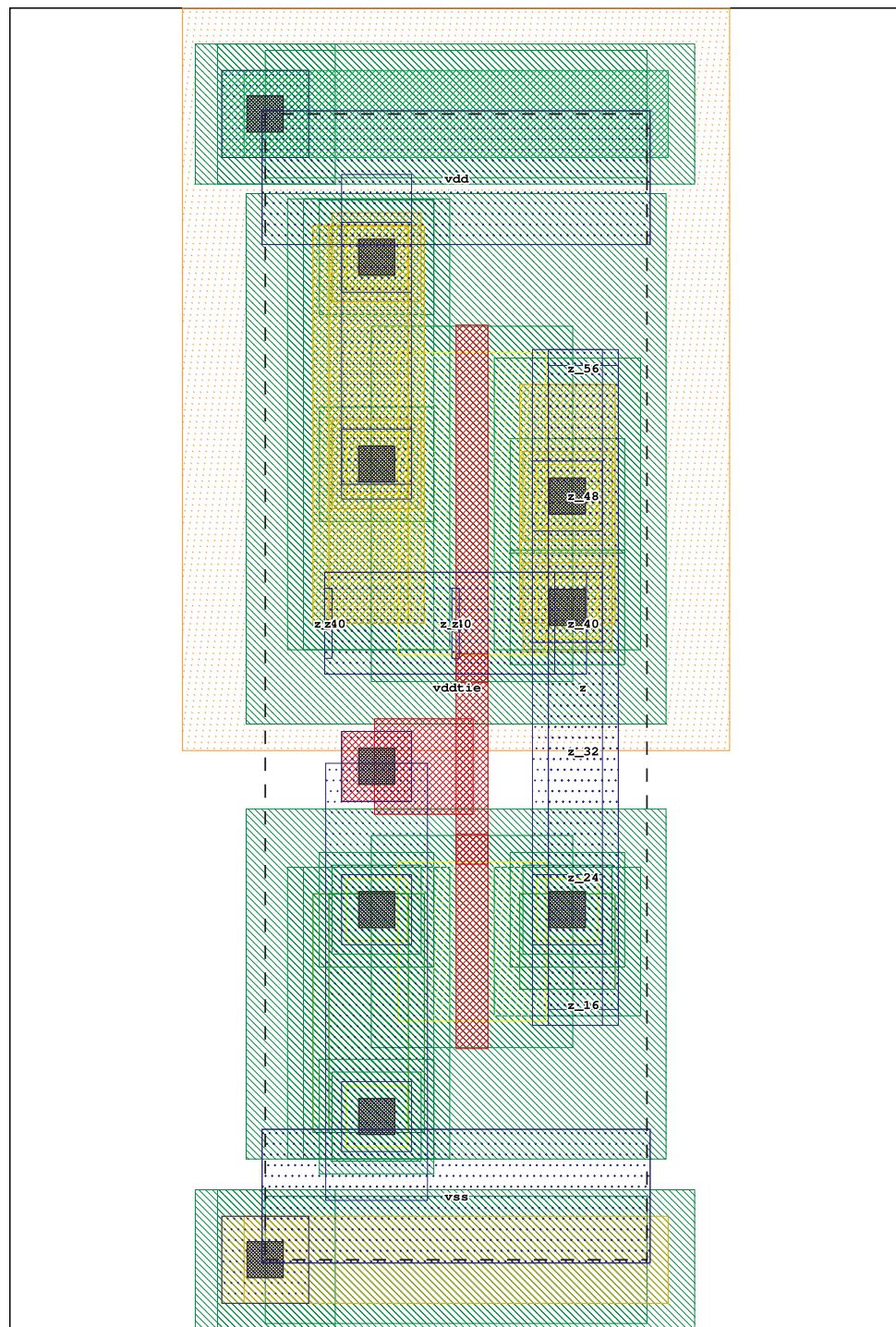


3.105 vddtie

```
ENTITY vddtie IS
  GENERIC (
    CONSTANT area          : NATURAL := 1728;
    CONSTANT transistors   : NATURAL := 2
  );
  PORT (
    z        : out BIT;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END vddtie;

ARCHITECTURE behaviour_data_flow OF vddtie IS

BEGIN
  ASSERT (vdd and not (vss))
  REPORT "power supply is missing on vddtie"
  SEVERITY WARNING;
  z <= '1';
END;
```

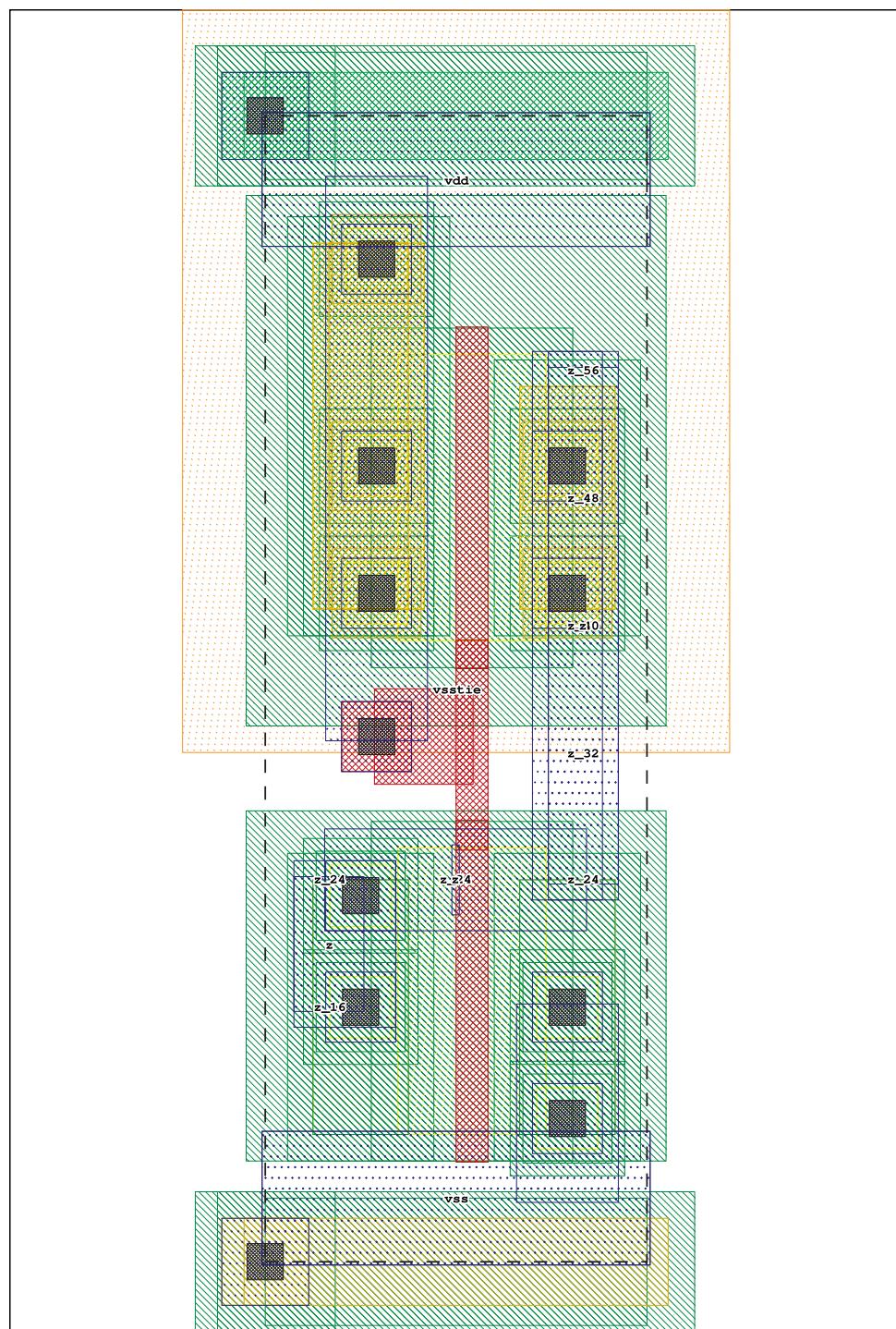


3.106 vsstie

```
ENTITY vsstie IS
  GENERIC (
    CONSTANT area          : NATURAL := 1728;
    CONSTANT transistors   : NATURAL := 2
  );
  PORT (
    z        : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END vsstie;

ARCHITECTURE behaviour_data_flow OF vsstie IS

BEGIN
  ASSERT (vdd and not (vss))
  REPORT "power supply is missing on vsstie"
  SEVERITY WARNING;
  z <= '0';
END;
```



3.107 xaon21v0x05

```

ENTITY xaon21v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5760;
    CONSTANT cin_b         : NATURAL := 5;
    CONSTANT cin_a1        : NATURAL := 5;
    CONSTANT cin_a2        : NATURAL := 5;
    CONSTANT rdown_b_z     : NATURAL := 3720;
    CONSTANT rdown_a1_z    : NATURAL := 4090;
    CONSTANT rdown_a2_z    : NATURAL := 4080;
    CONSTANT rup_b_z       : NATURAL := 4060;
    CONSTANT rup_a1_z      : NATURAL := 5250;
    CONSTANT rup_a2_z      : NATURAL := 5240;
    CONSTANT tplh_a1_z     : NATURAL := 74;
    CONSTANT tplh_a2_z     : NATURAL := 70;
    CONSTANT tphl_b_z      : NATURAL := 29;
    CONSTANT tphl_b_z      : NATURAL := 92;
    CONSTANT tphh_b_z      : NATURAL := 61;
    CONSTANT tphl_a1_z     : NATURAL := 79;
    CONSTANT tphl_a2_z     : NATURAL := 81;
    CONSTANT tp11_a1_z      : NATURAL := 97;
    CONSTANT tp11_a2_z      : NATURAL := 93;
    CONSTANT tp11_b_z       : NATURAL := 88;
    CONSTANT tpjh_a1_z      : NATURAL := 120;
    CONSTANT tpjh_a2_z      : NATURAL := 122;
    CONSTANT transistors   : NATURAL := 11
);
PORT (
    b      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END xaon21v0x05;

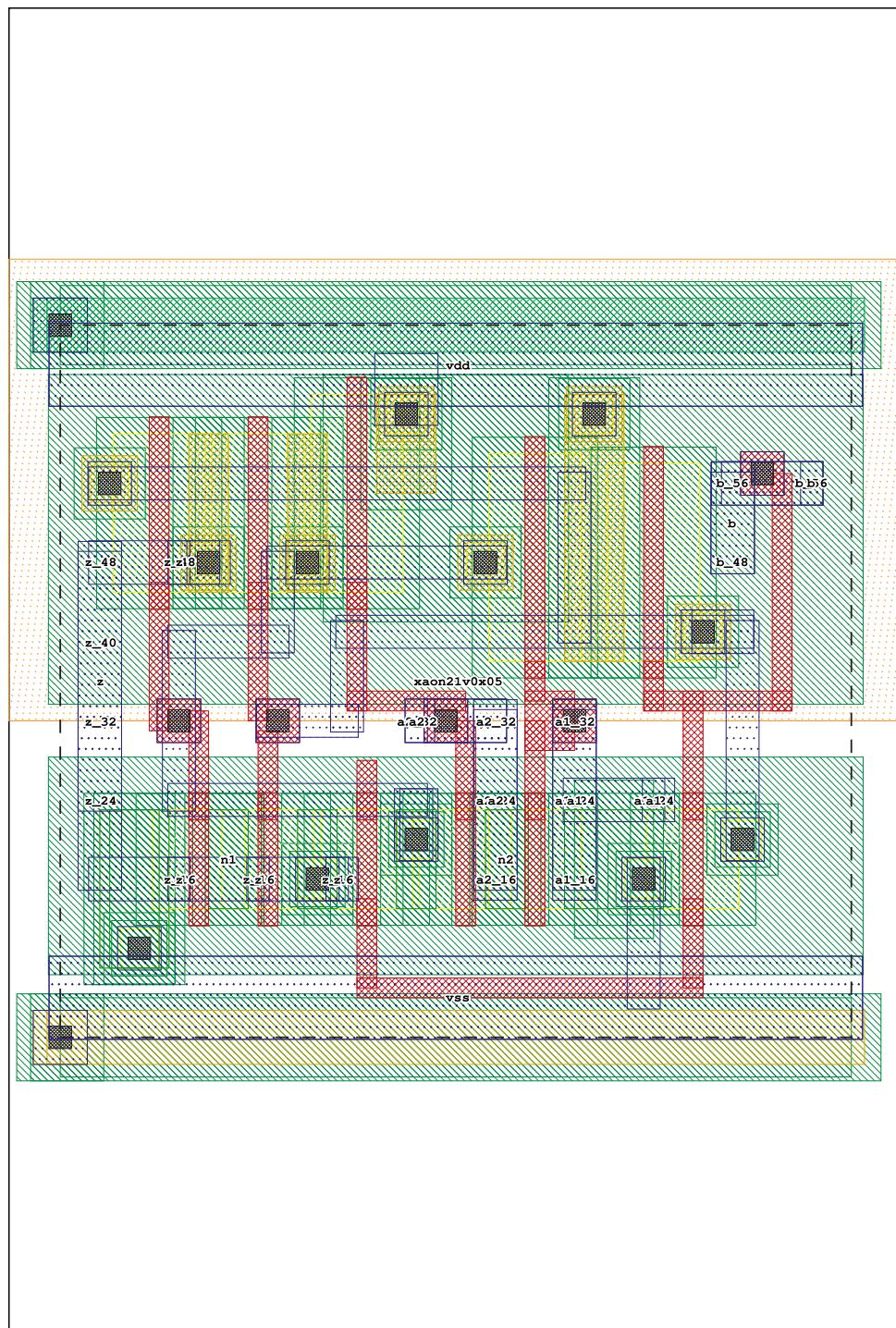
```

ARCHITECTURE behaviour_data_flow OF xaon21v0x05 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on xaon21v0x05"
    SEVERITY WARNING;
    z <= (b xor (a1 and a2)) after 194 ps;
END;

```



3.108 xnr2v8x05

```

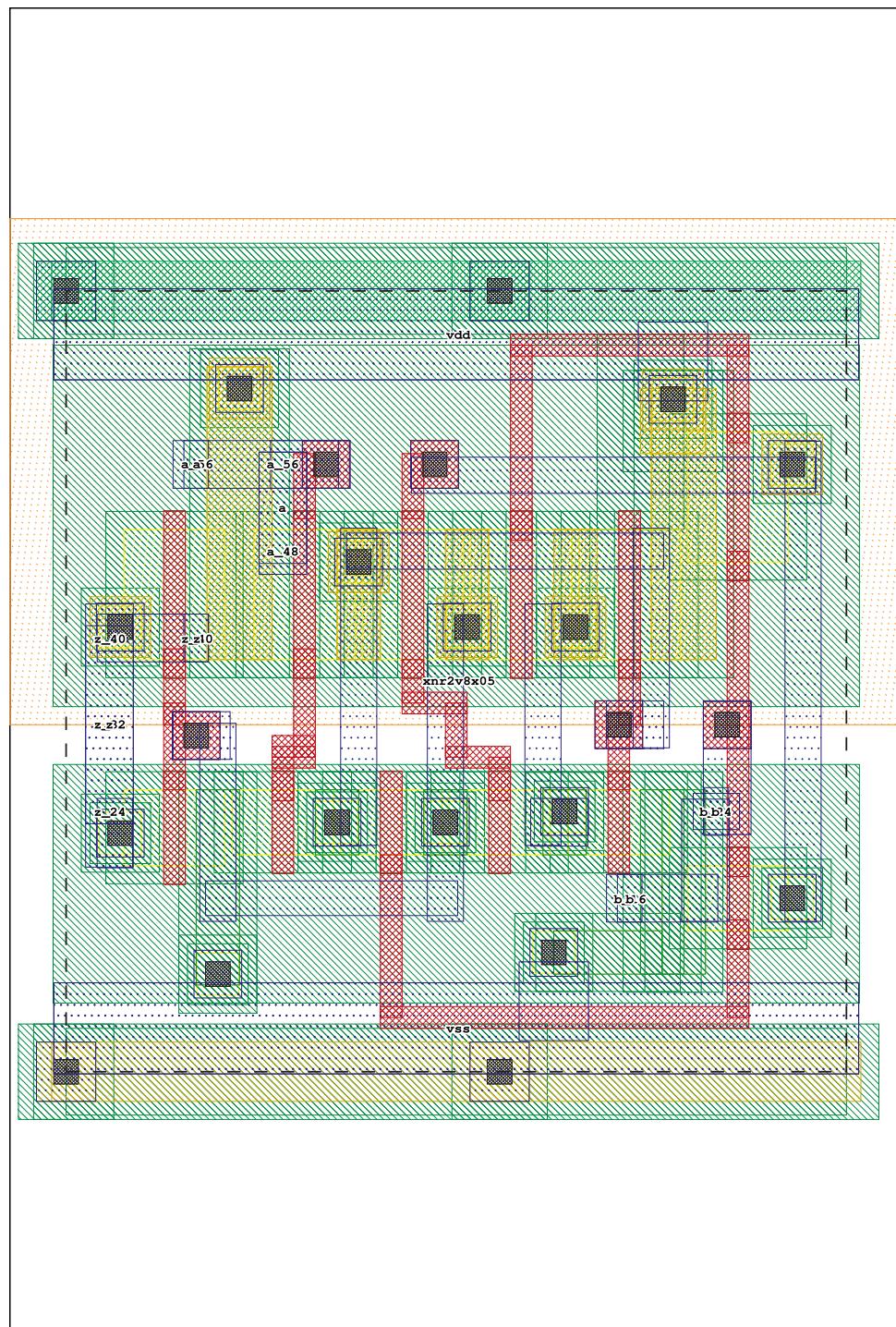
ENTITY xnr2v8x05 IS
GENERIC (
  CONSTANT area          : NATURAL := 5184;
  CONSTANT cin_b         : NATURAL := 6;
  CONSTANT cin_a         : NATURAL := 3;
  CONSTANT rdown_b_z    : NATURAL := 4070;
  CONSTANT rdown_a_z    : NATURAL := 4110;
  CONSTANT rup_b_z      : NATURAL := 5010;
  CONSTANT rup_a_z      : NATURAL := 5020;
  CONSTANT tphl_a_z     : NATURAL := 162;
  CONSTANT tphl_b_z     : NATURAL := 118;
  CONSTANT tplh_b_z     : NATURAL := 120;
  CONSTANT tplh_a_z     : NATURAL := 165;
  CONSTANT tphh_b_z     : NATURAL := 83;
  CONSTANT tpll_b_z     : NATURAL := 108;
  CONSTANT tphh_a_z     : NATURAL := 122;
  CONSTANT tpll_a_z     : NATURAL := 146;
  CONSTANT transistors   : NATURAL := 12
);
PORT (
  b      : in  BIT;
  a      : in  BIT;
  z      : out BIT;
  vdd    : in  BIT;
  vss    : in  BIT
);
END xnr2v8x05;

```

```

ARCHITECTURE behaviour_data_flow OF xnr2v8x05 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on xnr2v8x05"
  SEVERITY WARNING;
  z <= not ((b xor a)) after 242 ps;
END;

```



3.109 xnr3v1x05

```

ENTITY xnr3v1x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 9216;
    CONSTANT cin_a         : NATURAL := 4;
    CONSTANT cin_b         : NATURAL := 6;
    CONSTANT cin_c         : NATURAL := 5;
    CONSTANT rdown_a_z     : NATURAL := 4780;
    CONSTANT rdown_b_z     : NATURAL := 4770;
    CONSTANT rdown_c_z     : NATURAL := 4510;
    CONSTANT rup_a_z       : NATURAL := 6190;
    CONSTANT rup_b_z       : NATURAL := 6190;
    CONSTANT rup_c_z       : NATURAL := 5980;
    CONSTANT tphl_a_z      : NATURAL := 169;
    CONSTANT tphh_a_z      : NATURAL := 171;
    CONSTANT tphl_b_z      : NATURAL := 174;
    CONSTANT tphh_b_z      : NATURAL := 176;
    CONSTANT tphl_c_z      : NATURAL := 37;
    CONSTANT tphh_c_z      : NATURAL := 68;
    CONSTANT tplh_c_z      : NATURAL := 91;
    CONSTANT tpll_c_z      : NATURAL := 98;
    CONSTANT tplh_b_z      : NATURAL := 145;
    CONSTANT tpll_b_z      : NATURAL := 143;
    CONSTANT tpll_a_z      : NATURAL := 180;
    CONSTANT tpll_a_z      : NATURAL := 179;
    CONSTANT transistors   : NATURAL := 18
);
PORT (
    a      : in  BIT;
    b      : in  BIT;
    c      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END xnr3v1x05;

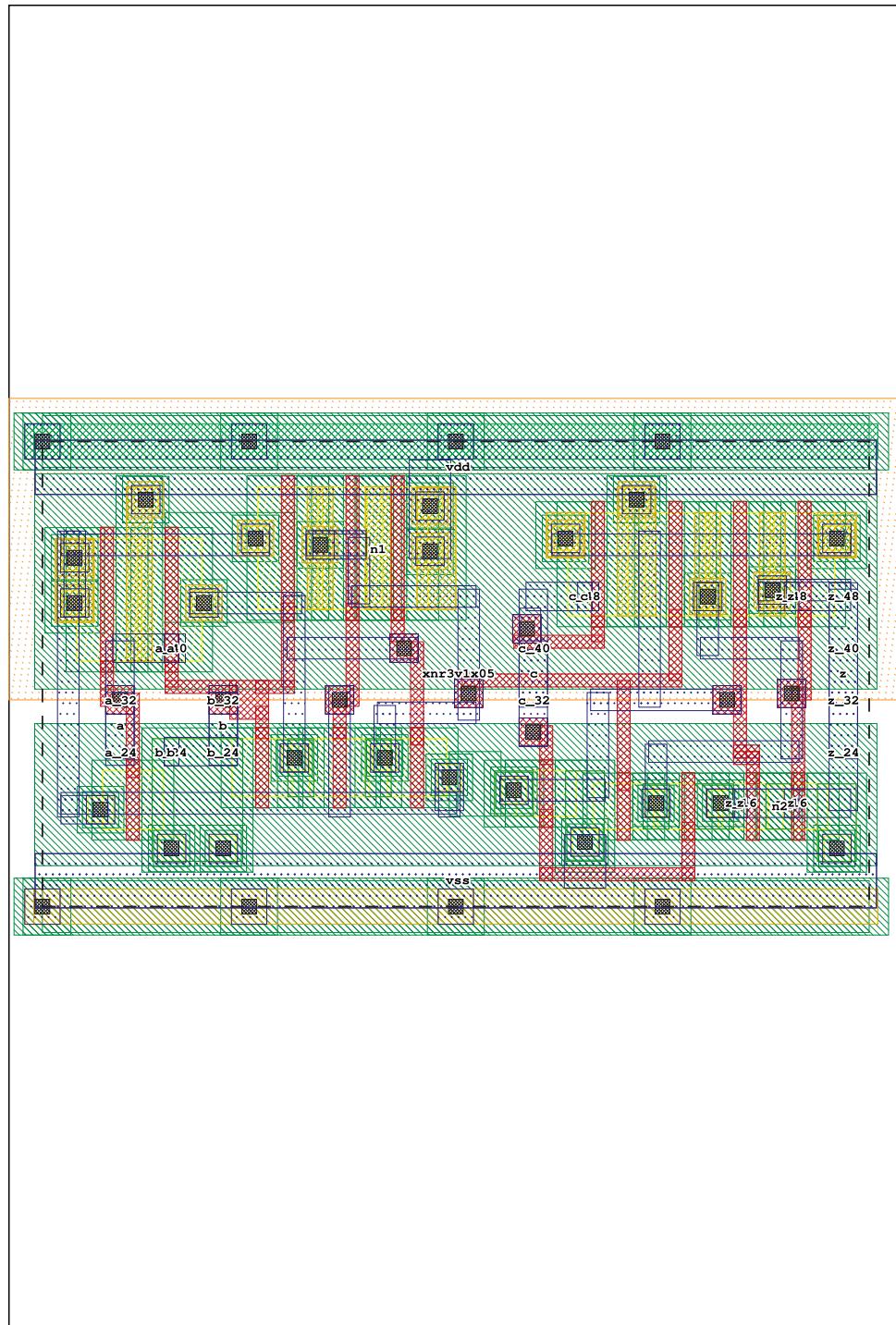
```

ARCHITECTURE behaviour_data_flow OF xnr3v1x05 IS

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on xnr3v1x05"
    SEVERITY WARNING;
    z <= not ((a xor b) xor c) after 271 ps;
END;

```



3.110 xoon21v0x05

```

ENTITY xoon21v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5760;
    CONSTANT cin_b         : NATURAL := 5;
    CONSTANT cin_a1        : NATURAL := 4;
    CONSTANT cin_a2        : NATURAL := 5;
    CONSTANT rdown_b_z     : NATURAL := 3840;
    CONSTANT rdown_a1_z    : NATURAL := 4720;
    CONSTANT rdown_a2_z    : NATURAL := 4690;
    CONSTANT rup_b_z       : NATURAL := 6870;
    CONSTANT rup_a1_z      : NATURAL := 6660;
    CONSTANT rup_a2_z      : NATURAL := 6660;
    CONSTANT tplh_a1_z     : NATURAL := 98;
    CONSTANT tplh_a2_z     : NATURAL := 90;
    CONSTANT tphl_b_z      : NATURAL := 39;
    CONSTANT tphl_b_z      : NATURAL := 96;
    CONSTANT tphh_b_z      : NATURAL := 72;
    CONSTANT tphl_a1_z     : NATURAL := 83;
    CONSTANT tphl_a2_z     : NATURAL := 74;
    CONSTANT tp11_a1_z     : NATURAL := 127;
    CONSTANT tp11_a2_z     : NATURAL := 119;
    CONSTANT tp11_b_z      : NATURAL := 108;
    CONSTANT tpjh_a1_z     : NATURAL := 118;
    CONSTANT tpjh_a2_z     : NATURAL := 108;
    CONSTANT transistors   : NATURAL := 11
);
PORT (
    b      : in  BIT;
    a1     : in  BIT;
    a2     : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END xoon21v0x05;

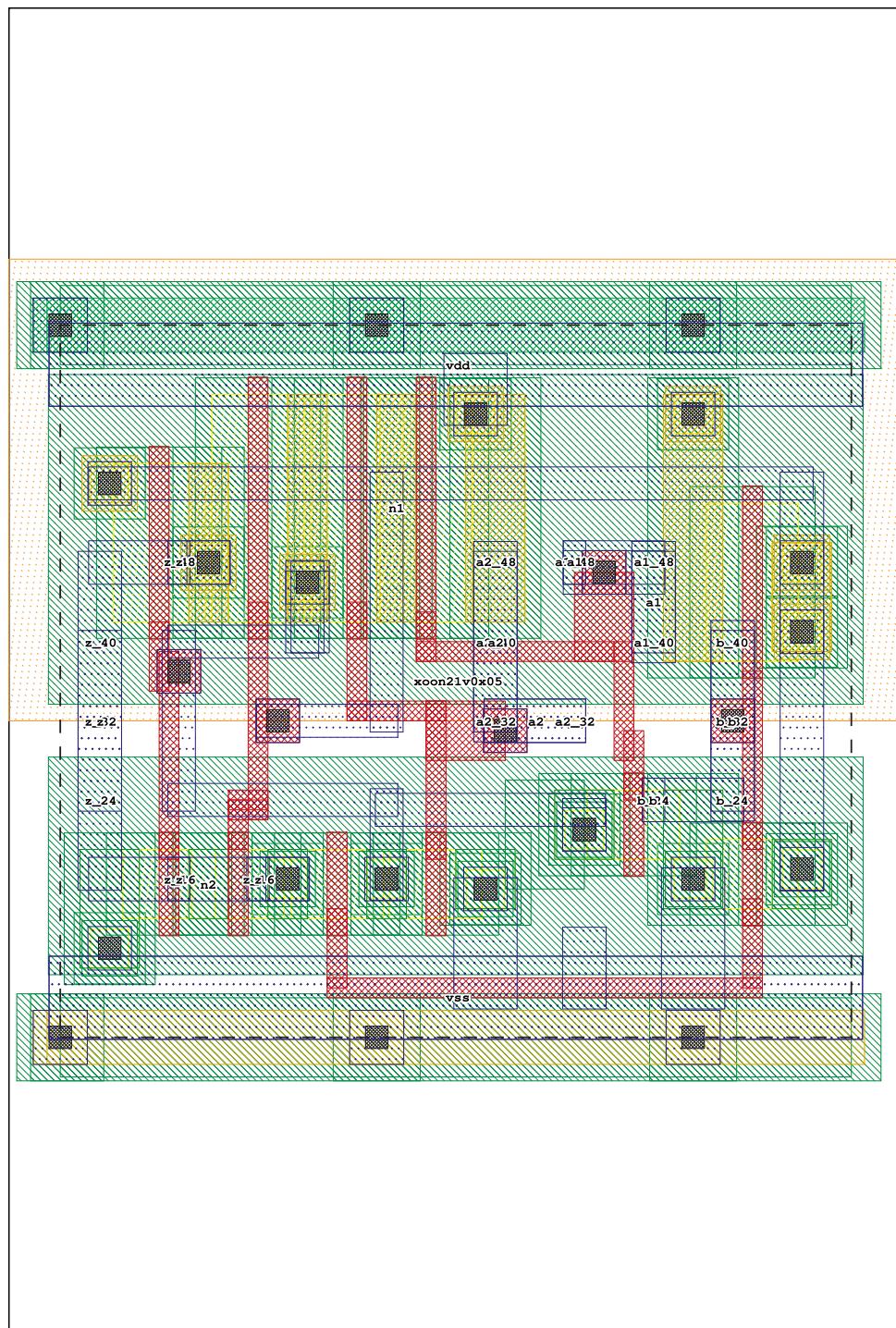
```

```
ARCHITECTURE behaviour_data_flow OF xoon21v0x05 IS
```

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on xoon21v0x05"
    SEVERITY WARNING;
    z <= (b xor (a1 or a2)) after 234 ps;
END;

```



3.111 xor2v0x05

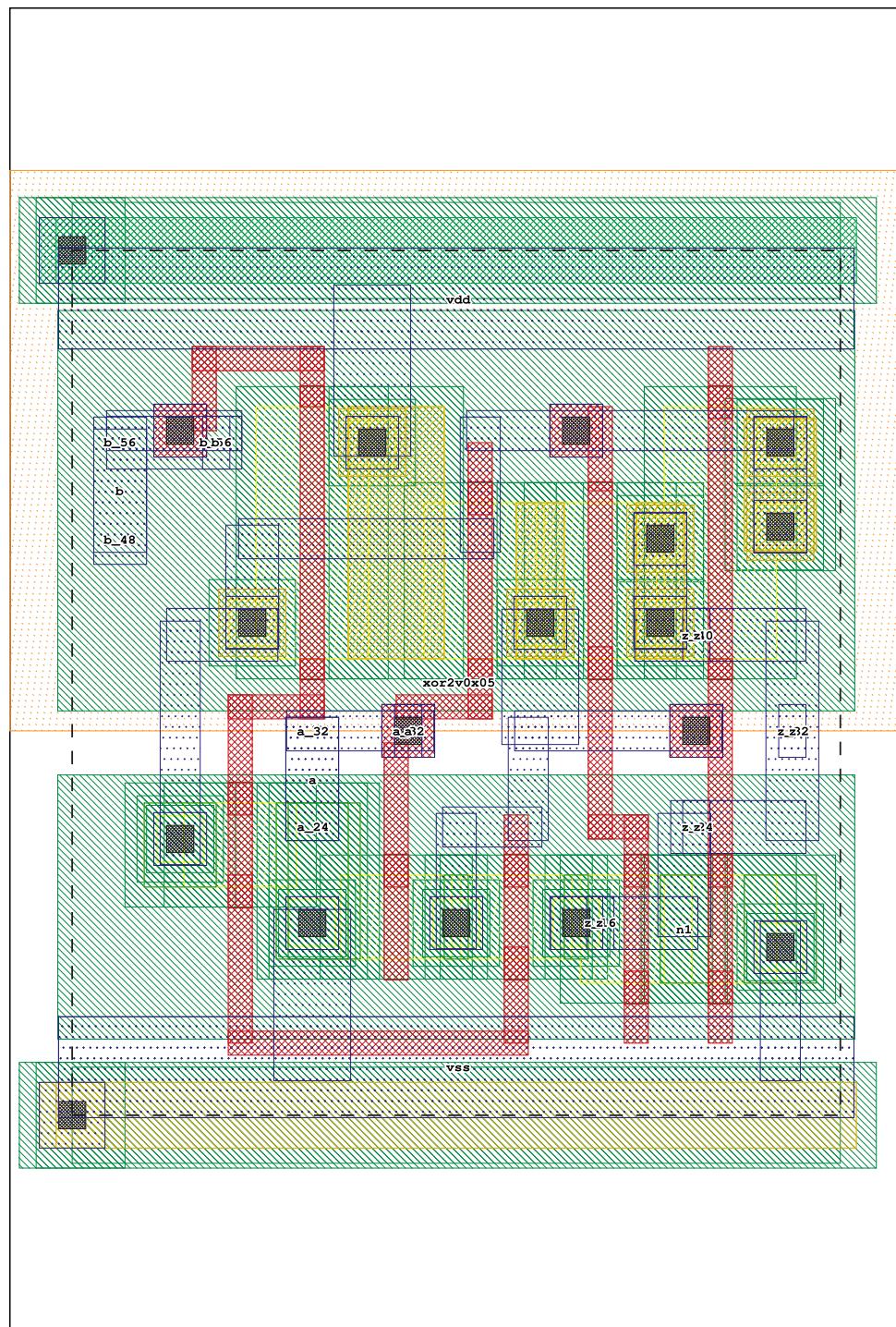
```

ENTITY xor2v0x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 4608;
    CONSTANT cin_b          : NATURAL := 5;
    CONSTANT cin_a          : NATURAL := 3;
    CONSTANT rdown_b_z      : NATURAL := 3890;
    CONSTANT rdown_a_z      : NATURAL := 4140;
    CONSTANT rup_b_z        : NATURAL := 5490;
    CONSTANT rup_a_z        : NATURAL := 5740;
    CONSTANT tplh_a_z       : NATURAL := 74;
    CONSTANT tphl_b_z       : NATURAL := 39;
    CONSTANT tphl_b_z       : NATURAL := 79;
    CONSTANT tphh_b_z       : NATURAL := 72;
    CONSTANT tphl_a_z       : NATURAL := 63;
    CONSTANT tp11_a_z       : NATURAL := 97;
    CONSTANT tp11_b_z       : NATURAL := 80;
    CONSTANT tphh_a_z       : NATURAL := 86;
    CONSTANT transistors    : NATURAL := 9
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END xor2v0x05;

ARCHITECTURE behaviour_data_flow OF xor2v0x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on xor2v0x05"
    SEVERITY WARNING;
    z <= (b xor a) after 194 ps;
END;

```



3.112 xor2v1x05

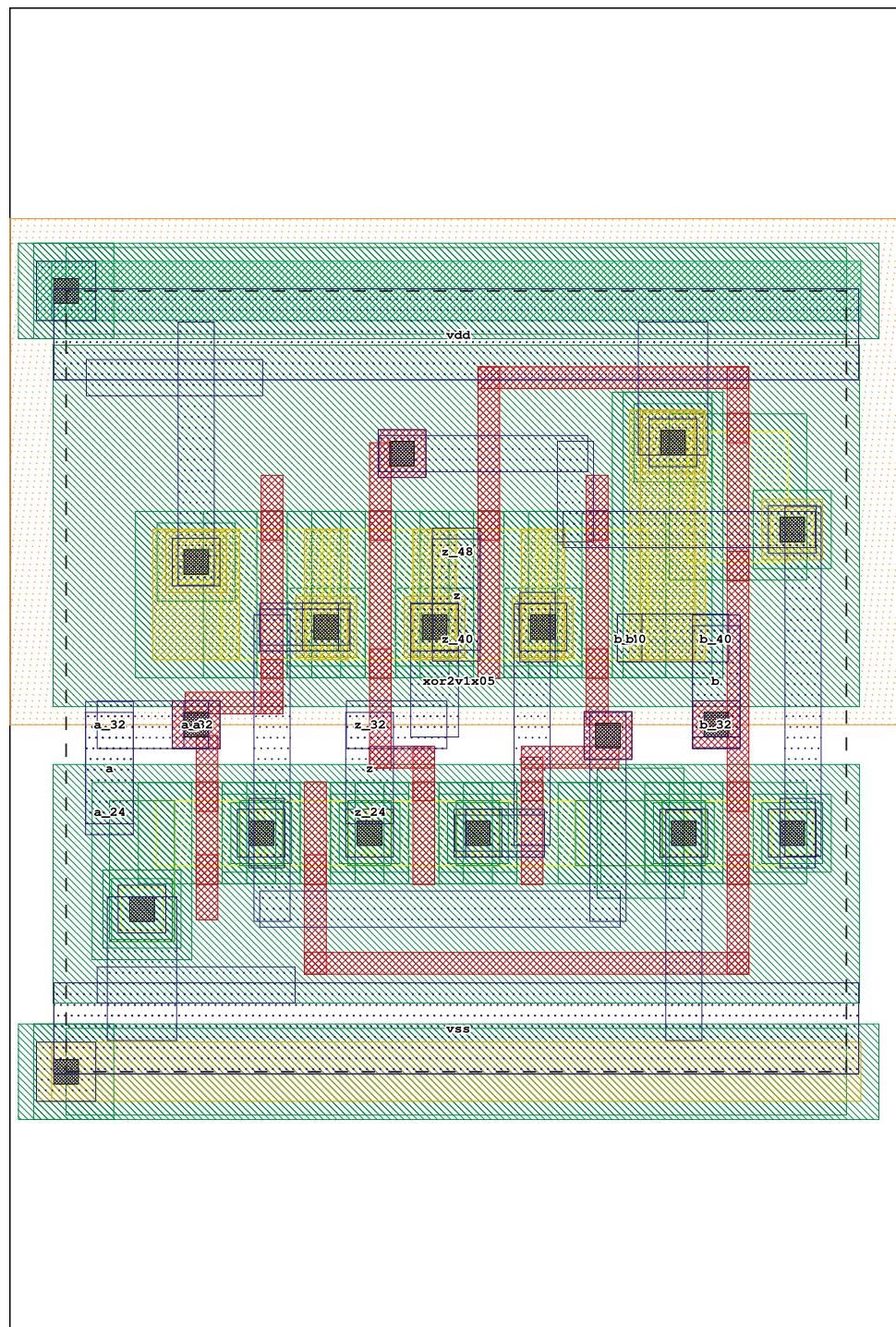
```

ENTITY xor2v1x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_b          : NATURAL := 5;
    CONSTANT cin_a          : NATURAL := 3;
    CONSTANT rdown_b_z      : NATURAL := 4750;
    CONSTANT rdown_a_z      : NATURAL := 5090;
    CONSTANT rup_b_z        : NATURAL := 6230;
    CONSTANT rup_a_z        : NATURAL := 6570;
    CONSTANT tplh_a_z       : NATURAL := 84;
    CONSTANT tphl_b_z       : NATURAL := 39;
    CONSTANT tphl_b_z       : NATURAL := 53;
    CONSTANT tphh_b_z       : NATURAL := 57;
    CONSTANT tphl_a_z       : NATURAL := 71;
    CONSTANT tp11_a_z       : NATURAL := 114;
    CONSTANT tp11_b_z       : NATURAL := 70;
    CONSTANT tphh_a_z       : NATURAL := 102;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END xor2v1x05;

ARCHITECTURE behaviour_data_flow OF xor2v1x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on xor2v1x05"
    SEVERITY WARNING;
    z <= (b xor a) after 215 ps;
END;

```



3.113 xor2v2x05

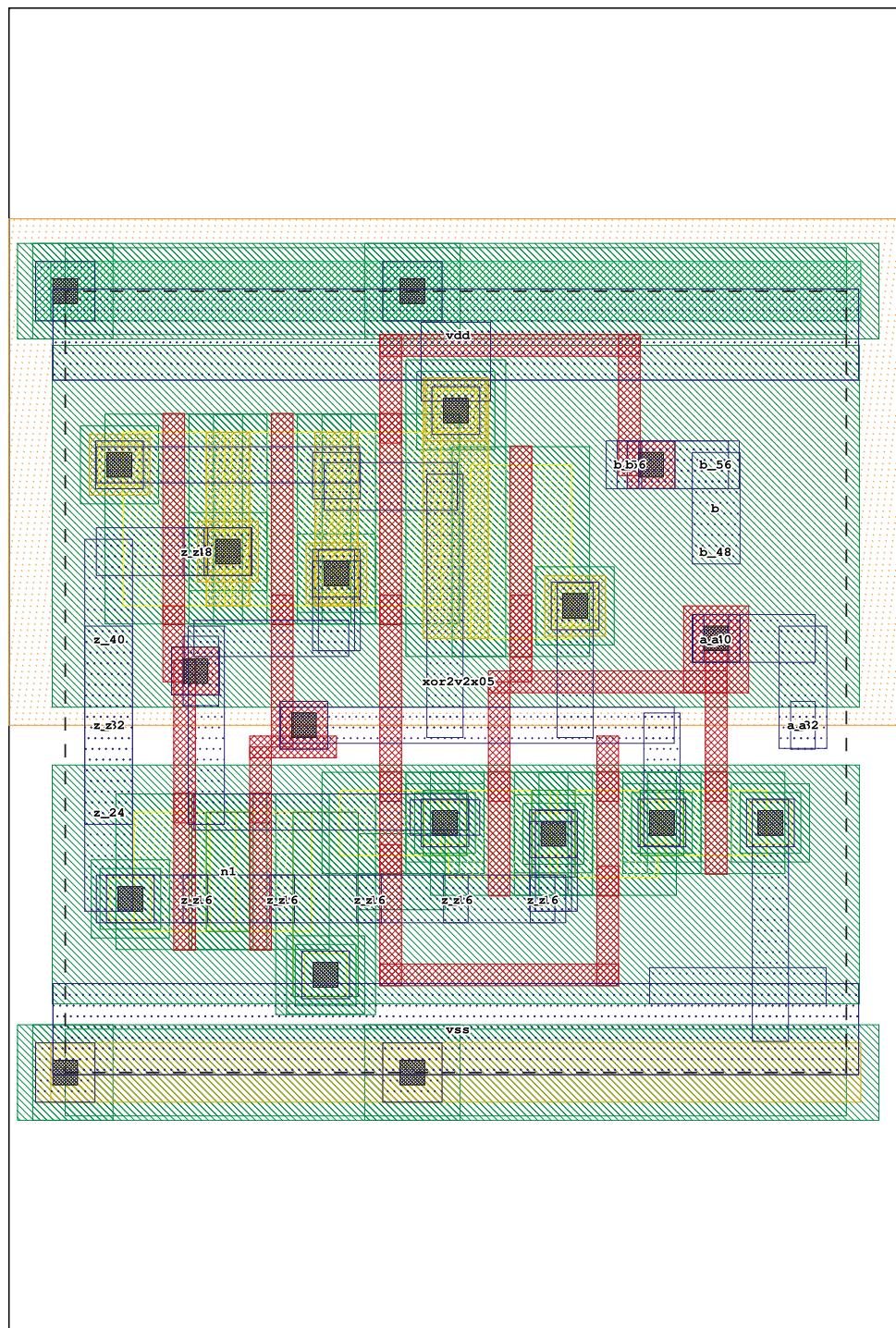
```

ENTITY xor2v2x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_b          : NATURAL := 4;
    CONSTANT cin_a          : NATURAL := 4;
    CONSTANT rdown_b_z      : NATURAL := 2980;
    CONSTANT rdown_a_z      : NATURAL := 2990;
    CONSTANT rup_b_z        : NATURAL := 4690;
    CONSTANT rup_a_z        : NATURAL := 4650;
    CONSTANT tplh_a_z       : NATURAL := 82;
    CONSTANT tphl_b_z       : NATURAL := 43;
    CONSTANT tphl_b_z       : NATURAL := 74;
    CONSTANT tphh_b_z       : NATURAL := 78;
    CONSTANT tphl_a_z       : NATURAL := 49;
    CONSTANT tpll_a_z       : NATURAL := 96;
    CONSTANT tpll_b_z       : NATURAL := 91;
    CONSTANT tphh_a_z       : NATURAL := 84;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END xor2v2x05;

ARCHITECTURE behaviour_data_flow OF xor2v2x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on xor2v2x05"
    SEVERITY WARNING;
    z <= (b xor a) after 170 ps;
END;

```



3.114 xor2v8x05

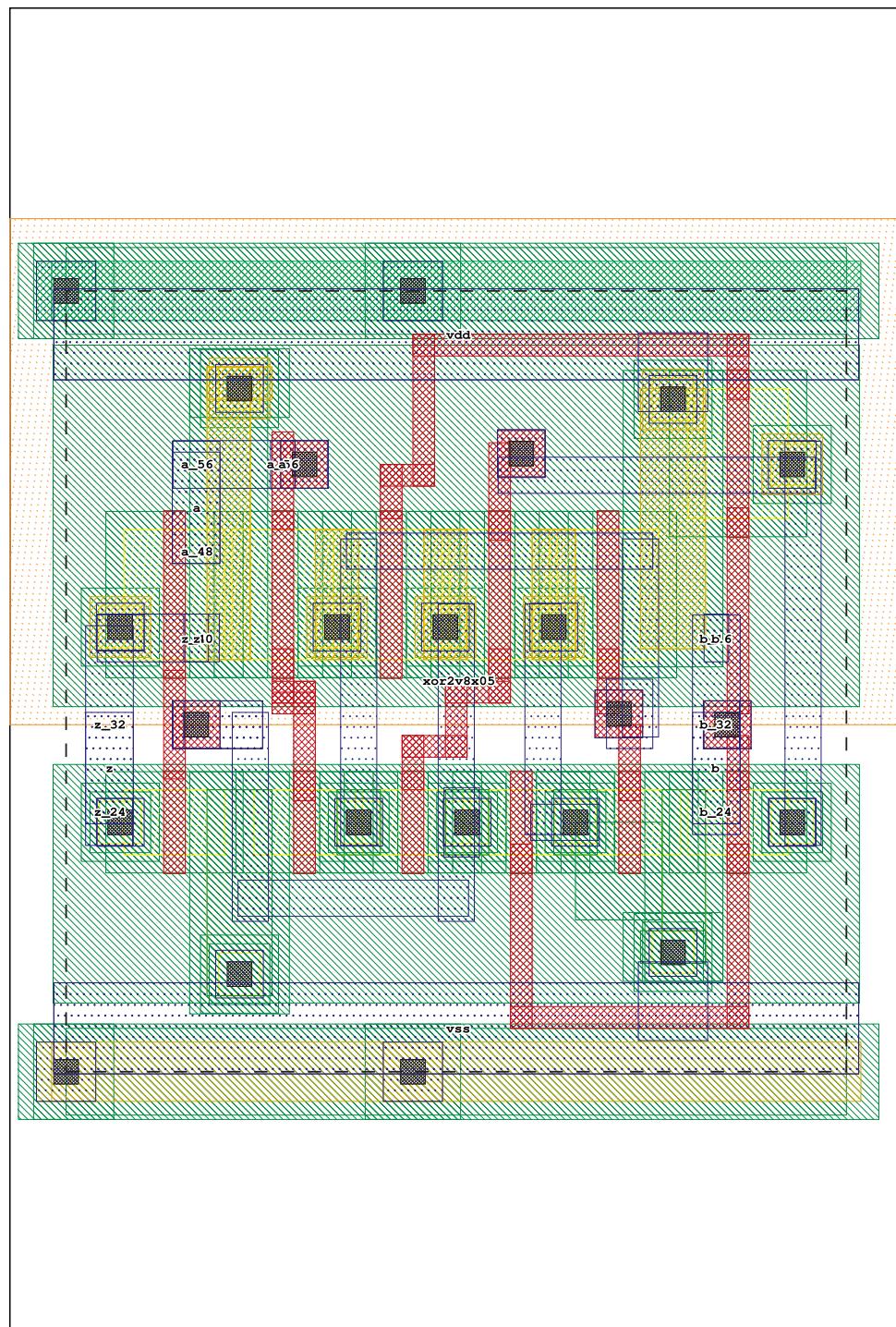
```

ENTITY xor2v8x05 IS
GENERIC (
    CONSTANT area          : NATURAL := 5184;
    CONSTANT cin_b          : NATURAL := 6;
    CONSTANT cin_a          : NATURAL := 3;
    CONSTANT rdown_b_z      : NATURAL := 4060;
    CONSTANT rdown_a_z      : NATURAL := 4100;
    CONSTANT rup_b_z        : NATURAL := 5010;
    CONSTANT rup_a_z        : NATURAL := 5010;
    CONSTANT tplh_a_z       : NATURAL := 161;
    CONSTANT tphl_b_z       : NATURAL := 116;
    CONSTANT tphl_b_z       : NATURAL := 117;
    CONSTANT tphh_b_z       : NATURAL := 85;
    CONSTANT tphl_a_z       : NATURAL := 161;
    CONSTANT tp11_a_z       : NATURAL := 144;
    CONSTANT tp11_b_z       : NATURAL := 104;
    CONSTANT tphh_a_z       : NATURAL := 122;
    CONSTANT transistors    : NATURAL := 12
);
PORT (
    b      : in  BIT;
    a      : in  BIT;
    z      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END xor2v8x05;

ARCHITECTURE behaviour_data_flow OF xor2v8x05 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on xor2v8x05"
    SEVERITY WARNING;
    z <= (b xor a) after 240 ps;
END;

```



3.115 xor3v1x05

```

ENTITY xor3v1x05 IS
GENERIC (
  CONSTANT area          : NATURAL := 8640;
  CONSTANT cin_a          : NATURAL := 4;
  CONSTANT cin_b          : NATURAL := 5;
  CONSTANT cin_c          : NATURAL := 5;
  CONSTANT rdown_a_z      : NATURAL := 4780;
  CONSTANT rdown_b_z      : NATURAL := 4780;
  CONSTANT rdown_c_z      : NATURAL := 4510;
  CONSTANT rup_a_z         : NATURAL := 6180;
  CONSTANT rup_b_z         : NATURAL := 6180;
  CONSTANT rup_c_z         : NATURAL := 5980;
  CONSTANT tphl_a_z        : NATURAL := 166;
  CONSTANT tphh_a_z        : NATURAL := 167;
  CONSTANT tphl_b_z        : NATURAL := 135;
  CONSTANT tphh_b_z        : NATURAL := 136;
  CONSTANT tphl_c_z        : NATURAL := 36;
  CONSTANT tphh_c_z        : NATURAL := 67;
  CONSTANT tplh_c_z        : NATURAL := 91;
  CONSTANT tpll_c_z        : NATURAL := 97;
  CONSTANT tplh_b_z        : NATURAL := 182;
  CONSTANT tpll_b_z        : NATURAL := 181;
  CONSTANT tpll_a_z        : NATURAL := 170;
  CONSTANT tpll_a_z        : NATURAL := 169;
  CONSTANT transistors     : NATURAL := 18
);
PORT (
  a      : in  BIT;
  b      : in  BIT;
  c      : in  BIT;
  z      : out BIT;
  vdd    : in  BIT;
  vss    : in  BIT
);
END xor3v1x05;

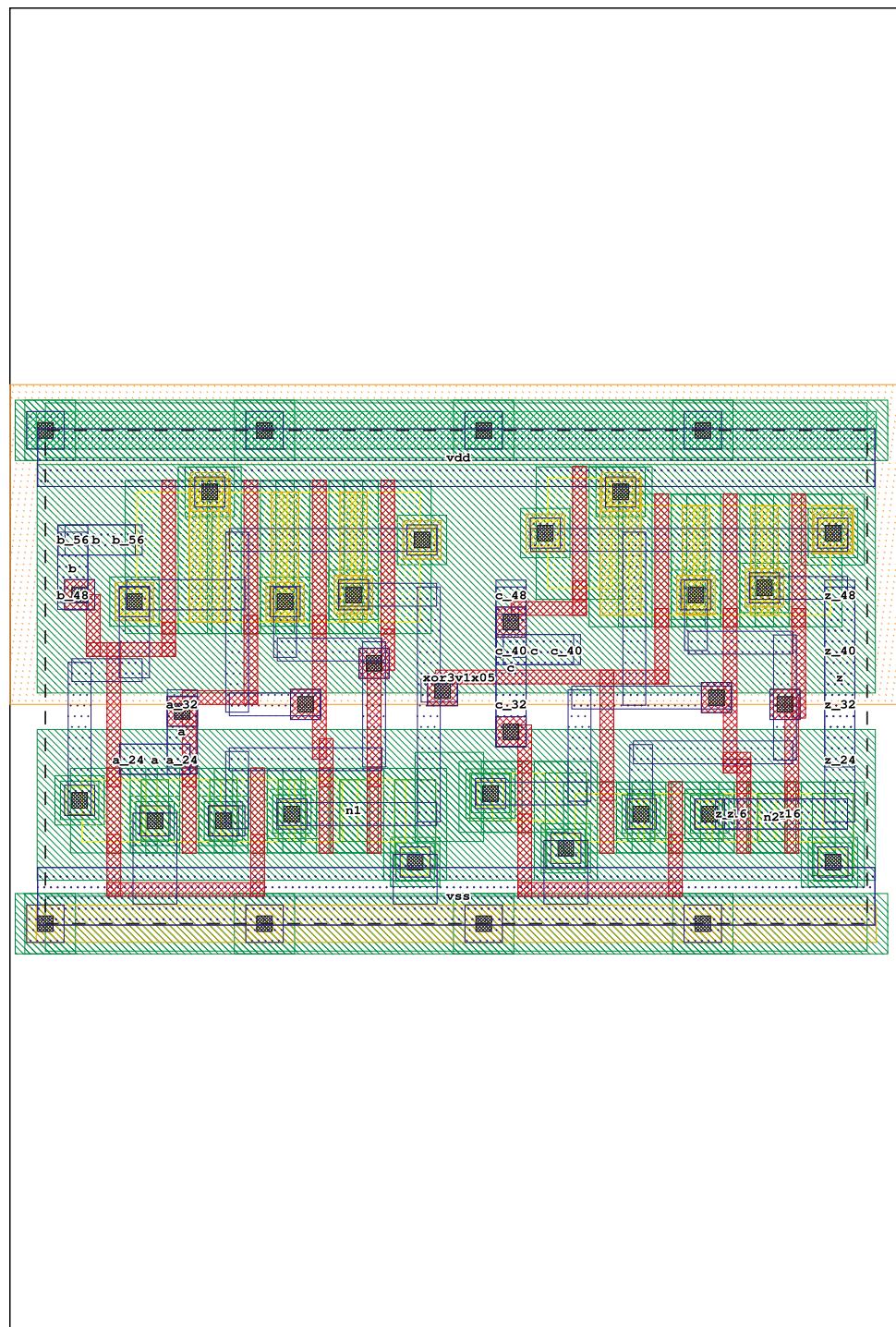
```

ARCHITECTURE behaviour_data_flow OF xor3v1x05 IS

```

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on xor3v1x05"
  SEVERITY WARNING;
  z <= ((a xor b) xor c) after 268 ps;
END;

```



4 RDS File for Skywater 130

This is the RDS file for Skywater 130.

```
# 20230301
#
# For SkyWater130
#
#
#
# globals define
#
define physical_grid      0.005
define lambda              0.075

table cif_layer
#
# rds_name      cif_name
#
rds_nwell      nwell
# rds_pwell      pwel
rds_activ      diff
rds_ntie       tap
rds_ptie       tap
rds_ndif       nsdm
rds_pdif       psdm
rds_nimp       nsdm
rds_pimp       psdm
rds_poly       poly
rds_alu1       li1
rds_alu2       met1
rds_alu3       met2
rds_alu4       met3
rds_alu5       met4
rds_alu6       met5
rds_cont       licon1
rds_via1       mcon
rds_via2       via
rds_via3       via2
rds_via4       via3
rds_via5       via4
rds_cpas       pad
end

table gds_layer
#
```

```
# rds_name      gds_number gds_datatype gds_pin_layer gds_pin_datatype
# This version is incompatible with oriinal Alliance for 2nd number
#
rds_nwell    64      20
rds_pwell    64      44
rds_activ    65      20
rds_ptie     65      44
rds_ntie     65      44
rds_pdif     94      20
rds_ndif     93      44
rds_pimp     94      20
rds_nimp     93      44
rds_poly     66      20
rds_alu1     67      20      67      16
rds_alu2     68      20      68      16
rds_alu3     69      20      69      16
rds_alu4     70      20      70      16
rds_alu5     71      20      71      16
rds_alu6     72      20      72      16
rds_cont     66      44
rds_via1     67      44
rds_via2     68      44
rds_via3     69      44
rds_via4     70      44
rds_via5     71      44
rds_cpas     76      20
end

table lynx_resistor
#
# rds_name square_resistor(ohm/square) # typical values
#
rds_poly     48
rds_alu1     13
rds_alu2     0.125
rds_alu3     0.125
rds_alu4     0.047
rds_alu5     0.047
rds_alu6     0.029
rds_cont     15
rds_via1     152
rds_via2     4.5
rds_via3     3.4
rds_via4     3.4
rds_via5     0.38
end

table lynx_capa
#
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
```

```
# _____
# rds_poly 106.2e-6 55.3e-6 # Ca max POLY_NWELL 2Cf0 max POLY_NWELL
# rds_alu1 37.9e-6 40.7e-6 # Ca max M1_NWELL 2Cf0 max M1_NWELL
# rds_alu2 25.8e-6 40.6e-6 # Ca max M2_NWELL 2Cf0 max M2_NWELL
# rds_alu3 16.9e-6 37.8e-6 # Ca max M3_NWELL 2Cf0 max M3_NWELL
# rds_alu4 12.4e-6 41.0e-6 # Ca max M4_NWELL 2Cf0 max M4_NWELL
# rds_alu5 8.4e-6 36.7e-6 # hyp
# rds_alu6 6.3e-6 38.9e-6
end

table lynx_capa_poly
# _____
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
# _____
# end

table lynx_capa_poly2
# _____
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
# _____
# end

table lynx_capa_alu1
# _____
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
# _____
# end

table lynx_capa_alu2
# _____
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
# _____
# end

table lynx_capa_alu3
# _____
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
# _____
# end

table lynx_capa_alu4
# _____
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
# _____
# end

table lynx_capa_alu5
# _____
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
# _____
```

4 RDS FILE FOR SKYWATER 130

```

end
table mbk_to_rds_segment
#
# mbk_name      rds_name1 dlr  dwr  offset mode      rds_name2 dlr  dwr  offset mode
#
# nwell        rds_nwell   vw    0.390   0.2   -0.1 all \
#                  rds_pimp    vw    0.09   -0.80    .275 all \
#                  rds_nimp    vw    0.09   -1.65    2.75 all
#                  rds_nimp    vw    0.225   0.170   .0   all
#
# pwell        rds_pwell   vw    0.390   0.0   .0   all
#                  rds_nimp    vw    0.225   0.170   .0   all
#
# ndif         rds_activ   vw    0.00    0.0   .0   all \
#                  rds_nimp    vw    0.125   0.24   .0   all \
#                  rds_ndif    vw    0.00    0.0   .0   all
#
# pdif         rds_activ   vw    0.00    0.0   .0   all \
#                  rds_pimp    vw    0.125   0.24   .0   all \
#                  rds_pdif    vw    0.00    0.0   .0   all
#
# ntie         rds_ntie    vw    0.10    0.11  .0   all \
#                  rds_nimp    vw    0.225   0.36   .0   all
#                  rds_activ   vw    0.15    0.0   .0   all
#
# ptie         rds_ptie    vw    0.10    0.11  .0   all \
#                  rds_pimp    vw    0.225   0.36   .0   all
#                  rds_activ   vw    0.15    0.0   .0   all
#                  rds_pwell   vw    0.460   0.510  .0   all
#
# ntrans        rds_poly    vw    0.13    0.00  .0   all \
#                  rds_nimp    vw    0.125   0.80   .0   all \
#                  rds_activ   vw    0.0     0.55   .0   drc \
#                  rds_ndif    lcw   0.0     0.275  .0   ext \
#                  rds_ndif    rcw   0.0     0.275  .0   ext
#
# ptrans        rds_poly    vw    0.13    0.00  .0   all \
#                  rds_pimp    vw    0.125   0.80   .0   all \
#                  rds_activ   vw    0.0     0.55   .0   drc \
#                  rds_pdif    lcw   0.0     0.275  .0   ext \
#                  rds_pdif    rcw   0.0     0.275  .0   ext
#
# poly          rds_poly    vw    0.00    0.0   .0   all
#
# alu1          rds_alu1    vw    0.01    0.03  .0   all
# calu1         rds_alu1    vw    0.01    0.03  .0   all
# talu1         rds_talu1   vw    0.01    0.03  .0   all

```

```
alu2      rds_alu2    vw     0.0     0.0     .0     all
calu2     rds_alu2    vw     0.0     0.0     .0     all
talu2     rds_talu2   vw     0.0     0.0     .0     all

alu3      rds_alu3    vw     0.0     0.0     .0     all
calu3     rds_alu3    vw     0.0     0.0     .0     all
talu3     rds_talu3   vw     0.0     0.0     .0     all

alu4      rds_alu4    vw     0.19    0.0     .0     all
calu4     rds_alu4    vw     0.19    0.0     .0     all
talu4     rds_talu4   vw     0.19    0.0     .0     all

alu5      rds_alu5    vw     0.225   0.0     .0     all
calu5     rds_alu5    vw     0.225   0.0     .0     all
talu5     rds_talu5   vw     0.225   0.0     .0     all

alu6      rds_alu6    vw     0.30    0.0     .0     all
calu6     rds_alu6    vw     0.30    0.0     .0     all
talu6     rds_talu6   vw     0.30    0.0     .0     all

talu7     rds_nimp    vw     0.00    0.0     .0     all
talu8     rds_pimp    vw     0.00    0.0     .0     all
end

table mbk_to_rds_connector
# _____
# mbk_name   rds_name  der  dwr
# _____
# end

table mbk_to_rds_reference
# _____
# mbk_name   rds_name  width
# _____
# ref_ref    rds_ref    0.330
# ref_con    rds_ref    0.330
# _____
# end

table mbk_to_rds_via
# _____
# mbk_name   rds_name1 width mode   rds_name2 width mode   ...
# _____
## _____
# difftap.5
# licon.7 0.170+0.120*2
cont_body_n \
  rds_cont      0.170  all \
  rds_alu1      0.410  all \
  rds_nimp      0.660  all \
  rds_ntie      0.410  all
```

```
# licon.7 0.170+0.120*2
# difftap.5
cont_body_p \
    rds_cont      0.170  all\
    rds_alu1     0.410  all\
    rds_pimp     0.660  all\
    rds_ptie     0.410  all

# licon.5c
cont_dif_n \
    rds_cont      0.170  all\
    rds_alu1     0.330  all\
    rds_activ    0.290  drc\
    rds_nimp     0.540  all\
    rds_ndif     0.420  all

# licon.5c
cont_dif_p \
    rds_cont      0.170  all\
    rds_alu1     0.330  all\
    rds_activ    0.290  drc\
    rds_pimp     0.540  all\
    rds_pdif     0.420  all

# licon.8a
# NPC —> poly2
cont_poly \
    rds_cont      0.170  all\
    rds_poly     0.330  all\
    rds_alu1     0.330  all

# m1.4
# NPC —> poly2
# m1.5
cont_via \
    rds_via1     0.170  all\
    rds_alu1     0.330  all\
    rds_alu2     0.330  all

# via.1b
# via.5b
# m2.5
cont_via2 \
    rds_via2     0.150  all\
    rds_alu2     0.370  all\
    rds_alu3     0.370  all

# via.1b
# via.5b
```

```
# m2.5
  cont_via3 \
    rds_via3      0.200  all \
    rds_alu3      0.370  all \
    rds_alu4      0.370  all

  cont_via4 \
    rds_via4      0.200  all \
    rds_alu4      0.490  all \
    rds_alu5      0.380  all
end

table mbk_to_rds_bigvia_hole
#
# mbk_via_name  rds_hole_name  side  step  mode
#
CONT_VIA  RDS_VIA1  0.17  0.34  ALL
CONT_VIA2 RDS_VIA2  0.15  0.32  ALL
CONT_VIA3 RDS_VIA3  0.20  0.37  ALL
CONT_VIA4 RDS_VIA4  0.20  0.38  ALL  # should be more than 4
CONT_VIA5 RDS_VIA5  0.80  1.60  ALL  # should be more than 4
end

table mbk_to_rds_bigvia_metal
#
# mbk_via_name  rds_name   dwr  overlap  mode
#
CONT_VIA  RDS_ALU1  0.0  0.330  ALL RDS_ALU2  0.0  0.330  ALL
CONT_VIA2 RDS_ALU2  0.0  0.370  ALL RDS_ALU3  0.0  0.370  ALL
CONT_VIA3 RDS_ALU3  0.0  0.370  ALL RDS_ALU4  0.0  0.370  ALL
CONT_VIA4 RDS_ALU4  0.0  0.5    ALL RDS_ALU5  0.0  0.380  ALL
CONT_VIA5 RDS_ALU5  0.0  0.5    ALL RDS_ALU6  0.0  0.8    ALL
end

table mbk_to_rds_turnvia
#
# mbk_name  rds_name  dwr  mode
#
  cont_turn1 rds_alu1      0.03  all
  cont_turn2 rds_alu2      0.03  all
  cont_turn3 rds_alu3      0.03  all
  cont_turn4 rds_alu4      0.00  all
  cont_turn5 rds_alu5      0.00  all
end

table lynx_bulk_implicit
#
# rds_name  type [ explicit | implicit ]
#
end
```

```
table lynx_transistor
#
# mbk_name trans_name compostion
#
# ntrans  ntrans c_x_n rds_poly rds_ndif rds_ndif rds_pwell
# ptrans  ptrans c_x_p rds_poly rds_pdif rds_pdif rds_nwell
end

table lynx_diffusion
#
# rds_name compostion
#
# rds_ndif  rds_activ 1 rds_nimp 1 rds_nwell 0
# rds_pdif  rds_activ 1 rds_pimp 1 rds_nwell 1
# rds_ntie  rds_activ 1 rds_nimp 1 rds_nwell 1
# rds_ptie  rds_activ 1 rds_pimp 1 rds_nwell 0
end

table lynx_graph
#
# rds_name in_contact_with rds_name1 rds_name2 ...
#
# rds_ndif  rds_cont  rds_ndif
# rds_pdif  rds_cont  rds_pdif
# rds_poly  rds_cont  rds_poly
# rds_cont  rds_pdif  rds_ndif  rds_poly  rds_alu1  rds_cont
# rds_alu1  rds_cont  rds_via1  rds_ref   rds_alu1
# rds_ref   rds_cont  rds_via1  rds_alu1  rds_ref
# rds_alu2  rds_via1  rds_via2  rds_alu2
# rds_alu3  rds_via2  rds_via3  rds_alu3
# rds_alu4  rds_via3  rds_via4  rds_alu4
# rds_alu5  rds_via4  rds_via5  rds_alu5
# RDS_VIA1 RDS_ALU1 RDS_ALU2 RDS_VIA1
# RDS_VIA2 RDS_ALU2 RDS_ALU3 RDS_VIA2
# RDS_VIA3 RDS_ALU3 RDS_ALU4 RDS_VIA3
# RDS_VIA4 RDS_ALU4 RDS_ALU5 RDS_VIA4
# RDS_VIA5 RDS_ALU5 RDS_ALU6 RDS_VIA5
end

table s2r_oversize_denotch
#
# rds_name oversized_value_for_denotching
#
# rds_nwell      0.635
# rds_pwell      0.635
# rds_poly       0.100
# rds_alu1       0.080
# rds_alu2       0.080
# rds_alu3       0.080
```

```
rds_alu4      0.080
rds_alu5      0.080
rds_activ     0.130
rds_ntie      0.190
rds_ptie      0.190
rds_nimp      0.190
rds_pimp      0.190
end

table s2r_bloc_ring_width
#
# rds_name ring_width_to_copy_up
#
rds_nwell    0. # [ RD_NWEL ]
# rds_pwell   0. # [ RD_PWEL ]
rds_poly     0. # [ RD_POLY ]
rds_alu1     0. # [ RD_ALU1 ]
rds_alu2     0. # [ RD_ALU2 ]
rds_alu3     0. # [ RD_ALU3 ]
rds_alu4     0. # [ RD_ALU3 ]
rds_alu5     0. # [ RD_ALU3 ]
rds_activ    0. # [ RD_ACTI ]
rds_ntie     0. # [ RD_NIMP ]
rds_ptie     0. # [ RD_PIMP ]
rds_nimp     0. # [ RD_NIMP ]
rds_pimp     0. # [ RD_PIMP ]
end

table s2r_minimum_layer_width
#
# rds_name min_layer_width_to_keep
#
rds_nwell    0.840
# rds_pwell   0.840
rds_poly     0.150
rds_alu1     0.170
rds_alu2     0.170
rds_alu3     0.170
rds_alu4     0.300
rds_alu5     0.300
rds_activ    0.420
rds_ntie     0.380
rds_ptie     0.380
rds_nimp     0.380
rds_pimp     0.380
end

table s2r_post_treat
#
# rds_name s2r_must_treat_or_not second_layer_whenever_scotch
```

```
# _____
#   rds_nwell      treat null
#   rds_pwell      treat null
#   rds_poly       treat null
#   rds_activ      treat null
#   rds_ntie       treat null
#   rds_ptie       treat null
#   rds_nimp       treat null
#   rds_pimp       treat null
#   rds_alu1       treat null
#   rds_alu2       treat null
#   rds_alu3       treat null
#   rds_alu4       treat null
#   rds_alu5       treat null
#   rds_cont       notreat null
end
```

DRC RULES

```
layer RDS_NWELL  0.840 ;
layer RDS_NTIE   0.380 ;
layer RDS_PTIE   0.380 ;
layer RDS_NIMP   0.380 ;
layer RDS_PIMP   0.380 ;
layer RDS_ACTIV  0.420 ;
layer RDS_CONT   0.170 ;
layer RDS_POLY   0.150 ;
layer RDS_VIA1   0.300 ;
layer RDS_VIA2   0.300 ;
layer RDS_VIA3   0.300 ;
layer RDS_VIA4   0.300 ;
layer RDS_VIA5   0.300 ;
layer RDS_ALU1   0.170 ;
layer RDS_ALU2   0.170 ;
layer RDS_ALU3   0.170 ;
layer RDS_ALU4   0.300 ;
layer RDS_ALU5   0.300 ;
layer RDS_ALU6   0.300 ;
layer RDS_USER0  0.005 ;
layer RDS_USER1  0.005 ;
layer RDS_USER2  0.005 ;
```

regles

```
# note : ``min'' is different from ``>=''.
# min is applied on polygons and >= is applied on rectangles.
# there is the same difference between max and <=.
# >= is faster than min, but min must be used where it is
# required to consider polygons, for example distance of
# two objects in the same layer
```

```
#  
#  
  
# check the nwell shapes  
#  
characterize RDS_NWELL (  
    rule    1 : width      >=      0.840 ;  
    rule    2 : intersection_length min      0.840 ;  
    rule    3 : notch       >=      1.270 ;  
);  
relation RDS_NWELL , RDS_NWELL (  
    rule    4 : spacing axial min      1.270 ;  
);  
relation RDS_NWELL , RDS_ACTI (  
    rule    5 : spacing axial min      0.340 ;  
);  
  
# check the RDS_PIMP shapes  
#  
characterize RDS_PIMP (  
    rule    6 : surface      min      0.265 ;  
    rule    7 : width        >=      0.380 ;  
    rule    8 : intersection_length min      0.380 ;  
    rule    9 : notch        >=      0.380 ;  
);  
relation RDS_PIMP , RDS_PIMP (  
    rule    10 : spacing axial min     0.380 ;  
);  
  
# check the RDS_NIMP shapes  
#  
characterize RDS_NIMP (  
    rule    11 : surface      min      0.265 ;  
    rule    12 : width        >=      0.380 ;  
    rule    13 : intersection_length min      0.380 ;  
    rule    14 : notch        >=      0.380 ;  
);  
relation RDS_NIMP , RDS_NIMP (  
    rule    15 : spacing axial min     0.380 ;  
);  
  
# check the RDS_PTIE shapes  
#  
characterize RDS_PTIE (  
#    rule    16 : surface      min      0.255 ;  
    rule    17 : width        >=      0.150 ;  
    rule    18 : intersection_length min      0.150 ;  
    rule    19 : notch        >=      0.270 ;  
);  
relation RDS_PTIE , RDS_PTIE (
```

```
rule    20 : spacing axial min      0.270 ;
);

# check the RDS_NTIE shapes
# -----
characterize RDS_NTIE (
# rule   21 : surface           min 0.265 ;
rule   22 : width            >= 0.150 ;
rule   23 : intersection_length min 0.150 ;
rule   24 : notch             >= 0.270 ;
);
relation RDS_NTIE , RDS_NTIE (
rule   25 : spacing axial min 0.270 ;
);

# check the RDS_ACTI shapes
# -----
characterize RDS_ACTI (
rule   26 : surface           min 0.000 ;
rule   27 : width            >= 0.420 ;
rule   28 : intersection_length min 0.420 ;
rule   29 : notch             >= 0.270 ;
);
relation RDS_ACTI, RDS_ACTI (
rule   30 : spacing axial min 0.270 ;
);

# check the RDS_NIMP RDS_PTIE exclusion
# -----
define RDS_NIMP , RDS_PTIE intersection -> NPIMP;
characterize NPIMP (
rule   31 : width = 0. ;
);
undefine NPIMP;

# check the RDS_NTIE RDS_PIMP exclusion
# -----
define RDS_NTIE , RDS_PIMP intersection -> NPIMP;
characterize NPIMP (
rule   32 : width = 0. ;
);
undefine NPIMP;

# check the RDS_POLY shapes
# -----
characterize RDS_POLY (
rule   33 : width >= 0.150 ;
rule   34 : intersection_length min 0.150 ;
rule   35 : notch >= 0.210 ;
);
```

```
relation RDS.POLY , RDS.POLY (
    rule 36 : spacing axial min      0.210 ;
);

define RDS_ACTI , RDS.POLY intersection -> channel;

# check the channel shapes
# _____
characterize channel (
    rule 37 : notch             >=      0.210 ;
);
relation channel , channel (
    rule 38 : spacing axial min      0.210 ;
);

undefine channel;

define RDS_ACTI , RDS.CONT intersection -> cont_diff;

relation RDS.POLY , cont_diff (
    rule 39 : spacing axial >=      0.055 ;
);

undefine cont_diff;

# check any_via layers , stacking are free
# _____
relation RDS.CONT , RDS.CONT (
    rule 40 : spacing axial >=      0.170 ;
);

characterize RDS.CONT (
    rule 41 : width            =      0.170 ;
    rule 42 : length           =      0.170 ;
);

# check RDS.POLY is distant from activ zone of transistor
# _____
relation RDS.POLY , RDS.ACTIV (
    rule 43 : spacing axial >=      0.075 ;
);

# check RDS_ALU1 shapes
# _____
characterize RDS_ALU1 (
    rule 44 : surface          min      0.060 ;
    rule 45 : width             >=      0.170 ;
    rule 46 : intersection_length min      0.170 ;
    rule 47 : notch              >=      0.170 ;
);
```

```
relation RDS_ALU1 , RDS_ALU1 (
    rule 48 : spacing axial min      0.170 ;
);

# check mcon layers , stacking are free
# -----
relation RDS_VIA1 , RDS_VIA1 (
    rule 49 : spacing axial >=      0.190 ;
);

characterize RDS_VIA1 (
    rule 50 : width          =      0.170 ;
    rule 51 : length         =      0.170 ;
);

# check RDS_ALU2 shapes
# -----
characterize RDS_ALU2 (
#   rule 52 : surface        min      0.085 ;
    rule 53 : width          >=      0.140 ;
    rule 54 : intersection_length min      0.140 ;
    rule 55 : notch           >=      0.140 ;
);
relation RDS_ALU2 , RDS_ALU2 (
    rule 56 : spacing axial min      0.140 ;
);

# check any_via layers , stacking are free
# -----
relation RDS_VIA2 , RDS_VIA2 (
    rule 57 : spacing axial >=      0.170 ;
);

characterize RDS_VIA2 (
    rule 58 : width          =      0.150 ;
    rule 59 : length         =      0.150 ;
);

# check RDS_ALU3 shapes
# -----
characterize RDS_ALU3 (
#   rule 60 : surface        min      0.070 ;
    rule 61 : width          >=      0.140 ;
    rule 62 : intersection_length min      0.140 ;
    rule 63 : notch           >=      0.140 ;
);
relation RDS_ALU3 , RDS_ALU3 (
```

```
rule    64 : spacing axial min      0.140 ;
);

# check any_via layers , stacking are free
#
relation RDS_VIA3 , RDS_VIA3 (
    rule    65 : spacing axial >=      0.200 ;
);

characterize RDS_VIA3 (
    rule    66 : width          =      0.200 ;
    rule    67 : length         =      0.200 ;
);
# check RDS_ALU4 shapes
#
characterize RDS_ALU4 (
#   rule    68 : surface        min      0.240 ;
    rule    69 : width          >=      0.300 ;
    rule    70 : intersection_length min      0.300 ;
    rule    71 : notch           >=      0.300 ;
);
relation RDS_ALU4 , RDS_ALU4 (
    rule    72 : spacing axial min      0.300 ;
);

# check any_via layers , stacking are free
#
relation RDS_VIA4 , RDS_VIA4 (
    rule    73 : spacing axial >=      0.200 ;
);

characterize RDS_VIA4 (
    rule    74 : width          =      0.200 ;
    rule    75 : length         =      0.200 ;
);
# check RDS_ALU5 shapes
#
characterize RDS_ALU5 (
#   rule    76 : surface        min      0.240 ;
    rule    77 : width          >=      0.300 ;
    rule    78 : intersection_length min      0.300 ;
    rule    79 : notch           >=      0.300 ;
);
relation RDS_ALU5 , RDS_ALU5 (
    rule    80 : spacing axial min      0.300 ;
);
```

```
# check any_via layers , stacking are free
#
relation RDS_VIA5 , RDS_VIA5 (
    rule 81 : spacing axial >=      0.200 ;
);

characterize RDS_VIA5 (
    rule 82 : width          =      0.200 ;
    rule 83 : length         =      0.200 ;
);

# check RDS_ALU6 shapes
#
characterize RDS_ALU6 (
#   rule 84 : surface        min      0.240 ;
    rule 85 : width          >=      0.300 ;
    rule 86 : intersection_length min      0.300 ;
    rule 87 : notch           >=      0.300 ;
);
relation RDS_ALU6 , RDS_ALU6 (
    rule 88 : spacing axial min      0.300 ;
);

end rules
DRC_COMMENT
1 (RDS_NWELL) Minimum width 0.840
2 (RDS_NWELL) Intersection length 0.840
3 (RDS_NWELL) Notch 1.270
4 (RDS_NWELL,RDS_NWELL) Manhattan distance min 1.270
5 (RDS_NWELL,RDS_ACTI) Manhattan distance min 0.340
6 (RDS_PIMP) Minimum area 0.265
7 (RDS_PIMP) Minimum width 0.380
8 (RDS_PIMP) Intersection length 0.380
9 (RDS_PIMP) Notch 0.380
10 (RDS_PIMP,RDS_PIMP) Manhattan distance min 0.380
11 (RDS_NIMP) Minimum area 0.265
12 (RDS_NIMP) Minimum width 0.380
13 (RDS_NIMP) Intersection length 0.380
14 (RDS_NIMP) Notch 0.380
15 (RDS_NIMP,RDS_NIMP) Manhattan distance min 0.380
16 (RDS_PTIE) Minimum area 0.255
17 (RDS_PTIE) Minimum width 0.150
18 (RDS_PTIE) Intersection length 0.150
19 (RDS_PTIE) Notch 0.270
20 (RDS_PTIE,RDS_PTIE) Manhattan distance min 0.270
21 (RDS_NTIE) Minimum area 0.265
22 (RDS_NTIE) Minimum width 0.150
23 (RDS_NTIE) Intersection length 0.150
24 (RDS_NTIE) Notch 0.270
```

25 (RDS_NTIE,RDS_NTIE) Manhattan distance min 0.270
26 (RDS_ACTI) Minimum area 0.0
27 (RDS_ACTI) Minimum width 0.420
28 (RDS_ACTI) Intersection length 0.420
29 (RDS_ACTI) Notch 0.270
30 (RDS_ACTI,RDS_ACTI) Manhattan distance min 0.270
31 (RDS_NIMP,RDS_PTIE) intersection width 0.
32 (RDS_PIMP,RDS_NTIE) intersection width 0.
33 (RDS_POLY) Minimum width 0.150
34 (RDS_POLY) Intersection length 0.150
35 (RDS_POLY) Notch 0.210
36 (RDS_POLY,RDS_POLY) Manhattan distance min 0.210
37 (channel) Notch 0.210
38 (channel) Manhattan distance min 0.210
39 (cont_diff) Manhattan distance min 0.055
40 (RDS_CONT,RDS_CONT) Manhattan distance min 0.170
41 (RDS_CONT) Width 0.170
42 (RDS_CONT) Length 0.170
43 (RDS_POLY,RDS_ACTIV) Manhattan distance min 0.075
44 (RDS_ALU1) Minimum area 0.060
45 (RDS_ALU1) Minimum width 0.170
46 (RDS_ALU1) Intersection length 0.170
47 (RDS_ALU1) Notch 0.170
48 (RDS_ALU1,RDS_ALU1) Manhattan distance min 0.170
49 (RDS_VIA1,RDS_VIA1) Manhattan distance mcon min 0.190
50 (RDS_VIA1) mcon width 0.170
51 (RDS_VIA1) mcon length 0.170
52 (RDS_ALU2) Minimum area 0.083
53 (RDS_ALU2) Minimum width 0.140
54 (RDS_ALU2) Intersection length 0.140
55 (RDS_ALU2) Notch 0.140
56 (RDS_ALU2,RDS_ALU2) Manhattan distance min 0.140
57 (RDS_VIA2,RDS_VIA2) Manhattan distance via min 0.170
58 (RDS_VIA2) via width 0.150
59 (RDS_VIA2) via length 0.150
60 (RDS_ALU3) Minimum area 0.0676
61 (RDS_ALU3) Minimum width 0.140
62 (RDS_ALU3) Intersection length 0.140
63 (RDS_ALU3) Notch 0.140
64 (RDS_ALU3,RDS_ALU3) Manhattan distance min 0.140
65 (RDS_VIA3,RDS_VIA3) Manhattan distance via min 0.200
66 (RDS_VIA3) via width 0.200
67 (RDS_VIA3) via length 0.200
68 (RDS_ALU4) Minimum area 0.240
69 (RDS_ALU4) Minimum width 0.300
70 (RDS_ALU4) Intersection length 0.300
71 (RDS_ALU4) Notch 0.300
72 (RDS_ALU4,RDS_ALU4) Manhattan distance min 0.300
73 (RDS_VIA4,RDS_VIA4) Manhattan distance via min 0.200
74 (RDS_VIA4) via width 0.200

4 RDS FILE FOR SKYWATER 130

```
75 (RDS_VIA4) via length 0.200
76 (RDS_ALU5) Minimum area 0.240
77 (RDS_ALU5) Minimum width 0.300
78 (RDS_ALU5) Intersection length 0.300
79 (RDS_ALU5) Notch 0.300
80 (RDS_ALU5,RDS_ALU5) Manhattan distance min 0.300
81 (RDS_VIA5,RDS_VIA5) Manhattan distance via min 0.200
82 (RDS_VIA5) via width 0.200
83 (RDS_VIA5) via length 0.200
84 (RDS_ALU6) Minimum area 0.240
85 (RDS_ALU6) Minimum width 0.300
86 (RDS_ALU6) Intersection length 0.300
87 (RDS_ALU6) Notch 0.300
88 (RDS_ALU6,RDS_ALU6) Manhattan distance min 0.300
END_DRC_COMMENT
END_DRC_RULES
```

5 RDS File for IHP sg13g2

This is the RDS file for IHP sg13g2.

```
# 20240522
#
# For IHP SG13G2 by Naohiko Shimizu
#
#
#
# globals define
#
define physical_grid      0.001
define lambda              0.075

table cif_layer
#
# rds_name      cif_name
#
rds_nwell      nwell
# rds_pwell      pwel
rds_activ      diff
rds_ntie       tap
rds_ptie       tap
rds_ndif       nsdm
rds_pdif       psdm
rds_nimp       nsdm
rds_pimp       psdm
rds_poly       poly
rds_alu1       li1
rds_alu2       met1
rds_alu3       met2
rds_alu4       met3
rds_alu5       met4
rds_alu6       met5
rds_cont       licon1
rds_via1       mcon
rds_via2       via
rds_via3       via2
rds_via4       via3
rds_via5       via4
rds_poly2      npc
rds_cpas       pad
end

table gds_layer
```

5 RDS FILE FOR IHP SG13G2

```
#  
# rds_name      gds_number gds_datatype  
# IHP uses only 0 gds_datatype for drawing  
#  
rds_nwell    31      0  
rds_pwell    46      0  
rds_activ     1       0  
rds_ptie     1       0  
rds_ntie     1       0  
rds_pdif     1       0  
rds_ndif     1       0  
rds_pimp    14      0  
rds_nimp     7       0  
rds_poly     5       0  
rds_alu1     8       0       8       2  
rds_alu2    10      0       10      2  
rds_alu3    30      0       30      2  
rds_alu4    50      0       50      2  
rds_alu5    67      0       67      2  
rds_alu6   126      0      126      2  
rds_cont     6       0  
rds_via1    19      0  
rds_via2    29      0  
rds_via3    49      0  
rds_via4    66      0  
rds_via5   125      0  
# rds_poly2   95      20  
rds_cpas     9       0  
end  
  
table lynx_resistor  
#  
# rds_name square_resistor(ohm/square) # typical values  
#  
# Poly resistor is differ from N-doped to P-doped. 7 ohm is for N-doped.  
# P-doped poly is 260 ohm  
  
rds_poly     7  
rds_alu1    0.115  
rds_alu2    0.088  
rds_alu3    0.088  
rds_alu4    0.088  
rds_alu5    0.088  
rds_alu6    0.018  
rds_cont    15  
rds_via1     9  
rds_via2     9  
rds_via3     9  
rds_via4     9  
rds_via5    2.2
```

5 RDS FILE FOR IHP SG13G2

```
end

table lynx_capa
# -----
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
#   rds_poly    35.3e-3  51.8e-6 # Ca max POLY_NWELL 2Cf0 max POLY_NWELL
#   rds_alu1    5.9e-5   8.5e-5 # Ca max M1_NWELL    2Cf0 max M1_NWELL
#   rds_alu2    6.8e-5   7.9e-5 # Ca max M2_NWELL    2Cf0 max M2_NWELL
#   rds_alu3    6.8e-5   6.8e-5 # Ca max M3_NWELL    2Cf0 max M3_NWELL
#   rds_alu4    6.8e-5   6.0e-5 # Ca max M4_NWELL    2Cf0 max M4_NWELL
#   rds_alu5    6.8e-5   6.0e-5 # hyp
#   rds_alu6    4.2e-5   6.0e-5
end

table lynx_capa_poly
# -----
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
# end

table lynx_capa_poly2
# -----
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
# end

table lynx_capa_alu1
# -----
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
# end

table lynx_capa_alu2
# -----
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
# end

table lynx_capa_alu3
# -----
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
# end

table lynx_capa_alu4
# -----
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
# end
```

```

table lynx_capa_alu5
#
# rds_name area_capa( pif/um^2) peri_capa( pif/um)
#
end
table mbk_to_rds_segment
#
# mbk_name      rds_name1 dlr dwr offset mode      rds_name2 dlr dwr offset mode
#
nwell    rds_nwell   vw    0.460   0.000   .0   all \
          rds_pimp    vw    0.075   -0.645   0.45   all \
          rds_nimp    vw    0.0    -1.53    2.88   all
#
# pwell    rds_pwell   vw    0.460   0.000   .0   all
#           rds_pimp    vw    0.225   0.170   .0   all
ndif     rds_activ   vw    0.01    0.015   .0   all \
          rds_nimp    vw    0.01    0.015   .0   all \
          rds_ndif    vw    0.01    0.015   .0   ext
pdif     rds_activ   vw    0.01    0.015   .0   all \
          rds_pimp    vw    0.19    0.380   .0   all \
          rds_pdif    vw    0.01    0.015   .0   all
ntie     rds_ntie    vw    0.010   0.015   .0   all \
          rds_nimp    vw    0.270   0.120   .0   all \
          rds_nwell   vw    0.460   0.510   .0   all
ptie     rds_ptie    vw    0.010   0.015   .0   all \
          rds_pimp    vw    0.270   0.040   .0   all \
#
#           rds_pwell   vw    0.460   0.510   .0   all
ntrans   rds_poly    vw    0.19    -0.020   .0   all \
          rds_activ   vw    0.01    0.48    .0   drc \
          rds_nimp    vw    0.01    0.48    .0   drc \
          rds_ndif    lcw   0.01    0.24    -0.005  all \
          rds_ndif    rcw   0.01    0.24    -0.005  all
ptrans   rds_poly    vw    0.19    -0.020   .0   all \
          rds_activ   vw    0.01    0.48    .0   drc \
          rds_pimp    vw    0.19    0.48    .0   all \
          rds_pdif    lcw   0.01    0.24    -0.005  all \
          rds_pdif    rcw   0.01    0.24    -0.005  all
poly     rds_poly    vw    0.0    -0.020   .0   all
alu1     rds_alu1    vw    0.005   0.01    .0   all
calu1   rds_alu1    vw    0.005   0.01    .0   all

```

5 RDS FILE FOR IHP SG13G2

```
talul    rds_talu1    vw    0.005    0.01    .0    all
alul    rds_alu2    vw    0.11    0.01    .0    all
calu2    rds_alu2    vw    0.11    0.01    .0    all
talul    rds_talu2    vw    0.11    0.01    .0    all
alul    rds_alu3    vw    0.11    0.0    .0    all
calu3    rds_alu3    vw    0.11    0.0    .0    all
talul    rds_talu3    vw    0.11    0.0    .0    all
alul    rds_alu4    vw    0.15    0.0    .0    all
calu4    rds_alu4    vw    0.15    0.0    .0    all
talul    rds_talu4    vw    0.15    0.0    .0    all
alul    rds_alu5    vw    0.15    0.0    .0    all
calu5    rds_alu5    vw    0.15    0.0    .0    all
talul    rds_talu5    vw    0.15    0.0    .0    all
talul    rds_nimp    vw    0.00    0.0    .0    all
talul    rds_pimp    vw    0.00    0.0    .0    all
end

table mbk_to_rds_connector
#
# mbk_name    rds_name    der    dwr
#
end

table mbk_to_rds_reference
#
# mbk_name    rds_name    width
#
ref_ref    rds_ref    0.330
ref_con    rds_ref    0.330
end

table mbk_to_rds_via
#
# mbk_name    rds_name1    width    mode    rds_name2    width    mode    ...
##
# difftap.5
# licon.7 0.170+0.120*2
cont_body_n \
    rds_cont    0.160    all \
    rds_alu1    0.300    all \
#    rds_nimp    0.430    all \
    rds_ntie    0.300    ext

# licon.7 0.170+0.120*2
# difftap.5
cont_body_p \
```

5 RDS FILE FOR IHP SG13G2

```
rds_cont      0.160  all \
rds_alu1      0.300  all \
rds_pimp      0.340  all \
rds_ptie      0.300  ext

# licon.5c
cont_dif_n \
rds_cont      0.160  all \
rds_alu1      0.300  all \
rds_activ     0.300  drc \
rds_ndif      0.420  ext

# licon.5c
cont_dif_p \
rds_cont      0.160  all \
rds_alu1      0.300  all \
rds_activ     0.300  drc \
rds_pimp      0.340  all \
rds_pdif      0.420  ext

# copy
cont_poly \
rds_cont      0.160  all \
rds_poly      0.300  all \
rds_alu1      0.300  all

# m1.4
# NPC —> poly2
# m1.5
cont_via \
rds_via1      0.190  all \
rds_alu1      0.300  all \
rds_alu2      0.380  all

# via.1b
# via.5b
# m2.5
cont_via2 \
rds_via2      0.190  all \
rds_alu2      0.380  all \
rds_alu3      0.380  all

# via.1b
# via.5b
# m2.5
cont_via3 \
rds_via3      0.190  all \
rds_alu3      0.380  all
```

5 RDS FILE FOR IHP SG13G2

```
rds_alu4      0.380  all
cont_via4 \
    rds_via4      0.190  all \
    rds_alu4      0.380  all \
    rds_alu5      0.380  all
end

table mbk_to_rds_bigvia_hole
# _____
# mbk_via_name   rds_hole_name side step mode
# _____
# end

table mbk_to_rds_bigvia_metal
# _____
# mbk_via_name   rds_name   dwr overlap mode
# _____
# end

table mbk_to_rds_turnvia
# _____
# mbk_name rds_name dwr mode
# _____
# cont_turn1 rds_alu1      0.085 all
# cont_turn2 rds_alu2      0.01  all
# cont_turn3 rds_alu3      0.01  all
# cont_turn4 rds_alu4      0.01  all
# cont_turn5 rds_alu5      0.01  all
end

table lynx_bulk_implicit
# _____
# rds_name type[ explicit | implicit ]
# _____
# end

table lynx_transistor
# _____
# mbk_name trans_name compostion
# _____
# ntrans  ntrans c_x_n rds_poly rds_ndif rds_ndif rds_pwell
# ptrans  ptrans c_x_p rds_poly rds_pdif rds_pimp rds_nwell
# _____
# end

table lynx_diffusion
# _____
# rds_name compostion
# _____
# end
```

5 RDS FILE FOR IHP SG13G2

```
table lynx_graph
#
# rds_name    in_contact_with    rds_name1   rds_name2   ...
#
rds_ndif      rds_cont       rds_ndif
rds_pdif      rds_cont       rds_pdif
rds_poly      rds_cont       rds_poly
rds_cont      rds_pdif       rds_ndif     rds_poly     rds_alu1   rds_cont
rds_alu1      rds_cont       rds_via1    rds_ref     rds_alu1
rds_ref       rds_cont       rds_via1    rds_alu1   rds_ref
RDS_VIA1     RDS_ALU1      RDS_ALU2    RDS_VIA1
RDS_VIA2     RDS_ALU2      RDS_ALU3    RDS_VIA2
RDS_VIA3     RDS_ALU3      RDS_ALU4    RDS_VIA3
RDS_VIA4     RDS_ALU4      RDS_ALU5    RDS_VIA4
RDS_VIA5     RDS_ALU5      RDS_ALU6    RDS_VIA5
rds_alu2      rds_via1      rds_via2    rds_alu2
rds_alu3      rds_via2      rds_via3    rds_alu3
rds_alu4      rds_via3      rds_via4    rds_alu4
rds_alu5      rds_via4      rds_via5    rds_alu5
end

table s2r_oversize_denoatch
#
# rds_name    oversized_value_for_denoatching
#
rds_nwell    0.635
rds_pwell    0.635
rds_poly     0.100
rds_alu1     0.080
rds_alu2     0.080
rds_alu3     0.080
rds_alu4     0.080
rds_alu5     0.080
rds_activ    0.130
rds_ntie     0.190
rds_ptie     0.190
rds_nimp     0.150
rds_pimp     0.150
end

table s2r_bloc_ring_width
#
# rds_name    ring_width_to_copy_up
#
rds_nwell    0. # [ RD_NWEL ]
rds_pwell    0. # [ RD_PWEL ]
rds_poly     0. # [ RD_POLY ]
rds_alu1     0. # [ RD_ALU1 ]
rds_alu2     0. # [ RD_ALU2 ]
```

5 RDS FILE FOR IHP SG13G2

```
rds_alu3      0. # [ RD_ALU3 ]
rds_alu4      0. # [ RD_ALU3 ]
rds_alu5      0. # [ RD_ALU3 ]
rds_activ     0. # [ RD_ACTI ]
rds_ntie      0. # [ RD_NIMP ]
rds_ptie      0. # [ RD_PIMP ]
rds_nimp      0. # [ RD_NIMP ]
rds_pimp      0. # [ RD_PIMP ]
end

table s2r_minimum_layer_width
# -----
# rds_name    min_layer_width_to_keep
#
# -----
rds_nwell      0.840
rds_pwell      0.840
rds_poly       0.150
rds_alu1       0.170
rds_alu2       0.170
rds_alu3       0.170
rds_alu4       0.300
rds_alu5       0.300
rds_activ      0.420
rds_ntie       0.380
rds_ptie       0.380
rds_nimp       0.310
rds_pimp       0.310
end

table s2r_post_treat
# -----
# rds_name    s2r_must_treat_or_not    second_layer_whenever_scotch
#
# -----
rds_nwell      treat rds_pwell
rds_pwell      treat rds_nwell
rds_poly       treat null
rds_activ      treat null
rds_ntie       treat rds_pimp
rds_ptie       treat rds_nimp
rds_nimp       treat rds_ptie
rds_pimp       treat rds_ntie
rds_alu1       treat null
rds_alu2       treat null
rds_alu3       treat null
rds_alu4       treat null
rds_alu5       treat null
rds_cont       notreat null
end
```

DRC RULES

```
layer RDS_NWELL    0.840 ;
layer RDS_NTIE     0.380 ;
layer RDS_PTIE     0.380 ;
layer RDS_NIMP      0.380 ;
layer RDS_PIMP      0.380 ;
layer RDS_ACTIV     0.420 ;
layer RDS_CONT      0.170 ;
layer RDS_POLY      0.150 ;
layer RDS_ALU1      0.170 ;
layer RDS_ALU2      0.170 ;
layer RDS_ALU3      0.170 ;
layer RDS_ALU4      0.300 ;
layer RDS_ALU5      0.300 ;
layer RDS_USER0     0.005 ;
layer RDS_USER1     0.005 ;
layer RDS_USER2     0.005 ;

regles

# note : ``min'' is different from ``>=''.
# min is applied on polygons and >= is applied on rectangles.
# there is the same difference between max and <=.
# >= is faster than min, but min must be used where it is
# required to consider polygons, for example distance of
# two objects in the same layer
#
# -----
# check the nwell shapes
# -----
characterize RDS_NWELL (
    rule    1 : width      >=      0.620 ;
    rule    2 : intersection_length min      0.620 ;
    rule    3 : notch       >=      0.62 ;
);
relation RDS_NWELL , RDS_NWELL (
    rule    4 : spacing axial   min      0.62 ;
);
relation RDS_NWELL , RDS_ACTI (
    rule    5 : spacing axial   min      0.31 ;
);

# check the RDS_PIMP shapes
# -----
characterize RDS_PIMP (
    rule    6 : surface        min      0.25 ;
    rule    7 : width          >=      0.310 ;
    rule    8 : intersection_length min      0.310 ;
    rule    9 : notch          >=      0.310 ;
```

5 RDS FILE FOR IHP SG13G2

```
);

relation RDS_PIMP , RDS_PIMP (
    rule 10 : spacing axial min      0.310 ;
);

# check the RDS_PTIE shapes
# -----
characterize RDS_PTIE (
    rule 16 : surface           min      0.255 ;
    rule 17 : width            >=      0.380 ;
    rule 18 : intersection_length min      0.380 ;
    rule 19 : notch             >=      0.380 ;
);
relation RDS_PTIE , RDS_PTIE (
    rule 20 : spacing axial min      0.380 ;
);

# check the RDS_NTIE shapes
# -----
characterize RDS_NTIE (
    rule 21 : surface           min      0.265 ;
    rule 22 : width            >=      0.380 ;
    rule 23 : intersection_length min      0.380 ;
    rule 24 : notch             >=      0.380 ;
);
relation RDS_NTIE , RDS_NTIE (
    rule 25 : spacing axial min      0.380 ;
);

# check the RDS_ACTI shapes
# -----
characterize RDS_ACTI (
    rule 26 : surface           min      0.125 ;
    rule 27 : width            >=      0.15 ;
    rule 28 : intersection_length min      0.15 ;
    rule 29 : notch             >=      0.21 ;
);
relation RDS_ACTI, RDS_ACTI (
    rule 30 : spacing axial min      0.210 ;
);

# check the RDS_NIMP RDS_PTIE exclusion
# -----
define RDS_NIMP , RDS_PTIE intersection -> NPIMP;
characterize NPIMP (
    rule 31 : width           =      0. ;
);
undefine NPIMP;
```

5 RDS FILE FOR IHP SG13G2

```
# check the RDS_NTIE RDS_PIMP exclusion
# _____
define RDS_NTIE , RDS_PIMP intersection -> NPIMP;
characterize NPIMP (
    rule 32 : width          =      0. ;
);
undefine NPIMP;

# check the RDS_POLY shapes
# _____
characterize RDS_POLY (
    rule 33 : width          >=     0.130 ;
    rule 34 : intersection_length min   0.130 ;
    rule 35 : notch           >=     0.18 ;
);
relation RDS_POLY , RDS_POLY (
    rule 36 : spacing axial min   0.18 ;
);

define RDS_ACTI , RDS_POLY intersection -> channel;

# check the channel shapes
# _____
characterize channel (
    rule 37 : notch           >=     0.18 ;
);
relation channel , channel (
    rule 38 : spacing axial min   0.18 ;
);

undefine channel;

define RDS_ACTI , RDS_CONT intersection -> cont_diff;

relation RDS_POLY , cont_diff (
    rule 39 : spacing axial >=     0.11 ;
);

undefine cont_diff;

# check RDS_ALU1 shapes
# _____
characterize RDS_ALU1 (
    rule 40 : surface          min   0.090 ;
    rule 41 : width            >=     0.160 ;
    rule 42 : intersection_length min   0.160 ;
    rule 43 : notch            >=     0.180 ;
);
relation RDS_ALU1 , RDS_ALU1 (
    rule 44 : spacing axial min   0.180 ;
);
```

5 RDS FILE FOR IHP SG13G2

```
);

# check any_via layers , stacking are free
#
relation RDS_CONT , RDS_CONT (
    rule 45 : spacing axial >=      0.180 ;
);

characterize RDS_CONT (
    rule 46 : width          =      0.160 ;
    rule 47 : length         =      0.160 ;
);

# check RDS_POLY is distant from activ zone of transistor
#
relation RDS_POLY , RDS_ACTIV (
    rule 48 : spacing axial >=      0.07 ;
);

end rules
DRC_COMMENT
1 (RDS_NWELL) Minimum width 0.620
2 (RDS_NWELL) Intersection length 0.620
3 (RDS_NWELL) Notch 0.62
4 (RDS_NWELL,RDS_NWELL) Manhattan distance min 0.62
5 (RDS_NWELL,RDS_ACTI) Manhattan distance min 0.310
6 (RDS_PIMP) Minimum area 0.25
7 (RDS_PIMP) Minimum width 0.310
8 (RDS_PIMP) Intersection length 0.310
9 (RDS_PIMP) Notch 0.310
10 (RDS_PIMP,RDS_PIMP) Manhattan distance min 0.310
16 (RDS_PTITE) Minimum area 0.255
17 (RDS_PTITE) Minimum width 0.380
18 (RDS_PTITE) Intersection length 0.380
19 (RDS_PTITE) Notch 0.380
20 (RDS_PTITE,RDS_PTITE) Manhattan distance min 0.380
21 (RDS_NTITE) Minimum area 0.265
22 (RDS_NTITE) Minimum width 0.380
23 (RDS_NTITE) Intersection length 0.380
24 (RDS_NTITE) Notch 0.380
25 (RDS_NTITE,RDS_NTITE) Manhattan distance min 0.380
26 (RDS_ACTI) Minimum area 0.125
27 (RDS_ACTI) Minimum width 0.15
28 (RDS_ACTI) Intersection length 0.15
29 (RDS_ACTI) Notch 0.210
30 (RDS_ACTI,RDS_ACTI) Manhattan distance min 0.210
31 (RDS_NIMP,RDS_PTIE) intersection width 0.
32 (RDS_PIMP,RDS_NTIE) intersection width 0.
33 (RDS_POLY) Minimum width 0.130
34 (RDS_POLY) Intersection length 0.130
```

5 RDS FILE FOR IHP SG13G2

```
35 (RDS.POLY) Notch 0.18
36 (RDS.POLY,RDS.POLY) Manhattan distance min 0.18
37 (channel) Notch 0.18
38 (channel) Manhattan distance min 0.18
39 (cont_diff) Manhattan distance min 0.11
40 (RDS_ALU1) Minimum area 0.090
41 (RDS_ALU1) Minimum width 0.160
42 (RDS_ALU1) Intersection length 0.160
43 (RDS_ALU1) Notch 0.180
44 (RDS_ALU1,RDS_ALU1) Manhattan distance min 0.180
45 (RDS_CONT,RDS_CONT) Manhattan distance min 0.180
46 (RDS_CONT) Width 0.160
47 (RDS_CONT) Length 0.160
48 (RDS.POLY,RDS.ACTIV) Manhattan distance min 0.07
END.DRC.COMMENT
END.DRC.RULES
```