

# NSXLIB v2.0 User Manual

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# 1 Scalable Design Rules

Back to 80s, we had the lambda based scalable design rules, especially the book 'The Introduction to VLSI Systems' by Mead and Conway was famous. MOSIS keep the scalable design rules as SCMSOS for years. But it have been difficult to keep the rules scalable and the processes available to the SCMSOS decrease. The latest SCMSOS rules is the MOSIS SCMSOS DEEP design rules v8.0<sup>1</sup>. On the other hand, Alliance also uses lambda based design system. Unlike Mead and Conway method, Alliance has modification ability for each segments in the design. Typically, the segments in a cell like the poly or metal, can be enlarge or en-wide with parameter file called RDS.

## 1.1 The scalable cell library sxlib

Alliance has a scalable cell library named sxlib. It has many cells in the library and long time used in LIP6. The segments are defined in lambda. But the RDS adjust the segments in micro meters. The sxlib uses one lambda for the minimum design future. Then the gate width of transistor is one lambda, where MOSIS SCMSOS uses two lambda for the gate width. The cell design in sxlib uses center to center alignment for bending segments. The figure 1 shows a example of the transformation of the lambda segments to the real layout.

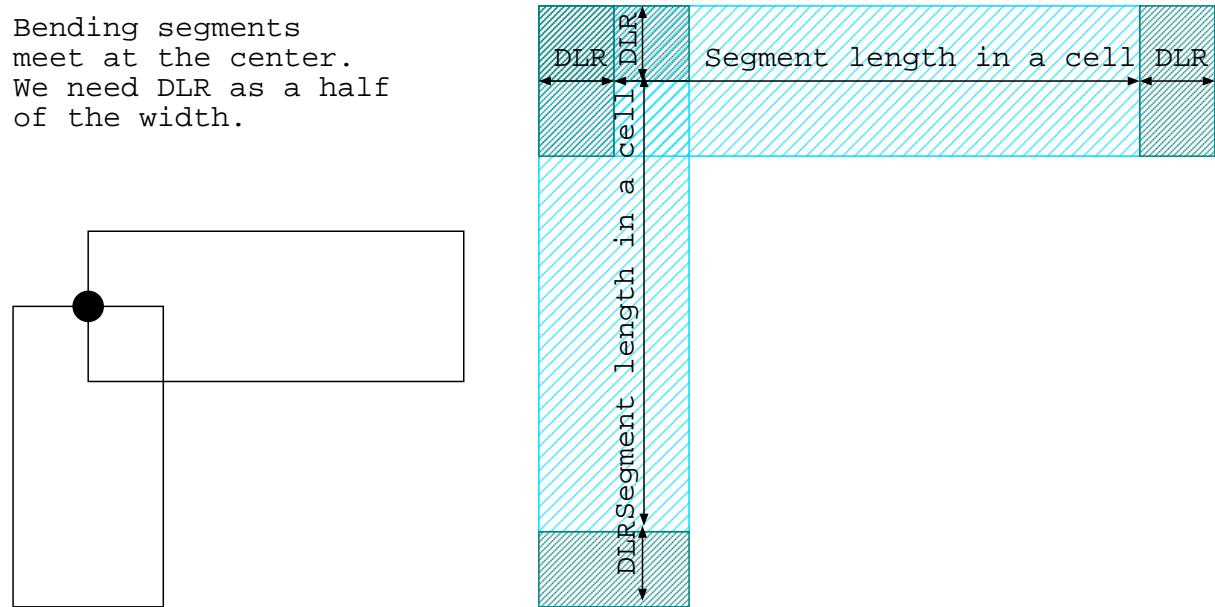


Figure 1: An example of the segment transformation on a bending segment

The figure 2 shows that the typical problem of Sxlib on the adaptation to fine processes. The diffusion area is conductive. And Sxlib treat it as a wire. But on finner processes, the gap between transistor and diffusion area can be greater than Sxlib expected. That makes Sxlib pseudo lambda much greater than one expected in real lambda. For example, my Rohm 0.18 micron technology request 0.27 micron lambda makes over 2 times larger area for each cell. To avoid the problem, nsxlib try to reduce the diffusion steps.

<sup>1</sup>[https://www.egr.msu.edu/classes/ece-410/demlow/files/DRC\\_rule\\_scmos.pdf](https://www.egr.msu.edu/classes/ece-410/demlow/files/DRC_rule_scmos.pdf)

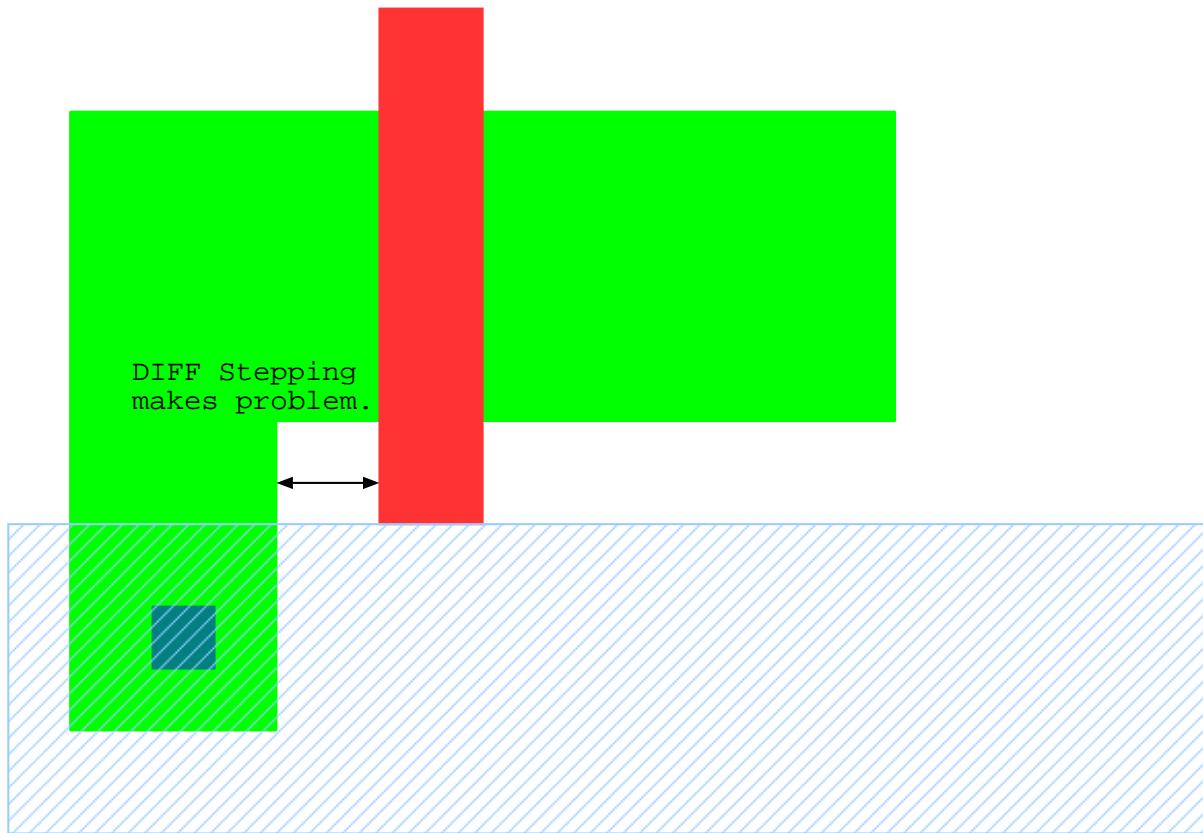


Figure 2: An example of the DIFF stepping in sxlib

## 1.2 The scalable cell library nsxlib

For adapting sxlib to MOSIS SCMOS or various other fabrication processes is a little difficult and I rewrite the sxlib to use the SCOMS rules for virtual lambda rules on the design as nsxlib.

I follow the following steps.

1. Translate the sxlib with a script to double the lambda in the cell.
2. Wrote DRC database against MOSIS SCMOS DEEP for 0.18 micron rules. (Lambda equals 0.09 micron)
3. Check all the cells on DRC and modify one by one whenever required
4. Adapt the library against Phenitec 0.6 micron rules. Adjust the cells again.
5. Adapt the library against Hibikino Lab 2.0 micron rules. Adjust the cells to meet all the rules.
6. Adapt the library against FreePDK45 45 nano meter rules. Adjust the cells to meet all the rules.
7. For the 0.18 micron rules, we have the SPICE parameter against TSMC CL018. We extract SPICE net list with cougar and transform it to the VHDL with yagle. Then we check all the cells with proof for formal verification.

The figure 3 shows the design flow of the nsxlib. We used many Alliance tools for verification of each cells.

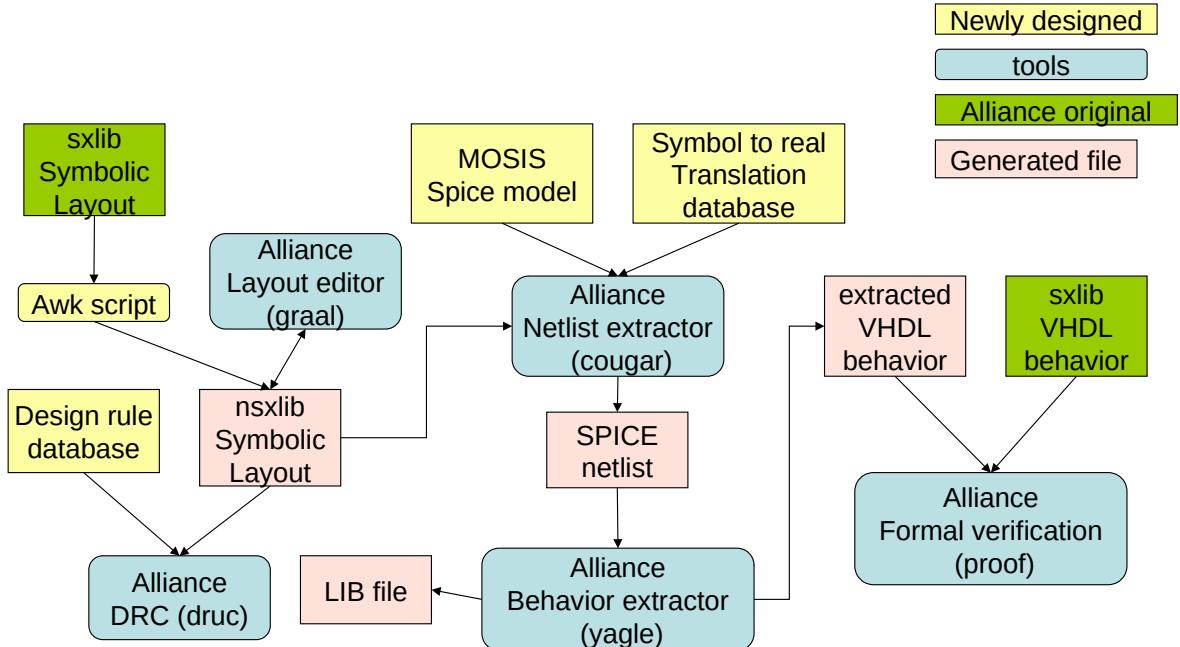


Figure 3: NSXLIB design flow with Alliance tools

### 1.3 VLSI making with NSXLIB: Phenitec 0.6 micron shuttle

#### 1.3.1 Phenitec Chips 2017: Q172TKD

At the first slot of Phenitec shuttle in 2017, I confirmed the operation of basic cells in nsxlib. Then the second slot of their shuttle in 2017, I tried to make a CPU for my lecture<sup>2</sup>. And a ring buffer. I made also the IO circuits with Alliance tools.

- I wrote my CPU with NSL<sup>3</sup>, then convert it to Alliance compatible VHDL with nsl2vh compiler.
- Place and Route with Alliance 5.0, nero and ocp.
- Put the IO circuits and the CPU, a ring oscillator manually.
- Merge the frame data from Phenitec with the GDS from Alliance.
- submit the data to Phenitec
- They confirmed that all the layout was compatible to their own rules checked by Caribre.

<sup>2</sup><https://www.slideshare.net/NaohikoShimizu/computer-design-and-architecture-with-simple-cpu>

<sup>3</sup><https://www.ip-arch.jp/indexe.html>

## Klayout merge

Phenitec provides a special frame GDS data. And we have to use the frame to submit for their shuttle. Unfortunately, Alliance could not read their GDS, I used Klayout to merge the GDS from Phenitec against GDS from Alliance.

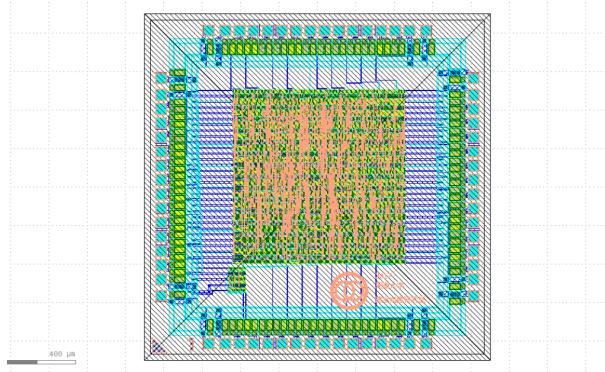


Figure 4: Merging the frame data from Phenitec against GDS from Alliance

## Testing the functionality of the CPU

I use FPGA to evaluate the functionality of the CPU. For the first trial, I feed clock signal with switches on the board. The CPU has many pins as shown in Table 1, and I connected them with cables as shown in Figure 5.

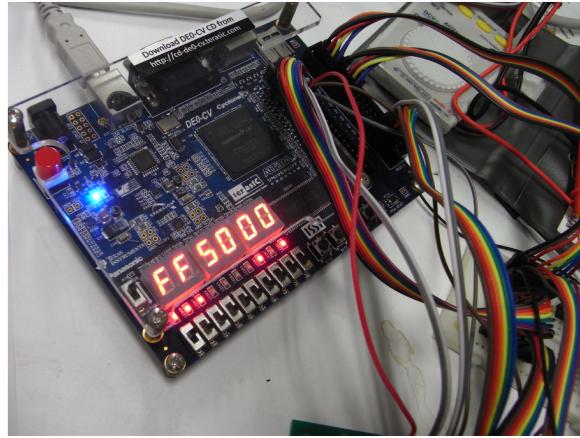


Figure 5: Testing the CPU with an FPGA

Unfortunately, the CPU worked only partially. The testing steps are following.

1. set power on reset assert then toggle the clock

Table 1: The cpu signals for IO

name	num.	dir	function
m_clock	1	IN	master clock
p_reset	1	IN	power on reset
start	1	IN	start cpu
dati	8	IN	data input
dato	8	OUT	data output
adr	8	OUT	address output
mr	1	OUT	memory read request
mw	1	OUT	memory write request
stgi	1	OUT	instruction fetch stage
stgd	1	OUT	instruction decode stage
stgx	1	OUT	instruction execution stage
stgm	1	OUT	instruction memory stage
stgh	1	OUT	instruction halt stage

2. set power on reset negate, then toggle the clock
3. set start to 1, toggle the clock. We confirmed the instruction stage active
4. set start to 0, feed instruction pattern to the dati input, toggle the clock.
5. The stage did not advance to the decode.

The IO circuits and some part of the CPU works. But it does not seem to advance the instruction stages. We are not sure the reason, but we are suspicious that the hold time violation might be occurred on the staging flip flops.

### Ring Oscillator

We put 32 inverters and a nand gate to make a ring oscillator. It works great without problem. Figure 6 shows the output of the ring oscillator.

We evaluated various power line voltages on the oscillator. The Table 2 shows the results.

Table 2: Ring Oscillator performance against power voltage

Power (V)	Freq (MHz)	Delay/inv (pS)
5.0	81.2	373
4.5	74.8	405
4.0	67.0	452
3.5	58.6	517
3.0	49.8	608
2.5	37.5	808
0.0	24.5	1237



Figure 6: Waveform captured with Tektronics Oscilloscope

### 1.3.2 Phenitec Chips 2020

In year 2020, we made another chip with Phenitec. Because we thought the chip in 2017 was failed on hold time violation, we tried to make a clock tree with Coriolis. At this time, Coriolis does not support wiring to the IO circuits. Then I made the GDS for the core and manually wire the rest.

Chip came to my lab, but unfortunately, university closed because of COVID-19. After 3 years, there is no student who is interested in VLSI. Then the evaluation is hold until now.

Figure 7 shows the chip photo. This chip integrate SN/X 16 bit CPU with a ring oscillator. It has many IO pins for input, output, address and separate instruction data. Then it is more hard to connect for FPGA manually.

## 1.4 The scalable cell library nsxlib v2.0

The first version of nsxlib is direct descendant of sxlib. We need many modifications to meet the various design rules. But the basic layout is the same.

On adapting various processes, it was a little difficult to adjust the RDS parameters. It may come from the center to center alignment of bending segments. If we have different width segments to connect, we will have improper figure on the real layouts.

The cell design in nsxlib v2.0 uses edge to edge alignment for bending segments. The figure 8 shows a example of the transformation of the lambda segments to the real layout.

Also we suppose, the shortage of well contact may induce some difficult instability. Also some of the layout in sxlib are not so clean.

The Figure 9 shows the current situation of the development. I am concentrates on modifying the cells and the evaluation step is intentionally delayed.

From these reasons, I am rewriting all the cells for v2.0. The layout detail will be shown in the next section. The modification step is as following.

1. Write a script to add well contacts on the layout. We will see the script in Figure 10. The script also modify the metal width, segments length.
2. Manually modify the cells, one by one. It is not completely finished, but it is at least DRC clean.

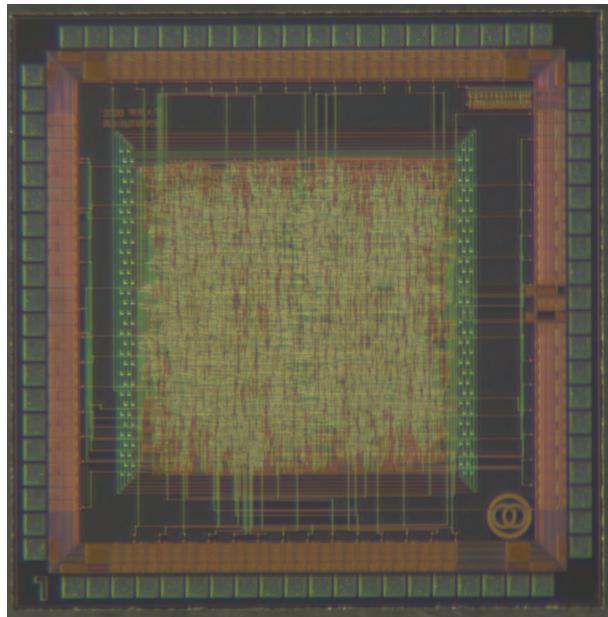


Figure 7: Phenitec 2020 shuttle chip. It integrate SNX 16 bit CPU with a ring oscillator

Bending segments  
meet at edge.  
DLR must be zero

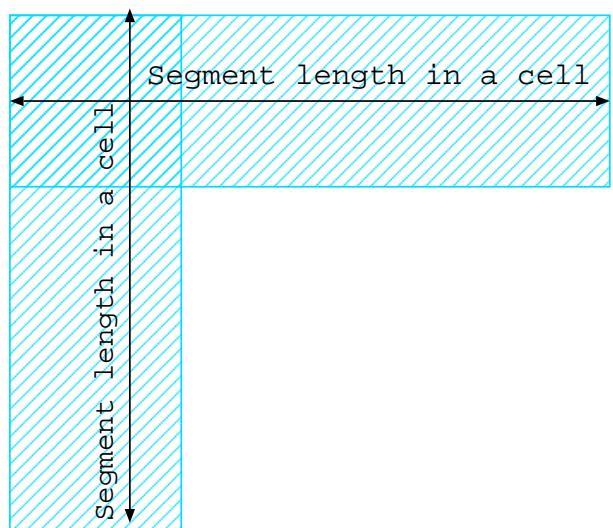
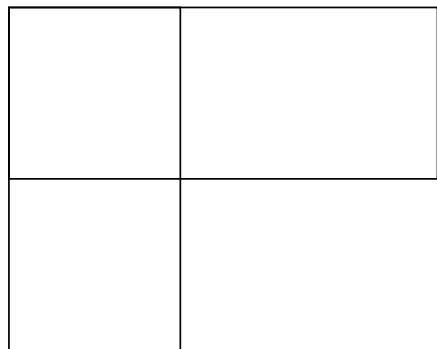


Figure 8: An example of the segment transformation on a bending segment in nsxlib v2.0

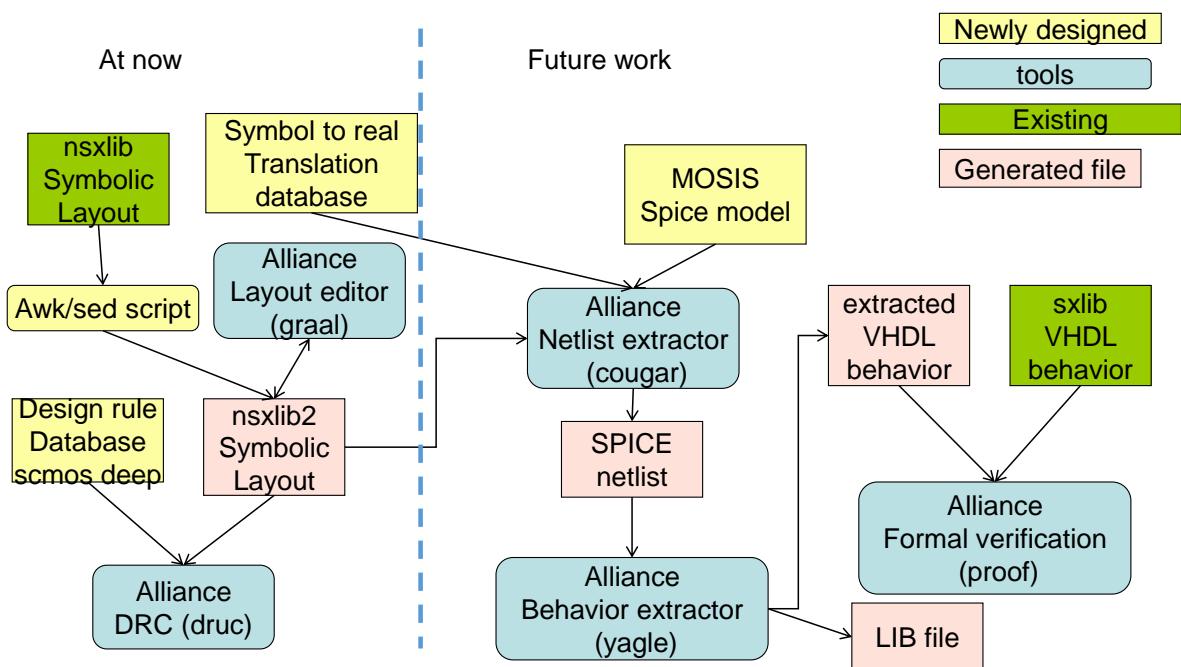


Figure 9: NSXLIB v2.0 design flow with Alliance tools

```

#!/bin/sh
if [ "x" = "$2x" ]; then
cp $MBK_TARGET_LIB/$1 ./ $1
fi
ABOX='awk 'BEGIN {FS=","}\n    /^A / {print $3};' $1'
echo 1
sed -i '/WELL/{s/ -300,/ -500,/g; s/7800/7300/g; s/6000/6400/g}' $1
awk -i inplace 'BEGIN {FS=",";OFS=","}\n    /NWELL/ { $3=int($3/1000)*1000 + 500; }\n    {print $0}', $1
awk -i inplace 'BEGIN {FS=",";OFS=","}\n    /vss/ { $1="S -200"; $2=500; $4=500; $3=int($3/1000)*1000 + 200; $5=1400}\n    /vdd/ { $1="S -200"; $2=9500; $4=9500; $3=int($3/1000)*1000 + 200; $5=1400}\n    {print $0}', $1
echo 2
sed -i '/ALU/s/,300,/ ,400,/g' $1
echo 3
sed -i '/WELL/{h; p; s/NWELL/NTIE/g; s/-500/-200/; s/7300/10000/g; s/6400/400/g; }' $1
echo 4
sed -i '/NTIE/{h; p; s/NTIE/PTIE/g; s/10000/0/g; }' $1
awk -i inplace 'BEGIN {FS=",";OFS=","}\n    /TIE/ { $3=int($3/1000)*1000 + 200; }\n    {print $0}', $1
echo 5
i=0
while [ $i -le $ABOX ]
do
    echo $i $ABOX
    sed -i '/EOF/iV '$i',0 ,CONT_BODY_P,* \
V '$i',10000 ,CONT_BODY_N,* '$1
    i=$(( $i + 1000 ))
done
echo 6
sed -i '/PTRAN/s/9500/9400/g' $1
sed -i '/PDIF/s/9300/9400/g' $1
echo 7

awk -i inplace 'BEGIN {FS=",";OFS=","}\n    function sign(a,b,c,d) {\n        if(a>b) return -c;\n        return c\n    }\n    /ALU1/ && $5==400 && ($7 == "UP" || $7 == "DOWN") { s=sign($2,$4,300,$7); $2=$2-s; $4=$4+s; }\n    /ALU1/ && $5==400 && ($7 == "RIGHT" || $7 == "LEFT") \
    { s=sign(substr($1,3),$3,300,$7); $1="S "(substr($1,3)-s); $3=$3+s; }\n    /POLY/ && ($7 == "UP" || $7 == "DOWN") { s=sign($2,$4,100,$7); $2=$2-s; $4=$4+s; }\n    /POLY/ && ($7 == "RIGHT" || $7 == "LEFT") { s=sign($2,$4,100,$7); $1="S "(substr($1,3)-s); $3=$3+s; }\n    /DIF/ && $4!=9400 && ($7 == "UP" || $7 == "DOWN") { s=sign($2,$4,200,$7); $2=$2-s; $4=$4+s; }\n    /DIF/ && $4==9400 && ($7 == "UP" || $7 == "DOWN") { s=sign($2,$4,200,$7); $2=$2-s; }\n    {print $0}', $1

```

Figure 10: First trial of automatic insertion of well contacts

## 2 Basic Layout for the nsxlib v2.0

The nsxlib follow the MOSIS SCMOS DEEP design rules v8.0. Also we will use the same routing grid as the sxlib on Alliance. Total cell height is  $100\lambda$ . Every cell has NTIE and PTIE on the layout to the well potential can be stable.

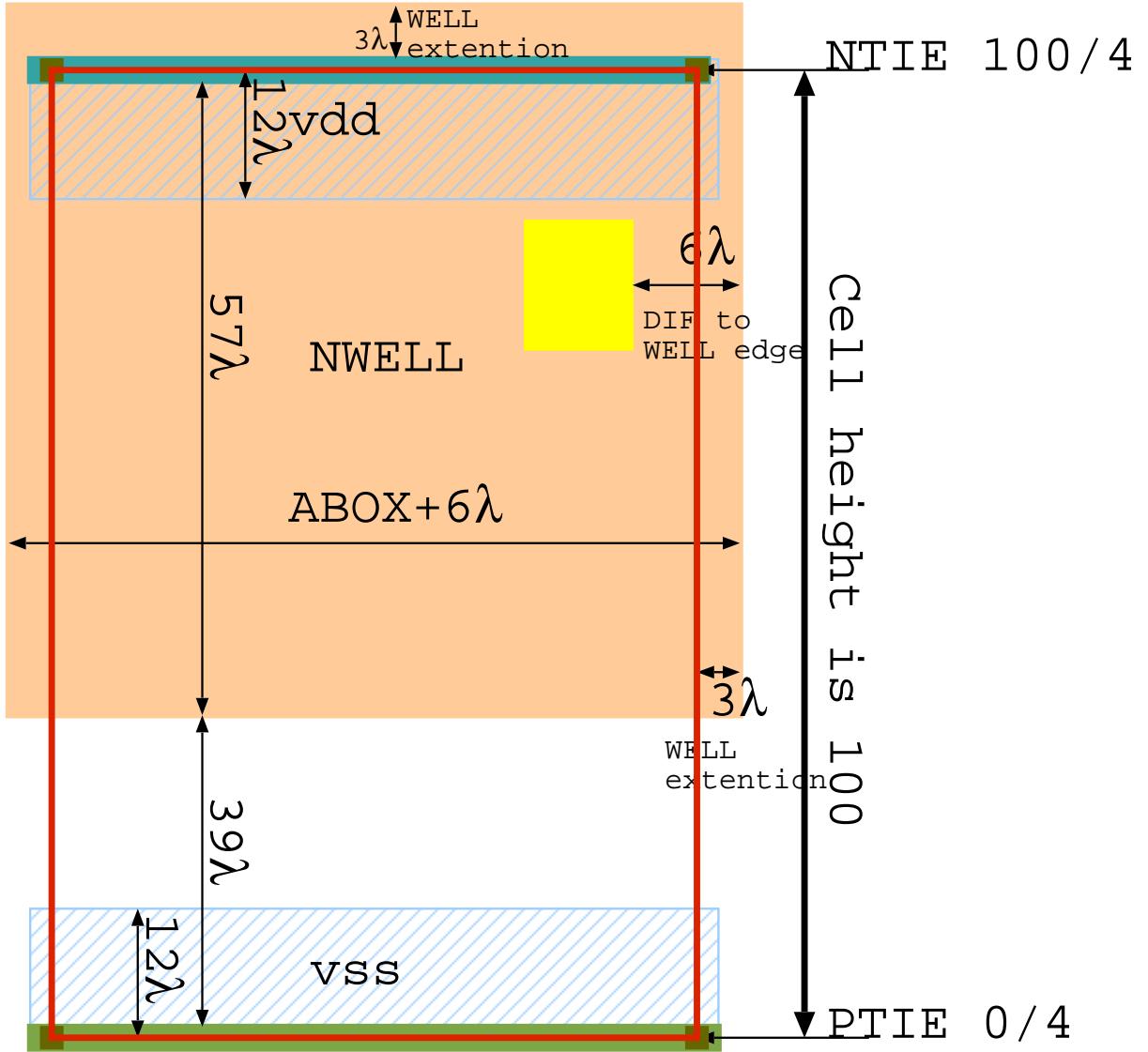


Figure 11: The basic layout strategy on Nsxlib v2.0

- NWEL has extension 3 lambda on both side of abox. It has extension 5 lambda on upper and lower side of abox.

This is because, active area must be apart 6 lambda each. The adjacent cells can be shared the space between them. Then we can place the active to 3 lambda from abox. It may break the design rules if we check each cell separately. So we extend the WELL 3 lambda to check individual cell

for design rules.

- PTIE locate at 0 width 4. WELL edge to tie active must apart 3 lambda. Then NWEL extension is 3 lambda down than the PTIE.
- NTIE locate at 100 width 4. WELL edge to tie active must apart 3 lambda. Then NWEL extension is 3 lambda upper than the NTIE.
- ALU1 Minimum width required is 3, but we use 4 lambda for wiring to cover VIA/CONT.
- POLY Minimum width is 2 lambda.

The previous nsxlib was direct descendant of the sxlib. There are some obscure decisions on the routing or placing of segments. I want to resolve these points, but it takes long time and careful observation will be required. At this time, I does not touch much of them, and just check the DRC violation for most of the cells. It is still under the consideration that we should extend the diffusion area on the power metal for placing the vias of power or not. Currently, I respect the layout of sxlib, but it may have to change.

## 2.1 Comparison between Sxlib, Nsxlib versus Nsxlib v2.0

In this section, we will see the comparison between these libraries. For the comparison, I selected 2 input nand gates. The Figure 12 shows the layout of these three libraries.

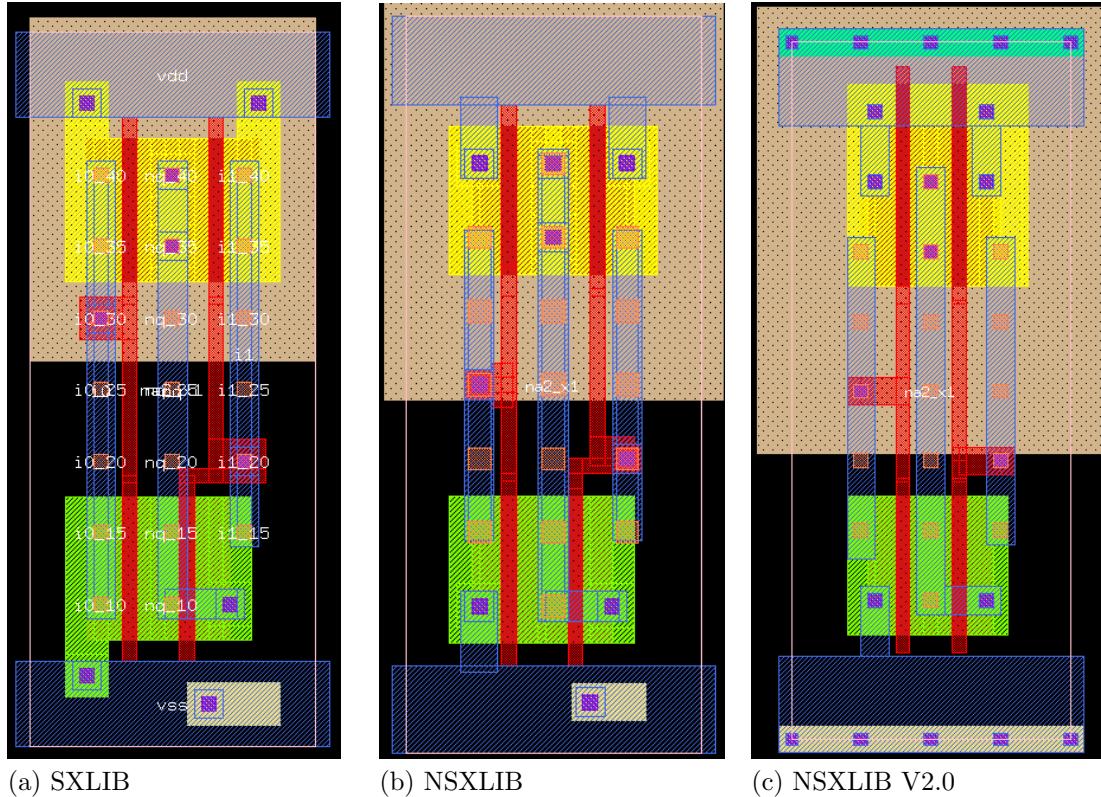
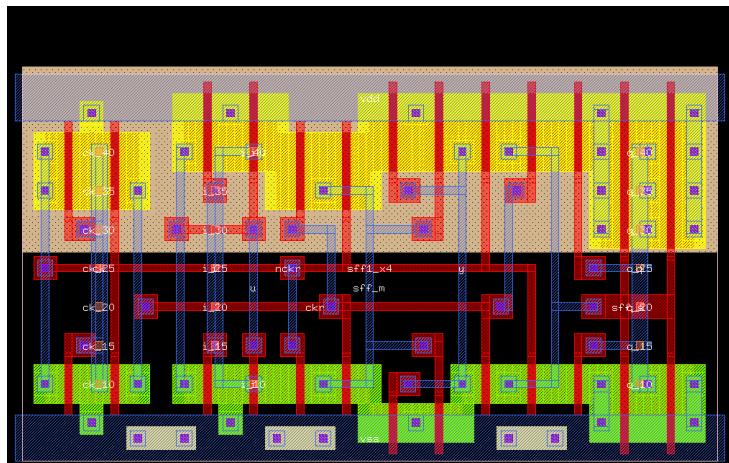


Figure 12: The comparison between Sxlib, Nsxlib versus Nsxlib v2.0

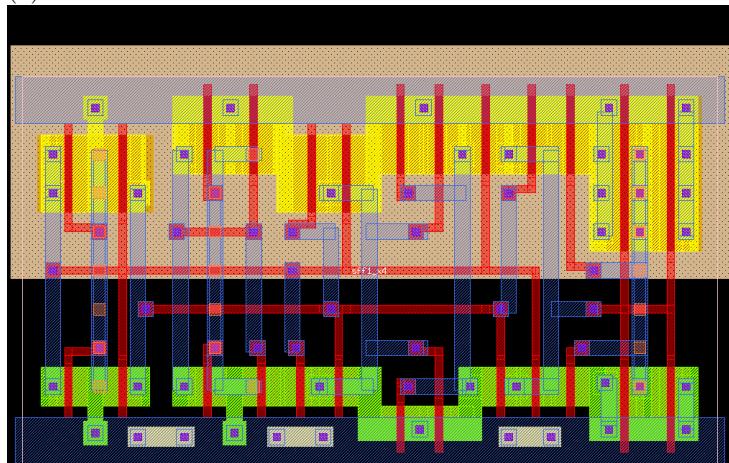
As shown in the figure, we can notice that sxlib uses diffusion step to feed the power to diffusion area. The nsxlib and v2.0 eliminated the diffusion step. Instead, we used metal line to feed the power on diffusion area. The nsxlib v2.0 refine the design of the cell to narrow the distance between diffusion contact to the transistor based on the MOSIS rules. It may increase the driving performance of the cell.

We can see explicitly placed body contact diffusion area on nsxlib v2.0. The sxlib and nsxlib does not have regular body contact diffusion on each cell.

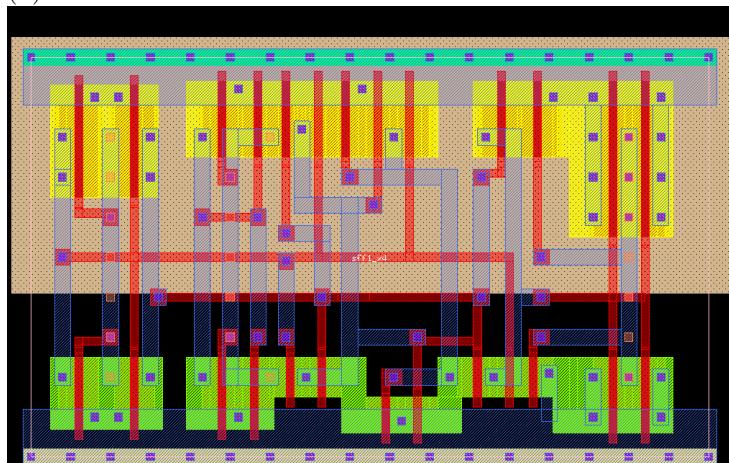
We will see more large cells. In this case, I have not optimized the layout yet. I did mechanically convert the nsxlib cell to v2.0. After then, I slightly modified to reduce the diffusion stepping.



(a) SXLIB



(b) NSXLIB



(c) NSXLIB V2.0

Figure 13: The comparison between Sxlib, Nsxlib versus Nsxlib v2.0 with Flip Flop cell

### **3 Future plan**

The nsxlib v2.0 is on the way. We need verification as previous nsxlib. Also we have to examine individual cells for the performance and usability.

I modified Alliance to support more transistor model. Now, RDS system on Alliance introduce 3 transistor model for PMOS and NMOS as normal, HVIO and FAST. But we may need more transistor models for current technologies.

RDS conversion table is based on micron, but if we can introduce lambda based table it may help us a lot. For example, we need to write DLR for 0.18 microns as 0.09, but DLR for 0.045 microns as 0.0225, respectively. If we can write them as 1.0L, in both RDS table and DRC rules, it will help us a lot.

I want to write a script which automatically generate RDS table when a lambda defined. The needs will be decreased if previous lambda based notation is acceptable. But still differences between the design rules in certain processes are large and it is hard to describe design rule definition tables. One because, the description of design rule are very different between foundry services.

## **4 Individual cells**

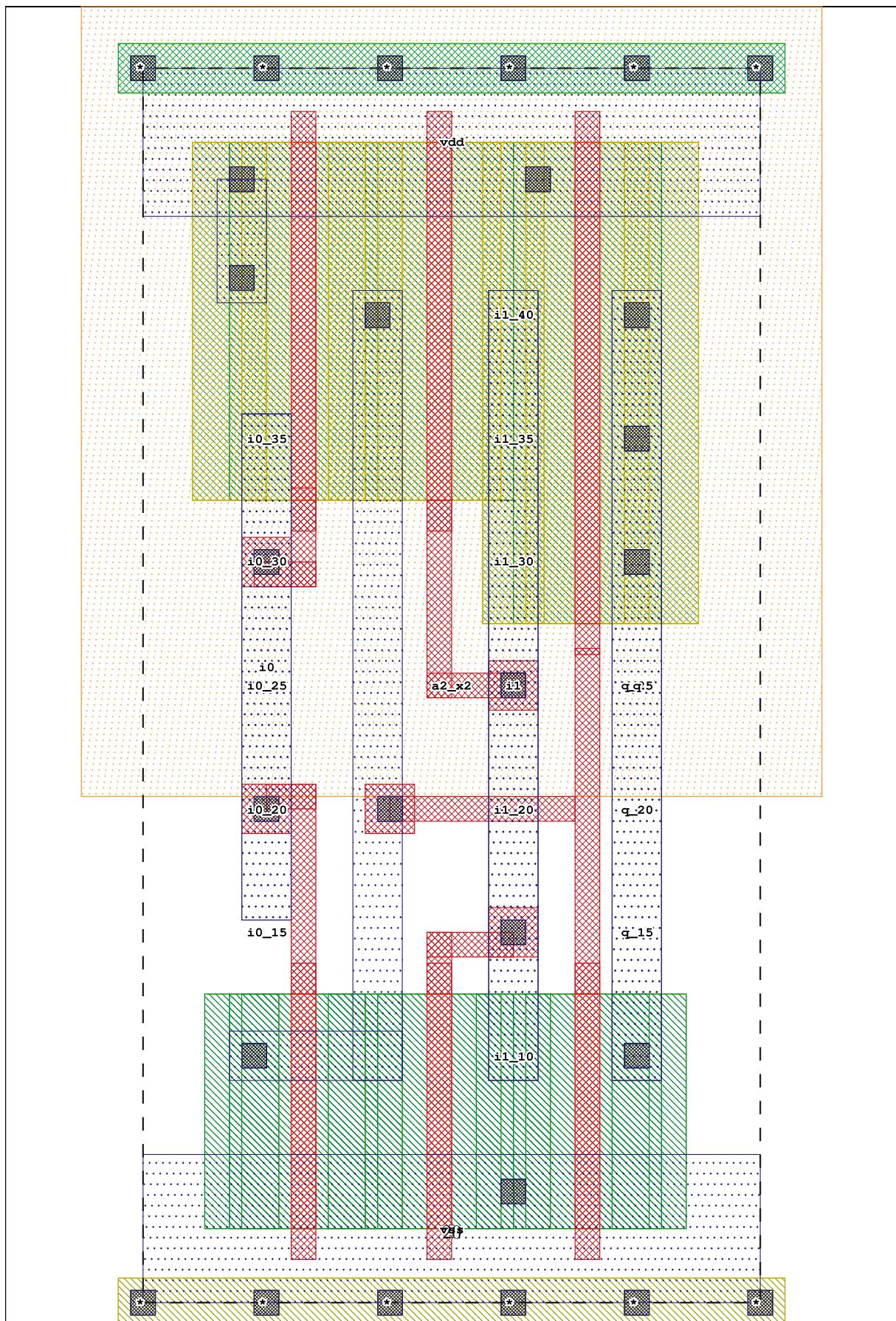
In this section, we will see the cells in nsxlib. We will show the cell behavior VHDL and layout.

#### 4.1 a2\_x2

```
ENTITY a2_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1250;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT tphh_i1_q      : NATURAL := 203;
    CONSTANT tphh_i0_q      : NATURAL := 261;
    CONSTANT tp11_i0_q       : NATURAL := 388;
    CONSTANT tp11_i1_q       : NATURAL := 434;
    CONSTANT transistors    : NATURAL := 6
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END a2_x2;

ARCHITECTURE behaviour_data_flow OF a2_x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on a2_x2"
  SEVERITY WARNING;
  q <= (i0 and i1) after 1000 ps;
END;
```

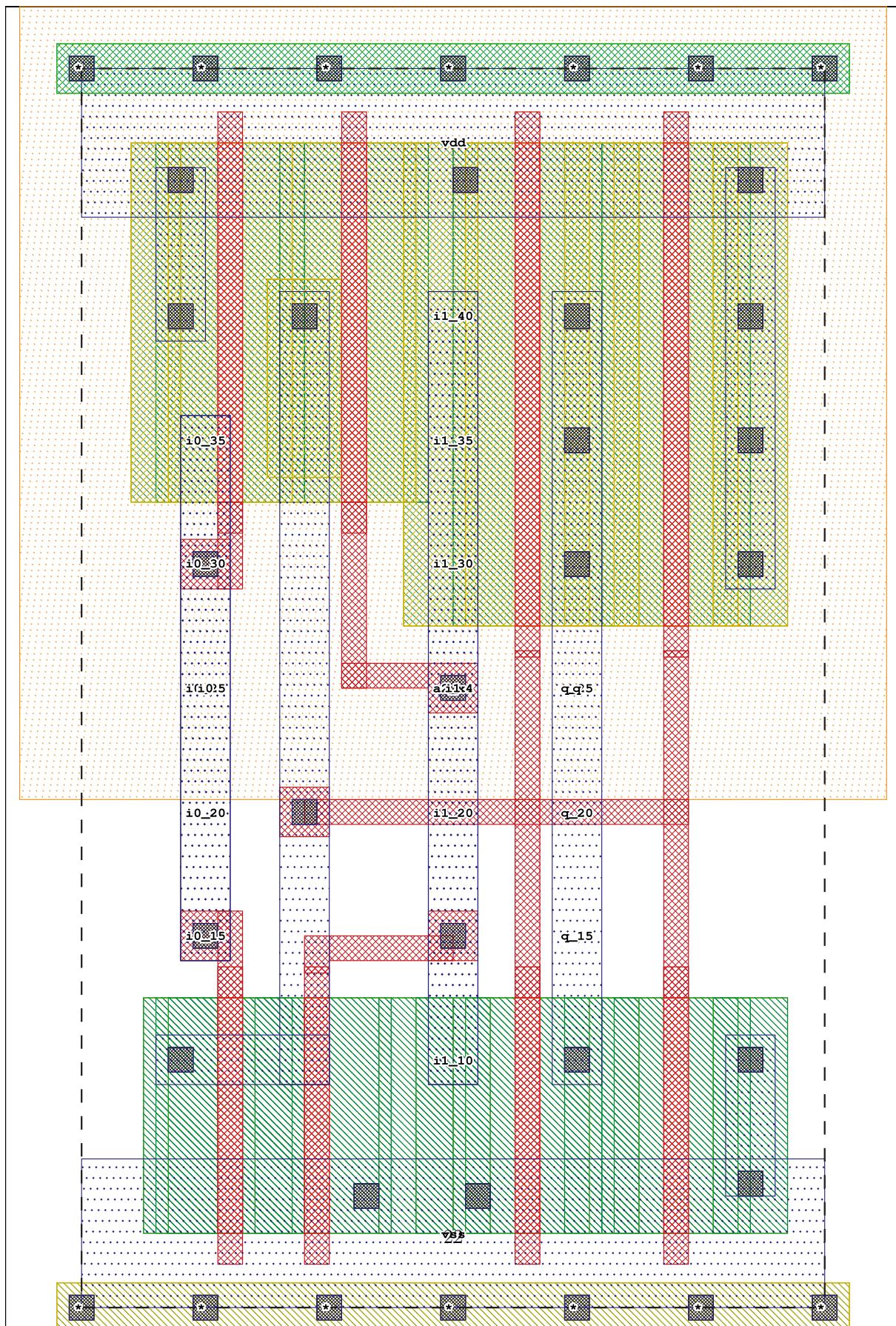


## 4.2 a2\_x4

```
ENTITY a2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT tphh_i1_q      : NATURAL := 269;
    CONSTANT tphh_i0_q      : NATURAL := 338;
    CONSTANT tp1l_i0_q       : NATURAL := 476;
    CONSTANT tp1l_i1_q       : NATURAL := 518;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END a2_x4;

ARCHITECTURE behaviour_data_flow OF a2_x4 IS

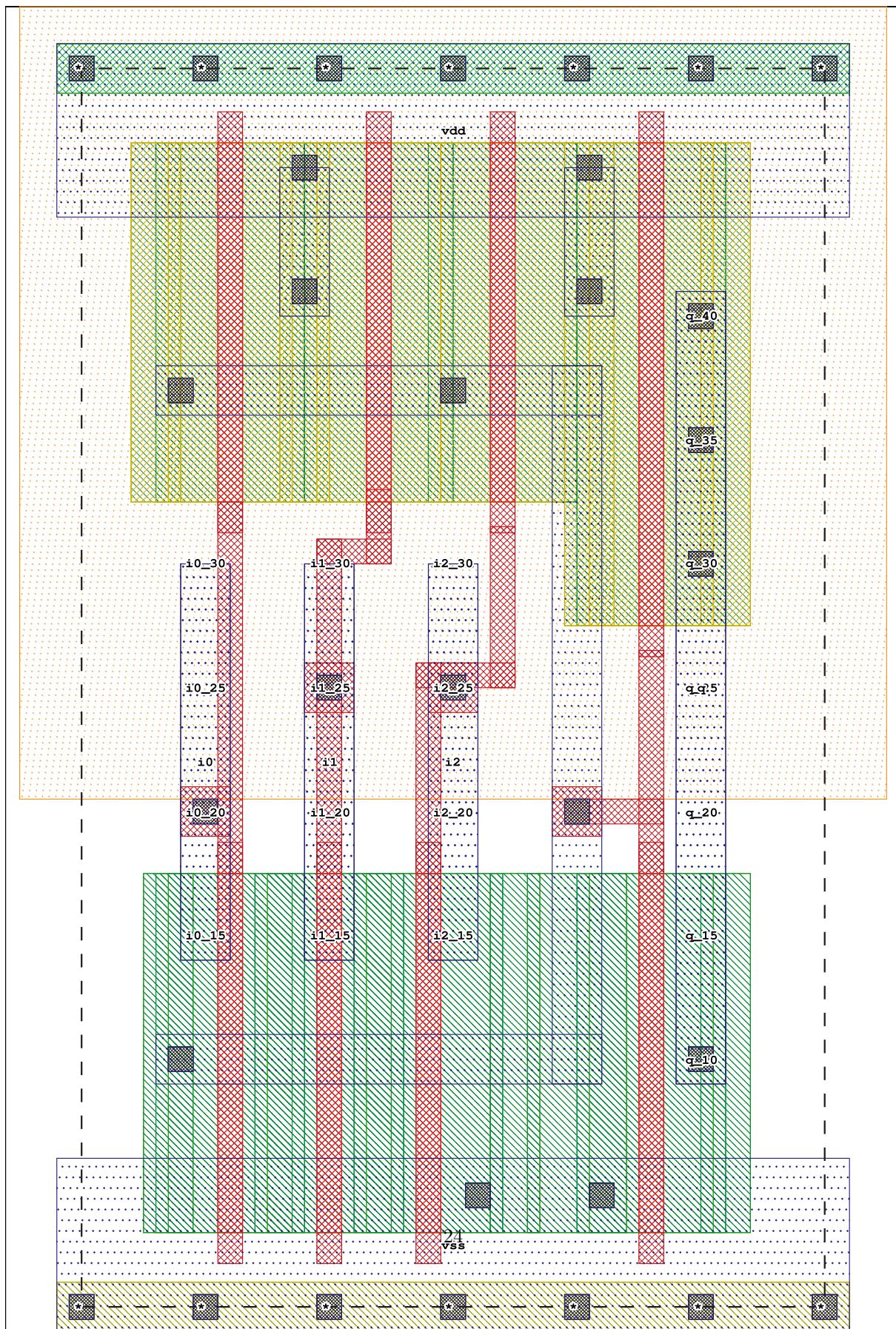
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on a2_x4"
  SEVERITY WARNING;
  q <= (i0 and i1) after 1100 ps;
END;
```



### 4.3 a3\_x2

```
ENTITY a3_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT cin_i2         : NATURAL := 10;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT tphh_i2_q      : NATURAL := 290;
    CONSTANT tphh_i1_q      : NATURAL := 353;
    CONSTANT tphh_i0_q      : NATURAL := 395;
    CONSTANT tp1l_i0_q       : NATURAL := 435;
    CONSTANT tp1l_i1_q       : NATURAL := 479;
    CONSTANT tp1l_i2_q       : NATURAL := 521;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END a3_x2;
```

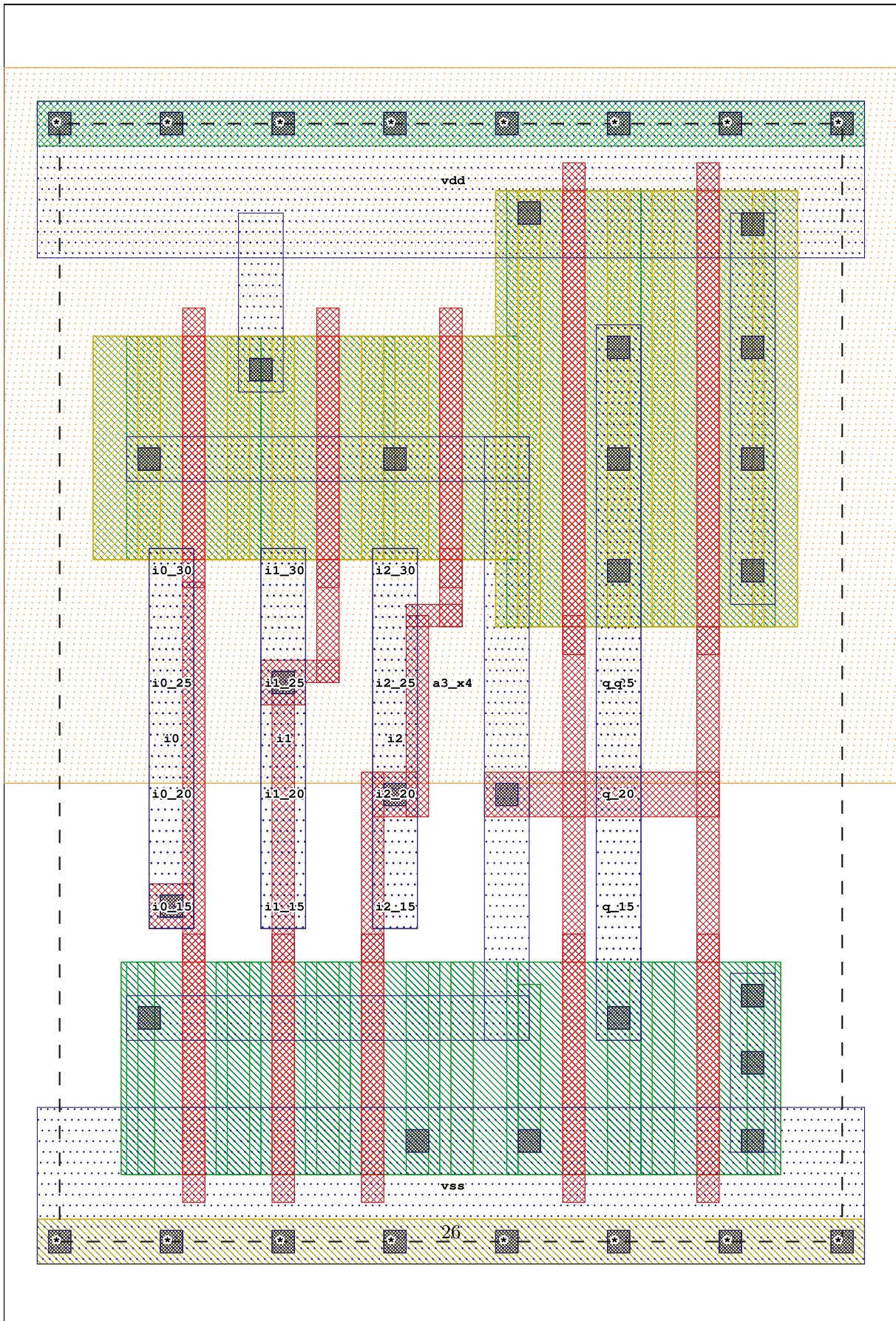
```
ARCHITECTURE behaviour_data_flow OF a3_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on a3_x2"
  SEVERITY WARNING;
  q <= ((i0 and i1) and i2) after 1100 ps;
END;
```



#### 4.4 a3\_x4

```
ENTITY a3_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT cin_i2         : NATURAL := 11;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT tphh_i2_q      : NATURAL := 356;
    CONSTANT tphh_i1_q      : NATURAL := 428;
    CONSTANT tphh_i0_q      : NATURAL := 478;
    CONSTANT tp1l_i0_q       : NATURAL := 514;
    CONSTANT tp1l_i1_q       : NATURAL := 554;
    CONSTANT tp1l_i2_q       : NATURAL := 592;
    CONSTANT transistors    : NATURAL := 10
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END a3_x4;
```

```
ARCHITECTURE behaviour_data_flow OF a3_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on a3_x4"
  SEVERITY WARNING;
  q <= ((i0 and i1) and i2) after 1200 ps;
END;
```



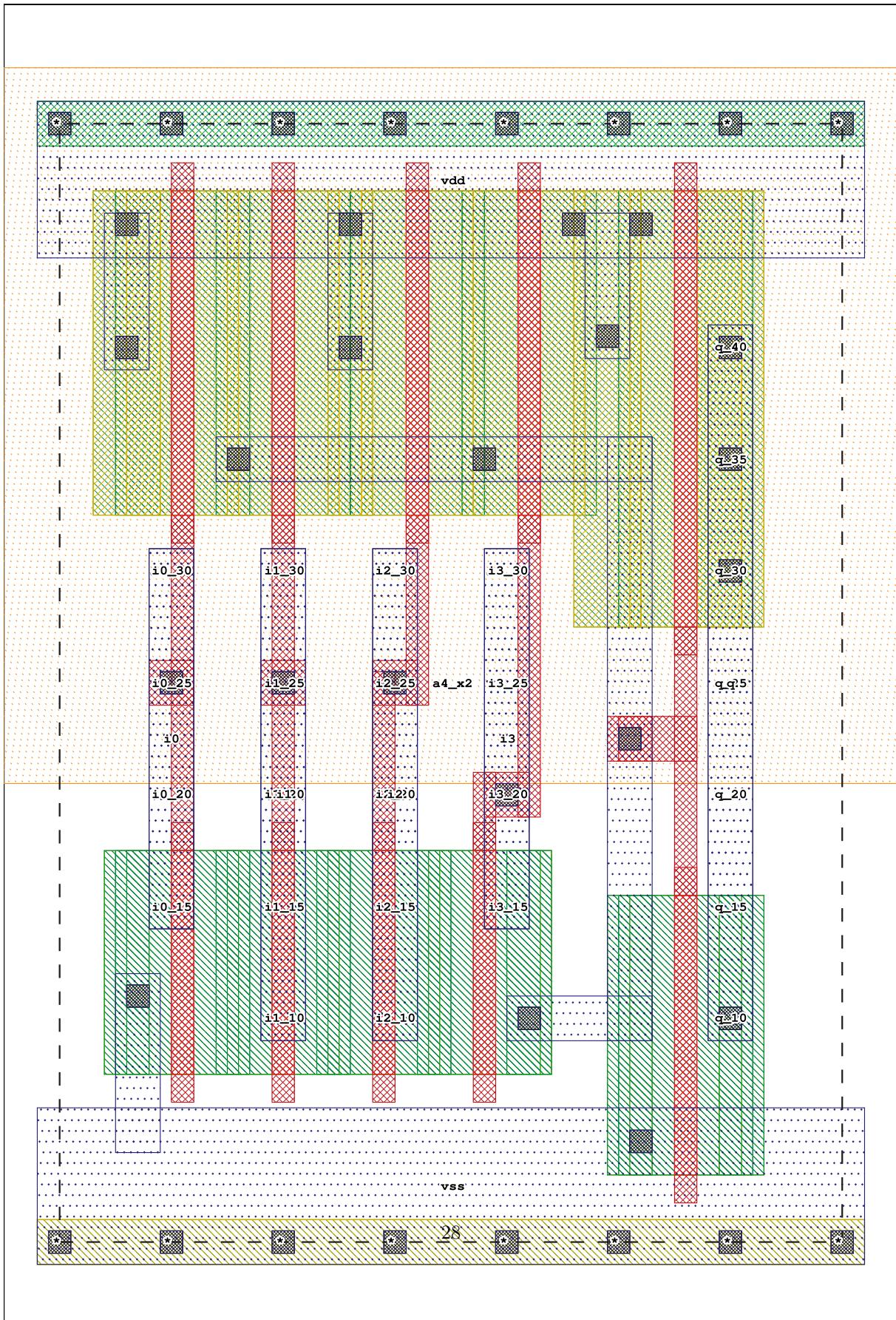
## 4.5 a4\_x2

```

ENTITY a4_x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT cin_i2         : NATURAL := 11;
    CONSTANT cin_i3         : NATURAL := 10;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rdown_i3_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT rup_i3_q       : NATURAL := 1790;
    CONSTANT tphh_i0_q      : NATURAL := 374;
    CONSTANT tphh_i1_q      : NATURAL := 441;
    CONSTANT tp11_i3_q      : NATURAL := 455;
    CONSTANT tp11_i2_q      : NATURAL := 482;
    CONSTANT tp11_i2_q      : NATURAL := 498;
    CONSTANT tp11_i3_q      : NATURAL := 506;
    CONSTANT tp11_i1_q      : NATURAL := 539;
    CONSTANT tp11_i0_q      : NATURAL := 578;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END a4_x2;

ARCHITECTURE behaviour_data_flow OF a4_x2 IS
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on a4_x2"
        SEVERITY WARNING;
    q <= (((i0 and i1) and i2) and i3) after 1200 ps;
END;

```



## 4.6 a4\_x4

```

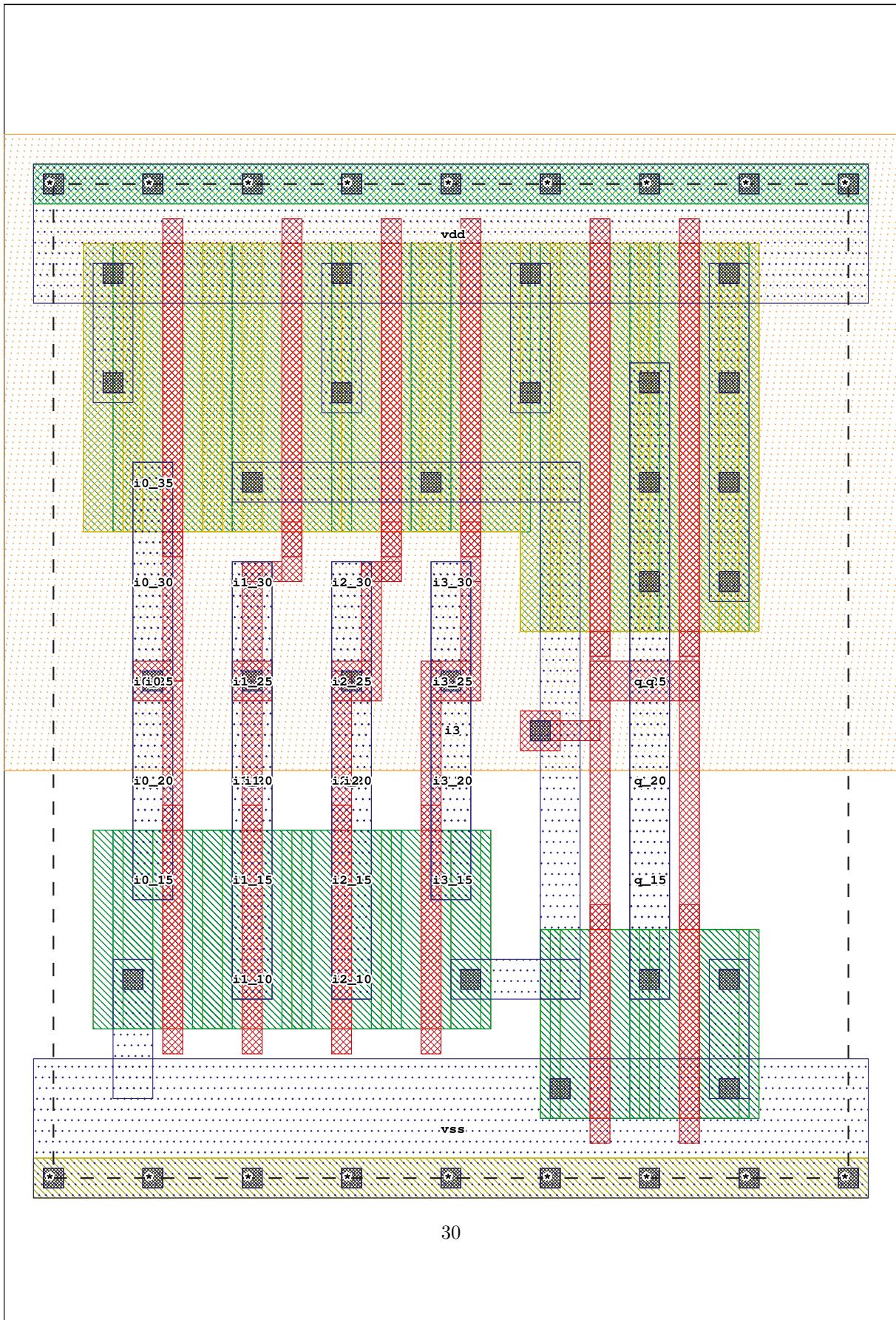
ENTITY a4_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT cin_i2         : NATURAL := 11;
    CONSTANT cin_i3         : NATURAL := 10;
    CONSTANT rdown_i0_q     : NATURAL := 540;
    CONSTANT rdown_i1_q     : NATURAL := 540;
    CONSTANT rdown_i2_q     : NATURAL := 540;
    CONSTANT rdown_i3_q     : NATURAL := 540;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT tphh_i0_q      : NATURAL := 505;
    CONSTANT tp11_i3_q      : NATURAL := 538;
    CONSTANT tp11_i2_q      : NATURAL := 576;
    CONSTANT tp11_i1_q      : NATURAL := 578;
    CONSTANT tp11_i1_q      : NATURAL := 614;
    CONSTANT tp11_i2_q      : NATURAL := 627;
    CONSTANT tp11_i0_q      : NATURAL := 650;
    CONSTANT tp11_i3_q      : NATURAL := 661;
    CONSTANT transistors    : NATURAL := 13
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END a4_x4;

```

```

ARCHITECTURE behaviour_data_flow OF a4_x4 IS
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on a4_x4"
        SEVERITY WARNING;
    q <= (((i0 and i1) and i2) and i3) after 1300 ps;
END;

```

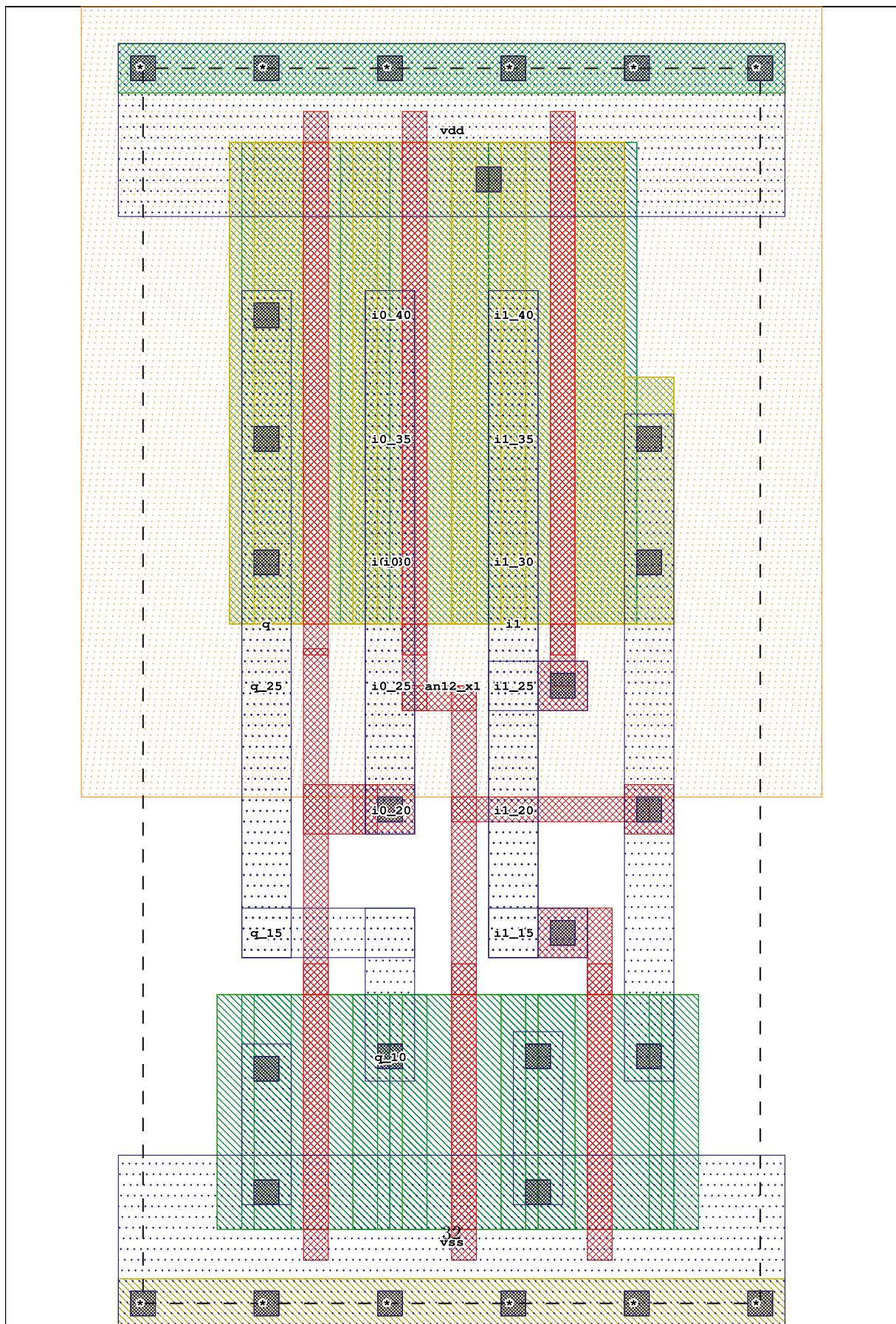


#### 4.7 an12\_x1

```
ENTITY an12_x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 1250;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 3640;
    CONSTANT rdown_i1_q     : NATURAL := 3640;
    CONSTANT rup_i0_q       : NATURAL := 3210;
    CONSTANT rup_i1_q       : NATURAL := 3210;
    CONSTANT tplh_i0_q      : NATURAL := 168;
    CONSTANT tphl_i0_q      : NATURAL := 200;
    CONSTANT tphh_i1_q      : NATURAL := 285;
    CONSTANT tp1l_i1_q      : NATURAL := 405;
    CONSTANT transistors    : NATURAL := 6
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END an12_x1;

ARCHITECTURE behaviour_data_flow OF an12_x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an12_x1"
    SEVERITY WARNING;
    q <= (not (i0) and i1) after 1000 ps;
END;
```

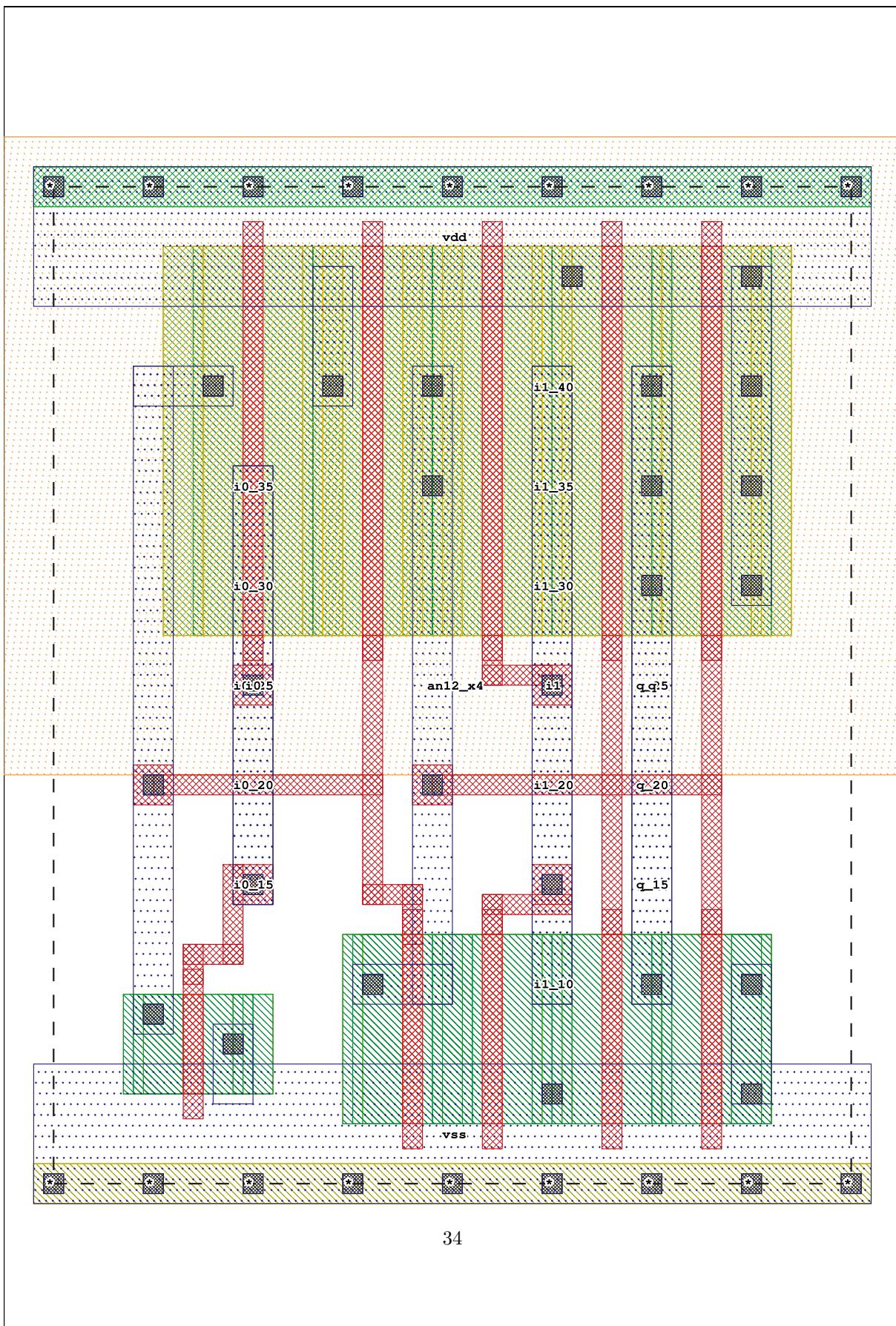


#### 4.8 an12\_x4

```
ENTITY an12_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT tphh_i1_q      : NATURAL := 269;
    CONSTANT tphl_i0_q      : NATURAL := 461;
    CONSTANT tphl_i0_q      : NATURAL := 471;
    CONSTANT tppll_i1_q     : NATURAL := 518;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END an12_x4;

ARCHITECTURE behaviour_data_flow OF an12_x4 IS

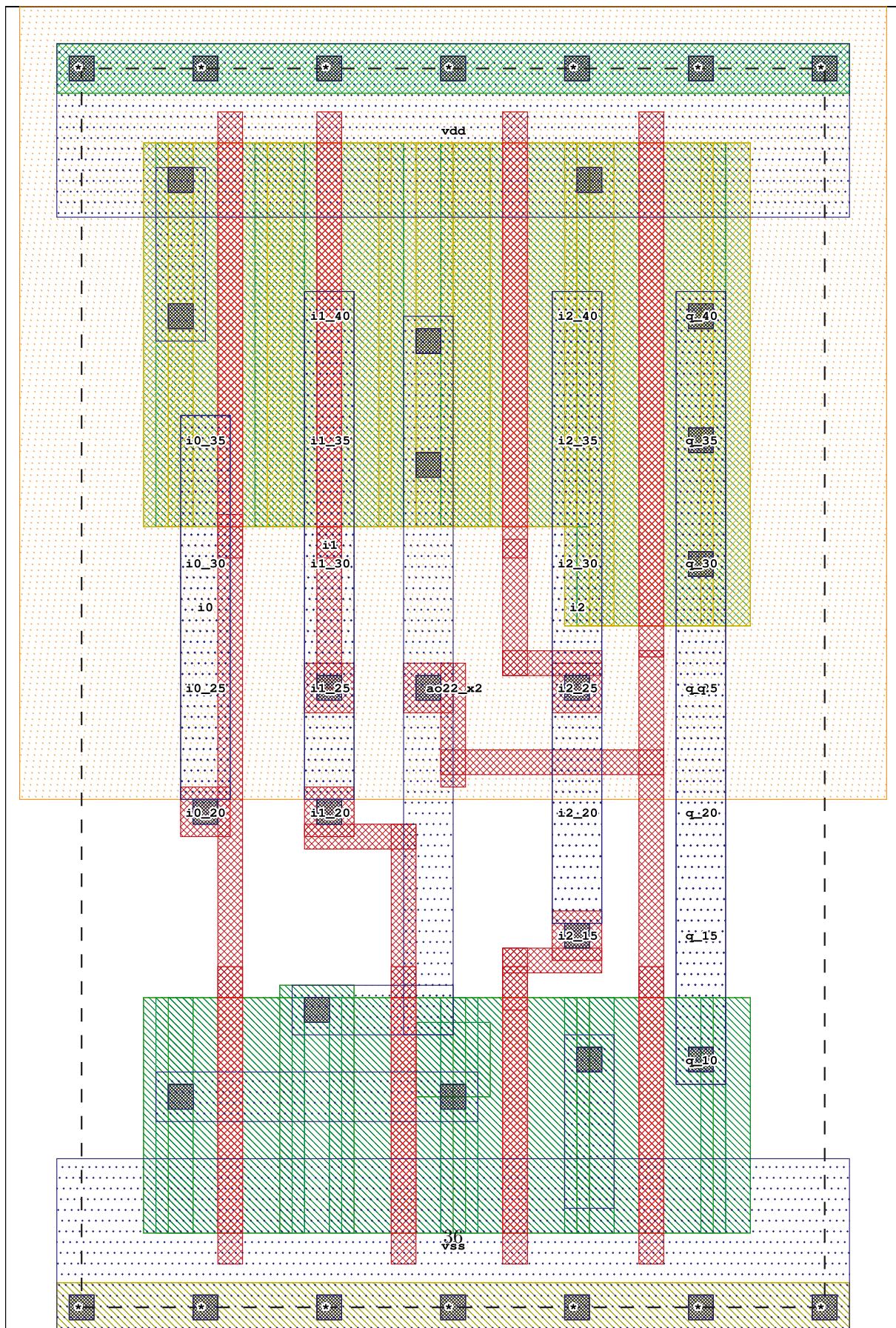
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on an12_x4"
    SEVERITY WARNING;
    q <= (not (i0) and i1) after 1100 ps;
END;
```



## 4.9 ao22\_x2

```
ENTITY ao22_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT tphh_i2_q      : NATURAL := 420;
    CONSTANT tp1l_i2_q      : NATURAL := 425;
    CONSTANT tp1l_i0_q      : NATURAL := 447;
    CONSTANT tp1h_i1_q      : NATURAL := 493;
    CONSTANT tp1l_i1_q      : NATURAL := 526;
    CONSTANT tp1h_i0_q      : NATURAL := 558;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END ao22_x2;
```

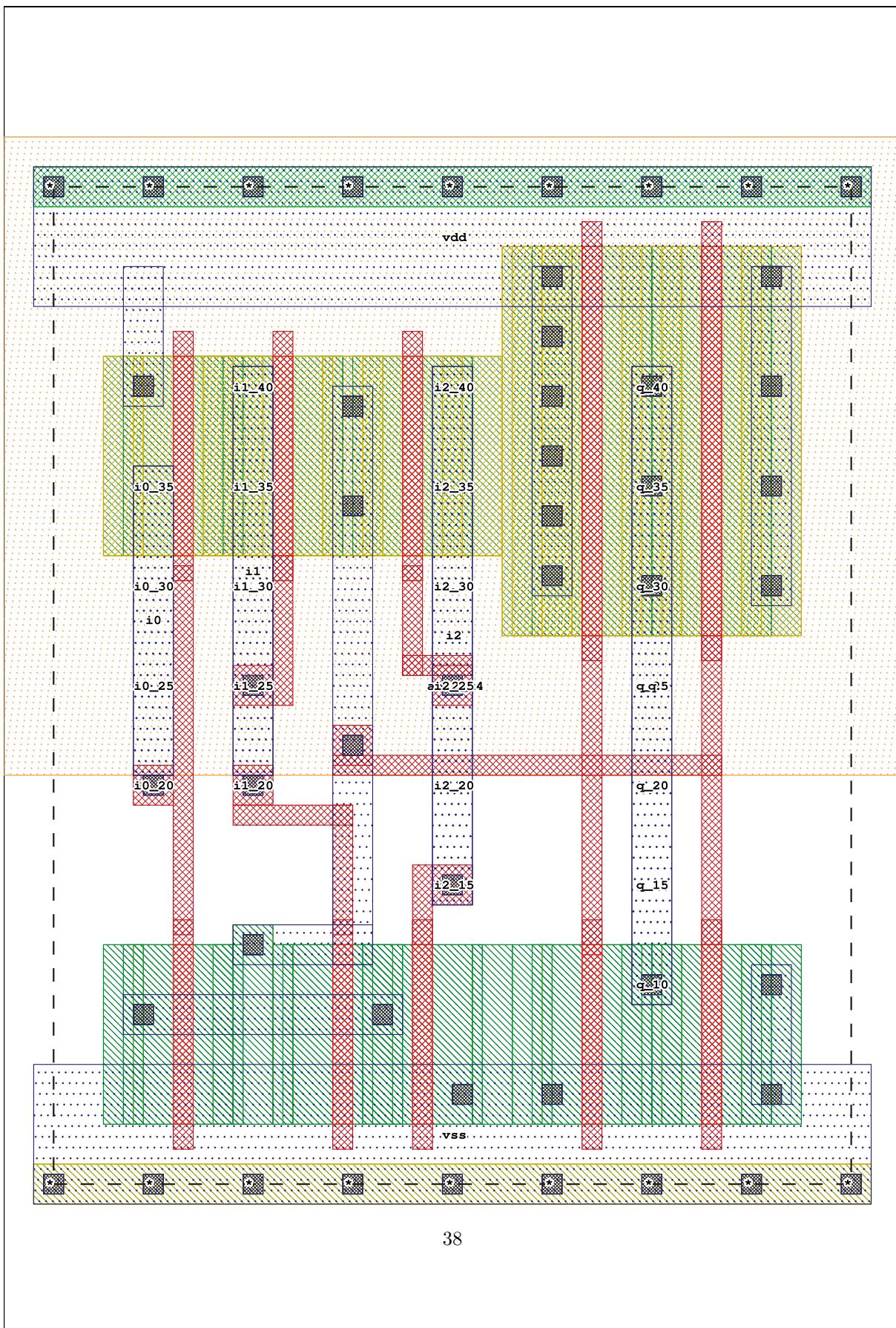
```
ARCHITECTURE behaviour_data_flow OF ao22_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on ao22_x2"
  SEVERITY WARNING;
  q <= ((i0 or i1) and i2) after 1200 ps;
END;
```



#### 4.10 ao22\_x4

```
ENTITY ao22_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT tpll_i2_q      : NATURAL := 505;
    CONSTANT tphh_i2_q      : NATURAL := 526;
    CONSTANT tpll_i0_q      : NATURAL := 552;
    CONSTANT tphh_i1_q      : NATURAL := 615;
    CONSTANT tpll_i1_q      : NATURAL := 647;
    CONSTANT tphh_i0_q      : NATURAL := 674;
    CONSTANT transistors    : NATURAL := 10
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END ao22_x4;
```

```
ARCHITECTURE behaviour_data_flow OF ao22_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on ao22_x4"
  SEVERITY WARNING;
  q <= ((i0 or i1) and i2) after 1300 ps;
END;
```



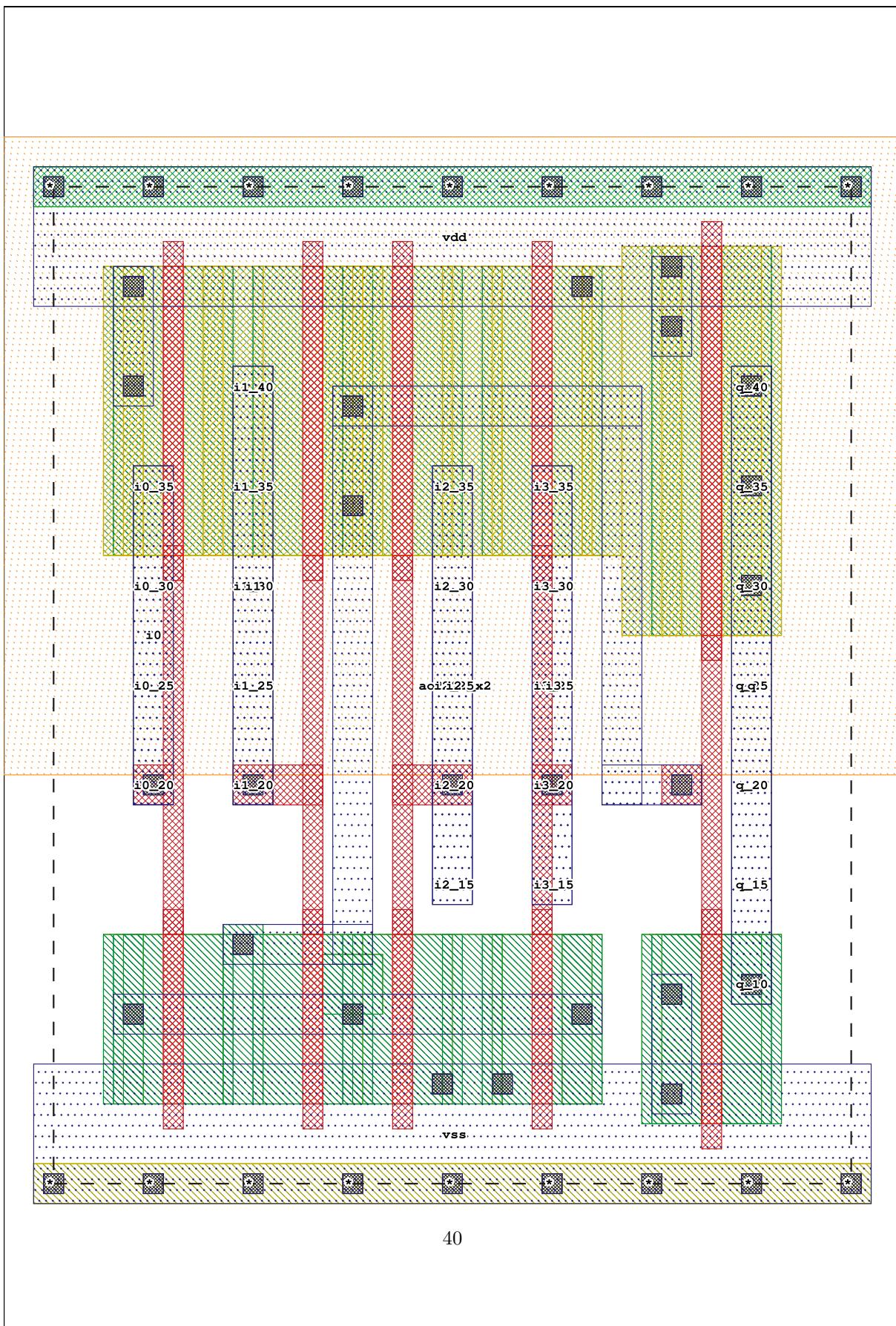
## 4.11 ao2o22\_x2

```

ENTITY ao2o22_x2 IS
GENERIC (
    CONSTANT area          : NATURAL := 2250;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT cin_i3         : NATURAL := 8;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rdown_i3_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT rup_i3_q       : NATURAL := 1790;
    CONSTANT tphh_i2_q      : NATURAL := 432;
    CONSTANT tp1l_i0_q       : NATURAL := 451;
    CONSTANT tp1h_i3_q       : NATURAL := 488;
    CONSTANT tp1h_i1_q       : NATURAL := 508;
    CONSTANT tp1l_i3_q       : NATURAL := 526;
    CONSTANT tp1l_i1_q       : NATURAL := 542;
    CONSTANT tphh_i0_q       : NATURAL := 572;
    CONSTANT tp1l_i2_q       : NATURAL := 627;
    CONSTANT transistors     : NATURAL := 10
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END ao2o22_x2;

ARCHITECTURE behaviour_data_flow OF ao2o22_x2 IS
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on ao2o22_x2"
        SEVERITY WARNING;
    q <= ((i0 or i1) and (i2 or i3)) after 1200 ps;
END;

```



## 4.12 ao2o22\_x4

```

ENTITY ao2o22_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 2500;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT cin_i3         : NATURAL := 8;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rdown_i3_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT tphh_i2_q      : NATURAL := 554;
    CONSTANT tp1l_i0_q       : NATURAL := 569;
    CONSTANT tp1h_i3_q       : NATURAL := 606;
    CONSTANT tp1h_i1_q       : NATURAL := 637;
    CONSTANT tp1l_i3_q       : NATURAL := 639;
    CONSTANT tp1l_i1_q       : NATURAL := 666;
    CONSTANT tphh_i0_q       : NATURAL := 696;
    CONSTANT tp1l_i2_q       : NATURAL := 744;
    CONSTANT transistors     : NATURAL := 12
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END ao2o22_x4;

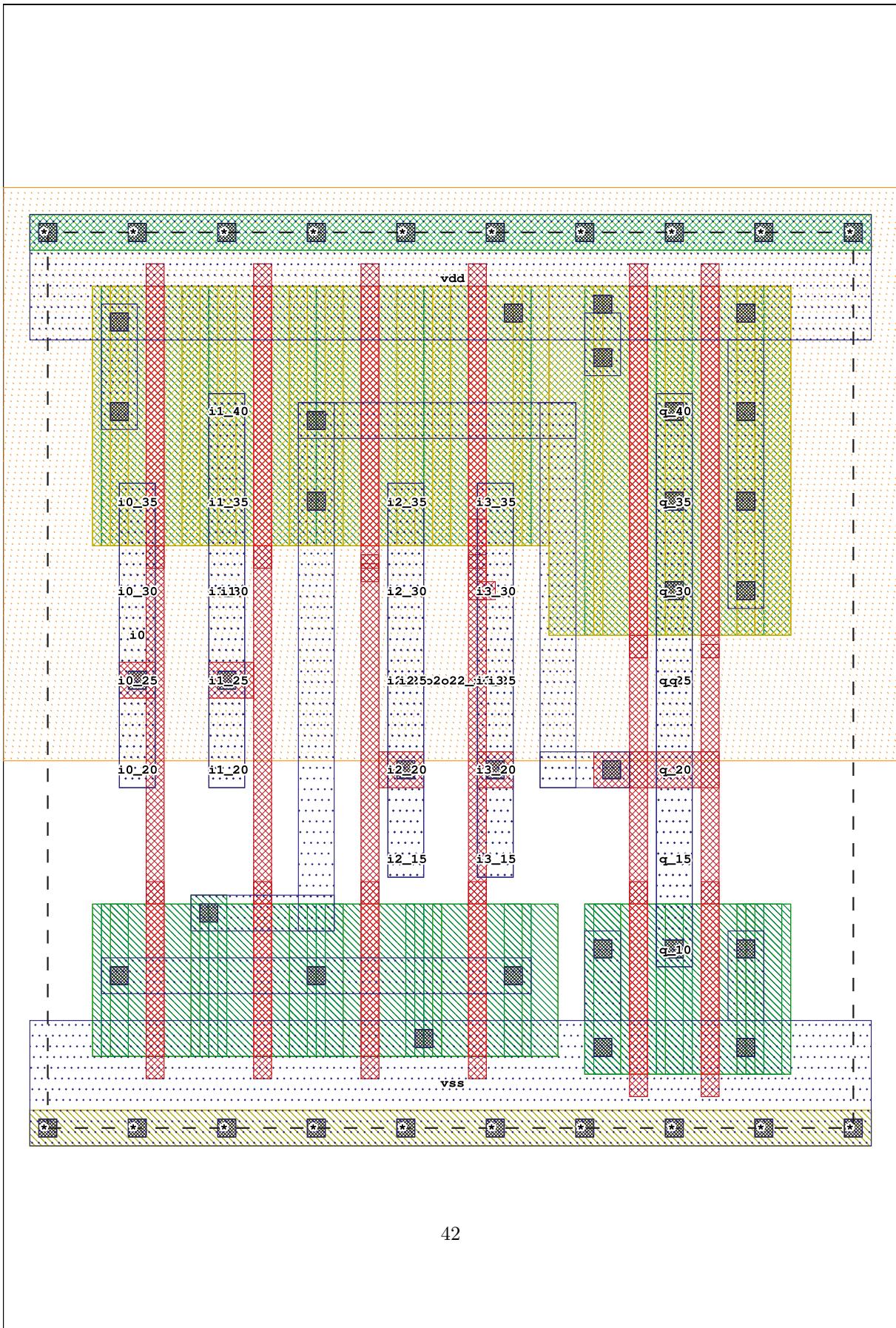
```

```
ARCHITECTURE behaviour_data_flow OF ao2o22_x4 IS
```

```

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on ao2o22_x4"
    SEVERITY WARNING;
    q <= ((i0 or i1) and (i2 or i3)) after 1300 ps;
END;

```

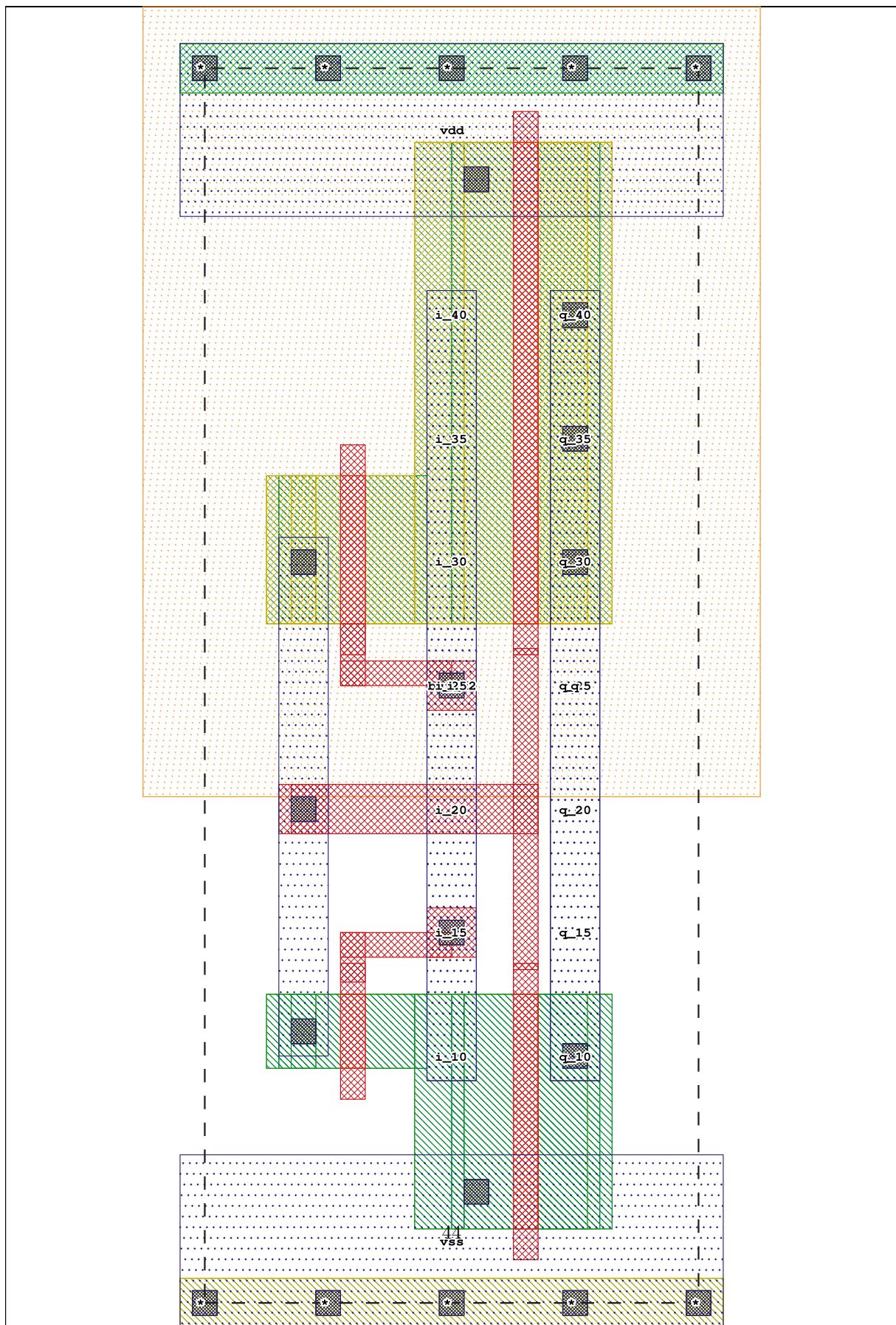


#### 4.13 buf\_x2

```
ENTITY buf_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1000;
    CONSTANT cin_i          : NATURAL := 6;
    CONSTANT rdown_i_q     : NATURAL := 1620;
    CONSTANT rup_i_q       : NATURAL := 1790;
    CONSTANT tpll_i_q      : NATURAL := 391;
    CONSTANT tphh_i_q      : NATURAL := 409;
    CONSTANT transistors   : NATURAL := 4
  );
  PORT (
    i        : in  BIT;
    q        : out BIT;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END buf_x2;

ARCHITECTURE behaviour_data_flow OF buf_x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on buf_x2"
    SEVERITY WARNING;
  q <= i after 1000 ps;
END;
```

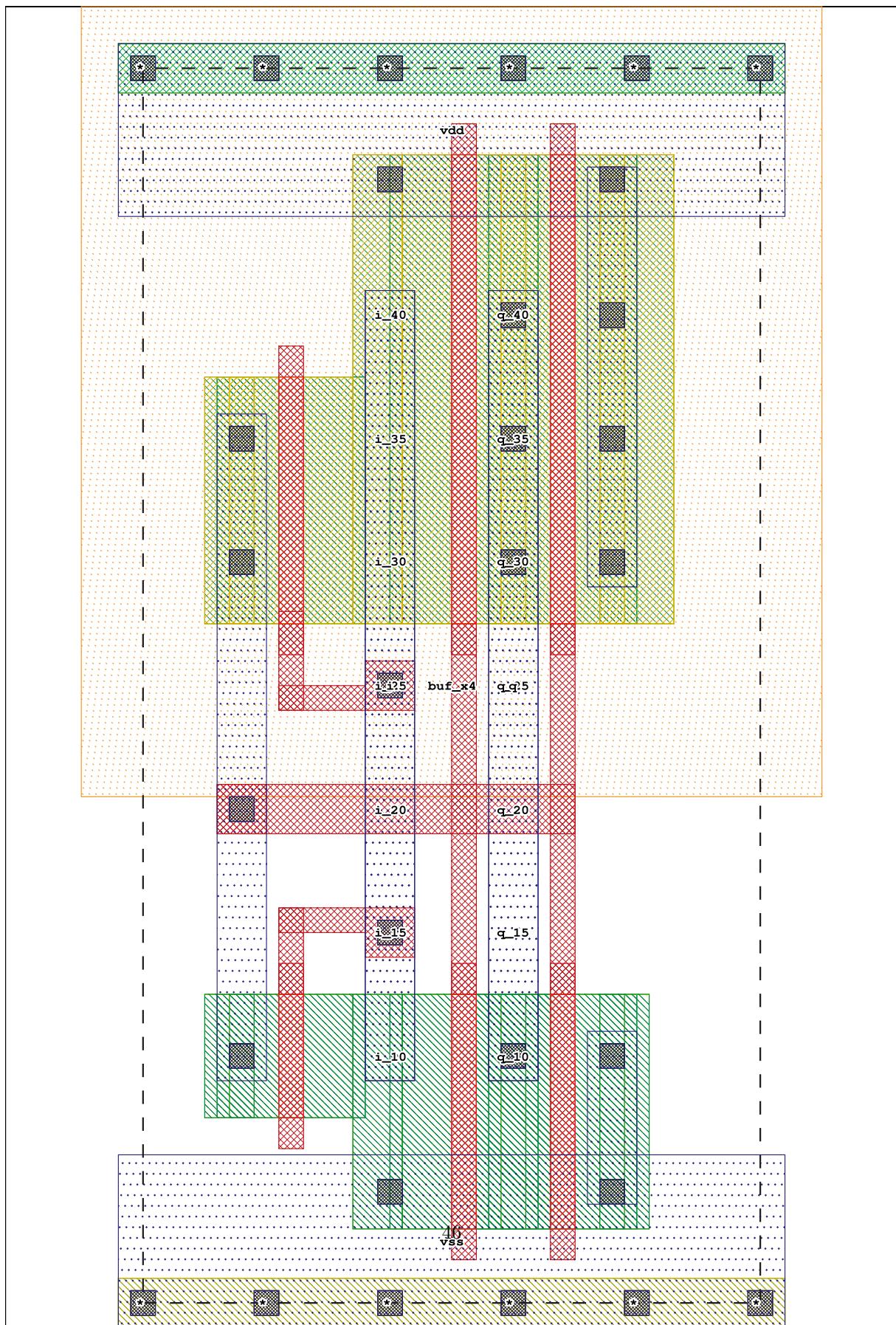


#### 4.14 buf\_x4

```
ENTITY buf_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1250;
    CONSTANT cin_i          : NATURAL := 9;
    CONSTANT rdown_i_q      : NATURAL := 810;
    CONSTANT rup_i_q        : NATURAL := 890;
    CONSTANT tphh_i_q       : NATURAL := 379;
    CONSTANT tp1l_i_q       : NATURAL := 409;
    CONSTANT transistors    : NATURAL := 6
  );
  PORT (
    i           : in  BIT;
    q           : out BIT;
    vdd         : in  BIT;
    vss         : in  BIT
  );
END buf_x4;

ARCHITECTURE behaviour_data_flow OF buf_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on buf_x4"
    SEVERITY WARNING;
  q <= i after 1000 ps;
END;
```

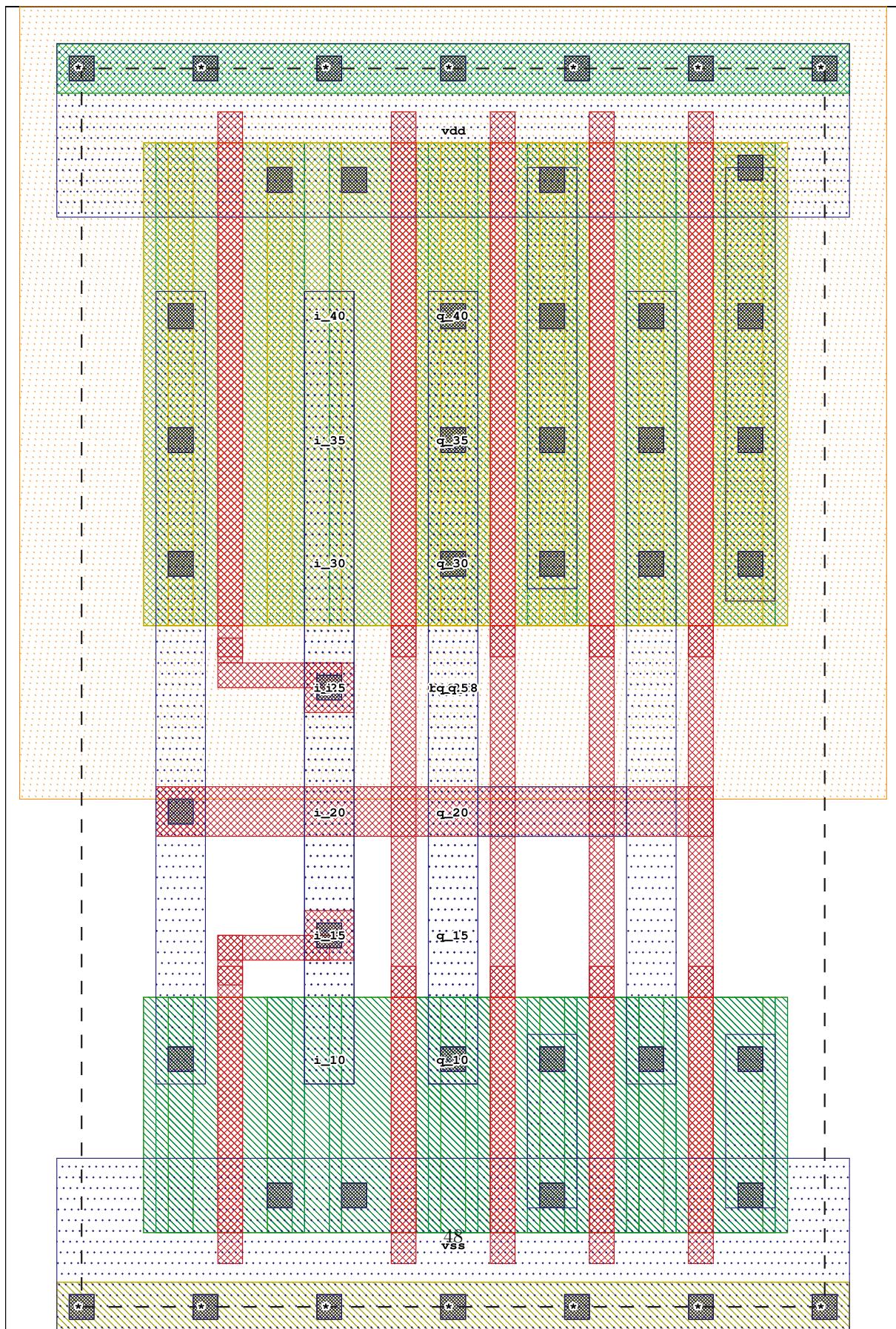


#### 4.15 buf\_x8

```
ENTITY buf_x8 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i          : NATURAL := 15;
    CONSTANT rdown_i_q      : NATURAL := 400;
    CONSTANT rup_i_q        : NATURAL := 450;
    CONSTANT tphh_i_q       : NATURAL := 343;
    CONSTANT tp1l_i_q       : NATURAL := 396;
    CONSTANT transistors   : NATURAL := 10
  );
  PORT (
    i           : in  BIT;
    q           : out BIT;
    vdd         : in  BIT;
    vss         : in  BIT
  );
END buf_x8;

ARCHITECTURE behaviour_data_flow OF buf_x8 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on buf_x8"
    SEVERITY WARNING;
  q <= i after 1000 ps;
END;
```

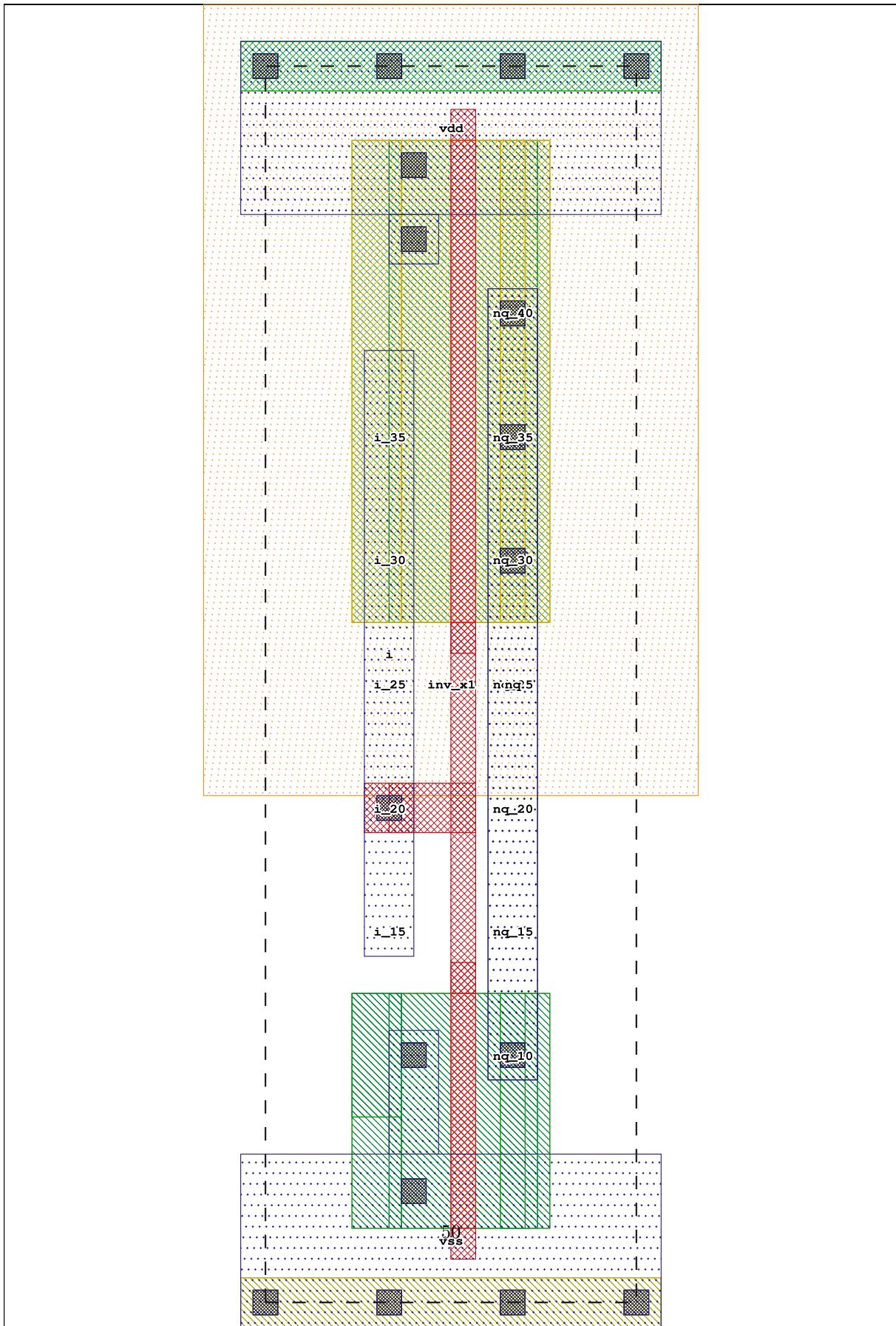


#### 4.16 inv\_x1

```
ENTITY inv_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 750;
    CONSTANT cin_i          : NATURAL := 8;
    CONSTANT rdown_i_nq     : NATURAL := 3640;
    CONSTANT rup_i_nq       : NATURAL := 3720;
    CONSTANT tphl_i_nq      : NATURAL := 101;
    CONSTANT tplh_i_nq      : NATURAL := 139;
    CONSTANT transistors    : NATURAL := 2
  );
  PORT (
    i           : in  BIT;
    nq          : out BIT;
    vdd         : in   BIT;
    vss         : in   BIT
  );
END inv_x1;

ARCHITECTURE behaviour_data_flow OF inv_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on inv_x1"
  SEVERITY WARNING;
  nq <= not (i) after 700 ps;
END;
```

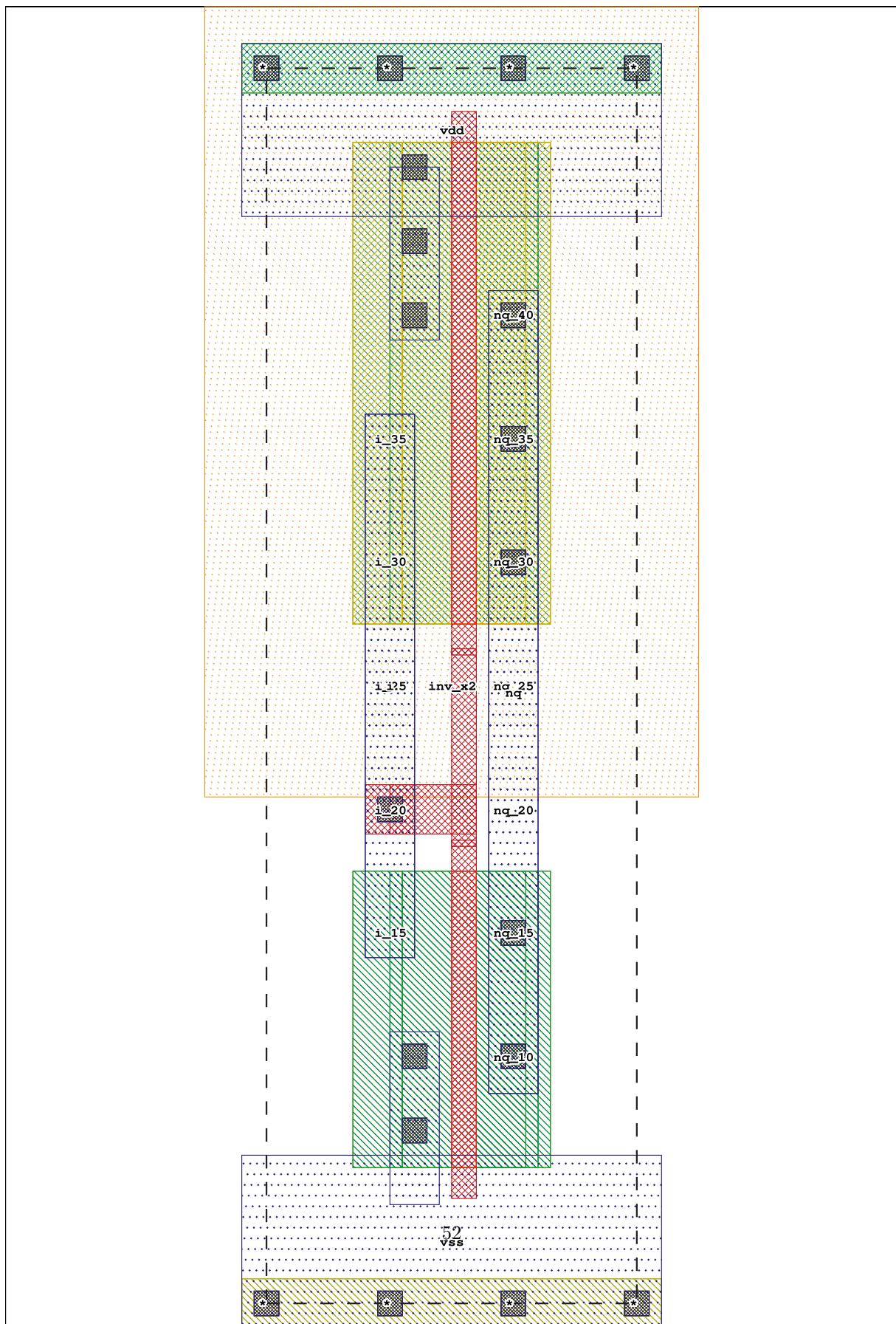


#### 4.17 inv\_x2

```
ENTITY inv_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 750;
    CONSTANT cin_i          : NATURAL := 12;
    CONSTANT rdown_i_nq    : NATURAL := 1620;
    CONSTANT rup_i_nq      : NATURAL := 2420;
    CONSTANT tphl_i_nq     : NATURAL := 69;
    CONSTANT tplh_i_nq     : NATURAL := 163;
    CONSTANT transistors   : NATURAL := 2
  );
  PORT (
    i           : in  BIT;
    nq          : out BIT;
    vdd         : in  BIT;
    vss         : in  BIT
  );
END inv_x2;

ARCHITECTURE behaviour_data_flow OF inv_x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on inv_x2"
  SEVERITY WARNING;
  nq <= not (i) after 800 ps;
END;
```

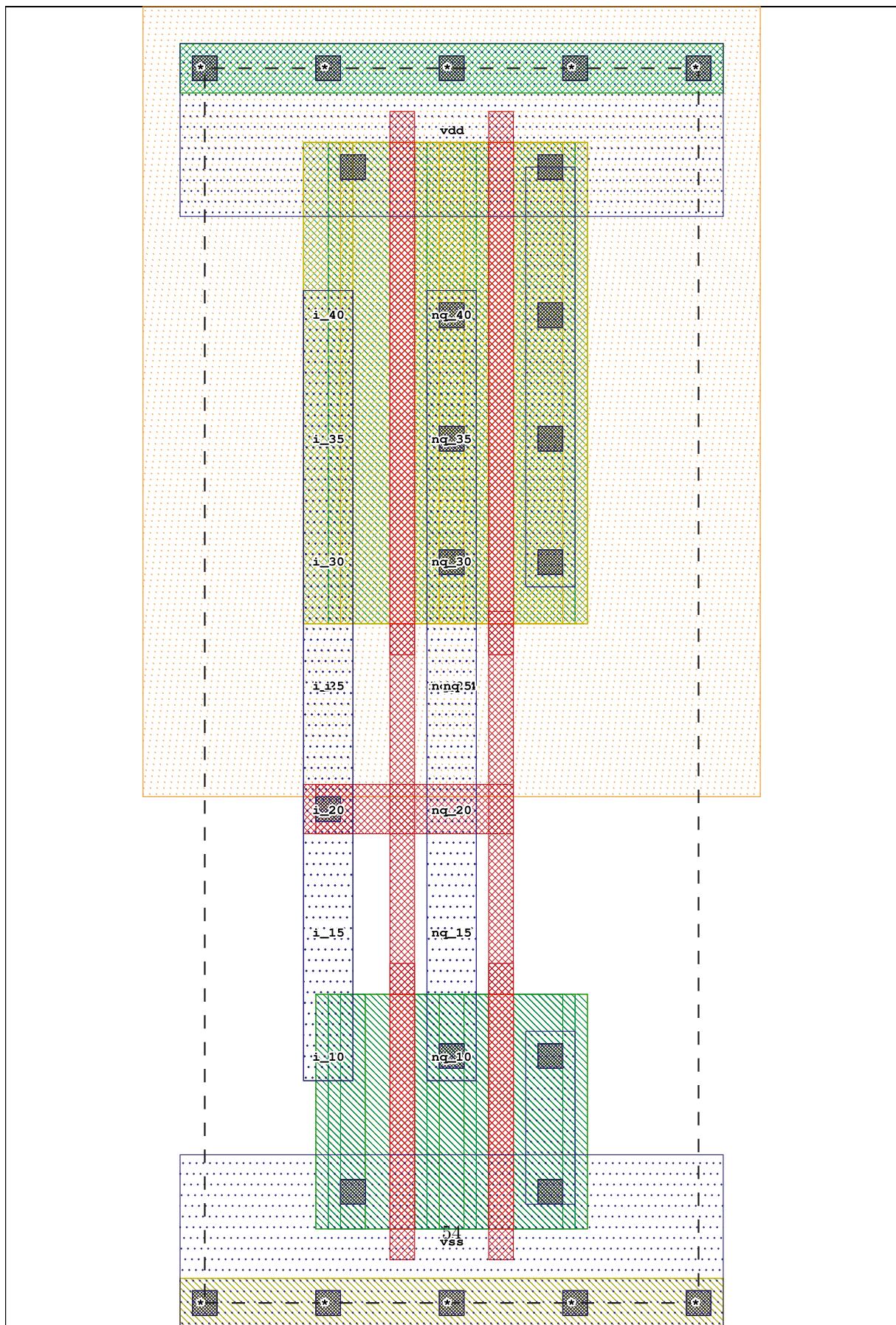


#### 4.18 inv\_x4

```
ENTITY inv_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1000;
    CONSTANT cin_i          : NATURAL := 26;
    CONSTANT rdown_i_nq    : NATURAL := 810;
    CONSTANT rup_i_nq      : NATURAL := 1060;
    CONSTANT tphl_i_nq     : NATURAL := 71;
    CONSTANT tplh_i_nq     : NATURAL := 143;
    CONSTANT transistors   : NATURAL := 4
  );
  PORT (
    i           : in  BIT;
    nq          : out BIT;
    vdd         : in  BIT;
    vss         : in  BIT
  );
END inv_x4;

ARCHITECTURE behaviour_data_flow OF inv_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on inv_x4"
  SEVERITY WARNING;
  nq <= not (i) after 700 ps;
END;
```

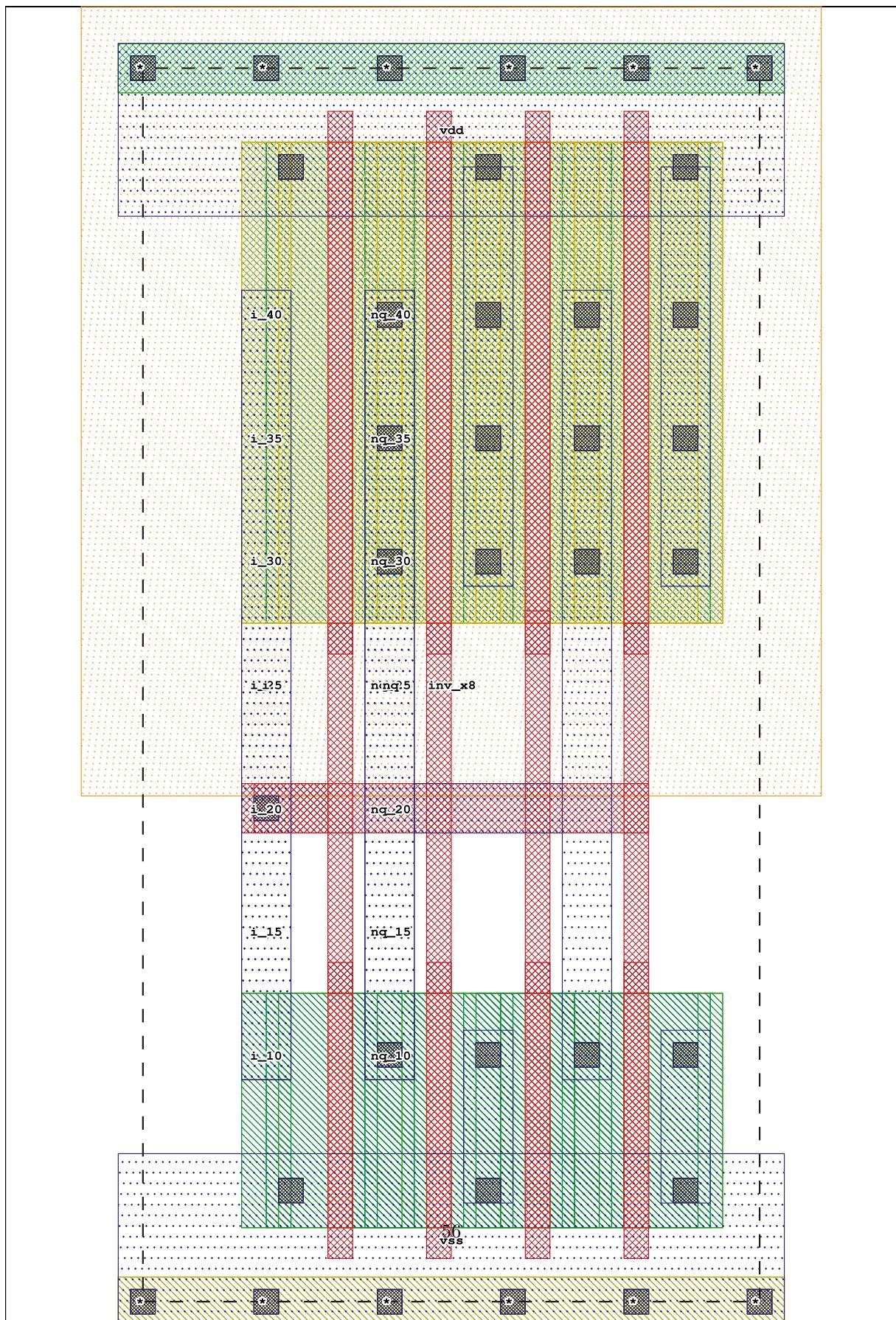


#### 4.19 inv\_x8

```
ENTITY inv_x8 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i          : NATURAL := 54;
    CONSTANT rdown_i_nq    : NATURAL := 400;
    CONSTANT rup_i_nq      : NATURAL := 450;
    CONSTANT tphl_i_nq     : NATURAL := 86;
    CONSTANT tplh_i_nq     : NATURAL := 133;
    CONSTANT transistors   : NATURAL := 8
  );
  PORT (
    i           : in  BIT;
    nq          : out BIT;
    vdd         : in  BIT;
    vss         : in  BIT
  );
END inv_x8;

ARCHITECTURE behaviour_data_flow OF inv_x8 IS

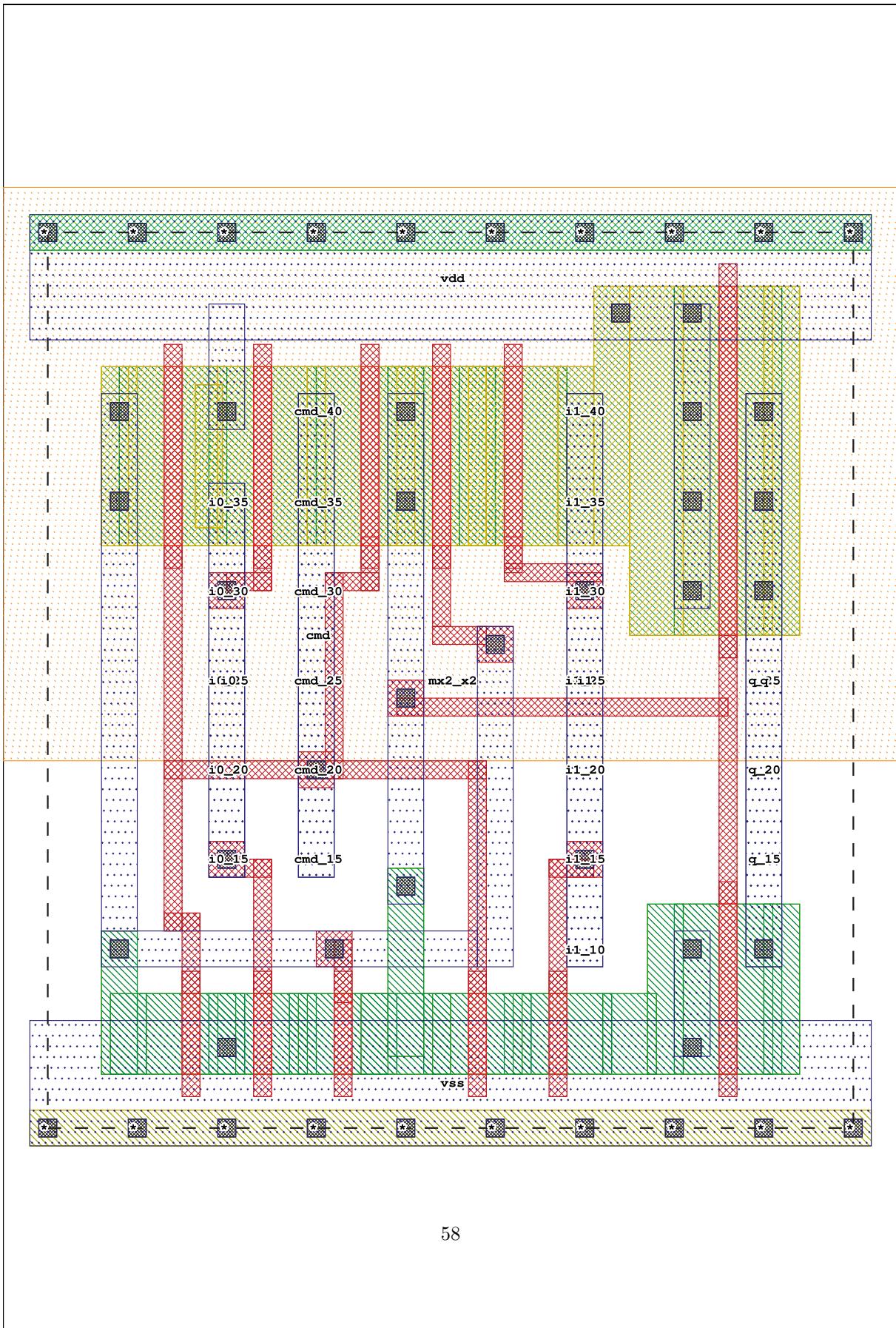
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on inv_x8"
  SEVERITY WARNING;
  nq <= not (i) after 700 ps;
END;
```



## 4.20 mx2\_x2

```
ENTITY mx2_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2250;
    CONSTANT cin_cmd       : NATURAL := 17;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT rdown_cmd_q   : NATURAL := 1620;
    CONSTANT rdown_i0_q    : NATURAL := 1620;
    CONSTANT rdown_i1_q    : NATURAL := 1620;
    CONSTANT rup_cmd_q     : NATURAL := 1790;
    CONSTANT rup_i0_q      : NATURAL := 1790;
    CONSTANT rup_i1_q      : NATURAL := 1790;
    CONSTANT tphh_i0_q     : NATURAL := 451;
    CONSTANT tphh_i1_q     : NATURAL := 451;
    CONSTANT tpll_i0_q     : NATURAL := 469;
    CONSTANT tpll_i1_q     : NATURAL := 469;
    CONSTANT tphh_cmd_q    : NATURAL := 484;
    CONSTANT tphl_cmd_q    : NATURAL := 485;
    CONSTANT tpll_cmd_q    : NATURAL := 522;
    CONSTANT tplh_cmd_q    : NATURAL := 534;
    CONSTANT transistors   : NATURAL := 12
  );
  PORT (
    cmd      : in  BIT;
    i0       : in  BIT;
    i1       : in  BIT;
    q        : out BIT;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END mx2_x2;
```

```
ARCHITECTURE behaviour_data_flow OF mx2_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on mx2_x2"
  SEVERITY WARNING;
  q <= ((i1 and cmd) or (not (cmd) and i0)) after 1100 ps;
END;
```

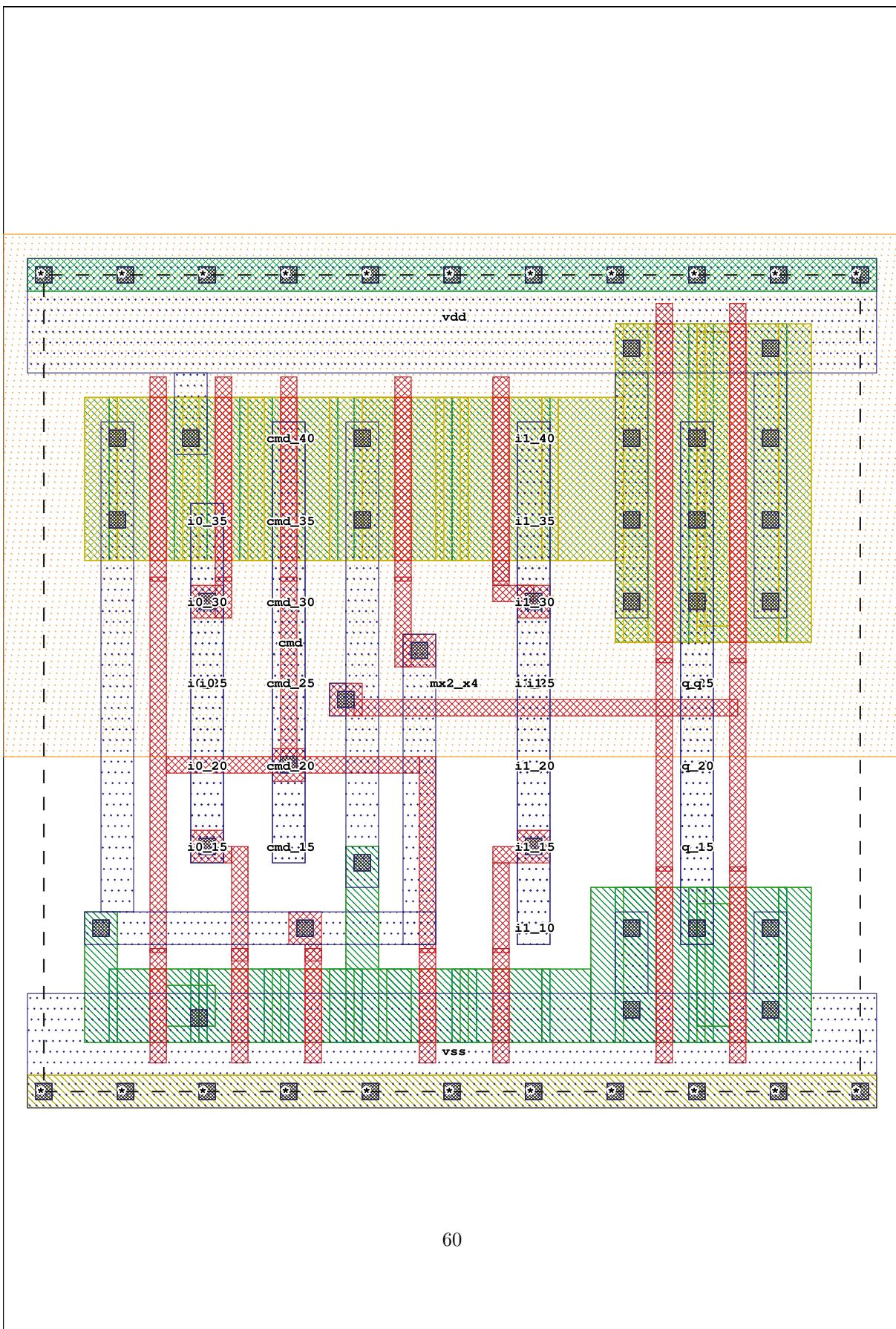


## 4.21 mx2\_x4

```
ENTITY mx2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2500;
    CONSTANT cin_cmd       : NATURAL := 17;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT rdown_cmd_q   : NATURAL := 810;
    CONSTANT rdown_i0_q    : NATURAL := 810;
    CONSTANT rdown_i1_q    : NATURAL := 810;
    CONSTANT rup_cmd_q     : NATURAL := 890;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT tphh_i0_q     : NATURAL := 564;
    CONSTANT tphh_i1_q     : NATURAL := 564;
    CONSTANT tphl_cmd_q    : NATURAL := 574;
    CONSTANT tpll_i0_q      : NATURAL := 576;
    CONSTANT tpll_i1_q      : NATURAL := 576;
    CONSTANT tphh_cmd_q    : NATURAL := 615;
    CONSTANT tphl_cmd_q    : NATURAL := 631;
    CONSTANT tpll_cmd_q    : NATURAL := 647;
    CONSTANT transistors   : NATURAL := 14
  );
  PORT (
    cmd      : in  BIT;
    i0       : in  BIT;
    i1       : in  BIT;
    q        : out BIT;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END mx2_x4;
```

```
ARCHITECTURE behaviour_data_flow OF mx2_x4 IS
```

```
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on mx2_x4"
  SEVERITY WARNING;
  q <= ((i1 and cmd) or (not (cmd) and i0)) after 1200 ps;
END;
```

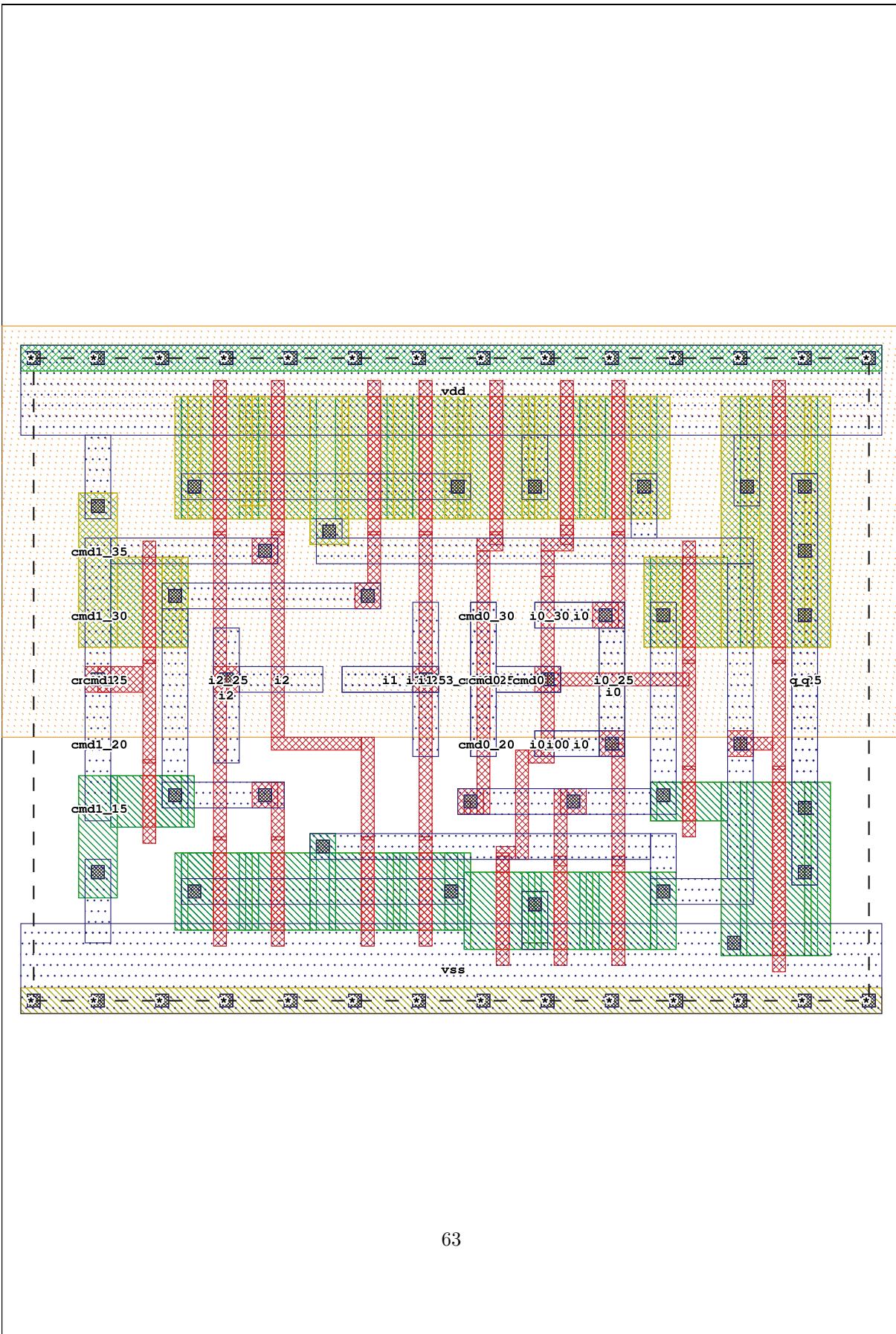


## 4.22 mx3\_x2

```
ENTITY mx3_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3250;
    CONSTANT cin_cmd0      : NATURAL := 15;
    CONSTANT cin_cmd1      : NATURAL := 15;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT rdown_cmd0_q   : NATURAL := 1620;
    CONSTANT rdown_cmd1_q   : NATURAL := 1620;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rup_cmd0_q     : NATURAL := 1790;
    CONSTANT rup_cmd1_q     : NATURAL := 1790;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT tphh_i0_q      : NATURAL := 538;
    CONSTANT tphh_cmd0_q    : NATURAL := 573;
    CONSTANT tphh_i1_q      : NATURAL := 654;
    CONSTANT tphh_i2_q      : NATURAL := 654;
    CONSTANT tpll_i0_q      : NATURAL := 658;
    CONSTANT tphh_cmd1_q    : NATURAL := 664;
    CONSTANT tpll_cmd0_q    : NATURAL := 680;
    CONSTANT tphh_cmd1_q    : NATURAL := 738;
    CONSTANT tphh_i1_q      : NATURAL := 739;
    CONSTANT tphh_cmd0_q    : NATURAL := 768;
    CONSTANT tphh_cmd0_q    : NATURAL := 792;
    CONSTANT tpll_i1_q      : NATURAL := 808;
    CONSTANT tpll_i2_q      : NATURAL := 808;
    CONSTANT tpll_cmd1_q    : NATURAL := 817;
    CONSTANT transistors    : NATURAL := 20
  );
  PORT (
    cmd0    : in  BIT;
    cmd1    : in  BIT;
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END mx3_x2;
```

```
ARCHITECTURE behaviour_data_flow OF mx3_x2 IS
```

```
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on mx3_x2"
    SEVERITY WARNING;
    q <= ((not (cmd0) and i0) or (cmd0 and ((cmd1 and i1) or (not (cmd1)
        and i2)))) after 1400 ps;
END;
```

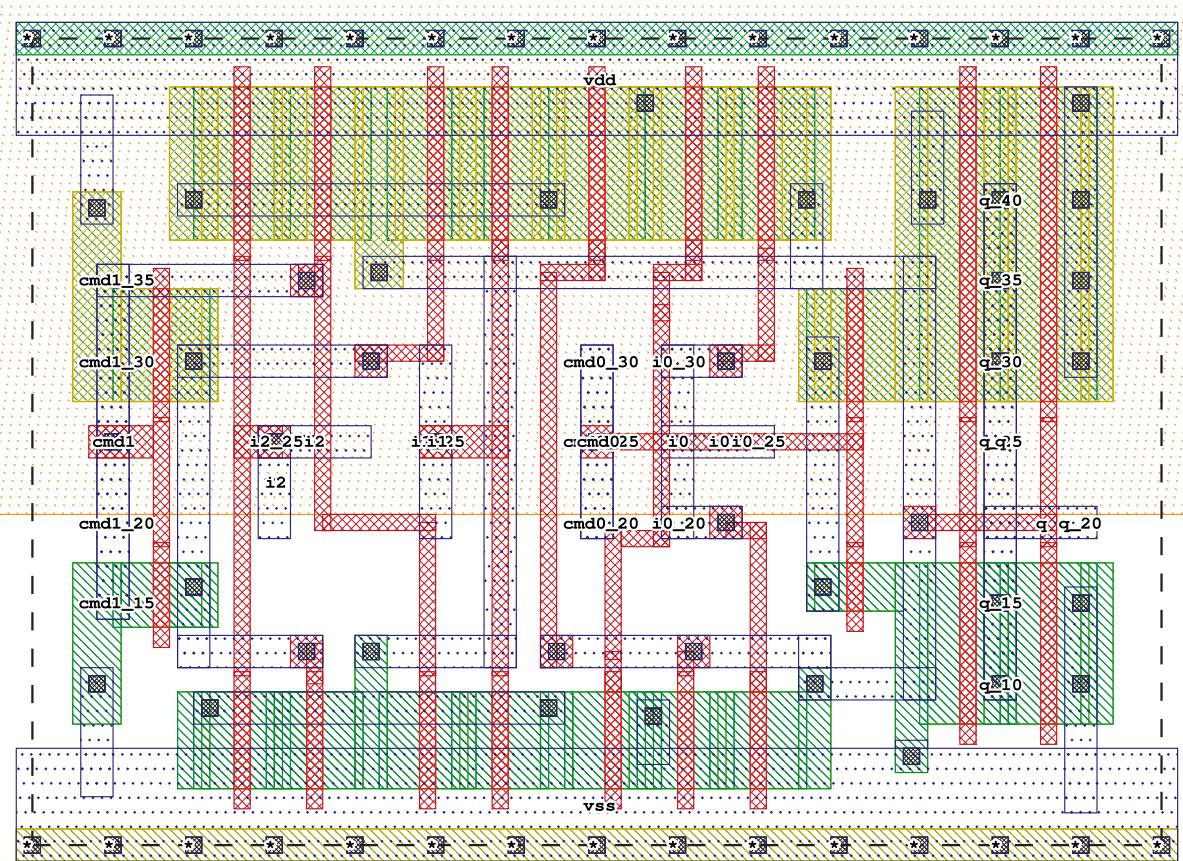


#### 4.23 mx3\_x4

```
ENTITY mx3_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3500;
    CONSTANT cin_cmd0      : NATURAL := 15;
    CONSTANT cin_cmd1      : NATURAL := 15;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT rdown_cmd0_q   : NATURAL := 810;
    CONSTANT rdown_cmd1_q   : NATURAL := 810;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rup_cmd0_q     : NATURAL := 890;
    CONSTANT rup_cmd1_q     : NATURAL := 890;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT tphh_i0_q      : NATURAL := 640;
    CONSTANT tphh_cmd0_q    : NATURAL := 683;
    CONSTANT tphh_i1_q      : NATURAL := 770;
    CONSTANT tphh_i2_q      : NATURAL := 770;
    CONSTANT tpll_i0_q      : NATURAL := 774;
    CONSTANT tpll_cmd0_q    : NATURAL := 779;
    CONSTANT tphh_cmd1_q    : NATURAL := 792;
    CONSTANT tphh_cmd0_q    : NATURAL := 844;
    CONSTANT tphh_cmd1_q    : NATURAL := 846;
    CONSTANT tphl_cmd1_q    : NATURAL := 872;
    CONSTANT tphl_cmd0_q    : NATURAL := 922;
    CONSTANT tpll_i1_q      : NATURAL := 948;
    CONSTANT tpll_i2_q      : NATURAL := 948;
    CONSTANT tpll_cmd1_q    : NATURAL := 967;
    CONSTANT transistors    : NATURAL := 22
  );
  PORT (
    cmd0    : in  BIT;
    cmd1    : in  BIT;
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END mx3_x4;
```

```
ARCHITECTURE behaviour_data_flow OF mx3_x4 IS
```

```
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on mx3_x4"
    SEVERITY WARNING;
    q <= ((not (cmd0) and i0) or (cmd0 and ((cmd1 and i1) or (not (cmd1)
        and i2)))) after 1600 ps;
END;
```

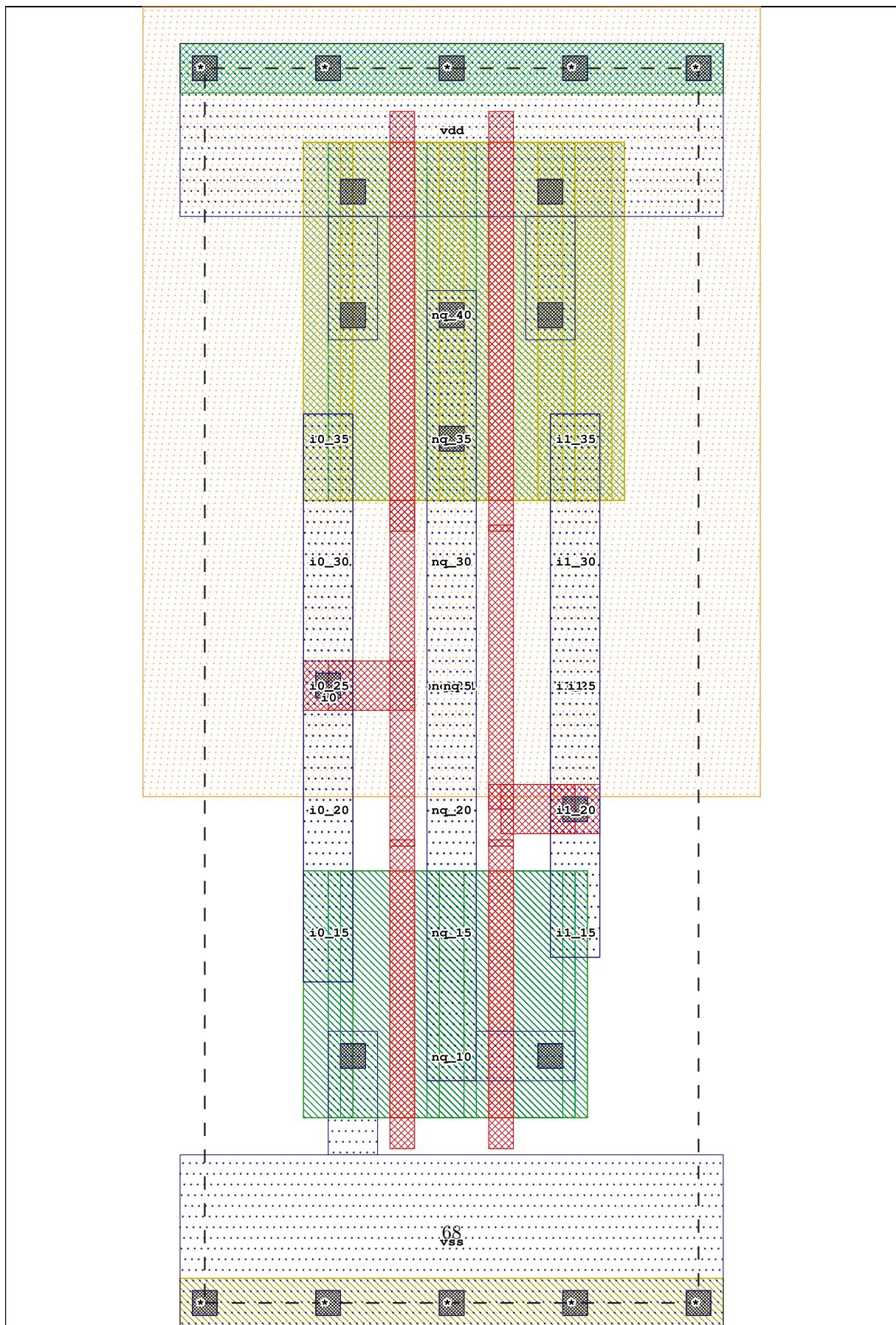


#### 4.24 na2\_x1

```
ENTITY na2_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1000;
    CONSTANT cin_i0         : NATURAL := 11;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT rdown_i0_nq   : NATURAL := 2850;
    CONSTANT rdown_i1_nq   : NATURAL := 2850;
    CONSTANT rup_i0_nq     : NATURAL := 3720;
    CONSTANT rup_i1_nq     : NATURAL := 3720;
    CONSTANT tphl_i0_nq    : NATURAL := 59;
    CONSTANT tphl_i1_nq    : NATURAL := 111;
    CONSTANT tplh_i1_nq    : NATURAL := 234;
    CONSTANT tplh_i0_nq    : NATURAL := 288;
    CONSTANT transistors   : NATURAL := 4
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END na2_x1;

ARCHITECTURE behaviour_data_flow OF na2_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on na2_x1"
  SEVERITY WARNING;
  nq <= not ((i0 and i1)) after 900 ps;
END;
```

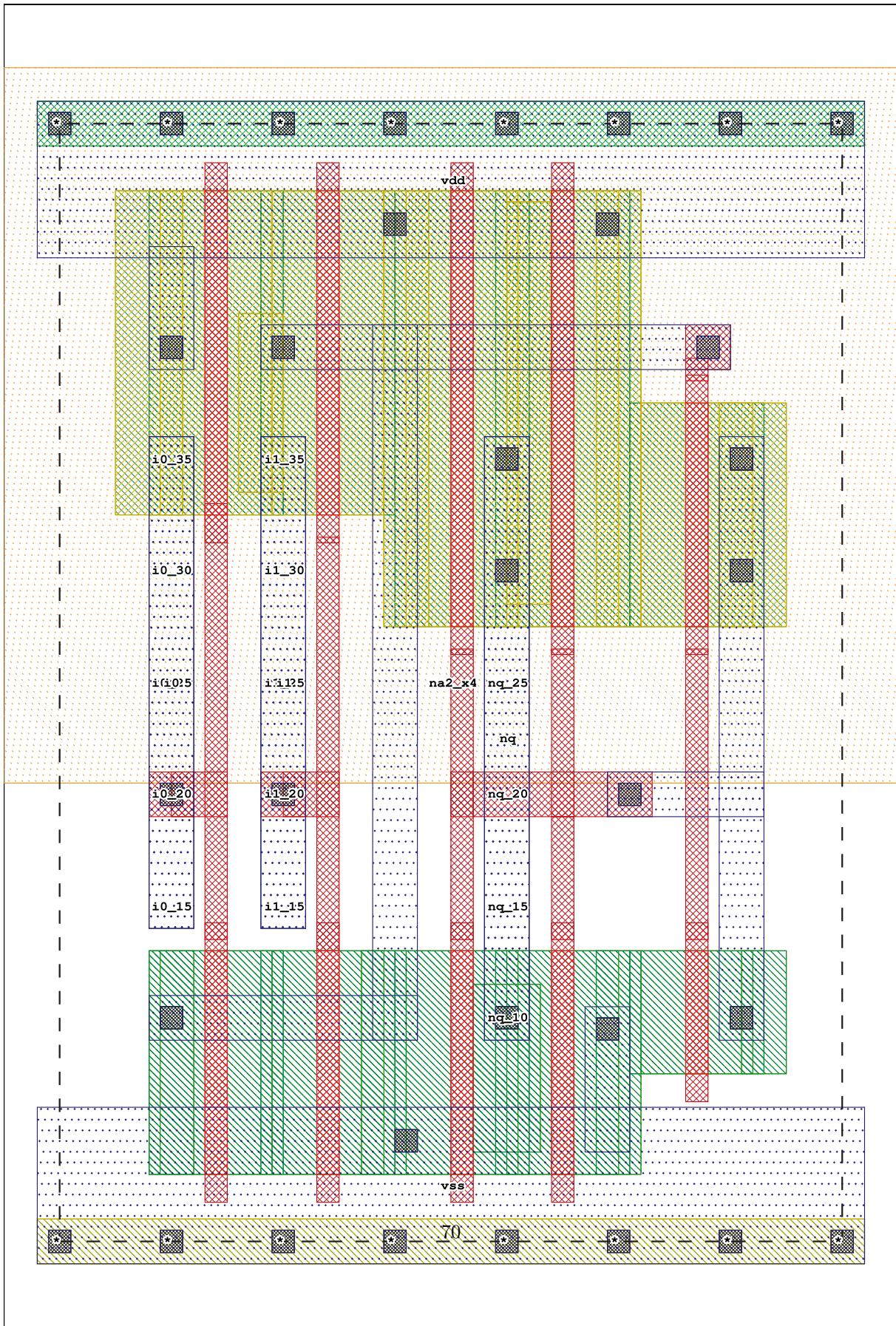


## 4.25 na2\_x4

```
ENTITY na2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT tphl_i1_nq    : NATURAL := 353;
    CONSTANT tphl_i0_nq    : NATURAL := 412;
    CONSTANT tplh_i0_nq    : NATURAL := 552;
    CONSTANT tplh_i1_nq    : NATURAL := 601;
    CONSTANT transistors   : NATURAL := 10
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END na2_x4;

ARCHITECTURE behaviour_data_flow OF na2_x4 IS

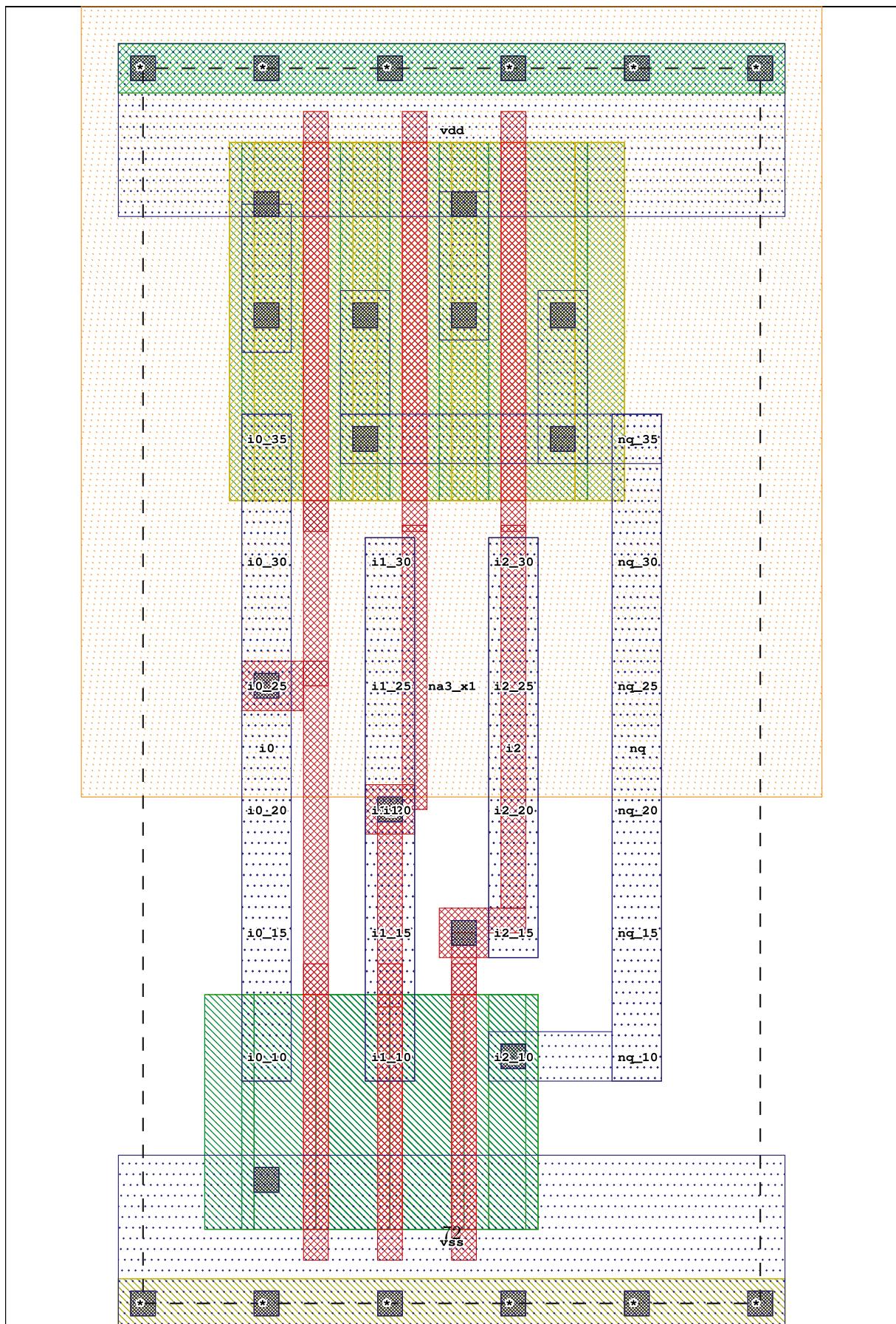
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on na2_x4"
  SEVERITY WARNING;
  nq <= not ((i0 and i1)) after 1200 ps;
END;
```



## 4.26 na3\_x1

```
ENTITY na3_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1250;
    CONSTANT cin_i0         : NATURAL := 11;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT cin_i2         : NATURAL := 11;
    CONSTANT rdown_i0_nq   : NATURAL := 4120;
    CONSTANT rdown_i1_nq   : NATURAL := 4120;
    CONSTANT rdown_i2_nq   : NATURAL := 4120;
    CONSTANT rup_i0_nq     : NATURAL := 3720;
    CONSTANT rup_i1_nq     : NATURAL := 3720;
    CONSTANT rup_i2_nq     : NATURAL := 3720;
    CONSTANT tphl_i0_nq    : NATURAL := 119;
    CONSTANT tphl_i1_nq    : NATURAL := 171;
    CONSTANT tphl_i2_nq    : NATURAL := 193;
    CONSTANT tplh_i2_nq    : NATURAL := 265;
    CONSTANT tplh_i1_nq    : NATURAL := 316;
    CONSTANT tplh_i0_nq    : NATURAL := 363;
    CONSTANT transistors   : NATURAL := 6
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END na3_x1;
```

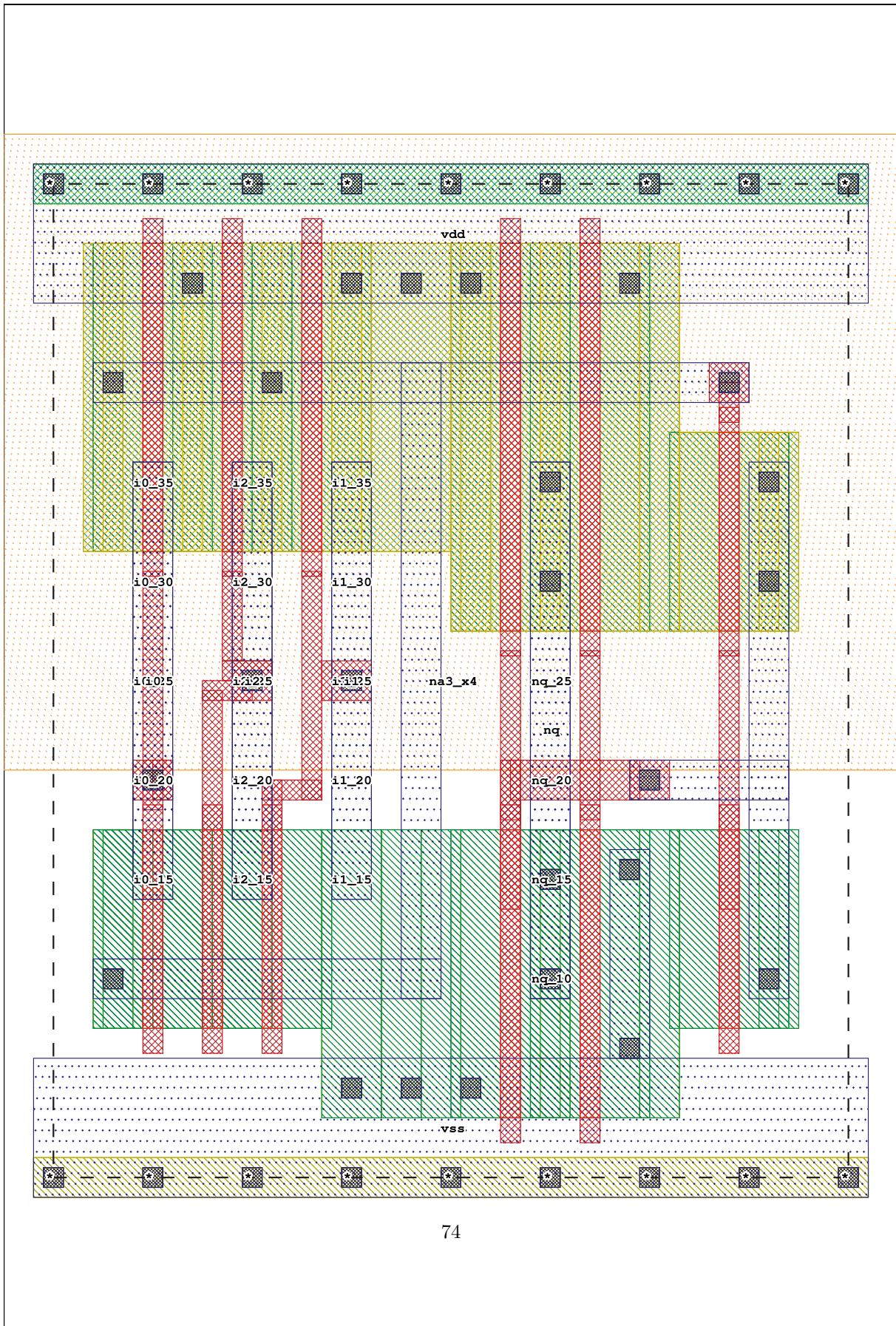
```
ARCHITECTURE behaviour_data_flow OF na3_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on na3_x1"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) and i2)) after 1000 ps;
END;
```



#### 4.27 na3\_x4

```
ENTITY na3_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT cin_i2         : NATURAL := 10;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rdown_i2_nq   : NATURAL := 810;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT rup_i2_nq     : NATURAL := 890;
    CONSTANT tphl_i1_nq    : NATURAL := 460;
    CONSTANT tphl_i2_nq    : NATURAL := 519;
    CONSTANT tphl_i0_nq    : NATURAL := 556;
    CONSTANT tplh_i0_nq    : NATURAL := 601;
    CONSTANT tplh_i2_nq    : NATURAL := 647;
    CONSTANT tplh_i1_nq    : NATURAL := 691;
    CONSTANT transistors   : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END na3_x4;
```

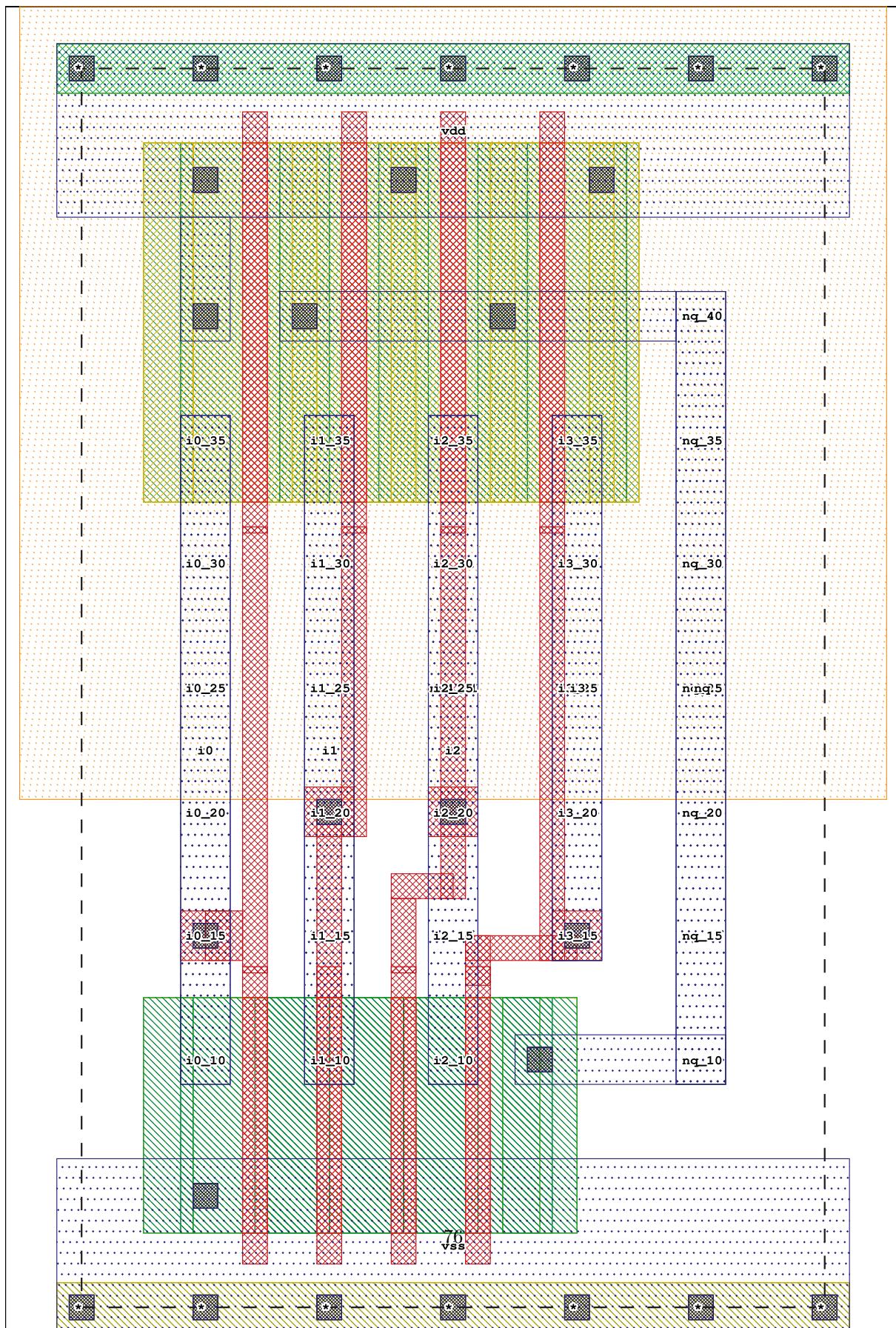
```
ARCHITECTURE behaviour_data_flow OF na3_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on na3_x4"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) and i2)) after 1300 ps;
END;
```



## 4.28 na4\_x1

```
ENTITY na4_x1 IS
  GENERIC (
    CONSTANT area : NATURAL := 1500;
    CONSTANT cin_i0 : NATURAL := 10;
    CONSTANT cin_i1 : NATURAL := 11;
    CONSTANT cin_i2 : NATURAL := 11;
    CONSTANT cin_i3 : NATURAL := 11;
    CONSTANT rdown_i0_nq : NATURAL := 5400;
    CONSTANT rdown_i1_nq : NATURAL := 5400;
    CONSTANT rdown_i2_nq : NATURAL := 5400;
    CONSTANT rdown_i3_nq : NATURAL := 5400;
    CONSTANT rup_i0_nq : NATURAL := 3720;
    CONSTANT rup_i1_nq : NATURAL := 3720;
    CONSTANT rup_i2_nq : NATURAL := 3720;
    CONSTANT rup_i3_nq : NATURAL := 3720;
    CONSTANT tphl_i0_nq : NATURAL := 179;
    CONSTANT tphl_i1_nq : NATURAL := 237;
    CONSTANT tphl_i2_nq : NATURAL := 269;
    CONSTANT tphl_i3_nq : NATURAL := 282;
    CONSTANT tplh_i3_nq : NATURAL := 302;
    CONSTANT tplh_i2_nq : NATURAL := 350;
    CONSTANT tplh_i1_nq : NATURAL := 395;
    CONSTANT tplh_i0_nq : NATURAL := 438;
    CONSTANT transistors : NATURAL := 8
  );
  PORT (
    i0 : in BIT;
    i1 : in BIT;
    i2 : in BIT;
    i3 : in BIT;
    nq : out BIT;
    vdd : in BIT;
    vss : in BIT
  );
END na4_x1;

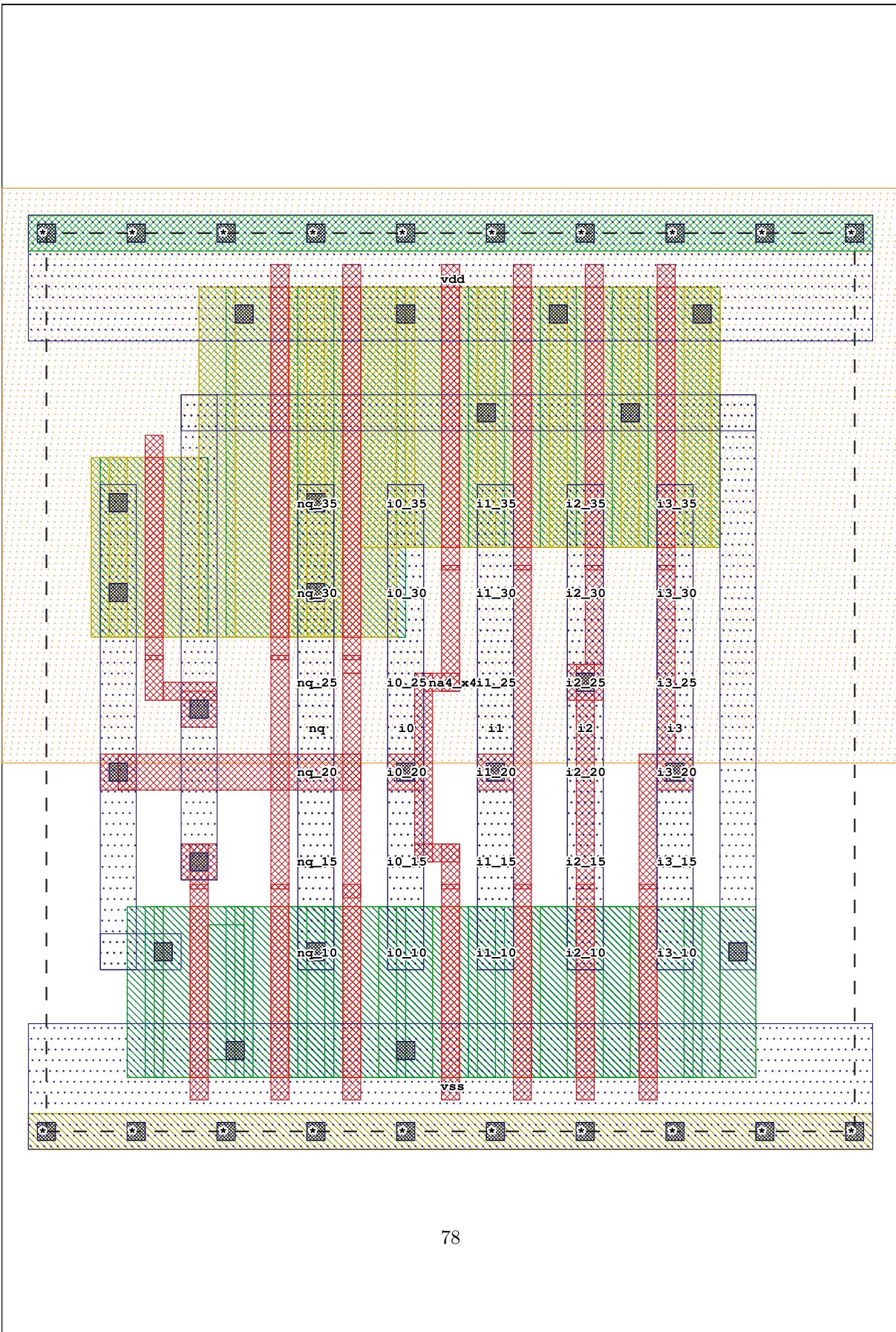
ARCHITECTURE behaviour_data_flow OF na4_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on na4_x1"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) and i2) and i3)) after 1000 ps;
END;
```



#### 4.29 na4\_x4

```
ENTITY na4_x4 IS
  GENERIC (
    CONSTANT area : NATURAL := 2500;
    CONSTANT cin_i0 : NATURAL := 10;
    CONSTANT cin_i1 : NATURAL := 11;
    CONSTANT cin_i2 : NATURAL := 11;
    CONSTANT cin_i3 : NATURAL := 11;
    CONSTANT rdown_i0_nq : NATURAL := 810;
    CONSTANT rdown_i1_nq : NATURAL := 810;
    CONSTANT rdown_i2_nq : NATURAL := 810;
    CONSTANT rdown_i3_nq : NATURAL := 810;
    CONSTANT rup_i0_nq : NATURAL := 890;
    CONSTANT rup_i1_nq : NATURAL := 890;
    CONSTANT rup_i2_nq : NATURAL := 890;
    CONSTANT rup_i3_nq : NATURAL := 890;
    CONSTANT tphl_i0_nq : NATURAL := 578;
    CONSTANT tphl_i1_nq : NATURAL := 643;
    CONSTANT tphl_i3_nq : NATURAL := 644;
    CONSTANT tphl_i2_nq : NATURAL := 681;
    CONSTANT tplh_i2_nq : NATURAL := 689;
    CONSTANT tphl_i3_nq : NATURAL := 703;
    CONSTANT tplh_i1_nq : NATURAL := 731;
    CONSTANT tplh_i0_nq : NATURAL := 771;
    CONSTANT transistors : NATURAL := 14
  );
  PORT (
    i0 : in BIT;
    i1 : in BIT;
    i2 : in BIT;
    i3 : in BIT;
    nq : out BIT;
    vdd : in BIT;
    vss : in BIT
  );
END na4_x4;

ARCHITECTURE behaviour_data_flow OF na4_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on na4_x4"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) and i2) and i3)) after 1400 ps;
END;
```

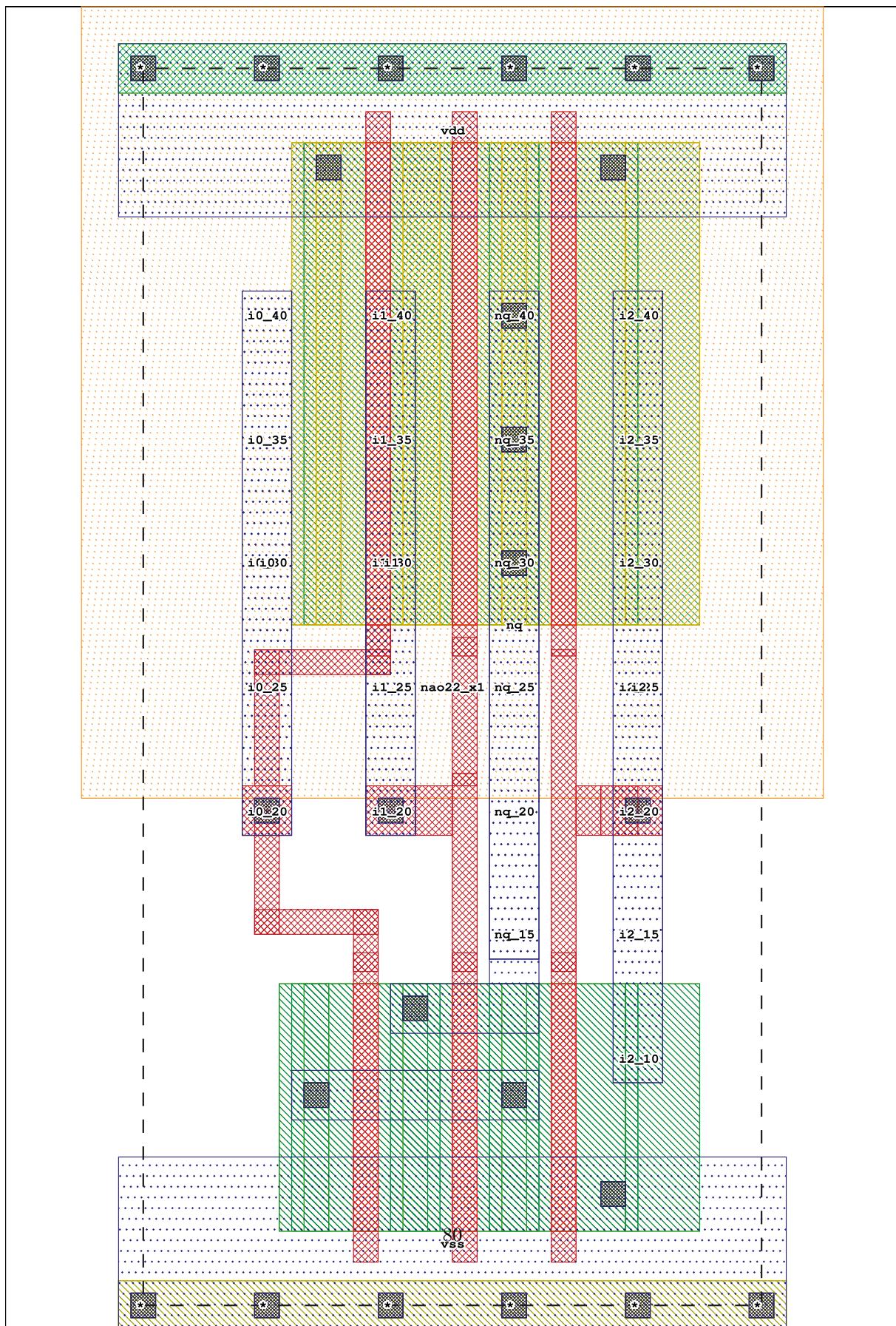


#### 4.30 nao22\_x1

```
ENTITY nao22_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 15;
    CONSTANT rdown_i0_nq    : NATURAL := 2850;
    CONSTANT rdown_i1_nq    : NATURAL := 2850;
    CONSTANT rdown_i2_nq    : NATURAL := 2850;
    CONSTANT rup_i0_nq      : NATURAL := 3210;
    CONSTANT rup_i1_nq      : NATURAL := 3210;
    CONSTANT rup_i2_nq      : NATURAL := 1790;
    CONSTANT tphl_i2_nq     : NATURAL := 165;
    CONSTANT tphl_i1_nq     : NATURAL := 218;
    CONSTANT tplh_i0_nq     : NATURAL := 226;
    CONSTANT tplh_i2_nq     : NATURAL := 238;
    CONSTANT tplh_i1_nq     : NATURAL := 287;
    CONSTANT tphl_i0_nq     : NATURAL := 294;
    CONSTANT transistors    : NATURAL := 6
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END nao22_x1;

ARCHITECTURE behaviour_data_flow OF nao22_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nao22_x1"
  SEVERITY WARNING;
  nq <= not (((i0 or i1) and i2)) after 900 ps;
END;
```

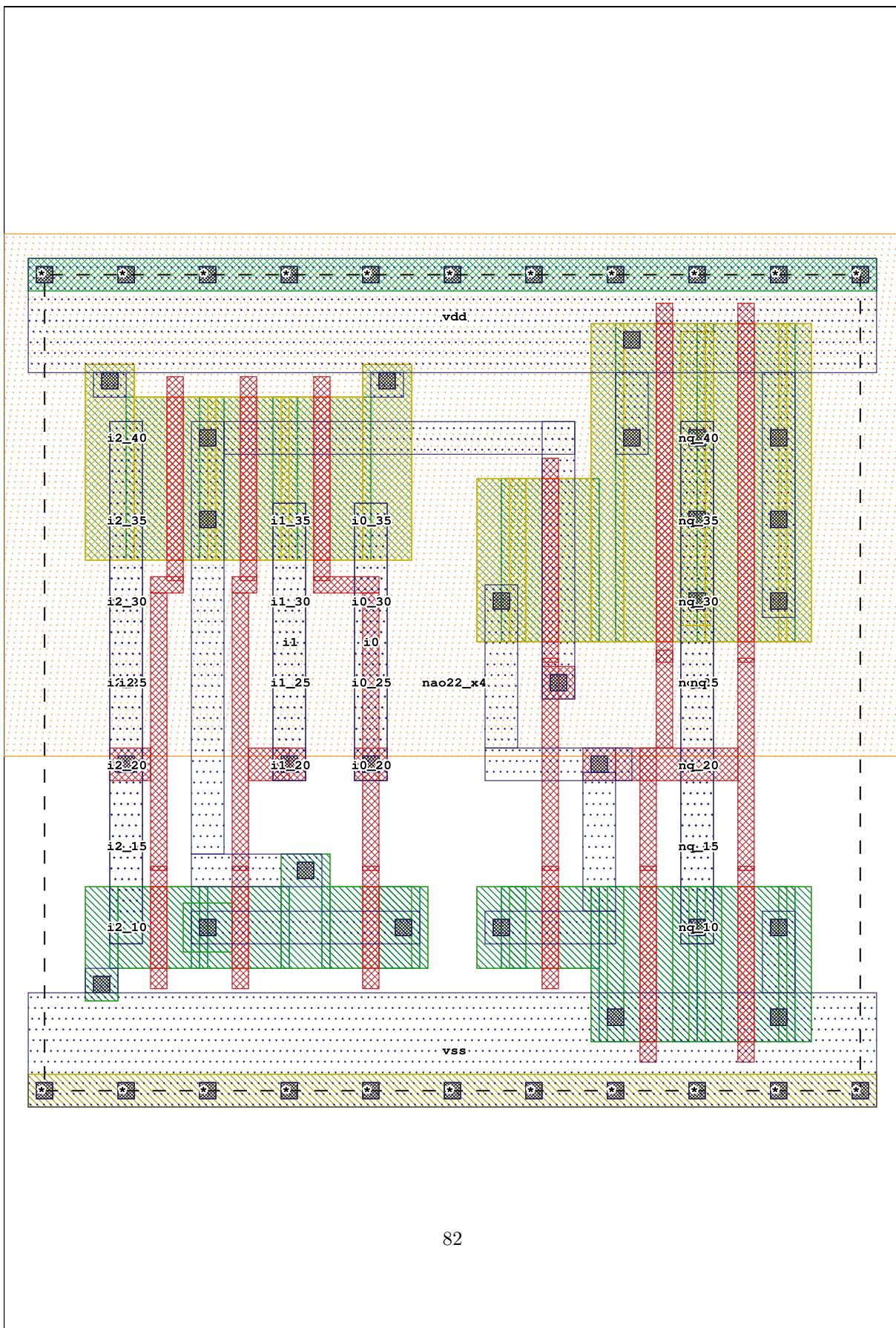


#### 4.31 nao22\_x4

```
ENTITY nao22_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2500;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rdown_i2_nq   : NATURAL := 810;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT rup_i2_nq     : NATURAL := 890;
    CONSTANT tphl_i2_nq    : NATURAL := 596;
    CONSTANT tphl_i2_nq    : NATURAL := 636;
    CONSTANT tphl_i0_nq    : NATURAL := 650;
    CONSTANT tphl_i1_nq    : NATURAL := 664;
    CONSTANT tphl_i1_nq    : NATURAL := 723;
    CONSTANT tphl_i0_nq    : NATURAL := 732;
    CONSTANT transistors   : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END nao22_x4;

ARCHITECTURE behaviour_data_flow OF nao22_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nao22_x4"
  SEVERITY WARNING;
  nq <= not (((i0 or i1) and i2)) after 1300 ps;
END;
```



### 4.32 nao2o22\_x1

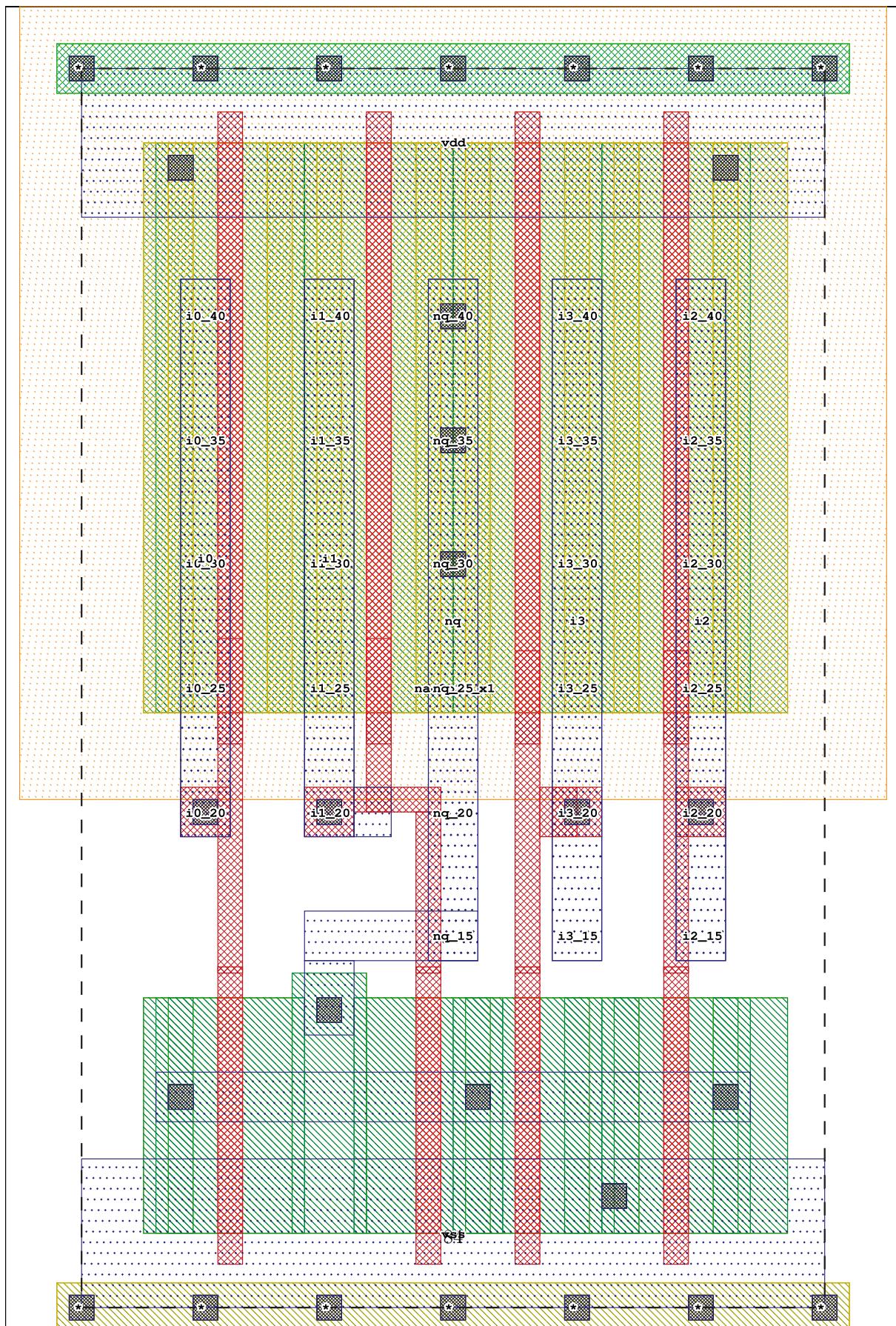
```

ENTITY nao2o22_x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 14;
    CONSTANT rdown_i0_nq    : NATURAL := 2850;
    CONSTANT rdown_i1_nq    : NATURAL := 2850;
    CONSTANT rdown_i2_nq    : NATURAL := 2850;
    CONSTANT rdown_i3_nq    : NATURAL := 2850;
    CONSTANT rup_i0_nq      : NATURAL := 3210;
    CONSTANT rup_i1_nq      : NATURAL := 3210;
    CONSTANT rup_i2_nq      : NATURAL := 3210;
    CONSTANT rup_i3_nq      : NATURAL := 3210;
    CONSTANT tphl_i3_nq     : NATURAL := 174;
    CONSTANT tphl_i1_nq     : NATURAL := 218;
    CONSTANT tphl_i0_nq     : NATURAL := 226;
    CONSTANT tphl_i2_nq     : NATURAL := 237;
    CONSTANT tplh_i1_nq     : NATURAL := 287;
    CONSTANT tplh_i0_nq     : NATURAL := 294;
    CONSTANT tplh_i2_nq     : NATURAL := 307;
    CONSTANT tplh_i3_nq     : NATURAL := 382;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END nao2o22_x1;

ARCHITECTURE behaviour_data_flow OF nao2o22_x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on nao2o22_x1"
        SEVERITY WARNING;
    nq <= not (((i0 or i1) and (i2 or i3))) after 1000 ps;
END;

```



### 4.33 nao2o22\_x4

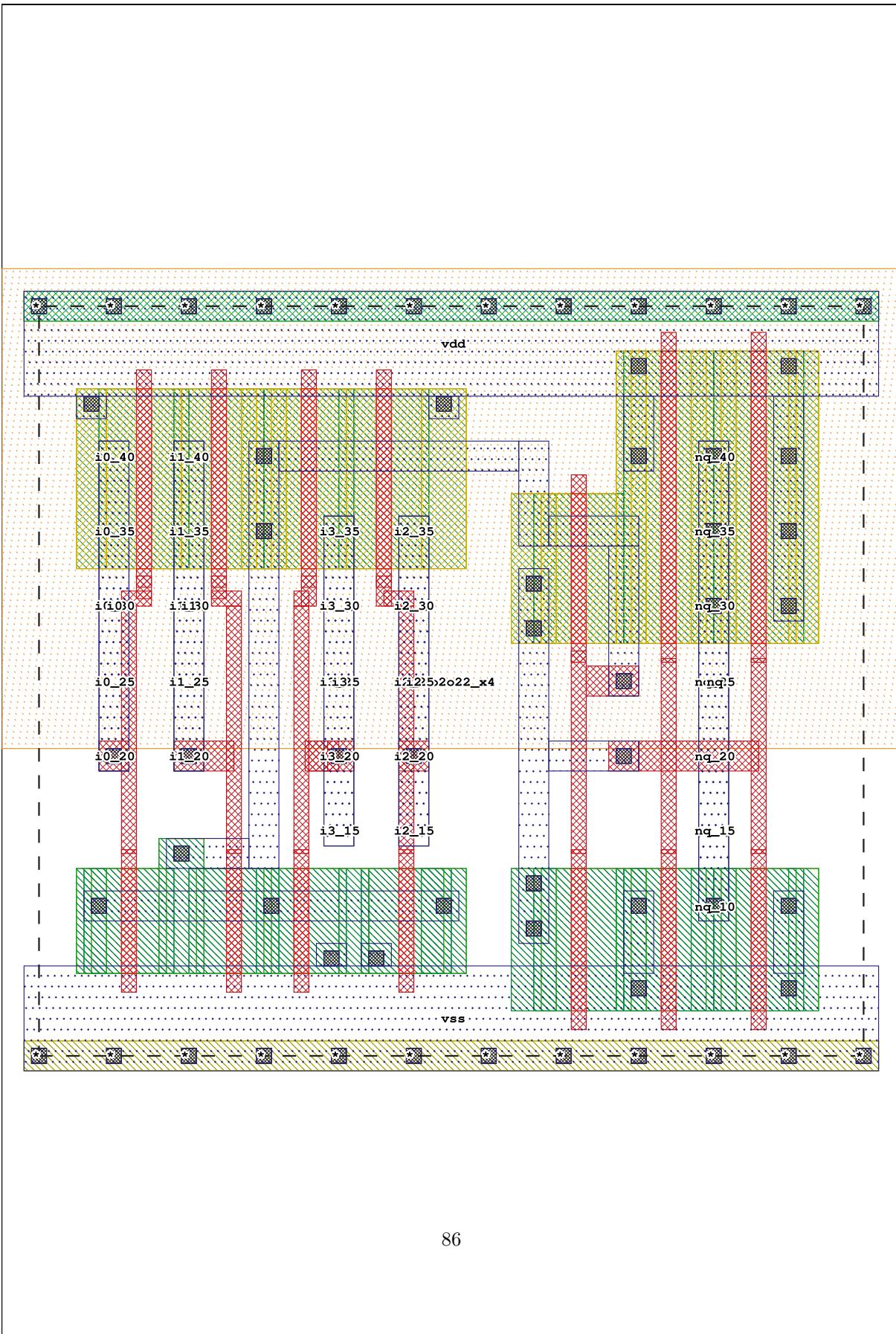
```

ENTITY nao2o22_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 2750;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT cin_i3         : NATURAL := 8;
    CONSTANT rdown_i0_nq    : NATURAL := 810;
    CONSTANT rdown_i1_nq    : NATURAL := 810;
    CONSTANT rdown_i2_nq    : NATURAL := 810;
    CONSTANT rdown_i3_nq    : NATURAL := 810;
    CONSTANT rup_i0_nq      : NATURAL := 890;
    CONSTANT rup_i1_nq      : NATURAL := 890;
    CONSTANT rup_i2_nq      : NATURAL := 890;
    CONSTANT rup_i3_nq      : NATURAL := 890;
    CONSTANT tphl_i3_nq     : NATURAL := 607;
    CONSTANT tplh_i0_nq     : NATURAL := 644;
    CONSTANT tplh_i2_nq     : NATURAL := 664;
    CONSTANT tplh_i1_nq     : NATURAL := 666;
    CONSTANT tplh_i1_nq     : NATURAL := 717;
    CONSTANT tplh_i2_nq     : NATURAL := 721;
    CONSTANT tplh_i0_nq     : NATURAL := 734;
    CONSTANT tplh_i3_nq     : NATURAL := 807;
    CONSTANT transistors    : NATURAL := 14
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END nao2o22_x4;

ARCHITECTURE behaviour_data_flow OF nao2o22_x4 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on nao2o22_x4"
        SEVERITY WARNING;
    nq <= not (((i0 or i1) and (i2 or i3))) after 1400 ps;
END;

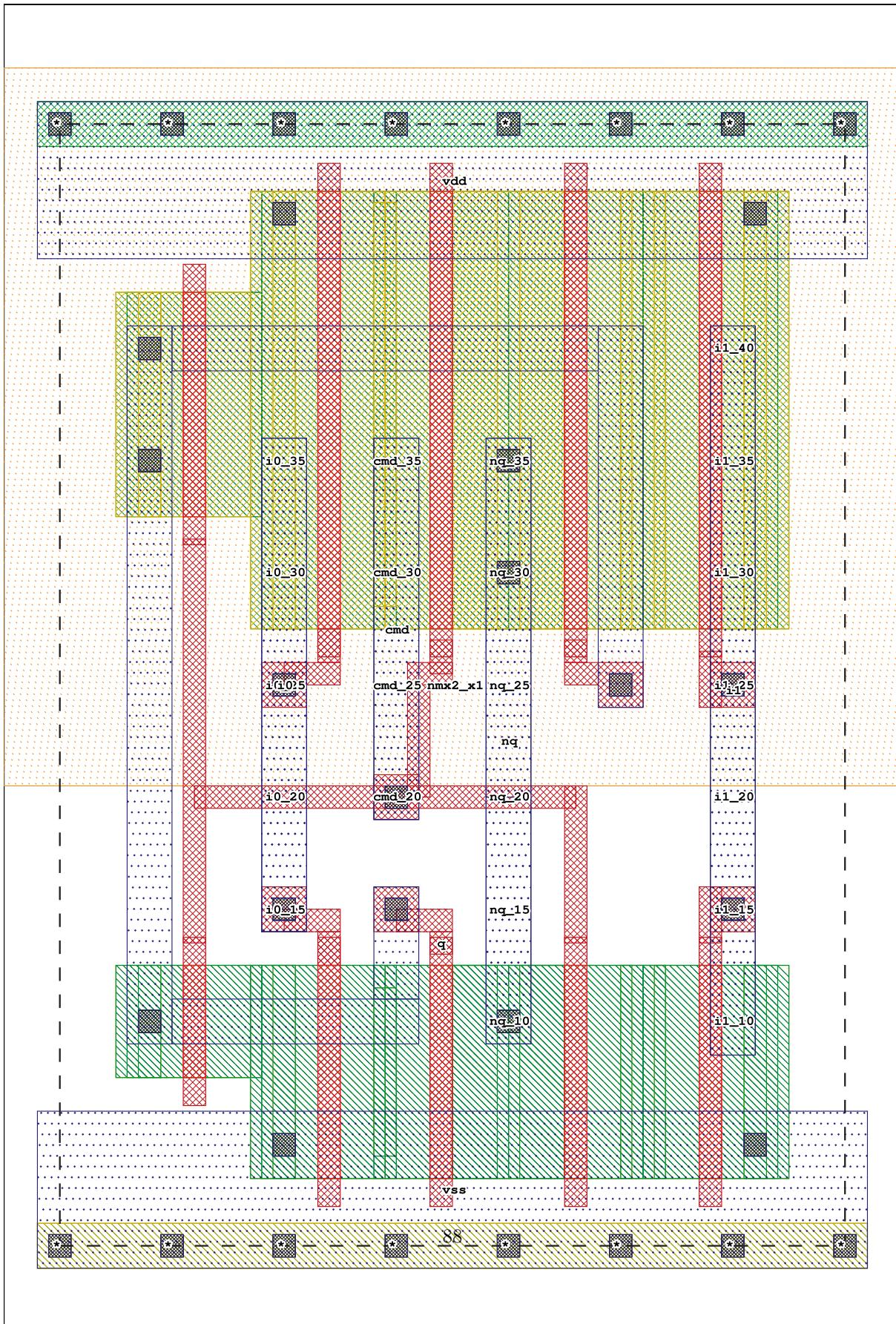
```



#### 4.34 nmx2\_x1

```
ENTITY nmx2_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_cmd       : NATURAL := 21;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT rdown_cmd_nq  : NATURAL := 2850;
    CONSTANT rdown_i0_nq   : NATURAL := 2850;
    CONSTANT rdown_i1_nq   : NATURAL := 2850;
    CONSTANT rup_cmd_nq   : NATURAL := 3210;
    CONSTANT rup_i0_nq     : NATURAL := 3210;
    CONSTANT rup_i1_nq     : NATURAL := 3210;
    CONSTANT tphl_i0_nq    : NATURAL := 217;
    CONSTANT tphl_i1_nq    : NATURAL := 217;
    CONSTANT tphl_cmd_nq   : NATURAL := 218;
    CONSTANT tplh_i0_nq    : NATURAL := 256;
    CONSTANT tplh_i1_nq    : NATURAL := 256;
    CONSTANT tplh_cmd_nq   : NATURAL := 287;
    CONSTANT tphh_cmd_nq   : NATURAL := 379;
    CONSTANT tpll_cmd_nq   : NATURAL := 410;
    CONSTANT transistors   : NATURAL := 10
  );
  PORT (
    cmd      : in  BIT;
    i0       : in  BIT;
    i1       : in  BIT;
    nq       : out BIT;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END nmx2_x1;

ARCHITECTURE behaviour_data_flow OF nmx2_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nmx2_x1"
    SEVERITY WARNING;
  nq <= not (((i0 and not (cmd)) or (i1 and cmd))) after 1000 ps;
END;
```

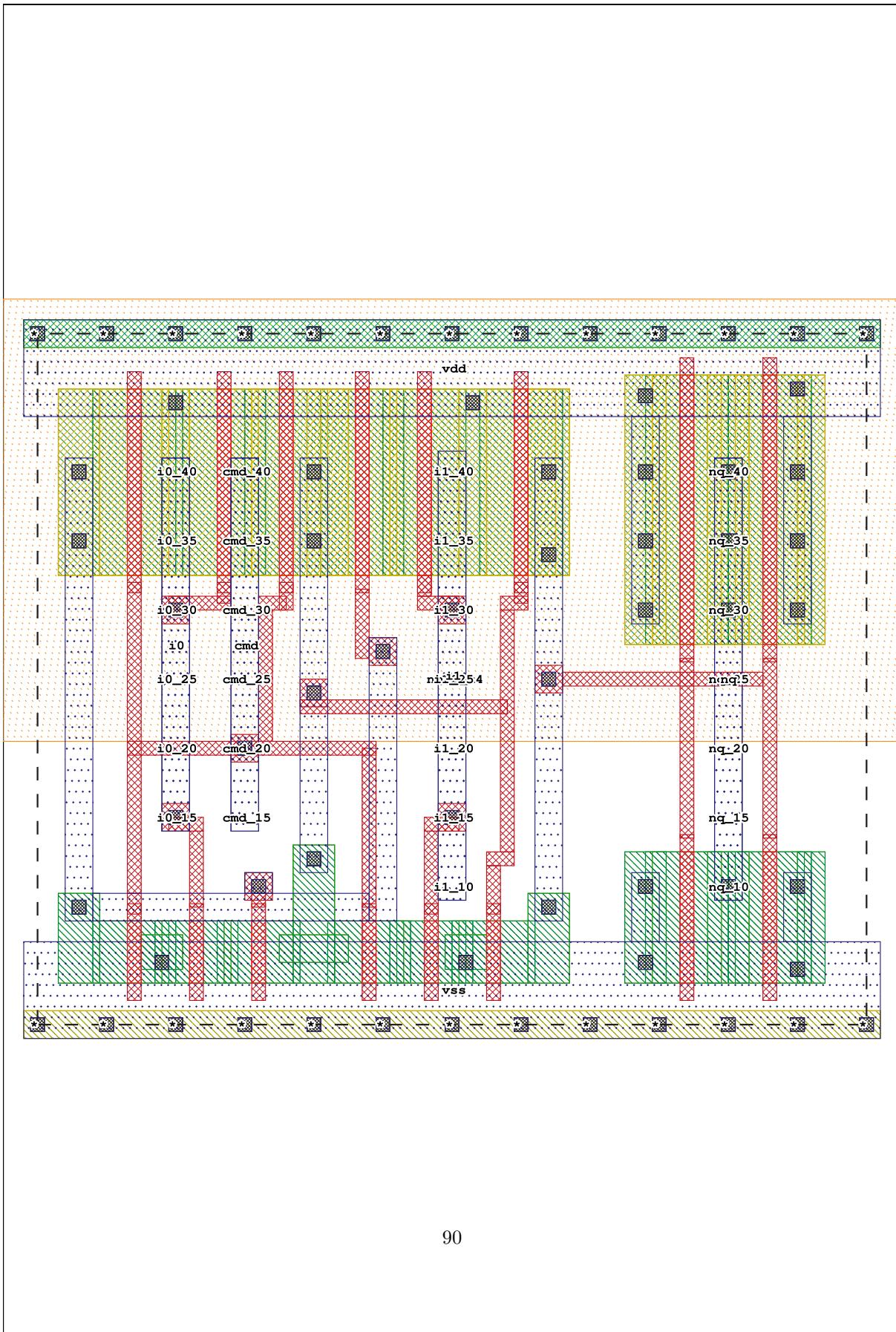


#### 4.35 nmx2\_x4

```
ENTITY nmx2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3000;
    CONSTANT cin_cmd       : NATURAL := 17;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT rdown_cmd_nq  : NATURAL := 810;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rup_cmd_nq    : NATURAL := 890;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT tphl_i0_nq    : NATURAL := 610;
    CONSTANT tphl_i1_nq    : NATURAL := 610;
    CONSTANT tphl_cmd_nq   : NATURAL := 632;
    CONSTANT tplh_i0_nq    : NATURAL := 653;
    CONSTANT tplh_i1_nq    : NATURAL := 653;
    CONSTANT tphh_cmd_nq   : NATURAL := 688;
    CONSTANT tpll_cmd_nq   : NATURAL := 703;
    CONSTANT tplh_cmd_nq   : NATURAL := 708;
    CONSTANT transistors   : NATURAL := 16
  );
  PORT (
    cmd      : in  BIT;
    i0       : in  BIT;
    i1       : in  BIT;
    nq       : out BIT;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END nmx2_x4;

ARCHITECTURE behaviour_data_flow OF nmx2_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nmx2_x4"
  SEVERITY WARNING;
  nq <= not (((i0 and not (cmd)) or (i1 and cmd))) after 1300 ps;
END;
```

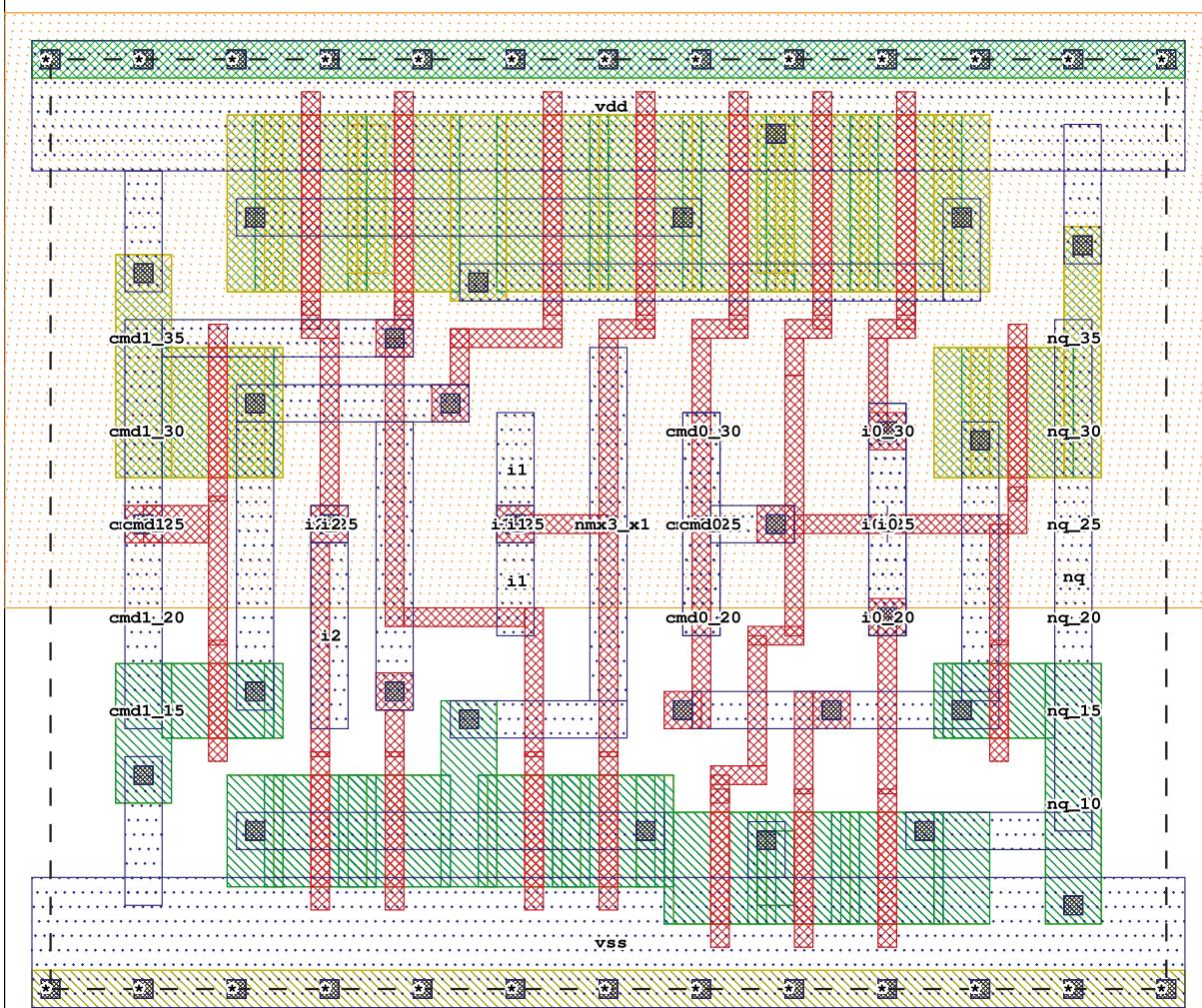


#### 4.36 nmx3\_x1

```
ENTITY nmx3_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3000;
    CONSTANT cin_cmd0      : NATURAL := 15;
    CONSTANT cin_cmd1      : NATURAL := 15;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT rdown_cmd0_nq : NATURAL := 7420;
    CONSTANT rdown_cmd1_nq : NATURAL := 7420;
    CONSTANT rdown_i0_nq   : NATURAL := 5140;
    CONSTANT rdown_i1_nq   : NATURAL := 7420;
    CONSTANT rdown_i2_nq   : NATURAL := 7420;
    CONSTANT rup_cmd0_nq   : NATURAL := 9760;
    CONSTANT rup_cmd1_nq   : NATURAL := 9760;
    CONSTANT rup_i0_nq     : NATURAL := 6680;
    CONSTANT rup_i1_nq     : NATURAL := 9760;
    CONSTANT rup_i2_nq     : NATURAL := 9760;
    CONSTANT tphl_i0_nq    : NATURAL := 315;
    CONSTANT tphl_cmd0_nq  : NATURAL := 356;
    CONSTANT tphl_cmd1_nq  : NATURAL := 414;
    CONSTANT tphl_i1_nq    : NATURAL := 429;
    CONSTANT tphl_i2_nq    : NATURAL := 429;
    CONSTANT tphy_i0_nq    : NATURAL := 441;
    CONSTANT tphy_cmd0_nq  : NATURAL := 495;
    CONSTANT tphy_cmd1_nq  : NATURAL := 519;
    CONSTANT tphy_i1_nq    : NATURAL := 520;
    CONSTANT tphy_i2_nq    : NATURAL := 566;
    CONSTANT tphy_cmd0_nq  : NATURAL := 582;
    CONSTANT tphy_i1_nq    : NATURAL := 582;
    CONSTANT tphy_i2_nq    : NATURAL := 582;
    CONSTANT tphy_cmd0_nq  : NATURAL := 586;
    CONSTANT transistors   : NATURAL := 18
  );
  PORT (
    cmd0   : in  BIT;
    cmd1   : in  BIT;
    i0     : in  BIT;
    i1     : in  BIT;
    i2     : in  BIT;
    nq     : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END nmx3_x1;
```

```
ARCHITECTURE behaviour_data_flow OF nmx3_x1 IS
```

```
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on nmx3_x1"
    SEVERITY WARNING;
    nq <= not (((not (cmd0) and i0) or (cmd0 and ((cmd1 and i1) or (not
        (cmd1) and i2))))) after 1200 ps;
END;
```

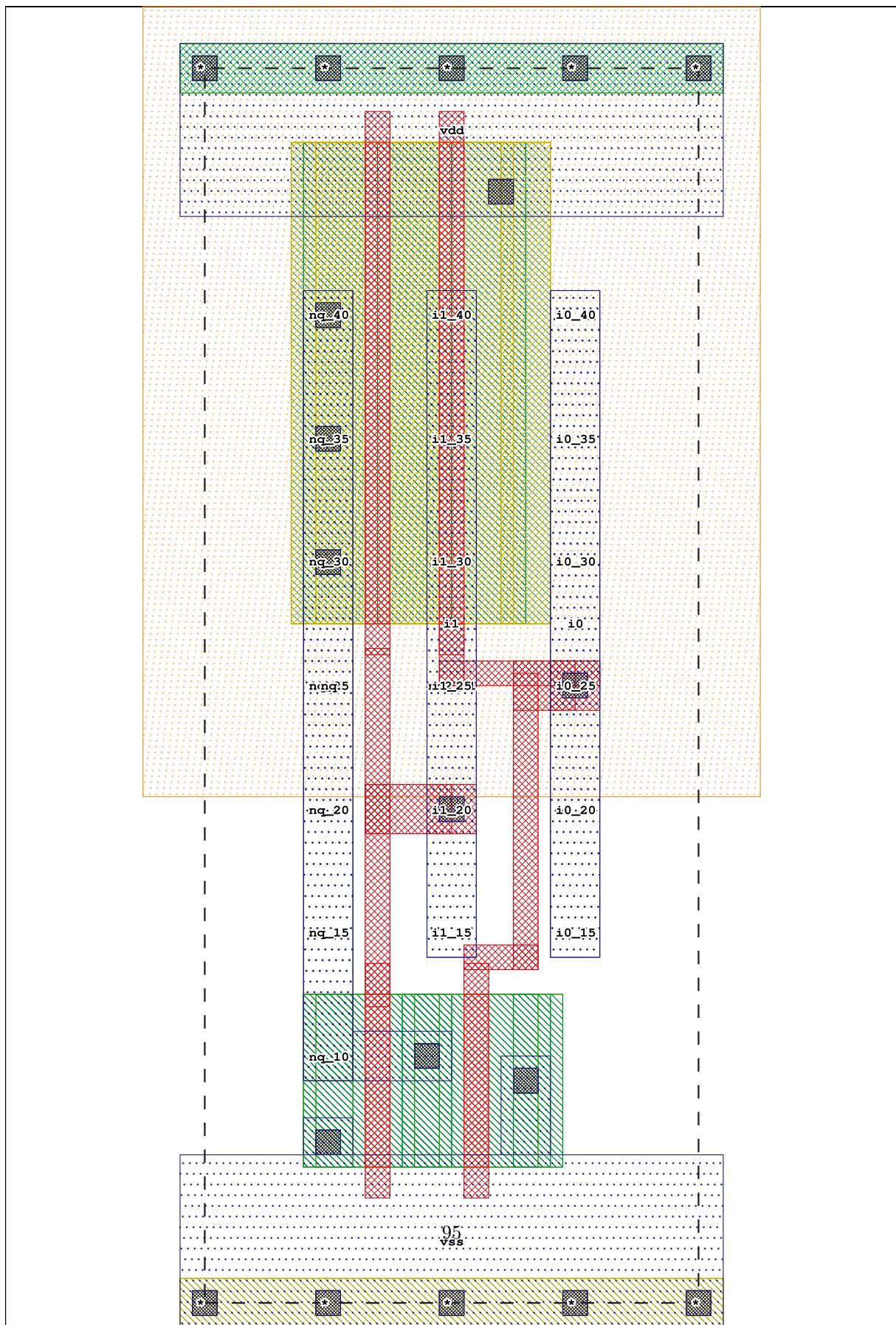


#### 4.37 no2\_x1

```
ENTITY no2_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1000;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 12;
    CONSTANT rdown_i0_nq   : NATURAL := 3640;
    CONSTANT rdown_i1_nq   : NATURAL := 3640;
    CONSTANT rup_i0_nq     : NATURAL := 3210;
    CONSTANT rup_i1_nq     : NATURAL := 3210;
    CONSTANT tplh_i0_nq    : NATURAL := 121;
    CONSTANT tplh_i1_nq    : NATURAL := 161;
    CONSTANT tphl_i1_nq    : NATURAL := 193;
    CONSTANT tphl_i0_nq    : NATURAL := 298;
    CONSTANT transistors   : NATURAL := 4
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END no2_x1;

ARCHITECTURE behaviour_data_flow OF no2_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on no2_x1"
  SEVERITY WARNING;
  nq <= not ((i0 or i1)) after 900 ps;
END;
```

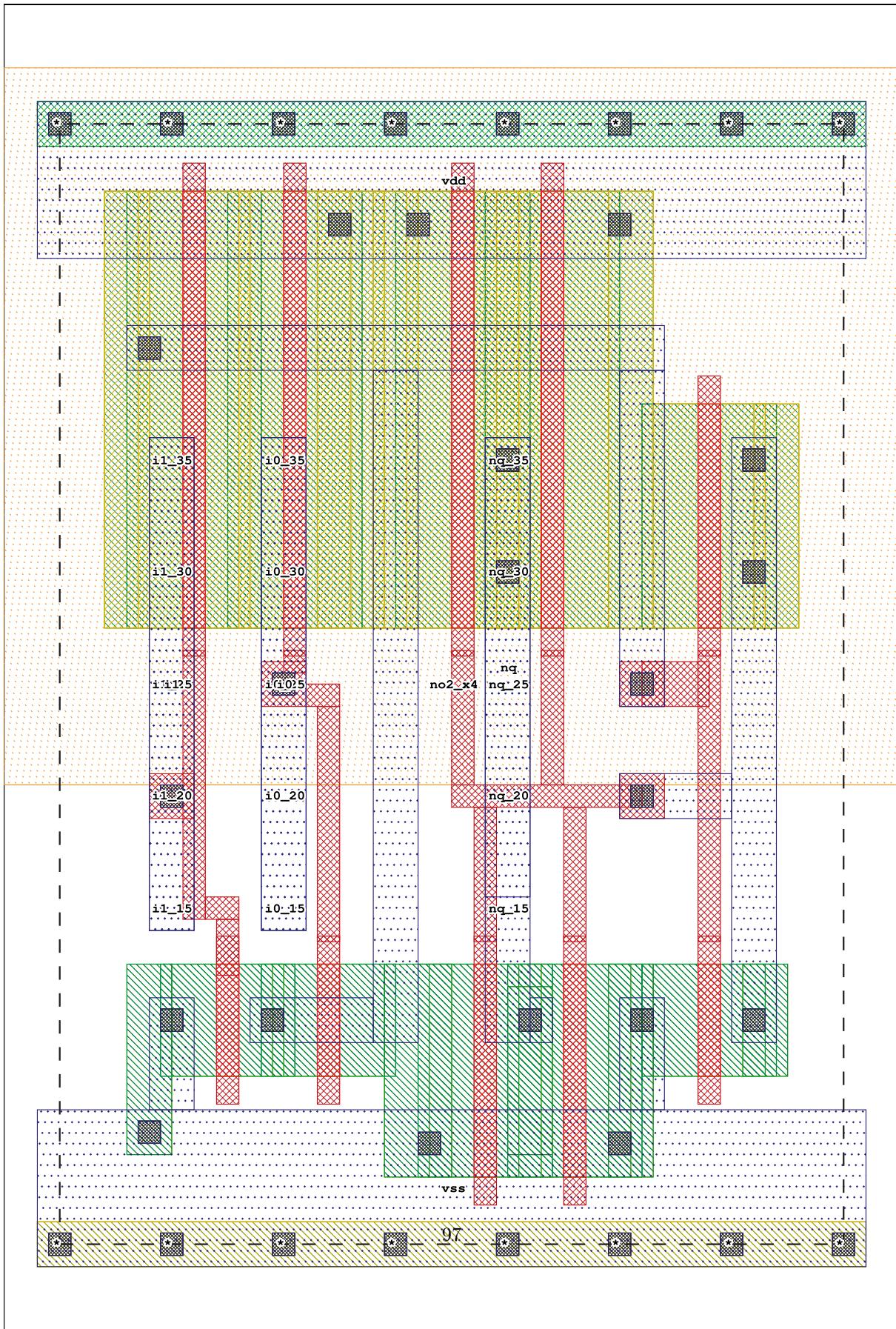


#### 4.38 no2\_x4

```
ENTITY no2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT tplh_i0_nq    : NATURAL := 447;
    CONSTANT tplh_i1_nq    : NATURAL := 504;
    CONSTANT tphl_i1_nq    : NATURAL := 522;
    CONSTANT tphl_i0_nq    : NATURAL := 618;
    CONSTANT transistors   : NATURAL := 10
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END no2_x4;

ARCHITECTURE behaviour_data_flow OF no2_x4 IS

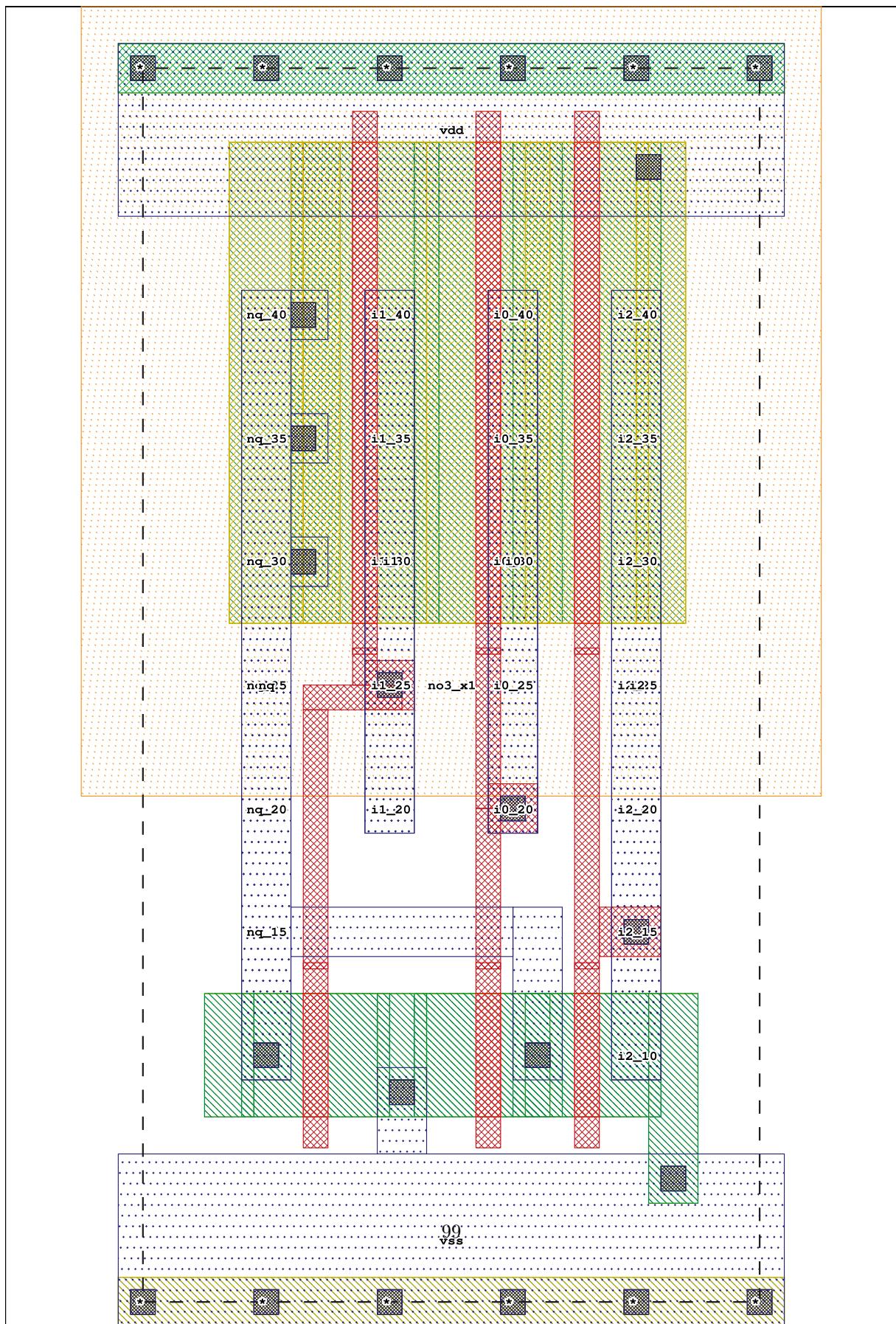
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on no2_x4"
  SEVERITY WARNING;
  nq <= not ((i0 or i1)) after 1200 ps;
END;
```



#### 4.39 no3\_x1

```
ENTITY no3_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1250;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 12;
    CONSTANT cin_i2         : NATURAL := 12;
    CONSTANT rdown_i0_nq   : NATURAL := 3640;
    CONSTANT rdown_i1_nq   : NATURAL := 3640;
    CONSTANT rdown_i2_nq   : NATURAL := 3640;
    CONSTANT rup_i0_nq     : NATURAL := 4690;
    CONSTANT rup_i1_nq     : NATURAL := 4690;
    CONSTANT rup_i2_nq     : NATURAL := 4690;
    CONSTANT tplh_i2_nq    : NATURAL := 192;
    CONSTANT tphl_i1_nq    : NATURAL := 215;
    CONSTANT tphl_i1_nq    : NATURAL := 243;
    CONSTANT tphl_i0_nq    : NATURAL := 246;
    CONSTANT tphl_i0_nq    : NATURAL := 318;
    CONSTANT tphl_i2_nq    : NATURAL := 407;
    CONSTANT transistors   : NATURAL := 6
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END no3_x1;
```

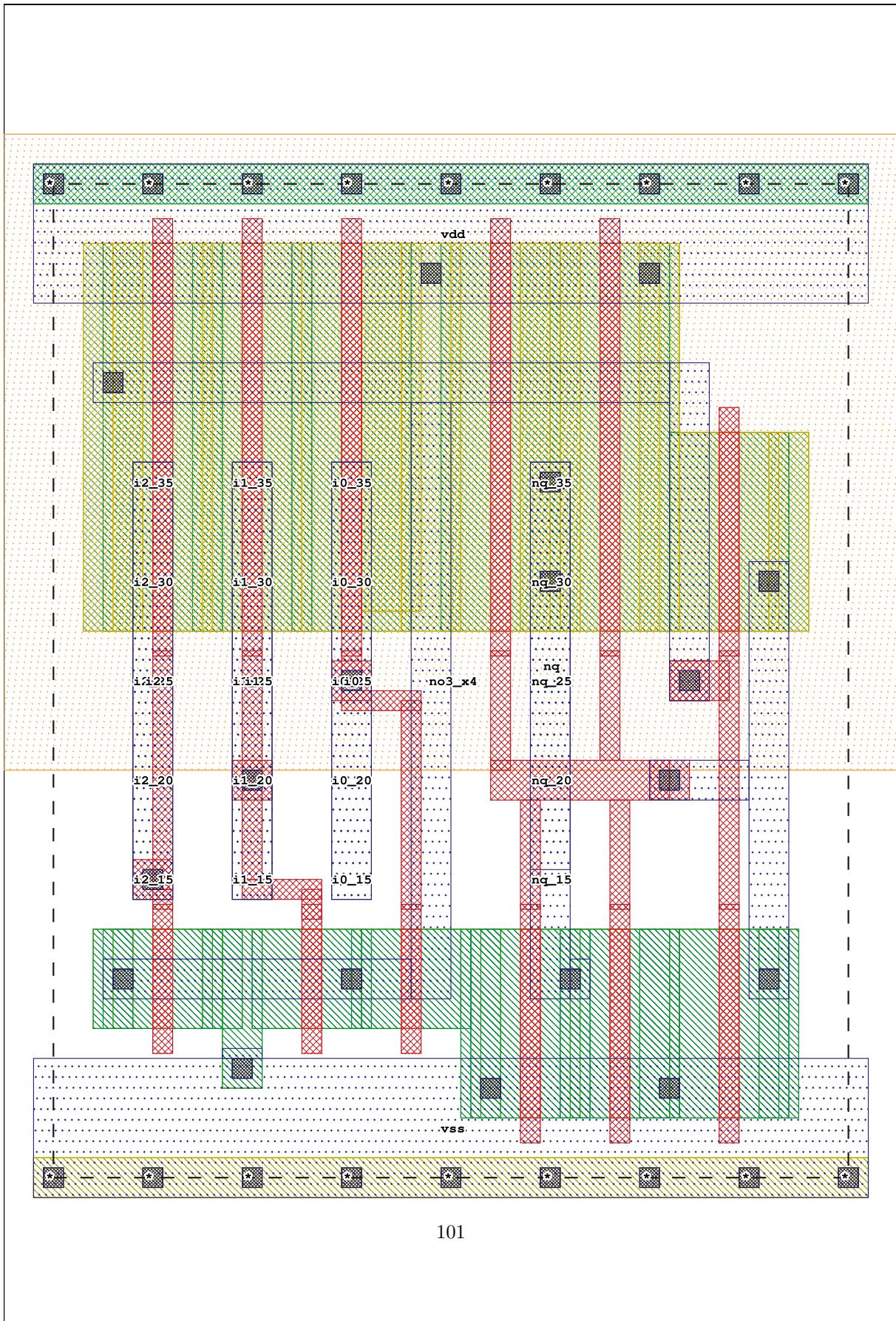
```
ARCHITECTURE behaviour_data_flow OF no3_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on no3_x1"
  SEVERITY WARNING;
  nq <= not (((i0 or i1) or i2)) after 1000 ps;
END;
```



#### 4.40 no3\_x4

```
ENTITY no3_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 12;
    CONSTANT cin_i2         : NATURAL := 11;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rdown_i2_nq   : NATURAL := 810;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT rup_i2_nq     : NATURAL := 890;
    CONSTANT tphl_i2_nq    : NATURAL := 545;
    CONSTANT tphl_i0_nq    : NATURAL := 561;
    CONSTANT tphl_i1_nq    : NATURAL := 623;
    CONSTANT tphl_i1_nq    : NATURAL := 638;
    CONSTANT tphl_i2_nq    : NATURAL := 640;
    CONSTANT tphl_i0_nq    : NATURAL := 722;
    CONSTANT transistors   : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END no3_x4;
```

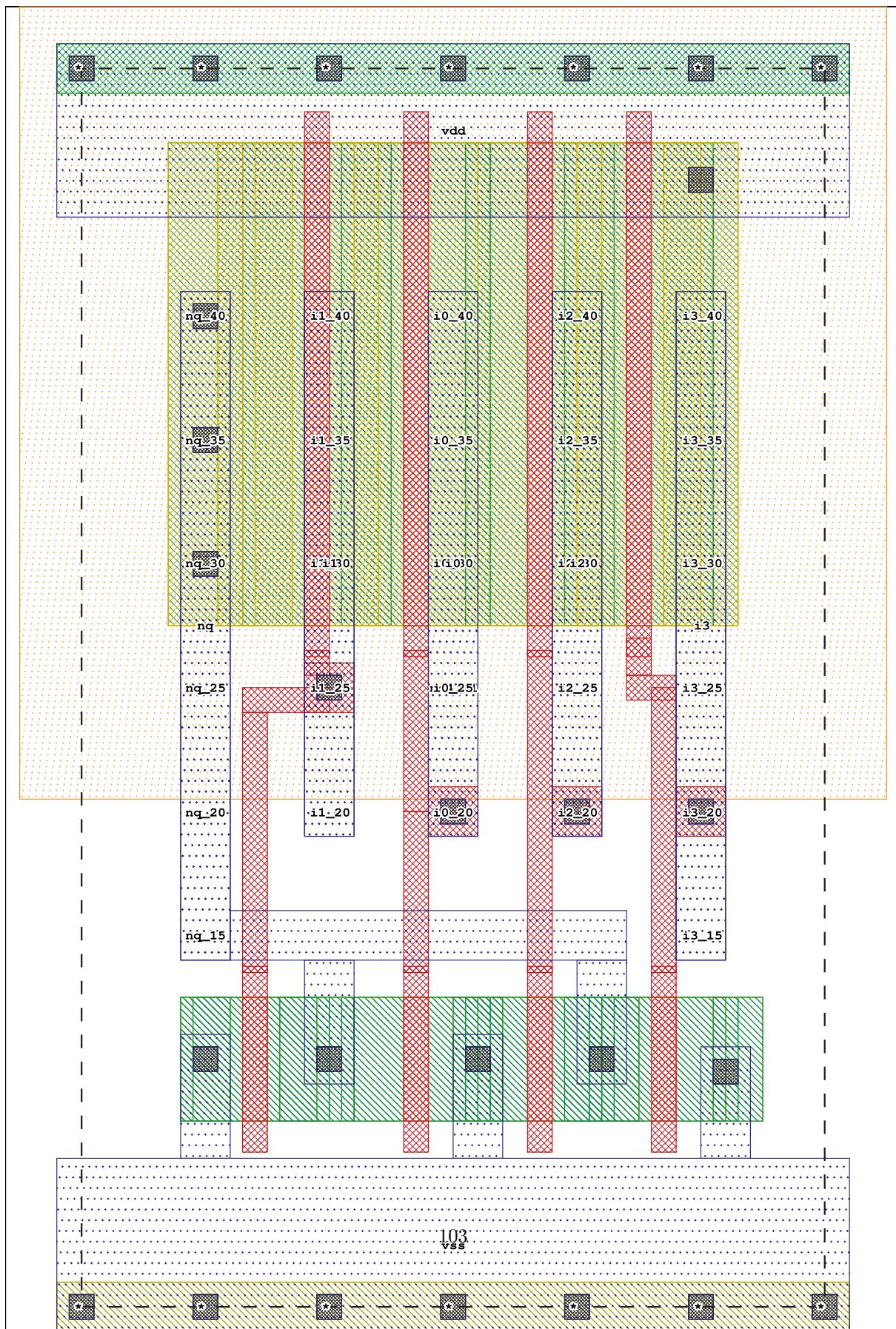
```
ARCHITECTURE behaviour_data_flow OF no3_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on no3_x4"
  SEVERITY WARNING;
  nq <= not (((i0 or i1) or i2)) after 1300 ps;
END;
```



#### 4.41 no4\_x1

```
ENTITY no4_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 12;
    CONSTANT cin_i2         : NATURAL := 12;
    CONSTANT cin_i3         : NATURAL := 12;
    CONSTANT rdown_i0_nq    : NATURAL := 3640;
    CONSTANT rdown_i1_nq    : NATURAL := 3640;
    CONSTANT rdown_i2_nq    : NATURAL := 3640;
    CONSTANT rdown_i3_nq    : NATURAL := 3640;
    CONSTANT rup_i0_nq      : NATURAL := 6190;
    CONSTANT rup_i1_nq      : NATURAL := 6190;
    CONSTANT rup_i2_nq      : NATURAL := 6190;
    CONSTANT rup_i3_nq      : NATURAL := 6190;
    CONSTANT tphl_i1_nq     : NATURAL := 230;
    CONSTANT tphl_i3_nq     : NATURAL := 271;
    CONSTANT tphl_i1_nq     : NATURAL := 320;
    CONSTANT tphl_i0_nq     : NATURAL := 330;
    CONSTANT tphl_i2_nq     : NATURAL := 333;
    CONSTANT tphl_i0_nq     : NATURAL := 340;
    CONSTANT tphl_i2_nq     : NATURAL := 419;
    CONSTANT tphl_i3_nq     : NATURAL := 499;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END no4_x1;

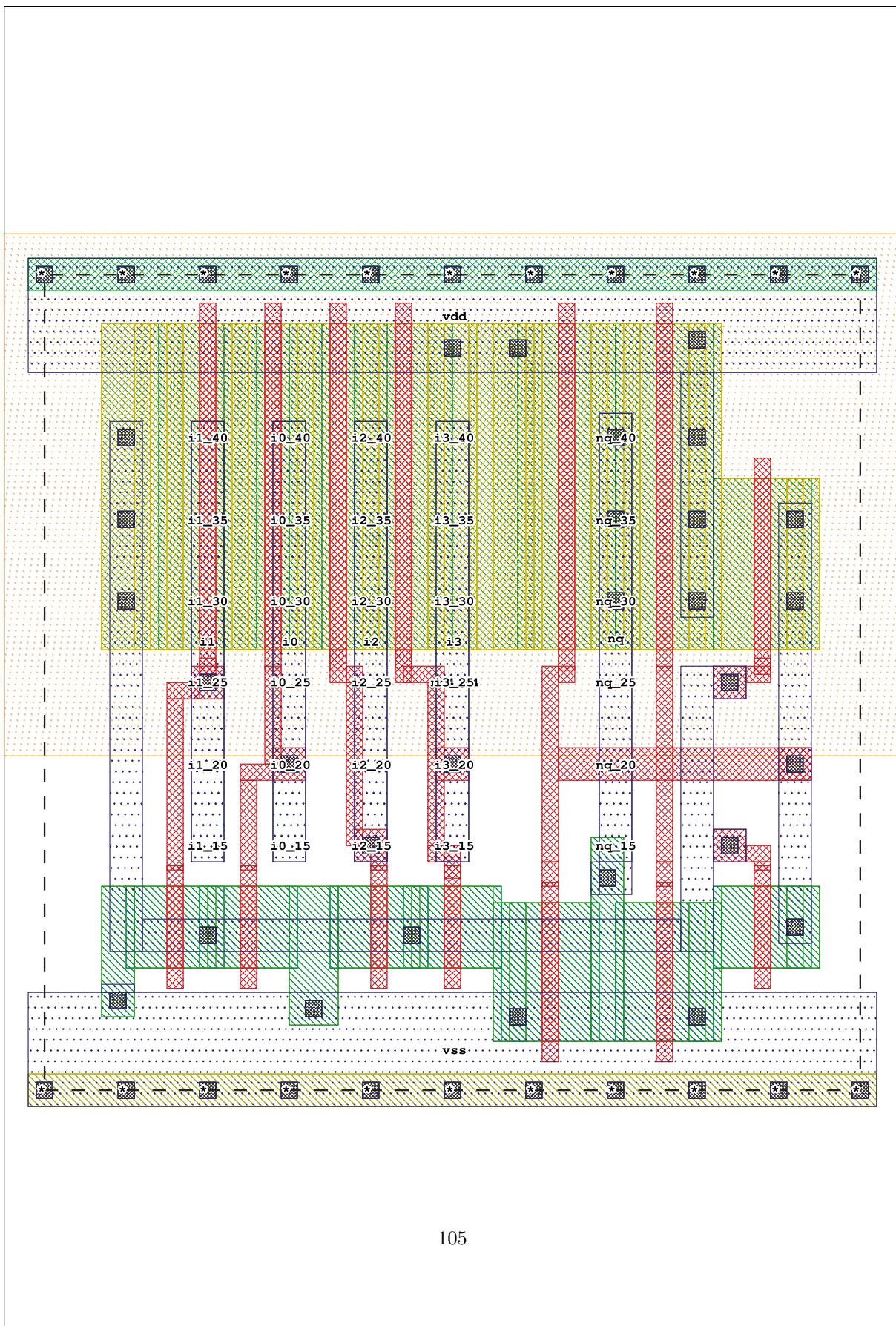
ARCHITECTURE behaviour_data_flow OF no4_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on no4_x1"
  SEVERITY WARNING;
  nq <= not (((i0 or i1) or i2) or i3)) after 1100 ps;
END;
```



#### 4.42 no4\_x4

```
ENTITY no4_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2500;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 12;
    CONSTANT cin_i2         : NATURAL := 12;
    CONSTANT cin_i3         : NATURAL := 12;
    CONSTANT rdown_i0_nq    : NATURAL := 810;
    CONSTANT rdown_i1_nq    : NATURAL := 810;
    CONSTANT rdown_i2_nq    : NATURAL := 810;
    CONSTANT rdown_i3_nq    : NATURAL := 810;
    CONSTANT rup_i0_nq      : NATURAL := 890;
    CONSTANT rup_i1_nq      : NATURAL := 890;
    CONSTANT rup_i2_nq      : NATURAL := 890;
    CONSTANT rup_i3_nq      : NATURAL := 890;
    CONSTANT tphl_i1_nq     : NATURAL := 564;
    CONSTANT tphl_i0_nq     : NATURAL := 656;
    CONSTANT tphl_i3_nq     : NATURAL := 693;
    CONSTANT tphl_i2_nq     : NATURAL := 739;
    CONSTANT tplh_i2_nq     : NATURAL := 761;
    CONSTANT tplh_i1_nq     : NATURAL := 768;
    CONSTANT tplh_i0_nq     : NATURAL := 777;
    CONSTANT tphl_i3_nq     : NATURAL := 816;
    CONSTANT transistors    : NATURAL := 14
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END no4_x4;

ARCHITECTURE behaviour_data_flow OF no4_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on no4_x4"
  SEVERITY WARNING;
  nq <= not (((i0 or i1) or i2) or i3)) after 1400 ps;
END;
```

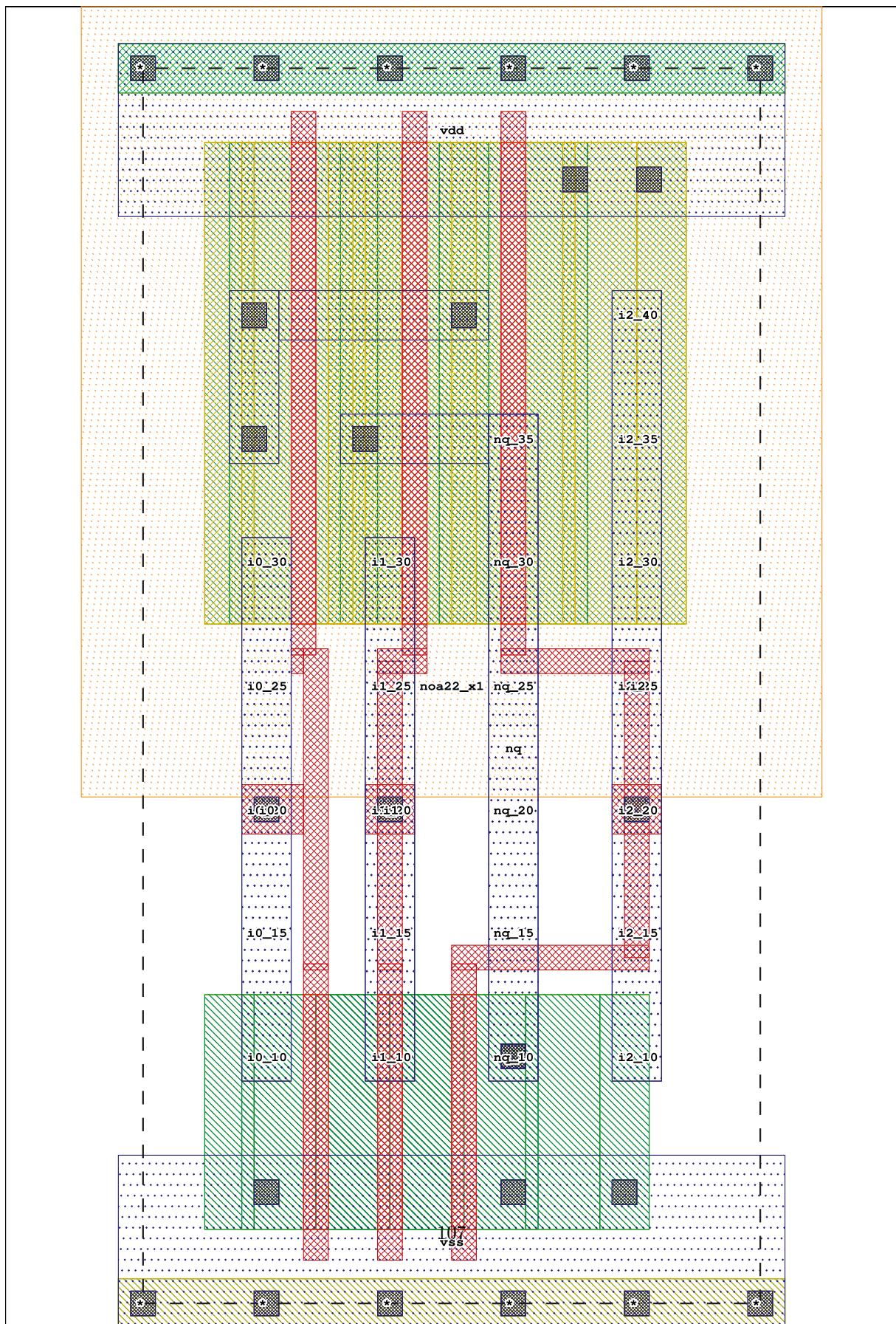


#### 4.43 noa22\_x1

```
ENTITY noa22_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 15;
    CONSTANT rdown_i0_nq   : NATURAL := 2850;
    CONSTANT rdown_i1_nq   : NATURAL := 2850;
    CONSTANT rdown_i2_nq   : NATURAL := 1620;
    CONSTANT rup_i0_nq     : NATURAL := 3210;
    CONSTANT rup_i1_nq     : NATURAL := 3210;
    CONSTANT rup_i2_nq     : NATURAL := 3210;
    CONSTANT tphl_i0_nq    : NATURAL := 151;
    CONSTANT tphl_i1_nq    : NATURAL := 218;
    CONSTANT tphl_i2_nq    : NATURAL := 218;
    CONSTANT tplh_i2_nq    : NATURAL := 241;
    CONSTANT tplh_i1_nq    : NATURAL := 287;
    CONSTANT tplh_i0_nq    : NATURAL := 327;
    CONSTANT transistors   : NATURAL := 6
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END noa22_x1;
```

```
ARCHITECTURE behaviour_data_flow OF noa22_x1 IS
```

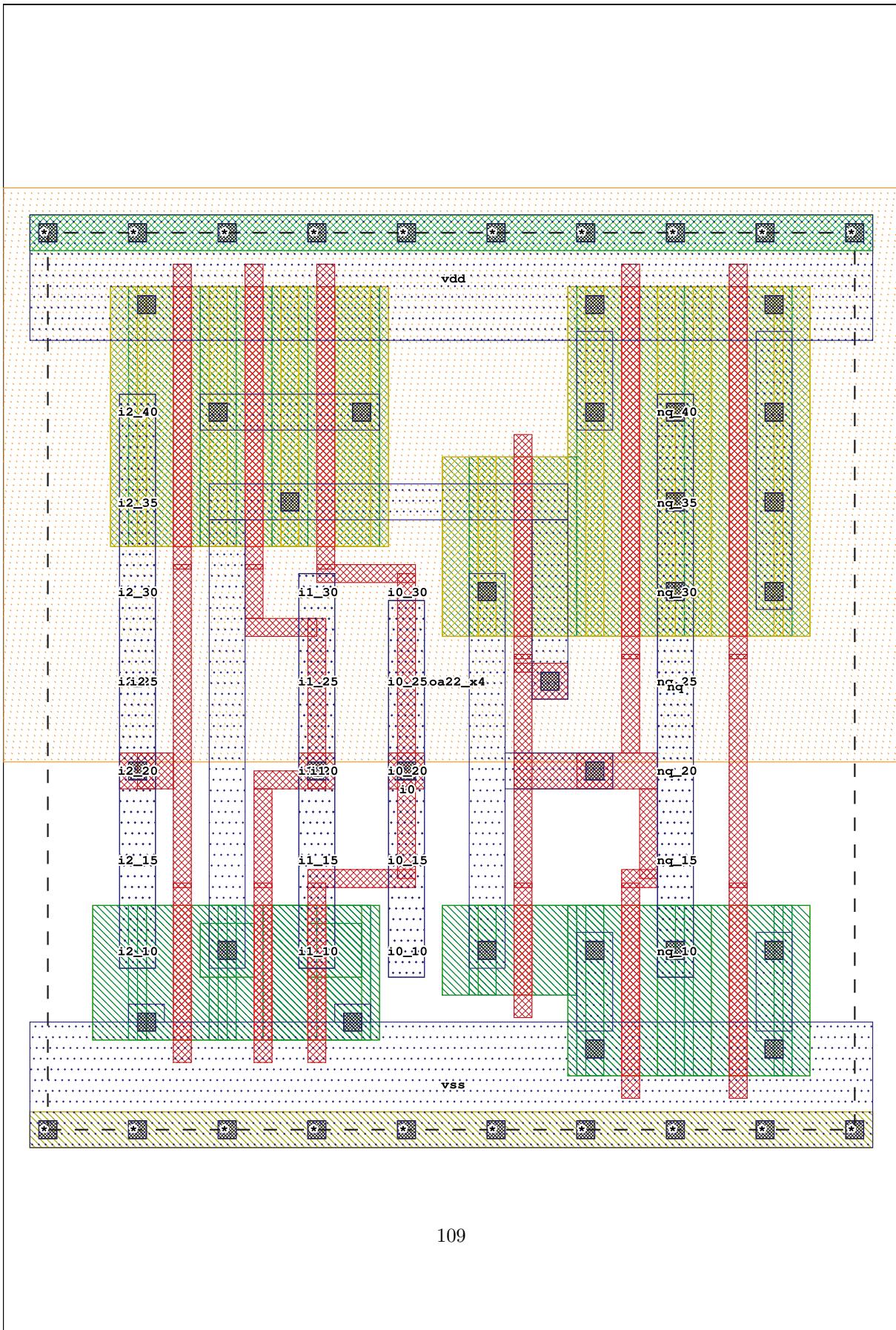
```
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa22_x1"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) or i2)) after 900 ps;
END;
```



#### 4.44 noa22\_x4

```
ENTITY noa22_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2500;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rdown_i2_nq   : NATURAL := 810;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT rup_i2_nq     : NATURAL := 890;
    CONSTANT tphl_i0_nq    : NATURAL := 550;
    CONSTANT tphl_i1_nq    : NATURAL := 610;
    CONSTANT tphl_i2_nq    : NATURAL := 643;
    CONSTANT tplh_i2_nq    : NATURAL := 646;
    CONSTANT tplh_i1_nq    : NATURAL := 709;
    CONSTANT tplh_i0_nq    : NATURAL := 740;
    CONSTANT transistors   : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END noa22_x4;
```

```
ARCHITECTURE behaviour_data_flow OF noa22_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa22_x4"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) or i2)) after 1300 ps;
END;
```



#### 4.45 noa2a22\_x1

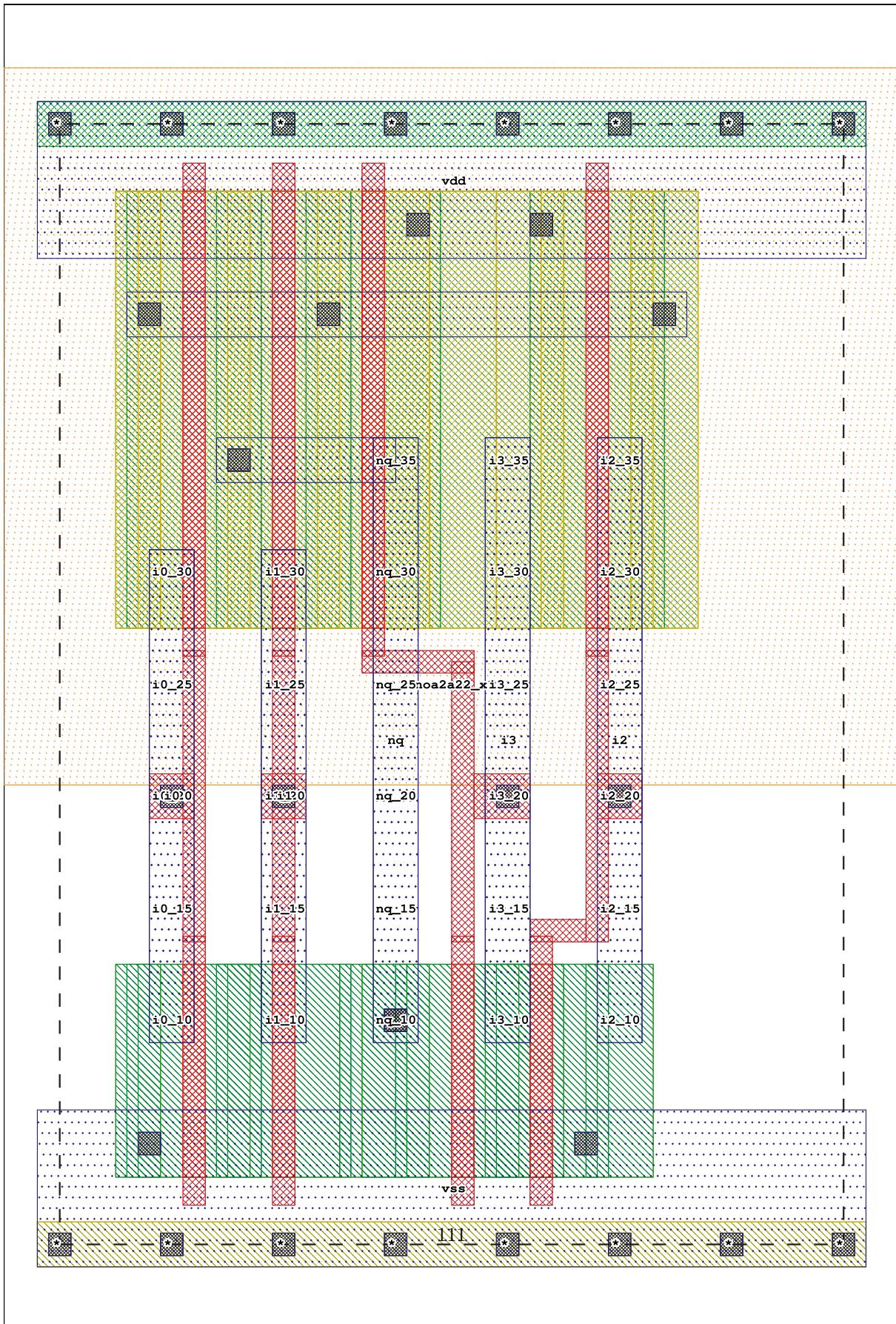
```

ENTITY noa2a22_x1 IS
GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 14;
    CONSTANT rdown_i0_nq    : NATURAL := 2850;
    CONSTANT rdown_i1_nq    : NATURAL := 2850;
    CONSTANT rdown_i2_nq    : NATURAL := 2850;
    CONSTANT rdown_i3_nq    : NATURAL := 2850;
    CONSTANT rup_i0_nq      : NATURAL := 3210;
    CONSTANT rup_i1_nq      : NATURAL := 3210;
    CONSTANT rup_i2_nq      : NATURAL := 3210;
    CONSTANT rup_i3_nq      : NATURAL := 3210;
    CONSTANT tphl_i0_nq     : NATURAL := 151;
    CONSTANT tphl_i1_nq     : NATURAL := 218;
    CONSTANT tphl_i3_nq     : NATURAL := 256;
    CONSTANT tphl_i2_nq     : NATURAL := 284;
    CONSTANT tplh_i1_nq     : NATURAL := 287;
    CONSTANT tplh_i2_nq     : NATURAL := 289;
    CONSTANT tplh_i0_nq     : NATURAL := 327;
    CONSTANT tplh_i3_nq     : NATURAL := 372;
    CONSTANT transistors    : NATURAL := 8
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END noa2a22_x1;

ARCHITECTURE behaviour_data_flow OF noa2a22_x1 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on noa2a22_x1"
        SEVERITY WARNING;
    nq <= not (((i0 and i1) or (i2 and i3))) after 1000 ps;
END;

```

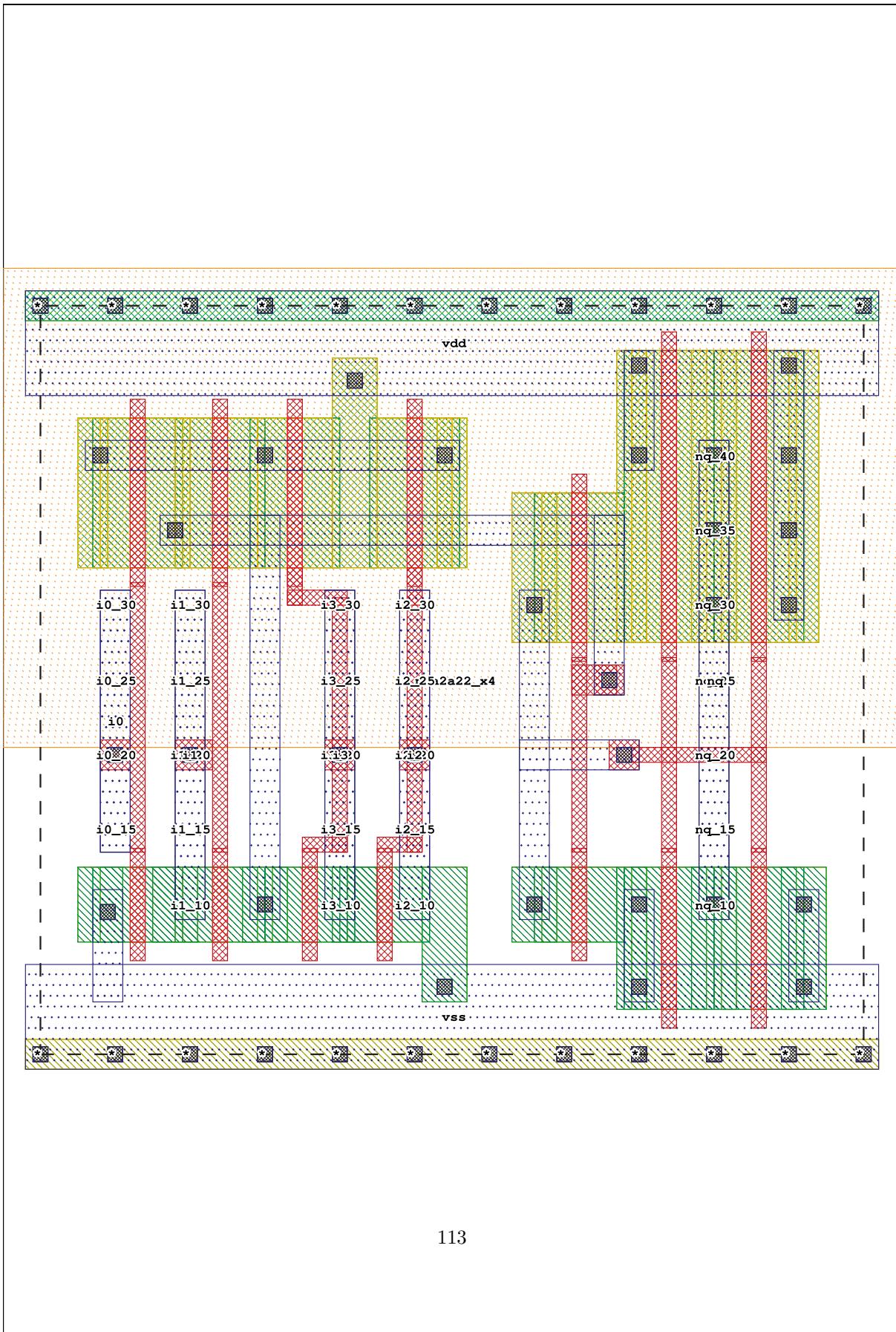


#### 4.46 noa2a22\_x4

```
ENTITY noa2a22_x4 IS
  GENERIC (
    CONSTANT area : NATURAL := 2750;
    CONSTANT cin_i0 : NATURAL := 8;
    CONSTANT cin_i1 : NATURAL := 8;
    CONSTANT cin_i2 : NATURAL := 8;
    CONSTANT cin_i3 : NATURAL := 8;
    CONSTANT rdown_i0_nq : NATURAL := 810;
    CONSTANT rdown_i1_nq : NATURAL := 810;
    CONSTANT rdown_i2_nq : NATURAL := 810;
    CONSTANT rdown_i3_nq : NATURAL := 810;
    CONSTANT rup_i0_nq : NATURAL := 890;
    CONSTANT rup_i1_nq : NATURAL := 890;
    CONSTANT rup_i2_nq : NATURAL := 890;
    CONSTANT rup_i3_nq : NATURAL := 890;
    CONSTANT tphl_i0_nq : NATURAL := 562;
    CONSTANT tphl_i1_nq : NATURAL := 646;
    CONSTANT tphl_i3_nq : NATURAL := 677;
    CONSTANT tphl_i2_nq : NATURAL := 701;
    CONSTANT tphl_i2_nq : NATURAL := 703;
    CONSTANT tphl_i1_nq : NATURAL := 714;
    CONSTANT tphl_i0_nq : NATURAL := 745;
    CONSTANT tphl_i3_nq : NATURAL := 805;
    CONSTANT transistors : NATURAL := 14
  );
  PORT (
    i0 : in BIT;
    i1 : in BIT;
    i2 : in BIT;
    i3 : in BIT;
    nq : out BIT;
    vdd : in BIT;
    vss : in BIT
  );
END noa2a22_x4;

ARCHITECTURE behaviour_data_flow OF noa2a22_x4 IS

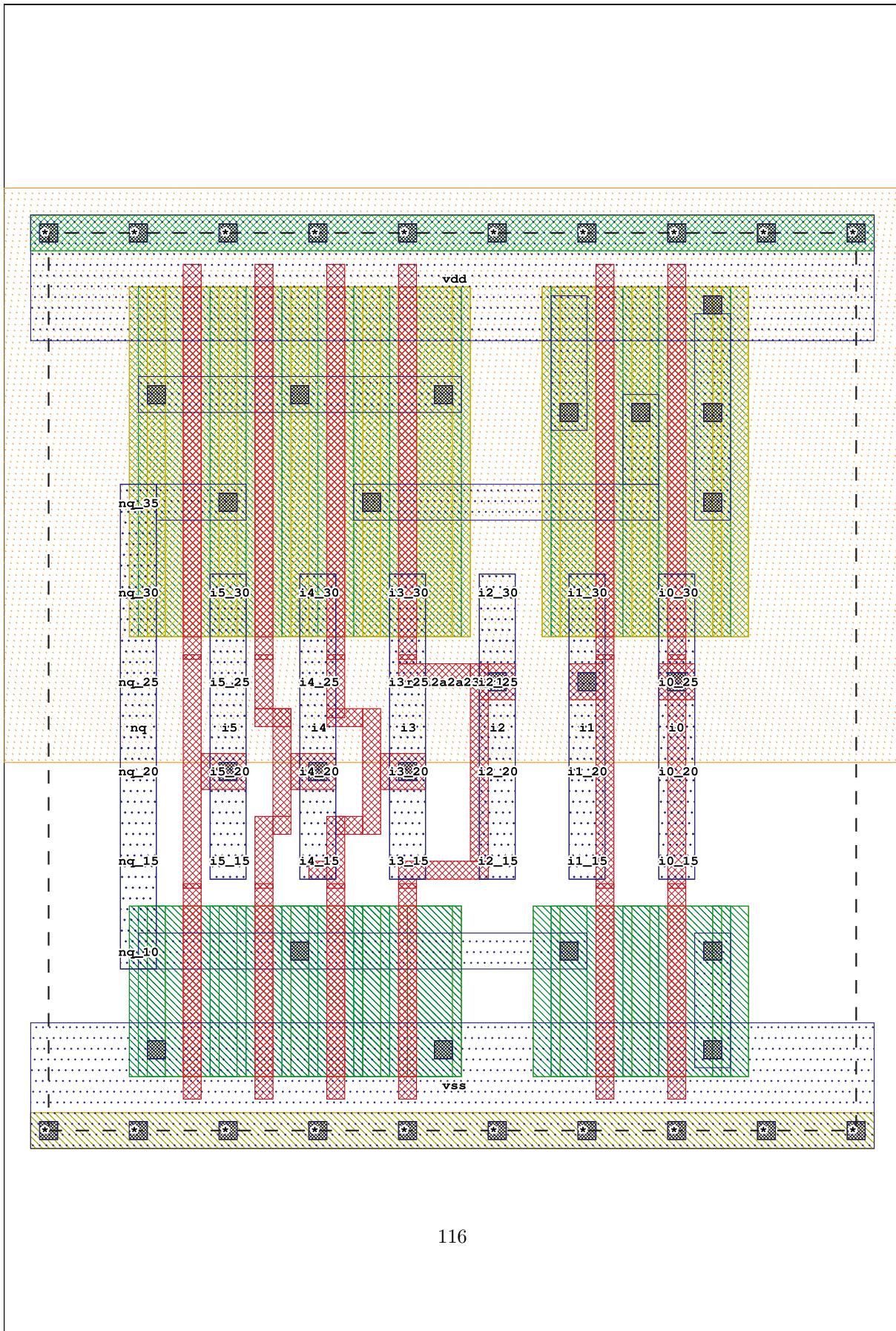
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa2a22_x4"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) or (i2 and i3))) after 1400 ps;
END;
```



#### 4.47 noa2a2a23\_x1

```
ENTITY noa2a2a23_x1 IS
  GENERIC (
    CONSTANT area : NATURAL := 2500;
    CONSTANT cin_i0 : NATURAL := 13;
    CONSTANT cin_i1 : NATURAL := 14;
    CONSTANT cin_i2 : NATURAL := 14;
    CONSTANT cin_i3 : NATURAL := 14;
    CONSTANT cin_i4 : NATURAL := 14;
    CONSTANT cin_i5 : NATURAL := 14;
    CONSTANT rdown_i0_nq : NATURAL := 2850;
    CONSTANT rdown_i1_nq : NATURAL := 2850;
    CONSTANT rdown_i2_nq : NATURAL := 2850;
    CONSTANT rdown_i3_nq : NATURAL := 2850;
    CONSTANT rdown_i4_nq : NATURAL := 2850;
    CONSTANT rdown_i5_nq : NATURAL := 2850;
    CONSTANT rup_i0_nq : NATURAL := 4690;
    CONSTANT rup_i1_nq : NATURAL := 4690;
    CONSTANT rup_i2_nq : NATURAL := 4690;
    CONSTANT rup_i3_nq : NATURAL := 4690;
    CONSTANT rup_i4_nq : NATURAL := 4690;
    CONSTANT rup_i5_nq : NATURAL := 4690;
    CONSTANT tphl_i5_nq : NATURAL := 178;
    CONSTANT tphl_i4_nq : NATURAL := 250;
    CONSTANT tphl_i2_nq : NATURAL := 307;
    CONSTANT tphl_i1_nq : NATURAL := 388;
    CONSTANT tphl_i3_nq : NATURAL := 398;
    CONSTANT tplh_i4_nq : NATURAL := 416;
    CONSTANT tplh_i0_nq : NATURAL := 425;
    CONSTANT tplh_i3_nq : NATURAL := 438;
    CONSTANT tplh_i5_nq : NATURAL := 464;
    CONSTANT tplh_i2_nq : NATURAL := 479;
    CONSTANT tphl_i0_nq : NATURAL := 525;
    CONSTANT tphl_i1_nq : NATURAL := 643;
    CONSTANT transistors : NATURAL := 12
  );
  PORT (
    i0 : in BIT;
    i1 : in BIT;
    i2 : in BIT;
    i3 : in BIT;
    i4 : in BIT;
    i5 : in BIT;
    nq : out BIT;
    vdd : in BIT;
    vss : in BIT
  );
END noa2a2a23_x1;
```

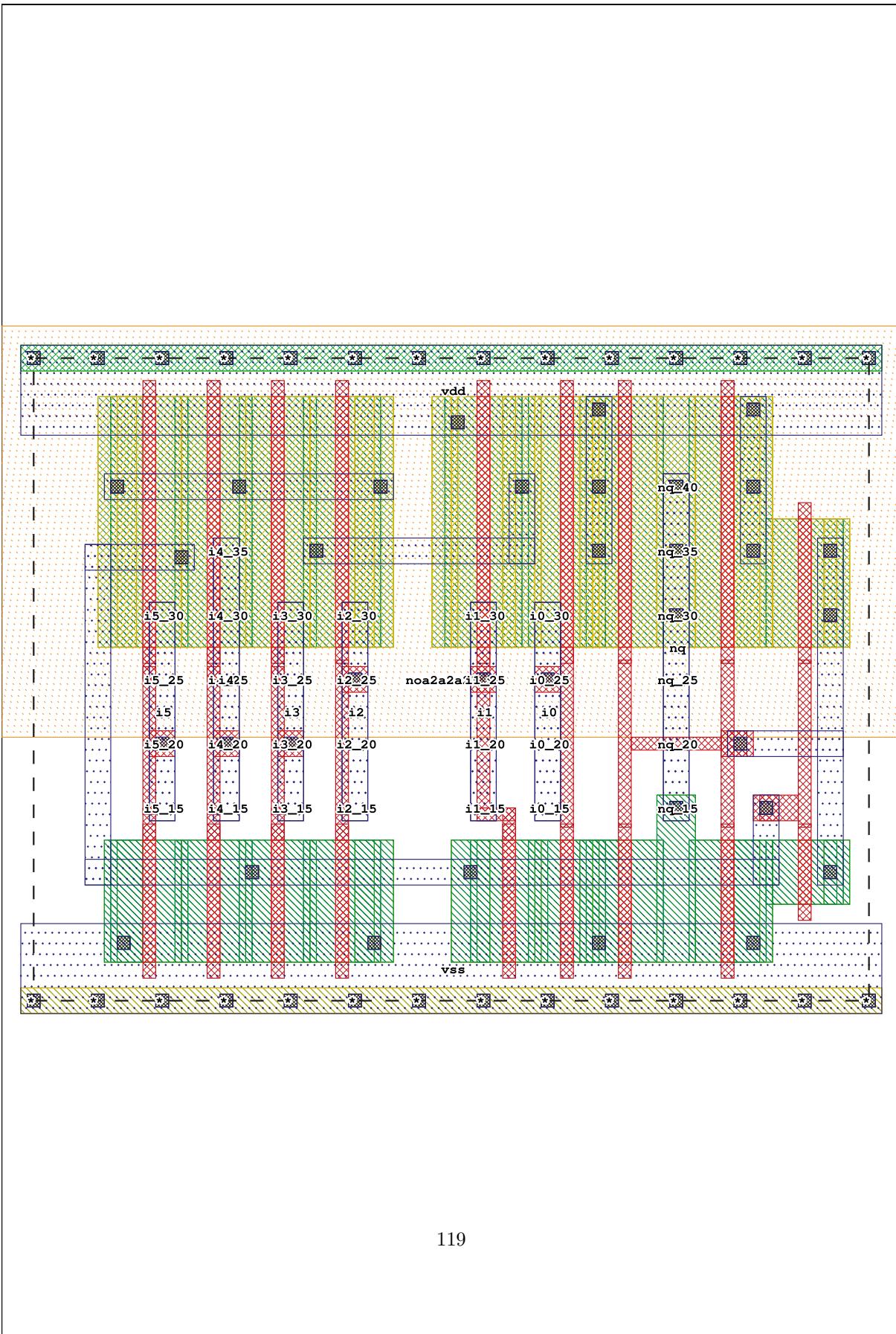
```
ARCHITECTURE behaviour_data_flow OF noa2a2a23_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa2a2a23_x1"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) or (i2 and i3)) or (i4 and i5))) after 1200 ps;
END;
```



#### 4.48 noa2a2a23\_x4

```
ENTITY noa2a2a23_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3250;
    CONSTANT cin_i0         : NATURAL := 13;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 14;
    CONSTANT cin_i4         : NATURAL := 14;
    CONSTANT cin_i5         : NATURAL := 14;
    CONSTANT rdown_i0_nq    : NATURAL := 810;
    CONSTANT rdown_i1_nq    : NATURAL := 810;
    CONSTANT rdown_i2_nq    : NATURAL := 810;
    CONSTANT rdown_i3_nq    : NATURAL := 810;
    CONSTANT rdown_i4_nq    : NATURAL := 810;
    CONSTANT rdown_i5_nq    : NATURAL := 810;
    CONSTANT rup_i0_nq      : NATURAL := 890;
    CONSTANT rup_i1_nq      : NATURAL := 890;
    CONSTANT rup_i2_nq      : NATURAL := 890;
    CONSTANT rup_i3_nq      : NATURAL := 890;
    CONSTANT rup_i4_nq      : NATURAL := 890;
    CONSTANT rup_i5_nq      : NATURAL := 890;
    CONSTANT tphl_i5_nq     : NATURAL := 496;
    CONSTANT tphl_i4_nq     : NATURAL := 574;
    CONSTANT tphl_i2_nq     : NATURAL := 620;
    CONSTANT tphl_i3_nq     : NATURAL := 716;
    CONSTANT tplh_i1_nq     : NATURAL := 778;
    CONSTANT tplh_i0_nq     : NATURAL := 814;
    CONSTANT tplh_i4_nq     : NATURAL := 819;
    CONSTANT tplh_i3_nq     : NATURAL := 833;
    CONSTANT tphl_i0_nq     : NATURAL := 834;
    CONSTANT tplh_i5_nq     : NATURAL := 865;
    CONSTANT tplh_i2_nq     : NATURAL := 873;
    CONSTANT tphl_i1_nq     : NATURAL := 955;
    CONSTANT transistors    : NATURAL := 18
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    i5      : in  BIT;
    nq      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END noa2a2a23_x4;
```

```
ARCHITECTURE behaviour_data_flow OF noa2a2a23_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa2a2a23_x4"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) or (i2 and i3)) or (i4 and i5))) after 1600 ps;
END;
```



#### 4.49 noa2a2a2a24\_x1

```
ENTITY noa2a2a2a24_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3500;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 13;
    CONSTANT cin_i3         : NATURAL := 13;
    CONSTANT cin_i4         : NATURAL := 13;
    CONSTANT cin_i5         : NATURAL := 13;
    CONSTANT cin_i6         : NATURAL := 14;
    CONSTANT cin_i7         : NATURAL := 14;
    CONSTANT rdown_i0_nq    : NATURAL := 2850;
    CONSTANT rdown_i1_nq    : NATURAL := 2850;
    CONSTANT rdown_i2_nq    : NATURAL := 2850;
    CONSTANT rdown_i3_nq    : NATURAL := 2850;
    CONSTANT rdown_i4_nq    : NATURAL := 2850;
    CONSTANT rdown_i5_nq    : NATURAL := 2850;
    CONSTANT rdown_i6_nq    : NATURAL := 2850;
    CONSTANT rdown_i7_nq    : NATURAL := 2850;
    CONSTANT rup_i0_nq      : NATURAL := 6190;
    CONSTANT rup_i1_nq      : NATURAL := 6190;
    CONSTANT rup_i2_nq      : NATURAL := 6190;
    CONSTANT rup_i3_nq      : NATURAL := 6190;
    CONSTANT rup_i4_nq      : NATURAL := 6190;
    CONSTANT rup_i5_nq      : NATURAL := 6190;
    CONSTANT rup_i6_nq      : NATURAL := 6190;
    CONSTANT rup_i7_nq      : NATURAL := 6190;
    CONSTANT tphl_i7_nq     : NATURAL := 200;
    CONSTANT tphl_i6_nq     : NATURAL := 270;
    CONSTANT tphl_i5_nq     : NATURAL := 329;
    CONSTANT tphl_i4_nq     : NATURAL := 419;
    CONSTANT tphl_i6_nq     : NATURAL := 535;
    CONSTANT tphl_i2_nq     : NATURAL := 550;
    CONSTANT tphl_i1_nq     : NATURAL := 562;
    CONSTANT tphl_i7_nq     : NATURAL := 591;
    CONSTANT tphl_i0_nq     : NATURAL := 606;
    CONSTANT tphl_i4_nq     : NATURAL := 613;
    CONSTANT tphl_i3_nq     : NATURAL := 616;
    CONSTANT tphl_i0_nq     : NATURAL := 649;
    CONSTANT tphl_i2_nq     : NATURAL := 662;
    CONSTANT tphl_i5_nq     : NATURAL := 662;
    CONSTANT tphl_i3_nq     : NATURAL := 667;
    CONSTANT tphl_i1_nq     : NATURAL := 775;
    CONSTANT transistors    : NATURAL := 16
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
```

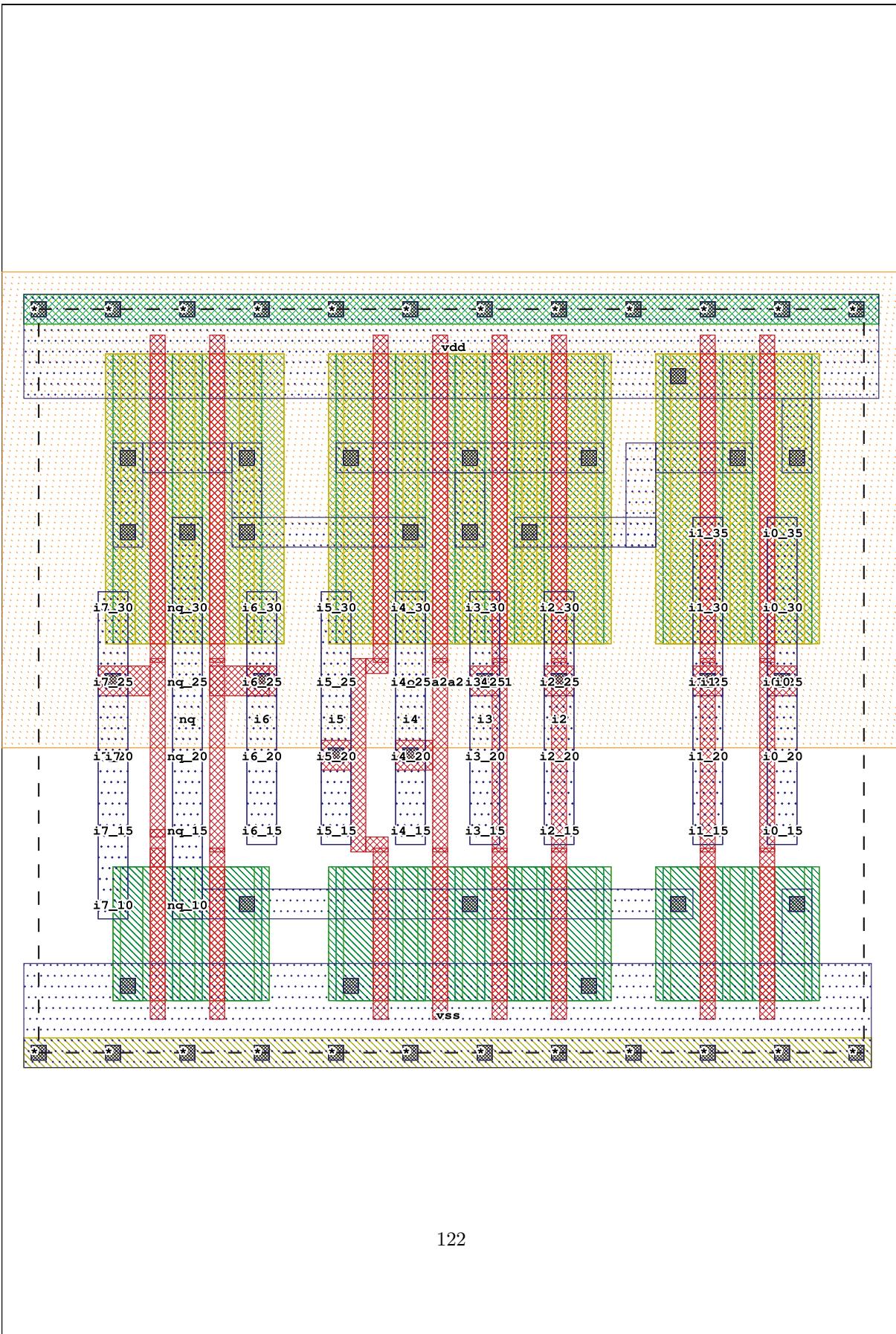
```

i2      : in  BIT;
i3      : in  BIT;
i4      : in  BIT;
i5      : in  BIT;
i6      : in  BIT;
i7      : in  BIT;
nq      : out BIT;
vdd     : in  BIT;
vss     : in  BIT
);
END noa2a2a2a24_x1;

ARCHITECTURE behaviour_data_flow OF noa2a2a2a24_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa2a2a2a24_x1"
  SEVERITY WARNING;
  nq <= not (((((i0 and i1) or (i2 and i3)) or (i4 and i5)) or (i6 and
  i7))) after 1400 ps;
END;

```



#### 4.50 noa2a2a2a24\_x4

```
ENTITY noa2a2a2a24_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4250;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 13;
    CONSTANT cin_i4         : NATURAL := 13;
    CONSTANT cin_i5         : NATURAL := 13;
    CONSTANT cin_i6         : NATURAL := 14;
    CONSTANT cin_i7         : NATURAL := 14;
    CONSTANT rdown_i0_nq    : NATURAL := 810;
    CONSTANT rdown_i1_nq    : NATURAL := 810;
    CONSTANT rdown_i2_nq    : NATURAL := 810;
    CONSTANT rdown_i3_nq    : NATURAL := 810;
    CONSTANT rdown_i4_nq    : NATURAL := 810;
    CONSTANT rdown_i5_nq    : NATURAL := 810;
    CONSTANT rdown_i6_nq    : NATURAL := 810;
    CONSTANT rdown_i7_nq    : NATURAL := 810;
    CONSTANT rup_i0_nq      : NATURAL := 890;
    CONSTANT rup_i1_nq      : NATURAL := 890;
    CONSTANT rup_i2_nq      : NATURAL := 890;
    CONSTANT rup_i3_nq      : NATURAL := 890;
    CONSTANT rup_i4_nq      : NATURAL := 890;
    CONSTANT rup_i5_nq      : NATURAL := 890;
    CONSTANT rup_i6_nq      : NATURAL := 890;
    CONSTANT rup_i7_nq      : NATURAL := 890;
    CONSTANT tphl_i7_nq     : NATURAL := 525;
    CONSTANT tphl_i6_nq     : NATURAL := 606;
    CONSTANT tphl_i5_nq     : NATURAL := 649;
    CONSTANT tphl_i4_nq     : NATURAL := 748;
    CONSTANT tphl_i2_nq     : NATURAL := 867;
    CONSTANT tphl_i0_nq     : NATURAL := 966;
    CONSTANT tphl_i3_nq     : NATURAL := 990;
    CONSTANT tplh_i6_nq     : NATURAL := 999;
    CONSTANT tplh_i1_nq     : NATURAL := 1005;
    CONSTANT tplh_i0_nq     : NATURAL := 1049;
    CONSTANT tplh_i7_nq     : NATURAL := 1052;
    CONSTANT tplh_i3_nq     : NATURAL := 1061;
    CONSTANT tplh_i4_nq     : NATURAL := 1061;
    CONSTANT tphl_i1_nq     : NATURAL := 1097;
    CONSTANT tplh_i2_nq     : NATURAL := 1106;
    CONSTANT tplh_i5_nq     : NATURAL := 1109;
    CONSTANT transistors    : NATURAL := 22
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
```

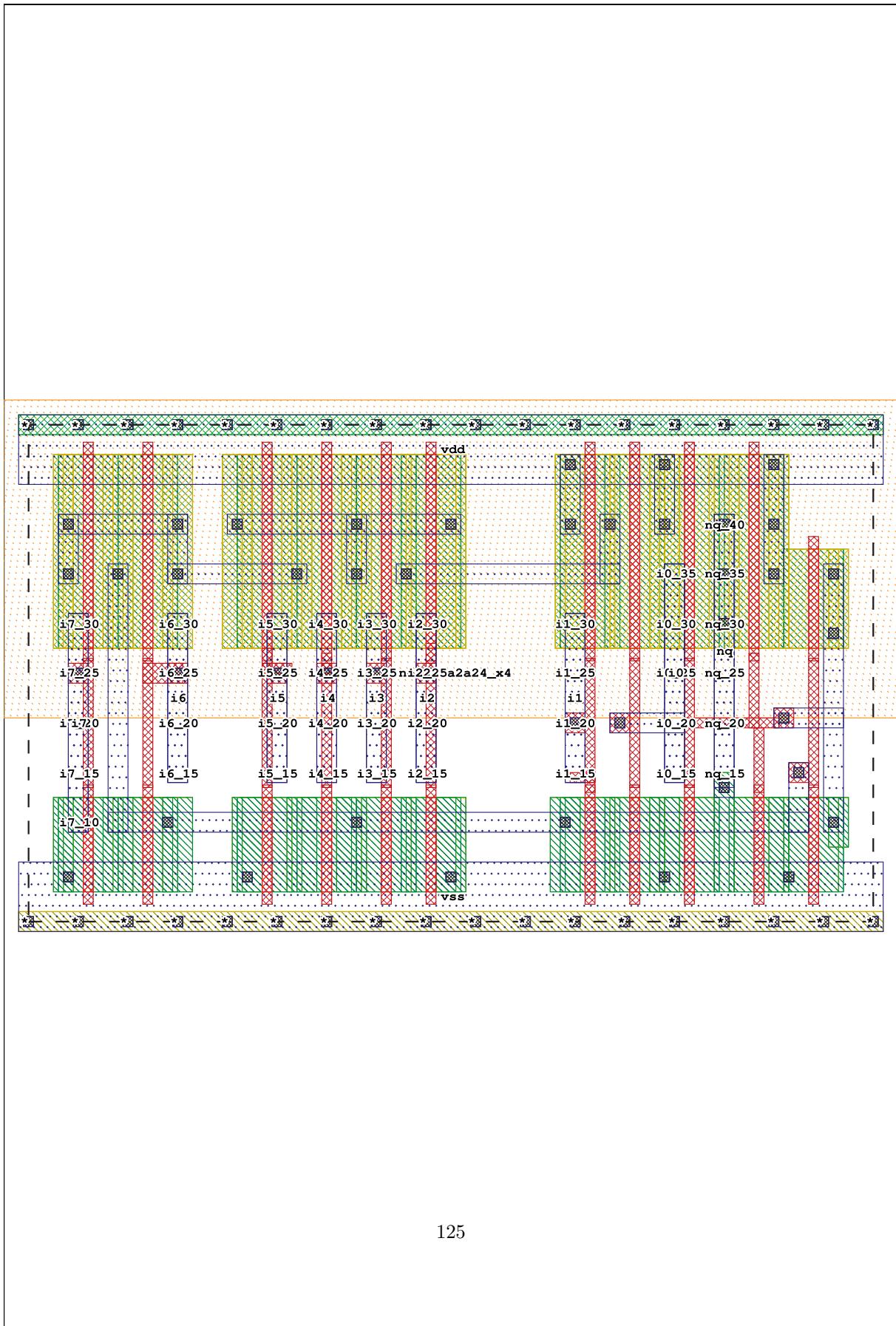
```

i2      : in  BIT;
i3      : in  BIT;
i4      : in  BIT;
i5      : in  BIT;
i6      : in  BIT;
i7      : in  BIT;
nq      : out BIT;
vdd     : in  BIT;
vss     : in  BIT
);
END noa2a2a2a24_x4;

ARCHITECTURE behaviour_data_flow OF noa2a2a2a24_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa2a2a2a24_x4"
  SEVERITY WARNING;
  nq <= not (((((i0 and i1) or (i2 and i3)) or (i4 and i5)) or (i6 and
  i7))) after 1700 ps;
END;

```

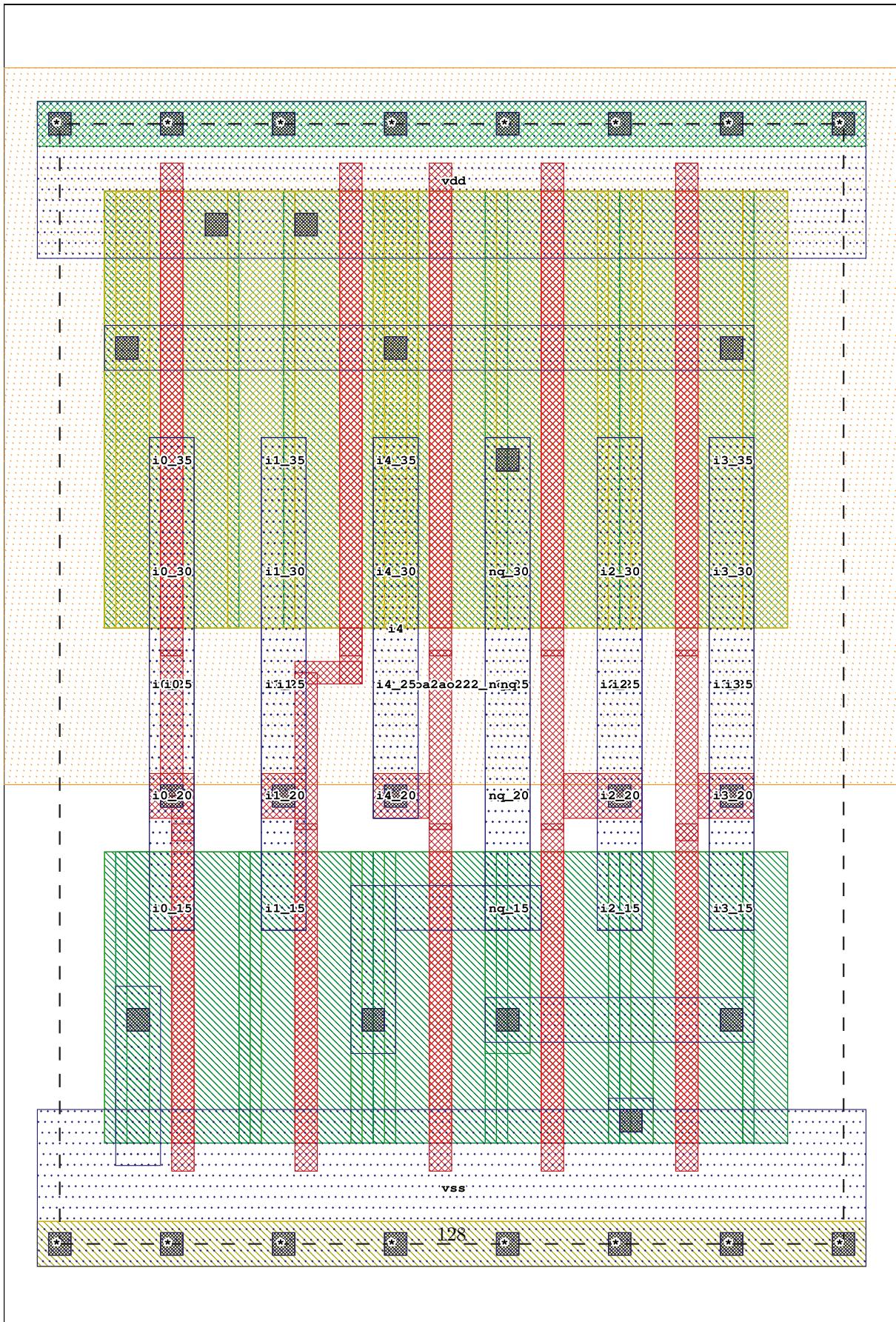


#### 4.51 noa2ao222\_x1

```
ENTITY noa2ao222_x1 IS
  GENERIC (
    CONSTANT area : NATURAL := 1750;
    CONSTANT cin_i0 : NATURAL := 11;
    CONSTANT cin_i1 : NATURAL := 11;
    CONSTANT cin_i2 : NATURAL := 13;
    CONSTANT cin_i3 : NATURAL := 13;
    CONSTANT cin_i4 : NATURAL := 13;
    CONSTANT rdown_i0_nq : NATURAL := 3210;
    CONSTANT rdown_i1_nq : NATURAL := 3210;
    CONSTANT rdown_i2_nq : NATURAL := 3210;
    CONSTANT rdown_i3_nq : NATURAL := 3210;
    CONSTANT rdown_i4_nq : NATURAL := 3210;
    CONSTANT rup_i0_nq : NATURAL := 5260;
    CONSTANT rup_i1_nq : NATURAL := 5260;
    CONSTANT rup_i2_nq : NATURAL := 5260;
    CONSTANT rup_i3_nq : NATURAL := 5260;
    CONSTANT rup_i4_nq : NATURAL := 3750;
    CONSTANT tphl_i2_nq : NATURAL := 186;
    CONSTANT tphl_i4_nq : NATURAL := 240;
    CONSTANT tphl_i3_nq : NATURAL := 256;
    CONSTANT tphl_i4_nq : NATURAL := 309;
    CONSTANT tphl_i0_nq : NATURAL := 348;
    CONSTANT tphl_i1_nq : NATURAL := 378;
    CONSTANT tphl_i0_nq : NATURAL := 422;
    CONSTANT tphl_i1_nq : NATURAL := 440;
    CONSTANT tphl_i3_nq : NATURAL := 459;
    CONSTANT tphl_i2_nq : NATURAL := 473;
    CONSTANT transistors : NATURAL := 10
  );
  PORT (
    i0 : in BIT;
    i1 : in BIT;
    i2 : in BIT;
    i3 : in BIT;
    i4 : in BIT;
    nq : out BIT;
    vdd : in BIT;
    vss : in BIT
  );
END noa2ao222_x1;

ARCHITECTURE behaviour_data_flow OF noa2ao222_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa2ao222_x1"
  SEVERITY WARNING;
```

```
nq <= not ((( i0 and i1 ) or (( i2 or i3 ) and i4 ))) after 1100 ps;  
END;
```



## 4.52 noa2ao222\_x4

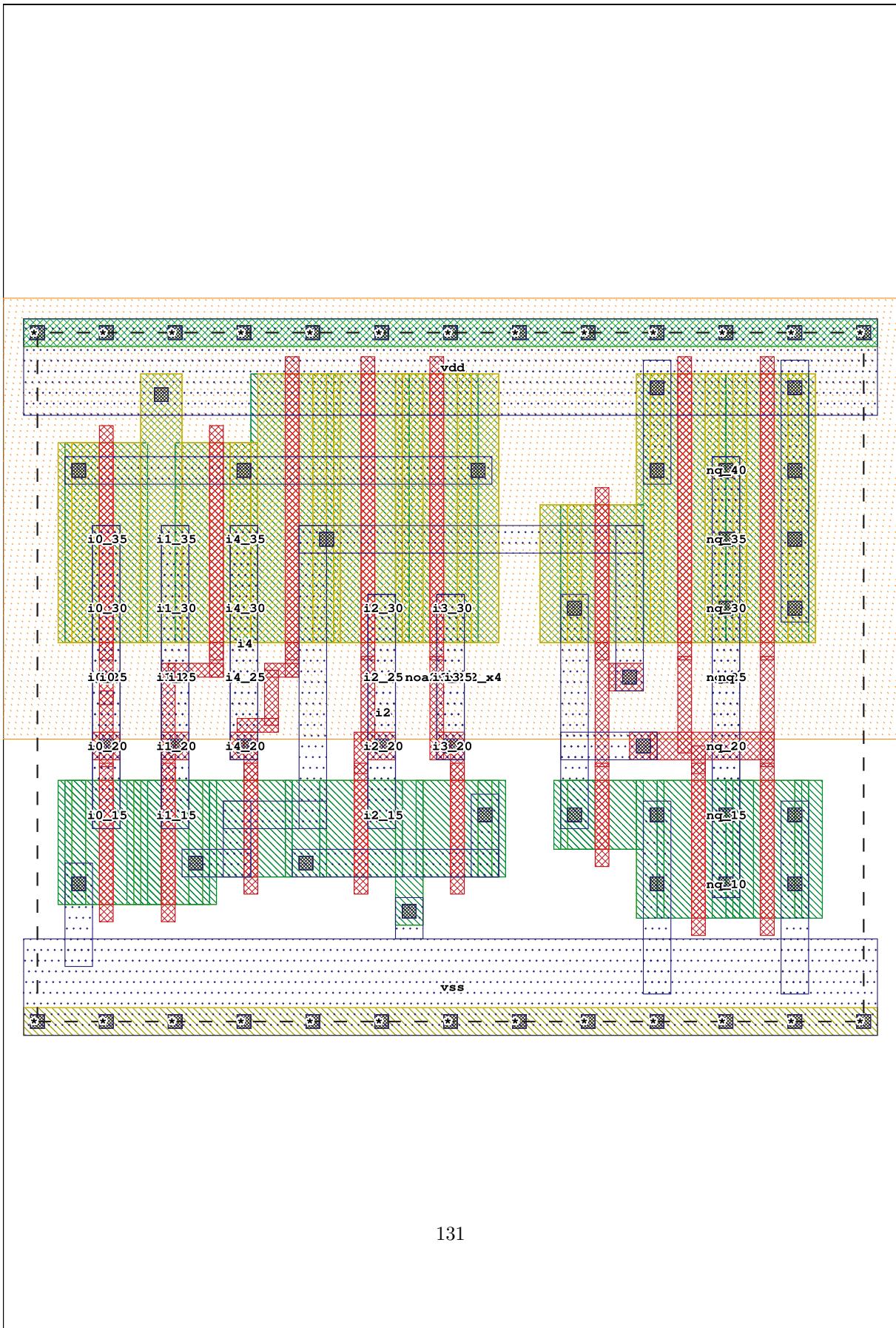
```

ENTITY noa2ao222_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 3000;
    CONSTANT cin_i0         : NATURAL := 11;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT cin_i2         : NATURAL := 11;
    CONSTANT cin_i3         : NATURAL := 11;
    CONSTANT cin_i4         : NATURAL := 11;
    CONSTANT rdown_i0_nq    : NATURAL := 810;
    CONSTANT rdown_i1_nq    : NATURAL := 810;
    CONSTANT rdown_i2_nq    : NATURAL := 810;
    CONSTANT rdown_i3_nq    : NATURAL := 810;
    CONSTANT rdown_i4_nq    : NATURAL := 810;
    CONSTANT rup_i0_nq      : NATURAL := 890;
    CONSTANT rup_i1_nq      : NATURAL := 890;
    CONSTANT rup_i2_nq      : NATURAL := 890;
    CONSTANT rup_i3_nq      : NATURAL := 890;
    CONSTANT rup_i4_nq      : NATURAL := 890;
    CONSTANT tphl_i2_nq     : NATURAL := 638;
    CONSTANT tphl_i4_nq     : NATURAL := 664;
    CONSTANT tphl_i0_nq     : NATURAL := 684;
    CONSTANT tphl_i4_nq     : NATURAL := 718;
    CONSTANT tphl_i3_nq     : NATURAL := 732;
    CONSTANT tphl_i1_nq     : NATURAL := 758;
    CONSTANT tphl_i1_nq     : NATURAL := 780;
    CONSTANT tphl_i3_nq     : NATURAL := 795;
    CONSTANT tphl_i0_nq     : NATURAL := 801;
    CONSTANT tphl_i2_nq     : NATURAL := 809;
    CONSTANT transistors    : NATURAL := 16
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    nq     : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END noa2ao222_x4;

ARCHITECTURE behaviour_data_flow OF noa2ao222_x4 IS
BEGIN
    ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on noa2ao222_x4"
    SEVERITY WARNING;

```

```
nq <= not ((( i0 and i1 ) or (( i2 or i3 ) and i4 ))) after 1400 ps;  
END;
```



#### 4.53 noa3ao322 x1

```
ENTITY noa3ao322_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2250;
    CONSTANT cin_i0         : NATURAL := 13;
    CONSTANT cin_i1         : NATURAL := 13;
    CONSTANT cin_i2         : NATURAL := 13;
    CONSTANT cin_i3         : NATURAL := 13;
    CONSTANT cin_i4         : NATURAL := 13;
    CONSTANT cin_i5         : NATURAL := 13;
    CONSTANT cin_i6         : NATURAL := 13;
    CONSTANT rdown_i0_nq    : NATURAL := 3370;
    CONSTANT rdown_i1_nq    : NATURAL := 3370;
    CONSTANT rdown_i2_nq    : NATURAL := 3370;
    CONSTANT rdown_i3_nq    : NATURAL := 3210;
    CONSTANT rdown_i4_nq    : NATURAL := 3210;
    CONSTANT rdown_i5_nq    : NATURAL := 3210;
    CONSTANT rdown_i6_nq    : NATURAL := 3210;
    CONSTANT rup_i0_nq      : NATURAL := 6700;
    CONSTANT rup_i1_nq      : NATURAL := 6700;
    CONSTANT rup_i2_nq      : NATURAL := 6700;
    CONSTANT rup_i3_nq      : NATURAL := 6700;
    CONSTANT rup_i4_nq      : NATURAL := 6700;
    CONSTANT rup_i5_nq      : NATURAL := 6700;
    CONSTANT rup_i6_nq      : NATURAL := 3690;
    CONSTANT tphl_i3_nq     : NATURAL := 196;
    CONSTANT tphl_i6_nq     : NATURAL := 246;
    CONSTANT tphl_i4_nq     : NATURAL := 264;
    CONSTANT tphl_i6_nq     : NATURAL := 311;
    CONSTANT tphl_i5_nq     : NATURAL := 328;
    CONSTANT tphl_i0_nq     : NATURAL := 396;
    CONSTANT tphl_i1_nq     : NATURAL := 486;
    CONSTANT tphl_i2_nq     : NATURAL := 488;
    CONSTANT tphl_i2_nq     : NATURAL := 546;
    CONSTANT tphl_i1_nq     : NATURAL := 552;
    CONSTANT tphl_i5_nq     : NATURAL := 581;
    CONSTANT tphl_i3_nq     : NATURAL := 599;
    CONSTANT tphl_i4_nq     : NATURAL := 608;
    CONSTANT tphl_i0_nq     : NATURAL := 616;
    CONSTANT transistors    : NATURAL := 14
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    i5      : in  BIT;
    i6      : in  BIT;
```

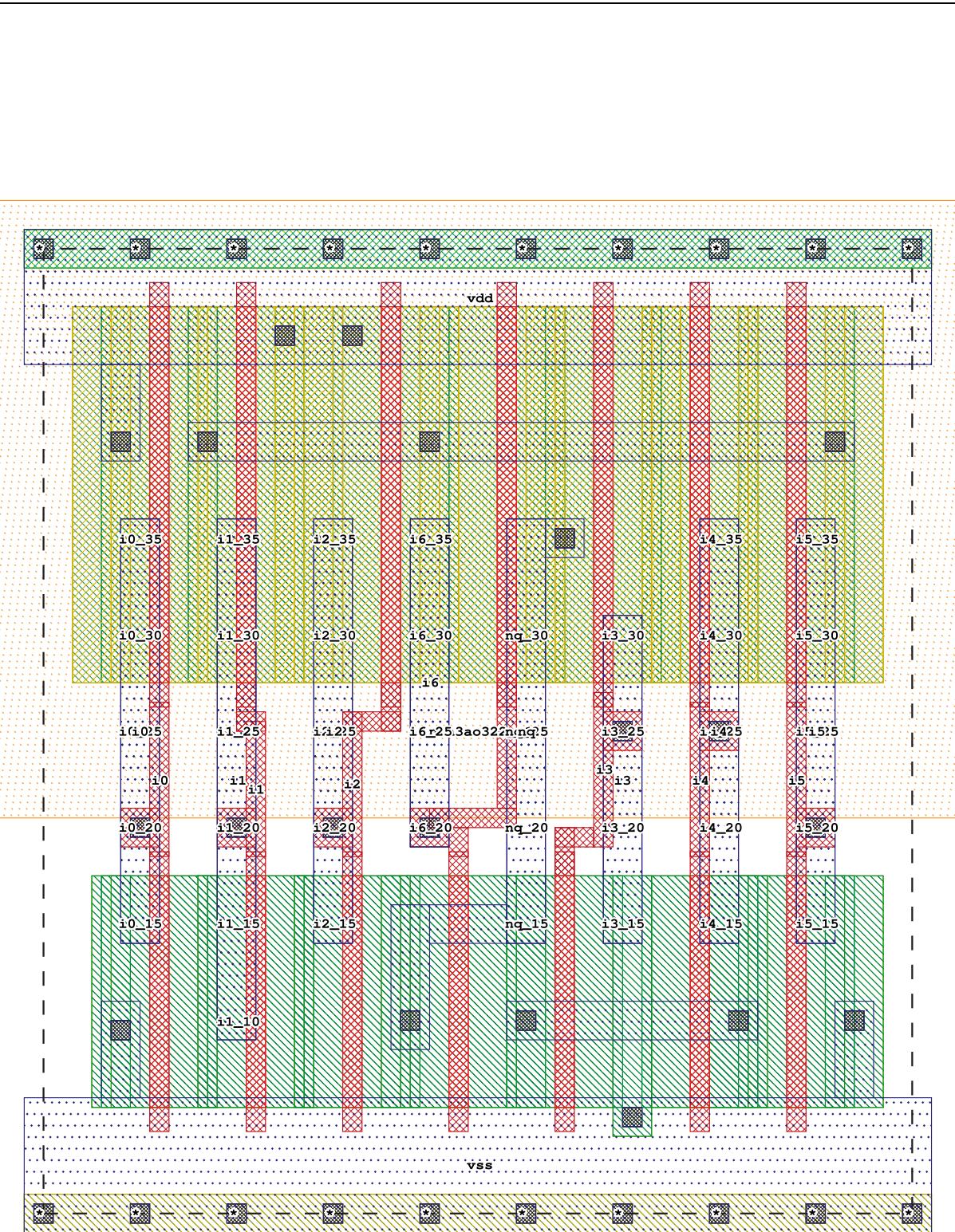
```

nq      : out BIT;
vdd     : in  BIT;
vss     : in  BIT
);
END noa3ao322_x1;

ARCHITECTURE behaviour_data_flow OF noa3ao322_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa3ao322_x1"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) and i2) or (((i3 or i4) or i5) and i6))) after 1200 ps;
END;

```



#### 4.54 noa3ao322 x4

```
ENTITY noa3ao322_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3250;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT cin_i3         : NATURAL := 9;
    CONSTANT cin_i4         : NATURAL := 9;
    CONSTANT cin_i5         : NATURAL := 9;
    CONSTANT cin_i6         : NATURAL := 9;
    CONSTANT rdown_i0_nq    : NATURAL := 810;
    CONSTANT rdown_i1_nq    : NATURAL := 810;
    CONSTANT rdown_i2_nq    : NATURAL := 810;
    CONSTANT rdown_i3_nq    : NATURAL := 810;
    CONSTANT rdown_i4_nq    : NATURAL := 810;
    CONSTANT rdown_i5_nq    : NATURAL := 810;
    CONSTANT rdown_i6_nq    : NATURAL := 810;
    CONSTANT rup_i0_nq      : NATURAL := 890;
    CONSTANT rup_i1_nq      : NATURAL := 890;
    CONSTANT rup_i2_nq      : NATURAL := 890;
    CONSTANT rup_i3_nq      : NATURAL := 890;
    CONSTANT rup_i4_nq      : NATURAL := 890;
    CONSTANT rup_i5_nq      : NATURAL := 890;
    CONSTANT rup_i6_nq      : NATURAL := 890;
    CONSTANT tplh_i6_nq     : NATURAL := 718;
    CONSTANT tphl_i3_nq     : NATURAL := 729;
    CONSTANT tphl_i6_nq     : NATURAL := 738;
    CONSTANT tphl_i0_nq     : NATURAL := 819;
    CONSTANT tphl_i4_nq     : NATURAL := 821;
    CONSTANT tphl_i2_nq     : NATURAL := 874;
    CONSTANT tphl_i5_nq     : NATURAL := 900;
    CONSTANT tphl_i5_nq     : NATURAL := 907;
    CONSTANT tphl_i1_nq     : NATURAL := 914;
    CONSTANT tphl_i4_nq     : NATURAL := 924;
    CONSTANT tphl_i3_nq     : NATURAL := 926;
    CONSTANT tphl_i1_nq     : NATURAL := 931;
    CONSTANT tphl_i0_nq     : NATURAL := 987;
    CONSTANT tphl_i2_nq     : NATURAL := 990;
    CONSTANT transistors    : NATURAL := 20
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    i5      : in  BIT;
    i6      : in  BIT;
```

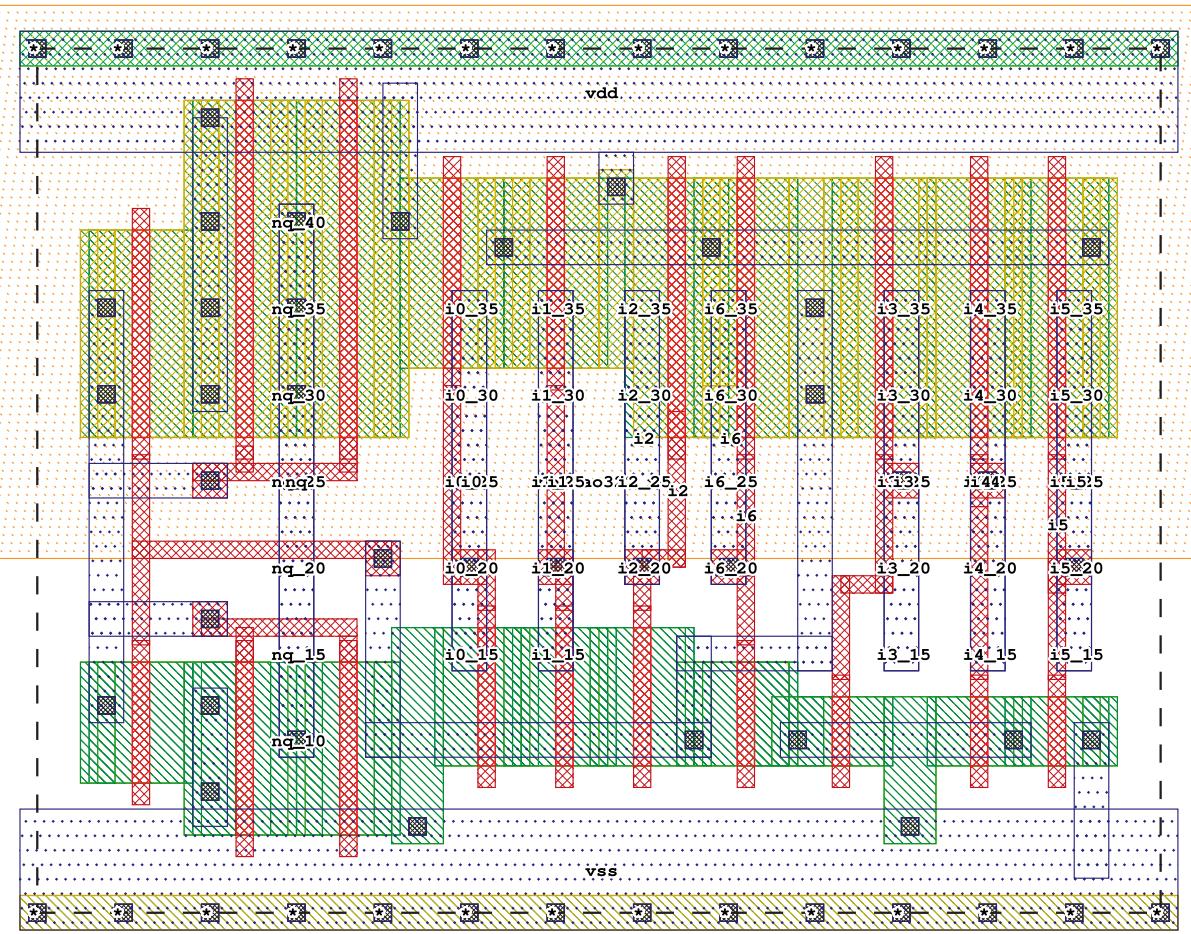
```

nq      : out BIT;
vdd     : in  BIT;
vss     : in  BIT
);
END noa3ao322_x4;

ARCHITECTURE behaviour_data_flow OF noa3ao322_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on noa3ao322_x4"
  SEVERITY WARNING;
  nq <= not (((i0 and i1) and i2) or (((i3 or i4) or i5) and i6))) after 1600 ps;
END;

```



#### 4.55 nts\_x1

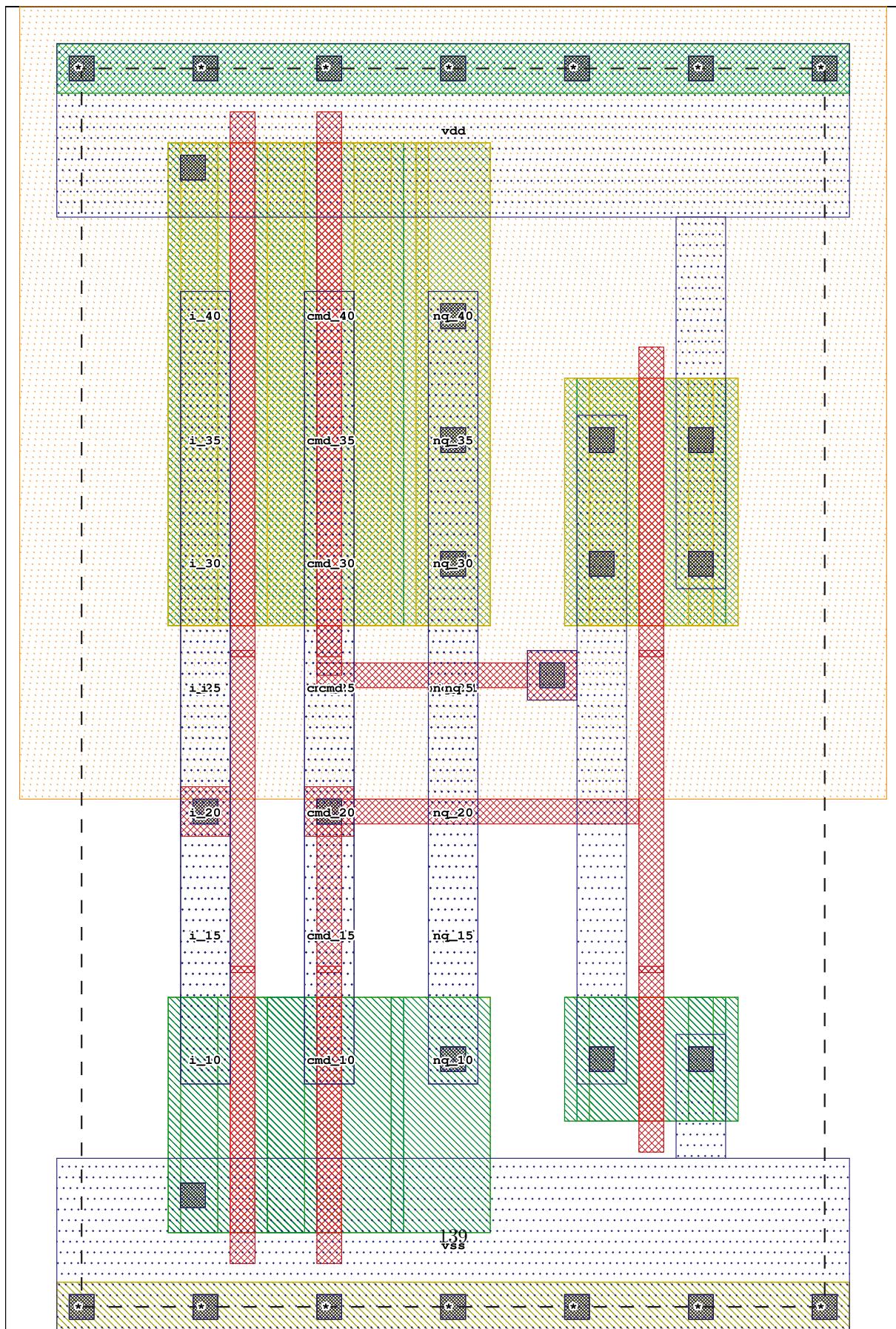
```
ENTITY nts_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_cmd       : NATURAL := 14;
    CONSTANT cin_i         : NATURAL := 14;
    CONSTANT rdown_cmd_nq : NATURAL := 2850;
    CONSTANT rdown_i_nq   : NATURAL := 2850;
    CONSTANT rup_cmd_nq   : NATURAL := 3210;
    CONSTANT rup_i_nq     : NATURAL := 3210;
    CONSTANT tphl_cmd_nq  : NATURAL := 41;
    CONSTANT tphl_i_nq    : NATURAL := 169;
    CONSTANT tplh_i_nq    : NATURAL := 201;
    CONSTANT tphh_cmd_nq  : NATURAL := 249;
    CONSTANT transistors   : NATURAL := 6
  );
  PORT (
    cmd      : in  BIT;
    i        : in  BIT;
    nq       : out MUX_BIT BUS;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END nts_x1;

ARCHITECTURE behaviour_data_flow OF nts_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nts_x1"
  SEVERITY WARNING;

  label0 : BLOCK (cmd = '1')
  BEGIN
    nq <= GUARDED not (i) after 800 ps;
  END BLOCK label0;

END;
```



#### 4.56 nts\_x2

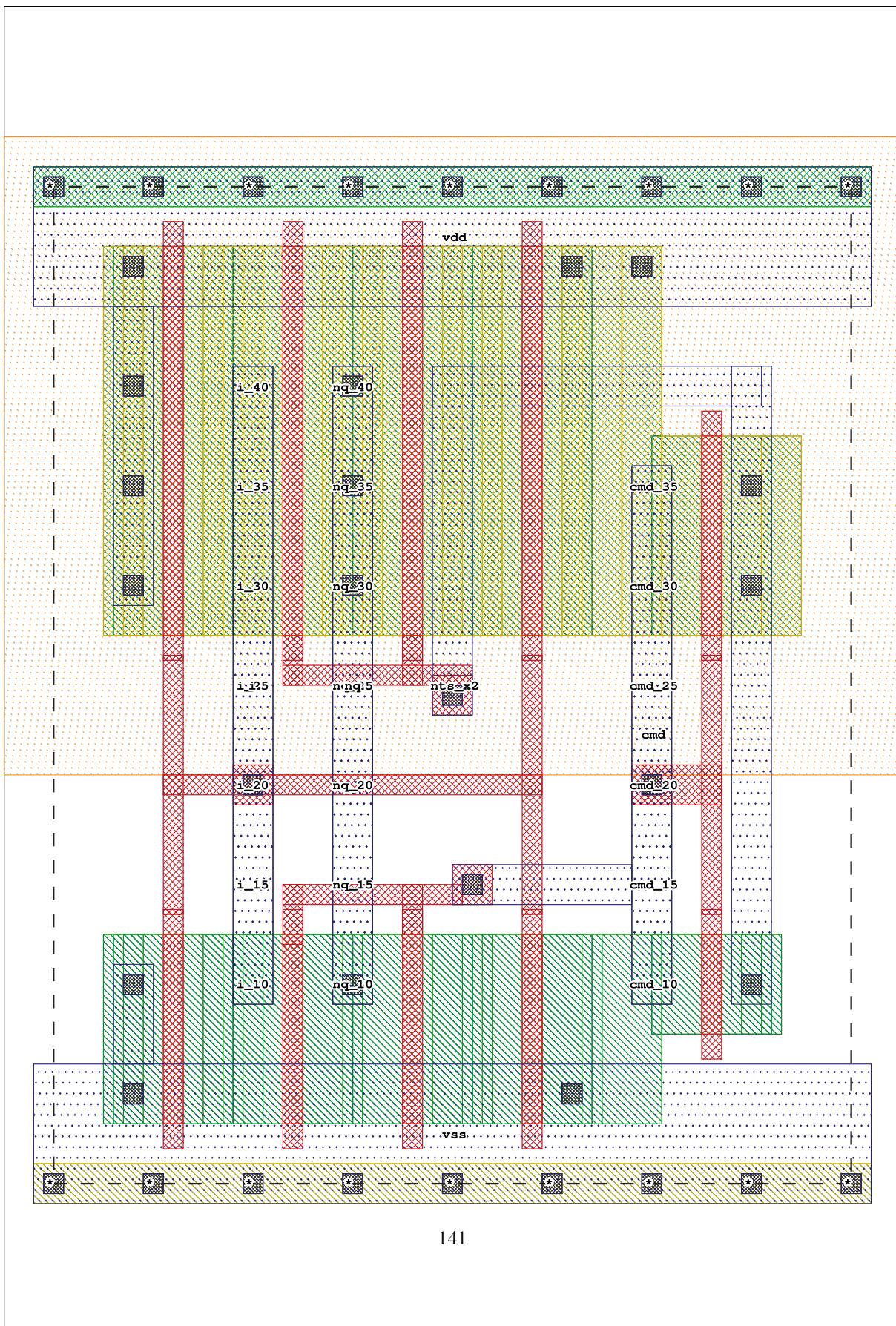
```
ENTITY nts_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_cmd       : NATURAL := 18;
    CONSTANT cin_i         : NATURAL := 28;
    CONSTANT rdown_cmd_nq : NATURAL := 1430;
    CONSTANT rdown_i_nq   : NATURAL := 1430;
    CONSTANT rup_cmd_nq   : NATURAL := 1600;
    CONSTANT rup_i_nq     : NATURAL := 1600;
    CONSTANT tphl_cmd_nq  : NATURAL := 33;
    CONSTANT tphl_i_nq    : NATURAL := 167;
    CONSTANT tplh_i_nq    : NATURAL := 201;
    CONSTANT tphh_cmd_nq  : NATURAL := 330;
    CONSTANT transistors   : NATURAL := 10
  );
  PORT (
    cmd      : in  BIT;
    i        : in  BIT;
    nq       : out MUX_BIT BUS;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END nts_x2;

ARCHITECTURE behaviour_data_flow OF nts_x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nts_x2"
  SEVERITY WARNING;

  label0 : BLOCK (cmd = '1')
  BEGIN
    nq <= GUARDED not (i) after 900 ps;
  END BLOCK label0;

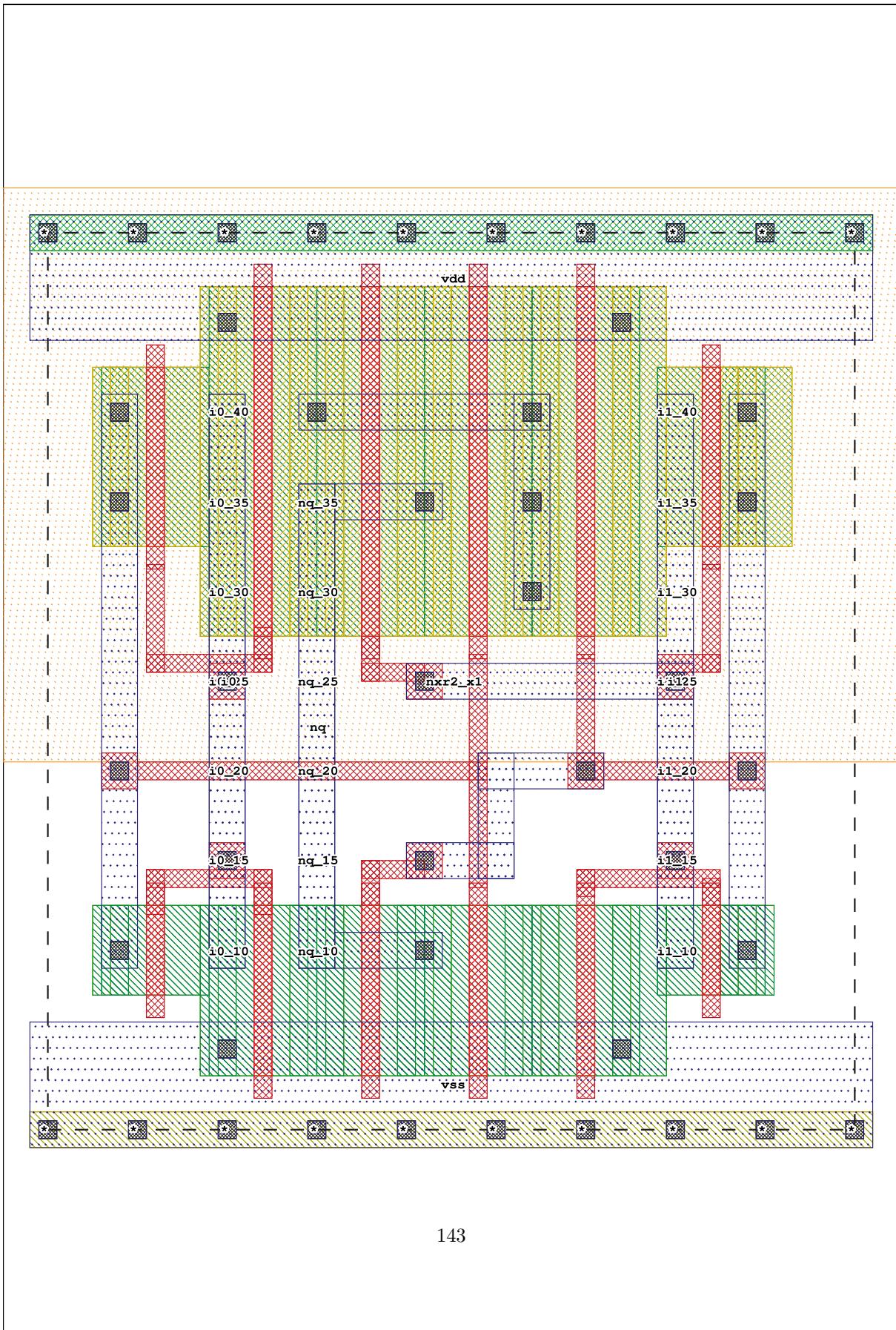
END;
```



#### 4.57 nxr2\_x1

```
ENTITY nxr2_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2250;
    CONSTANT cin_i0         : NATURAL := 21;
    CONSTANT cin_i1         : NATURAL := 22;
    CONSTANT rdown_i0_nq   : NATURAL := 2850;
    CONSTANT rdown_i1_nq   : NATURAL := 2850;
    CONSTANT rup_i0_nq     : NATURAL := 3210;
    CONSTANT rup_i1_nq     : NATURAL := 3210;
    CONSTANT tphl_i1_nq    : NATURAL := 156;
    CONSTANT tphl_i0_nq    : NATURAL := 288;
    CONSTANT tplh_i0_nq    : NATURAL := 293;
    CONSTANT tplh_i1_nq    : NATURAL := 327;
    CONSTANT tphh_i0_nq    : NATURAL := 366;
    CONSTANT tp11_i0_nq     : NATURAL := 389;
    CONSTANT tp11_i1_nq     : NATURAL := 395;
    CONSTANT tp11_i1_nq     : NATURAL := 503;
    CONSTANT transistors   : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END nxr2_x1;
```

```
ARCHITECTURE behaviour_data_flow OF nxr2_x1 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nxr2_x1"
  SEVERITY WARNING;
  nq <= not ((i0 xor i1)) after 1100 ps;
END;
```

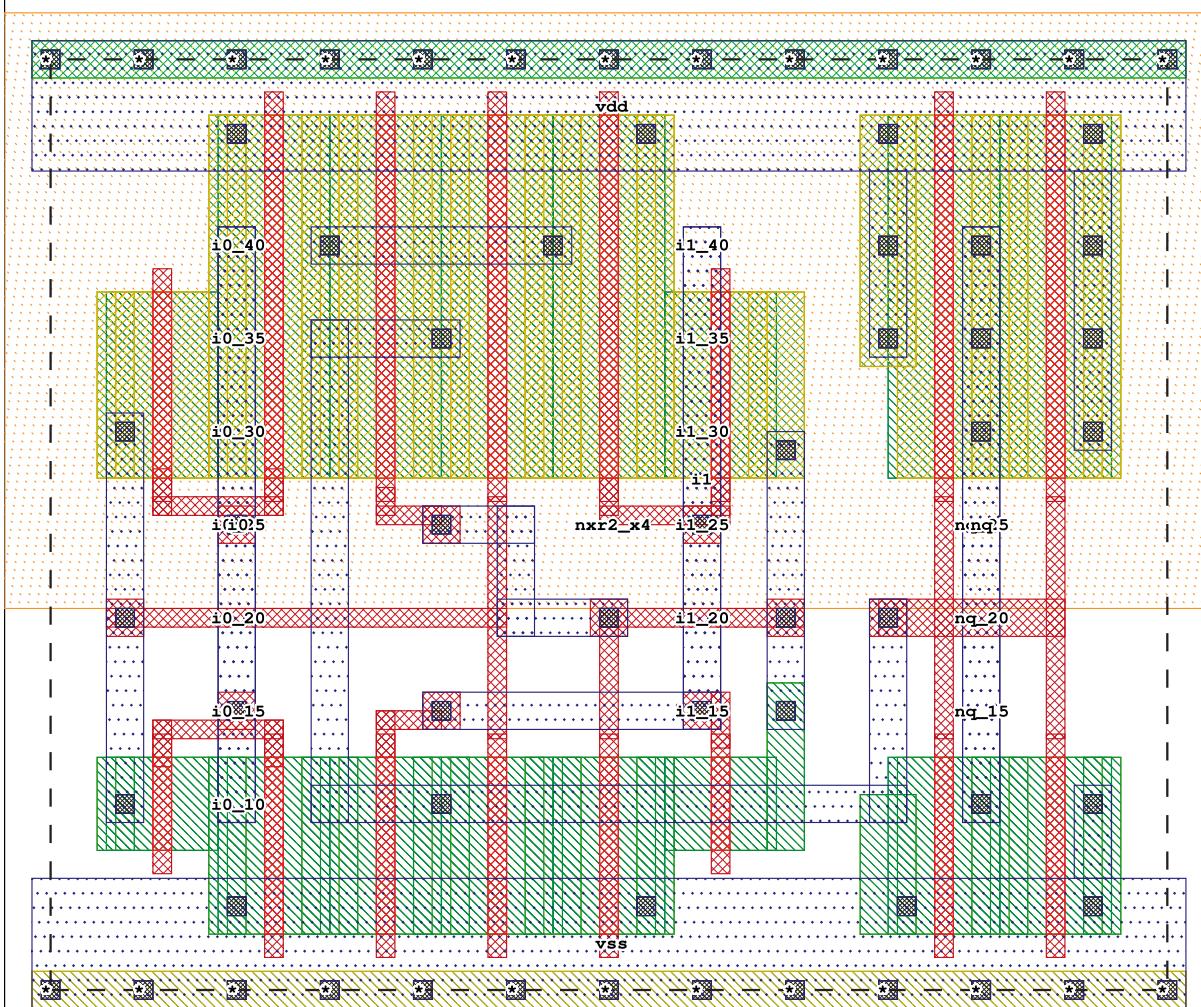


#### 4.58 nxr2\_x4

```
ENTITY nxr2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3000;
    CONSTANT cin_i0         : NATURAL := 20;
    CONSTANT cin_i1         : NATURAL := 21;
    CONSTANT rdown_i0_nq   : NATURAL := 810;
    CONSTANT rdown_i1_nq   : NATURAL := 810;
    CONSTANT rup_i0_nq     : NATURAL := 890;
    CONSTANT rup_i1_nq     : NATURAL := 890;
    CONSTANT tpll_i1_nq    : NATURAL := 453;
    CONSTANT tphh_i0_nq    : NATURAL := 469;
    CONSTANT tpll_i0_nq    : NATURAL := 481;
    CONSTANT tphl_i0_nq    : NATURAL := 522;
    CONSTANT tphl_i1_nq    : NATURAL := 542;
    CONSTANT tphl_i1_nq    : NATURAL := 553;
    CONSTANT tplh_i0_nq    : NATURAL := 553;
    CONSTANT tphh_i1_nq    : NATURAL := 568;
    CONSTANT transistors   : NATURAL := 16
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END nxr2_x4;

ARCHITECTURE behaviour_data_flow OF nxr2_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on nxr2_x4"
  SEVERITY WARNING;
  nq <= not ((i0 xor i1)) after 1200 ps;
END;
```

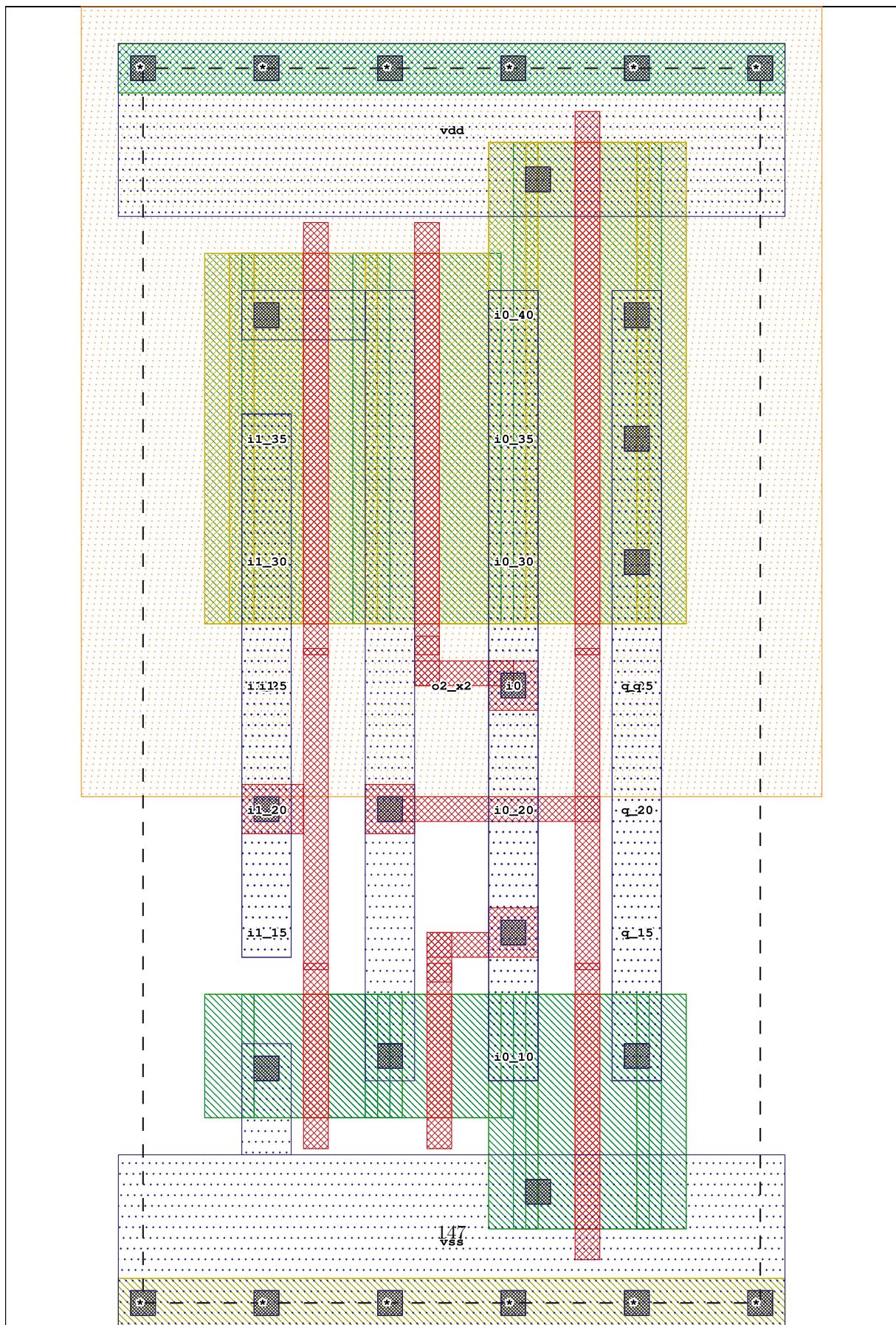


#### 4.59 o2\_x2

```
ENTITY o2_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1250;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT tpll_i0_q      : NATURAL := 310;
    CONSTANT tphh_i1_q      : NATURAL := 335;
    CONSTANT tpll_i1_q      : NATURAL := 364;
    CONSTANT tphh_i0_q      : NATURAL := 406;
    CONSTANT transistors    : NATURAL := 6
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END o2_x2;

ARCHITECTURE behaviour_data_flow OF o2_x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on o2_x2"
  SEVERITY WARNING;
  q <= (i0 or i1) after 1000 ps;
END;
```

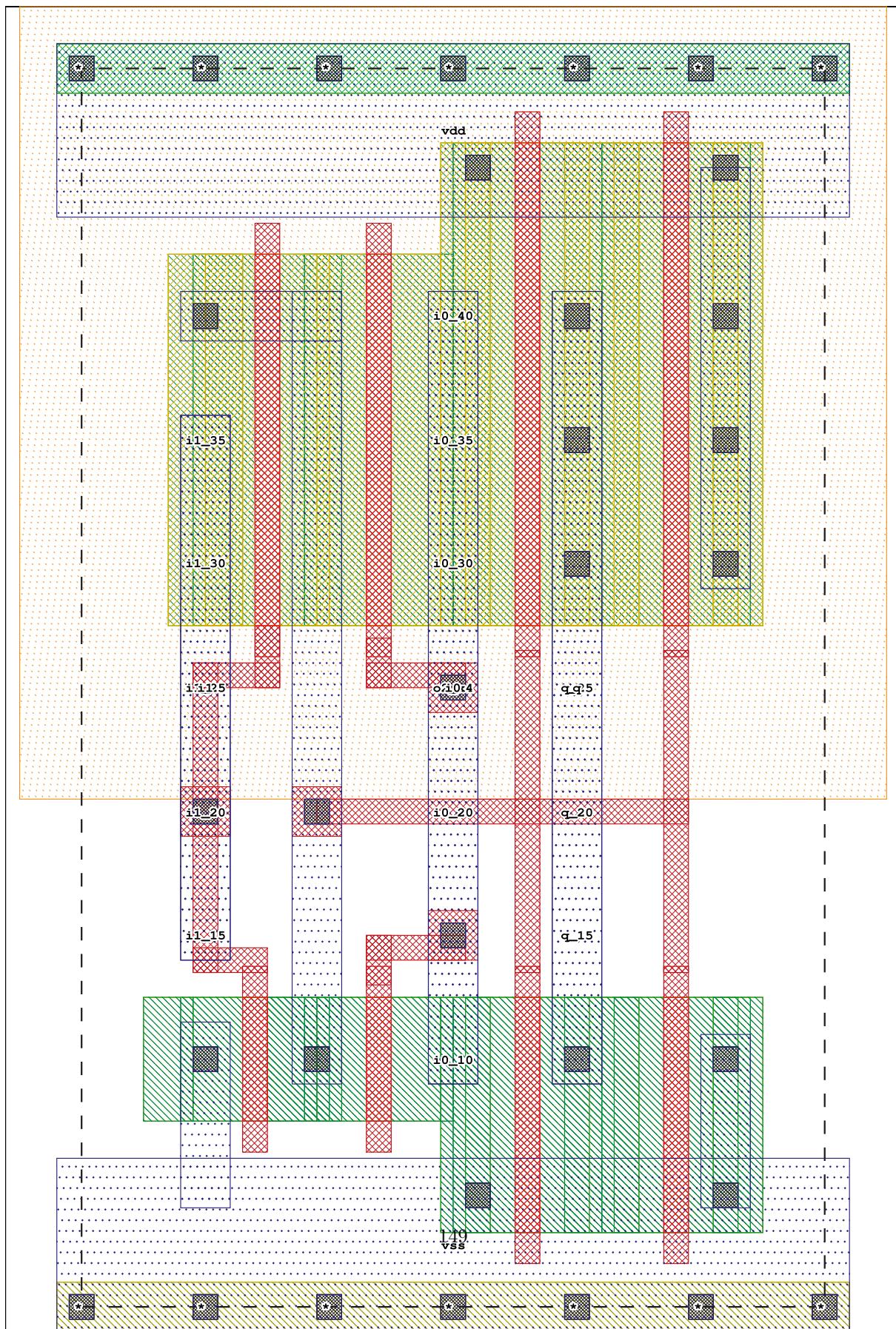


## 4.60 o2\_x4

```
ENTITY o2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT tpll_i0_q      : NATURAL := 394;
    CONSTANT tphh_i1_q      : NATURAL := 427;
    CONSTANT tpll_i1_q      : NATURAL := 464;
    CONSTANT tphh_i0_q      : NATURAL := 491;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END o2_x4;

ARCHITECTURE behaviour_data_flow OF o2_x4 IS

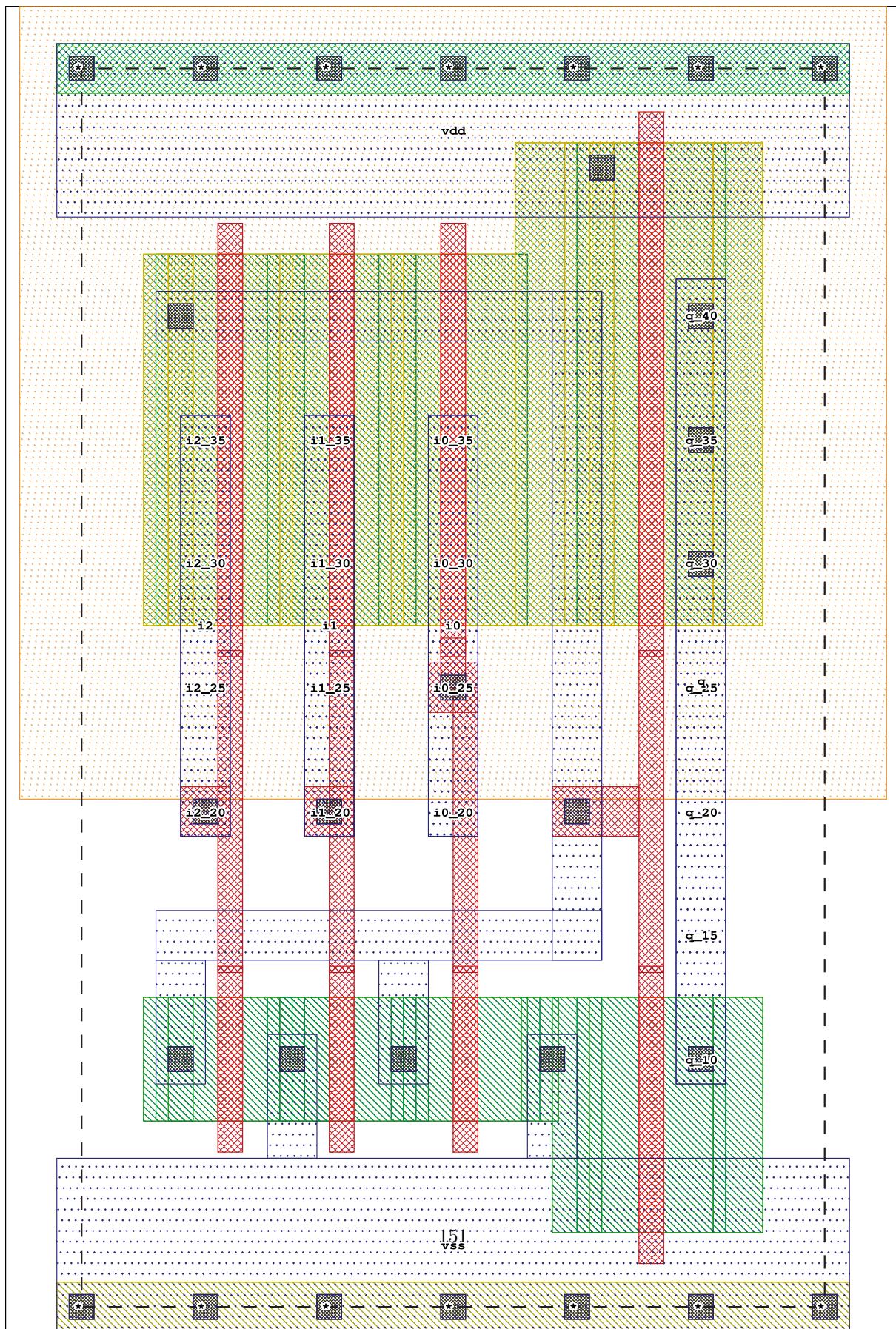
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on o2_x4"
  SEVERITY WARNING;
  q <= (i0 or i1) after 1100 ps;
END;
```



## 4.61 o3\_x2

```
ENTITY o3_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT tphh_i2_q      : NATURAL := 360;
    CONSTANT tp1l_i0_q       : NATURAL := 407;
    CONSTANT tp1l_i1_q       : NATURAL := 430;
    CONSTANT tp1l_i1_q       : NATURAL := 482;
    CONSTANT tp1h_i0_q       : NATURAL := 494;
    CONSTANT tp1l_i2_q       : NATURAL := 506;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END o3_x2;
```

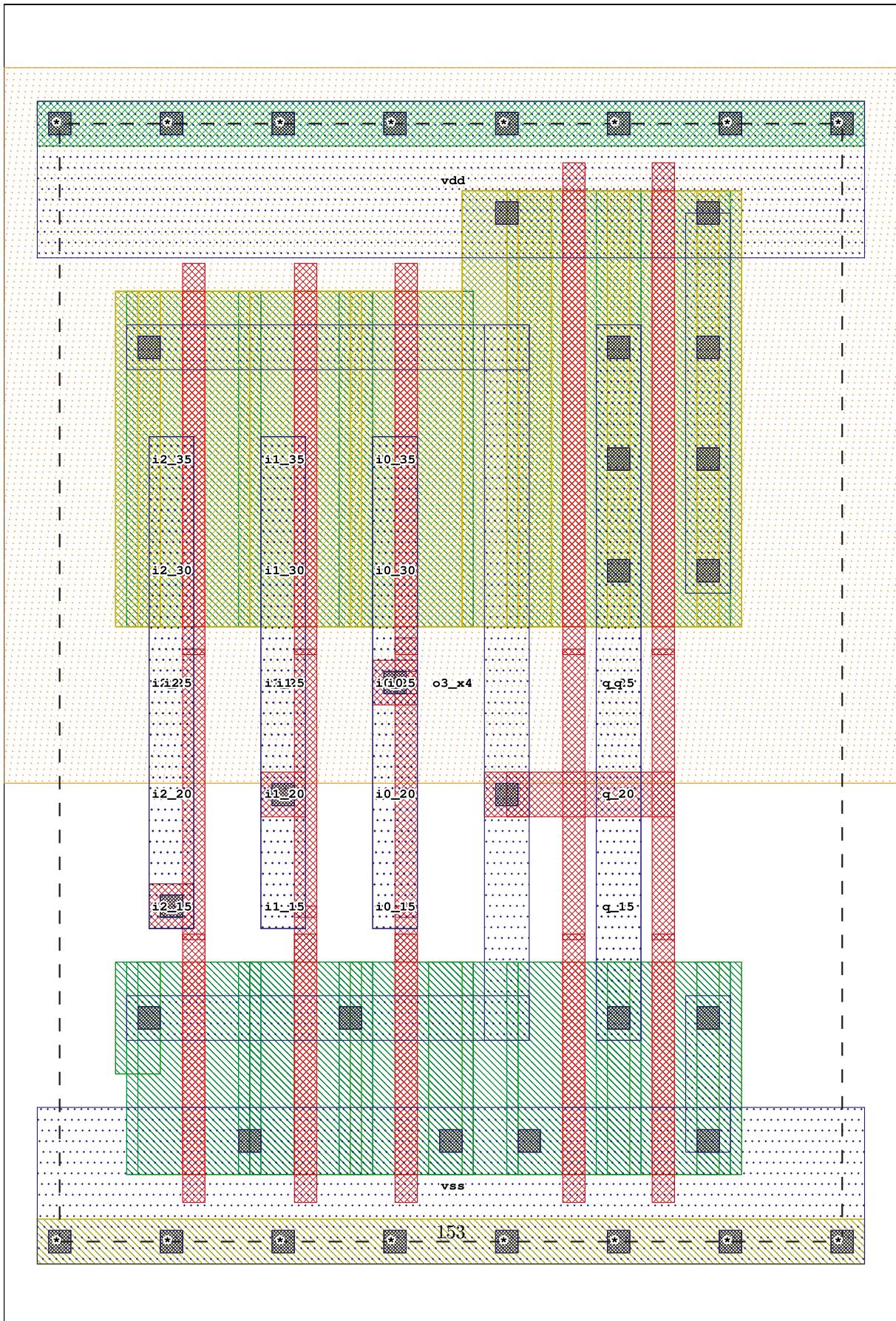
```
ARCHITECTURE behaviour_data_flow OF o3_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on o3_x2"
  SEVERITY WARNING;
  q <= ((i0 or i1) or i2) after 1100 ps;
END;
```



#### 4.62 o3\_x4

```
ENTITY o3_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT tphh_i2_q      : NATURAL := 447;
    CONSTANT tp1l_i0_q       : NATURAL := 501;
    CONSTANT tp1h_i1_q       : NATURAL := 510;
    CONSTANT tp1h_i0_q       : NATURAL := 569;
    CONSTANT tp1l_i1_q       : NATURAL := 585;
    CONSTANT tp1l_i2_q       : NATURAL := 622;
    CONSTANT transistors    : NATURAL := 10
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END o3_x4;
```

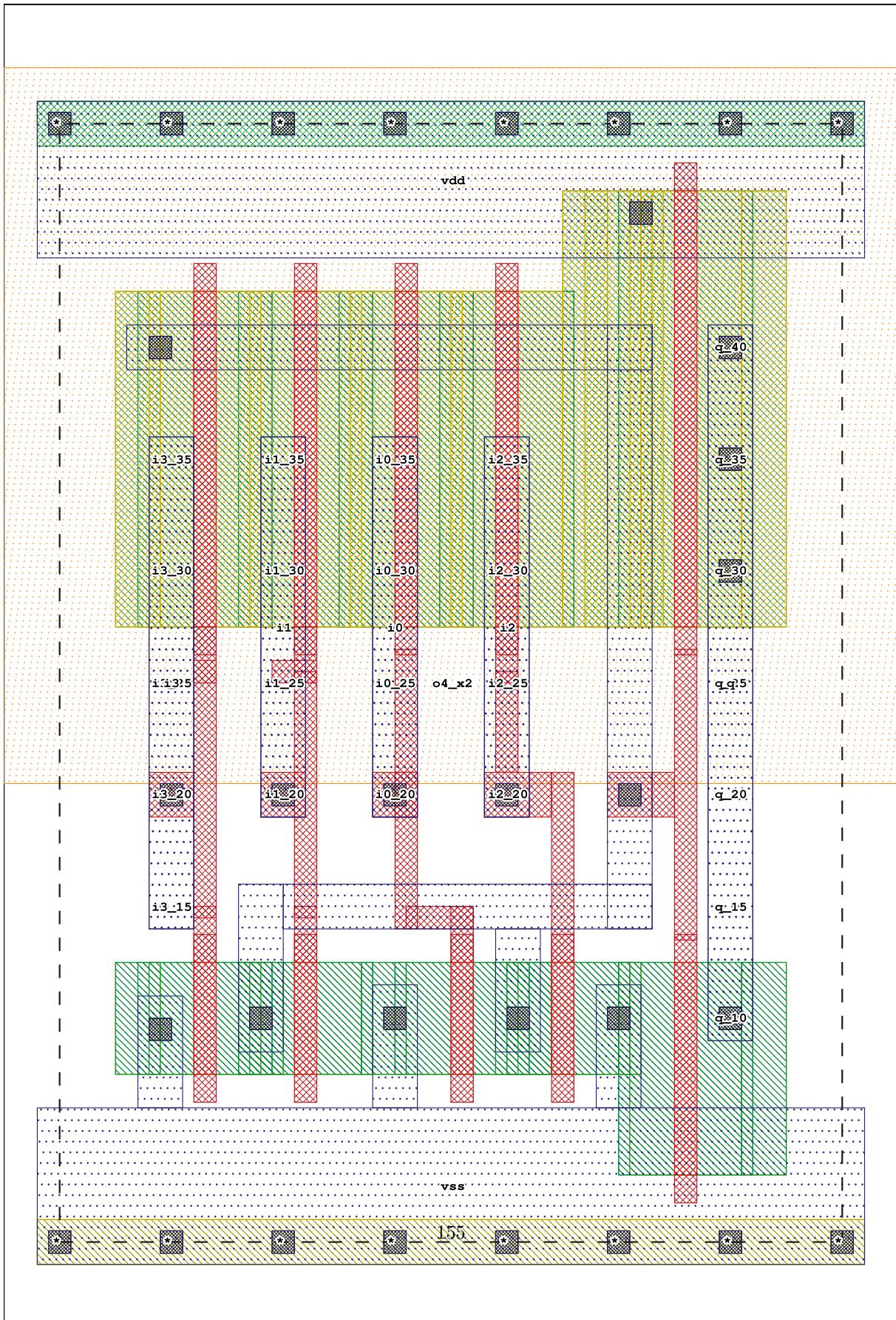
```
ARCHITECTURE behaviour_data_flow OF o3_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on o3_x4"
  SEVERITY WARNING;
  q <= ((i0 or i1) or i2) after 1200 ps;
END;
```



#### 4.63 o4\_x2

```
ENTITY o4_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT cin_i2         : NATURAL := 10;
    CONSTANT cin_i3         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rdown_i3_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT rup_i3_q       : NATURAL := 1790;
    CONSTANT tphh_i3_q      : NATURAL := 378;
    CONSTANT tphh_i1_q      : NATURAL := 446;
    CONSTANT tphh_i0_q      : NATURAL := 508;
    CONSTANT tpLL_i2_q      : NATURAL := 531;
    CONSTANT tpLL_i2_q      : NATURAL := 567;
    CONSTANT tpLL_i0_q      : NATURAL := 601;
    CONSTANT tpLL_i3_q      : NATURAL := 626;
    CONSTANT tpLL_i1_q      : NATURAL := 631;
    CONSTANT transistors    : NATURAL := 10
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END o4_x2;
```

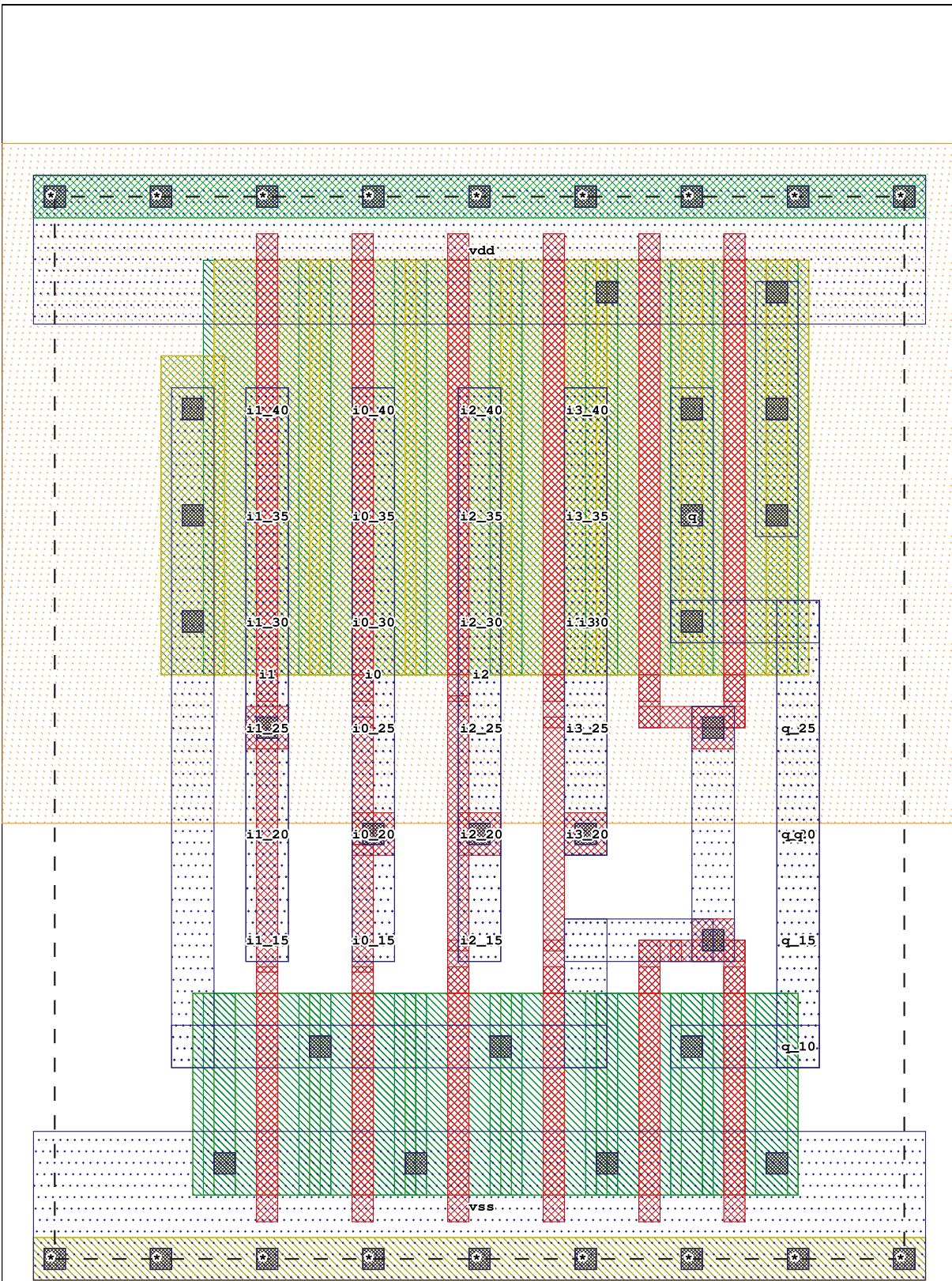
```
ARCHITECTURE behaviour_data_flow OF o4_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
    REPORT "power supply is missing on o4_x2"
    SEVERITY WARNING;
  q <= (((i0 or i1) or i2) or i3) after 1200 ps;
END;
```



#### 4.64 o4\_x4

```
ENTITY o4_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 12;
    CONSTANT cin_i1         : NATURAL := 12;
    CONSTANT cin_i2         : NATURAL := 12;
    CONSTANT cin_i3         : NATURAL := 12;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rdown_i3_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT tphh_i1_q      : NATURAL := 492;
    CONSTANT tp11_i3_q      : NATURAL := 536;
    CONSTANT tphh_i0_q      : NATURAL := 574;
    CONSTANT tp11_i2_q      : NATURAL := 611;
    CONSTANT tp11_i0_q      : NATURAL := 638;
    CONSTANT tphh_i2_q      : NATURAL := 649;
    CONSTANT tp11_i1_q      : NATURAL := 650;
    CONSTANT tphh_i3_q      : NATURAL := 721;
    CONSTANT transistors    : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END o4_x4;
```

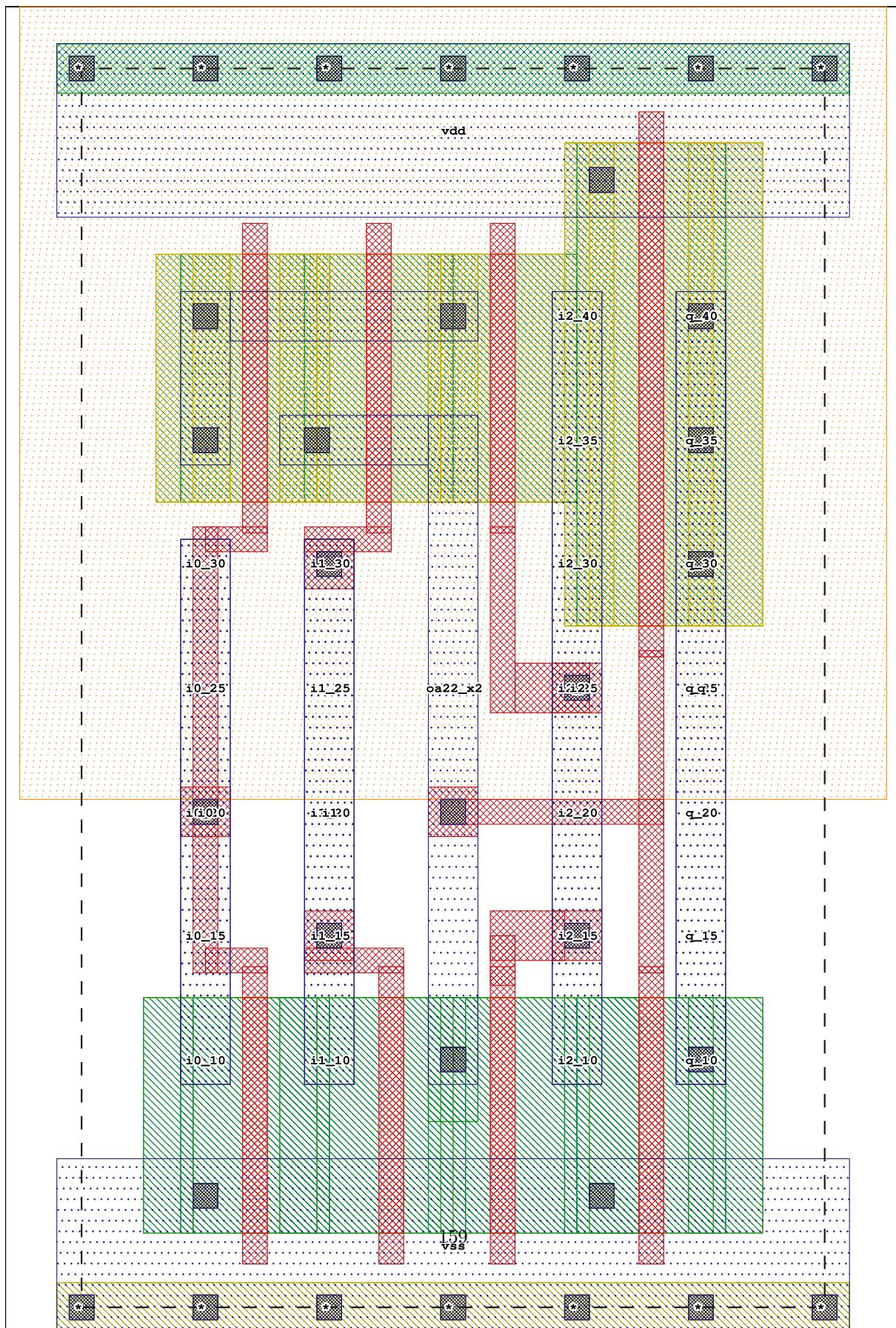
```
ARCHITECTURE behaviour_data_flow OF o4_x4 IS
  BEGIN
    ASSERT ((vdd and not (vss)) = '1')
      REPORT "power supply is missing on o4_x4"
      SEVERITY WARNING;
    q <= (((i0 or i1) or i2) or i3) after 1300 ps;
  END;
```



#### 4.65 oa22\_x2

```
ENTITY oa22_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1500;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT tphh_i0_q      : NATURAL := 390;
    CONSTANT tphh_i2_q      : NATURAL := 438;
    CONSTANT tpll_i2_q      : NATURAL := 454;
    CONSTANT tphh_i1_q      : NATURAL := 488;
    CONSTANT tpll_i1_q      : NATURAL := 525;
    CONSTANT tpll_i0_q      : NATURAL := 555;
    CONSTANT transistors    : NATURAL := 8
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oa22_x2;
```

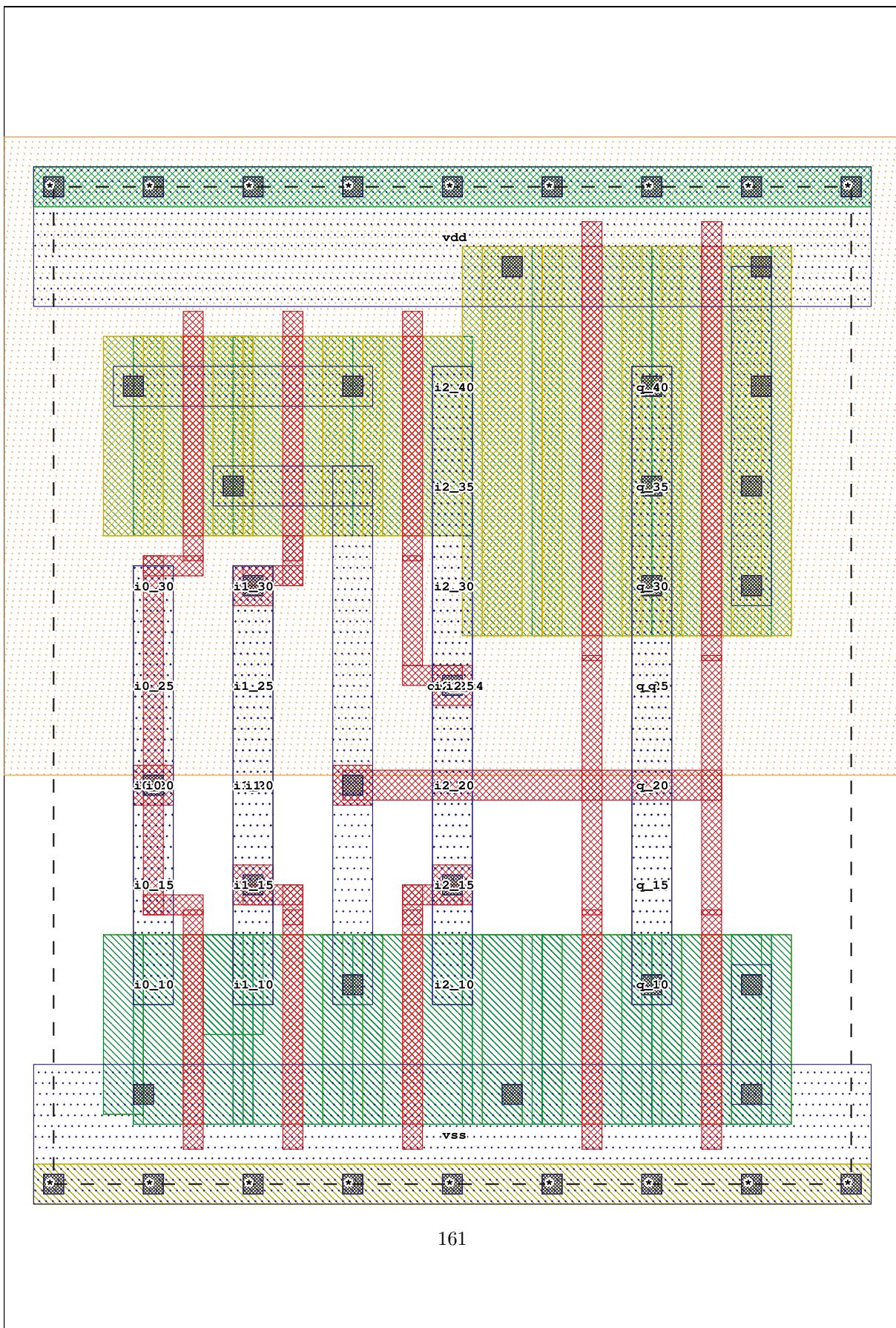
```
ARCHITECTURE behaviour_data_flow OF oa22_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa22_x2"
  SEVERITY WARNING;
  q <= ((i0 and i1) or i2) after 1200 ps;
END;
```



#### 4.66 oa22\_x4

```
ENTITY oa22_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT tphh_i0_q      : NATURAL := 511;
    CONSTANT tphh_i2_q      : NATURAL := 523;
    CONSTANT tp1l_i2_q       : NATURAL := 571;
    CONSTANT tp1l_i1_q       : NATURAL := 615;
    CONSTANT tp1l_i0_q       : NATURAL := 650;
    CONSTANT transistors    : NATURAL := 677;
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oa22_x4;
```

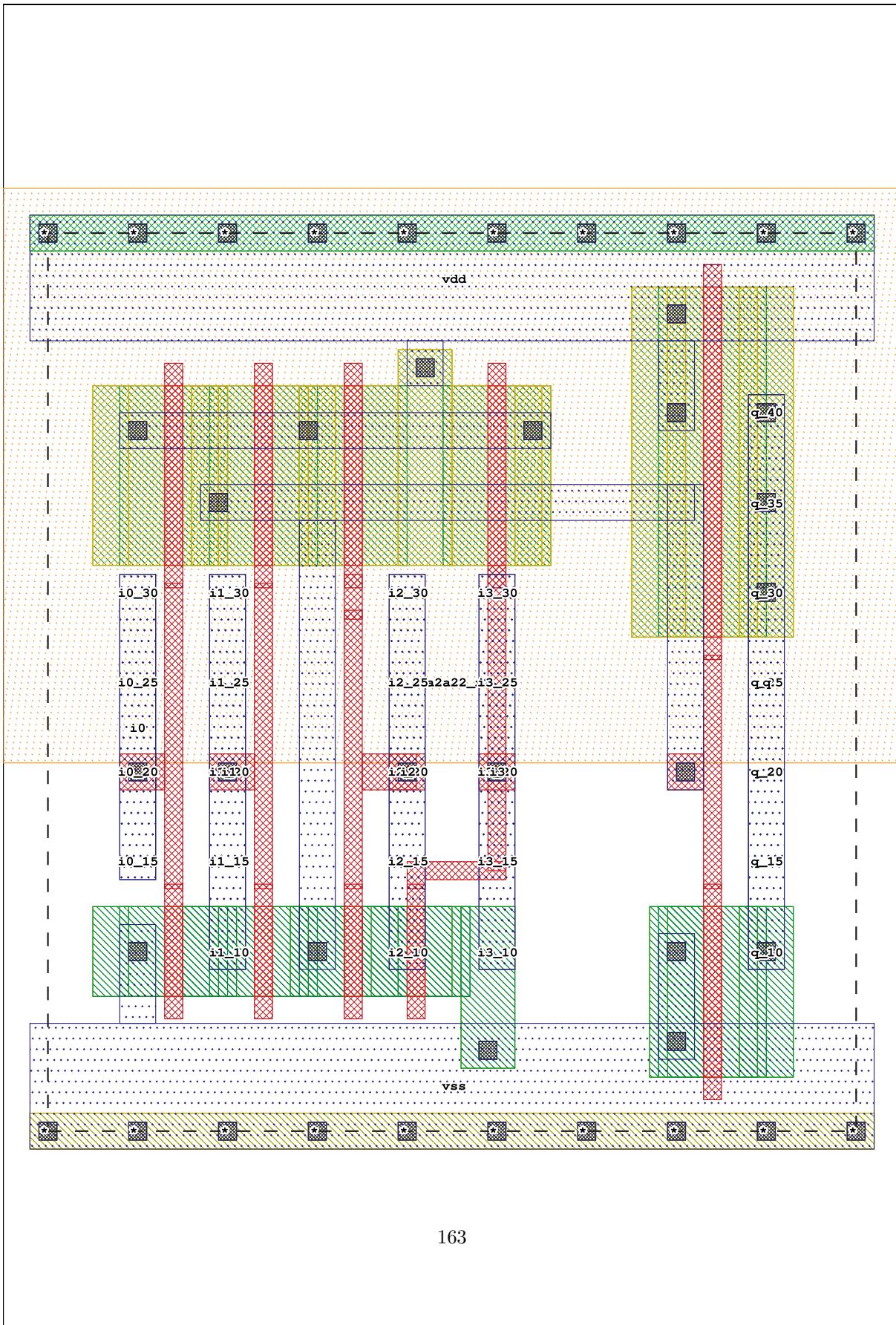
```
ARCHITECTURE behaviour_data_flow OF oa22_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa22_x4"
  SEVERITY WARNING;
  q <= ((i0 and i1) or i2) after 1300 ps;
END;
```



#### 4.67 oa2a22\_x2

```
ENTITY oa2a22_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2250;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT cin_i3         : NATURAL := 8;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rdown_i3_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT rup_i3_q       : NATURAL := 1790;
    CONSTANT tphh_i0_q      : NATURAL := 403;
    CONSTANT tp11_i2_q      : NATURAL := 487;
    CONSTANT tp11_i1_q      : NATURAL := 495;
    CONSTANT tp11_i3_q      : NATURAL := 512;
    CONSTANT tp11_i1_q      : NATURAL := 534;
    CONSTANT tp11_i3_q      : NATURAL := 537;
    CONSTANT tp11_i0_q      : NATURAL := 564;
    CONSTANT tp11_i2_q      : NATURAL := 646;
    CONSTANT transistors    : NATURAL := 10
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oa2a22_x2;

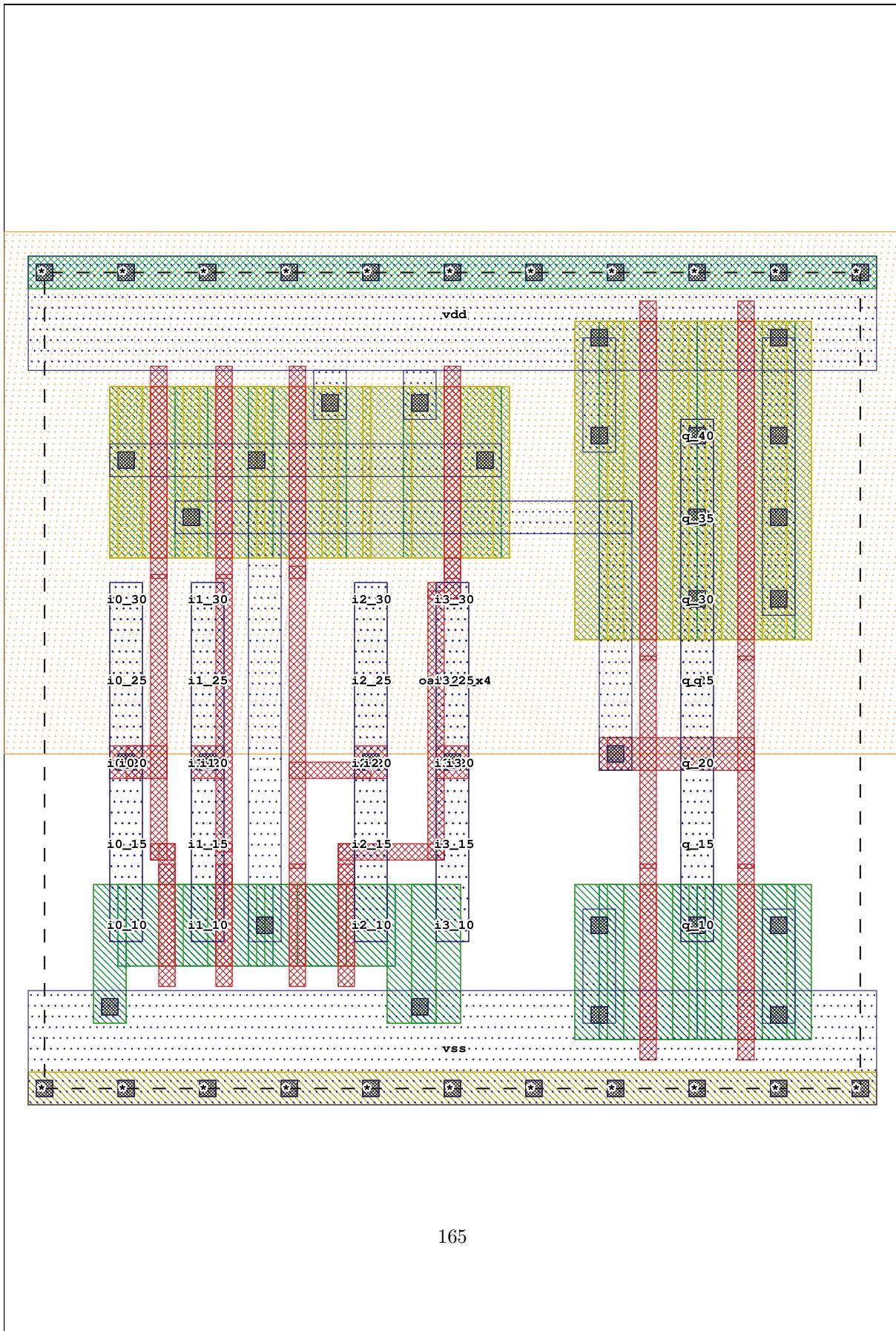
ARCHITECTURE behaviour_data_flow OF oa2a22_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2a22_x2"
  SEVERITY WARNING;
  q <= ((i0 and i1) or (i2 and i3)) after 1200 ps;
END;
```



#### 4.68 oa2a22\_x4

```
ENTITY oa2a22_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2500;
    CONSTANT cin_i0         : NATURAL := 8;
    CONSTANT cin_i1         : NATURAL := 8;
    CONSTANT cin_i2         : NATURAL := 8;
    CONSTANT cin_i3         : NATURAL := 8;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rdown_i3_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT tphh_i0_q      : NATURAL := 519;
    CONSTANT tp11_i2_q      : NATURAL := 596;
    CONSTANT tp11_i3_q      : NATURAL := 619;
    CONSTANT tp11_i1_q      : NATURAL := 624;
    CONSTANT tp11_i3_q      : NATURAL := 644;
    CONSTANT tp11_i1_q      : NATURAL := 669;
    CONSTANT tp11_i0_q      : NATURAL := 696;
    CONSTANT tp11_i2_q      : NATURAL := 763;
    CONSTANT transistors    : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oa2a22_x4;

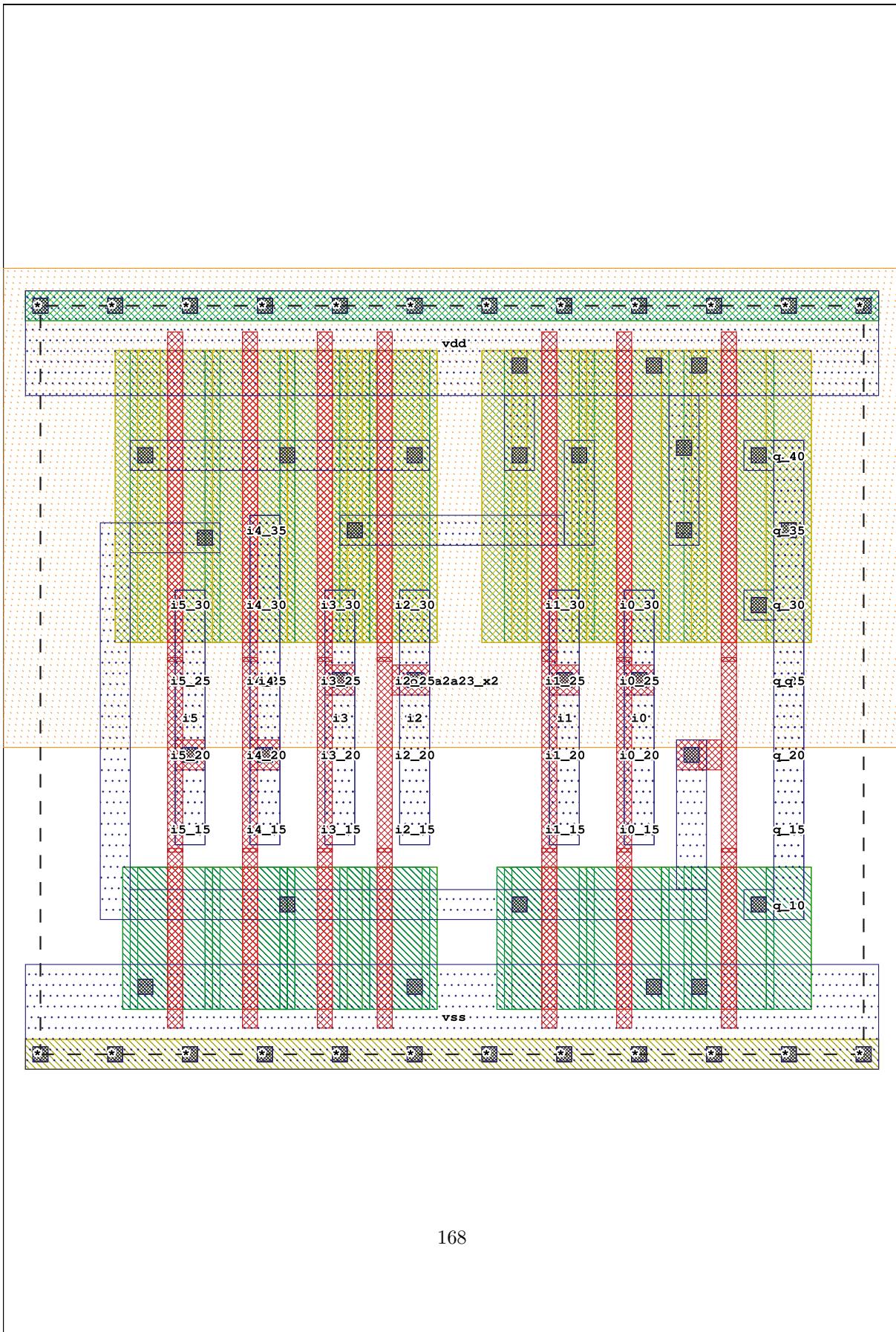
ARCHITECTURE behaviour_data_flow OF oa2a22_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2a22_x4"
  SEVERITY WARNING;
  q <= ((i0 and i1) or (i2 and i3)) after 1400 ps;
END;
```



#### 4.69 oa2a2a23\_x2

```
ENTITY oa2a2a23_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3000;
    CONSTANT cin_i0         : NATURAL := 13;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 14;
    CONSTANT cin_i4         : NATURAL := 14;
    CONSTANT cin_i5         : NATURAL := 14;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rdown_i3_q     : NATURAL := 1620;
    CONSTANT rdown_i4_q     : NATURAL := 1620;
    CONSTANT rdown_i5_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT rup_i3_q       : NATURAL := 1790;
    CONSTANT rup_i4_q       : NATURAL := 1790;
    CONSTANT rup_i5_q       : NATURAL := 1790;
    CONSTANT tphh_i5_q      : NATURAL := 321;
    CONSTANT tphh_i4_q      : NATURAL := 402;
    CONSTANT tphh_i2_q      : NATURAL := 441;
    CONSTANT tphh_i3_q      : NATURAL := 540;
    CONSTANT tp11_i1_q       : NATURAL := 542;
    CONSTANT tp11_i0_q       : NATURAL := 578;
    CONSTANT tp11_i4_q       : NATURAL := 591;
    CONSTANT tp11_i3_q       : NATURAL := 600;
    CONSTANT tp11_i5_q       : NATURAL := 636;
    CONSTANT tp11_i2_q       : NATURAL := 639;
    CONSTANT tphh_i0_q       : NATURAL := 653;
    CONSTANT tphh_i1_q       : NATURAL := 775;
    CONSTANT transistors    : NATURAL := 14
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    i5      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oa2a2a23_x2;
```

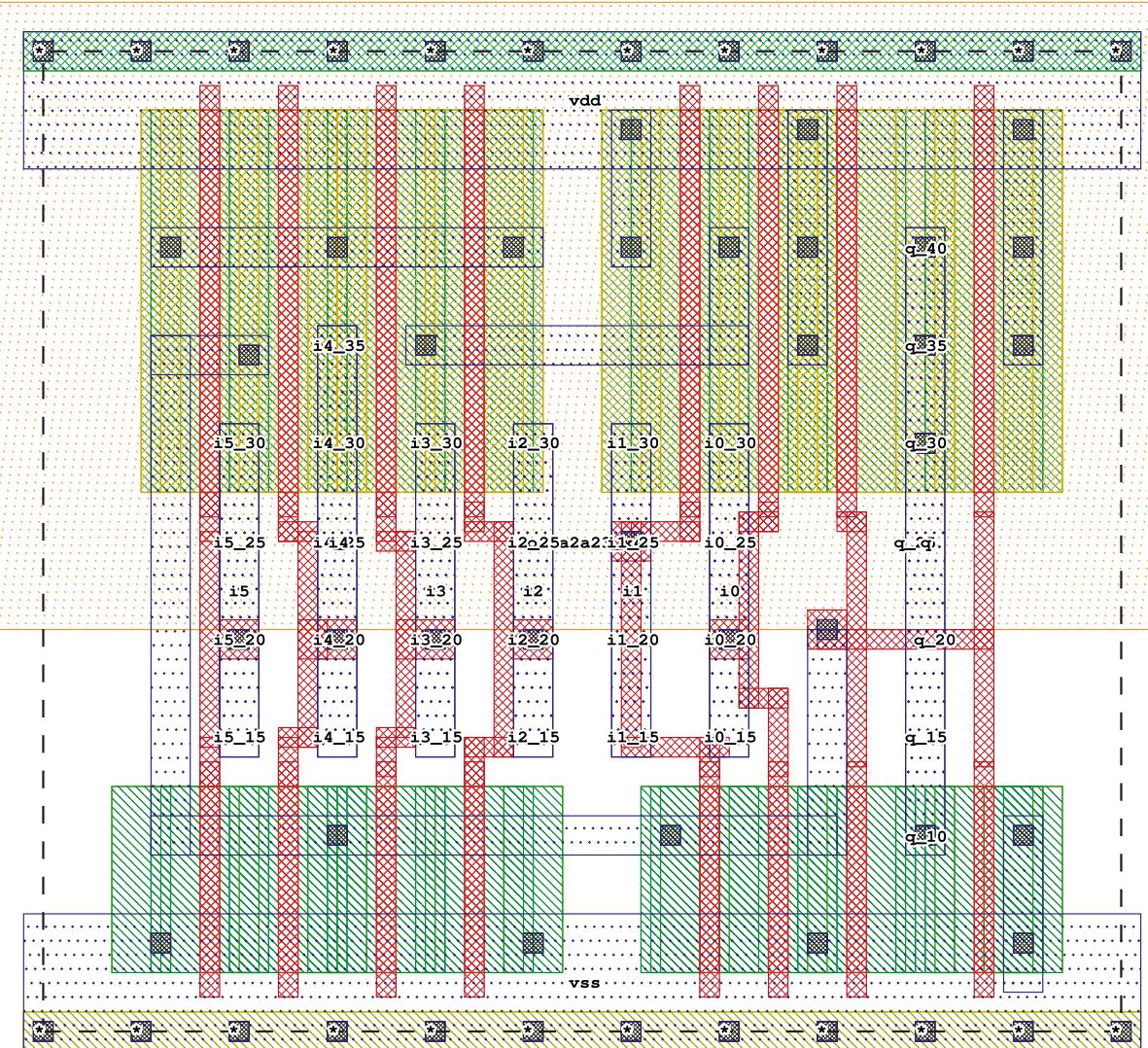
```
ARCHITECTURE behaviour_data_flow OF oa2a2a23_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2a2a23_x2"
  SEVERITY WARNING;
  q <= (((i0 and i1) or (i2 and i3)) or (i4 and i5)) after 1400 ps;
END;
```



#### 4.70 oa2a2a23\_x4

```
ENTITY oa2a2a23_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3250;
    CONSTANT cin_i0         : NATURAL := 13;
    CONSTANT cin_i1         : NATURAL := 14;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 14;
    CONSTANT cin_i4         : NATURAL := 14;
    CONSTANT cin_i5         : NATURAL := 14;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rdown_i3_q     : NATURAL := 810;
    CONSTANT rdown_i4_q     : NATURAL := 810;
    CONSTANT rdown_i5_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT rup_i4_q       : NATURAL := 890;
    CONSTANT rup_i5_q       : NATURAL := 890;
    CONSTANT tphh_i5_q      : NATURAL := 379;
    CONSTANT tphh_i4_q      : NATURAL := 464;
    CONSTANT tphh_i2_q      : NATURAL := 493;
    CONSTANT tphh_i3_q      : NATURAL := 594;
    CONSTANT tp11_i1_q       : NATURAL := 613;
    CONSTANT tp11_i0_q       : NATURAL := 648;
    CONSTANT tp11_i4_q       : NATURAL := 673;
    CONSTANT tp11_i3_q       : NATURAL := 677;
    CONSTANT tphh_i0_q       : NATURAL := 699;
    CONSTANT tp11_i5_q       : NATURAL := 714;
    CONSTANT tp11_i2_q       : NATURAL := 715;
    CONSTANT tphh_i1_q       : NATURAL := 822;
    CONSTANT transistors    : NATURAL := 16
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    i5      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oa2a2a23_x4;
```

```
ARCHITECTURE behaviour_data_flow OF oa2a2a23_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2a2a23_x4"
  SEVERITY WARNING;
  q <= (((i0 and i1) or (i2 and i3)) or (i4 and i5)) after 1400 ps;
END;
```



#### 4.71 oa2a2a2a24\_x2

```
ENTITY oa2a2a2a24_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3750;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 13;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 13;
    CONSTANT cin_i4         : NATURAL := 13;
    CONSTANT cin_i5         : NATURAL := 13;
    CONSTANT cin_i6         : NATURAL := 14;
    CONSTANT cin_i7         : NATURAL := 14;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rdown_i3_q     : NATURAL := 1620;
    CONSTANT rdown_i4_q     : NATURAL := 1620;
    CONSTANT rdown_i5_q     : NATURAL := 1620;
    CONSTANT rdown_i6_q     : NATURAL := 1620;
    CONSTANT rdown_i7_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT rup_i3_q       : NATURAL := 1790;
    CONSTANT rup_i4_q       : NATURAL := 1790;
    CONSTANT rup_i5_q       : NATURAL := 1790;
    CONSTANT rup_i6_q       : NATURAL := 1790;
    CONSTANT rup_i7_q       : NATURAL := 1790;
    CONSTANT tphh_i7_q      : NATURAL := 346;
    CONSTANT tphh_i6_q      : NATURAL := 426;
    CONSTANT tphh_i5_q      : NATURAL := 467;
    CONSTANT tphh_i4_q      : NATURAL := 565;
    CONSTANT tphh_i2_q      : NATURAL := 682;
    CONSTANT tp11_i6_q      : NATURAL := 748;
    CONSTANT tp11_i1_q      : NATURAL := 753;
    CONSTANT tp11_i0_q      : NATURAL := 780;
    CONSTANT tp11_i0_q      : NATURAL := 797;
    CONSTANT tp11_i7_q      : NATURAL := 800;
    CONSTANT tphh_i3_q      : NATURAL := 803;
    CONSTANT tp11_i3_q      : NATURAL := 810;
    CONSTANT tp11_i4_q      : NATURAL := 813;
    CONSTANT tp11_i2_q      : NATURAL := 856;
    CONSTANT tp11_i5_q      : NATURAL := 861;
    CONSTANT tphh_i1_q      : NATURAL := 909;
    CONSTANT transistors    : NATURAL := 18
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
```

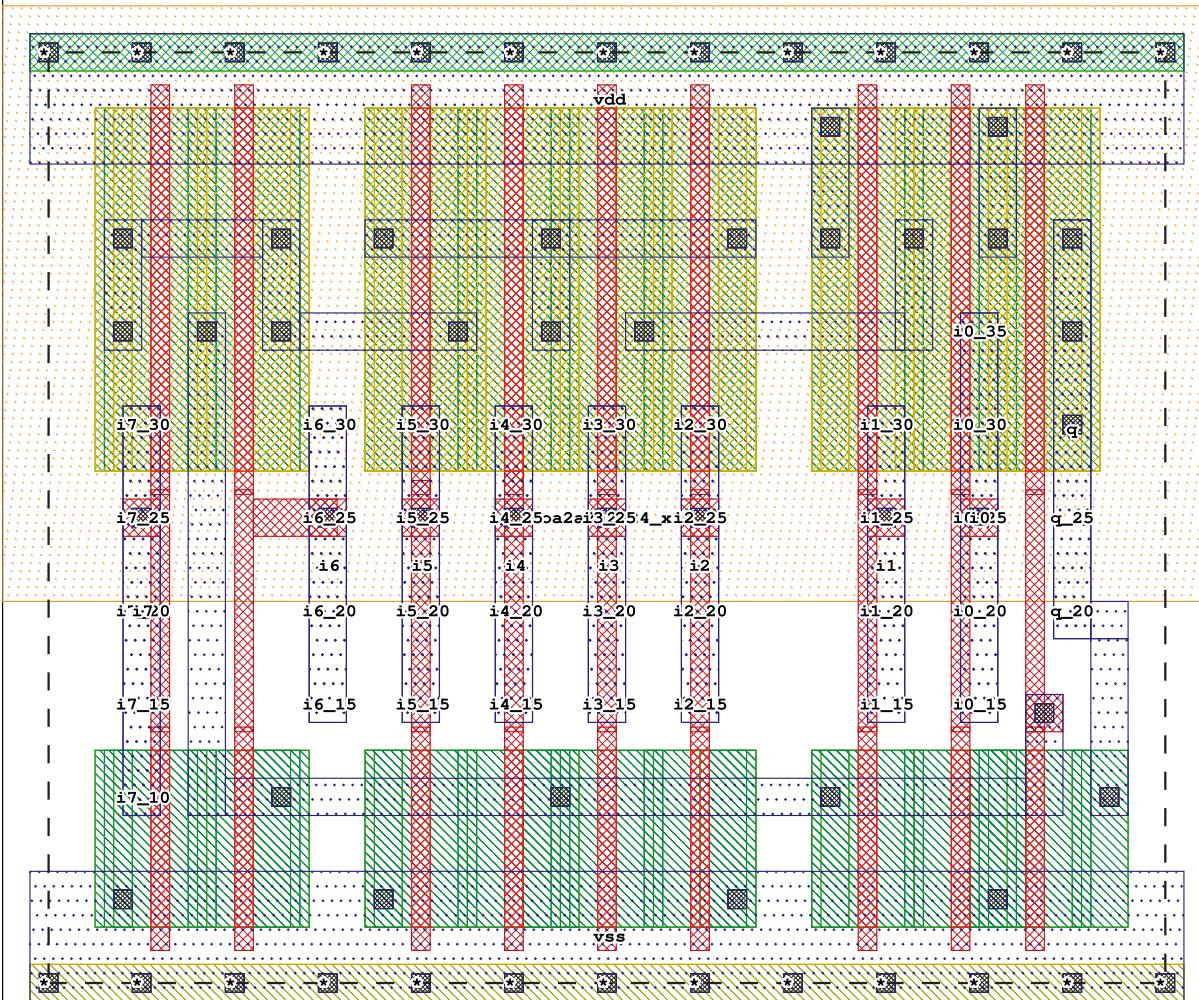
```

i2      : in  BIT;
i3      : in  BIT;
i4      : in  BIT;
i5      : in  BIT;
i6      : in  BIT;
i7      : in  BIT;
q       : out BIT;
vdd    : in  BIT;
vss    : in  BIT
);
END oa2a2a2a24_x2;

ARCHITECTURE behaviour_data_flow OF oa2a2a2a24_x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2a2a2a24_x2"
  SEVERITY WARNING;
  q <= (((i0 and i1) or (i2 and i3)) or (i4 and i5)) or (i6 and i7)) after 1500 ps;
END;

```



#### 4.72 oa2a2a2a24\_x4

```
ENTITY oa2a2a2a24_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4000;
    CONSTANT cin_i0         : NATURAL := 14;
    CONSTANT cin_i1         : NATURAL := 13;
    CONSTANT cin_i2         : NATURAL := 14;
    CONSTANT cin_i3         : NATURAL := 13;
    CONSTANT cin_i4         : NATURAL := 13;
    CONSTANT cin_i5         : NATURAL := 13;
    CONSTANT cin_i6         : NATURAL := 14;
    CONSTANT cin_i7         : NATURAL := 14;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rdown_i3_q     : NATURAL := 810;
    CONSTANT rdown_i4_q     : NATURAL := 810;
    CONSTANT rdown_i5_q     : NATURAL := 810;
    CONSTANT rdown_i6_q     : NATURAL := 810;
    CONSTANT rdown_i7_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT rup_i4_q       : NATURAL := 890;
    CONSTANT rup_i5_q       : NATURAL := 890;
    CONSTANT rup_i6_q       : NATURAL := 890;
    CONSTANT rup_i7_q       : NATURAL := 890;
    CONSTANT tphh_i7_q      : NATURAL := 399;
    CONSTANT tphh_i6_q      : NATURAL := 487;
    CONSTANT tphh_i5_q      : NATURAL := 515;
    CONSTANT tphh_i4_q      : NATURAL := 619;
    CONSTANT tphh_i2_q      : NATURAL := 726;
    CONSTANT tphh_i0_q      : NATURAL := 823;
    CONSTANT tp11_i1_q       : NATURAL := 835;
    CONSTANT tp11_i6_q       : NATURAL := 845;
    CONSTANT tp11_i3_q       : NATURAL := 851;
    CONSTANT tp11_i0_q       : NATURAL := 879;
    CONSTANT tp11_i3_q       : NATURAL := 895;
    CONSTANT tp11_i7_q       : NATURAL := 895;
    CONSTANT tp11_i4_q       : NATURAL := 902;
    CONSTANT tp11_i2_q       : NATURAL := 940;
    CONSTANT tp11_i5_q       : NATURAL := 949;
    CONSTANT tphh_i1_q       : NATURAL := 955;
    CONSTANT transistors     : NATURAL := 20
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
```

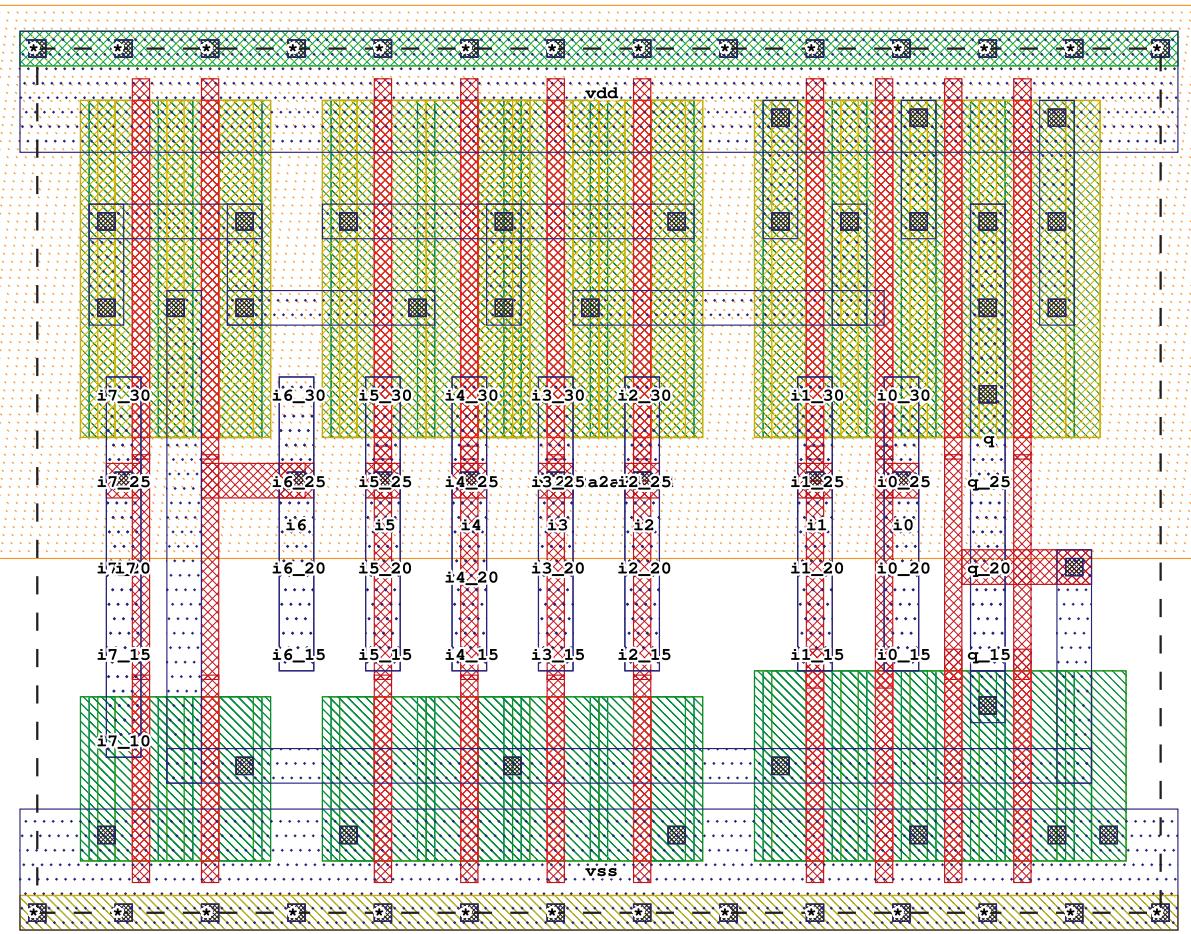
```

i2      : in  BIT;
i3      : in  BIT;
i4      : in  BIT;
i5      : in  BIT;
i6      : in  BIT;
i7      : in  BIT;
q       : out BIT;
vdd     : in  BIT;
vss     : in  BIT
);
END oa2a2a2a24_x4;

ARCHITECTURE behaviour_data_flow OF oa2a2a2a24_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2a2a2a24_x4"
  SEVERITY WARNING;
  q <= (((i0 and i1) or (i2 and i3)) or (i4 and i5)) or (i6 and i7)) after 1600 ps;
END;

```

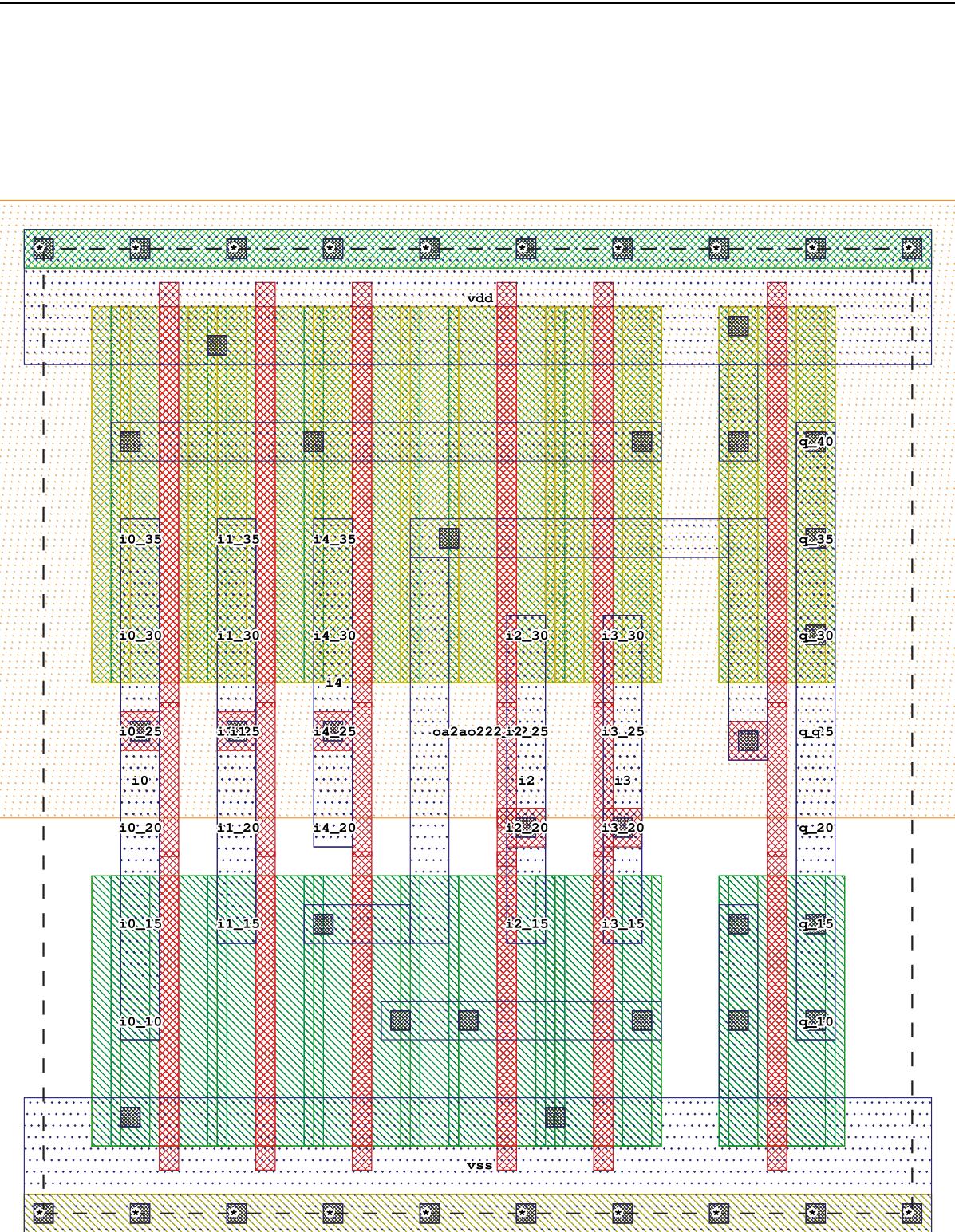


#### 4.73 oa2ao222\_x2

```
ENTITY oa2ao222_x2 IS
  GENERIC (
    CONSTANT area : NATURAL := 2500;
    CONSTANT cin_i0 : NATURAL := 11;
    CONSTANT cin_i1 : NATURAL := 11;
    CONSTANT cin_i2 : NATURAL := 11;
    CONSTANT cin_i3 : NATURAL := 11;
    CONSTANT cin_i4 : NATURAL := 11;
    CONSTANT rdown_i0_q : NATURAL := 1620;
    CONSTANT rdown_i1_q : NATURAL := 1620;
    CONSTANT rdown_i2_q : NATURAL := 1620;
    CONSTANT rdown_i3_q : NATURAL := 1620;
    CONSTANT rdown_i4_q : NATURAL := 1620;
    CONSTANT rup_i0_q : NATURAL := 1790;
    CONSTANT rup_i1_q : NATURAL := 1790;
    CONSTANT rup_i2_q : NATURAL := 1790;
    CONSTANT rup_i3_q : NATURAL := 1790;
    CONSTANT rup_i4_q : NATURAL := 1790;
    CONSTANT tp11_i4_q : NATURAL := 453;
    CONSTANT tphh_i2_q : NATURAL := 464;
    CONSTANT tphh_i0_q : NATURAL := 495;
    CONSTANT tp11_i1_q : NATURAL := 539;
    CONSTANT tphh_i3_q : NATURAL := 556;
    CONSTANT tphh_i4_q : NATURAL := 558;
    CONSTANT tp11_i3_q : NATURAL := 578;
    CONSTANT tp11_i0_q : NATURAL := 581;
    CONSTANT tphh_i1_q : NATURAL := 598;
    CONSTANT tp11_i2_q : NATURAL := 604;
    CONSTANT transistors : NATURAL := 12
  );
  PORT (
    i0 : in BIT;
    i1 : in BIT;
    i2 : in BIT;
    i3 : in BIT;
    i4 : in BIT;
    q : out BIT;
    vdd : in BIT;
    vss : in BIT
  );
END oa2ao222_x2;

ARCHITECTURE behaviour_data_flow OF oa2ao222_x2 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2ao222_x2"
  SEVERITY WARNING;
```

```
q <= ((i0 and i1) or (i4 and (i2 or i3))) after 1200 ps;  
END;
```

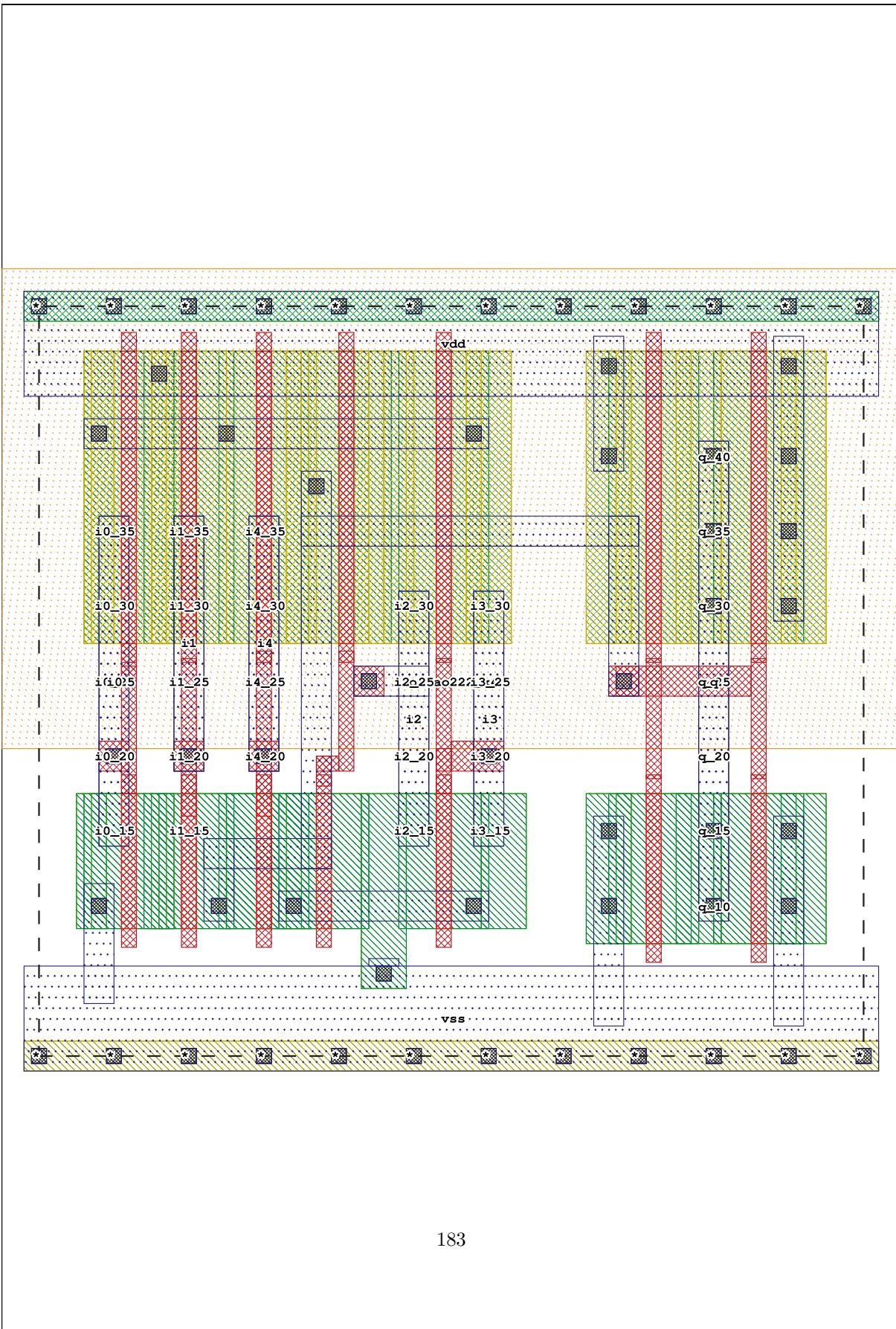


#### 4.74 oa2ao222\_x4

```
ENTITY oa2ao222_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2750;
    CONSTANT cin_i0         : NATURAL := 11;
    CONSTANT cin_i1         : NATURAL := 11;
    CONSTANT cin_i2         : NATURAL := 11;
    CONSTANT cin_i3         : NATURAL := 11;
    CONSTANT cin_i4         : NATURAL := 11;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rdown_i3_q     : NATURAL := 810;
    CONSTANT rdown_i4_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT rup_i4_q       : NATURAL := 890;
    CONSTANT tp11_i4_q      : NATURAL := 529;
    CONSTANT tphh_i2_q      : NATURAL := 552;
    CONSTANT tphh_i0_q      : NATURAL := 553;
    CONSTANT tp11_i1_q      : NATURAL := 616;
    CONSTANT tphh_i3_q      : NATURAL := 640;
    CONSTANT tphh_i4_q      : NATURAL := 656;
    CONSTANT tp11_i0_q      : NATURAL := 657;
    CONSTANT tp11_i3_q      : NATURAL := 660;
    CONSTANT tphh_i1_q      : NATURAL := 662;
    CONSTANT tp11_i2_q      : NATURAL := 693;
    CONSTANT transistors    : NATURAL := 14
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END oa2ao222_x4;

ARCHITECTURE behaviour_data_flow OF oa2ao222_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa2ao222_x4"
  SEVERITY WARNING;
```

```
q <= ((i0 and i1) or (i4 and (i2 or i3))) after 1300 ps;  
END;
```



#### 4.75 oa3ao322\_x2

```
ENTITY oa3ao322_x2 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2750;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT cin_i3         : NATURAL := 9;
    CONSTANT cin_i4         : NATURAL := 9;
    CONSTANT cin_i5         : NATURAL := 9;
    CONSTANT cin_i6         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 1620;
    CONSTANT rdown_i1_q     : NATURAL := 1620;
    CONSTANT rdown_i2_q     : NATURAL := 1620;
    CONSTANT rdown_i3_q     : NATURAL := 1620;
    CONSTANT rdown_i4_q     : NATURAL := 1620;
    CONSTANT rdown_i5_q     : NATURAL := 1620;
    CONSTANT rdown_i6_q     : NATURAL := 1620;
    CONSTANT rup_i0_q       : NATURAL := 1790;
    CONSTANT rup_i1_q       : NATURAL := 1790;
    CONSTANT rup_i2_q       : NATURAL := 1790;
    CONSTANT rup_i3_q       : NATURAL := 1790;
    CONSTANT rup_i4_q       : NATURAL := 1790;
    CONSTANT rup_i5_q       : NATURAL := 1790;
    CONSTANT rup_i6_q       : NATURAL := 1790;
    CONSTANT tpll_i6_q      : NATURAL := 540;
    CONSTANT tphh_i3_q      : NATURAL := 560;
    CONSTANT tphh_i6_q      : NATURAL := 563;
    CONSTANT tphh_i0_q      : NATURAL := 638;
    CONSTANT tphh_i4_q      : NATURAL := 649;
    CONSTANT tpll_i2_q      : NATURAL := 707;
    CONSTANT tphh_i5_q      : NATURAL := 734;
    CONSTANT tpll_i5_q      : NATURAL := 734;
    CONSTANT tphh_i1_q      : NATURAL := 735;
    CONSTANT tpll_i4_q      : NATURAL := 760;
    CONSTANT tpll_i1_q      : NATURAL := 764;
    CONSTANT tpll_i3_q      : NATURAL := 765;
    CONSTANT tphh_i2_q      : NATURAL := 806;
    CONSTANT tpll_i0_q      : NATURAL := 820;
    CONSTANT transistors    : NATURAL := 16
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    i5      : in  BIT;
    i6      : in  BIT;
```

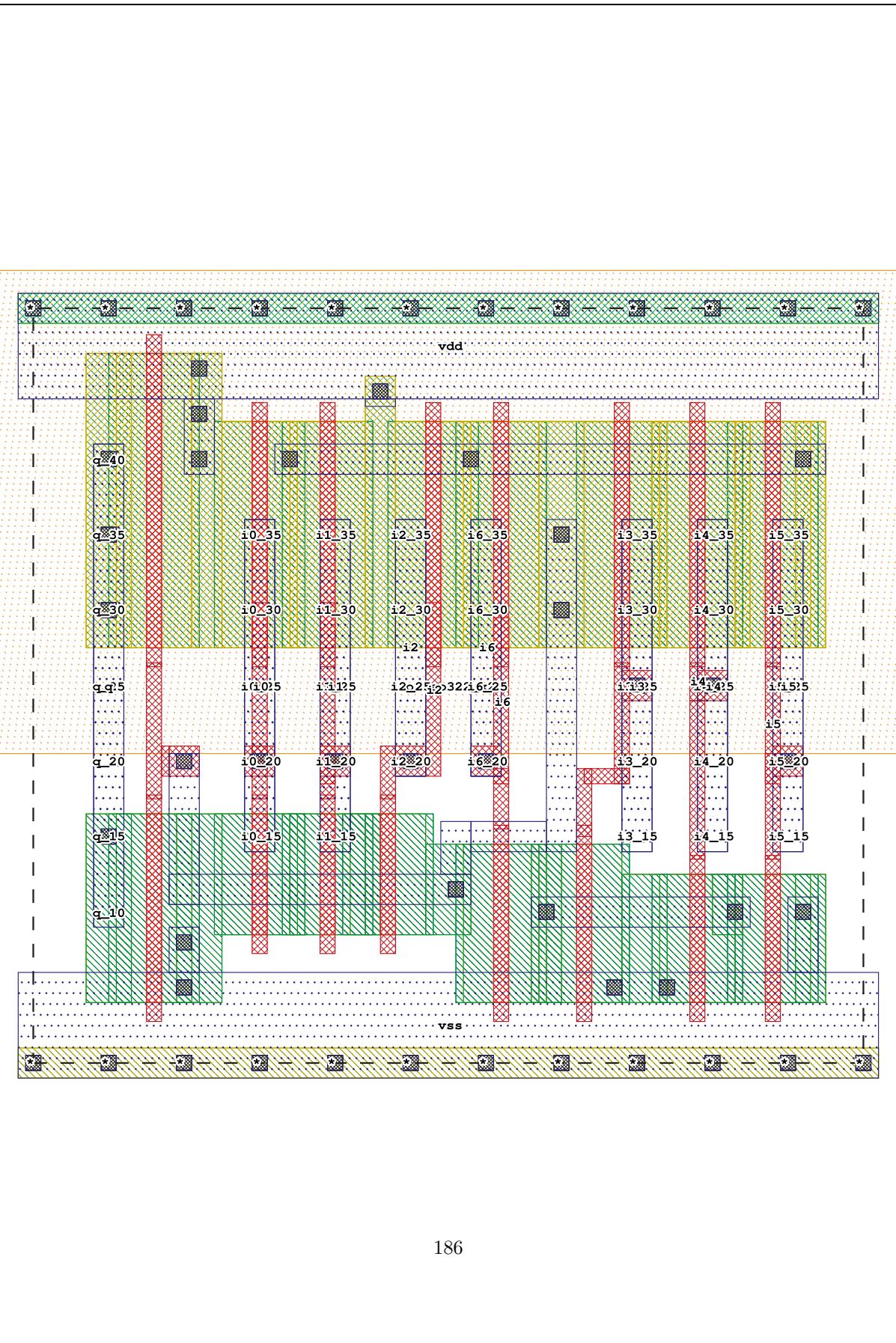
```

q      : out BIT;
vdd    : in  BIT;
vss    : in  BIT
);
END oa3ao322_x2;

ARCHITECTURE behaviour_data_flow OF oa3ao322_x2 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa3ao322_x2"
  SEVERITY WARNING;
  q <= (((i0 and i1) and i2) or (i6 and ((i3 or i4) or i5))) after 1400 ps;
END;

```



#### 4.76 oa3ao322\_x4

```
ENTITY oa3ao322_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3000;
    CONSTANT cin_i0         : NATURAL := 10;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT cin_i2         : NATURAL := 9;
    CONSTANT cin_i3         : NATURAL := 9;
    CONSTANT cin_i4         : NATURAL := 9;
    CONSTANT cin_i5         : NATURAL := 9;
    CONSTANT cin_i6         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rdown_i2_q     : NATURAL := 810;
    CONSTANT rdown_i3_q     : NATURAL := 810;
    CONSTANT rdown_i4_q     : NATURAL := 810;
    CONSTANT rdown_i5_q     : NATURAL := 810;
    CONSTANT rdown_i6_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT rup_i2_q       : NATURAL := 890;
    CONSTANT rup_i3_q       : NATURAL := 890;
    CONSTANT rup_i4_q       : NATURAL := 890;
    CONSTANT rup_i5_q       : NATURAL := 890;
    CONSTANT rup_i6_q       : NATURAL := 890;
    CONSTANT tpll_i6_q      : NATURAL := 651;
    CONSTANT tphh_i3_q      : NATURAL := 673;
    CONSTANT tphh_i6_q      : NATURAL := 684;
    CONSTANT tphh_i0_q      : NATURAL := 717;
    CONSTANT tphh_i4_q      : NATURAL := 758;
    CONSTANT tphh_i1_q      : NATURAL := 818;
    CONSTANT tpll_i2_q      : NATURAL := 834;
    CONSTANT tphh_i5_q      : NATURAL := 839;
    CONSTANT tpll_i5_q      : NATURAL := 865;
    CONSTANT tpll_i1_q      : NATURAL := 890;
    CONSTANT tphh_i2_q      : NATURAL := 894;
    CONSTANT tpll_i4_q      : NATURAL := 896;
    CONSTANT tpll_i3_q      : NATURAL := 898;
    CONSTANT tpll_i0_q      : NATURAL := 946;
    CONSTANT transistors    : NATURAL := 18
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    i2      : in  BIT;
    i3      : in  BIT;
    i4      : in  BIT;
    i5      : in  BIT;
    i6      : in  BIT;
```

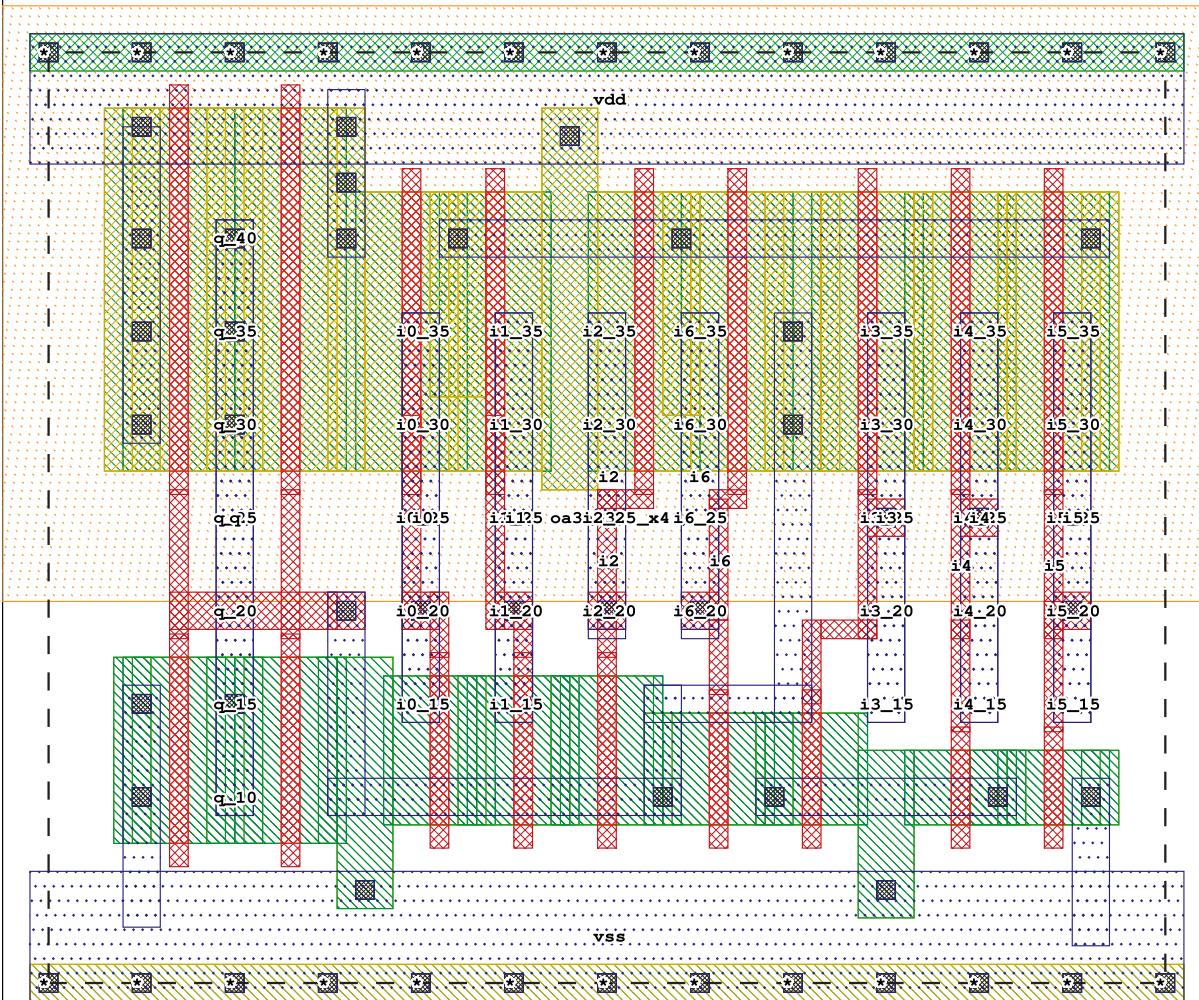
```

q      : out BIT;
vdd    : in  BIT;
vss    : in  BIT
);
END oa3ao322_x4;

ARCHITECTURE behaviour_data_flow OF oa3ao322_x4 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on oa3ao322_x4"
  SEVERITY WARNING;
  q <= (((i0 and i1) and i2) or (i6 and ((i3 or i4) or i5))) after 1500 ps;
END;

```

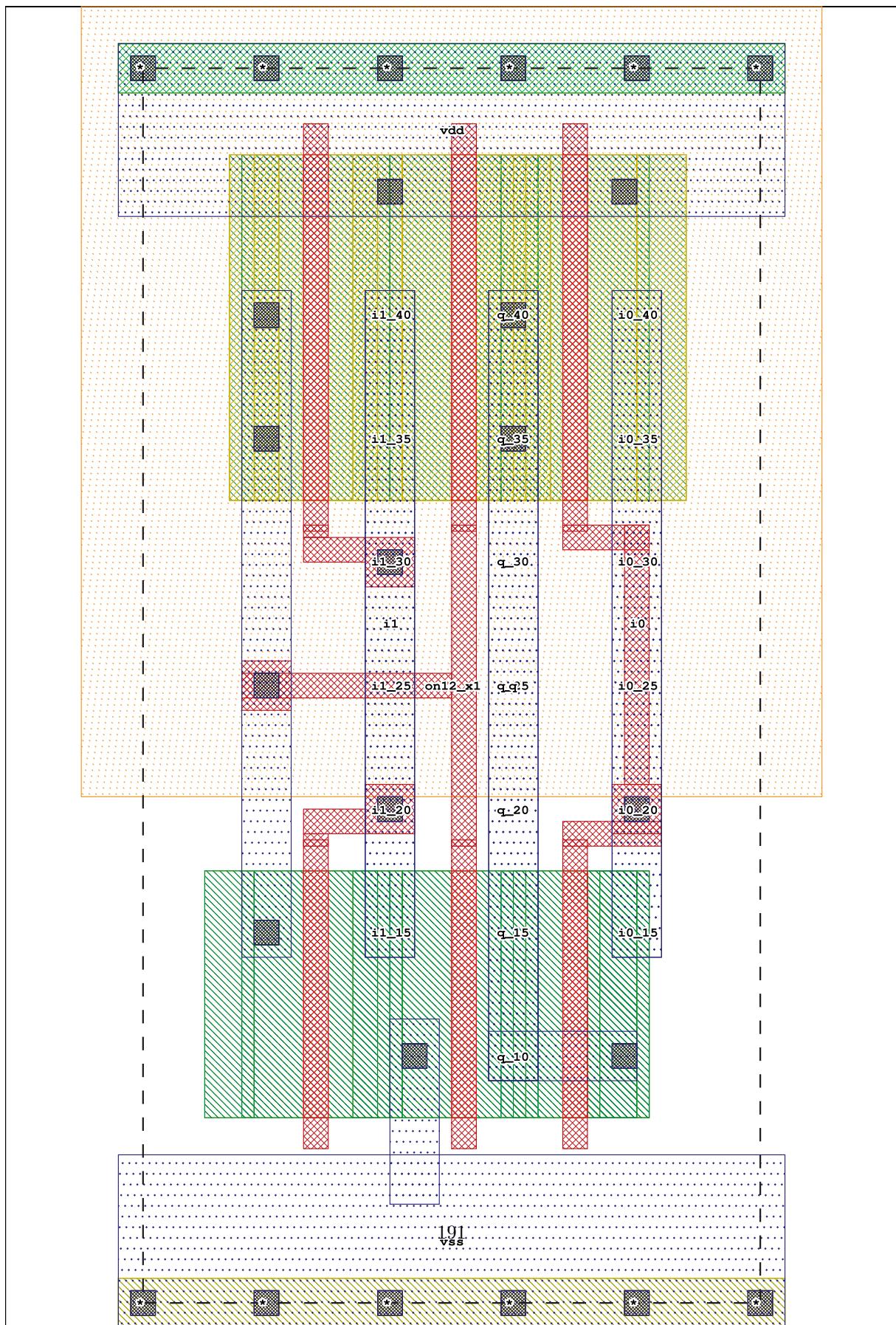


#### 4.77 on12\_x1

```
ENTITY on12_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1250;
    CONSTANT cin_i0         : NATURAL := 11;
    CONSTANT cin_i1         : NATURAL := 9;
    CONSTANT rdown_i0_q     : NATURAL := 2850;
    CONSTANT rdown_i1_q     : NATURAL := 2850;
    CONSTANT rup_i0_q       : NATURAL := 3720;
    CONSTANT rup_i1_q       : NATURAL := 3720;
    CONSTANT tphl_i0_q      : NATURAL := 111;
    CONSTANT tplh_i0_q      : NATURAL := 234;
    CONSTANT tp1l_i1_q       : NATURAL := 291;
    CONSTANT tp1h_i1_q       : NATURAL := 314;
    CONSTANT transistors    : NATURAL := 6
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END on12_x1;

ARCHITECTURE behaviour_data_flow OF on12_x1 IS

BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on on12_x1"
  SEVERITY WARNING;
  q <= (not (i0) or i1) after 900 ps;
END;
```

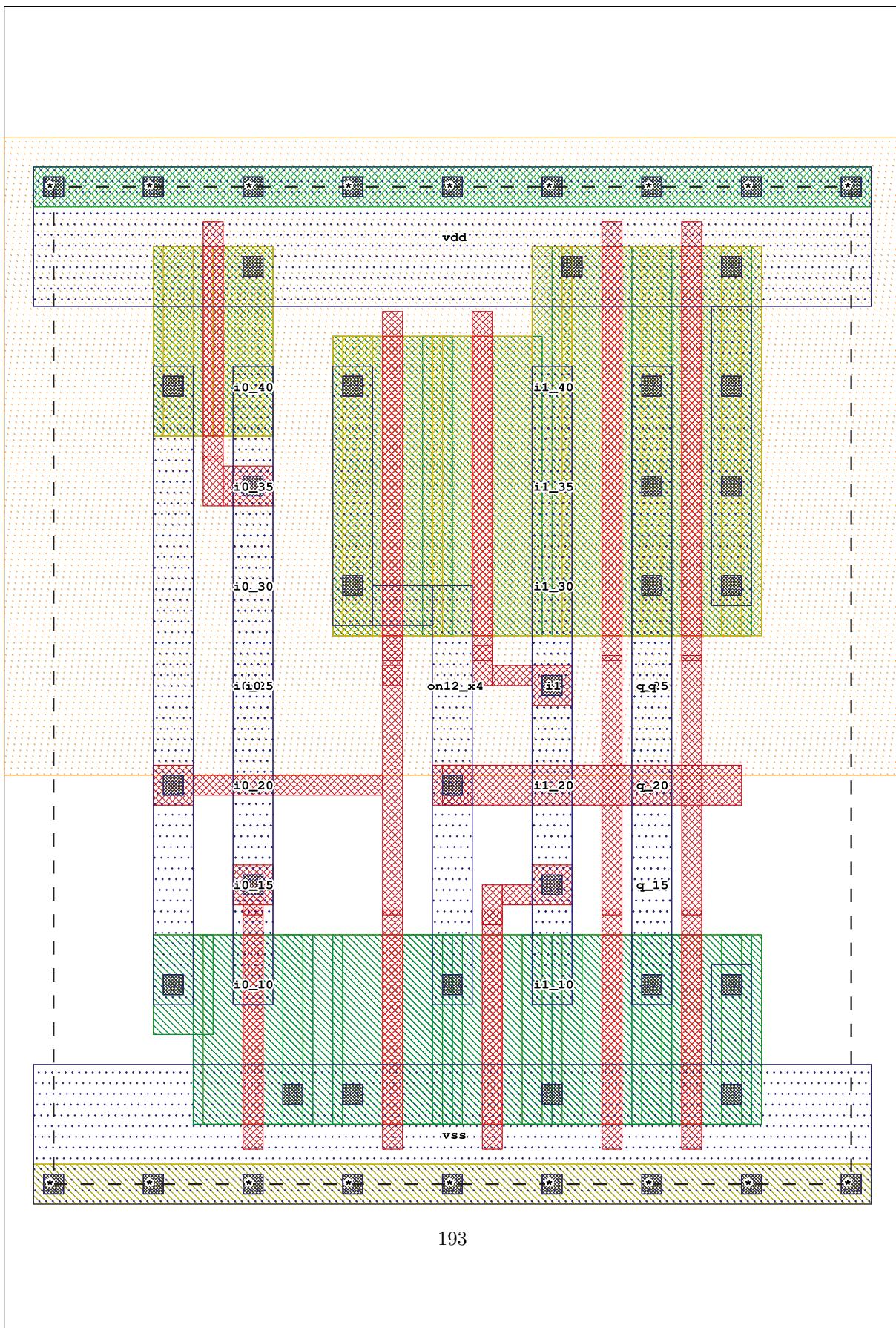


#### 4.78 on12\_x4

```
ENTITY on12_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 2000;
    CONSTANT cin_i0         : NATURAL := 9;
    CONSTANT cin_i1         : NATURAL := 10;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT tpll_i1_q      : NATURAL := 394;
    CONSTANT tphl_i0_q      : NATURAL := 474;
    CONSTANT tphh_i1_q      : NATURAL := 491;
    CONSTANT tplh_i0_q      : NATURAL := 499;
    CONSTANT transistors    : NATURAL := 10
);
PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
);
END on12_x4;

ARCHITECTURE behaviour_data_flow OF on12_x4 IS

BEGIN
    ASSERT ((vdd and not (vss)) = '1')
        REPORT "power supply is missing on on12_x4"
        SEVERITY WARNING;
    q <= (not (i0) or i1) after 1100 ps;
END;
```

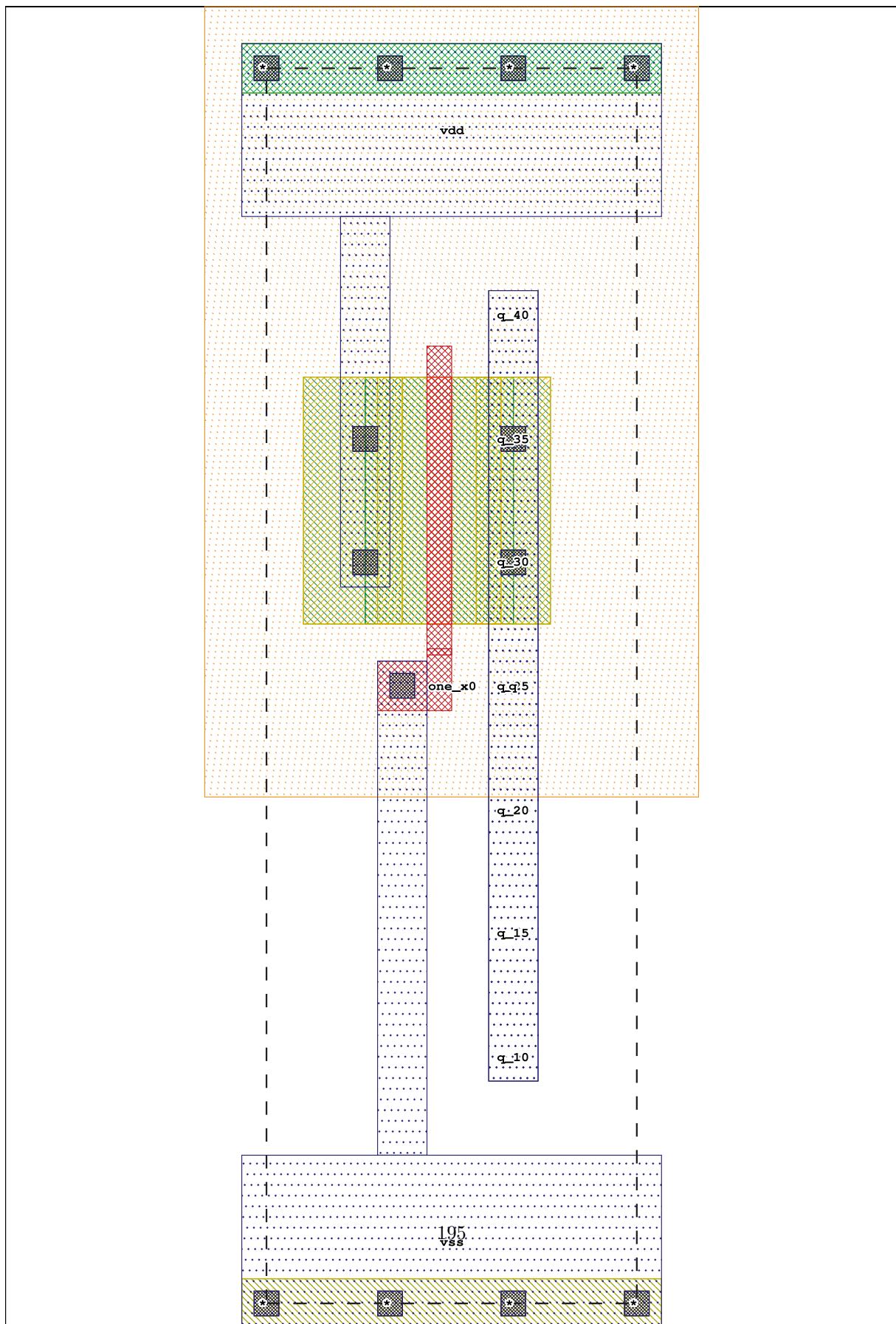


#### 4.79 one\_x0

```
ENTITY one_x0 IS
  GENERIC (
    CONSTANT area          : NATURAL := 750;
    CONSTANT transistors   : NATURAL := 1
  );
  PORT (
    q      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END one_x0;

ARCHITECTURE behaviour_data_flow OF one_x0 IS

BEGIN
  ASSERT (vdd and not (vss))
  REPORT "power supply is missing on one_x0"
  SEVERITY WARNING;
  q <= '1';
END;
```

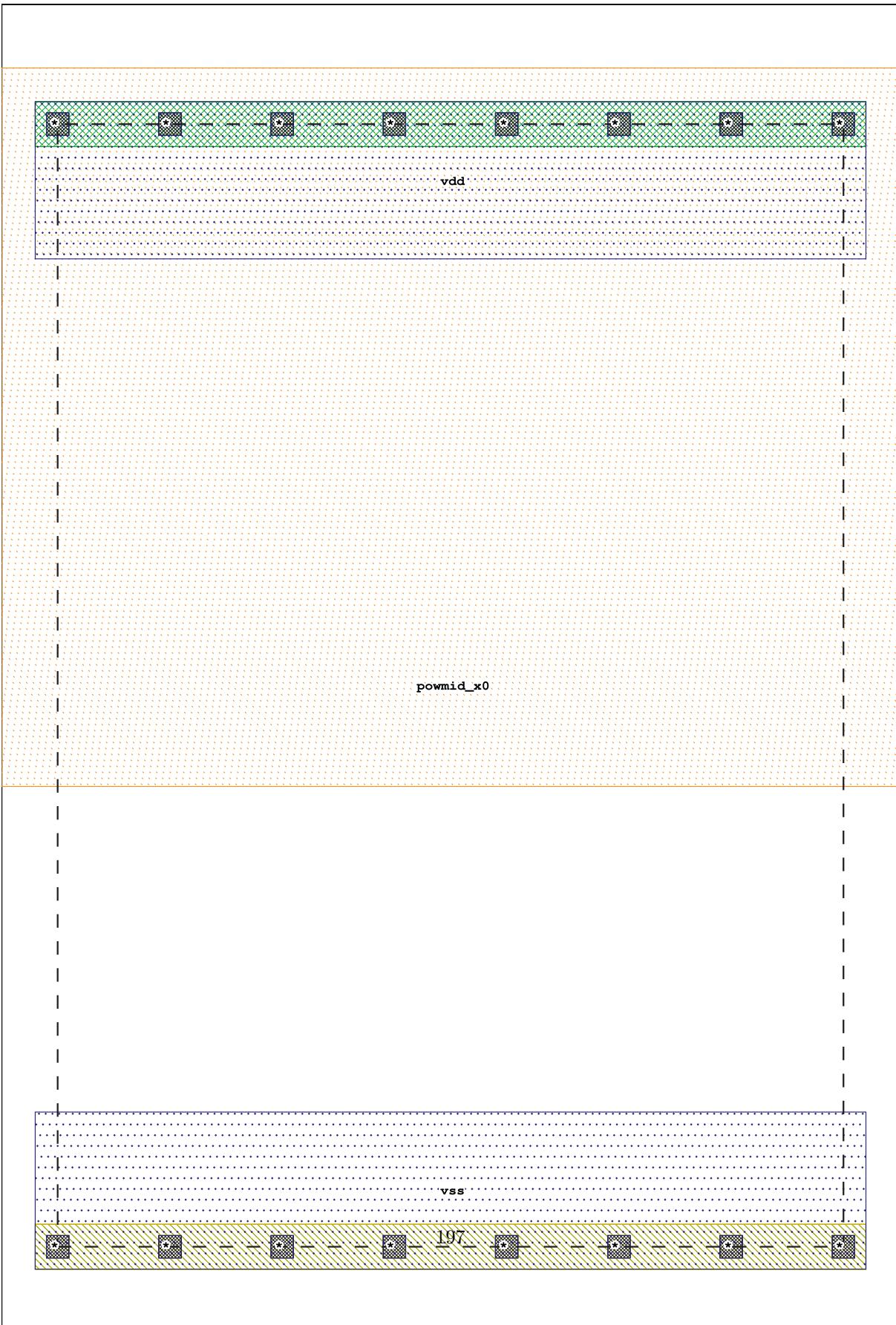


#### 4.80 powmid\_x0

```
ENTITY powmid_x0 IS
  GENERIC (
    CONSTANT area          : NATURAL := 1750;
    CONSTANT transistors   : NATURAL := 0
  );
  PORT (
    vdd      : in BIT;
    vss      : in BIT
  );
END powmid_x0;

ARCHITECTURE behaviour_data_flow OF powmid_x0 IS

BEGIN
  ASSERT (vdd and not (vss))
    REPORT "power supply is missing on powmid_x0"
    SEVERITY WARNING;
END;
```

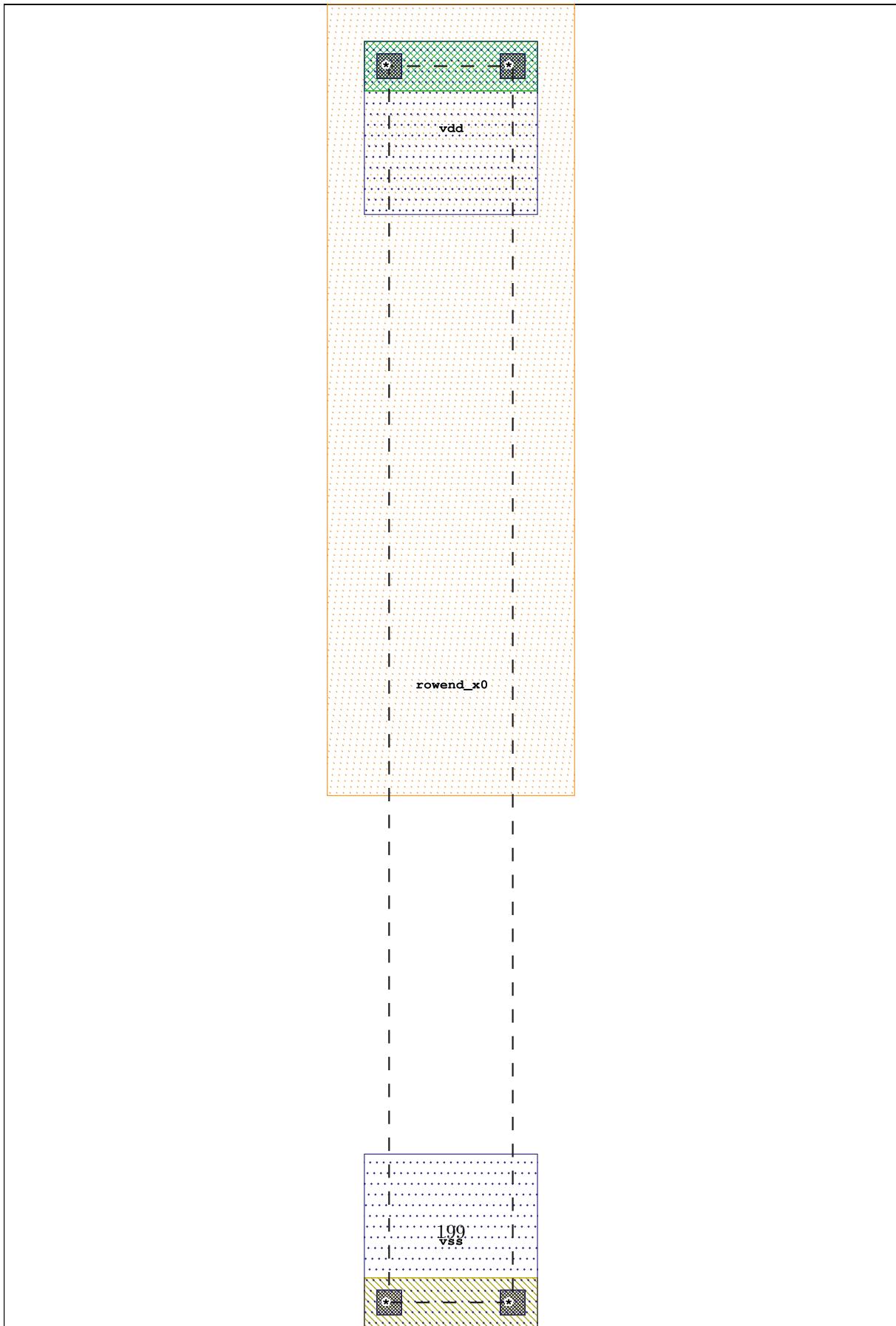


#### 4.81 rowend\_x0

```
ENTITY rowend_x0 IS
  GENERIC (
    CONSTANT area          : NATURAL := 250;
    CONSTANT transistors   : NATURAL := 0
  );
  PORT (
    vdd      : in BIT;
    vss      : in BIT
  );
END rowend_x0;

ARCHITECTURE behaviour_data_flow OF rowend_x0 IS

BEGIN
  ASSERT (vdd and not (vss))
    REPORT "power supply is missing on rowend_x0"
    SEVERITY WARNING;
END;
```



#### 4.82 sff1\_x4

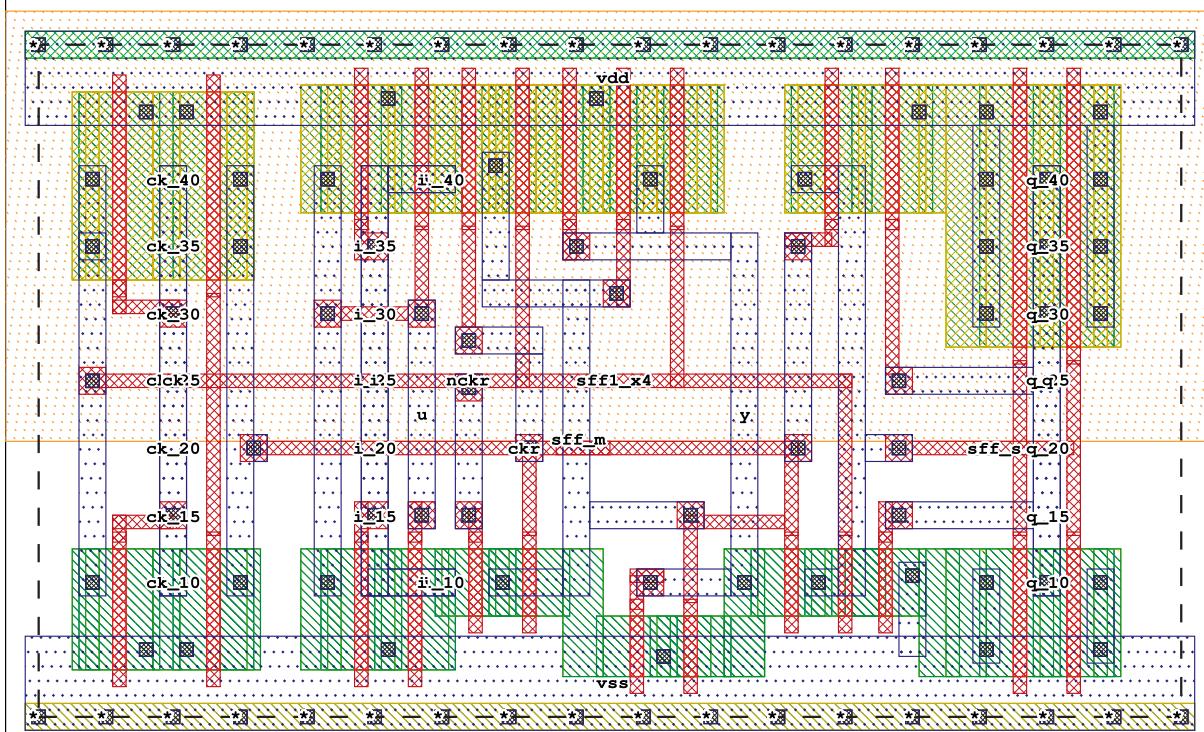
```
ENTITY sff1_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 4500;
    CONSTANT cin_ck        : NATURAL := 8;
    CONSTANT cin_i         : NATURAL := 8;
    CONSTANT rdown_ck_q   : NATURAL := 800;
    CONSTANT rup_ck_q     : NATURAL := 890;
    CONSTANT taf_ck_q     : NATURAL := 500;
    CONSTANT tar_ck_q     : NATURAL := 500;
    CONSTANT thf_i_ck     : NATURAL := 0;
    CONSTANT thr_i_ck     : NATURAL := 0;
    CONSTANT tsf_i_ck     : NATURAL := 585;
    CONSTANT tsr_i_ck     : NATURAL := 476;
    CONSTANT transistors  : NATURAL := 26
  );
  PORT (
    ck      : in  BIT;
    i       : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
  );
END sff1_x4;

ARCHITECTURE VBE OF sff1_x4 IS
  SIGNAL sff_m    : REG_BIT REGISTER;

BEGIN
  ASSERT (vdd and not (vss))
  REPORT "power supply is missing on sff1_x4"
  SEVERITY WARNING;

  label0 : BLOCK ((ck and not (ck'STABLE)) = '1')
  BEGIN
    sff_m <= GUARDED i;
  END BLOCK label0;

  q <= sff_m after 1700 ps;
END;
```



#### 4.83 sff1r\_x4

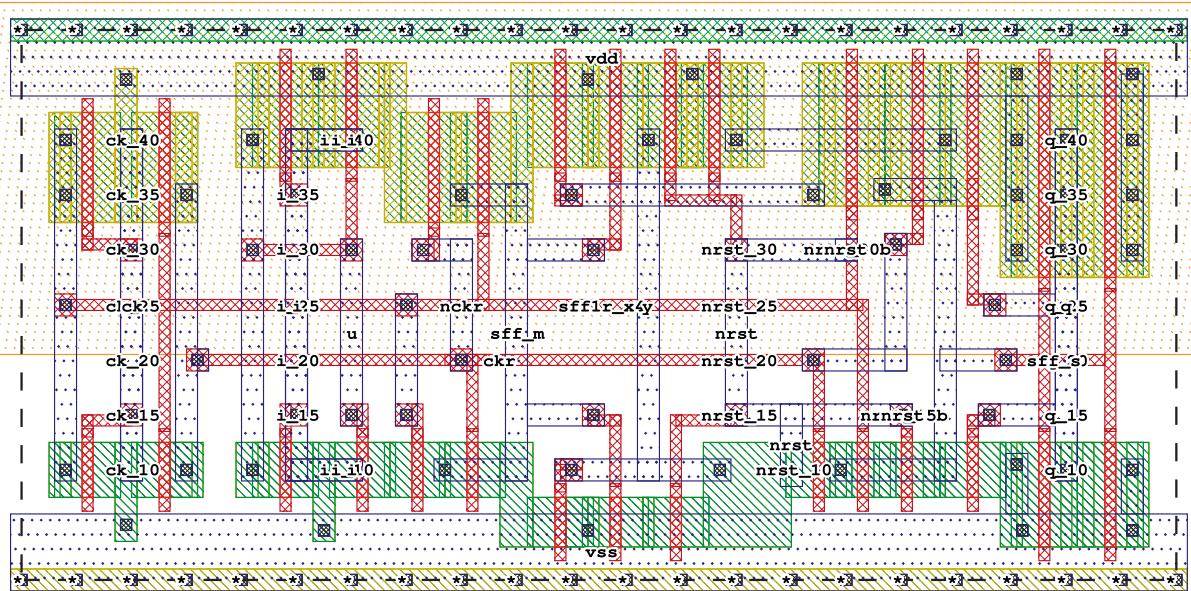
```

ENTITY sff1r_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 4500;
    CONSTANT cin_ck         : NATURAL := 8;
    CONSTANT cin_i          : NATURAL := 8;
    CONSTANT cin_nrst       : NATURAL := 16;
    CONSTANT rdown_ck_q     : NATURAL := 800;
    CONSTANT rup_ck_q       : NATURAL := 890;
    CONSTANT taf_ck_q       : NATURAL := 500;
    CONSTANT tar_ck_q       : NATURAL := 500;
    CONSTANT taf_nrst_q     : NATURAL := 500;
    CONSTANT tar_nrst_q     : NATURAL := 500;
    CONSTANT thf_i_ck       : NATURAL := 0;
    CONSTANT thr_i_ck       : NATURAL := 0;
    CONSTANT tsf_i_ck       : NATURAL := 585;
    CONSTANT tsr_i_ck       : NATURAL := 476;
    CONSTANT transistors    : NATURAL := 30
);
PORT (
    ck      : in  BIT;
    i       : in  BIT;
    nrst   : in  BIT;
    q       : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END sff1r_x4;

ARCHITECTURE VBE OF sff1r_x4 IS
    SIGNAL sff_m    : REG_BIT REGISTER;

BEGIN
    ASSERT (vdd and not (vss))
        REPORT "power supply is missing on sff1r_x4"
        SEVERITY WARNING;
    label0 : BLOCK (nrst = '0')
    BEGIN
        sff_m <= GUARDED '0';
    END BLOCK label0;
    label1 : BLOCK ( (nrst = '1') AND (ck AND NOT(ck'STABLE)) = '1' )
    BEGIN
        sff_m <= GUARDED i;
    END BLOCK label1;
    q <= sff_m after 1700 ps;
END;

```



#### 4.84 sff2\_x4

```

ENTITY sff2_x4 IS
GENERIC (
    CONSTANT area          : NATURAL := 6000;
    CONSTANT cin_ck         : NATURAL := 8;
    CONSTANT cin_cmd        : NATURAL := 16;
    CONSTANT cin_i0          : NATURAL := 8;
    CONSTANT cin_i1          : NATURAL := 7;
    CONSTANT rdown_ck_q     : NATURAL := 800;
    CONSTANT rup_ck_q       : NATURAL := 890;
    CONSTANT taf_ck_q       : NATURAL := 500;
    CONSTANT tar_ck_q       : NATURAL := 500;
    CONSTANT thf_cmd_ck    : NATURAL := 0;
    CONSTANT thf_i0_ck      : NATURAL := 0;
    CONSTANT thf_i1_ck      : NATURAL := 0;
    CONSTANT thr_cmd_ck    : NATURAL := 0;
    CONSTANT thr_i0_ck      : NATURAL := 0;
    CONSTANT thr_i1_ck      : NATURAL := 0;
    CONSTANT tsf_cmd_ck    : NATURAL := 833;
    CONSTANT tsf_i0_ck      : NATURAL := 764;
    CONSTANT tsf_i1_ck      : NATURAL := 764;
    CONSTANT tsr_cmd_ck    : NATURAL := 770;
    CONSTANT tsr_i0_ck      : NATURAL := 666;
    CONSTANT tsr_i1_ck      : NATURAL := 666;
    CONSTANT transistors   : NATURAL := 34
);
PORT (
    ck      : in  BIT;
    cmd    : in  BIT;
    i0     : in  BIT;
    i1     : in  BIT;
    q      : out BIT;
    vdd    : in  BIT;
    vss    : in  BIT
);
END sff2_x4;

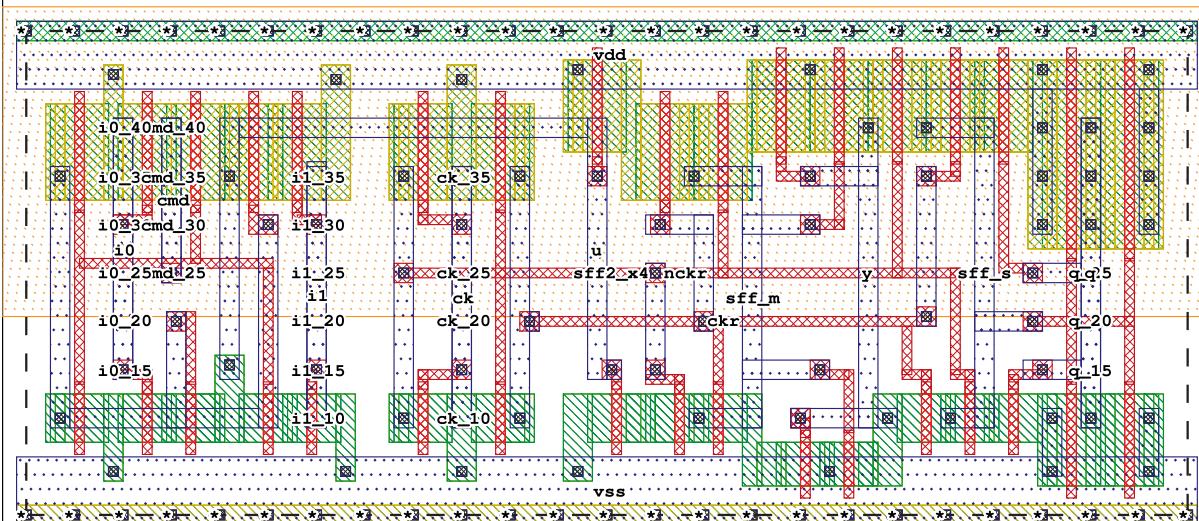
ARCHITECTURE VBE OF sff2_x4 IS
    SIGNAL sff_m    : REG_BIT REGISTER;

BEGIN
    ASSERT (vdd and not (vss))
    REPORT "power supply is missing on sff2_x4"
    SEVERITY WARNING;

    label0 : BLOCK ((ck and not (ck'STABLE)) = '1')
    BEGIN
        sff_m <= GUARDED ((i1 and cmd) or (i0 and not (cmd)));
    END BLOCK label0 ;

```

```
q <= sff_m after 2000 ps;  
END;
```

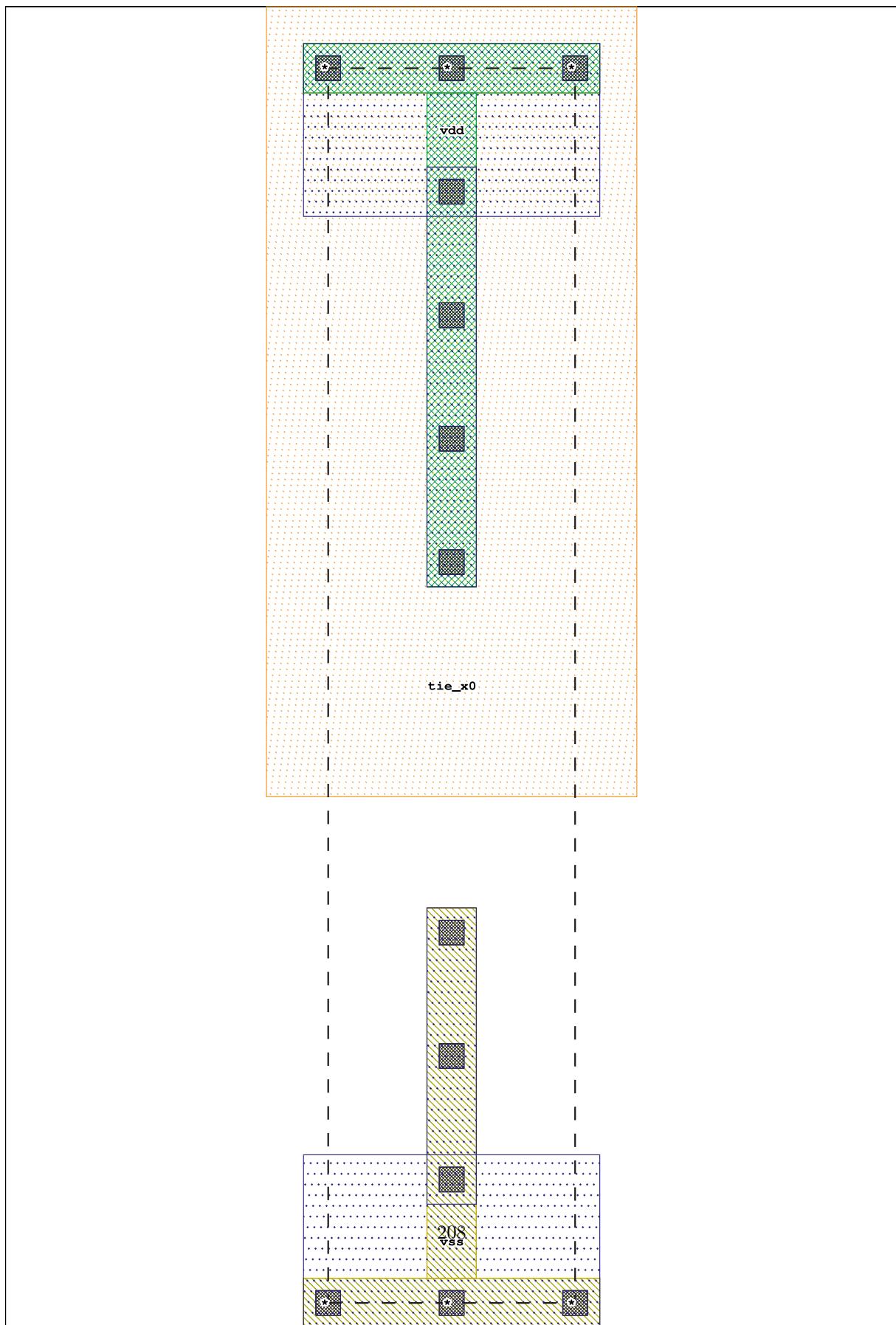


#### 4.85 tie\_x0

```
ENTITY tie_x0 IS
  GENERIC (
    CONSTANT area          : NATURAL := 500;
    CONSTANT transistors   : NATURAL := 0
  );
  PORT (
    vdd      : in  BIT;
    vss      : in  BIT
  );
END tie_x0;

ARCHITECTURE behaviour_data_flow OF tie_x0 IS

BEGIN
  ASSERT (vdd and not (vss))
    REPORT "power supply is missing on tie_x0"
    SEVERITY WARNING;
END;
```



#### 4.86 ts\_x4

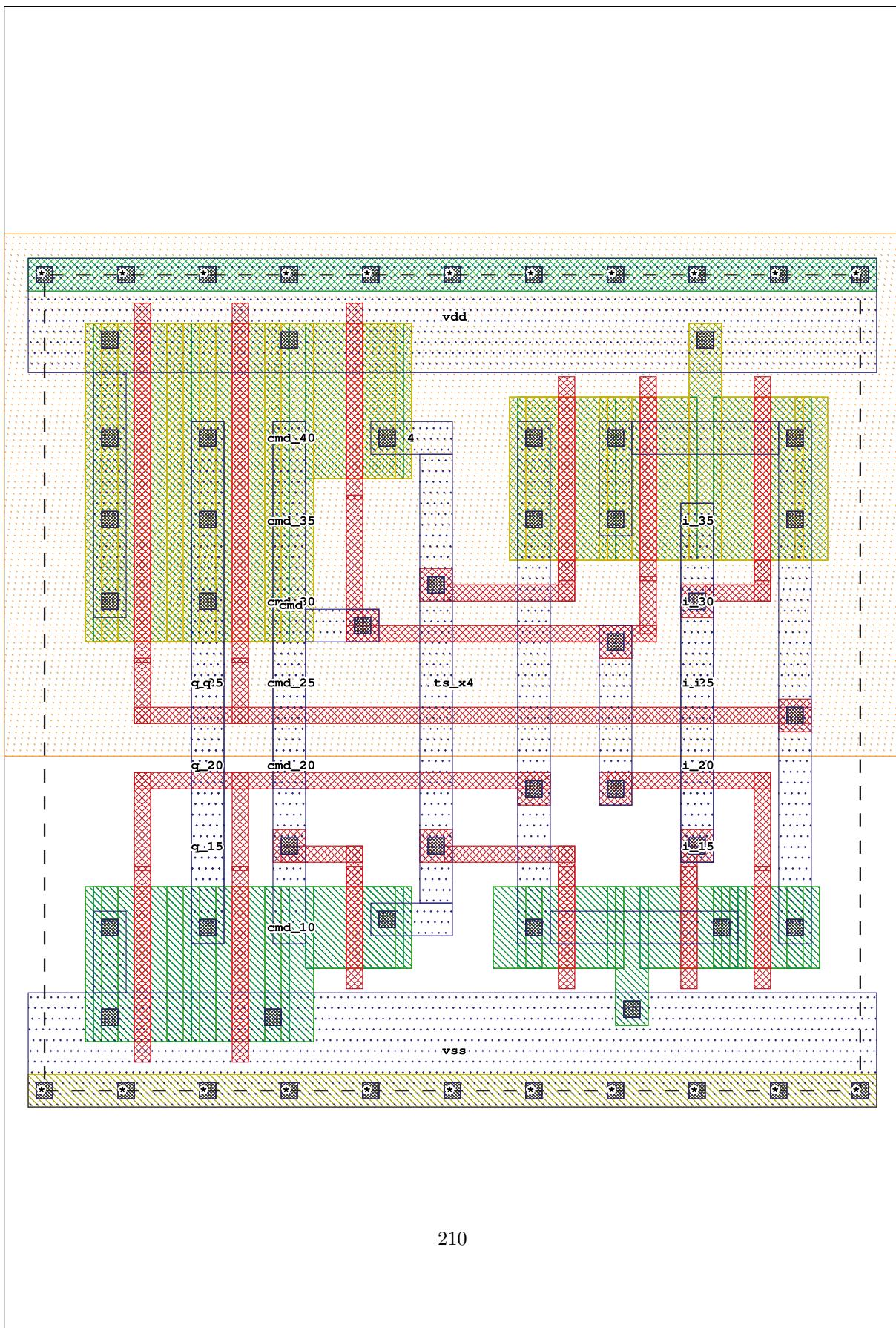
```
ENTITY ts_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2500;
    CONSTANT cin_cmd       : NATURAL := 19;
    CONSTANT cin_i         : NATURAL := 8;
    CONSTANT rdown_cmd_q  : NATURAL := 810;
    CONSTANT rdown_i_q    : NATURAL := 810;
    CONSTANT rup_cmd_q   : NATURAL := 890;
    CONSTANT rup_i_q     : NATURAL := 890;
    CONSTANT tphl_cmd_q  : NATURAL := 409;
    CONSTANT tpll_i_q    : NATURAL := 444;
    CONSTANT tphh_i_q    : NATURAL := 475;
    CONSTANT tphh_cmd_q  : NATURAL := 492;
    CONSTANT transistors : NATURAL := 12
  );
  PORT (
    cmd      : in  BIT;
    i        : in  BIT;
    q        : out MUX_BIT BUS;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END ts_x4;
```

```
ARCHITECTURE behaviour_data_flow OF ts_x4 IS
```

```
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on ts_x4"
  SEVERITY WARNING;

  label0 : BLOCK (cmd = '1')
  BEGIN
    q <= GUARDED i after 1100 ps;
  END BLOCK label0;

END;
```



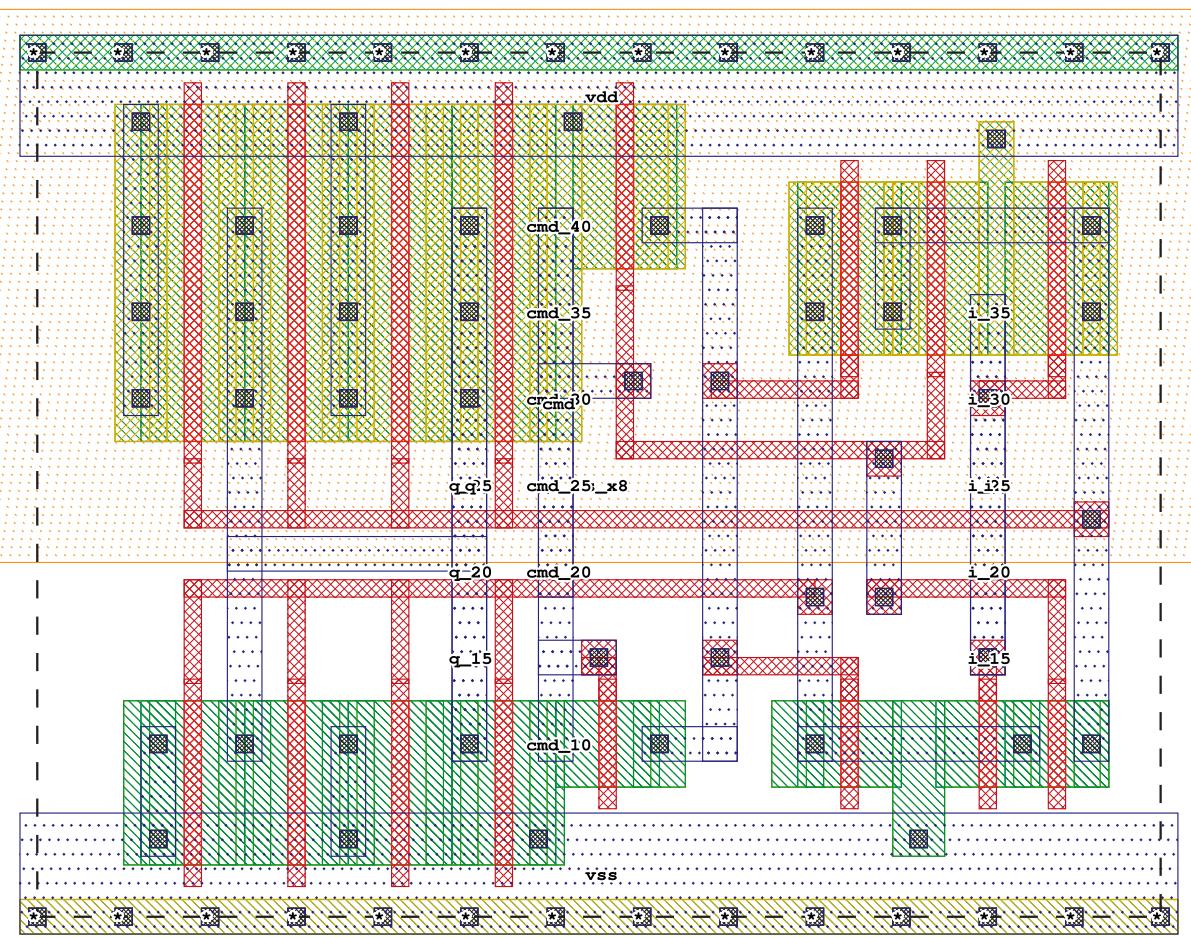
#### 4.87 ts\_x8

```
ENTITY ts_x8 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3250;
    CONSTANT cin_cmd       : NATURAL := 19;
    CONSTANT cin_i         : NATURAL := 8;
    CONSTANT rdown_cmd_q  : NATURAL := 400;
    CONSTANT rdown_i_q    : NATURAL := 400;
    CONSTANT rup_cmd_q   : NATURAL := 450;
    CONSTANT rup_i_q     : NATURAL := 450;
    CONSTANT tphl_cmd_q  : NATURAL := 466;
    CONSTANT tpll_i_q    : NATURAL := 569;
    CONSTANT tphh_i_q    : NATURAL := 613;
    CONSTANT tphh_cmd_q  : NATURAL := 626;
    CONSTANT transistors : NATURAL := 16
  );
  PORT (
    cmd      : in  BIT;
    i        : in  BIT;
    q        : out MUX_BIT BUS;
    vdd      : in  BIT;
    vss      : in  BIT
  );
END ts_x8;
```

```
ARCHITECTURE behaviour_data_flow OF ts_x8 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on ts_x8"
  SEVERITY WARNING;

  label0 : BLOCK (cmd = '1')
  BEGIN
    q <= GUARDED i after 1200 ps;
  END BLOCK label0;

END;
```

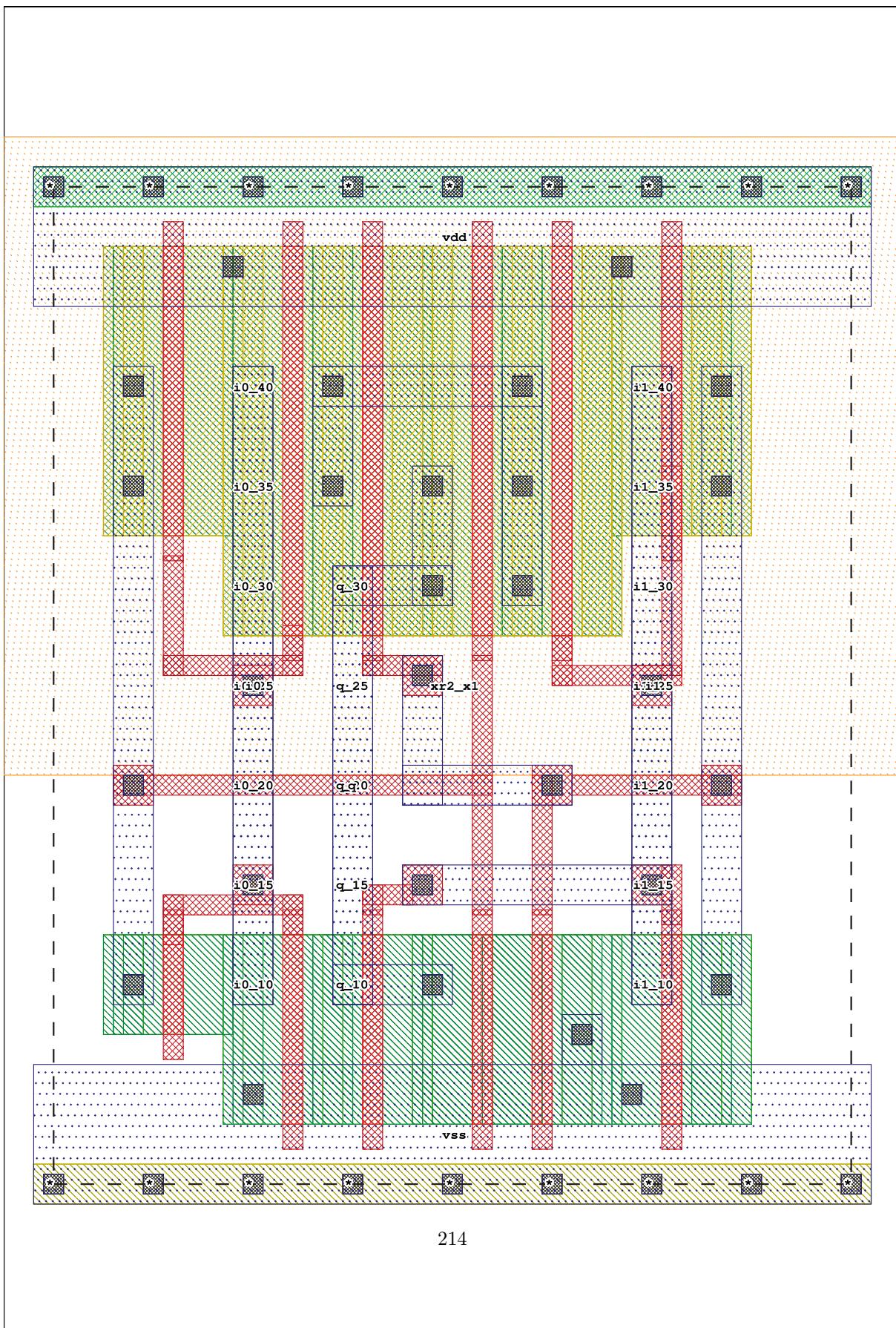


#### 4.88 xr2\_x1

```
ENTITY xr2_x1 IS
  GENERIC (
    CONSTANT area          : NATURAL := 2250;
    CONSTANT cin_i0         : NATURAL := 21;
    CONSTANT cin_i1         : NATURAL := 22;
    CONSTANT rdown_i0_q     : NATURAL := 2850;
    CONSTANT rdown_i1_q     : NATURAL := 2850;
    CONSTANT rup_i0_q       : NATURAL := 3210;
    CONSTANT rup_i1_q       : NATURAL := 3210;
    CONSTANT tplh_i1_q      : NATURAL := 261;
    CONSTANT tphl_i0_q      : NATURAL := 292;
    CONSTANT tphl_i0_q      : NATURAL := 293;
    CONSTANT tphh_i0_q      : NATURAL := 366;
    CONSTANT tphl_i1_q      : NATURAL := 377;
    CONSTANT tpll_i1_q      : NATURAL := 388;
    CONSTANT tpll_i0_q      : NATURAL := 389;
    CONSTANT tphh_i1_q      : NATURAL := 405;
    CONSTANT transistors    : NATURAL := 12
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END xr2_x1;

ARCHITECTURE behaviour_data_flow OF xr2_x1 IS

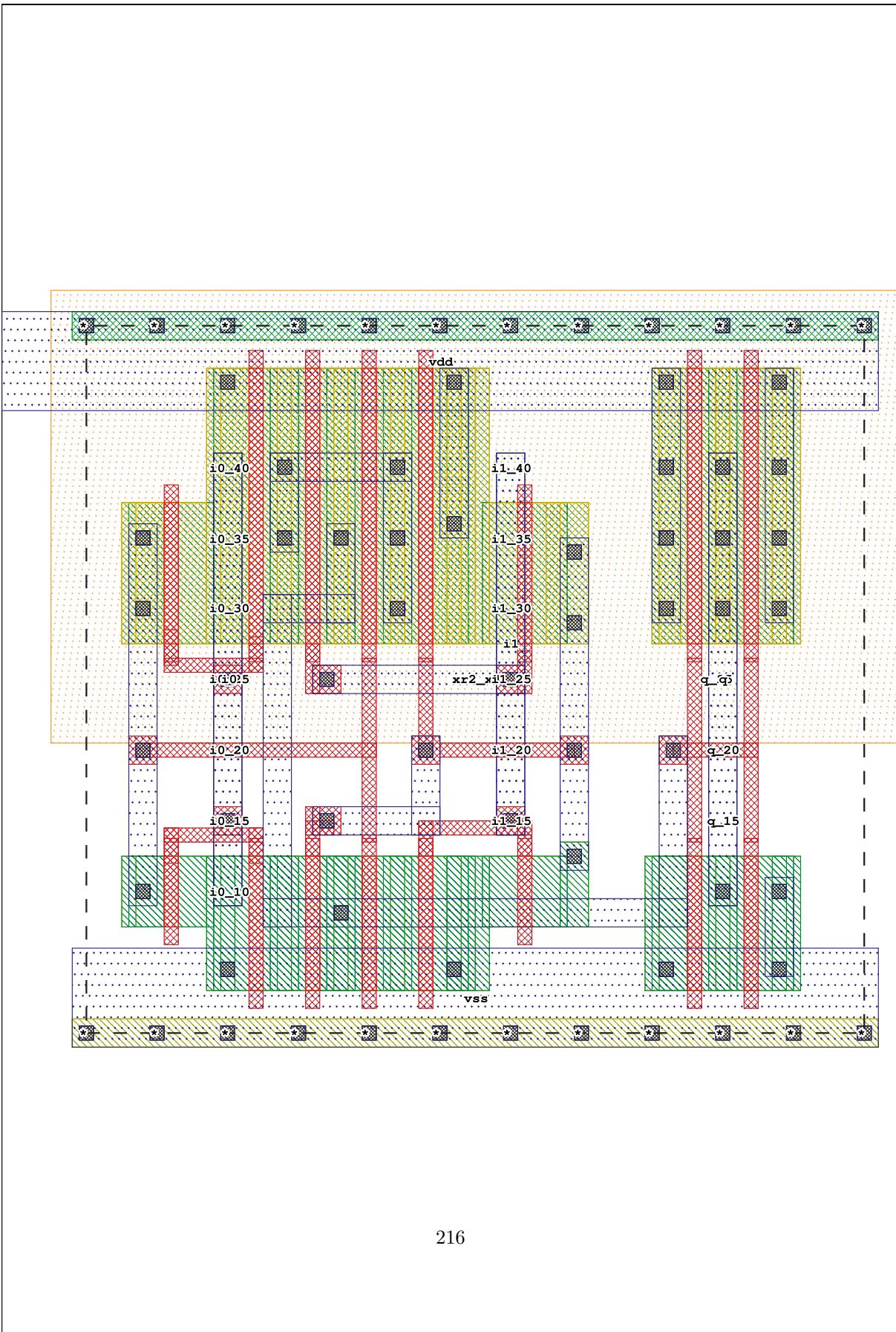
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on xr2_x1"
  SEVERITY WARNING;
  q <= (i0 xor i1) after 1000 ps;
END;
```



#### 4.89 xr2\_x4

```
ENTITY xr2_x4 IS
  GENERIC (
    CONSTANT area          : NATURAL := 3000;
    CONSTANT cin_i0         : NATURAL := 20;
    CONSTANT cin_i1         : NATURAL := 21;
    CONSTANT rdown_i0_q     : NATURAL := 810;
    CONSTANT rdown_i1_q     : NATURAL := 810;
    CONSTANT rup_i0_q       : NATURAL := 890;
    CONSTANT rup_i1_q       : NATURAL := 890;
    CONSTANT tphh_i1_q      : NATURAL := 357;
    CONSTANT tphh_i0_q      : NATURAL := 476;
    CONSTANT tp1l_i0_q       : NATURAL := 480;
    CONSTANT tp1l_i0_q       : NATURAL := 521;
    CONSTANT tp1l_i1_q       : NATURAL := 539;
    CONSTANT tp1l_i1_q       : NATURAL := 541;
    CONSTANT tp1h_i0_q       : NATURAL := 560;
    CONSTANT tp1h_i1_q       : NATURAL := 657;
    CONSTANT transistors    : NATURAL := 16
  );
  PORT (
    i0      : in  BIT;
    i1      : in  BIT;
    q       : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END xr2_x4;
```

```
ARCHITECTURE behaviour_data_flow OF xr2_x4 IS
BEGIN
  ASSERT ((vdd and not (vss)) = '1')
  REPORT "power supply is missing on xr2_x4"
  SEVERITY WARNING;
  q <= (i0 xor i1) after 1300 ps;
END;
```

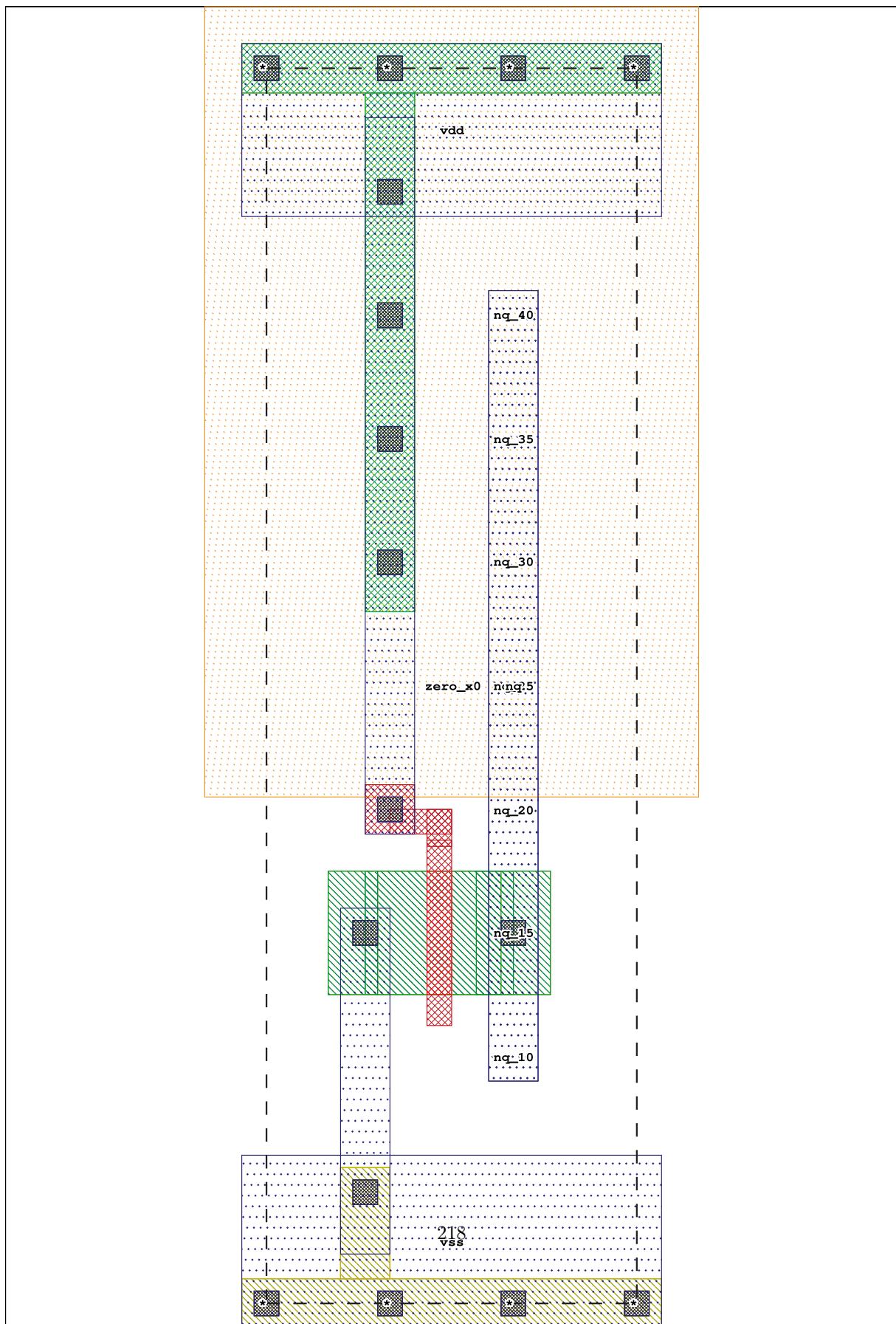


#### 4.90 zero\_x0

```
ENTITY zero_x0 IS
  GENERIC (
    CONSTANT area          : NATURAL := 750;
    CONSTANT transistors   : NATURAL := 1
  );
  PORT (
    nq      : out BIT;
    vdd     : in  BIT;
    vss     : in  BIT
  );
END zero_x0;

ARCHITECTURE behaviour_data_flow OF zero_x0 IS

BEGIN
  ASSERT (vdd and not (vss))
  REPORT "power supply is missing on zero_x0"
  SEVERITY WARNING;
  nq <= '0';
END;
```



## 5 RDS File for template $\lambda = 1.0$

```
# -----
# COPYRIGHT IS UNCERTAIN YET.
#
# This file is derived from the Alliance cmos.rds, adapted by
# Graham Petley for 0.13um and finally to MOSIS scn6m_deep by
# Naohiko Shimizu. It is a 2lambdas rules.
# This file is a template for MOSIS DEEP where lambda is set 1.0.
# You can scale the lambda and other RDS parameters as wish.
#
# To be used with the nsxlib library.
#
#
##-----
# PHYSICAL_GRID :
##-----
```

DEFINE PHYSICAL\_GRID 0.005

```
##-----
# LAMBDA :
##-----
```

DEFINE LAMBDA 1.0

```
##-----
# TABLE MBK_TO_RDS_SEGMENT :
#
# MBK      RDS layer 1          RDS layer 2
# name     name TRANS DLR DWR OFFSET   name TRANS DLR DWR OFFSET ...
```

---

TABLE MBK\_TO\_RDS\_SEGMENT

	RDS_PWELL	VW	0.00	0.0	0.0	ALL
PWELL	RDS_PWELL	VW	0.00	0.0	0.0	ALL
NWELL	RDS_NWELL	VW	0.00	0.0	0.0	ALL
NDIF	RDS_NDIF	VW	0.00	0.0	0.0	ALL \
	RDS_ACTIV	VW	0.00	0.0	0.0	DRC \
	RDS_NIMP	VW	0.00	0.00	0.0	DRC
PDIF	RDS_PDIF	VW	0.00	0.0	0.0	ALL \
	RDS_ACTIV	VW	0.00	0.0	0.0	DRC \
	RDS_PIMP	VW	0.00	0.00	0.0	DRC
NTIE	RDS_NTIE	VW	0.00	0.00	0.0	EXT \
	RDS_NTIE	VW	0.00	0.00	0.0	DRC \
	RDS_ACTIV	VW	0.00	0.00	0.0	DRC \

	RDS_NIMP	VW	0.00	0.00	0.0	DRC
PTIE	RDS_PTIE	VW	0.00	0.00	0.0	EXT \
	RDS_PTIE	VW	0.00	0.00	0.0	DRC \
	RDS_ACTIV	VW	0.00	0.00	0.0	DRC \
	RDS_PIMP	VW	0.00	0.00	0.0	DRC
# The GATE layer is the poly which makes the						
# transistor. It is used to measure the ENDCAP						
# value.						
NTRANS	RDS_POLY	VW	2.50	0.00	0.0	ALL \
	RDS_GATE	VW	0.00	0.00	0.0	DRC \
	RDS_NDIF	LCW	0.00	4.00	0.0	EXT \
	RDS_NDIF	RCW	0.00	4.00	0.0	EXT \
	RDS_NDIF	VW	0.00	8.00	0.0	DRC \
	RDS_ACTIV	VW	0.00	8.00	0.0	ALL \
	RDS_NIMP	VW	0.00	10.00	0.0	DRC \
	RDS_NIMP	VW	0.00	10.00	0.0	DRC
PTRANS	RDS_POLY	VW	2.50	0.00	0.0	ALL \
	RDS_GATE	VW	0.00	0.00	0.0	DRC \
	RDS_PDIF	LCW	0.00	4.00	0.0	EXT \
	RDS_PDIF	RCW	0.00	4.00	0.0	EXT \
	RDS_PDIF	VW	0.00	8.00	0.0	DRC \
	RDS_ACTIV	VW	0.00	8.00	0.0	ALL \
	RDS_PIMP	VW	0.00	10.00	0.0	ALL \
	RDS_PIMP	VW	0.00	10.00	0.0	DRC
POLY	RDS_POLY	VW	0.00	0.00	0.0	ALL
ALU1	RDS_ALU1	VW	0.00	0.00	0.0	ALL
# Layers VALU2–VALU6 and TALU2–TALU6 are used to						
# check for the end overlap of the metal to via.						
ALU2	RDS_ALU2	VW	0.000	0.00	0.0	ALL
ALU3	RDS_ALU3	VW	0.000	0.00	0.0	ALL
ALU4	RDS_ALU4	VW	0.000	0.00	0.0	ALL
ALU5	RDS_ALU5	VW	0.000	0.00	0.0	ALL
ALU6	RDS_ALU6	VW	0.000	0.00	0.0	ALL
CALU1	RDS_ALU1	VW	0.00	0.0	0.0	ALL
CALU2	RDS_ALU2	VW	0.000	0.0	0.0	ALL
CALU3	RDS_ALU3	VW	0.000	0.0	0.0	ALL
CALU4	RDS_ALU4	VW	0.000	0.0	0.0	ALL
CALU5	RDS_ALU5	VW	0.000	0.0	0.0	ALL
CALU6	RDS_ALU6	VW	0.000	0.0	0.0	ALL

END

---

```
##_
# TABLE MBK_TO_RDS_CONNECTOR :
#
```

```

# MBK      RDS layer
# name      name      DER DWR
##
```

---

TABLE MBK\_TO\_RDS\_CONNECTOR

POLY	RDS.POLY	0.00	0.00
ALU1	RDS_ALU1	0.00	0.00
ALU2	RDS_ALU2	0.00	0.00
ALU3	RDS_ALU3	0.00	0.00
ALU4	RDS_ALU4	0.00	0.00
ALU5	RDS_ALU5	0.00	0.00
ALU6	RDS_ALU6	0.00	0.00

END

```

##
```

---

```

# TABLE MBK_TO_RDS_REFERENCE :
#
# MBK ref      RDS layer
# name          name      width
##
```

---

TABLE MBK\_TO\_RDS\_REFERENCE

REF_REF	RDS_REF	2.00				
REF_CON	RDS_VALU1	2.00	RDS_TVIA1	2.00	RDS_TALU2	2.00

END

```

##
```

---

```

# TABLE MBK_TO_RDS_VIA :
#
# MBK via      RDS layer 1   RDS layer 2   RDS layer 3   RDS layer 4
# name          name      width     name      width     name      width
##
```

---

TABLE MBK\_TO\_RDS\_VIA

# The NIMP/PIMP layers are not visualised in Graal. If you want to  
# see the layers, change the keyword for NIMP/PIMP from DRC to ALL.

```

CONT_BODY_P\
    RDS_PTIE  2.00 DRC\
    RDS_PTIE  2.00 EXT\
    RDS_CONT  2.00 ALL\
    RDS_ALU1  2.00 ALL\
    RDS_ACTIV 2.00 DRC\
    RDS_PIMP  2.00 DRC
CONT_BODY_N\
    RDS_NTIE  2.00 DRC\

```

```

RDS_NTIE 2.00 EXT\
RDS_CONT 2.00 ALL\
RDS_ALU1 2.00 ALL\
RDS_ACTIV 2.00 DRC\
RDS_NIMP 2.00 DRC
CONT_DIF_N\
    RDS_NDIF 2.00 ALL\
    RDS_CONT 2.00 ALL\
    RDS_ALU1 2.00 ALL\
    RDS_ACTIV 2.00 DRC\
    RDS_NIMP 2.00 DRC
CONT_DIF_P\
    RDS_PDIF 2.00 ALL\
    RDS_CONT 2.00 ALL\
    RDS_ALU1 2.00 ALL\
    RDS_ACTIV 2.00 DRC\
    RDS_PIMP 2.00 DRC
CONT_POLY\
    RDS_POLY 4.00 ALL\
    RDS_CONT 2.00 ALL\
    RDS_ALU1 2.00 ALL
CONT_VIA\
    RDS_ALU1 2.00 ALL\
    RDS_VIA1 2.00 ALL\
    RDS_ALU2 2.00 ALL
CONT_VIA2\
    RDS_ALU2 2.00 ALL\
    RDS_VIA2 2.00 ALL\
    RDS_ALU3 2.00 ALL
CONT_VIA3\
    RDS_ALU3 2.00 ALL\
    RDS_VIA3 2.00 ALL\
    RDS_ALU4 2.00 ALL
CONT_VIA4\
    RDS_ALU4 2.00 ALL\
    RDS_VIA4 2.00 ALL\
    RDS_ALU5 2.00 ALL
CONT_VIA5\
    RDS_ALU5 2.00 ALL\
    RDS_VIA5 2.00 ALL\
    RDS_ALU6 2.00 ALL
C_X_N\
    RDS_POLY 4.00 ALL\
    RDS_NDIF 2.00 ALL\
    RDS_ACTIV 2.00 ALL
C_X_P\
    RDS_POLY 4.00 ALL\
    RDS_PDIF 2.00 ALL\
    RDS_ACTIV 2.00 ALL

```

END

```
##

---

# TABLE MBK_TO_RDS_BIGVIA_HOLE :

---

#

---

# MBK via      RDS Hole  
# name         name   side step mode

---

##
```

TABLE MBK\_TO\_RDS\_BIGVIA\_HOLE

CONT_VIA	RDS_VIA1	2.00	2.00	ALL
CONT_VIA2	RDS_VIA2	2.00	2.00	ALL
CONT_VIA3	RDS_VIA3	2.00	2.00	ALL
CONT_VIA4	RDS_VIA4	2.00	2.00	ALL
CONT_VIA5	RDS_VIA5	2.00	2.00	ALL

END

```
##

---

# TABLE MBK_TO_RDS_BIGVIA_METAL :

---

#

---

# MBK via      RDS layer 1           ...  
# name         name   delta-width overlap mode

---

##
```

TABLE MBK\_TO\_RDS\_BIGVIA\_METAL

CONT_VIA	RDS_ALU2	0.0	2.00	ALL	RDS_ALU2	0.0	2.00	ALL
CONT_VIA2	RDS_ALU2	0.0	2.00	ALL	RDS_ALU3	0.0	2.00	ALL
CONT_VIA3	RDS_ALU3	0.0	2.00	ALL	RDS_ALU4	0.0	2.00	ALL
CONT_VIA4	RDS_ALU4	0.0	2.00	ALL	RDS_ALU5	0.0	2.00	ALL
CONT_VIA5	RDS_ALU5	0.0	2.00	ALL	RDS_ALU6	0.0	2.00	ALL

END

```
##

---

# TABLE MBK_TO_RDS_TURNVIA :

---

#

---

# MBK via      RDS layer 1           ...  
# name         name   DWR MODE

---

##
```

TABLE MBK\_TO\_RDS\_TURNVIA

CONT_TURN1	RDS_ALU1	0.0	ALL
CONT_TURN2	RDS_ALU2	0.0	ALL
CONT_TURN3	RDS_ALU3	0.0	ALL
CONT_TURN4	RDS_ALU4	0.0	ALL
CONT_TURN5	RDS_ALU5	0.0	ALL
CONT_TURN6	RDS_ALU6	0.0	ALL

END

TABLE MBK\_WIRESETTING

X_GRID	10
Y_GRID	10
Y_SLICE	100
WIDTH_VDD	12
WIDTH_VSS	12
TRACK_WIDTH_ALU8	0
TRACK_WIDTH_ALU7	4
TRACK_WIDTH_ALU6	4
TRACK_WIDTH_ALU5	4
TRACK_WIDTH_ALU4	3
TRACK_WIDTH_ALU3	3
TRACK_WIDTH_ALU2	3
TRACK_WIDTH_ALU1	3
TRACK_SPACING_ALU8	0
TRACK_SPACING_ALU7	4
TRACK_SPACING_ALU6	4
TRACK_SPACING_ALU5	4
TRACK_SPACING_ALU4	4
TRACK_SPACING_ALU3	4
TRACK_SPACING_ALU2	4
TRACK_SPACING_ALU1	3
WMIN_ALU1	3
WMIN_ALU2	3
DMIN_ALU1_ALU1	5
DMIN_ALU2_ALU2	5
WVIA_ALU1	5
WVIA_ALU2	5
EXTENSION_ALU2	1
BV_VIA_VIA	8
WALIM	60

END

##

# TABLE LYNX\_GRAPH :

#

# RDS layer	Rds layer 1	Rds layer 2	...
# name	name	name	...

##

TABLE LYNX\_GRAPH

##

RDS_NDIF	RDS_CONT	RDS_NDIF
RDS_PDIF	RDS_CONT	RDS_PDIF

RDS_NTIE	RDS_CONT	RDS_NTIE						
RDS_PTIE	RDS_CONT	RDS_PTIE						
RDS_POLY	RDS_CONT	RDS_POLY						
RDS_CONT	RDS_PDIF	RDS_NDIF	RDS_POLY	RDS_PTIE	RDS_NTIE	RDS_ALU1	RDS_CONT	
RDS_ALU1	RDS_CONT	RDS_VIA1	RDS_ALU1					
RDS_VIA1	RDS_ALU1	RDS_ALU2	RDS_VIA1					
RDS_VIA2	RDS_ALU2	RDS_ALU3	RDS_VIA2					
RDS_VIA3	RDS_ALU3	RDS_ALU4	RDS_VIA3					
RDS_VIA4	RDS_ALU4	RDS_ALU5	RDS_VIA4					
RDS_VIA5	RDS_ALU5	RDS_ALU6	RDS_VIA5					
RDS_ALU2	RDS_VIA1	RDS_VIA2	RDS_ALU2					
RDS_ALU3	RDS_VIA2	RDS_VIA3	RDS_ALU3					
RDS_ALU4	RDS_VIA3	RDS_VIA4	RDS_ALU4					
RDS_ALU5	RDS_VIA4	RDS_VIA5	RDS_ALU5					
RDS_ALU6	RDS_VIA5		RDS_ALU6					

END

```

##  

# TABLE LYNX.CAPA :  

#  

# RDS layer      Surface capacitance    Perimetric capacitance  

# name           piF / Micron^2          piF / Micron  

##
```

## TABLE LYNX\_CAPA

#	poly	alu0	alu1	alu2	alu3	alu4	alu5	alu6
# pitch	7	14	14	16	16	16	16	36
RDS_POLY		10.10E-05		10.00e-05				
RDS_ALU1		3.400e-05		5.300e-05				
RDS_ALU2		1.400e-05		3.600e-05				
RDS_ALU3		0.900e-05		2.900e-05				
RDS_ALU4		0.700e-05		2.400e-05				
RDS_ALU5		0.500e-05		2.100e-05				
RDS_ALU6		0.400e-05		1.900e-05				

END

```
##  
# TABLE LYNX.RESISTOR :  
#  
# RDS layer      Surface resistor  
# name           Ohm / Micron^2  
##
```

TABLE LYNX\_RESISTOR

RDS-POLY 8.3

```
RDS_ALU1      0.08
RDS_ALU2      0.08
RDS_ALU3      0.08
RDS_ALU4      0.08
RDS_ALU5      0.07
RDS_ALU6      0.01
```

```
END
```

---

```
##_
# TABLE LYNX_TRANSISTOR :
#
# MBK layer   Transistor Type  MBK via
# name        name          name
##_
```

```
TABLE LYNX_TRANSISTOR
```

NTRANS	NTRANS	C_X_N	RDS_POLY	RDS_NDIF	RDS_NDIF	RDS_PWELL
PTRANS	PTRANS	C_X_P	RDS_POLY	RDS_PDIF	RDS_PDIF	RDS_NWELL

```
END
```

---

```
##_
# TABLE LYNX_DIFFUSION :
#
# RDS layer   RDS layer
# name        name
##_
```

```
TABLE LYNX_DIFFUSION
```

```
END
```

---

```
##_
# TABLE LYNX_BULK_IMPLICIT :
#
# RDS layer   Bulk type
# name        EXPLICIT/IMPLICIT
##_
```

```
TABLE LYNX_BULK_IMPLICIT
END
```

---

```
##_
# TABLE S2R_OVERSIZE_DENOTCH :
##_
```

```
TABLE S2R_OVERSIZE_DENOTCH
```

```

RDS_NWELL 0.0
RDS_PWELL 0.0
RDS_ACTIV 0.0
RDS_PDIF 0.0
RDS_NDIF 0.0
RDS_NTIE 0.0
RDS_PTIE 0.0
# The NIMP and PIMP values are used to set the width of WELL and
# IMPlant beyond the Abox. Values set equal to the NIMP/PIMP
# overlap of TIE contact so that thin slivers of IMPlant are not
# inserted between the TIE implant and well edge.
RDS_PIMP 0.0
RDS_NIMP 0.0
# Denotch NIMP and PIMP with user layers allowing single implant
# contact between two implant edges.
# Width is (2.5+6.2a)*2+6.1=(0.20+0.08)*2+0.16=0.72. Denotch just below.
RDS_POLY 0.0
RDS_ALU1 0.0
RDS_ALU2 0.0
RDS_ALU3 0.0
RDS_ALU4 0.0
RDS_ALU5 0.0
RDS_ALU6 0.0
END

##-
# TABLE S2R_BLOC_RING_WIDTH :
##-

TABLE S2R_BLOC_RING_WIDTH
END

##-
# TABLE S2R_MINIMUM_LAYER_WIDTH :
##-

TABLE S2R_MINIMUM_LAYER_WIDTH

RDS_NWELL 12.0
RDS_PWELL 12.0
RDS_NDIF 3.0
RDS_PDIF 3.0
RDS_NTIE 3.0
RDS_PTIE 3.0
RDS_PIMP 7.0
RDS_NIMP 7.0
RDS_POLY 2.0
RDS_CONT 2.0
RDS_ALU1 3.0
RDS_VIA1 3.0

```

```
RDS_ALU2      3.0
RDS_VIA2      3.0
RDS_ALU3      3.0
RDS_VIA3      3.0
RDS_ALU4      3.0
RDS_VIA4      3.0
RDS_ALU5      3.0
RDS_VIA5      3.0
RDS_ALU6      5.0
RDS_REF       2.0
```

```
END
```

---

```
##_____
# TABLE CIF_LAYER :
##_____
```

```
TABLE CIF_LAYER
# Layer definitions used by MOSIS
#_____
```

```
RDS_NWELL    CWN
RDS_PWELL    CWP
RDS_NDIF     CND
RDS_PDIF     CPD
```

```
# PTIE and NTIE actually provide the implants
# around the cutouts for CONT_BODY_N and _P.
```

```
RDS_PTIE     CSP
RDS_NTIE     CSN
RDS_ACTIV    CAA
RDS_PIMP    CSP
RDS_NIMP    CSN
RDS_POLY    CPG
RDS_CONT    CCC
RDS_ALU1    CM1
RDS_VIA1    CV1
RDS_ALU2    CM2
RDS_VIA2    CV2
RDS_ALU3    CM3
RDS_VIA3    CV3
RDS_ALU4    CM4
RDS_VIA4    CV4
RDS_ALU5    CM5
RDS_VIA5    CV5
RDS_ALU6    CM6
RDS_REF     REF
```

```
# RDS_TALU8    AB
```

```
# Layer definitions used by Alliance
#_____
# RDS_NWELL    LNWELL
```

```

# RDS_PWELL    LPWELL
# RDS_NDIF     LNDIF
# RDS_PDIF     LPDIF
# RDS_TPOLY    LTPOLY
# RDS_VPOLY    LVPOLY
# RDS_NTIE     LNTIE
# RDS_PTIE     LPTIE
# RDS_PIMP     LPIMP
# RDS_NIMP     LNIMP
# RDS_POLY     LPOLY
# RDS_POLY2    LPOLY2
# RDS_CONT     LCONT
# RDS_POLY2    LALU1
# RDS_ALU1     LALU1
# RDS_TALU1    LTALU1
# RDS_VIA1     LVIA
# RDS_ALU2     LALU2
# RDS_TALU2    LTALU2
# RDS_VIA2     LVIA2
# RDS_ALU3     LALU3
# RDS_TALU3    LTALU3
# RDS_VIA3     LVIA3
# RDS_ALU4     LALU4
# RDS_TALU4    LTALU4
# RDS_VIA4     LVIA4
# RDS_ALU5     LALU5
# RDS_TALU5    LTALU5
# RDS_VIA5     LVIA5
# RDS_ALU6     LALU6
# RDS_TALU6    LTALU6
# RDS_REF      LREF
END

```

---

```

##-----#
# TABLE GDS_LAYER :
##-----#

```

```

TABLE GDS_LAYER
# Layer definitions used by MOSIS
#
RDS_PWELL    41
RDS_NWELL    42
RDS_NDIF     43
RDS_PDIF     43
RDS_PTIE     44
RDS_NTIE     45
RDS_ACTIV    43
RDS_PIMP     44
RDS_NIMP     45
RDS_POLY     46  46

```

```

RDS_CONT      25
# RDS_POLY2    49 49
RDS_ALU1      49 49
RDS_VIA1      50
RDS_ALU2      51 51
RDS_VIA2      61
RDS_ALU3      62 62
RDS_VIA3      30
RDS_ALU4      31 31
RDS_VIA4      32
RDS_ALU5      33 33
RDS_VIA5      36
RDS_ALU6      37 37
# RDS_REF      24
# RDS_TALU8    63

```

END

---

```

##-
# TABLE S2R_POST_TREAT :
##-
```

---

TABLE S2R\_POST\_TREAT

```

RDS_NWELL TREAT NULL
RDS_PWELL TREAT NULL
RDS_NDIF  TREAT NULL
RDS_PDIF   TREAT NULL
RDS_NTIE   TREAT NULL
RDS_PTIE   TREAT NULL
RDS_NIMP   TREAT NULL
RDS_PIMP   TREAT NULL
RDS_ACTIV  TREAT NULL
RDS_POLY   TREAT NULL
RDS_CONT   NOTREAT NULL
RDS_VIA1   NOTREAT NULL
RDS_VIA2   NOTREAT NULL
RDS_VIA3   NOTREAT NULL
RDS_VIA4   NOTREAT NULL
RDS_VIA5   NOTREAT NULL
RDS_ALU1   TREAT NULL
RDS_ALU2   TREAT NULL
RDS_ALU3   TREAT NULL
RDS_ALU4   TREAT NULL
RDS_ALU5   TREAT NULL
RDS_ALU6   TREAT NULL

```

```

# Two RDS_TALU8 rectangles are written , one with no name and
# one with the cell name. When merged , the name is lost .
# It is prefered to have a single rectangle with no name rather

```

```

# than two, one of which is named.

END

##-----
## All layers used in the regles must be listed here first.
## Otherwise you get an error like :
# DRUC ERR: Undefined RDS LAYER
##-----
DRC_RULES

layer RDS_NWELL 12.0;
layer RDS_PWELL 12.0;
layer RDS_NTIE 3.0 ;
layer RDS_PTIE 3.0 ;
layer RDS_NDIF 3.0 ;
layer RDS_PDIF 3.0 ;
layer RDS_ACTIV 3.0 ;
layer RDS_PIMP 5.0 ;
layer RDS_NIMP 5.0 ;
layer RDS_CONT 2.0 ;
layer RDS_VIA1 3.0 ;
layer RDS_VIA2 3.0 ;
layer RDS_VIA3 3.0 ;
layer RDS_VIA4 3.0 ;
layer RDS_VIA5 4.0 ;
layer RDS_POLY 2.0 ;
layer RDS_GATE 2.0 ;
layer RDS_ALU1 3.0 ;
layer RDS_ALU2 3.0 ;
layer RDS_ALU3 3.0 ;
layer RDS_ALU4 3.0 ;
layer RDS_ALU5 3.0 ;
layer RDS_ALU6 5.0 ;

layer RDS_REF 2.0 ;

regles

# Note : ‘‘min’’ is different from ‘‘>=’’.
# min is applied on polygons and >= is applied on rectangles.
# There is the same difference between max and <=.
# >= is faster than min, but min must be used where it is
# required to consider polygons, for example distance of
# two objects in the same layer
#
# Check the NWELL shapes
#
caracterise RDS_NWELL (
    regle 110 : largeur >= 12.0 ;

```

```

    regle 111 : longueur_inter min 12.0 ;
    regle 130 : notch >= 12.0 ;
);
relation RDS_NWELL , RDS_NWELL (
    regle 131 : distance axiale min 6.0 ;
);

# Check the PWELL shapes
#
caracterise RDS_PWELL (
    regle 112 : largeur >= 12.0 ;
    regle 113 : longueur_inter min 12.0 ;
    regle 132 : notch >= 12.0 ;
);
relation RDS_PWELL , RDS_PWELL (
    regle 133 : distance axiale min 6.0 ;
);

define RDS_NWELL , RDS_PWELL intersection -> BOTH_WELLS;

# Check no NWELL and PWELL overlap
#
# Won't work with PWELL made from symbolic NWELL
caracterise BOTH_WELLS (
    regle 140 : largeur max 0.0 ;
);
relation RDS_PWELL , RDS_NWELL (
    regle 141 : distance axiale min 0.0 ;
);

undefine BOTH_WELLS;

# Check the RDS_PDIF shapes
#
caracterise RDS_PDIF (
    regle 210 : largeur >= 3.0 ;
    regle 211 : longueur_inter min 3.0 ;
    regle 220 : notch >= 3.0 ;
);
relation RDS_PDIF , RDS_PDIF (
    regle 221 : distance axiale min 3.0 ;
);

# Check the RDS_NDIF shapes
#
caracterise RDS_NDIF (
    regle 212 : largeur >= 3.0 ;
    regle 213 : longueur_inter min 3.0 ;
    regle 222 : notch >= 3.0 ;
);

```

```

relation RDS_NDIF , RDS_NDIF (
    regle 223 : distance axiale min 3.0 ;
);

# define PSUB and NSUB layers for easier
# understanding of design rules

# Check RDS_NDIF is outside NWELL
#
relation RDS_NDIF , RDS_NWELL (
    regle 230 : distance axiale >= 6.0 ;
    regle 231 : enveloppe longueur_inter < 0.0 ;
    regle 232 : croix longueur_inter < 0.0 ;
    regle 233 : intersection longueur_inter < 0.0 ;
    regle 234 : extension longueur_inter < 0.0 ;
    regle 235 : inclusion longueur_inter < 0.0 ;
);
relation RDS_NWELL , RDS_NDIF (
    regle 236 : marge longueur_inter < 0.0 ;
);

# Check RDS_PDIF is inside NWELL
#
relation RDS_NWELL , RDS_PDIF (
    regle 237 : enveloppe inferieure min 6.0 ;
);

# Check RDS_PTIE is outside NWELL
#
relation RDS_PTIE , RDS_NWELL (
    regle 240 : distance axiale >= 3.0 ;
    regle 241 : enveloppe longueur_inter < 0.0 ;
    regle 242 : croix longueur_inter < 0.0 ;
    regle 243 : intersection longueur_inter < 0.0 ;
    regle 244 : extension longueur_inter < 0.0 ;
    regle 245 : inclusion longueur_inter < 0.0 ;
);
relation RDS_NWELL , RDS_PTIE (
    regle 246 : marge longueur_inter < 0.0 ;
);

# Check RDS_NTIE is inside NWELL
#
relation RDS_NWELL , RDS_NTIE (
    regle 247 : enveloppe inferieure min 3.0 ;
);

# Check NDIF and PDIF separation
#
relation RDS_NDIF , RDS_PTIE (

```

```

regle 250 : distance axiale min 4.0 ;
regle 251 : intersection longueur_inter < 0.0 ;
regle 252 : extension longueur_inter < 0.0 ;
regle 253 : inclusion longueur_inter < 0.0 ;
);
relation RDS_PDIF , RDS_NTIE (
    regle 254 : distance axiale min 4.0 ;
    regle 255 : intersection longueur_inter < 0.0 ;
    regle 256 : extension longueur_inter < 0.0 ;
    regle 257 : inclusion longueur_inter < 0.0 ;
);
# Check RDS_PDIF is outside PWELL
#
relation RDS_PDIF , RDS_PWELL (
    regle 260 : distance axiale >= 6.0 ;
    regle 261 : enveloppe longueur_inter < 0.0 ;
    regle 262 : croix longueur_inter < 0.0 ;
    regle 263 : intersection longueur_inter < 0.0 ;
    regle 264 : extension longueur_inter < 0.0 ;
    regle 265 : inclusion longueur_inter < 0.0 ;
);
relation RDS_PWELL , RDS_PDIF (
    regle 266 : marge longueur_inter < 0.0 ;
);
# Check RDS_NDIF is inside PWELL
#
relation RDS_PWELL , RDS_NDIF (
    regle 267 : enveloppe inferieure min 6.0 ;
);
# Check RDS_NTIE is outside PWELL
#
relation RDS_NTIE , RDS_PWELL (
    regle 270 : distance axiale >= 3.0 ;
    regle 271 : enveloppe longueur_inter < 0.0 ;
    regle 272 : croix longueur_inter < 0.0 ;
    regle 273 : intersection longueur_inter < 0.0 ;
    regle 274 : extension longueur_inter < 0.0 ;
    regle 275 : inclusion longueur_inter < 0.0 ;
);
relation RDS_PWELL , RDS_NTIE (
    regle 276 : marge longueur_inter < 0.0 ;
);
# Check RDS_PTIE is inside PWELL
#
relation RDS_PWELL , RDS_PTIE (
    regle 277 : enveloppe inferieure min 3.0 ;
);

```

```

);

# Check opposite implant diffusion spacings
#
# These rules added to flag DRC errors even if
# NWELL and PWELL are not visualised in Graal
#
relation RDS_PDIF , RDS_NDIF (
# distance is nwell overlap pdif plus nwell space to ndif
    regle 280 : distance axiale min 12.0 ;
);
relation RDS_PDIF , RDS_PTIE (
# distance is nwell overlap pdif plus nwell space to ptie
    regle 281 : distance axiale min 9.0 ;
);
relation RDS_NTIE , RDS_NDIF (
# distance is nwell overlap ntie plus nwell space to ndif
    regle 282 : distance axiale min 9.0 ;
);
# distance is nwell overlap ntie plus nwell space to ptie
relation RDS_NTIE , RDS_PTIE (
    regle 283 : distance axiale min 6.0 ;
);

define RDS_ACTIV , RDS_Poly intersection -> CHANNEL;

# Check the RDS_Poly shapes
#
characterise RDS_Poly (
    regle 310 : largeur >= 2.0 ;
    regle 311 : longueur_inter >= 2.0 ;
    regle 320 : notch >= 3.0 ;
);
relation RDS_Poly , RDS_Poly (
    regle 321 : distance axiale min 3.0 ;
);

# Check the CHANNEL shapes
#
characterise CHANNEL (
    regle 322 : notch >= 3.0 ;
);
relation CHANNEL , CHANNEL (
    regle 323 : distance axiale min 3.0 ;
);

# Check POLY overlap of TRANSISTOR (ENDCAP)
#
relation RDS_Poly , RDS_PDIF (
    regle 330 : croix longueur_min min 2.5 ;

```

```

);
relation RDS_POLY , RDS_NDIF (
    regle 331 : croix longueur_min min 2.5 ;
);

# Check SOURCE/DRAIN width
#
relation RDS_PDIF , RDS_GATE (
    regle 340 : croix longueur_min min 4.0 ;
);
relation RDS_NDIF , RDS_GATE (
    regle 341 : croix longueur_min min 4.0 ;
);

# Check RDS_POLY separation to DIF
#
relation RDS_POLY , RDS_PDIF (
    regle 350 : distance axiale min 1.0 ;
);
relation RDS_POLY , RDS_NDIF (
    regle 351 : distance axiale min 1.0 ;
);
relation RDS_POLY , RDS_PTIE (
    regle 352 : distance axiale min 1.0 ;
);
relation RDS_POLY , RDS_NTIE (
    regle 353 : distance axiale min 1.0 ;
);

# Check RDS_POLY separation to TRANSISTOR CHANNEL
#
relation RDS_POLY , CHANNEL (
    regle 354 : distance axiale >= 1.0 ;
);

define RDS_POLY , CHANNEL exclusion -> FIELD_POLY;
define RDS_PDIF , RDS_POLY intersection -> PGATE;

# Check RDS_POLY does not overlap PDIF
#
relation PGATE , FIELD_POLY (
    regle 355 : inclusion longueur_inter < 0.0 ;
);
relation FIELD_POLY , PGATE (
    regle 356 : extension longueur_inter < 0.0 ;
);

undefine PGATE;
define RDS_NDIF , RDS_POLY intersection -> NGATE;

```

```

# Check RDS_POLY does not overlap NDIF
#
relation NGATE , FIELD.POLY (
    regle 357 : inclusion longueur_inter < 0.0 ;
);
relation FIELD.POLY , NGATE (
    regle 358 : extension longueur_inter < 0.0 ;
);

undefine NGATE;
define RDS_PDIF , CHANNEL intersection -> PTR;

# N-select and P-select rules
#
relation PTR , RDS.NIMP (
    regle 410 : distance axiale min 3.0 ;
);

undefine PTR;
define RDS_NDIF , CHANNEL intersection -> NTR;

relation NTR , RDS.PIMP (
    regle 411 : distance axiale min 3.0 ;
);

undefine NTR;
undefine FIELD.POLY;
relation RDS_PIMP , RDS.PDIF (
    regle 420 : enveloppe inferieure min 2.0 ;
);
relation RDS_NIMP , RDS_NDIF (
    regle 422 : enveloppe inferieure min 2.0 ;
);

define RDS_PIMP , RDS.PWELL intersection -> TIE_PIMP;
define RDS_NIMP , RDS.NWELL intersection -> TIE_NIMP;

# Check min SELECT widths for TIE implant
#
caracterise TIE_PIMP (
    regle 440 : largeur >= 4.0 ;
    regle 441 : longueur_inter min 4.0 ;
);
# This is the min NIMP width rule
relation TIE_PIMP , TIE_PIMP (
    regle 444 : distance axiale min 4.0 ;
);
caracterise TIE_NIMP (
    regle 442 : largeur >= 4.0 ;
    regle 443 : longueur_inter min 4.0 ;
);

```

```

);
# This is the min PIMP width rule
relation TIE_NIMP , TIE_NIMP (
    regle 445 : distance axiale min 4.0 ;
);

undefine TIE_NIMP;
undefine TIE_PIMP;
define RDS_POLY , RDS_CONT intersection -> POLY_CONT;

# Check CONT layer size , separation and overlaps
#
caracterise POLY_CONT (
    regle 510 : largeur max 2.0 ;
    regle 511 : largeur min 2.0 ;
);
relation RDS_POLY , RDS_CONT (
    regle 520 : enveloppe inferieure min 1.0 ;
);
relation RDS_CONT , RDS_CONT (
    regle 530 : distance axiale min 4.0 ;
);

# Check POLY CONTACT separation from TRANSISTOR CHANNEL
#
relation CHANNEL , POLY_CONT (
    regle 540 : distance axiale >= 3.0 ;
);

undefine POLY_CONT;
define RDS_CONT , CHANNEL intersection -> BAD_CONT;

# CONTACT not allowed over TRANSISTOR
#
caracterise BAD_CONT (
    regle 580 : largeur max 0.0 ;
);
undefine BAD_CONT;

define RDS_PDIF , RDS_CONT intersection -> PDIF_CONT;
caracterise PDIF_CONT (
    regle 610 : longueur max 2.0 ;
    regle 611 : longueur_inter min 2.0 ;
);
# Check PDIF CONTACT separation from TRANSISTOR CHANNEL
#
relation CHANNEL , PDIF_CONT (
    regle 640 : distance axiale >= 2.0 ;
);

```

```

undefine PDIF_CONT;
define RDS_NDIF , RDS_CONT intersection -> NDIF_CONT;

caracterise NDIF_CONT (
    regle 612 : longueur max 2.0 ;
    regle 613 : longueur_inter min 2.0 ;
);
# Check NDIF CONTACT separation from TRANSISTOR CHANNEL
#
relation CHANNEL , NDIF_CONT (
    regle 641 : distance axiale >= 2.0 ;
);

undefine NDIF_CONT;
define RDS_PTIE , RDS_CONT intersection -> PTIE_CONT;
caracterise PTIE_CONT (
    regle 614 : longueur max 2.0 ;
    regle 615 : longueur_inter min 2.0 ;
);
# Check PTIE CONTACT separation from TRANSISTOR CHANNEL
#
relation CHANNEL , PTIE_CONT (
    regle 642 : distance axiale >= 3.0 ;
);

undefine PTIE_CONT;
define RDS_NTIE , RDS_CONT intersection -> NTIE_CONT;

caracterise NTIE_CONT (
    regle 616 : longueur max 2.0 ;
    regle 617 : longueur_inter min 2.0 ;
);
# Check NTIE CONTACT separation from TRANSISTOR CHANNEL
#
relation CHANNEL , NTIE_CONT (
    regle 643 : distance axiale >= 3.0 ;
);

undefine NTIE_CONT;

relation RDS_PDIF , RDS_CONT (
    regle 620 : enveloppe inferieure min 1.0 ;
);
relation RDS_NDIF , RDS_CONT (
    regle 621 : enveloppe inferieure min 1.0 ;
);
relation RDS_PTIE , RDS_CONT (
    regle 622 : enveloppe inferieure min 1.0 ;
);

```

```

relation RDS_NTIE , RDS_CONT (
    regle 623 : enveloppe inferieure min 1.0 ;
);

undefine CHANNEL;

# Check RDS_ALU1 shapes
#
characterise RDS_ALU1 (
    regle 710 : largeur >= 3.0 ;
    regle 711 : longueur_inter min 3.0 ;
);
relation RDS_ALU1 , RDS_ALU1 (
    regle 724 : distance axiale min 3.0 ;
);
# Check ALU1 side overlap of CONT
#



# Check VIA layer size and separation
#
characterise RDS_VIA1 (
    regle 810 : largeur <= 3.0 ;
    regle 811 : largeur >= 3.0 ;
);
relation RDS_VIA1 , RDS_VIA1 (
    regle 820 : distance axiale min 3.0 ;
);

# Check ALU1 overlap of VIA1
#
relation RDS_ALU1 , RDS_VIA1 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 830 : enveloppe inferieure min 1.0 ;
    regle 831 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA1 , RDS_ALU1 (
#    regle 832 : intersection longueur_inter max 0.0 ;
#);

# Check RDS_ALU2 shapes
#
characterise RDS_ALU2 (
    regle 910 : largeur >= 3.0 ;
    regle 911 : longueur_inter min 3.0 ;
    regle 920 : notch >= 4.0 ;
);
relation RDS_ALU2 , RDS_ALU2 (

```

```

    regle 921 : distance axiale min 4.0 ;
);
# Check ALU2 overlap of VIA1
#
relation RDS_ALU2 , RDS_VIA1 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 930 : enveloppe inferieure min 1.0 ;
    regle 931 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA1 , RDS_ALU2 (
#   regle 932 : intersection longueur_inter max 0.0 ;
#);

# Check VIA2 layer size and separation
#
caracterise RDS_VIA2 (
    regle 1410 : largeur <= 3.0 ;
    regle 1411 : largeur >= 3.0 ;
);
relation RDS_VIA2 , RDS_VIA2 (
    regle 1420 : distance axiale min 3.0 ;
);

# Check ALU2 overlap of VIA2
#
relation RDS_ALU2 , RDS_VIA2 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 1430 : enveloppe inferieure min 1.0 ;
    regle 1431 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA2 , RDS_ALU2 (
#   regle 1432 : intersection longueur_inter max 0.0 ;
#);

# Check RDS_ALU3 shapes
#
caracterise RDS_ALU3 (
    regle 1510 : largeur >= 3.0 ;
    regle 1511 : longueur_inter min 3.0 ;
    regle 1520 : notch >= 4.0 ;
);
relation RDS_ALU3 , RDS_ALU3 (
    regle 1521 : distance axiale min 3.0 ;
);
# Check ALU3 overlap of VIA2
#

```

```

relation RDS_ALU3 , RDS_VIA2 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 1530 : enveloppe inferieure min 1.0 ;
    regle 1531 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA2 , RDS_ALU3 (
#    regle 1532 : intersection longueur_inter max 0.0 ;
#);

# Check VIA3 layer size and separation
#
caracterise RDS_VIA3 (
    regle 2110 : largeur <= 3.0 ;
    regle 2111 : largeur >= 3.0 ;
);
relation RDS_VIA3 , RDS_VIA3 (
    regle 2120 : distance axiale min 3.0 ;
);

# Check ALU3 overlap of VIA3
#
relation RDS_ALU3 , RDS_VIA3 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 2130 : enveloppe inferieure min 1.0 ;
    regle 2131 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA3 , RDS_ALU3 (
#    regle 2132 : intersection longueur_inter max 0.0 ;
#);

# Check RDS_ALU4 shapes
#
caracterise RDS_ALU4 (
    regle 2210 : largeur >= 3.0 ;
    regle 2211 : longueur_inter min 3.0 ;
    regle 2220 : notch >= 4.0 ;
);
relation RDS_ALU4 , RDS_ALU4 (
    regle 2221 : distance axiale min 4.0 ;
);
# Check ALU4 overlap of VIA3
#
relation RDS_ALU4 , RDS_VIA3 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 2230 : enveloppe inferieure min 1.0 ;
    regle 2231 : marge longueur_inter max 1.0 ;
);

```

```

);
#relation RDS_VIA3 , RDS_ALU4 (
#  regle 2232 : intersection longueur_inter max 0.0 ;
#);

# Check VIA4 layer size and separation
#
characterise RDS_VIA4 (
  regle 2510 : largeur <= 3.0 ;
  regle 2511 : largeur >= 3.0 ;
);
relation RDS_VIA4 , RDS_VIA4 (
  regle 2520 : distance axiale min 3.0 ;
);

# Check ALU4 overlap of VIA4
#
relation RDS_ALU4 , RDS_VIA4 (
# Case 1: side overlap
# Basic side overlap checked on all sides
  regle 2530 : enveloppe inferieure min 1.0 ;
  regle 2531 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA4 , RDS_ALU4 (
#  regle 2532 : intersection longueur_inter max 0.0 ;
#);

# Check RDS_ALU5 shapes
#
characterise RDS_ALU5 (
  regle 2610 : largeur >= 3.0 ;
  regle 2611 : longueur_inter min 3.0 ;
  regle 2620 : notch >= 4.0 ;
);
relation RDS_ALU5 , RDS_ALU5 (
  regle 2621 : distance axiale min 4.0 ;
);
# Check ALU5 overlap of VIA4
#
relation RDS_ALU5 , RDS_VIA4 (
# Case 1: side overlap
# Basic side overlap checked on all sides
  regle 2630 : enveloppe inferieure min 1.0 ;
  regle 2631 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA4 , RDS_ALU5 (
#  regle 2632 : intersection longueur_inter max 0.0 ;
#);

```

```

# VIA5 and ALU6 width and spacings
# larger than lower layers
#
# characterise RDS_VIA5 (
    regle 2910 : largeur <= 4.0 ;
    regle 2911 : largeur >= 4.0 ;
);
relation RDS_VIA5 , RDS_VIA5 (
    regle 2920 : distance axiale min 4.0 ;
);

# Check ALU5 overlap of VIA5
#
# relation RDS_ALU5 , RDS_VIA5 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 2930 : enveloppe inferieure min 1.0 ;
    regle 2931 : marge longueur_inter max 1.0 ;
);
#relation RDS_VIA5 , RDS_ALU5 (
#   regle 2932 : intersection longueur_inter max 0.0 ;
#);

# Check RDS_ALU6 shapes
#
# characterise RDS_ALU6 (
    regle 3010 : largeur >= 5.0 ;
    regle 3011 : longueur_inter min 5.0 ;
    regle 3020 : notch >= 5.0 ;
);
relation RDS_ALU6 , RDS_ALU6 (
    regle 3021 : distance axiale min 5.0 ;
);
# Check ALU6 overlap of VIA5
#
# relation RDS_ALU6 , RDS_VIA5 (
# Case 1: side overlap
# Basic side overlap checked on all sides
    regle 3030 : enveloppe inferieure min 2.0 ;
    regle 3031 : marge longueur_inter max 2.0 ;
);

fin regles
DRC_COMMENT
110 1.1 NWELL Width < 12.0um ( 12 lambda)
111 1.1 NWELL Width < 12.0um ( 12 lambda)
112 1.1 PWELL Width < 12.0um ( 12 lambda)

```

113 1.1 PWELL Width < 12.0um ( 12 lambda)  
 130 1.3 NWELL Notch < 6.0 um ( 6 lambda)  
 131 1.3 NWELL Space < 6.0 um ( 6 lambda)  
 132 1.3 PWELL Notch < 6.0 um ( 6 lambda)  
 133 1.3 PWELL Space < 6.0 um ( 6 lambda)  
 140 1.4 NWELL and PWELL must not overlap ( misaligned NWELL?)  
 141 1.4 NWELL and PWELL Space < 0um  
 210 2.1a PDIF Width < 3.0 um ( 3 lambda)  
 211 2.1a PDIF Width < 3.0 um ( 3 lambda)  
 220 2.2a PDIF Notch < 3.0 um ( 3 lambda)  
 221 2.2a PDIF Space < 3.0 um ( 3 lambda)  
 212 2.1a NDIF Width < 3.0 um ( 3 lambda)  
 213 2.1a NDIF Width < 3.0 um ( 3 lambda)  
 222 2.2a NDIF Notch < 3.0 um ( 3 lambda)  
 223 2.2a NDIF Space < 3.0 um ( 3 lambda)  
 214 2.1b PTIE Width < 3.0 um ( 3 lambda)  
 215 2.1b PTIE Width < 3.0 um ( 3 lambda)  
 224 2.2b PTIE Notch < 3.0 um ( 3 lambda)  
 225 2.2b PTIE Space < 3.0 um ( 3 lambda)  
 216 2.1b NTIE Width < 3.0 um ( 3 lambda)  
 217 2.1b NTIE Width < 3.0 um ( 3 lambda)  
 226 2.2b NTIE Notch < 3.0 um ( 3 lambda)  
 227 2.2b NTIE Space < 3.0 um ( 3 lambda)  
 230 2.3a NWELL to NDIF Space < 6.0 um ( 6 lambda)  
 231 2.3a NDIF must not touch NWELL  
 232 2.3a NDIF must not touch NWELL  
 233 2.3a NDIF must not touch NWELL  
 234 2.3a NDIF must not touch NWELL  
 235 2.3a NDIF must not touch NWELL  
 236 2.3a NDIF must not touch NWELL  
 237 2.3b NWELL Overlap of PDIF < 6.0 um ( 6 lambda)  
 240 2.4a NWELL to PTIE Space < 3.0 um (3 lambda)  
 241 2.4a PTIE must not touch NWELL  
 242 2.4a PTIE must not touch NWELL  
 243 2.4a PTIE must not touch NWELL  
 244 2.4a PTIE must not touch NWELL  
 245 2.4a PTIE must not touch NWELL  
 246 2.4a PTIE must not touch NWELL  
 247 2.4b NWELL Overlap of NTIE < 3.0 um (3 lambda)  
 250 2.5 NDIF to PTIE Space < 4.0 um (4 lambda)  
 251 2.5 NDIF must not touch or overlap PTIE  
 252 2.5 NDIF must not touch or overlap PTIE  
 253 2.5 NDIF must not touch or overlap PTIE  
 254 2.5 PDIF to NTIE Space < 4.0 um (4 lambda)  
 255 2.5 PDIF must not touch or overlap NTIE  
 256 2.5 PDIF must not touch or overlap NTIE  
 257 2.5 PDIF must not touch or overlap NTIE  
 260 2.3b PWELL to PDIF Space < 6.0 um (6 lambda)  
 261 2.3b PDIF must not touch PWELL  
 262 2.3b PDIF must not touch PWELL

263 2.3b PDIF must not touch PWELL  
 264 2.3b PDIF must not touch PWELL  
 265 2.3b PDIF must not touch PWELL  
 266 2.3b PDIF must not touch PWELL  
 267 2.3a PWELL Overlap of NDIF 6.0 um (6 lambda)  
 270 2.4b PWELL to NTIE Space 3.0 um (3 lambda)  
 271 2.4b NTIE must not touch PWELL  
 272 2.4b NTIE must not touch PWELL  
 273 2.4b NTIE must not touch PWELL  
 274 2.4b NTIE must not touch PWELL  
 275 2.4b NTIE must not touch PWELL  
 276 2.4b NTIE must not touch PWELL  
 277 2.4a PWELL Overlap of PTIE < 3.0 um (3 lambda)  
 280 2.8a PDIF to NDIF Space < 12.0um (12 lambda)  
 281 2.8b PDIF to PTIE Space < 9.0um (9 lambda)  
 282 2.8b NTIE to NDIF Space < 9.0um (9 lambda)  
 283 2.8c NTIE to PTIE Space < 6.0 um (6 lambda)  
 310 3.1 POLY Width < 2.0 um (2 lambda)  
 311 3.1 POLY Width < 2.0 um (2 lambda)  
 320 3.2 POLY Notch < 3.0 um (3 lambda)  
 321 3.2 POLY Space < 3.0 um (3 lambda)  
 322 3.2a CHANNEL Space < 4.0 um (4 lambda)  
 323 3.2a CHANNEL Space < 4.0 um (4 lambda)  
 330 3.3 POLY Overlap of P-TRANSISTOR < 2.5 um (2.5 lambda)  
 331 3.3 POLY Overlap of N-TRANSISTOR < 2.5 um (2.5 lambda)  
 340 3.4 P-TRANSISTOR SOURCE/DRAIN Width < 4.0 um (4 lambda)  
 341 3.4 N-TRANSISTOR SOURCE/DRAIN Width < 4.0 um (4 lambda)  
 350 3.5 PDIF to POLY Space < 1.0 um (1 lambda)  
 351 3.5 NDIF to POLY Space < 1.0 um (1 lambda)  
 352 3.5 PTIE to POLY Space < 1.0 um (1 lambda)  
 353 3.5 NTIE to POLY Space < 1.0 um (1 lambda)  
 354 3.5a POLY to GATE Space < 1.0 um (1 lambda)  
 355 3.5 POLY must not touch or overlap PDIF  
 356 3.5 POLY must not touch or overlap PDIF  
 357 3.5 POLY must not touch or overlap NDIF  
 358 3.5 POLY must not touch or overlap NDIF  
 410 4.1 NIMP to P-TRANSISTOR Space < 3.0 um (3 lambda)  
 411 4.1 PIMP to N-TRANSISTOR Space < 3.0 um (3 lambda)  
 420 4.2a PIMP Overlap of PDIF < 2.0 um (2 lambda)  
 421 4.2b PIMP Overlap of PTIE < 2.0 um (2 lambda)  
 422 4.2a NIMP Overlap of NDIF < 2.0 um (2 lambda)  
 423 4.2b NIMP Overlap of NTIE < 2.0 um (2 lambda)  
 440 4.4 PIMP in PWELL Width < 4.0 um (4 lambda)  
 441 4.4 PIMP in PWELL Width < 4.0 um (4 lambda)  
 442 4.4 NIMP in NWELL Width < 4.0 um (4 lambda)  
 443 4.4 NIMP in NWELL Width < 4.0 um (4 lambda)  
 444 4.4 PIMP in PWELL Space < 4.0 um (4 lambda)  
 445 4.4 NIMP in NWELL Space < 4.0 um (4 lambda)  
 510 5.1 POLY CONTACT Width > 2.0 um (2 lambda)  
 511 5.1 POLY CONTACT Width < 2.0 um (2 lambda)

520 5.2 POLY Overlap of CONTACT < 1.5um (1.5 lambda)  
 530 5.3 CONTACT Space < 4.0 um (4 lambda)  
 540 5.4 POLY CONTACT to CHANNEL Space < 2.0 um (2 lambda)  
 580 5.8 CONTACT not allowed over TRANSISTOR  
 610 6.1 PDIF CONTACT Width > 2.0 um (2 lambda)  
 611 6.1 PDIF CONTACT Width < 2.0 um (2 lambda)  
 612 6.1 NDIF CONTACT Width > 2.0 um (2 lambda)  
 613 6.1 NDIF CONTACT Width < 2.0 um (2 lambda)  
 614 6.1 PTIE CONTACT Width > 2.0 um (2 lambda)  
 615 6.1 PTIE CONTACT Width < 2.0 um (2 lambda)  
 616 6.1 NTIE CONTACT Width > 2.0 um (2 lambda)  
 617 6.1 NTIE CONTACT Width < 2.0 um (2 lambda)  
 620 6.2a PDIF Overlap of CONT < 1.5um (1.5 lambda)  
 621 6.2a NDIF Overlap of CONT < 1.5um (1.5 lambda)  
 622 6.2b PTIE Overlap of CONT < 1.5um (1.5 lambda)  
 623 6.2b NTIE Overlap of CONT < 1.5um (1.5 lambda)  
 640 6.4 PDIF CONTACT to CHANNEL Space < 2.0 um (2 lambda)  
 641 6.4 NDIF CONTACT to CHANNEL Space < 2.0 um (2 lambda)  
 642 4.1+4.2b+6.2b PTIE CONTACT to CHANNEL Space < 6.5 um (6.5 lambda)  
 643 4.1+4.2b+6.2b NTIE CONTACT to CHANNEL Space < 6.5 um (6.5 lambda)  
 710 7.1 ALU1 Width < 3.0 um (3 lambda)  
 711 7.1 ALU1 Width < 3.0 um (3 lambda)  
 720 7.2 ALU1 Notch < 3.0 um (3 lambda)  
 712 7.1 ALU0 Width < 3.0 um (3 lambda)  
 713 7.1 ALU0 Width < 3.0 um (3 lambda)  
 721 7.2 ALU0 Notch < 3.0 um (3 lambda)  
 723 7.2 ALU0 Space < 3.0 um (3 lambda)  
 724 7.2 ALU1 Space < 3.0 um (3 lambda)  
 730 7.3a ALU1 side Overlap of CONTACT < 1.0 um (1 lambda)  
 731 7.3a ALU1 side Overlap of CONTACT < 1.0 um (1 lambda)  
 732 7.3b ALU1 end Overlap of CONTACT <= 1.0 um (1 lambda)  
 733 7.3b ALU1 end Overlap of CONTACT < 1.0 um (small) (1 lambda)  
 734 7.3b ALU1 end Overlap of CONTACT < 1.0 um (big) (1 lambda)  
 735 7.3b ALU1 end Overlap of CONTACT < 1.0 um (small) (1 lambda)  
 736 7.3b ALU1 end Overlap of CONTACT < 1.0 um (big) (1 lambda)  
 750 7.5 REF Width > 3.0 um (3 lambda)  
 751 7.5 REF Width < 3.0 um (3 lambda)  
 760 7.6 REF Space < 3.0 um (3 lambda)  
 770 7.7 ALU1 must not touch or intersect REF  
 773 7.7 ALU1 Overlap of REF < 1.0 um (1 lambda)  
 774 7.7 ALU1 Overlap of REF < 1.0 um (1 lambda)  
 780 7.8 ALU1 end Overlap of REF < 1.0 um (small) (1 lambda)  
 781 7.8 ALU1 end Overlap of REF < 1.0 um (big) (1 lambda)  
 810 8.1 VIA1 Width > 3.0 um (3 lambda)  
 811 8.1 VIA1 Width < 3.0 um (3 lambda)  
 820 8.2 VIA1 Space < 3.0 um (3 lambda)  
 830 8.3a ALU1 side Overlap of VIA1 < 1.0 um (1 lambda)  
 831 8.3a ALU1 side Overlap of VIA1 < 1.0 um (1 lambda)  
 832 8.3 ALU1 must not touch or intersect VIA1  
 833 8.3b ALU1 end Overlap of VIA1 < 1.0 um (small) (1 lambda)

834 8.3b ALU1 end Overlap of VIA1 < 1.0 um (big) (1 lambda)  
 910 9.1 ALU2 Width < 3.0 um (3 lambda)  
 911 9.1 ALU2 Width < 3.0 um (3 lambda)  
 920 9.2 ALU2 Notch < 4.0 um (4 lambda)  
 921 9.2 ALU2 Space < 4.0 um (4 lambda)  
 930 9.3a ALU2 side Overlap of VIA1 < 1.0 um (1 lambda)  
 931 9.3a ALU2 side Overlap of VIA1 < 1.0 um (1 lambda)  
 932 9.3 ALU2 must not touch or intersect VIA1  
 933 9.3b ALU2 end Overlap of VIA1 < 1.0 um (small) (1 lambda)  
 934 9.3b ALU2 end Overlap of VIA1 < 1.0 um (big) (1 lambda)  
 1410 14.1 VIA2 Width > 3.0 um (3 lambda)  
 1411 14.1 VIA2 Width < 3.0 um (3 lambda)  
 1420 14.2 VIA2 Space < 4.0 um (4 lambda)  
 1430 14.3a ALU2 side Overlap of VIA2 < 1.0 um (1 lambda)  
 1431 14.3a ALU2 side Overlap of VIA2 < 1.0 um (1 lambda)  
 1432 14.3 ALU2 must not touch or intersect VIA2  
 1433 14.3b ALU2 end Overlap of VIA2 < 1.0 um (small) (1 lambda)  
 1434 14.3b ALU2 end Overlap of VIA2 < 1.0 um (big) (1 lambda)  
 1510 15.1 ALU3 Width < 3.0 um (3 lambda)  
 1511 15.1 ALU3 Width < 3.0 um (3 lambda)  
 1520 15.2 ALU3 Notch < 4.0 um (4 lambda)  
 1521 15.2 ALU3 Space < 4.0 um (4 lambda)  
 1530 15.3a ALU3 side Overlap of VIA2 < 1.0 um (1 lambda)  
 1531 15.3a ALU3 side Overlap of VIA2 < 1.0 um (1 lambda)  
 1532 15.3 ALU3 must not touch or intersect VIA2  
 1533 15.3b ALU3 end Overlap of VIA2 < 1.0 um (small) (1 lambda)  
 1534 15.3b ALU3 end Overlap of VIA2 < 1.0 um (big) (1 lambda)  
 2110 21.1 VIA3 Width > 3.0 um (3 lambda)  
 2111 21.1 VIA3 Width < 3.0 um (3 lambda)  
 2120 21.2 VIA3 Space < 4.0 um (4 lambda)  
 2130 21.3a ALU3 side Overlap of VIA3 < 1.0 um (1 lambda)  
 2131 21.3a ALU3 side Overlap of VIA3 < 1.0 um (1 lambda)  
 2132 21.3 ALU3 must not touch or intersect VIA3  
 2133 21.3b ALU3 end Overlap of VIA3 < 1.0 um (small) (1 lambda)  
 2134 21.3b ALU3 end Overlap of VIA3 < 1.0 um (big) (1 lambda)  
 2210 22.1 ALU4 Width < 3.0 um (3 lambda)  
 2211 22.1 ALU4 Width < 3.0 um (3 lambda)  
 2220 22.2 ALU4 Notch < 4.0 um (4 lambda)  
 2221 22.2 ALU4 Space < 4.0 um (4 lambda)  
 2230 22.3a ALU4 side Overlap of VIA3 < 1.0 um (1 lambda)  
 2231 22.3a ALU4 side Overlap of VIA3 < 1.0 um (1 lambda)  
 2232 22.3 ALU4 must not touch or intersect VIA3  
 2233 22.3b ALU4 end Overlap of VIA3 < 1.0 um (small) (1 lambda)  
 2234 22.3b ALU4 end Overlap of VIA3 < 1.0 um (big) (1 lambda)  
 2510 25.1 VIA4 Width > 3.0 um (3 lambda)  
 2511 25.1 VIA4 Width < 3.0 um (3 lambda)  
 2520 25.2 VIA4 Space < 4.0 um (4 lambda)  
 2530 25.3a ALU4 side Overlap of VIA4 < 1.0 um (1 lambda)  
 2531 25.3a ALU4 side Overlap of VIA4 < 1.0 um (1 lambda)  
 2532 25.3 ALU4 must not touch or intersect VIA4

2533 25.3b ALU4 end Overlap of VIA4 < 1.0 um (small) (1 lambda)  
 2534 25.3b ALU4 end Overlap of VIA4 < 1.0 um (big) (1 lambda)  
 2610 26.1 ALU5 Width < 3.0 um (3 lambda)  
 2611 26.1 ALU5 Width < 3.0 um (3 lambda)  
 2620 26.2 ALU5 Notch < 4.0 um (4 lambda)  
 2621 26.2 ALU5 Space < 4.0 um (4 lambda)  
 2630 26.3a ALU5 side Overlap of VIA4 < 1.0 um (1 lambda)  
 2631 26.3a ALU5 side Overlap of VIA4 < 1.0 um (1 lambda)  
 2632 26.3 ALU5 must not touch or intersect VIA4  
 2633 26.3b ALU5 end Overlap of VIA4 < 1.0 um (small) (1 lambda)  
 2634 26.3b ALU5 end Overlap of VIA4 < 1.0 um (big) (1 lambda)  
 2910 29.1 VIA5 Width > 4.0 um (4 lambda)  
 2911 29.1 VIA5 Width < 4.0 um (4 lambda)  
 2920 29.2 VIA5 Space < 4.0 um (4 lambda)  
 2930 29.3a ALU5 side Overlap of VIA5 < 1.0 um (1 lambda)  
 2931 29.3a ALU5 side Overlap of VIA5 < 1.0 um (1 lambda)  
 2932 29.3 ALU5 must not touch or intersect VIA5  
 2933 29.3b ALU5 end Overlap of VIA5 < 1.0 um (small) (1 lambda)  
 2934 29.3b ALU5 end Overlap of VIA5 < 1.0 um (big) (1 lambda)  
 3010 30.1 ALU6 Width < 5.0 um (5 lambda)  
 3011 30.1 ALU6 Width < 5.0 um (5 lambda)  
 3020 30.2 ALU6 Notch < 5.0 um (5 lambda)  
 3021 30.2 ALU6 Space < 5.0 um (5 lambda)  
 3030 30.3a ALU6 side Overlap of VIA5 < 2.0 um (2 lambda)  
 3031 30.3a ALU6 side Overlap of VIA5 < 2.0 um (2 lambda)  
 3032 30.3 ALU6 must not touch or intersect VIA5  
 3033 30.3b ALU6 end Overlap of VIA5 < 2.0 um (small) (2 lambda)  
 3034 30.3b ALU6 end Overlap of VIA5 < 2.0 um (big) (2 lambda)  
 5010 50.1 AB Overlap of PTIE < 4.0 um (4 lambda)  
 5011 50.1 AB Overlap of NTIE < 4.0 um (4 lambda)  
 5020 50.2 AB Overlap of PDIF < 1.5um (1.5 lambda)  
 5021 50.2 AB Overlap of NDIF < 1.5um (1.5 lambda)  
 5030 50.3 AB Overlap of POLY < 1.5um (1.5 lambda)  
 5040 50.4 AB Overlap of ALU1 < 1.5um (1.5 lambda)  
 5041 50.4 AB Overlap of ALU0 < 1.5um (1.5 lambda)  
 5050 50.5 AB Overlap of REF < 2.0 um (2 lambda)  
 END\_DRC\_COMMENT  
 END\_DRC\_RULES