SoC	Part Name	Die Area	Manufacturing Locatior	CI_fab (fab carbon intensity)	Lithography	EPA (energy per area)	Gas Abatement	GPA (gas per area)	MPA (raw mater	Yield	Num of Dies	E_soc
Unit	N/A	cm^2	N/A	g CO2 / kWh	nm	kWh / cm^2	%	g CO2 / cm^2	g CO2 / cm^2			g CO2
CPU	Intel Xeon Gold 6248	4	USA	380	14	1.2	95	200	500	0.875	1	5284.57
CPU	Intel Xeon Platinum 8260	4	USA	380	14	1.2	95	200	500	0.875	1	5284.57
GPU	Nvidia Volta V100	8.15	TSMC	583	12	1.3375	95	220	500	0.875	1	13969.22

Figure 1.1

Update:

- Filled out the table to calculate the E_soc for Intel Xeon gold 6248, Intel Xeon Platinum 8260, and Nvidia Volta V100
- Found the mechanical drawing for the Intel Xeon series: https://www.mouser.com/pdfDocs/second-gen-xeon-scalable-tmsdg-338847-rev001.pdf

Implementation Choices:

1. For the die area of the Intel Xeon Gold 6248 and Intel Xeon Platinum 8260 the mechanical drawing pdf (pg 41) labeled the die as XCC (figure 1.2)

Table 5-1. Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications

Processor Brand String	TDP (W)	Core Count	Frequency (GHz)	Die	Heatsink Form Factor	System Form Factor	C1E Offset Disable[8]	$T_{CONTROL}$ (°C)	Thermal Profiles		T_{CASE_MAX} (°C)	DTS_{MAX} (°C)	Smiling Pond Correction Factor (°C/W)	Stepping	Sample Type
									T_{CASE} (°C)	DTS (°C)					
Intel® Xeon® Platinum 8280 CPU	205	28	2.7	XCC	2U	Spread Core	0	10	[0.180*P]+47	[0.263*P]+47	84	101	0	B1	Revenue
Intel® Xeon® Platinum 8270 CPU	205	26	2.7	XCC	2U	Spread Core	0	10	[0.180*P]+47	[0.278*P]+47	84	104	0	B1	Revenue
Intel® Xeon® Platinum 8268 CPU	205	24	2.9	XCC	2U	Spread Core	0	10	[0.180*P]+47	[0.278*P]+47	84	104	0	B1	Revenue
Intel® Xeon® Gold 6254 CPU	200	18	3.1	XCC	2U	Spread Core	0	10	[0.175*P]+47	[0.285*P]+47	82	104	0.001	B1	Revenue
Intel® Xeon® Gold 6246 CPU	165	12	3.3	XCC	2U	Spread Core	0	10	[0.182*P]+46	[0.321*P]+46	76	99	0.00031	B1	Revenue

Figure 1.2

2. A quick search on: https://en.wikichip.org/wiki/intel/microarchitectures/skylake_(server) reveals that the die size is ~694 mm^2 (Figure 1.3).

Extreme Core Count (XCC) [e

- 14 nm process
- 13 metal layers
- ~694 mm² die size (estimated)
- 28 cores
- 30 tiles (5x6)

Figure 1.3

3. Found the die area and lithography for Nvidia Volta V100 here: https://en.wikipedia.org/wiki/Volta_(microarchitecture)

Model	Launch	Code Name (s)	Fab (nm)	Transistors (billion)	Die size (mm^2)	Bus Interfa
Nvidia Titan V[17]	December 7, 2017	GV100-400-A1	TSMC 12 nm	21.1	815	PCIe 3 ×16
Nvidia Quadro GV100[18]	March 27, 2018	GV100				
Nvidia Titan V CEO Edition[19][20]	June 21, 2018					

Figure 1.4

4. The lithography of the Intel Xeon Gold 6248 and the Intel Xeon Platinum 8260 come from the Intel sites directly:
    - https://ark.intel.com/content/www/us/en/ark/products/192446/intel-xeon-gold-6248-processor-27-5m-cache-2-50-ghz.html
    - https://www.intel.com/content/www/us/en/products/sku/192474/intel-xeon-platinum-8260-processor-35-75m-cache-2-40-ghz/specifications.html
5. Used the MPA from the materials.json file from Facebook ACT github:

```
(base) lipet@Peters-MacBook-Pro logic % cat materials.json
{
  "28nm" : 500  ,
  "20nm" : 500 ,
  "14nm" : 500 ,
  "10nm" : 500 ,
  "8nm"  : 500 ,
  "7nm"  : 500 ,
  "5nm"  : 500 ,
  "3nm"  : 500
}
```

6.

Figure 1.5

6. Used the gpa_95.json from the Facebook ACT github:

```
(base) lipet@Peters-MacBook-Pro logic % cat gpa_95.json
{
  "28nm" : 175,
  "20nm" : 190,
  "14nm" : 200,
  "10nm" : 240,
  "8nm"  : 240,
  "7nm"  : 350,
  "5nm"  : 430,
  "3nm"  : 470
}
```

Figure 1.6

7. And the EPA from the epa.json

```
(base) lipet@Peters-MacBook-Pro logic % cat epa.json
{
  "28nm" : 0.90,
  "20nm" : 1.200,
  "14nm" : 1.200,
  "10nm" : 1.475,
  "8nm"  : 1.520,
  "7nm"  : 2.150,
  "5nm"  : 2.750,
  "3nm"  : 3.250
}
```

Figure 1.7

8. However these json's don't have a 12nm lithography option so for the Nvidia Volta V100, I just averaged the 14nm and 10nm
9. I used the example yield of 0.875 found in the logic_model.py example provided for us

```
10 class Fab_Logic():
11     def __init__(self, process_node=14,
12                          gpa="97",
13                          carbon_intensity="loc_taiwan",
14                          debug=False,
15                          fab_yield=0.875):
16
17         self.debug = debug
18
```

Figure 1.8