PROJECT REPORT

EE 112

Assignment-16

By:

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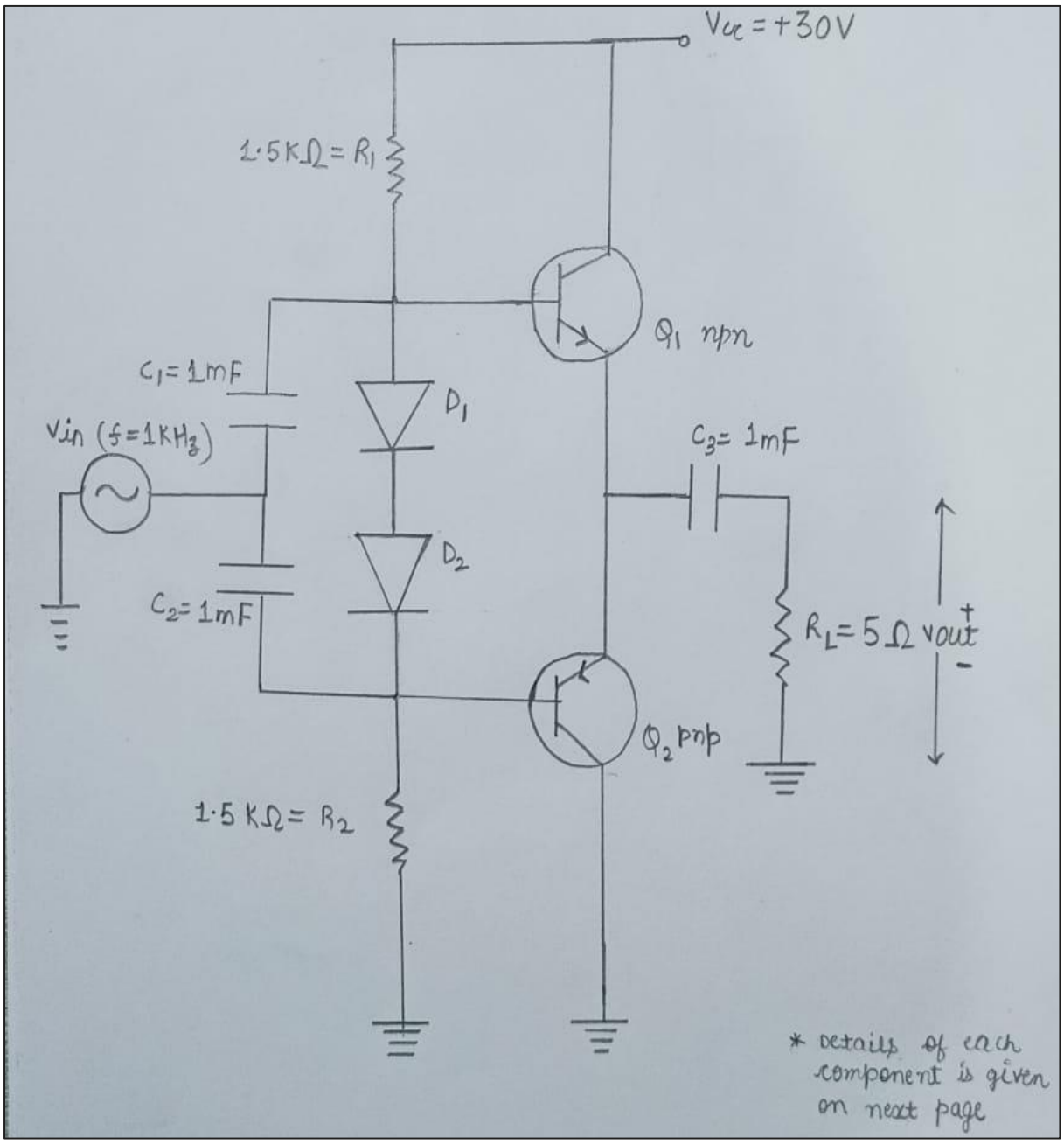
Aim: To design a push-pull amplifier with a load resistance of 5 ohms and an AC-output compliance of 15 V

Circuit Design:



Components :

1. A constant voltage source (V_{CC}) of 30V.
2. Biasing resistors R_1 and R_2 of resistance 1.5 kOhm each.
3. 3 capacitors of capacitance 1 mF each.
4. Load resistor R_L of resistance 5 ohms.
5. Complementary pair of a NPN transistor and a PNP transistor (identical I-V characteristics).
6. 2 diodes with I-V characteristics identical to that of the base emitter junction of the transistors.
7. An AC voltage source (frequency 1 kHz.)

Circuit Analysis:

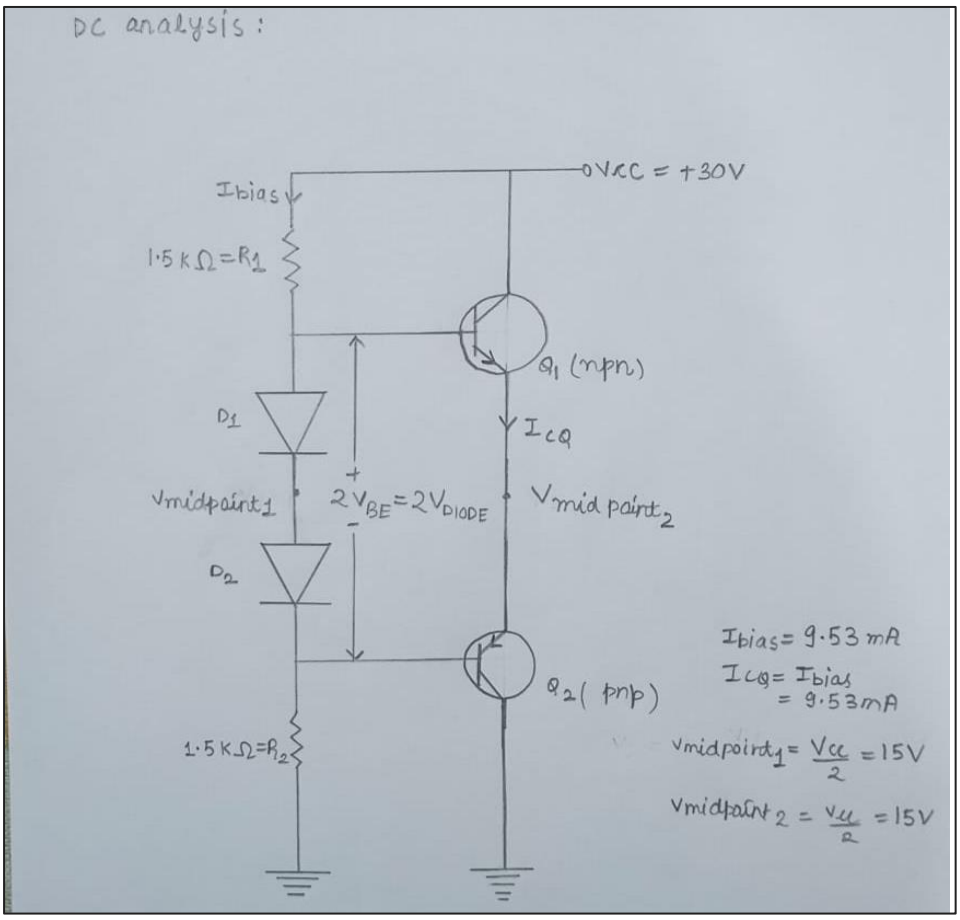
1. Input AC source is connected to the base of both the transistors. The emitters of both the transistors are connected. R_L is connected to this emitter junction.
2. Thus, we have 2 emitter follower circuits in parallel.
3. The balancing is precisely managed such that when $v_{in} = 0$, we have

    A) V_{BE} for the NPN transistor is (0.7 - ε) V, V_{BE} for the PNP transistor is (-0.7 V + ε) V and both the transistors are in **cut-off** initially. (ε is very small)
    B) Since $R_1 = R_2$, and the diodes are identical, potential at the mid-point of the biasing circuit is $V_{CC}/2 = 15$ V.
    C) Because of the symmetry of the circuit and the identical I-V characteristics of both the transistors, V_{CEQ} for the NPN transistor = $V_{CC}/2 = 15$ V.

4. When $v_{in} > 0$:
    A) V_{BE} for the NPN transistor becomes more than 0.7 V, making it forward bias, hence the NPN transistor is **active**.
    B) V_{BE} for the PNP transistor is more than -0.7 V ($|V_{BE}| < 0.7$V), hence the PNP transistor is in **cutoff**.
5. When $v_{in} < 0$:
    C) V_{BE} for the NPN transistor is less than 0.7 V, hence the NPN transistor is in **cutoff**.

D) V_{BE} for the PNP transistor becomes less than - 0.7 V ($|V_{BE}|>0.7V$), making it forward bias, hence the PNP transistor is **active**.

DC Analysis:



Applying KVL in left (biasing) line we have:

$$V_{CC} - I_{bias}R_1 - V_{diode} - V_{diode} - I_{bias}R_2 = 0$$

$$V_{CC} - I_{bias}(R_1 + R_2) - 0.7\ V - 0.7\ V = 0$$

$$I_{bias} = (30 - 1.4)V/(3\ kOhm) = 9.53\ mA$$

Since the I-V characteristics of the diodes and the BE junctions of the transistors are identical, the quiescent current $I_{CQ} = I_{bias} = 9.53$ mA.

AC Analysis

Diagram 1:

AC load line

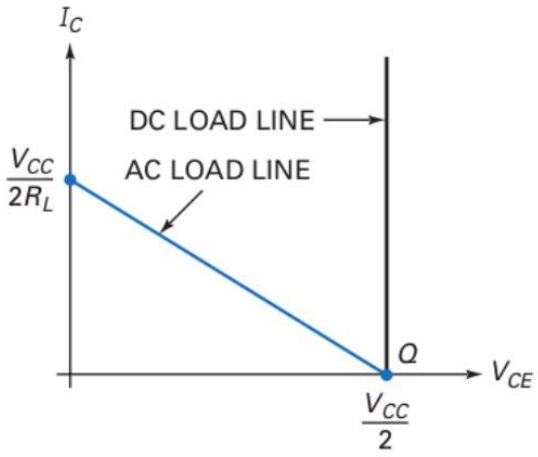
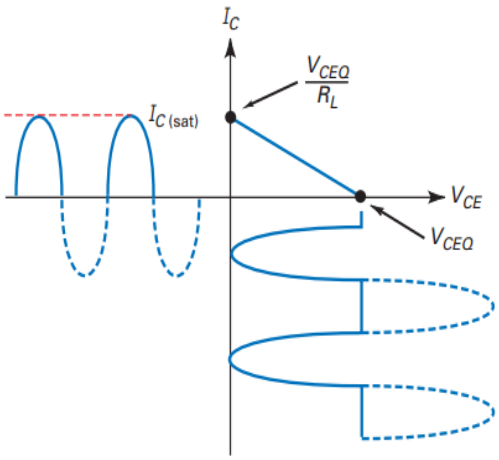


Diagram 2:

Amplitude of output voltage=V_{CE} in NPN



1. For $v_{in} > 0$, only the NPN transistor is active. Saturation current ($I_{C(sat)}$) flows through when $V_{CE} = 0$. Hence, $I_{C(sat)} = V_{CC}/2R_L = 3$ A.

2. In the circuit used, we have **AC-output compliance(v_P)=V_{CEQ}=$V_{CC}/2$ = 15 V.** This formula of AC output compliance is valid in our circuit because I_{CQ} is much smaller than $I_{C(sat)}$ i.e. Q point is close to cut-off and output voltage (=V_{CE}) can fluctuate from $V_{CC}/2$ to 0 (at saturation) as shown in diagram 2 above.

3. Using the approach given in Malvino we have,
   $I_{av} = I_{C(sat)}/\pi = 0.95$ A
   $I_{total} = 0.95$ A + $I_{CQ} = 0.96$ A
   We can neglect r'_e of the transistor since:
   $r'_e = 25\text{mV}/0.96\text{A} = 26.04$ mOhms << $R_L = 5$ ohms.
   Thus, in all our previous calculations we have neglected the presence of r'_e.

4. For Emitter follower circuits we know that,
   $A_v = R_L/(R_L + r_e') \approx 1$.
   So, since our AC output compliance is 15V we have,
   Maximum Amplitude of v_{in}= $v_P/A_v \approx$ 15V
   (where v_P is the AC output compliance)

Benefits of this Design:

1. Using diodes instead of 2 more biasing resistors allows us to avoid Thermal Runaway i.e. since the diodes follow the same I-V characteristic as the transistor BE junction thus temperature fluctuations in the transistor does not lead to significant change in transistor current since diode voltage changes accordingly.

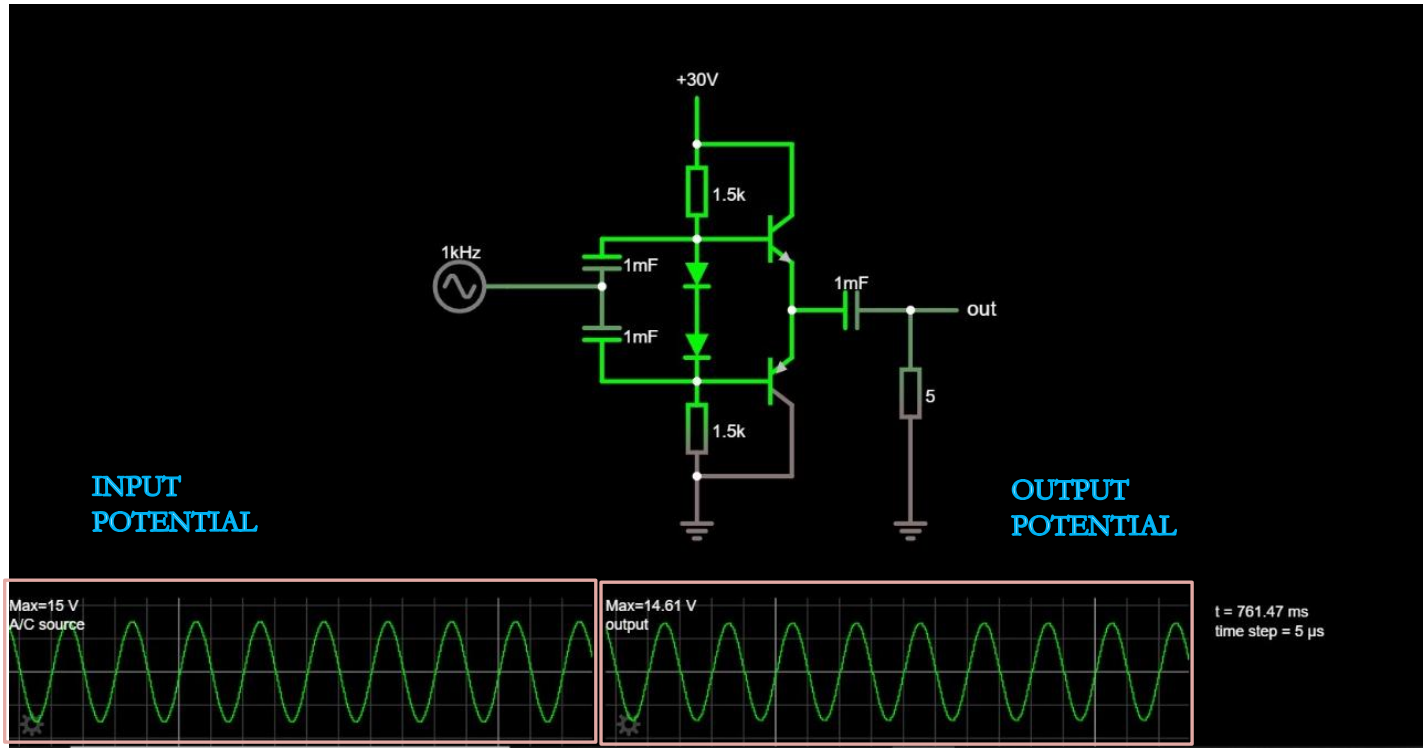
2. For our circuit, angular frequency of the AC input is w = 2 π kHz and capacitance of the capacitors is C = 1 mF. Hence wC = 2 π is large enough that capacitors are closed lines for AC and open lines for DC.

Simulations

We simulated our circuit on FALSTAD and tested it for 2 cases:

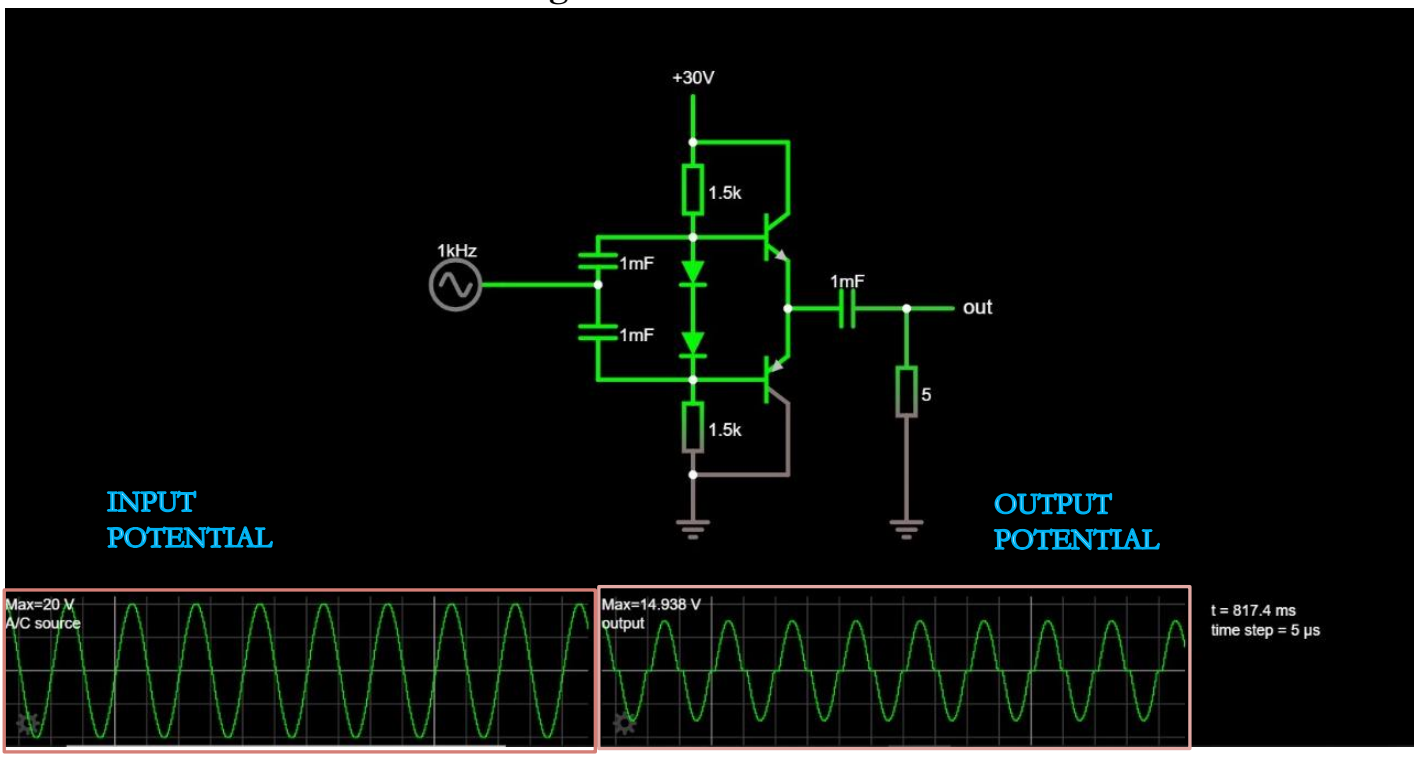
1. v_{in} = 15 V = desired AC compliance
   Result: no distortions in the output voltage, it is a sinusoid of amplitude 14.61 V. This matches the expected output.

Figure: Falstad screenshot



2. V_{in} = 20 V > desired AC compliance
   Result: output voltage never exceeds 14.9 V, the output wave is distorted.
   This signifies that the AC output compliance of the circuit is 14.9 V ≈ 15 V.

Figure:Falstad screenshot 2



Bibliography:

1. EE 112 course Class slides
2. EE 112 course Tutorials
3. Electronic principles by Albert Malvino and David Bates 8th Edition