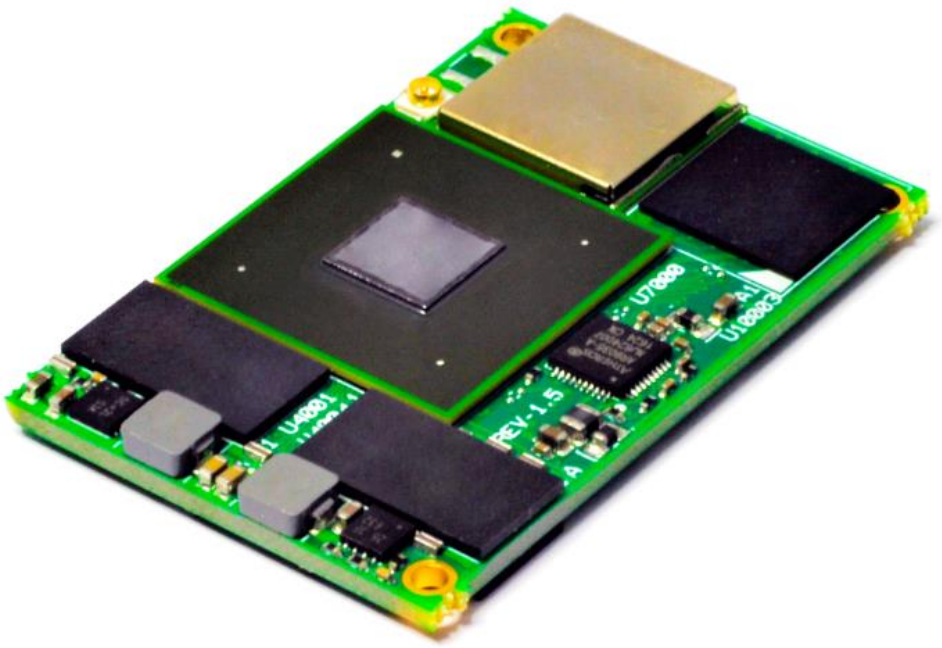
SolidRun

SR-SOM-MX6 User Manual

Freescale i.MX6™ based SOM



Revisions and Notes

Date	Owner	Revision	Notes
2014 18-June	Rabeeh Khoury	1.0	Initial release
2014 19-June	Kossay Omary	1.1	Review and slight fixes
2014 09-November	Ohad Barany	1.2	Change picture, add products description and add ordering information
2017 24-July	Rabeeh Khoury	1.3	Covers SOM rev 1.5 Documentation of booting from GPIOs

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1 CONTENTS

2 Introduction

This User Manual relates to the SolidRun SR-SOM-MX6 series, which includes

- Single core ARM A9 (1 GHz) of the i.MX6 SoC: SOM-i1 (C1000S-D512-FE)
- Dual lite core ARM A9 (1GHz) of the i.MX6 SoC: SOM-i2 (C1000DL-D1024-FE)
- Dual core ARM A9 (1GHz) of the i.MX6 SoC: SOM-i2eX (C1000DM-D1024-GE-W)
- Quad core ARM A9 (1GHz) of the i.MX6 SoC: SOM-i4 (C1000QM-D2048-GE-W)

3 Overview

The SolidRun SR-SOM-MX6 is a high performance micro system on module (S.O.M.) based on the highly integrated Freescale i.MX6 family of products.

4 Highlighted Features

- Ultra small footprint SOM (47x30mm) including three board-to-board connectors. Mating height is carrier board dependent.
- Freescale i.MX6 SoC (supports solo, dual lite, dual and quad versions)
    - Up to quad Cortex A9 and up to 1.2GHz
    - Integrated multi format decoders and encoders, de-interlacing and color conversion functions
    - Integrated OpenVG, OpenGL ES 2.0 and OpenCL 1.1 EP GPU
- DDR3 memories in x32 or x64 configurations (either 2 x16 or 4 x16 on a single chip select)
- Power management devices
- Gigabit Ethernet phy based on Qualcomm Atheros 8035 (footprint compatible with 8030 fast Ethernet phy)
- Broadcom BCM4330 based WiFi 11n and Bluetooth 4.0 (2.4GHz)

5 Supporting Products

The following products are provided from SolidRun both as production level platforms and as reference examples on how to incorporate the SOM in different levels of integration:

- HummingBoard – A board computer that incorporates the SOM retains the same Android and different Linux distributions while adding extra hardware functionalities and access to the hardware.
- CuBox-i – A minicomputer that is only 2"x2"x2" in size that runs Android and Linux with different distribution variants, use cases.

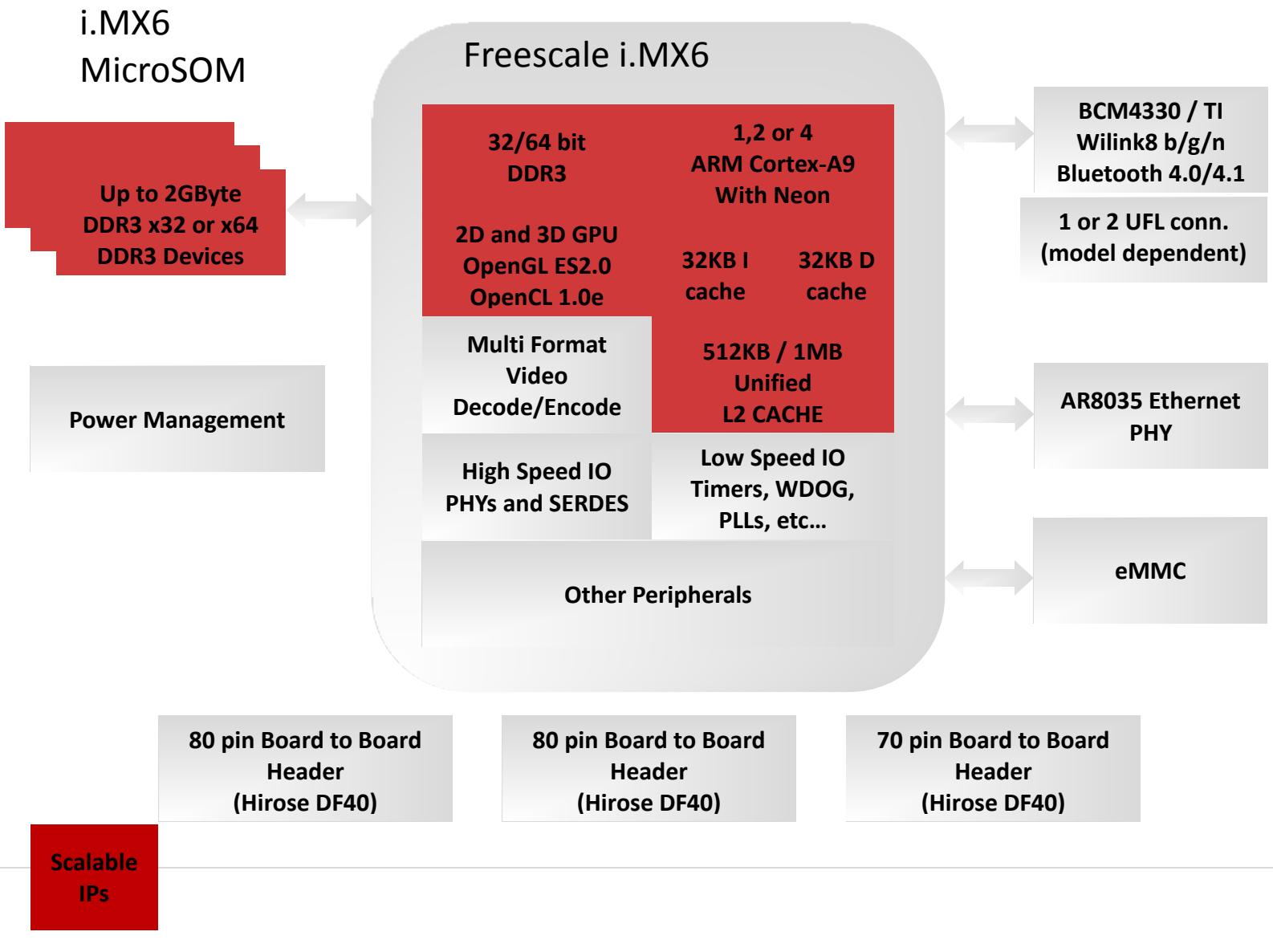
6 Summary of Features

Following is the features summary of the SOM. Notice that some of the features are pinout multiplexed (please refer to the pin muxing below and the Freescale i.MX6 data sheets):

- Freescale i.MX6 series SoC (Solo/Dual Lite/Dual/Quad ARM® Cortex™ A9 Processor, up to 1.2 GHz)
- Up to 2GByte (Special 4GByte orders are possible) DDR3 memory
- HDMI 1.4 interface
- LVDS display interface
- MIPI DSI
- MIPI CSI-2
- Parallel camera interface
- Parallel display interface
- 10/100/1000 Mbps Ethernet PHY

- SOM rev 1.3 - Wireless LAN 802.11 b/g/n and Bluetooth 4.0
- SOM rev 1.5 – SISO or dual MIMO 2.4 or 5GHz (depends on part) 802.11 b/g/n with Bluetooth 4.1
- 1 x USB 2.0 host and 1 x USB 2.0 OTG
- 3 x SD / MMC interfaces
- Serial interfaces
- CAN Bus
- Required power supplies –
    - One 3.3V to 5.0V interface (called in the doc VIN_5V0)
    - One 3.3V (called in the doc NVCC_EIM0)
    - One SNVS and VDDHIGH_IN power supply (called in the doc VSNVS_3V0) Notice how NVCC_EIM0 and VSNVS_3V0 can be combined into one in the HummingBoard design.
    - Optionally two SD interface power supplies (NVCC_SD2, NVCC_SD3) can be externally set to either 3.3v or 1.8v for UHS-1 support.

6.1 Block Diagram of the SR-SOM-MX6



7 Core System Components

7.1 i.MX6 SoC Family

The Freescale i.MX6 SoC is an implementation of the ARM CortexTM-A9 core, which operates at frequencies up to 1.2 GHz. The i.MX6 provides a variety of interfaces and supports the following main features:

- Single, dual and quad processor ARM Cortex™-A9 SMP configuration. Each processor includes:
  - 32 Kbyte L1 Instruction Cache
  - 32 Kbyte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor:
    - SIMD Media Processing Architecture
    - NEON register file with 32x64-bit general-purpose registers
    - NEON Integer execute pipeline (ALU, Shift, MAC)
    - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
    - NEON load/store and permute pipeline
- Unified L2 cache
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- Integrated Power Management unit:
  - Die temperature sensor with alarms
  - Dynamic voltage and frequency scaling for low power modes
  - Flexible clock gating control scheme
- Graphics, Multimedia & hardware acceleration engines:
  - Video Processing Unit (VPU) – A DSP with hardware acceleration engines for video decoding and encoding
  - Image Processing Unit (IPUv3) – A hardware engine for processing images, frames, de-interlacing and various other tasks
  - 3D Graphics Processing Engine (3D GPU) – OpenGL ES 2.0 and OpenCL 1.1 EP GPU engine scalable from one shader up to 4
  - 2D Graphics Processing Engine (2D GPU) – For BitBlt function etc…
  - 2D Graphics Processing Engine (OpenVG) – OpenVG compliant GPU
  - Asynchronous sample rate converters (ASRC)
- Security:
  - ARM TrustZone including the TZ architecture (interrupt and memory separation)
  - CAAM module – cipher acceleration and assurance module including a true pseudo random number generator (NIST certified)
  - Secure boot (HAB) and central security unit controlled via OTP fuses
- I/O:
  - High Speed USB 2.0 OTG (Up to 480 Mbps) with integrated HS USB Phy
  - High Speed USB 2.0 HOST (Up to 480Mbps) with integrated USB phy
  - Single lane PCI-Express 2.0 (includes clock generation)
  - Misc. SD and MMC interface with 3.3v / 1.8v voltage level support (for UHS-1 speeds)
  - Misc. serial interfaces (SPI, NOR, I2S, I2C, CAN etc…)

Please refer to Freescale i.MX6 datasheets with regards to differences between the various devices, number of processors, L2 cache size, GPU supported (i.e. gc880 vs gc2000), etc…

8 10/100/1000 Mbps Ethernet PHY

The Ethernet PHY is based on the Qualcomm / Atheros AR8035 phy and incorporates the following features:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- IEEE 802.3az EEE
- Green ETHOS power saving modes with internal automatic DSP power-saving scheme
- SmartEEE
- Wake on LAN
- Automatic MDI/MDIX crossover and polarity correction
- IEEE 802.3u compliant auto negotiation
- Cable Diagnostic Test (CDT)

The phy is connected via the i.MX6 RGMII interface.

9 BCM 4330 based (SOM rev 1.3) - Wireless LAN 802.11 b/g/n and Bluetooth 4.0 SiP

The system in package (SiP) is based on the AzureWave AW-NH660 module and incorporates the following features:

- BCM4330 WiFi / BT based
- WiFi / BT co-existence support
- WiFi :
    - Integrated CPU with on-chip memory for complete WLAN subsystem minimizing the need to wake up the application processor
    - SDIO based interface (connected via the i.MX6 SD1 interface)
    - Single band 2.4 GHz 802.11 b/g/n
    - Supports IEEE 802.11d, e, j, I, j, r, k, w
    - WEP, WPA/WPA2, AES, TKIP, CKIP (SW) based security
    - WMM/WMM-PS/WMM-SA
    - Proprietary protocols – CCXv2/CCXv3/CCXv4/CCXv5, WFAEC
- Bluetooth:
    - Fully supports Bluetooth 4.0 + EDR (AFH, QoS, eSCO, fast connect, SSP, SSR, EPR, EIR, LST)
    - High speed UART (max 4Mbps) and PCM for Bluetooth support (connected via i.MX6 UART4 interface and i.MX6 AUD3 audio PCM interface)
    - HS packet types, class 1 or class 2 transmitter type operation

10TI WILINK 8 BASED (SOM REV 1.5) - WIRELESS LAN 802.11 B/G/N & BLUETOOTH 4.1 SIP

The SiP (System in package) incorporates the following features –

- TI Wilink 8 WiFi / BT based
- WiFi / BT co-existence support
- WiFi :
    - Integrated RF front end, power amplified, DC-DC, crystal, switches, filters and power management
    - SDIO based interface (connected via the i.MX6 SD1 interface)
    - 2.4 GHz or 5 GHz (depending on model) 802.11 a/b/g/n
    - SISO or MIMO (two antennas)
    - 20 and 40 MHz channels on 2.4/5 GHz bands
    - Wi-Fi direct multi-role multi-channel
    - Up to 10 clients supported in AP role
- Bluetooth:
    - Fully supports Bluetooth 4.0 + EDR including Bluetooth low energy
    - High speed UART (max 4Mbps) and PCM for Bluetooth support (connected via i.MX6 UART4 interface

11 SR-SOM-MX6 INTERFACES

11.1 SR-SOM-MX6 EXTERNAL INTERFACES

The SOM incorporates three Hirose DF40 board-to-board headers.

The selection of the Hirose DF40 is due to the following criteria:

- Miniature (0.4m pitch)
- Highly reliable manufacturer
- Availability (worldwide distribution channels)
- Excellent signal integrity (supports 6Gbps)
    - Please contact Hirose or SolidRun for reliability and test result data.
- Mating height of between 1.5mm to 4.0mm (1.5mm to 3.0mm if using 70-pin Board-to-Board header). SR-SOM-MX6 headers are fixed, the final mating height is determined by carrier implementation

The different board-to-board functionality is defined as follows:

- Main 80pin B2B. Includes the following functionality:
    - Main supply +3.3v to +5.0v in (5 pins)
    - I/O supply +3.3V and SD2, SD3 supplies (can be fixed +3.3V or externally switched +3.3V / 1.8V to support UHS-1)
    - Ethernet MDI (4 differential pairs), LED activity or link (10/100/1000) and Ethernet TCT
    - SATA TX/RX (2 differential pairs)
    - USB OTG and HOST (2 differential pairs)
    - Various GPIOs and pins that can be muxed. By default, it is configured to be 2xI2C, PWMs (1 through 4), SPI 2, SD2 interface and USB enable.
- Second 80pin B2B. The board-to-board exposes the following functionality:
    - System power on reset
    - HDMI 1.4 (4 differential pairs), CEC, +5V boosted I2C and HDMI HPD
    - PCI express 2.0 (3 differential pairs include TX/RX and clock)
    - USB OTG charge detect and USB OTG ID
    - MIPI CSI 2 (3 differential pairs for solo / dual lite and 5 differential pairs for dual / quad versions)
    - MIPI DSI (3 differential pairs)
    - LVDS 0 (5 differential pairs)
    - UART1 (typically used for main system debug port)
    - Various GPIOs and pins that can be muxed. By default, it is configured to be AUD5 I2S interface, CCM CLKO1/CLKO2, SD2 voltage select, SPDIF out, USB HOST / OTG over current indication.
- Third 70pin B2B. This board-to-board exposes the following functionality:
    - Power management (EIM_WAIT, TAMPER, PMIC standby, MX6_ONOFF, PMIC_ON_REQ)
    - Boot mode override
    - MLB interface (marked as reserved. Contact SolidRun about availability of i.MX6 SOM with MLB interface)
    - Various GPIOs and pins that can be muxed. By default it is configured to be UART3, SPDIF in, Display and camera parallel interface, UART2, Watchdog timer, SD3 and SD4 interfaces)

11.2 SR-SOM-MX6 On Board Functions

11.2.1 10/100/1000 Mbps PHY

The SOM incorporates a Qualcomm / Atheros AR8035 PHY. The phy connectivity is as follows:

- Uses 2.5V interface voltage level
- RGMII (optional AR8030 with RMII)
- Phy reset function via i.MX6 pad V5 (KEY_ROW4). Active low
- Default phy address either 0x0 or 0x4 (depends on LED activity reset strap, either pulled down or pulled up)

* Note that due to internal i.MX6 buses the 1000Mbps interface speed is limited to 470Mbps.

11.2.2 802.11 b/g/n and Bluetooth SiP

The SOM incorporates AzureWave AW-660 SiP or TI Wilink8 SiP. The SiP interfaces are:

1. WiFi connectivity via i.MX6 SDIO1
2. Bluetooth connectivity via i.MX6 UART4
3. Audio PCM connectivity via i.MX6 AUD3
4. Antenna via onboard UFL connector

12 SR-SOM-MX6 External Interfaces Detailed Description

As previously described, the SOM incorporates three Hirose DF40 based board-to-board headers.

The SOM uses the header of these board-to-board connectors which is fixed in height, while the mating height is determined by the carrier, by using different Hirose DF40 receptacle mating heights (1.5 to 4.0mm) (1.5mm to 3.0mm if using 70-pin Board-to-Board header).

Following is a color legend to be used for the description of the board-to-board connectors:

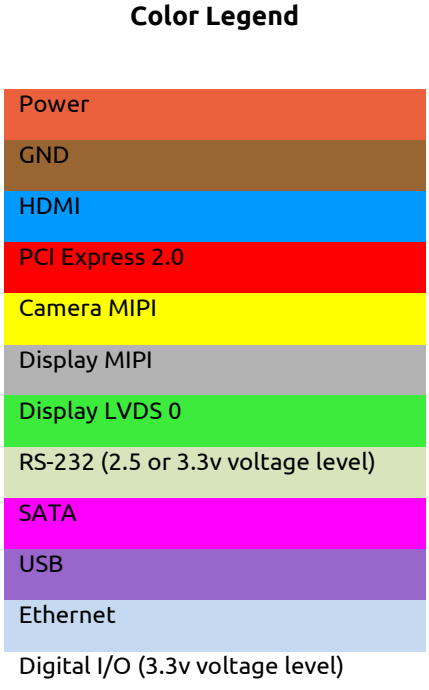


Figure 1 Board-to-Board color legend

12.1 Main Board-to-Board Header pin description

This board-to-board header uses Hirose DF40 DH40C-80DP-0.4V(51) header. The pin description may be found in the following tables:

Notes	IC ball #	IC pad name	Driving IC	Schematics pad	Pin #	Pin #	Schematics pad	Driving IC	IC pad name	IC ball #	Notes
				GND	2	1	MDI_TRXN3	Ethernet PHY	MDI_TRXN3	19	Diff 100 Ω
Diff 100 Ω	B14	SATA_RXP	i.MX6	SATA_RXP	4	3	MDI_TRXP3	Ethernet PHY	MDI_TRXP3	18	Diff 100 Ω
Diff 100 Ω	A14	SATA_RXM	i.MX6	SATA_RXN	6	5	GND				
				GND	8	7	MDI_TRXN2	Ethernet PHY	MDI_TRXN2	16	Diff 100 Ω
Diff 100 Ω	B12	SATA_TXM	i.MX6	SATA_TXN	10	9	MDI_TRXP2	Ethernet PHY	MDI_TRXP2	15	Diff 100 Ω
Diff 100 Ω	A12	SATA_TXP	i.MX6	SATA_TXP	12	11	GND				
				GND	14	13	MDI_TRXN1	Ethernet PHY	MDI_TRXN1	13	Diff 100 Ω
Diff 90 Ω	A6	USB_OTG_DP	i.MX6	USB_OTG_DP	16	15	MDI_TRXP1	Ethernet PHY	MDI_TRXP1	12	Diff 100 Ω
Diff 90 Ω	B6	USB_OTG_DN	i.MX6	USB_OTG_DN	18	17	GND				
				GND	20	19	MDI_TRXN0	Ethernet PHY	MDI_TRXN0	10	Diff 100 Ω
Diff 90 Ω	E10	USB_H1_DP	i.MX6	USB_HOST_DP	22	21	MDI_TRXP0	Ethernet PHY	MDI_TRXP0	9	Diff 100 Ω
Diff 90 Ω	F10	USB_H1_DN	i.MX6	USB_HOST_DN	24	23	GND				
				GND	26	25	LED_10_100_1000	Ethernet PHY	LED_10_100_1000	22	
	T5	GPIO_0	i.MX6	USB_H1_PWR_EN	28	27	LED_ACT	Ethernet PHY	LED_ACT	21	
	E23	EIM_D22	i.MX6	USB_OTG_PWR_EN	30	29	ETH_TCT	Ethernet PHY	ETH_TCT	N/A	
BOOT_CFG4[5]	K20	EIM_RW	i.MX6	ECSPI2_SS0	32	31	I2C3_SCL	i.MX6	EIM_D17	F21	4.7kohm NVCC_EIM0 pulled up
BOOT_CFG4[2]	K22	EIM_LBA	i.MX6	ECSPI2_SS1	34	33	I2C3_SDA	i.MX6	EIM_D18	D24	4.7kohm NVCC_EIM0 pulled up

				GND	36	35	GND				
	C21	SD2_CLK	i.MX6	SD2_CLK	38	37	SD3_CLK	i.MX6	SD3_CLK	D14	
	F19	SD2_CMD	i.MX6	SD2_CMD	40	39	SD3_CMD	i.MX6	SD3_CMD	B13	
	A22	SD2_DATA0	i.MX6	SD2_DATA0	42	41	PWM2_OUT	i.MX6	DISP0_DAT9	T25	
	E20	SD2_DATA1	i.MX6	SD2_DATA1	44	43	USB_OTG_VBUS	i.MX6	USB_OTG_VBUS	E9	
	A23	SD2_DATA2	i.MX6	SD2_DATA2	46	45	ECSPI2_MISO	i.MX6	EIM_OE	J24	
	B22	SD2_DATA3	i.MX6	SD2_DATA3	48	47	ECSPI2_MOSI	i.MX6	EIM_CS1	J23	
	R6	GPIO_4	i.MX6	SD2_CD_B	50	49	ECSPI2_SCLK	i.MX6	EIM_CS0	H24	
	D10	USB_H1_VBUS	i.MX6	USB_H1_VBUS	52	51	I2C1_SDA	i.MX6	EIM_D28	G23	4.7kohm NVCC_EIM0 pulled up
BOOT_CFG1[6]	K25	EIM_DA6	i.MX6	DISP1_DATA03	54	53	I2C1_SCL	i.MX6	EIM_D21	H20	4.7kohm NVCC_EIM0 pulled up
BOOT_CFG1[7]	L25	EIM_DA7	i.MX6	DISP1_DATA02	56	55	PWM3_OUT	i.MX6	SD4_DAT1	B19	
BOOT_CFG1[3]	K24	EIM_DA3	i.MX6	DISP1_DATA06	58	57	PWM4_OUT	i.MX6	SD4_DAT2	F17	
BOOT_CFG2[0]	L24	EIM_DA8	i.MX6	DISP1_DATA01	60	59	__NC__SPDIF_CLK_IN	NC			
BOOT_CFG1[4]	L22	EIM_DA4	i.MX6	DISP1_DATA05	62	61	NVCC_SD2	i.MX6	NVCC_SD2	G17	
BOOT_CFG1[5]	L23	EIM_DA5	i.MX6	DISP1_DATA04	64	63	NVCC_SD3	i.MX6	NVCC_SD3	G14	
BOOT_CFG2[1]	M21	EIM_DA9	i.MX6	DISP1_DATA00	66	65	NVCC_EIM0				Although called NVCC_EIM0, this power rail supplies the i.MX6, Ethernet phy, WiFi / BT and others. Refer to the public schematics for more details.
	R22	DISP0_DAT8	i.MX6	PWM1_OUT	68	67	NVCC_EIM0	Many			
				GND	70	69	VSNVS_3V0	i.MX6	Rev 1.1 – VDD_SNVS_IN Rev 1.2 and beyond - VDD_SNVS_IN and	Rev 1.1 – G11 Rev 1.2 -G11, H9 and	In rev 1.2 and beyond this is VDD_SNVS_IN and VDDHIGH_IN power domains

								VDDHIGH_IN	J9	
				GND	72	71	VIN_5V0			
				GND	74	73	VIN_5V0			Supply for –
				GND	76	75	VIN_5V0			Power management.
				GND	78	77	VIN_5V0			WiFi / BT VBAT
				GND	80	79	VIN_5V0			I2C Boost

Figure 2 12.1 MAIN BOARD-TO-BOARD HEADER PIN DESCRIPTION

12.2 Second Board-to-Board Header pin description

This board-to-board header uses Hirose DF40 DH40C-80DP-0.4V(51) header. The pin description is described below:

Notes	IC ball #	IC pad name	Driving IC	Schematics pad	Pin #	Pin #	Schematics pad	Driving IC	IC pad name	IC ball #	Notes
Diff 85 Ω	B1	PCIE_RXM	i.MX6	PCIE_RXM	2	1	CLK1_P	i.MX6	CLK1_P	D7	Diff 85 Ω
Diff 85 Ω	B2	PCIE_RXP	i.MX6	PCIE_RXP	4	3	CLK1_N	i.MX6	CLK1_N	C7	Diff 85 Ω
				GND	6	5	GND				
Diff 100 Ω	E4	CSI_D0M	i.MX6	CSI_D0M	8	7	PCIE_TXM	i.MX6	PCIE_TXM	A3	Diff 85 Ω
Diff 100 Ω	E3	CSI_D0P	i.MX6	CSI_D0P	10	9	PCIE_TXP	i.MX6	PCIE_TXP	B3	Diff 85 Ω
				GND	12	11	GND				
Diff 100 Ω	D1	CSI_D1M	i.MX6	CSI_D1M	14	13	CSI_CLK0P	i.MX6	CSI_CLK0M	F3	Diff 100 Ω
Diff 100 Ω	D2	CSI_D1P	i.MX6	CSI_D1P	16	15	CSI_CLK0M	i.MX6	CSI_CLK0P	F4	Diff 100 Ω
				GND	18	17	GND				
Diff 100 Ω	E1	CSI_D2M	i.MX6	CSI_D2M	20	19	HDMI_D2P	i.MX6	HDMI_D2P	K4	Diff 100 Ω
Diff 100 Ω	E2	CSI_D2P	i.MX6	CSI_D2P	22	21	HDMI_D2M	i.MX6	HDMI_D2M	K3	Diff 100 Ω
				GND	24	23	GND		GND		
Diff 100 Ω	F2	CSI_D3M	i.MX6	CSI_D3M	26	25	HDMI_D1P	i.MX6	HDMI_D1P	J4	Diff 100 Ω
Diff 100 Ω	F1	CSI_D3P	i.MX6	CSI_D3P	28	27	HDMI_D1M	i.MX6	HDMI_D1M	J3	Diff 100 Ω
				GND	30	29	GND		GND		
Diff 100 Ω	H2	DSI_D1M	i.MX6	DSI_D1M	32	31	HDMI_D0P	i.MX6	HDMI_D0P	K6	Diff 100 Ω
Diff 100 Ω	H1	DSI_D1P	i.MX6	DSI_D1P	34	33	HDMI_D0M	i.MX6	HDMI_D0M	K5	Diff 100 Ω
				GND	36	35	GND		GND		

Diff 100 Ω	G2	DSI_D0M	i.MX6	DSI_D0M	38	37	HDMI_CLKP	i.MX6	HDMI_CLKP	J6	Diff 100 Ω
Diff 100 Ω	G1	DSI_D0P	i.MX6	DSI_D0P	40	39	HDMI_CLKM	i.MX6	HDMI_CLKM	J5	Diff 100 Ω
				GND	42	41	GND				
Diff 100 Ω	H3	DSI_CLK0M	i.MX6	DSI_CLK0M	44	43	HDMI_TX_CEC_LINE	i.MX6	KEY_ROW2	W4	
Diff 100 Ω	H4	DSI_CLK0P	i.MX6	DSI_CLK0P	46	45	HDMI_TX_DDC_SCL	i.MX6	KEY_COL3	U5	Boosted to 5V and 4.7kohm pulled up
				GND	48	47	HDMI_TX_DDC_SDA	i.MX6	KEY_ROW3	T7	
	R1	GPIO_17	i.MX6	SPDIF_OUT	50	49	HDMI_HPD	i.MX6	HDMI_HPD	K1	Level shifted to 3.3v
	M1	CSI0_DAT10	i.MX6	UART1_TX_DATA	52	51	AUD5_TXC	i.MX6	KEY_COL0	W5	
	M3	CSI0_DAT11	i.MX6	UART1_RX_DATA	54	53	AUD5_TXD	i.MX6	KEY_ROW0	V6	
	T4	GPIO_1	i.MX6	USB_OTG_ID	56	55	AUD5_TXFS	i.MX6	KEY_COL1	U7	
				GND	58	57	AUD5_RXD	i.MX6	DISP0_DAT19	U23	
Diff 100 Ω	U2	LVDS0_TX0_N	i.MX6	LVDS0_TX0_N	60	59	CCM_CLKO1	i.MX6	GPIO_5	R4	
Diff 100 Ω	U1	LVDS0_TX0_P	i.MX6	LVDS0_TX0_P	62	61	GND				
				GND	64	63	CCM_CLKO2	i.MX6	NANDF_CS2	A17	
Diff 100 Ω	U4	LVDS0_TX1_N	i.MX6	LVDS0_TX1_N	66	65	POR_B	i.MX6	POR_B	C11	Rev 1.5 adds 100nF capacitance on this signal
Diff 100 Ω	U3	LVDS0_TX1_P	i.MX6	LVDS0_TX1_P	68	67	USB_OTG_OC	i.MX6	KEY_COL4	T6	
				GND	70	69	USB_H!_OC	i.MX6	GPIO_3	R7	
Diff 100 Ω	V2	LVDS0_TX2_N	i.MX6	LVDS0_TX2_N	72	71	USB_OTG_CHD_B	i.MX6	USB_OTG_CHD_B	B8	
Diff 100 Ω	V1	LVDS0_TX2_P	i.MX6	LVDS0_TX2_P	74	73	SD2_VSELECT	i.MX6	KEY_ROW1	U6	
				GND	76	75	GND				
Diff 100 Ω	V4	LVDS0_CLK_N	i.MX6	LVDS0_CLK_N	78	77	LVDS0_TX3_P	i.MX6	LVDS0_TX3_P	W1	Diff 100 Ω

Diff 100 Ω	V3	LVDS0_CLK_P	i.MX6	LVDS0_CLK_P	80	79	LVDS0_TX3_N	i.MX6	LVDS0_TX3_N	W2	Diff 100 Ω

Figure 3 12.2 SECOND BOARD-TO-BOARD HEADER PIN DESCRIPTION

12.3 Third Board-to-Board Header pin description

Rev 1.5 - Pins marked with rev 1.5 are previously NC or reserved and are added in SOM version 1.5

Notes	IC ball #	IC pad name	Driving IC	Schematics pad	Pin #	Pin #	Schematics pad	Driving IC	IC pad name	IC ball #	Notes
	F13	SD3_DAT7	i.MX6	SD3_DATA7	2	1	EIM_WAIT	i.MX6	EIM_WAIT	M25	BOOT_CFG4[1]
	E13	SD3_DAT6	i.MX6	SD3_DATA6	4	3	BOOT_MODE0	i.MX6	BOOT_MODE0	C12	
	C13	SD3_DAT5	i.MX6	SD3_DATA5	6	5	BOOT_MODE1	i.MX6	BOOT_MODE1	F12	
	D13	SD3_DAT4	i.MX6	SD3_DATA4	8	7	TAMPER	i.MX6	TAMPER	E11	
				GND	10	9	PMIC_STBY_REQ	i.MX6	PMIC_STBY_REQ	F11	
Rev 1.5	W6	KEY_COL2	i.MX6	FLEXCAN1_TX (1.5)	12	11	GPIO3_IO19	i.MX6	EIM_D19	G21	Rev 1.5
Rev 1.5	R3	GPIO_7	i.MX6	GPIO7 (1.5)	14	13	MX6_ONOFF	i.MX6	ONOFF	D12	
				GND	16	15	PMIC_ON_REQ	i.MX6	PMIC_ON_REQ	D11	
	B15	SD3_DAT3	i.MX6	SD3_DATA3	18	17	EIM_A25	i.MX6	EIM_A25	H19	Rev 1.5
	A15	SD3_DAT2	i.MX6	SD3_DATA2	20	19	EIM_D16	i.MX6	EIM_D16	C25	Rev 1.5
	F14	SD3_DAT1	i.MX6	SD3_DATA1	22	21	EIM_BCLK	i.MX6	EIM_BCLK	N22	Rev 1.5
	E14	SD3_DAT0	i.MX6	SD3_DATA0	24	23	EIM_D20	i.MX6	EIM_D20	G20	Rev 1.5
	D15	SD3_RST	i.MX6	SD3_RST	26	25	EIM_D23	i.MX6	EIM_D23	D25	Rev 1.5
	P6	GPIO_18	i.MX6	SD3_VSELECT	28	27	EIM_D29	i.MX6	EIM_D29	J19	Rev 1.5
				GND	30	29	UART3_TX_DATA	i.MX6	EIM_D24	F22	
	E16	SD4_CLK	i.MX6	SD4_CLK	32	31	UART3_RX_DATA	i.MX6	EIM_D25	G22	
	B17	SD4_CMD	i.MX6	SD4_CMD	34	33	GND				
	D18	SD4_DAT0	i.MX6	SD4_DATA0	36	35	SPDIF_IN	i.MX6	ENET_RX_ER	W23	

	A20	SD4_DAT3	i.MX6	SD4_DATA3	38	37	EIM_EB2	i.MX6	EIM_EB2	E22	Rev 1.5 BOOT_CFG4[6]
	J20	EIM_D30	i.MX6	DISP1_DATA21	40	39	EIM_EB3	i.MX6	EIM_EB3	F23	Rev 1.5 BOOT_CFG4[7]
	H21	EIM_D31	i.MX6	WDOG1_B	42	41	DI1_PIN02	i.MX6	EIM_DA11	M20	BOOT_CFG2[3]
	E18	SD4_DAT4	i.MX6	UART2_RX_DATA	44	43	DI1_PIN15	i.MX6	EIM_DA10	M22	BOOT_CFG2[2]
	D19	SD4_DAT7	i.MX6	UART2_TX_DATA	46	45	DI1_D0_CS	i.MX6	EIM_DA13	M23	BOOT_CFG2[5]
	B20	SD4_DAT6	i.MX6	UART2_CTS_B	48	47	GND				
	C19	SD4_DAT5	i.MX6	UART2_RTS_B	50	49	DI1_D1_CS	i.MX6	EIM_DA14	N23	BOOT_CFG2[6]
				GND	52	51	DI1_PIN03	i.MX6	EIM_DA12	M24	BOOT_CFG2[4]
BOOT_CFG3[0]	H25	EIM_A16	i.MX6	DI1_DISP_CLK	54	53	DI1_PIN01	i.MX6	EIM_DA15	N24	BOOT_CFG2[7]
BOOT_CFG3[7]	J21	EIM_A23	i.MX6	DISP1_DATA18	56	55	DISP1_DATA08	i.MX6	EIM_DA1	J25	BOOT_CFG1[1]
	H21	EIM_D31	i.MX6	DISP1_DATA20	58	57	DISP1_DATA10	i.MX6	EIM_EB1	K23	BOOT_CFG4[4]
BOOT_CFG1[0]	L20	EIM_DA0	i.MX6	DISP1_DATA09	60	59	DISP1_DATA12	i.MX6	EIM_A17	G24	BOOT_CFG3[1]
BOOT_CFG3[4]	H22	EIM_A20	i.MX6	DISP1_DATA15	62	61	DISP1_DATA22	i.MX6	EIM_D26	E24	
BOOT_CFG3[2]	J22	EIM_A18	i.MX6	DISP1_DATA13	64	63	DISP1_DATA14	i.MX6	EIM_A19	G25	BOOT_CFG3[3]
BOOT_CFG3[5]	H23	EIM_A21	i.MX6	DISP1_DATA16	66	65	DISP1_DATA23	i.MX6	EIM_D27	E25	
BOOT_CFG4[3]	K21	EIM_EB0	i.MX6	DISP1_DATA11	68	67	DISP1_DATA19	i.MX6	EIM_A24	F25	BOOT_CFG4[0]
BOOT_CFG1[2]	L21	EIM_DA2	i.MX6	DISP1_DATA07	70	69	DISP1_DATA17	i.MX6	EIM_A22	F24	BOOT_CFG3[6]

Figure 4 12.3 THIRD BOARD-TO-BOARD HEADER PIN DESCRIPTION

13 SR-SOM-MX6 INTEGRATION MANUAL

13.1 SR-SOM-MX6 POWER UP SEQUENCE

Integration with the SR-SOM-MX6 is easy, power sequencing wise. Note the following requirements:

- The SOM internal power management contains a soft-start clamp that gradually raises its internally generated power supplies once VIN_5V0 is applied. The soft-start timing is set to be 800us (typ.). SNVS_3V0 must be applied well ahead of the internal power rails. We recommend that SNVS_3V0 be applied no later than 200uS after VIN_5V0.
- SNVS_3V0 must be applied before NVCC_EIM0, NVCC_SD2 and NVCC_SD3. Alternatively, SNVS_3V0 can be shorted with those power supplies as long as they do not exceed 3.3v (absolute maximum including overvoltage ripples).
  Notice the HummingBoard design, where there is a single 3.2V power rail generated from the 5V DC IN (either via LDO or external DC-DC), and that rail is directly applied to VSNVS_3V0, NVCC_EIM0 together with the VIN_5V0.
- Notice that a cost saving practice when integrating SR-SOM-MX6 is to have a single DC-DC of output voltage 3.2v, and -+100mV ripple that supplies all the SR-SOM-MX6 supplies, except the USB_OTG_VBUS and USB_HOST_VBUS which are 5V when used.

13.2 SR-SOM-MX6 GPIO (INTERNAL) BOOT SOURCE CONFIGURATION

i.MX6 is very flexible when it comes to selecting the boot source. This section describes how to set pull up /down on the carrier board in order to perform boot indicated by GPIOs pins.

Blowing the device's eFuses is alternative to using GPIOs in order to set boot source. This topic is widely covered on the SolidRun wiki pages.

If the boot method is set, via eFuses (irreversible operation) then boot select via GPIO pull up/down will be void and ONLY the eFusing configuration regulates the boot device.

The section below assumes that the SOM's boot eFuses are not set, it also assumes that the boot mode is set to BOOT_MODE[1:0] = 0b10, indicating boot from GPIOs.

The following are the general instructions on how to perform boot from different common sources, the guideline in general is the following –

1. BOOT_CFGx[7:0] is pulled down in reset and then reverts to pull up.
2. The user should pull up the required pins, but making sure that all pins in the bus are either floating, tri-stated in reset (POR_B) or pulled down.

Since the above forces the user to pull up/down the entire bus, below are more pervasive examples of 3 different boot sources used as in HummingBoard Edge:

- SDHC2 SD
- SDHC3 eMMC
- SATA

13.3 SR-SOM-MX6 BOOT FROM SDHC2 EXTERNAL SD CARD (AS IN HUMMINGBOARD EDGE/GATE) –

The following is an example of booting from SD card through schematics signals SD2_*:

The following must be pulled up (10 kohm or lower):

BOOT CFG name	i.MX6 pad name	Schematics pad name
BOOT_CFG1[6]	EIM_DA6	DISP1_DATA03
BOOT_CFG2[3]	EIM_DA11	DI1_PIN02

SolidRun tested pulling down the signals as described below, but the user can experiment with the signals that are not marked with 'Must be 0'; but SolidRun does not test those signals behavior.

BOOT CFG name	i.MX6 pad name	Schematics pad name	Notes
BOOT_CFG1[0]	EIM_DA0	DISP1_DATA09	Can be either 0 or 1
BOOT_CFG1[1]	EIM_DA1	DISP1_DATA08	If 1 power cycles the external device
BOOT_CFG1[2]	EIM_DA2	DISP1_DATA07	Can be either 0 or 1
BOOT_CFG1[3]	EIM_DA3	DISP1_DATA06	Must be 0
BOOT_CFG1[4]	EIM_DA4	DISP1_DATA05	Must be 0
BOOT_CFG1[5]	EIM_DA5	DISP1_DATA04	Must be 0
BOOT_CFG1[7]	EIM_DA7	DISP1_DATA02	Must be 0
BOOT_CFG2[0]	EIM_DA8	DISP1_DATA01	Must be 0
BOOT_CFG2[1]	EIM_DA9	DISP1_DATA00	Must be 0
BOOT_CFG2[2]	EIM_DA10	DI1_PIN15	Must be 0
BOOT_CFG2[4]	EIM_DA12	DI1_PIN03	Must be 0
BOOT_CFG2[5]	EIM_DA13	DI1_D0_CS	Can be 1 in case of 4 bit SD
BOOT_CFG2[6]	EIM_DA14	DI1_D1_CS	Must be 0
BOOT_CFG2[7]	EIM_DA15	DI1_PIN01	Must be 0
BOOT_CFG3[6]	EIM_A22	DISP1_DATA17	Must be 0
BOOT_CFG3[7]	EIM_A23	DISP1_DATA18	Must be 0
BOOT_CFG3[2]	EIM_A18	DISP1_DATA13	Boot freq – preferred 0
BOOT_CFG4[7]	EIM_EB3	EIM_EB3	Must be 0

The other signals in BOOT_CFG3 and BOOT_CFG4 that are not defined in the above two tables do not affect this boot method.

13.4 SR-SOM-MX6 Boot from SDHC3 eMMC (as in HummingBoard edge eMMC or SOM 1.5 on SOM eMMC)

The following is an example of booting SD card through schematics signals SD3_*:

The following must be pulled up (10 kohm or lower):

BOOT CFG name	i.MX6 pad name	Schematics pad name
BOOT_CFG1[5]	EIM_DA5	DISP1_DATA04
BOOT_CFG1[6]	EIM_DA6	DISP1_DATA03
BOOT_CFG2[4]	EIM_DA11	DI1_PIN03

SolidRun tested pulling down the signals as described below, but the user can experiment with the signals that are not marked with 'Must be 0'; but SolidRun does not test those signals behavior.

BOOT CFG name	i.MX6 pad name	Schematics pad name	Notes
BOOT_CFG1[0]	EIM_DA0	DISP1_DATA09	Can be either 0 or 1
BOOT_CFG1[1]	EIM_DA1	DISP1_DATA08	Must be 0
BOOT_CFG1[2]	EIM_DA2	DISP1_DATA07	Must be 0
BOOT_CFG1[3]	EIM_DA3	DISP1_DATA06	Must be 0
BOOT_CFG1[4]	EIM_DA4	DISP1_DATA05	Must be 0
BOOT_CFG1[7]	EIM_DA7	DISP1_DATA02	Must be 0
BOOT_CFG2[0]	EIM_DA8	DISP1_DATA01	Must be 0
BOOT_CFG2[1]	EIM_DA9	DISP1_DATA00	Must be 0
BOOT_CFG2[2]	EIM_DA10	DI1_PIN15	Must be 0
BOOT_CFG2[3]	EIM_DA11	DI1_PIN02	Must be 0
BOOT_CFG2[5]	EIM_DA13	DI1_D0_CS	Can be 1 or 0
BOOT_CFG2[6]	EIM_DA14	DI1_D1_CS	Must be 0
BOOT_CFG2[7]	EIM_DA15	DI1_PIN01	Must be 0
BOOT_CFG3[6]	EIM_A22	DISP1_DATA17	Must be 0
BOOT_CFG3[7]	EIM_A23	DISP1_DATA18	Must be 0
BOOT_CFG3[2]	EIM_A18	DISP1_DATA13	Boot freq – preferred 0
BOOT_CFG4[7]	EIM_EB3	EIM_EB3	Must be 0

The other signals in BOOT_CFG3 and BOOT_CFG4 that are not defined in the above two tables do not affect this boot method.

13.5 SR-SOM-MX6 BOOT FROM SATA (AS IN HUMMINGBOARD EDGE M.2) –

The following must be pulled up (10 kohm or lower):

BOOT CFG name	i.MX6 pad name	Schematics pad name
BOOT_CFG1[5]	EIM_DA5	DISP1_DATA04
BOOT_CFG2[4]	EIM_DA11	DI1_PIN03

SolidRun tested pulling down the signals as described below, but the user can experiment with the signals that are not marked with 'Must be 0'; but SolidRun does not test those signals behavior.

BOOT CFG name	i.MX6 pad name	Schematics pad name	Notes
BOOT_CFG1[4]	EIM_DA4	DISP1_DATA05	Must be 0
BOOT_CFG1[6]	EIM_DA6	DISP1_DATA03	Must be 0
BOOT_CFG1[7]	EIM_DA7	DISP1_DATA02	Must be 0
BOOT_CFG2[0]	EIM_DA8	DISP1_DATA01	Refer to spec about BOOT_CFG2[1:0]
BOOT_CFG2[1]	EIM_DA9	DISP1_DATA00	As above; defines cable length
BOOT_CFG2[2]	EIM_DA10	DI1_PIN15	Can be either 0 or 1
BOOT_CFG2[3]	EIM_DA11	DI1_PIN02	Can be either 0 or 1 (RX spread spectrum)
BOOT_CFG2[4]	EIM_DA11	DI1_PIN03	Can be either 0 or 1 (TX spread spectrum)
BOOT_CFG3[6]	EIM_A22	DISP1_DATA17	Must be 0
BOOT_CFG3[7]	EIM_A23	DISP1_DATA18	Must be 0
BOOT_CFG3[2]	EIM_A18	DISP1_DATA13	Boot freq – preferred 0
BOOT_CFG4[7]	EIM_EB3	EIM_EB3	Must be 0

The other signals in BOOT_CFG1, BOOT_CFG2, BOOT_CFG3 and BOOT_CFG4 that are not defined in the above two tables do not affect this boot method.

13.6 SR-SOM-MX6 Rev 1.3 Debugging Capability

Rev 1.3 of SR-SOM-MX6 exposes two main debugging interfaces:

1. UART interface
2. JTAG interface

The UART interface is a null modem interface that is internally pulled up to two different voltage levels:

1. NVCC_EIM0 voltage in case AzureWave SiP is not used (typically 3.3V)
2. 2.8v when the AzureWave SiP is used (signals are shared with SDIO interface that is limited to 2.8V)

The UART interface is optional to use and mentioned here since most of the software infrastructure used in CuBox-i and HummingBoard uses those two signals for debugging.

JTAG interface is on the SR-SOM-mx6 and is exposed as test pins. Following is a snapshot of the test points and its connectivity traces:

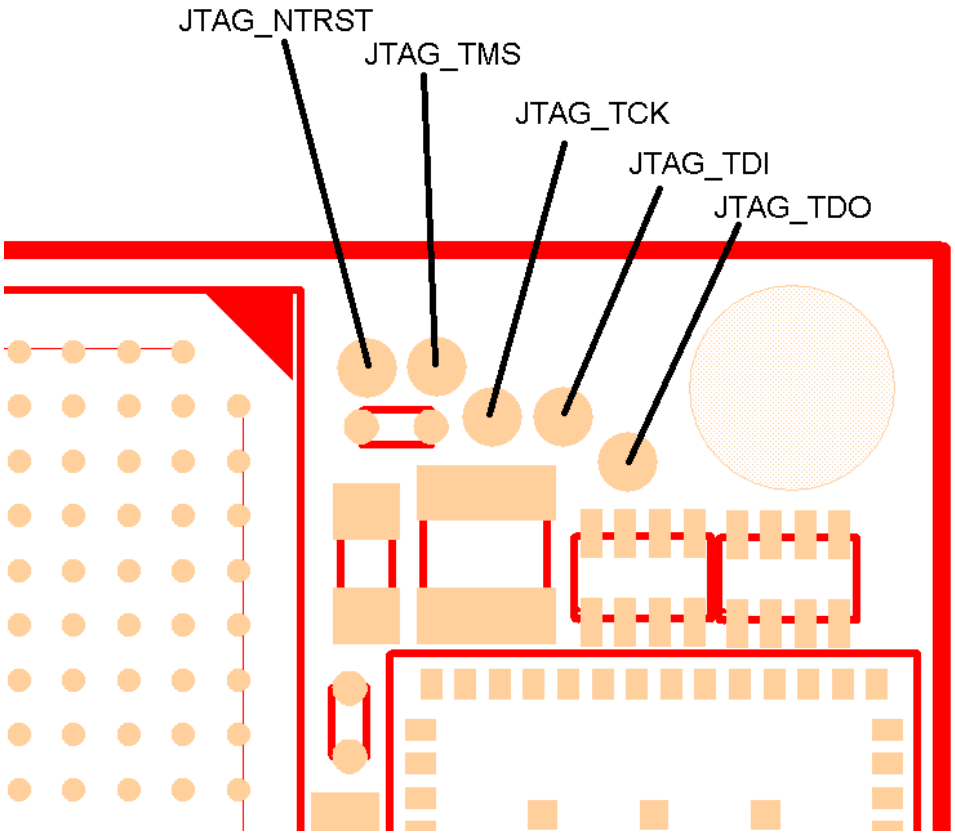


Figure 5 JTAG test point pins

13.7 SR-SOM-MX6 Rev 1.5 Debugging Capability

Rev 1.5 of SR-SOM-MX6 exposes the UART interface which is the main debugging interface.

The UART interface is a null modem interface.

14 DIFFERENCES BETWEEN SR-SOM-MX6 VERSIONS

14.1 CHANGES BETWEEN SR-SOM-MX6 REV 1.1 TO REV 1.2:

Moved VDD_HIGH_IN power rail from NVCC_EIM0 power pin to SNVS_3V0 power pin.

14.2 CHANGES BETWEEN SR-SOM-MX6 REV 1.2 TO REV 1.3:

Added three mechanical holes for RF cage to cover BRCM4330 based WiFi/BT SiP.

14.3 CHANGES BETWEEN SR-SOM-MX6 REV 1.3 TO REV 1.5:

Refer to PCN #20160901000 on SolidRun's wiki pages for more details, the highlights are –

1. Replaced BCM4330 based SiP with TI Wilink8
2. Added optional eMMC. Note that if the SOM has eMMC assembled then the SD3_* signals are not routed to the board-to-board headers but are used locally for the eMMC on the SOM.

15 SR-SOM-MX6 Typical Power Consumption

The following power measurements were performed on a CuBox-i4pro based system, where the main supply is 5V and internally a 5V to 3.3V LDO is being used on the carrier board (refer to CuBox-i rev-1.1 schematics).

The CuBox-i4pro incorporates the quad processor at 1GHz, 2GByte of DDR3 memory, gigabit Ethernet phy and the WiFi and Bluetooth chipset.

Setup	5V DC input power consumption	Notes
Android idle	240mA	Performance governor, HDMI is on, USB, eSata, WiFi and Ethernet are off
Android idle with Ethernet	340mA	Performance governor, HDMI is on, USB, eSata, WiFi and Ethernet is 1Gbps (note #1)
Android Nenamark2 benchmark	750mA	Performance governor, HDMI is on, usb, sata, wifi and Ethernet are off
Full load - Android Nenamark2 benchmark + 4 processors running 100% (dd command memory to memory)	1190mA	Performance governor, HDMI is on, USB, eSata, WiFi and Ethernet is 1Gbps (note #1). Tj is 55c
Full load - Android Nenamark2 benchmark + 4 processors running 100% (dd command memory to memory)	1300mA	Performance governor, HDMI is on, usb, sata, wifi and Ethernet is 1Gbps (note #1). Tj is 87c (note #2)
Video 1080p Big Buck Bunny with AC3 audio codec (gstreamer from local SD)	Varies between 340mA to 410mA	Performance governor, HDMI is on, USB, eSata, WiFi and Ethernet are off
Linux idle	170mA	Performance governor, HDMI, USB, eSata, WiFi and Ethernet are all off.
Linux suspend to memory	30mA	Note #3

Figure 6 Typical Power Consumption: CuBox-i4pro

Notes:

1. CuBox-i uses an LDO that provides 5V to 3.3V conversion that feeds the Ethernet PHY on the SOM. Due to that, the addition of 100mA on the 3.3V rail when PHY is set to 1Gbps, adds 100mA consumption on the 5.0V power rails.
2. Notice the power difference between the same workload while Tjunction of the die is 55c and 87c (~110mA difference from the 5V power rail).
   It takes about 60 minutes to reach that stable 87c Tjunction.
3. This is using Linux suspend to memory when the front LED is off. This consumption is mainly due to DDR entering self-refresh (2GByte) and some consumption on the 3.3V LDO and leakage on the processor and SoC digital part rails.

15.1 SR-SOM-MX6 MAXIMUM RATING

Following are the maximum ratings on different power signals and power rails.

Parameter Description	Symbol	Min	Max	Unit
Supplies VDD_SNVS_IN and VDD_HIGH_IN on i.MX6 starting rev 1.2	VSNVS_3V0	2.8	3.3	V
eMMC/SD supply voltage	NVCC_SD2 NVCC_SD3	1.65	3.6	V
Main 3.3v supply voltage for i.MX6, Ethernet phy and other	NVCC_EIM0	3.2	3.6	V
USB OTG and H1 supply voltage	USB_OTG_VBUS USB_H1_VBUS	4.4	5.25	V
DC-DC supplies, HDMI I2C boost and WiFi/BT main supply (1)	VIN_5V0	3.2	6	V
Supplies VDD_SNVS_IN and VDD_HIGH_IN on i.MX6	VSNVS_3V0	-	250	mA
Supplies i.MX6 (GPIO, Parallel display interface etc…), AR8030/AR8035 Ethernet phy, part of the AzureWave SiP	NVCC_EIM0	-	300 (2) (5)	mA
SD2 I/O	NVCC_SD2	-	22 (3)	mA
SD3 I/O	NVCC_SD3	-	40 (3)	mA
Supplies all SR-SOM-MX6 power management devices.	VIN_5V0	-	1500 (4) (5)	mA

Figure 7 maximum power ratings

1. HDMI I2C is voltage boosted using VIN_5V0 power rail. Due to that VIN_5V0 = 5V is recommended since HDMI EDID requires 5V voltage levels.
2. AR8035 Gigabit Ethernet PHY consumes 150mA out of those in a 100-meter cable configuration.
   This is reduced to 150mA when the AR8035 is not active.
3. Assumes ultra-high speed: 1.8v, 100MHz clock rate and double data rate on data; 4-bit data on SD2 and 8-bit data on SD3.
4. Assumes VIN_5V0 = 5v. When supplying less than 5V, the maximum current increases accordingly; it is recommended to add additional margins on current limit.
   Notice that a common practice when integrating SR-SOM-MX6 is to have a single DC-DC, of 3.2v that supplies all the SR-SOM-MX6 supplies, except the USB_OTG_VBUS and USB_HOST_VBUS.
5. SR-SOM-MX6 rev 1.5 incorporates TI WiLink8 based device vs. BCM4330. This adds 285mA on the NVCC_EIM0 but remove 200mA requirement from VIN_5V0.

16 SR-SOM-MX6 MECHANICAL DESCRIPTION

Following is a diagram of the TOP VIEW of the SR-SOM-MX6.

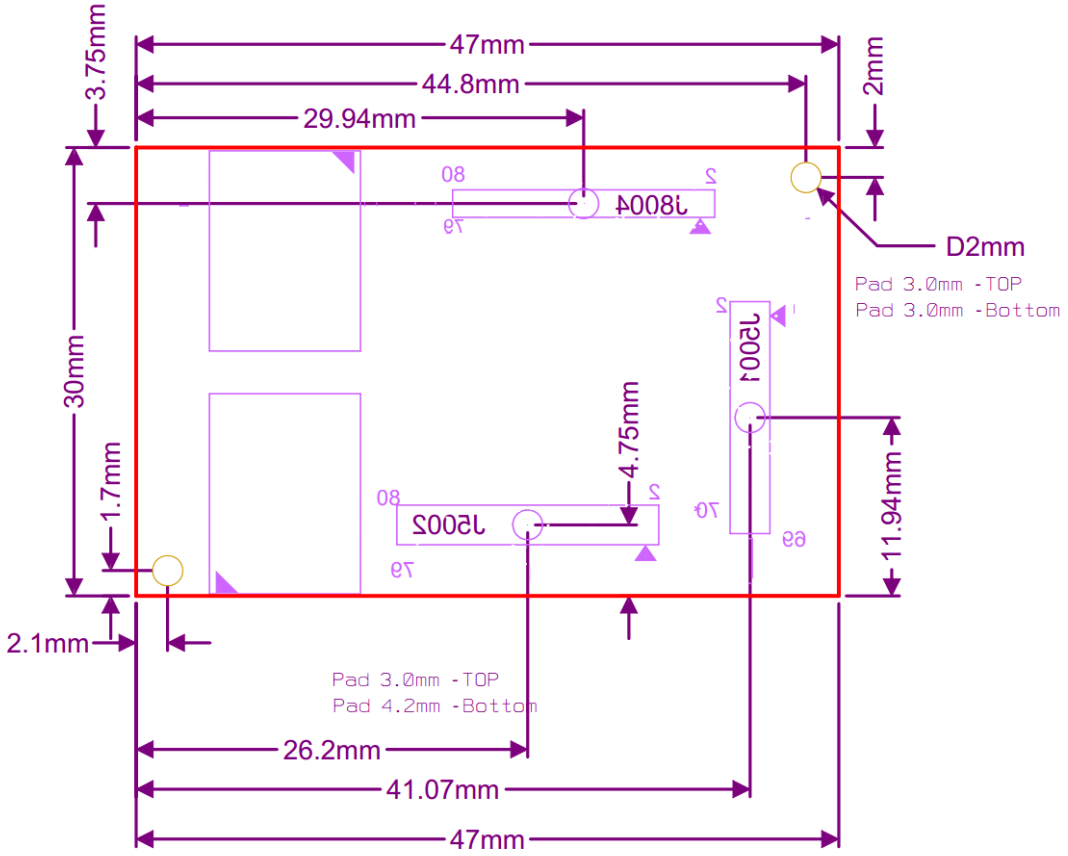


Figure 8 Top mechanical view of the SR-SOM-MX6

Note the following details:

- The carrier board must use the same footprint as in the above mechanical footprint. Since this is a TOP VIEW of the print side of the SR-SOM-MX6, the diagram above describes the dimensions and placement of the board-to-board headers, mechanical holes and boundaries of the SR-SOM-MX6, as-is.
- J5002 is the main board-to-board header (bottom side in the diagram).
- J8004 is the second board-to-board header (upper side in the diagram).
- J5001 is the third board-to-board header (right side in the diagram).
- CuBox-i design does not use the mechanical holes, since the mating strength of two Hirose DF40 pairs and the internal heat spreader is satisfactory for the design requirements.
- In case 1.5mm mating height was chosen, then the SR-SOM-MX6 requirement would be that all area beneath it on the carrier will be all dedicated ONLY for the board-to-board connectivity; no other components are allowed.
  In case higher mating is chosen, then 1.5mm should be reserved for the SR-SOM-MX6. For instance, if 3.5mm mating height is chosen, then 1.5mm is dedicated to the SR-SOM-MX6 print side components and the remaining 2mm for the carrier components underneath the SR-SOM-MX6.

Refer to SolidRun HummingBoard and CuBox-i design and layout, where there are examples of the main and second 80 pin header board-to-board usage.

17 ORDERING INFORMATION

Please refer to the SolidRun website for more information regarding part numbers and the procedure for placing an order.

www.solid-run.com

18 Federal Communications Commission (FCC) Statement

18.1 Labelling requirement for small device statement (FCC15.19(3))

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

18.2 Radio Frequency Interference (RFI) (FCC 15.105)

This equipment has been tested and found to comply with the limits for Class B digital devices pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try and correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the
- receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

18.3 Modifications (FCC 15.21)

Changes or modifications to this equipment not expressly approved by SolidRun Ltd. may void the user's authority to operate this equipment.

18.4 RF Exposure info (FCC 2.1093)

This equipment has been approved for mobile applications where the equipment should be used at distances greater than 20cm from the human body (with the Exception of hands, wrists, feet and ankles). Operation at distances less than 20 cm is strictly prohibited

19 CANADIAN COMPLIANCE

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

The device meets the exemption from the routine evaluation limits in section 2.5 of RSS 102 and compliance with RSS-102 RF exposure, users can obtain Canadian information on RF exposure and compliance.

Le dispositif rencontre l'exemption des limites courantes d'évaluation dans la section 2.5 de RSS 102 et la conformité à l'exposition de RSS-102 rf, utilisateurs peut obtenir l'information canadienne sur l'exposition et la conformité de rf.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body.

Cet émetteur ne doit pas tre Co-placé ou ne fonctionnant en même temps qu'aucune autre antenne ou émetteur. Cet équipement devrait être installé et actionné avec une distance minimum de 20 centimètres entre le radiateur et votre corps.

This radio transmitter with model: SR-SOM-mx6 has been approved by Industry Canada to operate with the antenna type listed below with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna type not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Le présent émetteur radio with model: SR-SOM-mx6 a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Antenna	Manufacture	Brand	Module Name	Antenna Type	Connector	Gain (dBi)	Frequency band
xxxx	SRT	SRT	SRT-2.4G-PCB-8	SRT-2.4G-PCB-8	IPEX	3DBI	2.4~2.5G

19.1 RF EXPOSURE INFO(IC RSS-102)

“The installer of this radio equipment must ensure that the antenna is located or pointed such that it does not emit RF field in excess of Health Canada limits for the general population; consult Safety Code 6, obtainable from Heath Canada’s website www.hc-sc.gc.ca/rpb.”

19.2 CLASS B NOTICE FOR CANADA

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

20 Contact Information and Resources

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