
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32F777NIHx
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	05/09/2021

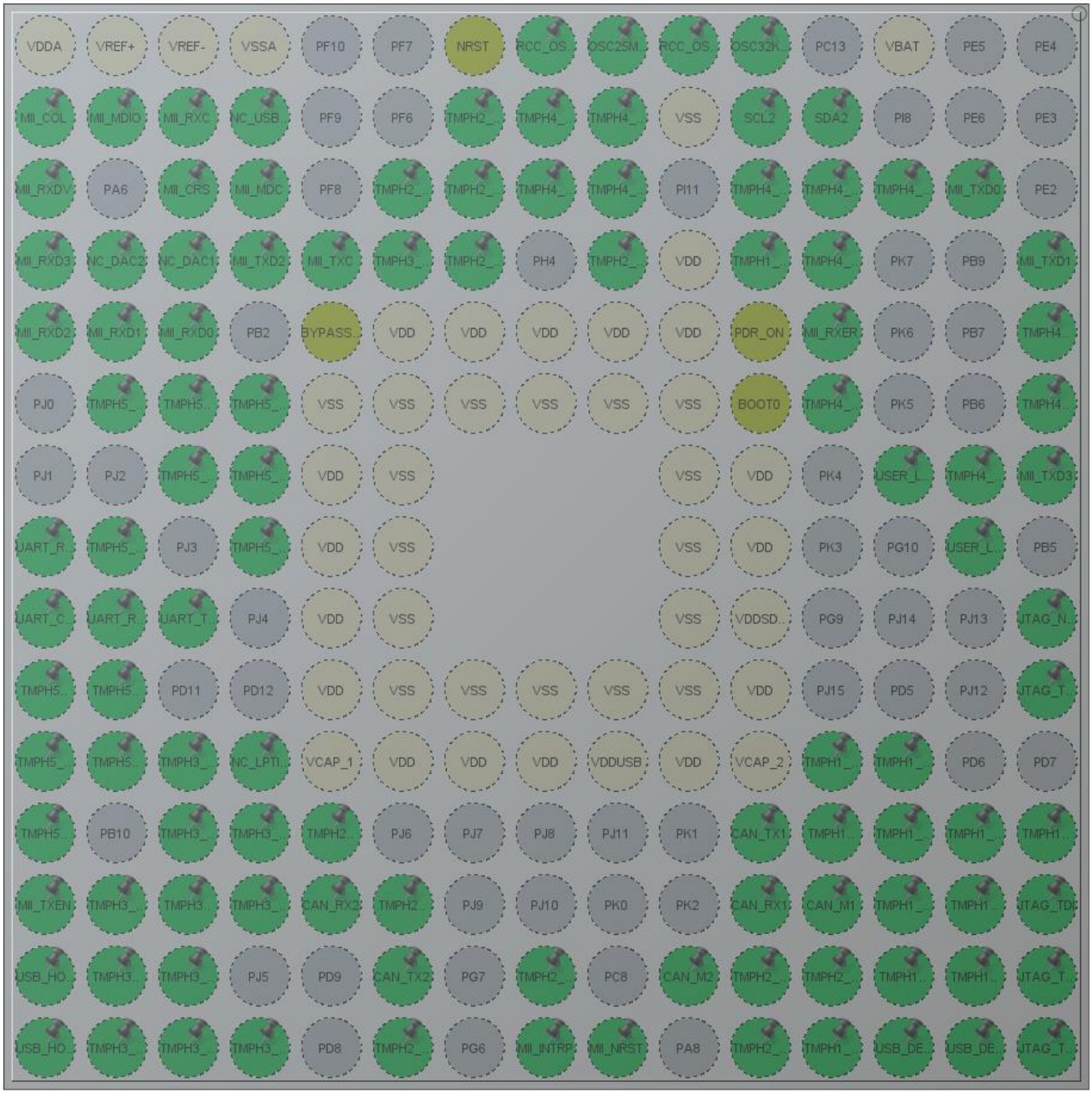
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F777NIHx
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



TFBGA216 (Top view - Rotated +90°)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A4	PG14	I/O	ETH_TXD1	MII_TXD1
A5	PE1	I/O	UART8_TX	TMPH4_PE1_TXD8
A6	PE0	I/O	UART8_RX	TMPH4_PE0_RXD8
A7	PB8	I/O	ETH_TXD3	MII_TXD3
A9	PB4	I/O	SYS_JTRST	JTAG_NTRST
A10	PB3	I/O	SYS_JTDO-SWO	JTAG_TDO_TRACE_SWO
A12	PC12	I/O	UART5_TX	TMPH1_PC12_TXD5
A13	PA15	I/O	SYS_JTDI	JTAG_TDI
A14	PA14	I/O	SYS_JTCK-SWCLK	JTAG_TCK_SW_CLK
A15	PA13	I/O	SYS_JTMS-SWDIO	JTAG_TMS_SW_DIO
B3	PG13	I/O	ETH_TXD0	MII_TXD0
B7	PG15 *	I/O	GPIO_Analog	TMPH4_PG15
B8	PG11 *	I/O	GPIO_Output	USER_LED1
B12	PD0	I/O	UART4_RX	TMPH1_PD0_RXD4
B13	PC11	I/O	USART3_RX	TMPH1_PC11_RXD3
B14	PC10	I/O	USART3_TX	TMPH1_PC10_TXD3
B15	PA12	I/O	USB_OTG_FS_DP	USB_DEV_DP
C1	VBAT	Power		
C3	PI4 *	I/O	GPIO_Analog	TMPH4_PI4
C7	PG12 *	I/O	GPIO_Output	USER_LED2
C11	PD3 *	I/O	GPIO_Analog	TMPH1_PD3
C12	PD1	I/O	UART4_TX	TMPH1_PD1_TXD4
C13	PI3 *	I/O	GPIO_Analog	TMPH1_PI3
C14	PI2	I/O	TIM8_CH4	TMPH1_PI2_PWM84
C15	PA11	I/O	USB_OTG_FS_DM	USB_DEV_DM
D2	PF0	I/O	I2C2_SDA	SDA2
D3	PI5	I/O	TIM8_CH1	TMPH4_PI5_PWM81
D4	PI7	I/O	TIM8_CH3	TMPH4_PI7_PWM83
D5	PI10	I/O	ETH_RX_ER	MII_RXER
D6	PI6	I/O	TIM8_CH2	TMPH4_PI6_PWM82
D11	PD4 *	I/O	GPIO_Analog	TMPH1_PD4
D12	PD2	I/O	UART5_RX	TMPH1_PD2_RXD5
D13	PH15 *	I/O	GPIO_Output	CAN_M1
D14	PI1 *	I/O	GPIO_Analog	TMPH2_PI1
D15	PA10 *	I/O	GPIO_Analog	TMPH1_PA10
E1	PC14/OSC32_IN	I/O	RCC_OSC32_IN	OSC32K_IN

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
E2	PF1	I/O	I2C2_SCL	SCL2
E3	PI12 *	I/O	GPIO_Analog	TMPH4_PI12
E4	PI9 *	I/O	GPIO_Analog	TMPH1_PI9
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDDSDMMC	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E12	PH13	I/O	CAN1_TX	CAN_TX1
E13	PH14	I/O	CAN1_RX	CAN_RX1
E14	PI0 *	I/O	GPIO_Analog	TMPH2_PI0
E15	PA9 *	I/O	GPIO_Analog	TMPH2_PA9
F1	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F14	PC9 *	I/O	GPIO_Output	CAN_M2
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	OSC25M_IN
G2	PF2 *	I/O	GPIO_Analog	TMPH4_PF2
G3	PI13 *	I/O	GPIO_Analog	TMPH4_PI13
G4	PI15 *	I/O	GPIO_Analog	TMPH2_PI15
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G15	PC7 *	I/O	GPIO_Output	MII_NRST
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	GPIO_Analog, ADC3_IN9	TMPH4_PF3_ADC39
H3	PI14 *	I/O	GPIO_Analog	TMPH4_PI14
H5	VDD	Power		
H6	VSS	Power		

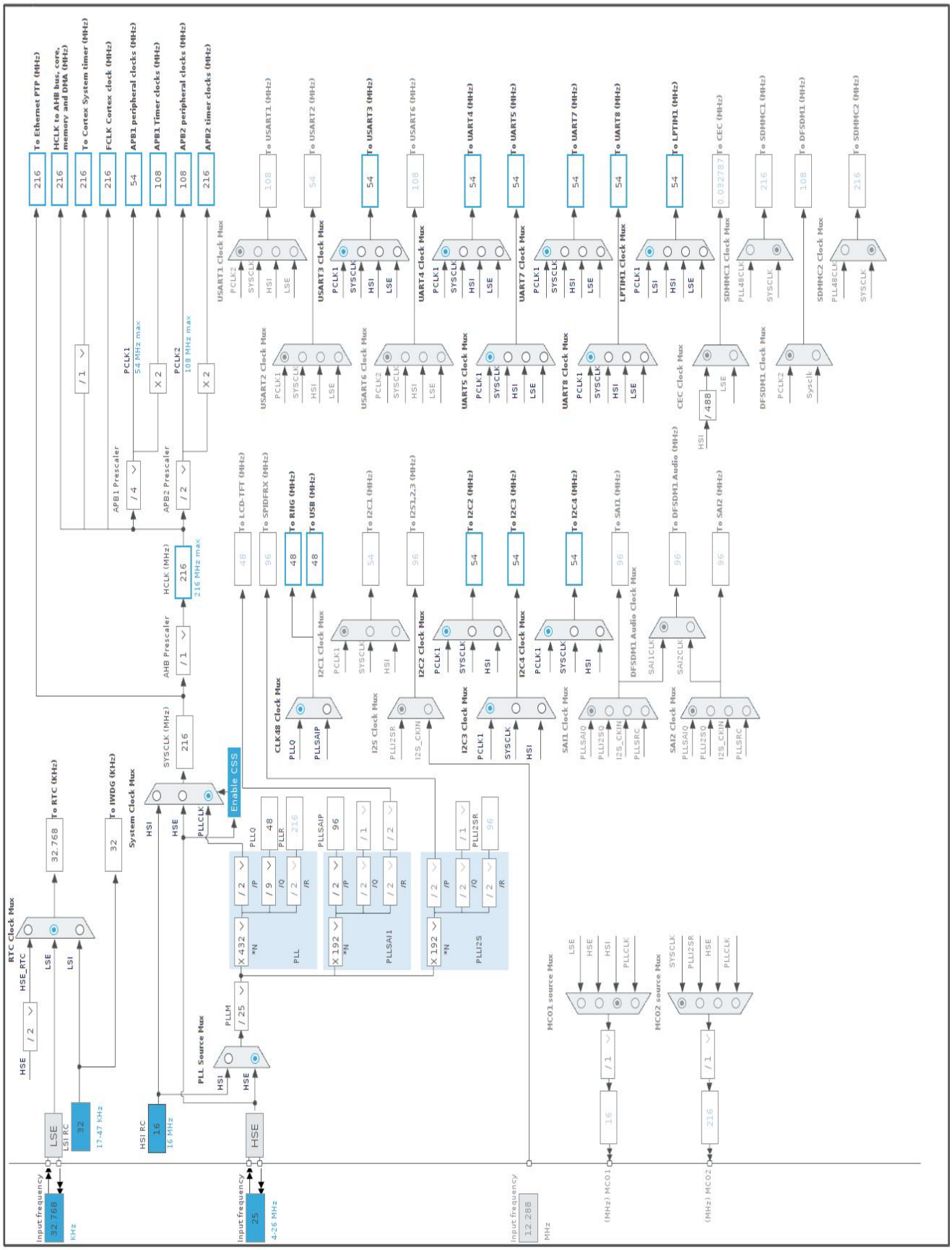
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H10	VSS	Power		
H11	VDD	Power		
H14	PG8 *	I/O	GPIO_Analog	TMPH2_PG8
H15	PC6	I/O	GPIO_EXTI6	MII_INTRP
J1	NRST	Reset		
J2	PF4	I/O	GPIO_Analog, ADC3_IN14	TMPH2_PF4_ADC314
J3	PH5	I/O	SPI5_NSS	TMPH2_PH5_NSS5
J4	PH3 *	I/O	GPIO_Analog	TMPH2_PH3
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
K3	PF5	I/O	GPIO_Analog, ADC3_IN15	TMPH2_PF5_ADC315
K4	PH2 *	I/O	GPIO_Analog	TMPH3_PH2
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K13	PD15	I/O	UART8_RTS	TMPH2_PD15_RTS8
K14	PB13	I/O	CAN2_TX	CAN_TX2
K15	PD10 *	I/O	GPIO_Analog	TMPH2_PD10
L4	PC3	I/O	ETH_TX_CLK	MII_TXC
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	UART8_CTS	TMPH2_PD14_CTS8
L13	PB12	I/O	CAN2_RX	CAN_RX2
M1	VSSA	Power		
M2	PC0 *	I/O	GPIO_Output	NC_USB_HOST_VBUS
M3	PC1	I/O	ETH_MDC	MII_MDC
M4	PC2	I/O	ETH_TXD2	MII_TXD2
M6	PF12 *	I/O	GPIO_Analog	TMPH5_PF12

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
M7	PG1 *	I/O	GPIO_Analog	TMPH5_PG1
M8	PF15	I/O	I2C4_SDA	TMPH5_PF15_SDA4
M11	PD13	I/O	LPTIM1_OUT	NC_LPTIM1
M12	PG3 *	I/O	GPIO_Analog	TMPH3_PG3
M13	PG2 *	I/O	GPIO_Analog	TMPH3_PG2
M15	PH12 *	I/O	GPIO_Analog	TMPH3_PH12
N1	VREF-	Power		
N2	PA1	I/O	ETH_RX_CLK	MII_RXC
N3	PA0/WKUP	I/O	ETH_CRS	MII_CRS
N4	PA4	I/O	DAC_OUT1	NC_DAC1
N5	PC4	I/O	ETH_RXD0	MII_RXD0
N6	PF13	I/O	I2C4_SMBA	TMPH5_PF13_SMBA4
N7	PG0 *	I/O	GPIO_Analog	TMPH5_PG0
N9	PE8	I/O	UART7_TX	UART_TXD7
N11	PG5 *	I/O	GPIO_Analog	TMPH3_PG5
N12	PG4 *	I/O	GPIO_Analog	TMPH3_PG4
N13	PH7	I/O	I2C3_SCL	TMPH3_PH7_SCL3_MISO5
N14	PH9 *	I/O	GPIO_Analog	TMPH3_PH9
N15	PH11 *	I/O	GPIO_Analog	TMPH3_PH11
P1	VREF+	Power		
P2	PA2	I/O	ETH_MDIO	MII_MDIO
P4	PA5	I/O	DAC_OUT2	NC_DAC2
P5	PC5	I/O	ETH_RXD1	MII_RXD1
P6	PF14	I/O	I2C4_SCL	TMPH5_PF14_SCL4
P8	PF11	I/O	SPI5_MOSI	TMPH5_PF11_MOSI5
P9	PE9	I/O	UART7_RTS	UART_RTS7
P10	PE11	I/O	SPI4_NSS	TMPH5_PE11_NSS4
P11	PE14	I/O	SPI4_MOSI	TMPH5_PE14_MOSI4
P13	PH6	I/O	SPI5_SCK	TMPH3_PH6_SCK5
P14	PH8	I/O	I2C3_SDA	TMPH3_PH8_SDA3
P15	PH10 *	I/O	GPIO_Analog	TMPH3_PH10
R1	VDDA	Power		
R2	PA3	I/O	ETH_COL	MII_COL
R3	PA7	I/O	ETH_RX_DV	MII_RXDV
R4	PB1	I/O	ETH_RXD3	MII_RXD3
R5	PB0	I/O	ETH_RXD2	MII_RXD2
R8	PE7	I/O	UART7_RX	UART_RXD7
R9	PE10	I/O	UART7_CTS	UART_CTS7
R10	PE12	I/O	SPI4_SCK	TMPH5_PE12_SCK4

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R11	PE15 *	I/O	GPIO_Analog	TMPH5_PE15
R12	PE13	I/O	SPI4_MISO	TMPH5_PE13_MISO4
R13	PB11	I/O	ETH_TX_EN	MII_TXEN
R14	PB14	I/O	USB_OTG_HS_DM	USB_HOST_DM
R15	PB15	I/O	USB_OTG_HS_DP	USB_HOST_DP

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32F777NIHx
Project Folder	/home/slz/EmbedTools/STM32CubeMX/tiac_magpie
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_CAN1_Init	CAN1
5	MX_CAN2_Init	CAN2
6	MX_I2C2_Init	I2C2
7	MX_UART7_Init	UART7
8	MX_I2C4_SMBUS_Init	I2C4
9	MX_ADC3_Init	ADC3
10	MX_IWDG_Init	IWDG
11	MX_TIM8_Init	TIM8

Rank	Function Name	Peripheral Instance Name
12	MX_CRC_Init	CRC
13	MX_CRYP_Init	CRYP
14	MX_HASH_Init	HASH
15	MX_RNG_Init	RNG
16	MX_RTC_Init	RTC
17	MX_FATFS_Init	FATFS
18	MX_LWIP_Init	LWIP
19	MX_MBEDTLS_Init	MBEDTLS
20	MX_USB_DEVICE_Init	USB_DEVICE
21	MX_USB_HOST_Init	USB_HOST
22	MX_DAC_Init	DAC
23	MX_LPTIM1_Init	LPTIM1
24	MX_UART4_Init	UART4
25	MX_UART5_Init	UART5
26	MX_USART3_UART_Init	USART3
27	MX_UART8_Init	UART8
28	MX_SPI4_Init	SPI4
29	MX_I2C3_Init	I2C3
30	MX_SPI5_Init	SPI5

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F777NIHx
Datasheet	DS11243_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

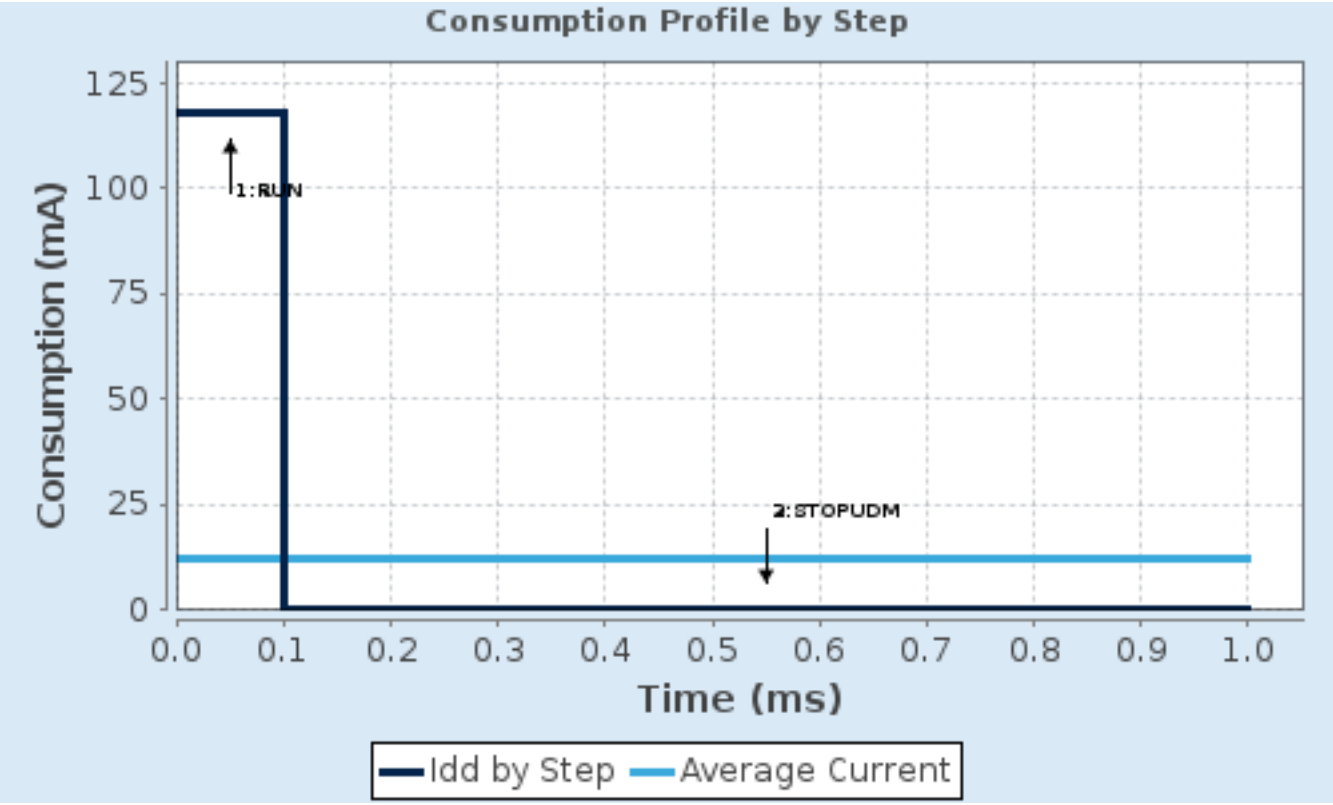
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	93.71	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC3

mode: IN9

mode: IN14

mode: IN15

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 9
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CAN1

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**4 ***
Time Quantum	**74.07407407407408 ***
Time Quanta in Bit Segment 1	**7 Times ***
Time Quanta in Bit Segment 2	**7 Times ***

Time for one Bit	**1111.11 ***
Baud Rate	**900000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.3. CAN2

mode: Activated

7.3.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**4 ***
Time Quantum	**74.07407407407408 ***
Time Quanta in Bit Segment 1	**7 Times ***
Time Quanta in Bit Segment 2	**7 Times ***
Time for one Bit	**1111.11 ***
Baud Rate	**900000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.4. CRC

mode: Activated

7.4.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.5. CRYP

mode: Activated

7.5.1. Parameter Settings:

Algorithm:

Data encryption algorithm	**AES ECB ***

Parameters:

Data type	32b(no swapping)
Key size	128b
Encryption/Decryption key	00000000 00000000 00000000 00000000
Data width unit	Word

7.6. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

7.6.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

7.7. ETH

Mode: MII

mode: Activate Rx Err signal

7.7.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled
Speed	100 MBits/s
Duplex Mode	Full Duplex

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	**7 ***

Ethernet Basic Configuration:

Rx Mode	Interrupt Mode
TX IP Header Checksum Computation	By hardware

7.7.2. Advanced Parameters:

External PHY Configuration:

PHY	**user PHY ***
PHY Address Value	7
PHY name	**KSZ8081 ***
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	

	0x0000 *
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***

7.8. HASH

mode: Activated

7.8.1. Parameter Settings:

Algorithm:

Secure hash algorithm type	**HMAC SHA224 ***

Parameters:

Hash data type in bit	32
pKey input type	HEXA
pKey user input	00

7.9. I2C2

I2C: I2C

7.9.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled

Timing	**0x6000030D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.10. I2C3

I2C: I2C

7.10.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.11. I2C4

I2C: SMBus-Alert-mode

7.11.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0

Analog Filter	Enabled
Timing	**0x20404768 ***

SMBus Features:

Packet Error Check Mode	**PEC Enabled ***
Peripheral Mode	**Peripheral Mode Smbus Master ***

SMBus Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	1

Timeout configuration:

Extended Clock Timeout	Disabled
Idle Clock Timeout Detection	Disabled
Timeout Time (ns)	25000000
Timeout	**0x00008293 ***

7.12. IWDG

mode: Activated

7.12.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	4
IWDG window value	4095
IWDG down-counter reload value	4095

7.13. LPTIM1

Mode: Counts internal clock events

mode: Waveform Generation

7.13.1. Parameter Settings:

Clock:

Clock Prescaler	Prescaler Div1

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	**RTC Alarm A ***
Active Edge	Active Edge Rising
Sample Time	Direct Transition

Output:

Output Polarity	Output Polarity High

7.14. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.14.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.15. RNG

mode: Activated

7.16. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm A

7.16.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127

Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	**Friday ***
Month	January
Date	1
Year	0

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	**Enable ***
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	**Weekday ***
Alarm Week Day	**Sunday ***

7.17. SPI4

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.17.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**54.0 MBits/s ***
Clock Polarity (CPOL)	Low

Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

7.18. SPI5

Mode: Half-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.18.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**54.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

7.19. SYS

Debug: JTAG (5 pins)

Timebase Source: SysTick

7.20. TIM8

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: Input Capture direct mode

7.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**32767 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**32767 ***

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**32767 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.21. UART4

Mode: Asynchronous

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.22. UART5

Mode: Asynchronous

7.22.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.23. UART7

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.23.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.24. UART8

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.24.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.25. USART3

Mode: Asynchronous

7.25.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.26. USB_OTG_FS
Mode: Device_Only

7.26.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	**Enabled ***

7.27. USB_OTG_HS
Internal FS Phy: Host_Only

7.27.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	**Enabled ***

Physical interface	Internal Phy
Signal start of frame	**Enabled ***

7.28. FATFS
mode: USB Disk
7.28.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000

USE_MUTEX	Disabled
SYNC_t (O/S sync object)	osSemaphoreId_t
FS_LOCK (Number of files opened simultaneously)	2

7.28.2. Advanced Settings:

USBH:

USBH instance	USB Host MSC HS
Use dma template	Enabled

7.29. FREERTOS

Interface: CMSIS_V2

7.29.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	**Enabled ***

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled

USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	**Enabled ***

7.29.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled

xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.29.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.30. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.30.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	Enabled

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled
CMSIS_VERSION (CMSIS API Version used)	CMSIS v2

MBEDTLS Dependency:

WITH_MBEDTLS (Use MBEDTLS ** CubeMX specific **)	Enabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	**Enabled ***

LWIP_DNS (DNS Module)	Enabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.30.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	24
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0
LWIP_SOCKET_SELECT (Select for Socket)	Enabled
LWIP_SOCKET_POLL (Poll for Socket)	Enabled

7.30.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.30.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	**Enabled ***

7.30.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	**Enabled ***

7.30.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	**Enabled ***

7.30.7. SNTP/SMTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	**Enabled ***

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	**Enabled ***

7.30.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	**Enabled ***

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	**Enabled ***

7.30.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	**Enabled ***

7.30.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Enabled

7.30.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled

CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.30.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

7.31. MBEDTLS
mode: Enabled
7.31.1. Version and modes:

Version:

MBEDTLS version	2.16.2

TCP/IP stack:

TCP/IP stack	LWIP

RNG dependency:

RNG IP	HW RNG

Modes:

MBEDTLS_SSL_CLI_C	Defined
MBEDTLS_SSL_SRV_C	Defined

7.31.2. Feature support:

System support:

MBEDTLS_HAVE_ASM	Defined
MBEDTLS_NO_UDBL_DIVISION	Defined
MBEDTLS_HAVE_TIME	Defined
MBEDTLS_HAVE_TIME_DATE	Defined

General:

MBEDTLS_ECP_NIST_OPTIM	Defined
MBEDTLS_ECDSA_DETERMINISTIC	Defined
MBEDTLS_PK_PARSE_EC_EXTENDED	Defined

MBEDTLS_ERROR_STRERROR_DUMMY	Defined
MBEDTLS_GENPRIME	Defined
MBEDTLS_NO_PLATFORM_ENTROPY	Defined
MBEDTLS_PK_RSA_ALT_SUPPORT	Defined
MBEDTLS_PKCS1_V15	Defined
MBEDTLS_PKCS1_V21	Defined
MBEDTLS_SELF_TEST	Defined
MBEDTLS_VERSION_FEATURES	Defined

Ciphering:

MBEDTLS_CIPHER_MODE_CBC	Defined
MBEDTLS_CIPHER_MODE_CFB	Defined
MBEDTLS_CIPHER_MODE_CTR	Defined
MBEDTLS_CIPHER_MODE_OFB	Defined
MBEDTLS_CIPHER_MODE_XTS	Defined
MBEDTLS_CIPHER_PADDING_PKCS7	Defined
MBEDTLS_CIPHER_PADDING_ONE_AND_ZEROS	Defined
MBEDTLS_CIPHER_PADDING_ZEROS_AND_LEN	Defined
MBEDTLS_CIPHER_PADDING_ZEROS	Defined
MBEDTLS_REMOVE_ARC4_CIPHERSUITES	Defined
MBEDTLS_REMOVE_3DES_CIPHERSUITES	Defined

Elliptic curves:

MBEDTLS_ECP_DP_SECP192R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP224R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP256R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP384R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP521R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP192K1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP224K1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP256K1_ENABLED	Defined
MBEDTLS_ECP_DP_BP256R1_ENABLED	Defined
MBEDTLS_ECP_DP_BP384R1_ENABLED	Defined
MBEDTLS_ECP_DP_BP512R1_ENABLED	Defined
MBEDTLS_ECP_DP_CURVE25519_ENABLED	Defined
MBEDTLS_ECP_DP_CURVE448_ENABLED	Defined

Key exchange:

MBEDTLS_KEY_EXCHANGE_PSK_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_DHE_PSK_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_ECDHE_PSK_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_RSA_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_DHE_RSA_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_ECDHE_RSA_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_ECDH_ECDSA_ENABLED	Defined

MBEDTLS_KEY_EXCHANGE_ECDH_RSA_ENABLED	Defined

SSL:

MBEDTLS_SSL_ALL_ALERT_MESSAGES	Defined
MBEDTLS_SSL_ENCRYPT_THEN_MAC	Defined
MBEDTLS_SSL_EXTENDED_MASTER_SECRET	Defined
MBEDTLS_SSL_FALLBACK_SCSV	Defined
MBEDTLS_SSL_CBC_RECORD_SPLITTING	Defined
MBEDTLS_SSL_RENEGOTIATION	Defined
MBEDTLS_SSL_PROTO_TLS1	Defined
MBEDTLS_SSL_PROTO_TLS1_1	Defined
MBEDTLS_SSL_PROTO_DTLS	Defined
MBEDTLS_SSL_ALPN	Defined
MBEDTLS_SSL_DTLS_ANTI_REPLAY	Defined
MBEDTLS_SSL_DTLS_HELLO_VERIFY	Defined
MBEDTLS_SSL_DTLS_CLIENT_PORT_REUSE	Defined
MBEDTLS_SSL_DTLS_BADMAC_LIMIT	Defined
MBEDTLS_SSL_SESSION_TICKETS	Defined
MBEDTLS_SSL_EXPORT_KEYS	Defined
MBEDTLS_SSL_SERVER_NAME_INDICATION	Defined
MBEDTLS_SSL_TRUNCATED_HMAC	Defined

X509:

MBEDTLS_X509_CHECK_KEY_USAGE	Defined
MBEDTLS_X509_CHECK_EXTENDED_KEY_USAGE	Defined
MBEDTLS_X509_RSASSA_PSS_SUPPORT	Defined

7.31.3. Alternate implementation:

7.31.4. Modules:

General:

MBEDTLS_AESNI_C	Defined
MBEDTLS_AES_C	Defined
MBEDTLS_ARC4_C	Defined
MBEDTLS_ASN1_PARSE_C	Defined
MBEDTLS_ASN1_WRITE_C	Defined
MBEDTLS_BASE64_C	Defined
MBEDTLS_BIGNUM_C	Defined
MBEDTLS_BLOWFISH_C	Defined
MBEDTLS_CAMELLIA_C	Defined
MBEDTLS_CCM_C	Defined

MBEDTLS_CERTS_C	Defined
MBEDTLS_CIPHER_C	Defined
MBEDTLS_CHACHA20_C	Defined
MBEDTLS_CHACHAPOLY_C	Defined
MBEDTLS_CTR_DRBG_C	Defined
MBEDTLS_DES_C	Defined
MBEDTLS_DHM_C	Defined
MBEDTLS_ECDH_C	Defined
MBEDTLS_ECDSA_C	Defined
MBEDTLS_ECP_C	Defined
MBEDTLS_ENTROPY_C	Defined
MBEDTLS_ERROR_C	Defined
MBEDTLS_GCM_C	Defined
MBEDTLS_HKDF_C	Defined
MBEDTLS_HMAC_DRBG_C	Defined
MBEDTLS_MD_C	Defined
MBEDTLS_MD5_C	Defined
MBEDTLS_NET_C	Defined
MBEDTLS_NIST_KW_C	Not Defined
MBEDTLS_OID_C	Defined
MBEDTLS_PADLOCK_C	Defined
MBEDTLS_PEM_PARSE_C	Defined
MBEDTLS_PEM_WRITE_C	Defined
MBEDTLS_PK_C	Defined
MBEDTLS_PK_PARSE_C	Defined
MBEDTLS_PK_WRITE_C	Defined
MBEDTLS_PKCS5_C	Defined
MBEDTLS_PKCS12_C	Defined
MBEDTLS_PLATFORM_C	Defined
MBEDTLS_RIPEMD160_C	Defined
MBEDTLS_POLY1305_C	Defined
MBEDTLS_RSA_C	Defined
MBEDTLS_SHA1_C	Defined
MBEDTLS_SHA256_C	Defined
MBEDTLS_SHA512_C	Defined
MBEDTLS_SSL_CACHE_C	Defined
MBEDTLS_SSL_COOKIE_C	Defined
MBEDTLS_SSL_TICKET_C	Defined
MBEDTLS_SSL_TLS_C	Defined
MBEDTLS_VERSION_C	Defined
MBEDTLS_X509_USE_C	Defined
MBEDTLS_X509_CRT_PARSE_C	Defined
MBEDTLS_X509_CRL_PARSE_C	Defined

MBEDTLS_X509_CSR_PARSE_C	Defined
MBEDTLS_X509_CREATE_C	Defined
MBEDTLS_X509_CRT_WRITE_C	Defined
MBEDTLS_X509_CSR_WRITE_C	Defined
MBEDTLS_XTEA_C	Defined

7.31.5. Modules Configuration:

7.32. USB_DEVICE
Class For FS IP: Download Firmware Update Class (DFU)
7.32.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING_DESC (Enable user string descriptor)	Enabled
USBD_SELF_POWERED (Enabled self power)	**Disabled ***
USBD_DEBUG_LEVEL (USBD Debug Level)	**2: User + Error messages ***
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USBD_DFU_MAX_ITF_NUM (DFU maximum interface numbers)	1
USBD_DFU_XFER_SIZE	1024
USBD_DFU_APP_DEFAULT_ADD (Base Address 0x)	**0x08000000 ***
USBD_DFU_MEDIA Interface	@Internal Flash /0x08000000/03*016Ka,01*016Kg,01*064Kg,07*128Kg,04*016Kg,01*064Kg,07*1

7.32.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	57105
PRODUCT_STRING (Product Identifier)	STM32 DownLoad Firmware Update

CONFIGURATION_STRING (Configuration Identifier)	DFU Config
INTERFACE_STRING (Interface Identifier)	DFU Interface

7.33. USB_HOST

Class For HS IP: Host Supporting ALL Classes

7.33.1. Parameter Settings:

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	5
USBH_MAX_NUM_INTERFACES (Maximun number of interfaces)	10
USBH_MAX_NUM_SUPPORTED_CLASS (Maximun number of supported class)	5
USBH_MAX_NUM_CONFIGURATION (Maximun number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximun size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximun size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	**2: User + Error messages ***

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS)	Enabled
USBH_PROCESS_PRIO (The CMSIS-RTOS osPriority value specifies the priority for the USB Host thread)	priority: normal (default)
USBH_PROCESS_STACK_SIZE (The CMSIS-RTOS stack size requirements in words)	128

7.33.2. Platform Settings:

Drive_VBUS_HS	PC0

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC3	PF3	ADC3_IN9	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PF3_ADC39
	PF4	ADC3_IN14	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PF4_ADC314
	PF5	ADC3_IN15	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PF5_ADC315
CAN1	PH13	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN_TX1
	PH14	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN_RX1
CAN2	PB13	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN_TX2
	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN_RX2
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	NC_DAC1
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	NC_DAC2
ETH	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_TXD1
	PB8	ETH_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_TXD3
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_TXD0
	PI10	ETH_RX_ER	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_RXER
	PC3	ETH_TX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_TXC
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_MDC
	PC2	ETH_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_TXD2
	PA1	ETH_RX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_RXC
	PA0/WKUP	ETH_CRS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_CRS
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_RXD0

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_MDIO
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_RXD1
	PA3	ETH_COL	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_COL
	PA7	ETH_RX_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_RXDV
	PB1	ETH_RXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_RXD3
	PB0	ETH_RXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_RXD2
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MII_TXEN
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	SDA2
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	SCL2
I2C3	PH7	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	TMPH3_PH7_SCL3_MISO5
	PH8	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	TMPH3_PH8_SDA3
I2C4	PF15	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	TMPH5_PF15_SDA4
	PF13	I2C4_SMBA	Alternate Function Open Drain	Pull-up	**Very High ***	TMPH5_PF13_SMBA4
	PF14	I2C4_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	TMPH5_PF14_SCL4
LPTIM1	PD13	LPTIM1_OUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	NC_LPTIM1
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	OSC32K_IN
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	OSC25M_IN
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI4	PE11	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	TMPH5_PE11_NSS4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH5_PE14_MOSI4
	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH5_PE12_SCK4
	PE13	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH5_PE13_MISO4
SPI5	PH5	SPI5_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH2_PH5_NSS5
	PF11	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH5_PF11_MOSI5
	PH6	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH3_PH6_SCK5
SYS	PB4	SYS_JTRST	n/a	n/a	n/a	JTAG_NTRST
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	JTAG_TDO_TRACE_SWO
	PA15	SYS_JTDI	n/a	n/a	n/a	JTAG_TDI
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	JTAG_TCK_SW_CLK
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	JTAG_TMS_SW_DIO
TIM8	PI2	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	TMPH1_PI2_PWM84
	PI5	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TMPH4_PI5_PWM81
	PI7	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TMPH4_PI7_PWM83
	PI6	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TMPH4_PI6_PWM82
UART4	PD0	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH1_PD0_RXD4
	PD1	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH1_PD1_TXD4
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH1_PC12_TXD5
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH1_PD2_RXD5
UART7	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	UART_TXD7
	PE9	UART7_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	UART_RTS7
	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	UART_RXD7

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PE10	UART7_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	UART_CTS7
UART8	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH4_PE1_TXD8
	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH4_PE0_RXD8
	PD15	UART8_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH2_PD15_RTS8
	PD14	UART8_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH2_PD14_CTS8
USART3	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH1_PC11_RXD3
	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	TMPH1_PC10_TXD3
USB_OTG_FS	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_DEV_DP
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_DEV_DM
USB_OTG_HS	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_HOST_DM
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	USB_HOST_DP
GPIO	PG15	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PG15
	PG11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USER_LED1
	PI4	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PI4
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USER_LED2
	PD3	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH1_PD3
	PI3	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH1_PI3
	PD4	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH1_PD4
	PH15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAN_M1
	PI1	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PI1
	PA10	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH1_PA10
	PI12	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PI12
	PI9	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH1_PI9
	PI0	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PI0
	PA9	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PA9
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAN_M2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF2	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PF2
	PI13	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PI13
	PI15	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PI15
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MII_NRST
	PF3	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PF3_ADC39
	PI14	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH4_PI14
	PG8	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PG8
	PC6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	MII_INTRP
	PF4	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PF4_ADC314
	PH3	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PH3
	PF5	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PF5_ADC315
	PH2	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PH2
	PD10	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH2_PD10
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NC_USB_HOST_VBUS
	PF12	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH5_PF12
	PG1	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH5_PG1
	PG3	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PG3
	PG2	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PG2
	PH12	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PH12
	PG0	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH5_PG0
	PG5	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PG5
	PG4	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PG4
	PH9	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PH9
	PH11	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PH11
	PH10	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH3_PH10
	PE15	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	TMPH5_PE15

8.2. DMA configuration

DMA request	Stream	Direction	Priority
UART7_RX	DMA1_Stream3	Peripheral To Memory	Low
UART7_TX	DMA1_Stream1	Memory To Peripheral	Low
ADC3	DMA2_Stream1	Peripheral To Memory	Low
TIM8_CH1	DMA2_Stream2	Peripheral To Memory	Low
TIM8_CH2	DMA2_Stream3	Peripheral To Memory	Low
TIM8_CH3	DMA2_Stream4	Peripheral To Memory	Low
TIM8_CH4/TRIG/COM	DMA2_Stream7	Peripheral To Memory	Low
UART8_RX	DMA1_Stream6	Peripheral To Memory	Low
UART8_TX	DMA1_Stream0	Memory To Peripheral	Low

UART7_RX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte
Peripheral Burst Size:	Single
Memory Burst Size:	Single

UART7_TX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte
Peripheral Burst Size:	Single
Memory Burst Size:	Single

ADC3: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

TIM8_CH1: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

TIM8_CH2: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

TIM8_CH3: DMA2_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***

FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

TIM8_CH4/TRIG/COM: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

UART8_RX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte
Peripheral Burst Size:	Single
Memory Burst Size:	Single

UART8_TX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte

Memory Data Width:	Byte
Peripheral Burst Size:	Single
Memory Burst Size:	Single

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RCC global interrupt	true	5	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
ADC1, ADC2 and ADC3 global interrupts	true	5	0
CAN1 TX interrupts	true	5	0
CAN1 RX0 interrupts	true	5	0
CAN1 RX1 interrupt	true	5	0
CAN1 SCE interrupt	true	5	0
I2C2 event interrupt	true	5	0
I2C2 error interrupt	true	5	0
USART3 global interrupt	true	5	0
RTC alarms (A and B) interrupt through EXTI line 17	true	5	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	5	0
TIM8 capture compare interrupt	true	5	0
UART4 global interrupt	true	5	0
UART5 global interrupt	true	5	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	5	0
DMA2 stream1 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
DMA2 stream3 global interrupt	true	5	0
DMA2 stream4 global interrupt	true	5	0
Ethernet global interrupt	true	5	0
CAN2 TX interrupts	true	5	0
CAN2 RX0 interrupts	true	5	0
CAN2 RX1 interrupt	true	5	0

Interrupt Table	Enable	Preenmption Priority	SubPriority
CAN2 SCE interrupt	true	5	0
USB On The Go FS global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
I2C3 event interrupt	true	5	0
I2C3 error interrupt	true	5	0
USB On The Go HS End Point 1 Out global interrupt	true	5	0
USB On The Go HS End Point 1 In global interrupt	true	5	0
USB On The Go HS global interrupt	true	5	0
CRYP global interrupt	true	5	0
HASH and RNG global interrupts	true	5	0
UART7 global interrupt	true	5	0
UART8 global interrupt	true	5	0
SPI4 global interrupt	true	5	0
SPI5 global interrupt	true	5	0
LPTIM1 global interrupt	true	5	0
I2C4 event interrupt	true	5	0
I2C4 error interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	true	true
RCC global interrupt	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
ADC1, ADC2 and ADC3 global interrupts	false	true	true
CAN1 TX interrupts	false	true	true
CAN1 RX0 interrupts	false	true	true
CAN1 RX1 interrupt	false	true	true
CAN1 SCE interrupt	false	true	true
I2C2 event interrupt	false	true	true
I2C2 error interrupt	false	true	true
USART3 global interrupt	false	true	true
RTC alarms (A and B) interrupt through EXTI line 17	false	true	true
TIM8 trigger and commutation interrupts and TIM14 global interrupt	false	true	true
TIM8 capture compare interrupt	false	true	true
UART4 global interrupt	false	true	true
UART5 global interrupt	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true
DMA2 stream1 global interrupt	false	true	true
DMA2 stream2 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true
DMA2 stream4 global interrupt	false	true	true
Ethernet global interrupt	false	true	true
CAN2 TX interrupts	false	true	true
CAN2 RX0 interrupts	false	true	true
CAN2 RX1 interrupt	false	true	true
CAN2 SCE interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true
DMA2 stream7 global interrupt	false	true	true
I2C3 event interrupt	false	true	true
I2C3 error interrupt	false	true	true
USB On The Go HS End Point 1 Out global interrupt	false	true	true
USB On The Go HS End Point 1 In global interrupt	false	true	true
USB On The Go HS global interrupt	false	true	true
CRYP global interrupt	false	true	true
HASH and RNG global interrupts	false	true	true

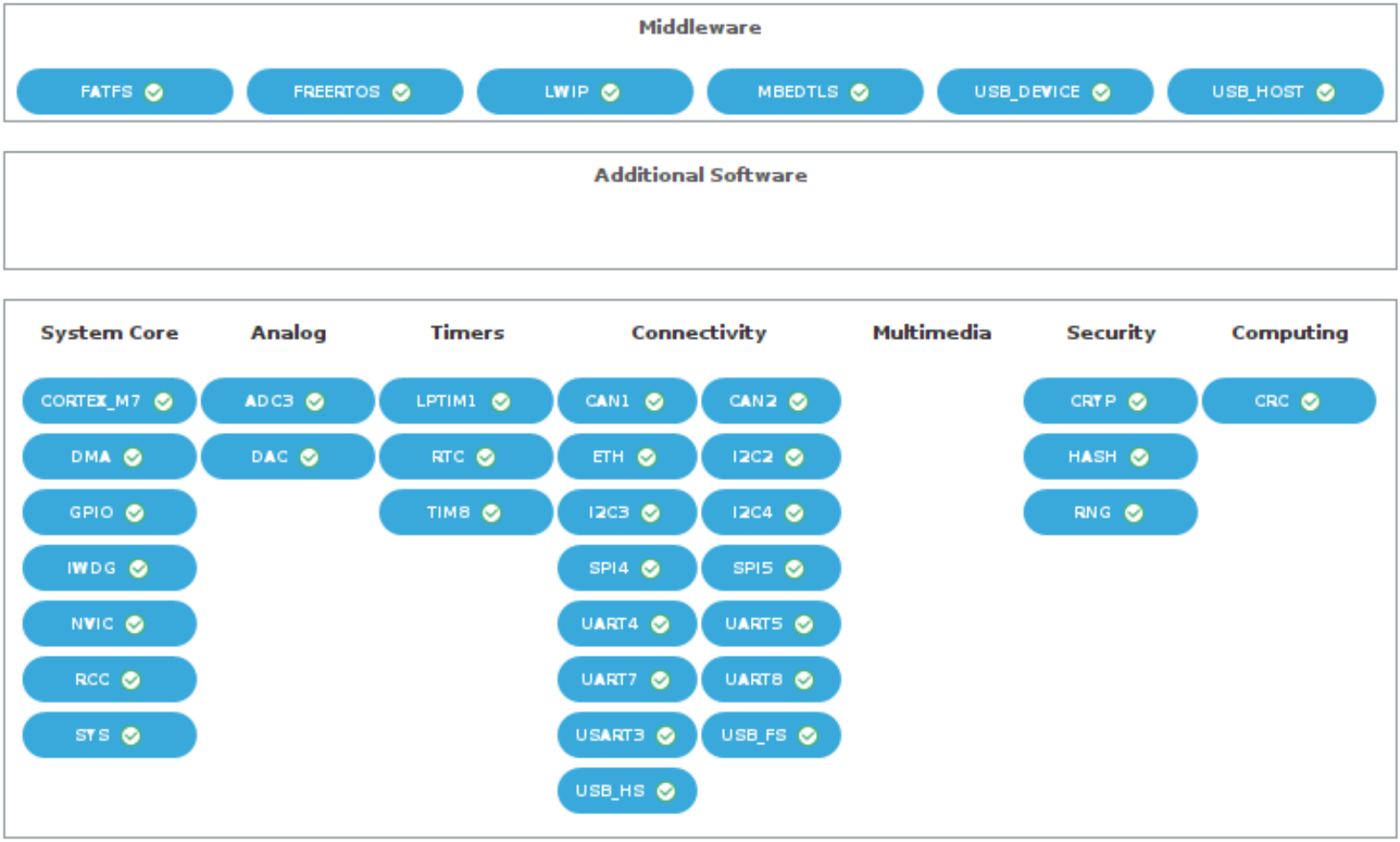
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
UART7 global interrupt	false	true	true
UART8 global interrupt	false	true	true
SPI4 global interrupt	false	true	true
SPI5 global interrupt	false	true	true
LPTIM1 global interrupt	false	true	true
I2C4 event interrupt	false	true	true
I2C4 error interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
RoweBots	I-CUBE-UNISONRTOS	5.5.0-4	Class : RTOS Group : KERNEL Version : 1.7.2 Class : RTOS Group : CMSIS Version : 1.7.2 Class : Device Group : Application Variant : simple Version : 1.0.0
wolfSSL	I-CUBE-wolfSSL	4.7.0	Class : wolfSSL Group : wolfSSL SubGroup : Core Version : 4.7.0 Class : wolfSSL Group : wolfCrypt SubGroup : Core Version : 4.7.0 Class : wolfSSL Group : wolfCrypt SubGroup : Test Version : 4.7.0

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00225424.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00224583.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00257543.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164549.pdf
Application note	http://www.st.com/resource/en/application_note/DM00173083.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210367.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf

Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf