Operation Mode For Non User

By GAO

## Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| **Version** | **Date** | **Author** | **Description** |
| 0.1 | May 12 | **GAO** | **Initial** |
| **0.2** | **May 14** | **GAO** | **Update IRC Trim** |
| **0.3** | **May 21** | **GAO** | 1. **Change the Mis-Match command to 8’h10101011** 2. **Remove the IRC\_TRIM\_END command** 3. **Add the OTP operation end command** 4. **Add OPCODE PROGRAM command** |
| **0.4** | **June 15** | **GAO** | **Define IRC4K TRIM CODE and IRC1K TRIM Code to 6bits respectively by MSB of otp\_dout[7:0]**  **1: IRC4M trim code**  **0: IRC1K trim code** |
| **0.5** | **July 3** | **GAO** | 1. **Change P50 as IRC1K Clock Output** 2. **Change P51 as IRC4M Clock Output** 3. **Change the section 1.4.5 for IRC1K and IRC 4M clock** |
| **0.6** | **July 24** | **GAO** | 1. **Add register Summary** |
| **0.7** | **July 26** | **GAO** | 1. **Refine the next operation description** |
|  |  |  |  |

## Reference Doc

1. **OTP Macro Test Methodology Version 1.3**
2. **SC201 Reference Manual Version 1.0 (Later prepared)**

## **Description**

The operation mode for non-user major includes two points: one is for OTP, the another is for IRC trimming.

The OTP operation includes test and normal operation modes, The test modes includes OTP margin-1 read, OTP margin-2 read, OTP off-state margin read. The normal operation modes include OTP program, OTP read.

Only Type-II in **OTP Macro Test Methodology** is used for OTP mass production test, all instructions for Type-II are supported in design, but it will be to be decided later for final test methodology.

The IRC trimming includes two steps, the first one is to find the best trim code for accurate IRC frequency, The 2nd step is to write the best trim code into the 1038 or 1037 (from 0) byte of OTP for auto load in user mode during reset.

These operations to OTP and IRC are encoded into different command types, the UART is used for communication between SC201 and external controller on PCB or external Desktop. The external 12Mhz external crystal is a must for accurate the baud rate of UART for all non-user operations. So the pin assignment in non-user mode is different with the user mode.

### Pin Configuration for non-user modes

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** | **Name** | **User Mode** | **Non-User Mode** | **Comment** |
| 1 | VDD | Power Supply | 5V/3.3V | For 5V and 3V device respectively |
| 2 | P65/OSCI | IO or crystal clock input | 12Mhz crystal clock In |  |
| 3 | P64/OSCO | IO or Crystal Clock  Output | 12Mhz Crystal Clock  Output |  |
| 4 | P63/RST/VPP | Input or external Reset | VPP: 7.35V or 7.6V | Mode Entry or OTP program |
| 5 | P67 | IO | Same as user mode |  |
| 6 | P50 | IO | 1K IRC Clock Output |  |
| 7 | P51 | IO | 4M IRC clock Output |  |
| 8 | P52 | IO | Same as user mode |  |
| 9 | P53 | IO | Same as user mode |  |
| 10 | P66 | IO | Same as user mode |  |
| 11 | P62/TCC | IO | Same as user mode |  |
| 12 | P61 | IO | TX | 38.4K baud rate |
| 13 | P60/INT | IO | RX | 38.4K baud rate |
| 14 | VSS | Power Ground | Same as user mode |  |

### Mode Entry

The always applied 7.35V or 7.6V voltage on VPP pad in non-user modes (100mV internal IR Drop) trig internal vpp\_high signal to logic high

### Command Type and Code

|  |  |  |
| --- | --- | --- |
| Operation | Code | Comment |
| OTP Program with VPP\_Lo, Vdd\_std | 8’b1010\_0001 | OTP: VPP=VPP\_Lo, VDD = Vdd\_std |
| OTP Program with VPP\_std, Vdd\_std | 8’b1010\_0010 | OTP: VPP=VPP\_std, VDD = Vdd\_std |
| User Mode OTP Read with Vdd\_Lo | 8’b1010\_0011 | OTP: VPP=Vdd\_Lo, VDD = Vdd\_Lo |
| User Mode OTP Read with Vdd\_Hi | 8’b1010\_0100 | OTP: VPP=Vdd\_Hi, VDD = Vdd\_Hi |
| Test Mode OTP Margin-1 Read with Vdd\_std | 8’b1010\_0101 | OTP: VPP=Vdd\_std, VDD = Vdd\_std |
| Test Mode OTP Margin-2 Read with Vdd\_std | 8’b1010\_0110 | OTP: VPP=Vdd\_std, VDD = Vdd\_std |
| Test Mode OTP off-state Margin Read with Vdd\_std | 8’b1010\_0111 | OTP: VPP=Vdd\_std, VDD = Vdd\_std |
| IRC Trim Code | 8’b1010\_1000 | OTP: VPP=Vdd\_std, VDD = Vdd\_std  Indicate the following data will be trim code |
| Program IRC Trim Code (Last Byte of OTP) with VPP\_std, Vdd\_std | 8’b1010\_1010 | OTP: VPP=VPP\_std, VDD = Vdd\_std |
|  |  |  |
| Data Match | 8’b1010\_1100 | Received data is same as transmitted |
| Data Mis-match | 8’b1010\_1011 | Received data is diff with transmitted |
| PROGRAM SCR | 8’b1010\_1101 | Program opcode |
| OTP Operation End | 8’b1010\_1111 | all operation end |

Note: VPP\_Lo=7.25V, VPP\_std =7.5V,

Vdd\_Lo=2V, Vdd\_std=3.3V, Vdd\_Hi=3.6V

### Communication Protocol

The physical layer protocol is general uart protocol, its configuration and operation can be found in DW8051 doc.

In order to improve the reliability, all data transaction are confirmed by shakehand, The transmitter send the data to slave, then the slave send the received data back to transmitter, The transmitter compare the received data from slave, then send the data match or mismatch code to slave, the transmitter will re-send the last data after sending the data mis-match code, else it will send the next data after send the data match code

The transmitter always initiates the data transaction, compares the original data with received data, and send data match or mismatch command, re-send the data or send next data

The slave (receiver) always receives and sends back the data.

After completion of current transaction, the internal controller will be started from test code again.

### Sequence and Direction For Data Match

|  |  |  |  |
| --- | --- | --- | --- |
| Data-1 | Received data | Data-Match command | Data-2 |
| Transmitter to slave | slave to Transmitter | Transmitter to slave | Transmitter to slave |

### Sequence and Direction For Data Mismatch

|  |  |  |  |
| --- | --- | --- | --- |
| Data-1 | Received data | Data-Mismatch command | Data-1 (re-send) |
| Transmitter to slave | slave to Transmitter | Transmitter to slave | Transmitter to slave |

There are a few types data transmitted: test code, command code, program code, IRC trim code.

The test code is dedicated to 8’h55, 8’haa in sequence, it is used to test if the connection is ready, After 100us from 7.5V applied on VPP, the transmitter can start to send the test code to SC201. In case of 8’h55 can be transferred successfully, but failed in 8’haa, then it is required to restart test code from 8’h55.

After test code, the following transmission is command codes, which indicate what it will do in next step, the next command can be transacted when last command execution is end without test code re-transaction, non-user operations are described as following.

### OTP Program

|  |  |  |
| --- | --- | --- |
| Test Code | OTP Program Command(8’ha1 or 8’ha2) | 10bits-Begin Address(8bits per byte) |
| 10bits-Program Length in Byte (8bits per byte) | | Program Code |

In OTP program, The external controller is transmitter, The SC201 is slave or receiver.

The 10bits begin address define the starting location of program code, 10bits program length define the how many bytes which will be programmed into OTP in current program operation. The program code is 8bits data which user want to program.

After completion of current length transaction, the next transaction operation will be started from test code.

### OTP Read

|  |  |  |
| --- | --- | --- |
| Test Code | OTP Read Command(8’ha3 to 8’ha7) | Begin Address |
| Read Length in Byte (8bits per byte) | | Program Code in OTP |

In OTP read, The external controller is transmitter in command, address, length transaction, The SC201 is transmitter in program code transaction from OTP to external.

The 10bits begin address define the starting location of reakback, 10bits read length define the how many bytes which will be readback from OTP in current read operation. The program code is 8bits data which user want to readback.

After completion of current length transaction, the next transaction operation will be started from test code.

### IRC Trim Code

|  |  |  |  |
| --- | --- | --- | --- |
| Test Code | IRC Trim Code command (8’ha8) | Trim Code-1 | |
| Test Code | IRC Trim Code command (8’ha8) | Trim Code-2 |  |

In IRC trim code, The external controller is transmitter, The SC201 is slave or receiver,

The MSB of trim code is to indicate IRC1K or IRC4M trim

0: The trim code is for IRC1K oscillator

1: The trim code is for IRC4M oscillator

Any one trim code transaction will start from test code

### Program IRC Trim Code

|  |  |  |
| --- | --- | --- |
| Test Code | Program IRC Trim Code command (8’haa) | One byte Trim Code |

In OTP program, The external controller is transmitter, The SC201 is slave or receiver.

### Program SCR

|  |  |  |
| --- | --- | --- |
| Test Code | Program SCR Command(8’had) | One byte SCR |

In OTP program, The external controller is transmitter, The SC201 is slave or receiver.

### Register Summary

**SCR**: **System Configuration Register, Address is ‘d1039**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | RESET | WDGE | CLK2 | CLK1 | CS | SUT1 | SUT0 | RCOUT |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | Read Only | | | | | | | |

|  |  |  |
| --- | --- | --- |
| 7 | RESET | Reset function enable or disable on P63 pin  1: P63 is not a reset pin  0: P63 is a reset pin |
| 6 | WDGE | Watch Dog module enable or disable from power on or recover from LVD reset  1: Watchdog is enabled  0: Watchdog is disabled |
| 5:4 | CLK[2:1] | System clock configuration  2’b00: LXT, Crystal oscillator low frequency mode,32Khz-1Mhz  2’b01: HXT, Crystal oscillator high frequency mode, 1Mhz-14Mhz  2’b10: ERC, External RC oscillator  2’b11: IRC, Internal RC 4Mhz oscillator |
| 3 | CS | Chip Security for preventing un-authorization read  1: Program in OTP is protected for read  0: Program in OTP is free for read |
| 2:1 | SUT[1:0] | Crystal Start Up time configuration  2’b00: 18ms  2’b01: 36ms  2’b10: 4.5ms  2’b11: 72ms |
| 0 | RCOUT | OSCO/P64 function selection  1:OSCO function is selected  0: P64 as general purpose IO is selected |
|  |  |  |

**IRC4MTRIM**: **4MHZ IRC TRIMMING Register, The address is ‘d1038**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | Reserved | | IRC4MTRIM | | | | | |
| Default |  |  | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | Read Only | | | | | | | |

|  |  |  |
| --- | --- | --- |
| 7:6 |  | Reserved |
| 5:0 | IRC4MTRIM[5:0] | IRC4MHZ clock trimming |

**IRC1KTRIM**: **1KHZ IRC TRIMMING Register, The address is ‘d1037**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | Reserved | | IRC1KTRIM | | | | | |
| Default |  |  | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | Read Only | | | | | | | |

|  |  |  |
| --- | --- | --- |
| 7:6 |  | Reserved |
| 5:0 | IRC1KTRIM[5:0] | IRC1KHZ clock trimming |