Counters

Laboratory Assignment 10
ECE 201: Digital Circuits and Systems

Learning Objectives

After completing this lab, you will be able to

- design a counter using flip-flops
- describe sequential logic circuits using a HDL
- implement a sequential logic circuit on a FPGA and utilize clocking resources on a FPGA development board.

Equipment and Materials

- DE10-Lite Board
- Intel Quartus Prime Design Software v15.1

Pre-Lab Assignment

Prior to attending your assigned laboratory section, complete the following tasks

- Sketch the schematic for the 8-bit synchronous counter that you will design in part 1
- Read section 3.2 of the DE10-Lite User Manual . This section explains how to use the internal clocking circuitry on the DE-series board

Part I: Design of Synchronous Counters Using Flip-Flops

Consider the circuit in Figure 1. It is a 4-bit synchronous counter which uses four T-type flip-flops. The counter increments its value on each positive edge of the clock signal if the *Enable* signal is high. The counter is reset to 0 on the next positive clock edge if the synchronous *Clear* input is low. You are to implement an 8-bit counter of this type.

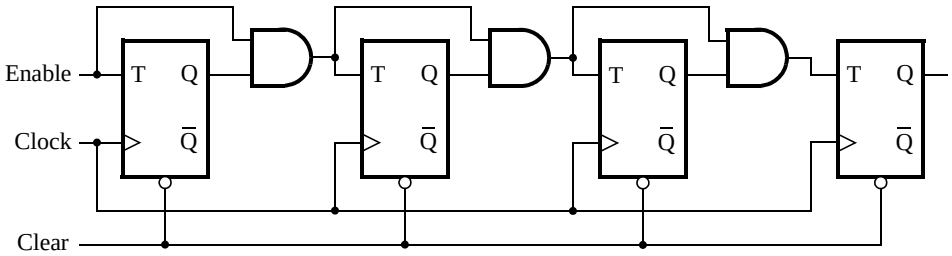

Figure 1: A 4-bit counter.

1. Write a VHDL file that defines an 8-bit counter by using the structure depicted in Figure 1. Your code should include a T flip-flop entity that is instantiated eight times to create the counter. Compile the circuit. How many logic elements (LEs) are used to implement your circuit?
2. Simulate your circuit to verify its correctness.
3. Augment your VHDL file to use the pushbutton KEY_0 as the *Clock* input and switches SW_1 and SW_0 as *Enable* and *Clear* inputs, and 7-segment displays *HEX1-0* to display the hexadecimal count as your circuit operates. Make the necessary pin assignments needed to implement the circuit on your DE-series board, and compile the circuit.
4. Download your circuit into the FPGA chip and test its functionality by operating the switches.

Part II: Design of Synchronous Counters Using Behavioral HDL

Another way to specify a counter is by using a register and adding 1 to its value. This can be accomplished using the following VHDL statement:

$$Q <= Q + 1;$$

Compile a 16-bit version of this counter. Implement the counter on your DE-series board, using the displays *HEX3-0* to show the counter value.

Part III: Clocking Circuitry

Design and implement a circuit that successively flashes digits 0 through 9 on the 7-segment display *HEX0*. Each digit should be displayed for about one second. Use a counter to determine the one-second intervals. The counter should be incremented by the 50-MHz clock signal provided on the DE-series boards. Do not derive any other clock signals in your design–make sure that all flip-flops in your circuit are clocked directly by the 50-MHz clock signal. A partial design of the required circuit is shown in Figure 2. The figure shows how a large bit-width counter can be used to produce an enable signal for a smaller counter. The rate at which the smaller counter increments can be controlled by choosing an appropriate number of bits in the larger counter.

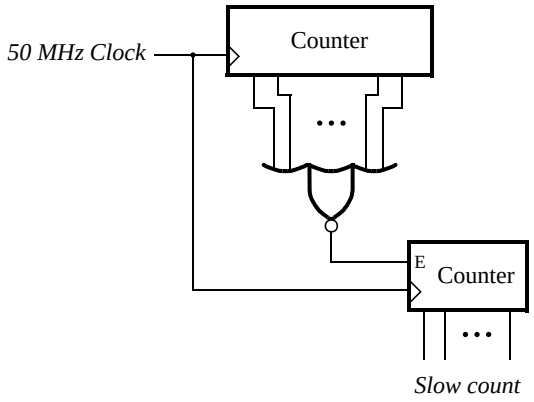

Figure 2: Making a slow counter.

Part IV: Rotating Word Display

Design and implement a circuit that displays a word with four letters on four 7-segment displays $HEX3-0$. There are many ways to design the required circuit. One solution is to re-use the VHDL code designed in Laboratory Exercise 1, Part V. Using that code, the main change needed is to replace the two switches that are used to select the characters being rotated on the displays with a 2-bit counter that increments at one-second intervals.

Count	Characters			
00	d	E	1	0
01	E	1	0	d
10	1	0	d	E
11	0	d	E	1

Table 1: Example rotating the word "dE10" on four displays.

Part V: Augmenting the Rotating Display

Augment your circuit from Part IV so that it can rotate the word over all of the 7-segment displays on your DE-series board. The shifting pattern for the DE10-Lite is shown in Table 2.

Count	Character pattern					
000			d	E	1	0
001		d	E	1	0	
010	d	E	1	0		
011	E	1	0			d
100	1	0			d	E
101	0			d	E	1

Table 2: Rotating the word dE10 on six displays.