1. Description

1.1. Project

Project Name	f4interpolatortest
Board Name	STM32F4DISCOVERY
Generated with:	STM32CubeMX 4.22.0
Date	09/14/2017

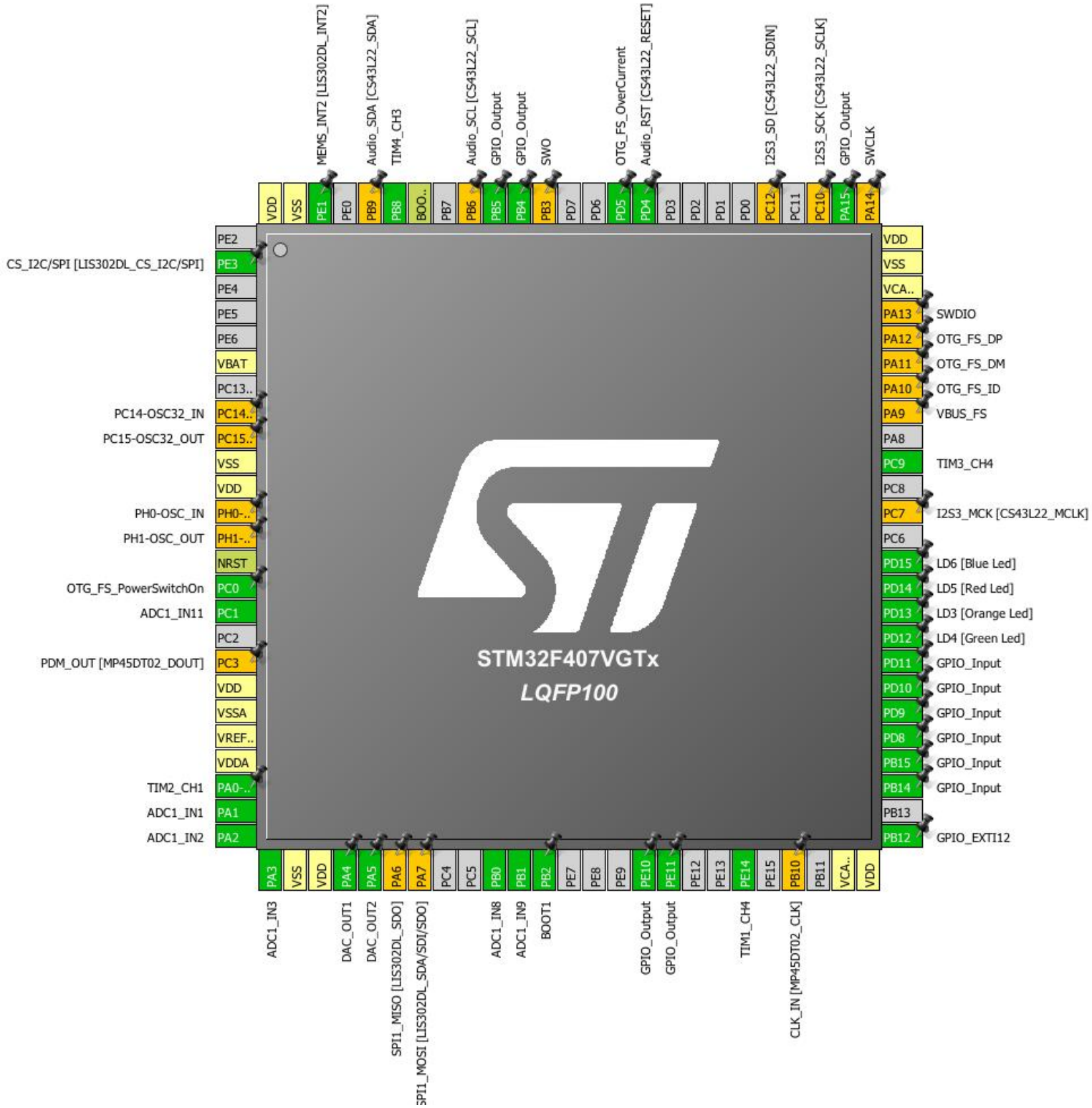
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Caution

The report was generated although the configuration was in a modified state. It may be not accurate

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3 *	I/O	GPIO_Output	CS_I2C/SPI [LIS302DL_CS_I2C/SPI]
6	VBAT	Power		
8	PC14-OSC32_IN **	I/O	RCC_OSC32_IN	PC14-OSC32_IN
9	PC15-OSC32_OUT **	I/O	RCC_OSC32_OUT	PC15-OSC32_OUT
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN **	I/O	RCC_OSC_IN	PH0-OSC_IN
13	PH1-OSC_OUT **	I/O	RCC_OSC_OUT	PH1-OSC_OUT
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	OTG_FS_PowerSwitchOn
16	PC1	I/O	ADC1_IN11	
18	PC3 **	I/O	I2S2_SD	PDM_OUT [MP45DT02_DOUT]
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM2_CH1	
24	PA1	I/O	ADC1_IN1	
25	PA2	I/O	ADC1_IN2	
26	PA3	I/O	ADC1_IN3	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	DAC_OUT1	
30	PA5	I/O	DAC_OUT2	
31	PA6 **	I/O	SPI1_MISO	SPI1_MISO [LIS302DL_SDO]
32	PA7 **	I/O	SPI1_MOSI	SPI1_MOSI [LIS302DL_SDA/SDI/SDO]
35	PB0	I/O	ADC1_IN8	
36	PB1	I/O	ADC1_IN9	
37	PB2 *	I/O	GPIO_Input	BOOT1
41	PE10 *	I/O	GPIO_Output	
42	PE11 *	I/O	GPIO_Output	
45	PE14	I/O	TIM1_CH4	

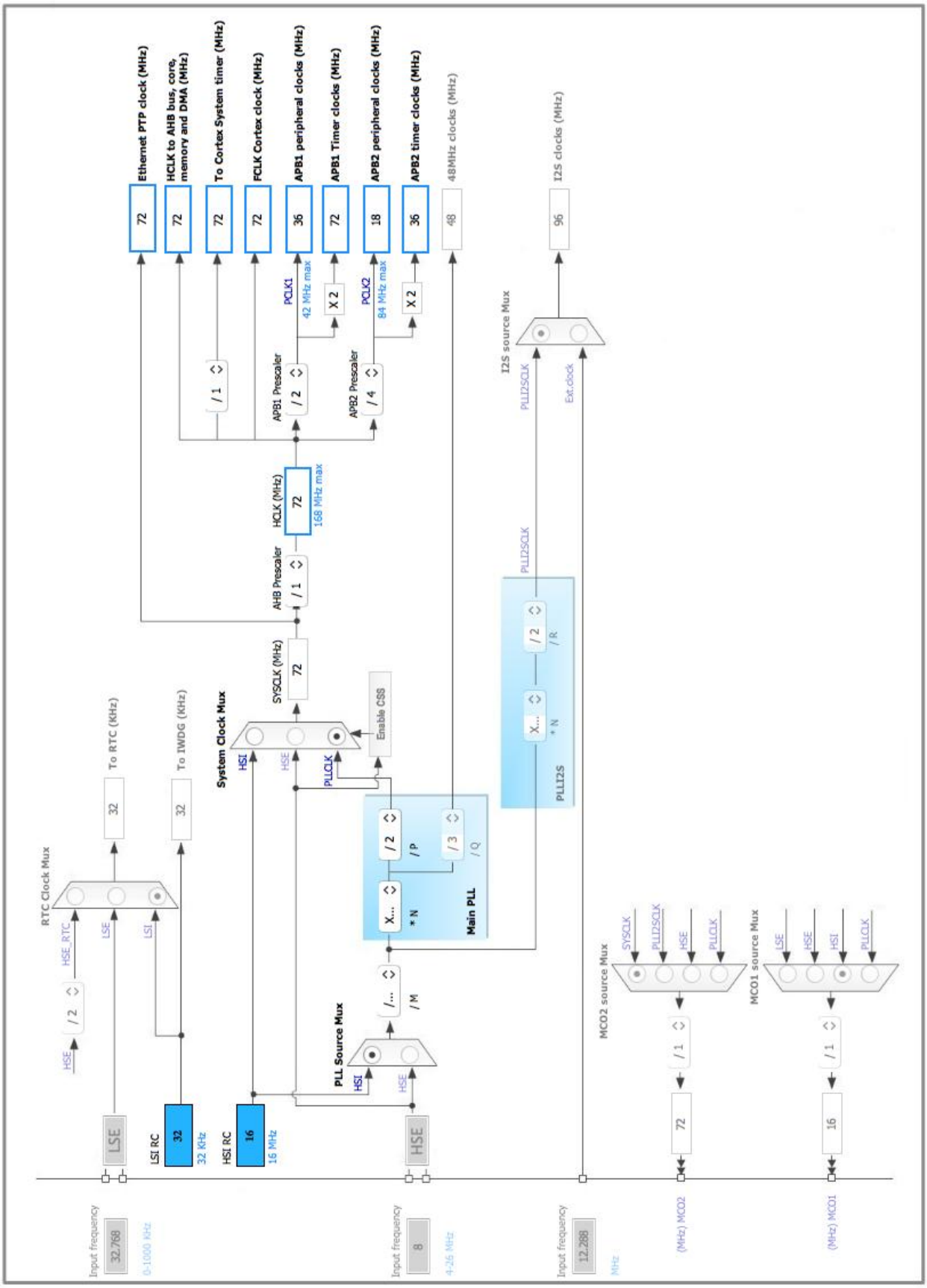
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
47	PB10 **	I/O	I2S2_CK	CLK_IN [MP45DT02_CLK]
49	VCAP_1	Power		
50	VDD	Power		
51	PB12	I/O	GPIO_EXTI12	
53	PB14 *	I/O	GPIO_Input	
54	PB15 *	I/O	GPIO_Input	
55	PD8 *	I/O	GPIO_Input	
56	PD9 *	I/O	GPIO_Input	
57	PD10 *	I/O	GPIO_Input	
58	PD11 *	I/O	GPIO_Input	
59	PD12 *	I/O	GPIO_Output	LD4 [Green Led]
60	PD13 *	I/O	GPIO_Output	LD3 [Orange Led]
61	PD14 *	I/O	GPIO_Output	LD5 [Red Led]
62	PD15 *	I/O	GPIO_Output	LD6 [Blue Led]
64	PC7 **	I/O	I2S3_MCK	I2S3_MCK [CS43L22_MCLK]
66	PC9	I/O	TIM3_CH4	
68	PA9 **	I/O	USB_OTG_FS_VBUS	VBUS_FS
69	PA10 **	I/O	USB_OTG_FS_ID	OTG_FS_ID
70	PA11 **	I/O	USB_OTG_FS_DM	OTG_FS_DM
71	PA12 **	I/O	USB_OTG_FS_DP	OTG_FS_DP
72	PA13 **	I/O	SYS_JTMS-SWDIO	SWDIO
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 **	I/O	SYS_JTCK-SWCLK	SWCLK
77	PA15 *	I/O	GPIO_Output	
78	PC10 **	I/O	I2S3_CK	I2S3_SCK [CS43L22_SCLK]
80	PC12 **	I/O	I2S3_SD	I2S3_SD [CS43L22_SDIN]
85	PD4 *	I/O	GPIO_Output	Audio_RST [CS43L22_RESET]
86	PD5 *	I/O	GPIO_Input	OTG_FS_OverCurrent
89	PB3 **	I/O	SYS_JTDO-SWO	SWO
90	PB4 *	I/O	GPIO_Output	
91	PB5 *	I/O	GPIO_Output	
92	PB6 **	I/O	I2C1_SCL	Audio_SCL [CS43L22_SCL]
94	BOOT0	Boot		
95	PB8	I/O	TIM4_CH3	
96	PB9 **	I/O	I2C1_SDA	Audio_SDA [CS43L22_SDA]

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
98	PE1	I/O	GPIO_EXTI1	MEMS_INT2 [LIS302DL_INT2]
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN1

mode: IN2

mode: IN3

mode: IN8

mode: IN9

mode: IN11

5.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion
ADC_Regular_ConversionMode:	
Number Of Conversion	**6 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**56 Cycles ***
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**56 Cycles ***
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**56 Cycles ***

Rank	**4 ***
Channel	**Channel 8 ***
Sampling Time	**56 Cycles ***
Rank	**5 ***
Channel	**Channel 9 ***
Sampling Time	**56 Cycles ***
Rank	**6 ***
Channel	**Channel 11 ***
Sampling Time	**56 Cycles ***
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

5.2. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

5.2.1. Parameter Settings:

DAC Out1 Settings:	
Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled
DAC Out2 Settings:	
Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

5.3. SYS

Timebase Source: SysTick

5.4. TIM1

Channel4: PWM Generation CH4

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**15-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4096 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.5. TIM2

Channel1: Input Capture direct mode

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.6. TIM3

Channel4: PWM Generation CH4

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4096 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4096 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.7. TIM4

Channel3: PWM Generation CH3

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**15-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4096 ***

Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.8. TIM6

mode: Activated

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1-1
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
TIM1	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	PC14-OSC32_IN
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	PC15-OSC32_OUT
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-OSC_IN
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-OSC_OUT
	PC3	I2S2_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	PDM_OUT [MP45DT02_DOUT]
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_MISO [LIS302DL_SDO]
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_MOSI [LIS302DL_SDA/SDI/SDO]
	PB10	I2S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	CLK_IN [MP45DT02_CLK]
	PC7	I2S3_MCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S3_MCK [CS43L22_MCLK]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	VBUS_FS
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_ID
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_DM

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_DP
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PC10	I2S3_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S3_SCK [CS43L22_SCLK]
	PC12	I2S3_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S3_SD [CS43L22_SDIN]
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Low	Audio_SCL [CS43L22_SCL]
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Low	Audio_SDA [CS43L22_SDA]
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_I2C/SPI [LIS302DL_CS_I2C/SPI]
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OTG_FS_PowerSwitchOn
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD8	GPIO_Input	Input mode	**Pull-up ***	n/a	
	PD9	GPIO_Input	Input mode	**Pull-up ***	n/a	
	PD10	GPIO_Input	Input mode	**Pull-up ***	n/a	
	PD11	GPIO_Input	Input mode	**Pull-up ***	n/a	
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD4 [Green Led]
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Orange Led]
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD5 [Red Led]
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD6 [Blue Led]
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Audio_RST [CS43L22_RESET]
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OTG_FS_OverCurrent
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE1	GPIO_EXTI1	**External Event Mode with Rising edge**	No pull-up and no pull-down	n/a	MEMS_INT2 [LIS302DL_INT2]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			trigger detection *			

6.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC1	DMA1_Stream5	Memory To Peripheral	**Very High ***
DAC2	DMA1_Stream6	Memory To Peripheral	**Very High ***
ADC1	DMA2_Stream0	Peripheral To Memory	**Medium ***

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

DAC2: DMA1_Stream6 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream5 global interrupt	true	1	0
DMA1 stream6 global interrupt	true	1	0
TIM2 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	1	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
DMA2 stream0 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	022152_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	f4interpolatortest
Project Folder	/Users/willmitchell/Documents/stm32 workspace/f4interpolatortest
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No