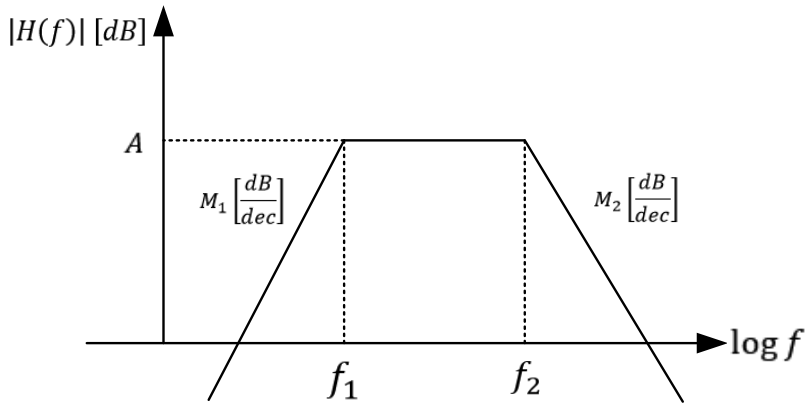
PSPICE PROJECT

You will design an amplifier according to the following specifications.

The values of some of the specs depend on your ID numbers: You need to sum the 2 ID numbers and use the 9 right side digits defined as: ABCDEFGHI.

For example: if the sum of your 2 IDs is 1380245793, so the 9 right side digits are 380245793 when A is 3, B is 8, etc.

The transfer function of your amplifier should look like so:



Where the specs are determined by your IDs:

$A = (35 + 2 \cdot D)\ [dB]$

$f_1 = (G + H)\ [kHz]$

$f_2 = (G + H) \cdot 100[kHz]$

if C is odd : $M_1 = 20\left[\frac{dB}{dec}\right], M_2 = -40\left[\frac{dB}{dec}\right]$

if C is even : $M_1 = 40\left[\frac{dB}{dec}\right], M_2 = -20\left[\frac{dB}{dec}\right]$

The amplifier input and output resistances should be:

$R_{out} = 10 + F[\text{k}\Omega]$ if F is odd

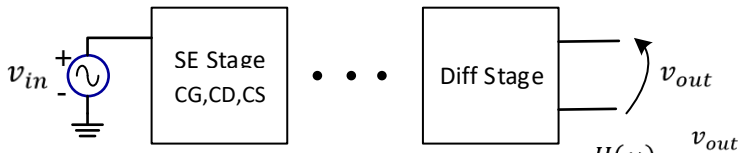
$R_{out} = 5 + F[k\Omega]$ if F is even

** **Notice that if your output is differential than you must connect your test source between the 2 outputs!**

The requirements should be met within $0.01f_1 \leq f \leq 100f_2$

Your amplifier schematic will be defined as follows:

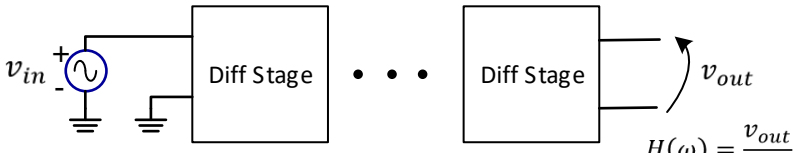
If A and D are both odd:



Input: Single Ended, Output: Differential

$$H(\omega) = \frac{v_{out}}{v_{in}}$$

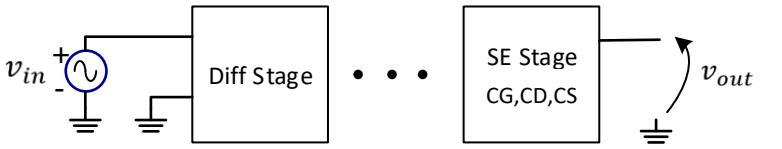
If A and D are both even:



Input: Differential, Output: Differential

$$H(\omega) = \frac{v_{out}}{v_{in}}$$

If for A and D one is even and the other is odd:



Input: Differential, Output: Single Ended

$$H(\omega) = \frac{v_{out}}{v_{in}}$$

Components

Use only MbreakN, MbreakP transistors with $K_P = \frac{1mA}{V^2}, |V_{TH}| = 0.5V, \lambda = 0$

No DC sources are allowed except the V_{DD}***!***

*** ***Notice that*** V_{TH} ***of PMOS must be defined as negative.***

Design limitations

1. The sum of used resistances should not go over 5MΩ.
2. The sum of used capacitances should not go over 1mF.
3. Supply voltage are 5V.
4. The tolerance of all required specs is 5% (5% from linear gain and not dB gain)
5. You can use as many amplification stages as you want.
6. DC power dissipation should not go over 0.1W.

Submission requirements

1. Show your IDs and summation in a table.
2. Explain the following:
   A. The reason behind using every stage and its purpose.
   B. Bias point and small signal considerations for every stage.
3. Analyze the amplifiers bias point operation and validate them with simulations.
4. Analyze the amplifiers small signal operation and validate them with simulations.
5. Show the Bode plot of the amplifier with data points for slopes, gain and 3-dB frequencies.
6. Show the input and output resistance vs. frequency.

- Submission is in pairs only!
- The submission deadline is the moed A exam 05/07/23

- You will submit a zip file with all submission requirements in the designated section in the course moodle that includes a PDF document and the PSPICE files (Files that can be used to open your design).
- The file name should be: First_name1_last_name1_ID1_ First_name2_last_name2_ID2
- The PDF documents should be clean, **not hand -written (including iPad)** and well-organized. A messy submission will lose points.