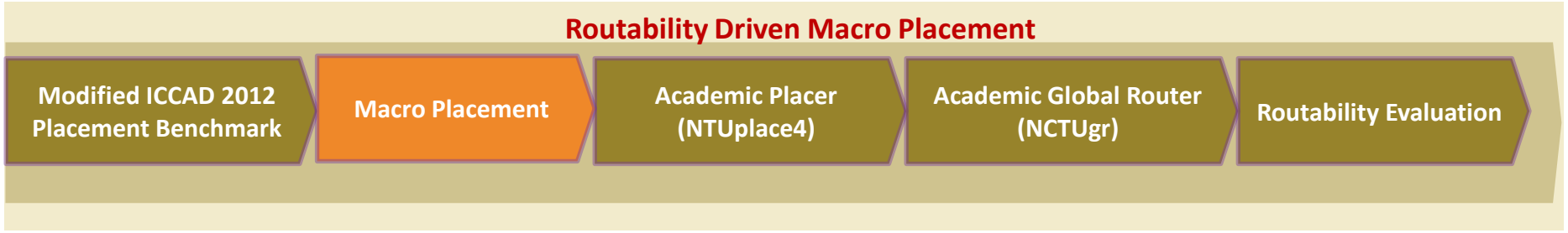
Benchmark Description

Contest Flow



✓ **Evaluation flow**

- Academic placer using NTUplace3
- Academic router using NCTUgr
- Routability evaluation using script provided by IBM in 2012 ICCAD CAD Contest.

✓ **What are the weakness of current mixed size placement solution?**

- Macro placement significantly impact subsequent timing, design rule violations, routability and chip area which are not handled properly using current mixed size placement solution.
- Macro placement relies on knowledge of dataflow in which current macro placement has lots of room for improvement.

MEDIATEK

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2015 ICCAD Contest

INPUT BENCHMARK FORMAT

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Overview of Benchmark Files

- ✓ **Modifications made from MMS Benchmark**
  - Add .route file
  - Reset macro locations

- ✓ **The benchmark format comprise of the following files**
  - circuit.aux
  - circuit.node **(describe movetype, width and height of nodes)**
  - circuit.nets **(describe connection behavior of nodes)**
  - circuit.wts **(contestant can ignore this file, necessary standard format)**
  - circuit.pl **(describe initial location of nodes)**
  - circuit.scl **(will be automatically generated based on input placement file)**
  - circuit.shapes **(contestant can ignore this file, necessary standard format)**
  - circuit.route **(will be automatically generated based on input placement file)**

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Circuit.aux

- ✓ **Auxiliary file listing all the files that describe/specify the benchmark**
- ✓ **The macro placer should parse the files listed in the "circuit.aux" file to get the benchmark information**
  - In this contest, circuit.wts will have 0 nets and circuit.shapes will have 0 shapes
- ✓ **Single line giving all the file names**

An example of Circuit.aux

```
RowBasedPlacement : circuit.nodes circuit.nets circuit.wts circuit.pl circuit.scl circuit.shapes circuit.route
```


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Circuit.nodes

- ✓ **For each node in the design, it specifies**
  - Design hierarchy based name
  - Dimension (width and height)
  - Movetype
- ✓ **The nodes can have one of two move types**
  - movable : these nodes can be arbitrary moved by placer
  - fixed node : macro placer needs to obtain the location of these nodes
- ✓ **If a line does not specify a move type, the associated node is a movable node**

An example of circuit.nodes

```
UCLA nodes 1.0
# File header with version information, etc.
# Anything following # is a comment and should be ignored

NumNodes        :  4                          # Total Number of nodes (movable + fixed)
NumTerminals    :  2                          # Number of fixed nodes

    o0          12          12                # Movable node with width = 4, height = 9
    o1           6          12
    o2           6          12
    o3          12          24      terminal  # Macro block with width = 12, height = 24
    o4          15          27      terminal  # Macro block with width = 12, height = 24
```


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Circuit.nets

- ✓ **Specifies the circuit netlist – the set of nets or connections in the hypergraph**
- ✓ **The macro placer should parse the files listed in the "circuit.aux" file to get the benchmark information**
  - In this contest, circuit.wts will have 0 nets and circuit.shapes will have 0 shapes
- ✓ **Single line giving all the file names**

An example of circuit.nets

```
UCLA nets 1.0
# File header with version information, etc.
# Anything following # is a comment and should be ignored

NumNets             :  2
NumPins             :  5

NetDegree  :    3    n0
        o3   O      :     6.0000     6.0000
        o0   I      :    -6.0000     0.0000
NetDegree  :    2    n1
        o0   O      :     6.0000     0.0000
        o1   I      :    -3.0000     3.0000
        o2   I      :    -3.0000     3.0000
NetDegree  :    2    n2
        o2   O      :     3.0000    -3.0000
        o4   I      :    -6.0000    10.5000
```

 # Total number of nets in the circuit
 # Total number of pins in the netlist

 # NetDegree : [Total Number of Pins] [Net Name]
 # [Node Name] [Direction] : [pin_Xoffset] [pin_Yoffset]

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Circuit.pl

- ✓ **Gives the coordinate (x,y) and orientation for each node**
  - All coordinates are the lower-left coordinate
- ✓ **The coordinate for all movable nodes will be (0,0) and will be determined by cell placer (NTUplace4)**
- ✓ **The default orientation is "vertical and face up" – N (North)**
  - No flipping / mirroring / rotation of the nodes is allowed

An example of circuit.pl

```
UCLA pl 1.0
# File header with version information, etc.
# Anything following # is a comment and should be ignored

# node_name     lower_left_x   lower_left_y        orientation        movetype

     o0              30             36       :        N
     o1              48             24       :        N
     o2              60             36       :        N
     o3               6              6       :        N             /FIXED
     o4              69              3       :        N             /FIXED
```

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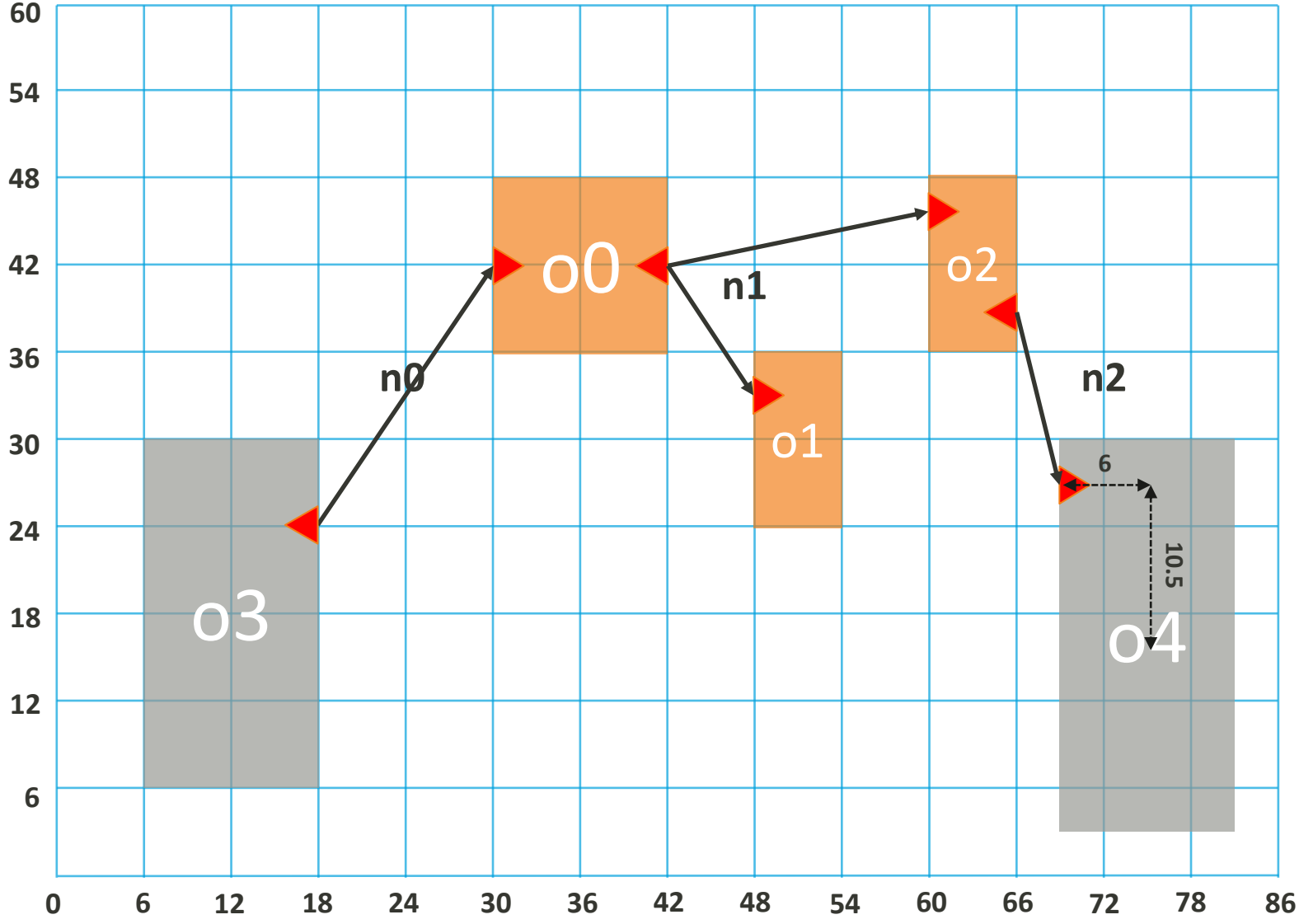
Illustration of netlist



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Circuit.scl

- ✓ **Specifies the placement image (individual circuit rows for standard cell placement)**
  - NumRows : Number of circuit rows for placement
  - Coordinate : **Y-coordinate** of the bottom edge of the circuit row
  - Height : circuit row height (= standard cell height)
  - Sitespacing/SiteWidth : can be ignored, will always be 1
  - SubrowOrigin : **X-coordinate** of the left edge of the subrow
  - NumSites : number of placement sites in this subrow
- ✓ **Right X-coordinate of subrow = SubrowOrigin + NumSites * Sitespacing**

An example of circuit.scl

```
UCLA scl 1.0
# File header with version information, etc.
# Anything following # is a comment and should be ignored

NumRows    :    5

CoreRow Horizontal                                  # Will always be horizontal row
     Coordinate      :       0
     Height          :       12
     SiteWidth       :       1                      # Optional : equal to sitespacing
     SiteSpacing     :       1
     Siteorient      :       N                      # Optional : can be ignored
     Sitesymmetry    :       Y                      # Optional : can be ignored
     SubrowOrigin    :       6       NumSites  :  80
End
..
..
```


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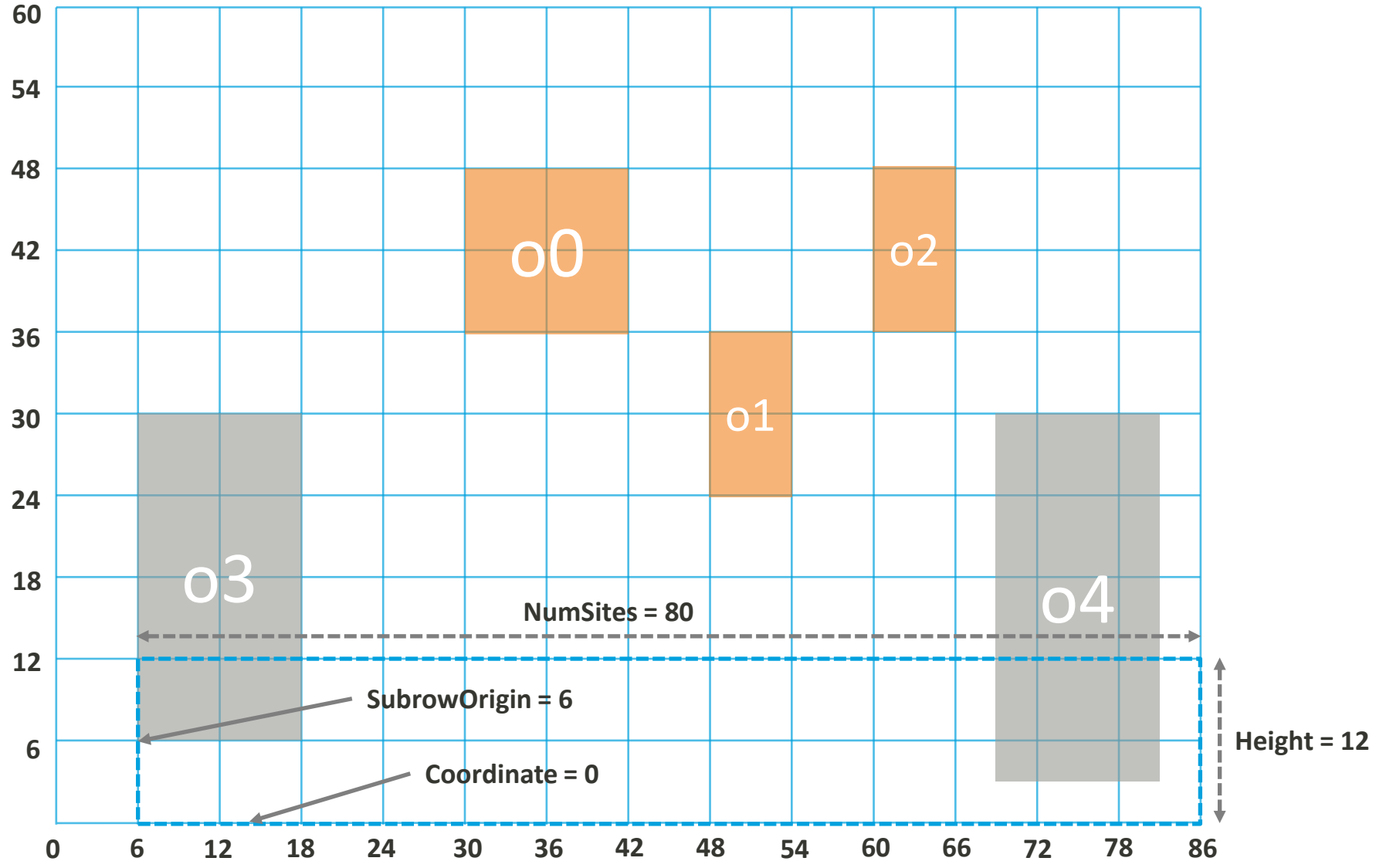
Illustration of .scl file



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Circuit.shapes

✓ **Specifies the component shapes for non-rectangular nodes**

- All shapes are removed in 2015 ICCAD contest, number of non-rectangular nodes will always be 0
- This file is necessary for routability evaluation. **Contestant can ignore this file.**

An example of circuit.shapes

```
shapes 1.0
# File header with version information, etc.
# Anything following # is a comment and should be ignored

NumNonRectangularNodes   :   0                    # Will always be horizontal row
```


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Circuit.route

- ✓ **Adopted from ISPD 2008 Contest**
  - Please reference http://archive.sigda.org/ispd2008/contests/ispd08rc.html
- ✓ **This file will be generated based on input macro placement file**

An example of circuit.route

```
route 1.0
# File header with version information, etc.
# Anything following # is a comment and should be ignored

Grid : 304 403 9
VerticalCapacity        :   0   80    0  80    0  80    0  80    0
HorizontalCapacity      :   0    0   80   0   80   0   80    0  80
MinWireWidth            :   1    1    1   1    2   2    2    4   4
MinWireSpacing          :   1    1    1   1    2   2    2    4   4
ViaSpacing              :   0    0    0   0    0   0    0    0   0
GridOrigin              :  18   18
TileSize                :  40   40
BlockagePorosity        :   0

NumNiTerminals          :   0                          # Will always be 0

NumBlockageNodes        :   2
    o3      4    1    2    3    4                     # o3/o4 block 4 metal layers (layer 1, 2, 3, 4 )
    o4      4    1    2    3    4                     # within all routing tiles they overlap.
```


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2015 ICCAD Contest

OUTPUT BENCHMARK FORMAT

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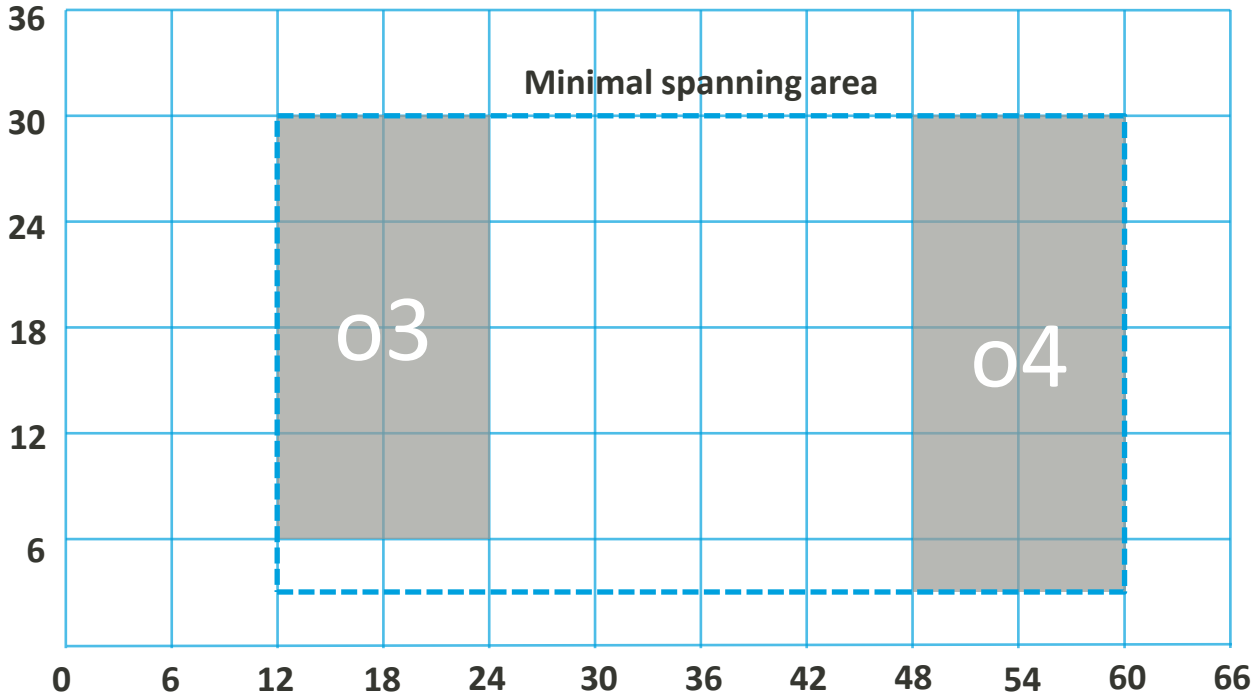
Circuit.fp

✓ **Output of the macro placement file**

- [design].fp
- Contestant only needs to determine the location for **all fixed block** using minimal area with minimal routing congestion
- The placement of fixed blocks must not overlap with one another
- Placer will place the standard cells and router will connect the netlist to determine routing congestion

An example of circuit.fp

```
o3 : 12  6 : N /FIXED
o4 : 48  3 : N /FIXED
```



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