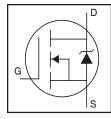
International Rectifier

IRLB3034PbF

HEXFET® Power MOSFET

Applications

- DC Motor Drive
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}	40V
R _{DS(on)} typ.	$1.4 \mathrm{m}\Omega$
max.	1.7 m Ω
D (Silicon Limited)	343A ①
I _D (Package Limited)	195A

Benefits

- Optimized for Logic Level Drive
- Very Low R_{DS(ON)} at 4.5V V_{GS}
- Superior R*Q at 4.5V V_{GS}
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dl/dt Capability
- Lead-Free



G	D	S		
Gate	Drain	Source		

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	343①	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	243 ①	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	195	7 ^
I _{DM}	Pulsed Drain Current ②	1372	
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
dv/dt	Peak Diode Recovery ④	4.6	V/ns
T _J	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range	-55 10 + 175	°C
	Soldering Temperature, for 10 seconds	300	7
	(1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf·in (1.1N·m)	

Avalanche Characteristics

E _{AS (Thermally limited)}	Single Pulse Avalanche Energy ③	255	mJ
I _{AR}	Avalanche Current ②	Coo Fig. 14, 15, 220, 22b	Α
E _{AR}	Repetitive Avalanche Energy ②	See Fig. 14, 15, 22a, 22b,	mJ

Thermal Resistance

110-1102									
Symbol	Parameter	Тур.	Max.	Units					
$R_{\theta JC}$	Junction-to-Case ®		0.4						
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5		°C/W					
$R_{\theta JA}$	Junction-to-Ambient		62	Ī					

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Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40			٧	$V_{GS} = 0V, I_{D} = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.04		V/°C	Reference to 25°C, I _D = 5mA ²
Ь	Static Drain-to-Source On-Resistance		1.4	1.7	m0	$V_{GS} = 10V, I_D = 195A$ (5)
R _{DS(on)}			1.6	2.0	11157	$V_{GS} = 4.5V, I_D = 172A $ §
$V_{GS(th)}$	Gate Threshold Voltage	1.0		2.5	٧	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I _{DSS}	Drain-to-Source Leakage Current			20	υΑ	$V_{DS} = 40V, V_{GS} = 0V$
				250	ĮμΑ	$V_{DS} = 40V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I _{GSS}	Gate-to-Source Forward Leakage			100	π Λ	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage			-100	nA	V _{GS} = -20V
R _{G(int)}	Internal Gate Resistance		2.1		Ω	

Dynamic @ $T_J = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
gfs	Forward Transconductance	286			S	$V_{DS} = 10V, I_{D} = 195A$
Q_g	Total Gate Charge		108	162		I _D = 185A
Q_{gs}	Gate-to-Source Charge		29		nC	$V_{DS} = 20V$
Q_{gd}	Gate-to-Drain ("Miller") Charge		54		IIIC	V _{GS} = 4.5V ⑤
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})		54		1	$I_D = 185A, V_{DS} = 0V, V_{GS} = 4.5V$
t _{d(on)}	Turn-On Delay Time		65			$V_{DD} = 26V$
t _r	Rise Time		827		ا ا	I _D = 195A
t _{d(off)}	Turn-Off Delay Time		97		ns	$R_G = 2.1\Omega$
t _f	Fall Time		355			V _{GS} = 4.5V ⑤
C _{iss}	Input Capacitance		10315			$V_{GS} = 0V$
C _{oss}	Output Capacitance		1980			$V_{DS} = 25V$
C _{rss}	Reverse Transfer Capacitance		935		рF	f = 1.0MHz
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)		2378			$V_{GS} = 0V$, $V_{DS} = 0V$ to 32V \odot
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related) ®		2986			$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V $

Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
I _S	Continuous Source Current			343①		MOSFET symbol
	(Body Diode)			3430	A	showing the
I _{SM}	Pulsed Source Current			1372	^	integral reverse
	(Body Diode) ②			13/2		p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25$ °C, $I_S = 195$ A, $V_{GS} = 0$ V (§)
t _{rr}	Reverse Recovery Time		39			$T_J = 25$ °C $V_R = 34V$,
			41			$T_J = 125^{\circ}C$ $I_F = 195A$
Q _{rr}	Reverse Recovery Charge		39			$T_J = 25^{\circ}C$ di/dt = 100A/ μ s \odot
			46		nC	$T_J = 125^{\circ}C$
I _{RRM}	Reverse Recovery Current		1.7		Α	$T_J = 25^{\circ}C$
t _{on}	Forward Turn-On Time	Intrins	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)			

Notes:

- ① Calcuted continuous current based on maximum allowable junction temperature Bond wire current limit is 195A. Note that current limitation arising from heating of the device leds may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- $\mbox{\@ifnextcoloredge}$ Limited by $T_{Jmax},$ starting $T_J=25^{\circ}C,\,L=0.013mH$ $R_G=25\Omega,\,I_{AS}=195A,\,V_{GS}=10V.$ Part not recommended for use above this value .
- $\textcircled{4} \ \ I_{SD} \leq 195 A, \ di/dt \leq 841 A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \ T_{J} \leq 175^{\circ}C.$

- $\ \ \, \ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \ \,$ $\ \$ $\$ $\ \$ $\ \$ $\$ $\ \$ $\$ $\ \$ $\$
- $\ \ \,$ C $_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as C $_{oss}$ while V $_{DS}$ is rising from 0 to 80% V $_{DSS}.$
- ® R_θ is measured at T_J approximately 90°C

2 www.irf.com

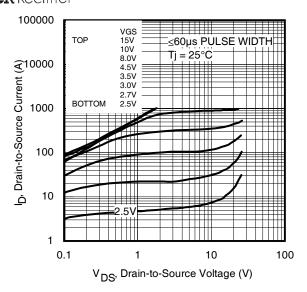


Fig 1. Typical Output Characteristics

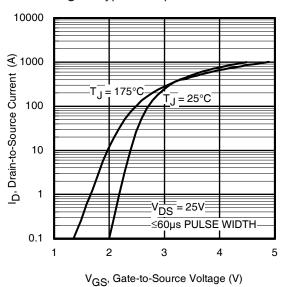


Fig 3. Typical Transfer Characteristics

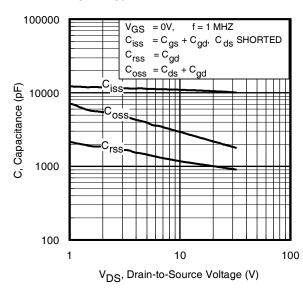


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage www.irf.com

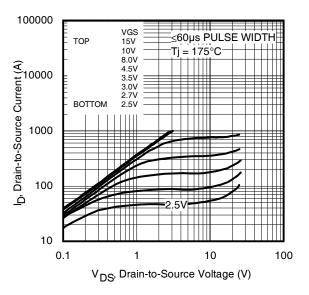


Fig 2. Typical Output Characteristics

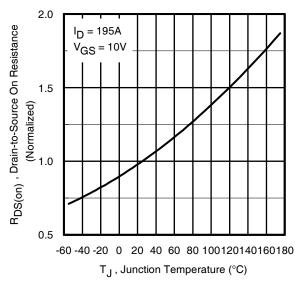


Fig 4. Normalized On-Resistance vs. Temperature

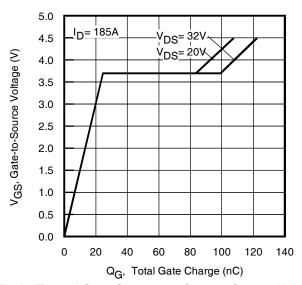


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

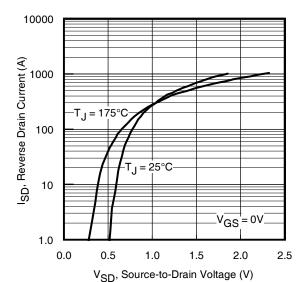
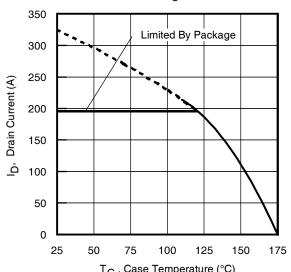
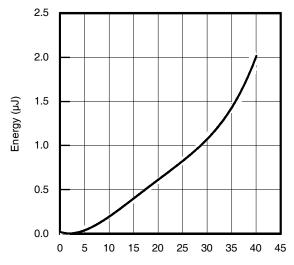


Fig 7. Typical Source-Drain Diode Forward Voltage



T_C , Case Temperature (°C) **Fig 9.** Maximum Drain Current vs.

Case Temperature



V_{DS,} Drain-to-Source Voltage (V) **Fig 11.** Typical C_{OSS} Stored Energy

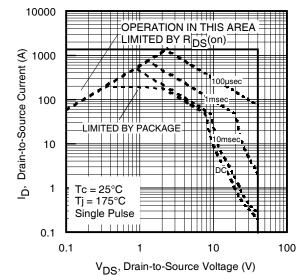


Fig 8. Maximum Safe Operating Area

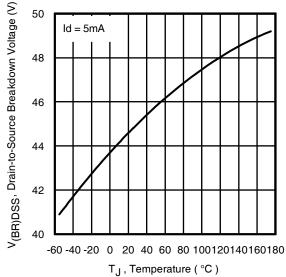


Fig 10. Drain-to-Source Breakdown Voltage

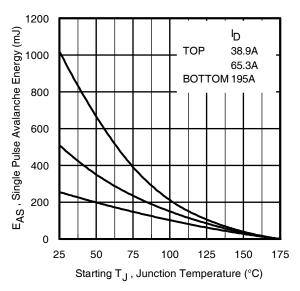


Fig 12. Maximum Avalanche Energy vs. DrainCurrent www.irf.com

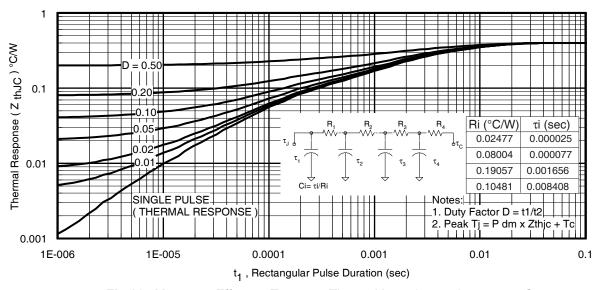


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

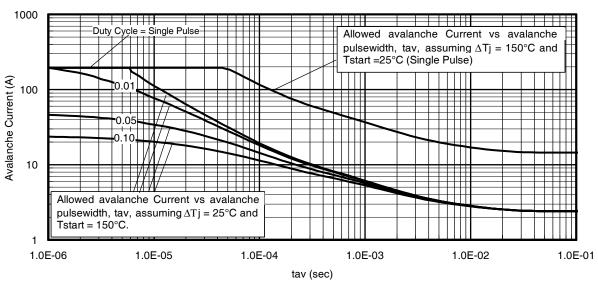


Fig 14. Typical Avalanche Current vs. Pulsewidth

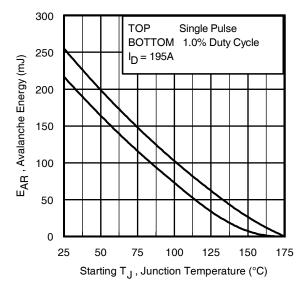


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15: (For further info, see AN-1005 at www.irf.com)

- 1. Avalanche failures assumption:
- Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long asT_{imax} is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
- 4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. I_{av} = Allowable avalanche current.
- 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 - t_{av} = Average time in avalanche.
 - D = Duty cycle in avalanche = $t_{av} \cdot f$

 $Z_{th,JC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$\begin{split} P_{D \text{ (ave)}} &= 1/2 \text{ (} 1.3 \cdot \text{BV} \cdot \text{I}_{av} \text{)} = \triangle \text{T/ Z}_{thJC} \\ I_{av} &= 2\triangle \text{T/ [} 1.3 \cdot \text{BV} \cdot \text{Z}_{th} \text{]} \\ E_{AS \text{ (AR)}} &= P_{D \text{ (ave)}} \cdot t_{av} \end{split}$$

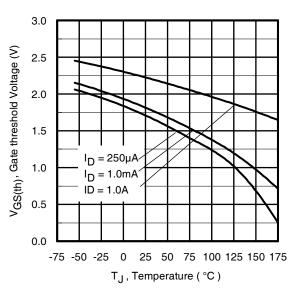


Fig 16. Threshold Voltage vs. Temperature

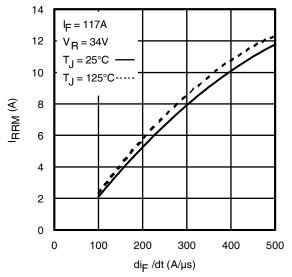


Fig. 18 - Typical Recovery Current vs. dif/dt

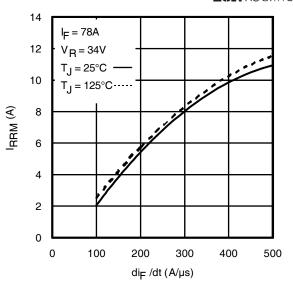


Fig. 17 - Typical Recovery Current vs. di_f/dt

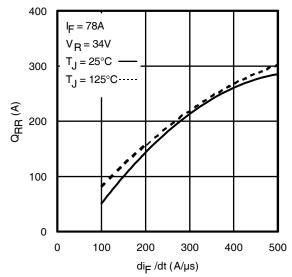


Fig. 19 - Typical Stored Charge vs. dif/dt

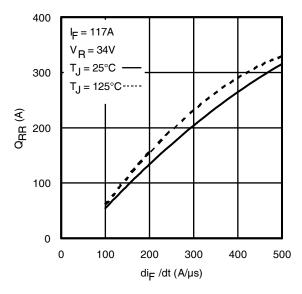


Fig. 20 - Typical Stored Charge vs. dif/dt

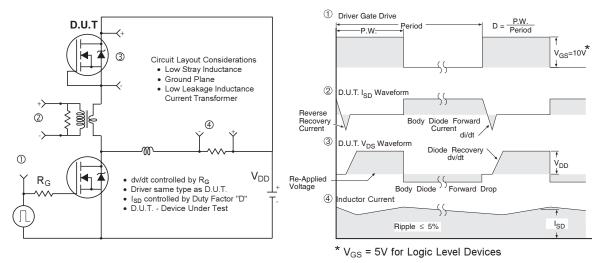


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

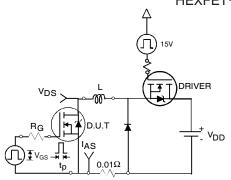


Fig 22a. Unclamped Inductive Test Circuit

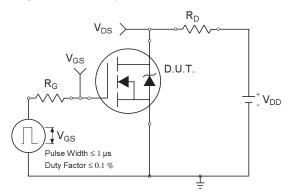


Fig 23a. Switching Time Test Circuit

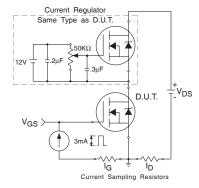


Fig 24a. Gate Charge Test Circuit www.irf.com

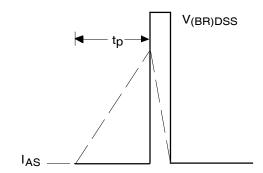


Fig 22b. Unclamped Inductive Waveforms

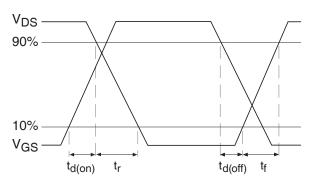


Fig 23b. Switching Time Waveforms

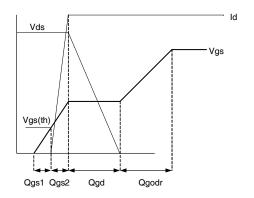
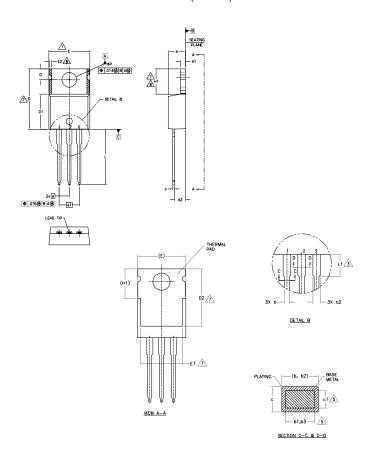


Fig 24b. Gate Charge Waveform

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]. LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.

- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
 DIMENSION D, 10 & E DO NOT INCLUDE MOLD FLASH MOLD FLASH
 SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE
 MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
 CONTROLLING DIMENSION: INCHES.
 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E.H1,D2 & E1

- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

	DIMENSIONS						
SYMBOL	MILLIM	ETERS	INC	HES			
	MIN.	MAX.	MIN.	MAX.	NOTES		
Α	3,56	4.83	.140	.190			
A1	0.51	1.40	.020	.055			
A2	2.03	2.92	.080	.115			
ь	0.38	1.01	.015	.040			
ь1	0.38	0.97	.015	.038	5		
b2	1,14	1.78	.045	.070			
b3	1,14	1.73	.045	.068	5		
С	0.36	0.61	.014	.024			
c1	0.36	0,56	.014	.022	5		
D	14.22	16.51	.560	.650	4		
D1	8.38	9.02	.330	.355			
D2	11.68	12.88	.460	.507	7		
Ε	9.65	10.67	.380	.420	4,7		
E1	6.86	8.89	.270	.350	7		
E2	-	0.76	-	.030	8		
е	2.54	2.54 BSC		BSC			
e1	5.08	BSC	.200 BSC				
H1	5,84	6.86	.230	.270	7,8		
L	12.70	14.73	.500	.580			
L1	3.56	4.06	.140	.160	3		
øΡ	3,54	4.08	.139	.161			
Q	2.54	3.42	.100	.135			

LEAD ASSIGNMENTS HEXFET ICBTs. CoPACK 1.- GATE 2.- COLLECTOR 3.- EMITTER DIODES 1.- ANODE 2.- CATHODE 3.- ANODE

TO-220AB Part Marking Information

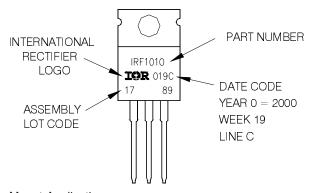
EXAMPLE: THIS IS AN IRF 1010

LOT CODE 1789

ASSEMBLED ON WW 19, 2000 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position

indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice. This product has been designed and qualified for the Industrial market. Qualification Standards can be found on IR's Web site.



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TAC Fax: (310) 252-7903

Mouser Electronics

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