

Internal Register Set

CHX003

North Module

Bus 0 Device 0 Function 2

SVAD DVAD Control

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| --- |
| Revision 052 |
| July 10, 2019 |

**Shanghai Zhaoxin Semiconductor**

# IRS Revision History

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Doc Rev.** | **Chip Rev.** | **Date** | **Revision Descriptions** | **Department** | **Name** |
| R052 | A0 | 7/9/2019 | 1. Change Rx90[31:28] HW attr to RO 2. Change RxB8[31:3] SW attr to RO and HW attr to NA 3. Correct default value for RSVAD\_MEXXLADDR[45:28] and RTopA 4. Correct some description | NB | Chunhui Zheng |
| R051 | A0 | 6/25/2019 | Update SVAD according to SW review result | CPU | Sharon Gao |
| R050 | A0 | 6/14/2019 | Update PCI Config space Figure | NB | Chunhui Zheng |
| R003 | A0 | 3/15/2019 | 1. add RSVAD\_MMIOB2G\_DIS at Rx9C[1] | NB | Chunhui Zheng |
| R002 | A0 | 3/8/2019 | 1. add PCIE capability and Power Management Capability 2. move SVAD register to Rx90h~Rx3FFh, TPR start offset to Rx400h 3. Remove DVAD registers 4. Add legacy IO decoder by Sharon 5. Add DPR control | NB | Chunhui Zheng |
| R001 | A0 | 3/6/2019 | Initial internal release based on CHX002 | CPU | Sharon Gao |

# Lists of TIC Tags

## TIC Question Tag

[([TIC Question 1. End of questions. Thanks!]) 63](#_Toc501530740)

## TIC Editing Tag

[([ TIC Editing Note 1. The default value should be changed to nnnnh in SPM. ]) 12](#_Toc501530746)

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# IRS Style Brief Introduction (For IRS Rule V3.R3)

## Tags and Colors

To distinguish different levels of confidentiality, TIC uses “tags” and “colors” to identify registers with different purposes. Each of them represents different meanings.

#### *Tags and Colors Used by TIC*

* **TIC Question Tag:** This tag is used for questions and issues. All questions in IRS will also be listed in the TOC section.
* **TIC Editing Note :** Notes for TIC writers as editing reminders.
* **TIC XXX Feature Tag:** To point out the related registers with some specific product features.

All TIC tags are enclosed between square brackets that are set inside parenthesis. **“([…])”**

#### *Color Used For Internal Content*

* **((Internal Content)):** Used to represent internal registers or contents that cannot be released to customers.
  + Double parenthesis “**(( ... ))**“ will be added before and after the internal registers or contents.
  + “**For Internal Reference[..]**” should be added before those contents or after register names.
  + Internal signal names can NOT be used in external content. (Only top module names are allowed to be public)

***shading-fillingHow to use Highlight:***

1. *Enable [View] > [Tool Bar] > [Table and Border], and you will see an icon of a paint-bucket shown in tool bar for the Shading-Filling tool. If you cannot see it, do the next step.*
2. *From [View] > [Tool Bar] > [Customize], select [Commands] > Categories = [Borders], Commands = [Border and Shading]. Draw that item to tool bar. Apply it to some text. Go back to step 1. You should be able to see that icon then.*
3. *Or you can select the icon from [Commands] > [All Commands] > “Shading-Color”.*

## Columns of The Register Table

* + **Default:** Default value of this register. Only allow using binary/hexadecimal value (or 0) in this field.  
     The defined keywords for special default values are listed as follows.
* **Dip :** the default value is set by dip switch or strapping.
* **HwInit :** Hardware initialized; bit default value is set by hardware to reflect related status.
* **ROMSIP :** The default value is defined in ROMSIP.
* **((Bonding)) :** The default value is depend on different product.
  + **Mnemonic:** An asterisk (\*) before a mnemonic indicates this mnemonic is referenced in some other content*.*
  + **PwrDm:** Power Domain. Following values can be used to indicate the power source of this register:
* **vbat** : for battery well
* **vsus** : for suspend well
* **vcc** : for VCC well
  + **Others:** Please refer to Outlook:\\RD\_Project\# IRS Guideline\Checker&Rules\**IRS Checker-Format Rules.doc**  
     for more details.

## Columns of Suggested Values:

* + **S:** Stable/Safe. Set to this value for best stability and/or reliability.   
    At least make sure the system can be booted without any problem.  
    *Stability = the system can be run over periods of time without crashing or otherwise malfunctioning.  
    Reliability = perform the required functions under stated conditions for a specified period of time.*
  + **P:** Performance. Set to this value for taking less time to complete the required task.
  + **E:** Energy. Set to this value for power saving.

***The Suggestion Values:***

* **0/1** : ( without the suffix ‘b’ ) Indicates the binary value for the setting. (ex. 010)
* **h** : *Use suffix ‘h’* to indicate the hex value. (ex.6Ah)
* **R** : Indicates the RO register **with fixed register value**. No suggestion value will be provided.
* **x** : Indicates the value is don't-care. No suggestion value will be provided. (ex. x)
* **\***  : Indicates the setting depends on other bits or requires specific programming sequence.  
   The detailed setting information should be described in bit description column. (ex. \*10)

# IRS Register Attributes

## Attribute Definitions

***Basic Attributes:*** *indicate common read-write operations.*

**RO:** Read Only.

**WO:** Write Only. (register value can not be read by the software)

**RW:** Read / Write.

**RW1:** Write Once then Read Only after that.

**RW1C:** Read / Write of “1” clears bit to zero.

**RWL:** Lockable Read / Write. Read/writable with lock bit control: RW when lock bit=0, Read-Only when lock bit=1.

***Extended Attributes:*** *indicate combinational or internal access methods.*

**RO((shadow)):** Value of this register is copied from another register.

**RO((RW)):** Used to indicate the existence of the internal guard bit.

**RO/RW:** Used to indicate the public guard bit. (ex. if the guard bit is defined in spec)

**RW((RWHC)): R/W-able with hardware clear automatically.**

***Sticky Attributes*:**

Adding an “**S**” in tail indicates a **sticky** register, which means that register will not be set or altered by hot reset.

Adding the “**RS**” in tail indicates a **reset-sticky** register, which means that register will not be reset unless the system entered S4/S5 state.

**ROS**: Sticky-Read-Only.

**WOS**: Sticky-Write-Only.

**RWS**: Sticky-Read/Write.

**RW1S**: Sticky-Write-Once.

**RW1CS**: Sticky-Write-1-to-Clear.

**RWLS**: Sticky-Lockable Read/Write.

**RORS**: Reset-Sticky-Read-Only.

**WORS**: Reset-Sticky-Write-Only.

**RWRS**: Reset-Sticky-Read/Write.

**RW1RS**: Reset-Sticky-Write-Once.

**RW1CRS**: Reset-Sticky-Write-1-to-Clear.

**ROS((shadows)):** Sticky-shadow

**ROS((RWS)):** Sticky-RO((RW))

**ROS/RWS:** Sticky-RO/RW

**RW((RWHC))S:** Sticky-RW((RWHC))

**RORS((shadows))**: Reset-Sticky-shadow

**RORS((RWS))**: Reset-Sticky-RO((RW))

**RORS/RWRS**: Reset-Sticky-RO/RW

**RW((RWHC))RS**: Reset-Sticky-RW((RWHC))

**((Internal Notes:**

**1. For RW1Set in xHCI spec: per discussion, it is the same with RW((RWHC)).**

***RW1Set****: Read / Write of “1” sets bit to “1”. (Writing a 0 has no effect)*

***RW1SetS****: Sticky-Write-1-to-Set ))*

## Default Value Definitions

**Dip:** Means the default value is set by dip switch or strapping.

**HwInit:** Hardware initialized; bit default value is set by hardware to reflect related status.

**ROMSIP:** The default will be overwritten by the value defined in ROMSIP after system reset.

**(( Bonding:** The default value depends on different product. **))**

# Device 0 Function 2 (D0F2): System SVAD DVAD Controller

@((SOURCE: CHIP\_SRC=CHX002(A0), DOC\_SRC= CHX003 IRS\_NB\_D0F2\_SVADDVAD\_R003, IRS\_STYLE\_VER=V3 ))

@((MODULE(MOD\_D0F2, 1x1): PRJ=CHX003, REG\_SPACE\_NUM=1, ADDR\_WIDTH=12 ))

@((REG\_SPACE [0]: TYPE=PCI, NAME=D0F2, SEL=AD11, SPACE\_LEVEL=1, RANGE=(0h, FFFh) ))

@((DEFAULT\_GUARDBIT=RPEROWEN D0F5 RXF0[0]))

@((REG\_GROUP(PCI Header Registers): RANGE=(0h, 3Fh) ))

## PCI Configuration Space

This chip integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in **Figure 1** below.

Device 0 Function 2 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 2. For example, I/O write CF8h, with the data having the following format. And then I/O read CFCh, to get the data or I/O write CFCh, to write data (32 bits). Registers in this function can also be accessed using PCIE enhanced configuration mechanism when it is enabled by programming D0F2Rx40[17:0].

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit [31]** | **Bits [30:24]** | **Bits [23:16]** | **Bits [15:11]** | **Bits [10:8]** | **Bits [7:2]** | **Bit [1]** | **Bit [0]** |
| Enable | Reserved | Bus Number | Device Number | Function Number | Register Number | 0 | 0 |
| 1 | 000\_0000 | 0000\_0000 | 0\_0000 | **010** | RX offset address with bit [1:0] = 00b | | |



Figure 1. System Block Diagram for D0F2

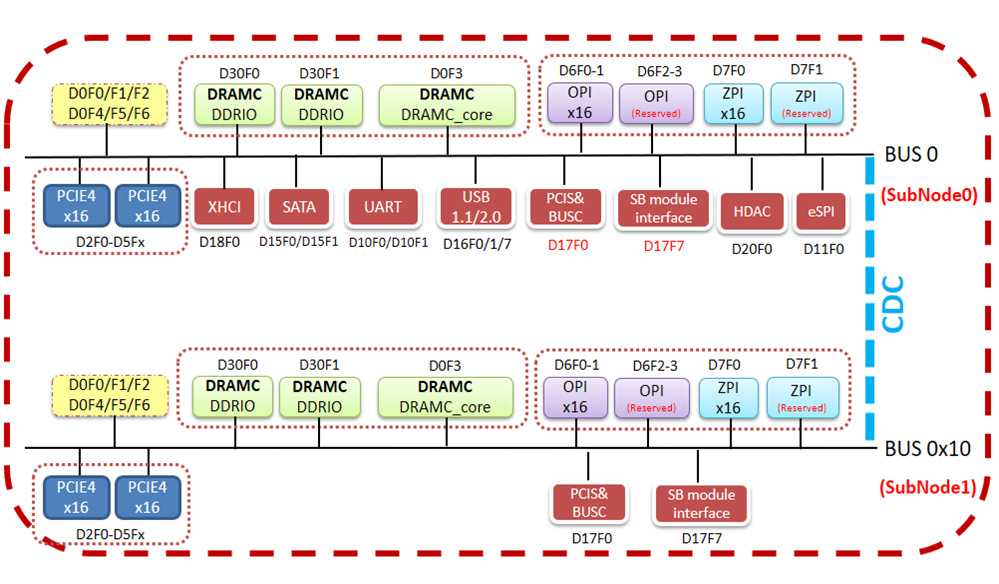


Figure 2. Register Level Block Diagram for D0F2

### Header Registers (00-3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

([ TIC Editing Note 1. The default value should be changed to nnnnh in SPM. ])

Offset Address: 01-00h (D0F2)   
Vendor ID Default Value: 1D17h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:0 | RO((RWL)) | NA | 1D17h | **Vendor ID**  Used to identify the manufacturer of this device.  ((For Internal Reference: @((#USER=PCISPEC))  @((#control\_lock=lock\_port RVID\_DID\_LOCK\_D0F2))  @((#control\_default=NB\_VID\_SEL))  @((#VENDOR\_OPTION=1106h))  )) | VendorID[15:0] |  | vcc | x | x | x |

Offset Address: 03-02h (D0F2)   
Device ID Default Value: 31B1h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:0 | RO((RWL)) | NA | 31B1h | **Device ID**  Used to identify this function.  ((For Internal Reference: @((#USER=PCISPEC))  @((#control\_lock=lock\_port RDID\_RID\_LOCK\_D0F2))  )) | DEVID[15:0] |  | vcc | x | x | x |

Offset Address: 05-04h (D0F2)   
PCI Command Default Value: 0006h

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. ((For Internal Reference: The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6](RENPPB) = 0) or D19F0 (when D17F7Rx4F[6](RENPPB) = 1).))

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:10 | RO | NA | 0 | **Reserved** | Rx04[15:10] |  | vcc | R | x | x |
| 9 | RO | NA | 0 | **Fast Back-to-back Cycle Enable**  It is used to enable the fast back-to-back capability on the PCI bus for the PCI bus controller. | RFBACK |  | vcc | R | x | x |
| 8 | RO | NA | 0 | **SERR# Enable**  It is used to enable the SERR# driver which asserts SERR# signal on the PCI bus. | RSERR |  | vcc | R | x | x |
| 7 | RO | NA | 0 | **Address/Data Stepping**  It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus. | RSETP |  | vcc | R | x | x |
| 6 | RO | NA | 0 | **Parity Error Response**  It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not. | \*RPTYERR |  | vcc | R | x | x |
| 5 | RO | NA | 0 | **VGA Palette Snooping**  It controls how VGA compatible Graphics devices handle accesses to VGA palette registers.  This bit is fixed at 0. | RVGA |  | vcc | R | x | x |
| 4 | RO | NA | 0 | **Memory Write and Invalidate**  It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus. | RMWINV |  | vcc | R | x | x |
| 3 | RO | NA | 0 | **Respond to Special Cycle**  It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus. | RSPCYC |  | vcc | R | x | x |
| 2 | RO | NA | 1b | **PCI Master Function**  It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus. | RMSTR |  | vcc | R | x | x |
| 1 | RO | NA | 1b | **Memory Space Access**  It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus. | RENMEM |  | vcc | R | x | x |
| 0 | RO | NA | 0 | **I/O Space Access**  It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus. | RENIO |  | vcc | R | x | x |

Offset Address: 07-06h (D0F2)PCI StatusDefault Value: 0210h

The value of this register won’t reflect what happened on the PCI bus. ((For Internal Reference: The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7 Rx4F[6](RENPPB) = 0) or D19F0 (when D17F7 Rx4F[6](RENPPB) = 1).))

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15 | RO | NA | 0 | **Detected Parity Error**  It is used to indicate a parity error had been detected by the PCI bus controller. | SPERRS |  | vcc | R | x | x |
| 14 | RO | NA | 0 | **Signaled System Error (SERR# Asserted)**  It is used to indicate the PCI bus controller had asserted the SERR#. | SERRS |  | vcc | R | x | x |
| 13 | RO | NA | 0 | **Received Master-abort (Except Special Cycle)**  It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction. | SMABORT |  | vcc | R | x | x |
| 12 | RO | NA | 0 | **Received Target-abort**  It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction. | STABORTM |  | vcc | R | x | x |
| 11 | RO | NA | 0 | **Target-abort Assertion**  It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it. | STABORTS |  | vcc | R | x | x |
| 10:9 | RO | NA | 01b | **DEVSEL# Timing**  It is used to indicate the response latency for the timing of PCI signal DEVSEL#.  00: Fast 01: Medium  10: Slow 11: Reserved  These bits won’t affect the DEVSEL# timing on the PCI bus. | DEVS[1:0] |  | vcc | R | x | x |
| 8 | RO | NA | 0 | **Master Data Parity Error**  It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. It includes three cases:  (1) As a target, the PCI bus controller asserts PERR# on a read cycle or observes the assertion of PERR# on a write cycle.  (2) As a initiator, the PCI bus controller encounters error upon the cycle it initiates.  (3) Parity Error Response bit at Rx04[6](RPTYERR) is set. | SDPERRS |  | vcc | R | x | x |
| 7 | RO | NA | 0 | **Capable of Accepting Fast Back-to-back as a Target**  It is used to indicate the capability of accepting fast back-to-back cycles. | RFBKS |  | vcc | R | x | x |
| 6 | RO | NA | 0 | **User Definable Features**  It is reserved for user to define. | RUDF |  | vcc | R | x | x |
| 5 | RO | NA | 0 | **66MHz Capability**  It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.  ((For Internal Reference: @((EXT = ECO)) )) | R66M |  | vcc | R | x | x |
| 4 | RO | NA | 1b | **Support New Capability List**  It indicates whether this device implements the pointer for a New Capabilities linked list at offset 34h.  0: New capability linked list is not available.  1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., new capability linked list is supported. | RCAP |  | vcc | R | x | x |
| 3:0 | RO | NA | 0 | **Reserved** | Rx04[19:16] |  | vcc | R | x | x |

Offset Address: 08h (D0F2)  
Revision ID Default Value: 04h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO((RWL)) | NA | 04h | **Revision Code**  It indicates the revision ID of this function.  ((For Internal Reference: @((#USER=PCISPEC))  @((#control\_lock=lock\_port RDID\_RID\_LOCK\_D0F2))  )) | Rx08[7:0] |  | vcc | x | x | x |

Offset Address: 0B-09h (D0F2)  
Class Code Default Value: 06 0000h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 23:0 | RO((RWL)) | NA | 06 0000h | **Class Code**  06 0000h indicates this function is a host bridge.  ((For Internal Reference: @((#USER=PCISPEC)) @((#control\_lock=lock\_port RCLASS\_CODE\_LOCK\_D0F2)) )) | ClassCode[23:0] |  | vcc | x | x | x |

Offset Address: 0Ch (D0F2)  
Cache Line Size Default Value: 00h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RW | NA | 0 | **Cache Line Size**  It indicates the cache-line size in a cache-line transaction in units of double words.  ((Writing 1 or 0 to these registers does not change any behavior of this chip.))  ((For Internal Reference: Some HCT software requires these registers to be R/W to have warning free report.)) | Rx0C[7:0] |  | vcc | x | x | x |

Offset Address: 0Dh (D0F2)  
PCI Master Latency Timer Default Value: 00h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Maximum Time Slice for This Function as a Master on the PCI Bus**  It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The unit is 8 PCI Clocks. They do not have any impact to the behaviors of this chip. | Rx0C[15:8] |  | vcc | R | x | x |

Offset Address: 0Eh (D0F2)  
Header Type Default Value: 80h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 80h | **Header Type**  Bit [7] in this register is used to identify a multifunction device. If bit [7] = 0, the device is single function. If bit [7] = 1, the device is multiple functions. Bits [6:0] identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value 80h indicates that this is a multi-function device. | Rx0C[23:16] |  | vcc | R | x | x |

Offset Address: 0Fh (D0F2)  
Built In Self Test (BIST) Default Value: 00h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **BIST Support**  Bit [7] = 0 indicates that this function does not support BIST. Writing a 1 to bit [6] will invoke the BIST operation. The value of 0h on bits [3:0] means the device has passed its test. Non-zero values on bits [3:0] means the device failed. This chip does not support BIST through these registers. | Rx0C[31:24] |  | vcc | R | x | x |

Offset Address: 13-10h (D0F2)   
Base Address Registers 0 Default Value: 0000 0000h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RO | NA | 0 | **Base Address 0**  This function does not claim base address. | Rx10[31:0] |  | vcc | R | x | x |

Offset Address: 17-14h (D0F2)   
Base Address Registers 1 Default Value: 0000 0000h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RO | NA | 0 | **Base Address 1**  This function does not claim base address. | Rx14[31:0] |  | vcc | R | x | x |

Offset Address: 1B-18h (D0F2)   
Base Address Registers 2 Default Value: 0000 0000h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RO | NA | 0 | **Base Address 2**  This function does not claim base address. | Rx18[31:0] |  | vcc | R | x | x |

Offset Address: 1F-1Ch (D0F2)   
Base Address Registers 3 Default Value: 0000 0000h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RO | NA | 0 | **Base Address 3**  This function does not claim base address. | Rx1C[31:0] |  | vcc | R | x | x |

Offset Address: 23-20h (D0F2)   
Base Address Registers 4 Default Value: 0000 0000h

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RO | NA | 0 | **Base Address 4**  This function does not claim base address. | Rx20[31:0] |  | vcc | R | x | x |

Offset Address: 27-24h (D0F2)   
Base Address Registers 5 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RO | NA | 0 | **Base Address 5**  This function does not claim base address. | Rx24[31:0] |  | vcc | R | x | x |

Offset Address: 2B-28h (D0F2)   
CardBus CIS Pointer Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RO | NA | 0 | **CardBus CIS Pointer**  This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function. | Rx28[31:0] |  | vcc | R | x | x |

Offset Address: 2D-2Ch (D0F2)   
Subsystem Vendor ID Default Value: 1D17h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:0 | RW1 | NA | 1D17h | **Subsystem Vendor ID**  They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#. | Rx2C[15:0] |  | vcc | x | x | x |

Offset Address: 2F-2Eh (D0F2)   
Subsystem ID Default Value: 31B1h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:0 | RW1 | NA | 31B1h | **Subsystem ID**  They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#. | Rx2C[31:16] |  | vcc | x | x | x |

Offset Address: 30h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx30[7:0] |  | vcc | R | x | x |

Offset Address: 31h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx31[7:0] |  | vcc | R | x | x |

Offset Address: 32h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx32[7:0] |  | vcc | R | x | x |

Offset Address: 33h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx33[7:0] |  | vcc | R | x | x |

Offset Address: 34h (D0F2)   
Capability Pointer Default Value: 40h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO((RW)) | NA | 40h | **Capability List Pointer**  It indicates an offset address from the start of the configuration space. This pointer points to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to be specified. | CAPPTR[7:0] |  | vcc | 40h | x | x |

Offset Address: 35h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx35[7:0] |  | vcc | R | x | x |

Offset Address: 36h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx36[7:0] |  | vcc | R | x | x |

Offset Address: 37h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx37[7:0] |  | vcc | R | x | x |

Offset Address: 38h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx38[7:0] |  | vcc | R | x | x |

Offset Address: 39h (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx39[7:0] |  | vcc | R | x | x |

Offset Address: 3Ah (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx3A[7:0] |  | vcc | R | x | x |

Offset Address: 3Bh (D0F2)   
Reserved Default Value: 00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 7:0 | RO | NA | 0 | **Reserved** | Rx3B[7:0] |  | vcc | R | x | x |

Offset Address: 3D-3Ch (D0F2)   
Interrupt Line and Interrupt Pin Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:8 | RO | NA | 0 | **Interrupt Pin**  It tells which interrupt pin the device uses. It is not applicable to this function. | Rx3C[15:8] |  | vcc | R | x | x |
| 7:0 | RO | NA | 0 | **Interrupt Line**  It is used to communicate interrupt line routing information. It is not applicable to this function. | Rx3C[7:0] |  | vcc | R | x | x |

Offset Address: 3F-3Eh (D0F2)   
Minimum Grant and Maximum Latency Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:8 | RO | NA | 0 | **Maximum Latency**  It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function. | Rx3C[31:24] |  | vcc | R | x | x |
| 7:0 | RO | NA | 0 | **Minimum Grant**  It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function. | Rx3C[23:16] |  | vcc | R | x | x |

@((REG\_GROUP(Multi-Function Control and Legacy Space Access Control): RANGE=(40h, 7Fh) ))

### Reserved for PCI Express Capibility (40-7Fh)

Offset Address: 41-40h (D0F2)   
PCI Express List Default Value: 8010h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:8 | RO((RW)) | NA | 80h | **Next Pointer**  This 8-bit pointer points to the next capability of this function. Next capability is resided started from Rx88h | RX40[15:8] |  | vcc | 80h | x | x |
| 7:0 | RO | NA | 10h | **Capability ID**  This byte is read as 10h indicates a PCI Express Capability Structure. | RX40[7:0] |  | vcc | 10h | x | x |

Offset Address: 43-42h (D0F2)   
PCI Express Capabilities Default Value: 0042h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:14 | RO | NA | 0 | **Reserved** | RX42[15:14] |  | vcc | 0 | x | x |
| 13:9 | RO((RW)) | NA | 0 | **Interrupt Message Number** | RX42[13:9] |  | vcc | 0 | x | x |
| 8 | RO((RW)) | NA | 0 | **Slot Implemented** | RX42[8] |  | vcc | 0b | x | x |
| 7:4 | RO((RW)) | NA | 0100b | **Device / Port Type** | RX42[7:4] |  | vcc | 0100b | x | x |
| 3:0 | RO((RW)) | NA | 2h | **Capability Version Bit** | RX42[3:0] |  | vcc | 2h | x | x |

Offset Address: 47-44h (D0F2)   
Device Capabilities 1 Default Value: 0000 8000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:29 | RO | NA | 0 | **Reserved** | rsv\_19 |  | vcc | R | x | x |
| 28 | RO  ((RW)) | NA | 0 | **Function Level Reset Capability**  A value of 1 indicates this function supports the optional Function Level Reset (FLR) mechanism. This field applies to Endpoints only.  It is reserved for this root port.  ((For Internal Reference: This bit will be write-able when D0F5 RxF0[0] is programmed to 1.)) | tbd\_27 |  | vcc | 0 | x | x |
| 27:26 | RO | NA | 0 | **Captured Slot Power Limit Scale**  This field specifies the scale used for the Slot Power Limit Value (Rx44[25:18]).  Range of values:  00: 1.0x. 01: 0.1x.  10: 0.01x. 11: 0.001x.  Upon receiving the Set\_Slot\_Power\_Limit Message from the upper link, this field is set as the value specified in the message or is hardwired to 00b.  This bit is for upstream port only, it is reserved and always read as 00b for this root port. | rsv\_20 |  | vcc | 0 | x | x |
| 25:18 | RO | NA | 0 | **Captured Slot Power Limit Value**  In combination with the Slot Power Limit Scale value (Rx44[27:26]), this field specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field (Rx44[27:26]). Upon receiving the Set\_Slot\_Power\_Limit Message from the upper link, this field is set as the value specified in the message or is hardwired to 00h.  This bit is for upstream port only, it is reserved and always read as 00h for this root port | rsv\_21 |  | vcc | 0 | x | x |
| 17:16 | RO | NA | 0 | **Reserved** | rsv\_22 |  | vcc | R | x | x |
| 15 | RO  ((RW)) | NA | 1b | **Role-based Error Reporting**  When set to 1, this bit indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1.  0: Role-based error reporting is not supported.  1: Role-based error reporting is supported.  ((For Internal Reference: This chip does NOT fully support Role-Base Error reporting. It implemented the way to change the Non-fatal error to become correctable error in the system. However, the default value is 1 for passing Microsoft WLK test. Microsoft treat the root port support Role-Based Error Reporting as support PCIe 1.1.  This bit becomes write-able when D0F5 RxF0[0] is programmed to 1.)) | RRBERRP |  | vcc | 1 | x | x |
| 14 | RO | NA | 0 | **Power Indicator Present**  When set to 1, this bit indicates that a Power Indicator is implemented on the adapter and is electrically controlled by the component on the adapter using the Power\_Indicator\_On, Power\_Indicator\_Blink, and Power\_Indicator\_Off Messages.  It is reserved for root port.  Note: According to PCIE GEN3 SPEC, the value read from this bit is undefined. | rsv\_23 |  | vcc | 0 | x | x |
| 13 | RO | NA | 0 | **Attention Indicator Present**  When set to 1, this bit indicates that an Attention Indicator is implemented on the adapter and is electrically controlled by the component on the adapter using the Attention\_Indicator\_On, Attnetion\_Indicator\_Blink, and Attention\_indicator\_Off Messages.  It is reserved for root port.  Note: According to PCIE GEN3 SPEC, the value read from this bit is undefined. | rsv\_24 |  | vcc | 0 | x | x |
| 12 | RO | NA | 0 | **Attention Button Present**  When set to 1, this bit indicates that an Attention Button is implemented on adapter and is electrically controlled by the component on the adapter. Attention Button press events are reported using the Attention\_Button\_Pressed Message.  It is reserved for root port.  Note: According to PCIE GEN3 SPEC, the value read from this bit is undefined. | rsv\_25 |  | vcc | 0 | x | x |
| 11:9 | RO  ((RW)) | NA | 000b | **Endpoint L1 Acceptable Latency**  This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint’s internal buffering.  000: 1us 001: 2us  010: 4us 011: 8us  100: 16us 101: 32us  110: 64us 111: No limit  It is reserved for root port.  ((For Internal Reference: It is reserved for Root Port and supposed to be always 000b. And this bit becomes write-able when D0F5 RxF0[0] is programmed to 1.)) | DAL1AL\_ |  | vcc | 0 | x | x |
| 8:6 | RO | NA | 0 | **Endpoint L0s Acceptable Latency**  This field indicates the acceptable total latency that an Endpoint can withstand due to the transition for L0s state to L0 State.  000: 64ns 001: 128ns  010: 256ns 011: 512ns  100: 1024ns 101: 2us  110: 4us 111: No limit  It is reserved for root Port. | Rsv\_44 |  | vcc | 0 | x | x |
| 5 | RO  ((RW)) | NA | 0 | **Extended Tag Field Supported**  This bit indicates the maximum supported size of the tag field as a requester.  0: 5-bit tag field supported.  1: 8-bit tag field supported.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].)) | \*DAXTAGF |  | vcc | 0 | x | x |
| 4:3 | RO | NA | 0 | **Phantom Functions Supported**  This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers (called Phantom Functions) with the tag identifier. This field indicates the number of most significant bits of the function number portion of Requester ID that are logically combined with the tag identifier.  00: No function number bits used for Phantom Functions. That is, the Tag field of the requester remain at 8 bits.  01: First MSB of function number in Requester ID used for Phantom Functions. That is, MSB bit can be combined with the transaction Tag to form a 9 bits Tag to track the outstanding transactions.  10: First 2 MSB of function number in Requester ID used for Phantom Functions. That is, 2 MSB bits can be combined with the transaction Tag to form a 10 bits Tag to track the outstanding transactions.  11: All three bits of function number in Requester ID used for Phantom Functions. That is, all 3 function bits can be combined with the transaction Tag to form a 11 bits Tag to track the outstanding transactions.  This chip does not support the Phantom Functions. | rsv\_26 |  | vcc | 0 | x | x |
| 2:0 | RO  ((RW)) | NA | 000b | **Max Payload Size Supported**  This field indicates the maximum payload size that this root port can support for the upstream write requests.  000: 128 bytes (16 QW)  001: 256 bytes (32 QW)  010: 512 bytes (64 QW)  011: 1024 bytes (128 QW)  100: 2048 bytes (256 QW)  101: 4096 bytes (512 QW)  110, 111: Reserved.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].)) | DAMPSS\_ |  | vcc | 000b | x | x |

Offset Address: 49-48h (D0F2)   
Device Control 1 Default Value: 0010h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15 | RO | NA | 0 | **Reserved** | rsv\_27 |  | vcc | R | x | x |
| 14:12 | RO | NA | 0 | **Max Read Request Size**  This field sets the maximum Read Request size for the device as a Requestor.  000: 128 bytes Others: Reserved | DCMRRS\_ |  | vcc | 0 | x | x |
| 11 | RW | NA | 0 | **Enable No Snoop**  0: Disable 1: Enable  If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions to indicate that it does not require hardware enforced cache coherency. | DCENS |  | vcc | 0 | x | x |
| 10 | RW | NA | 0 | **Auxiliary Power PM Enable**  0: Disable 1: Enable  This bit when set enables device to draw AUX power independent of PME AUX power. | DCAPPME |  | vcc | 0 | x | x |
| 9 | RO | NA | 0 | **Phantom Functions Enable** | DCPFE |  | vcc | 0 | x | x |
| 8 | RO/RW | NA | 0 | **Extended Tag Field Enable**  When Rx44[5] (DAXTAGF) is set to 0, this bit is RO.  When Rx44[5] (DAXTAGF) is set to 1, this bit is RW.  ((For Internal Reference: This bit is RW when D0F2 Rx44[5] is set to 1.))  @((guardbit=DAXTAGF D0F2 RX44[5])) | DCETFE |  | vcc | 0 | x | x |
| 7:5 | RW | NA | 0 | **Max Payload Size**  Maximum TLP payload size.  000: 128bytes 001: 256 bytes  Others: Reserved | DCMPS\_ |  | vcc | 000 | 000 | x |
| 4 | RW | NA | 1b | **Enable Relaxed Ordering**  0: Disable 1: Enable  If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions to indicate that it does not require strong write ordering. | DCERO |  | vcc | 1 | x | x |
| 3 | RW | NA | 0 | **Unsupported Request Reporting Enable**  0: Disable 1: Enable  ((For internal verify reference: @((#TOGGLE=1)) )) | DCURRE |  | vcc | 0 | x | x |
| 2 | RW | NA | 0 | **Fatal Error Reporting Enable**  0: Disable 1: Enable  For a root port, the report of Fatal errors is internal to the root. No external ERR\_FATAL message is generated.  ((For internal verify reference: @((#TOGGLE=1)) )) | DCFERE |  | vcc | 0 | x | x |
| 1 | RW | NA | 0 | **Non-Fatal Error Reporting Enable**  0: Disable 1: Enable  For a root port, the report of Non-Fatal errors is internal to the root. No external ERR\_NONFATAL message is generated.  ((For internal verify reference: @((#TOGGLE=1)) )) | DCNFERE |  | vcc | 0 | x | x |
| 0 | RW | NA | 0 | **Correctable Error Reporting Enable**  0: Disable 1: Enable  For a root port, the report of correctable errors is internal to the root. No external ERR\_COR message is generated.  ((For internal verify reference: @((#TOGGLE=1)) )) | DCCERE |  | vcc | 0 | x | x |

Offset Address: 4B-4Ah (D0F2)   
Device Status 1 Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:6 | RO | NA | 0 | **Reserved** | Rsv\_4b |  | vcc | R | x | x |
| 5 | RO | NA | 0 | **Transactions Pending**  This bit when set indicates that the port has issued Non-Posted Requests on its own behalf (using the Requestor ID of the Port) which have not been completed. | DSTP |  | vcc | 0 | x | x |
| 4 | RO  ((RW)) | NA | 0 | **AUX Power Detected**  0: Not detected 1: Detected  ((For Internal Reference: RW/RO through D0F5 RxF0[0].)) | DSAPD |  | vcc | 0 | x | x |
| 3 | RO | NA | 0 | **Unsupported Request Detected (TL)**  0: Not detected 1: Detected | DSURD |  | vcc | 0 | x | x |
| 2 | RO | NA | 0 | **Fatal Error Detected (TL)**  0: Not detected 1: Detected | DSFED |  | vcc | 0 | x | x |
| 1 | RO | NA | 0 | **Non-Fatal Error Detected (TL)**  0: Not detected 1: Detected | DSNFED |  | vcc | 0 | x | x |
| 0 | RO | NA | 0 | **Correctable Error Detected (TL)**  0: Not detected 1: Detected | DSCED |  | vcc | 0 | x | x |

Offset Address: 4F-4Ch (D0F2)  
Link Capabilities 1 Default Value: 0A01 BC41h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:24 | RO  ((RW)) | NA | 0Ah | **Port Number**  This field indicates the PCI Express Port number for the given PCI Express Link.  ((For Internal Reference: RW when D0F5 RxF0[0] is set to 1.)) | LKPN\_ |  | vcc | x | x | x |
| 23:22 | RO | NA | 0 | **Reserved** | rsv\_31 |  | vcc | R | x | x |
| 21 | RO  ((RW)) | NA | 0 | **Link Bandwidth Notification Capability**  This bit indicates support for the Link Bandwidth Notification status and interrupt mechanism.  ((For Internal Reference: RW when D0F5 RxF0[0] is set to 1.)) | RLBWNTFC |  | vcc | 0b | x | x |
| 20 | RO  ((RW)) | NA | 0 | **Data Link Layer Link Active Reporting Capable**  This bit indicates support of reporting the DL\_Active state of DLCMSM.  ((For Internal Reference: RW when D0F5 RxF0[0] is set to 1.)) | RDL\_AR\_CAP |  | vcc | 0b | x | x |
| 19 | RO  ((RW)) | NA | 0 | **Surprise Down Error Reporting Capable**  This bit indicates support of detecting and reporting a Surprise Down error condition.  ((For Internal Reference: RW when D0F5 RxF0[0] is set to 1.)) | RLCASDERC |  | vcc | 0b | x | x |
| 18 | RO | NA | 0 | **Clock Power Management** | RLCACPM |  | vcc | 0 | x | x |
| 17:15 | RO  ((RW)) | NA | 011b | **L1 Exit Latency**  This field indicates the L1 exit latency (to L0) for the given PCIe Link.  Defined encoding for this latency Tl\_L1 are:  000: Tl\_L1 < 1us  001: 1us <= Tl\_L1< 2us  010: 2us <= Tl\_L1 < 4us  011: 4us <= Tl\_L1 < 8us  100: 8us <= Tl\_L1 < 16us  101: 16us <= Tl\_L1 < 32us  110: 32us <= Tl\_L1 < 64us  111: 64us <= Tl\_L1  ((For Internal Reference: RW when D0F5 RxF0[0] is set to 1.)) | LKL1EL\_ |  | vcc | x | x | x |
| 14:12 | RO((RW)) | NA | 011b | **L0s Exit Latency**  This field indicates the L0s exit latency (to L0) for the given PCIe Link.  Read return value is from following registers:  D2F4 RxE1[2:0] when PE3 in 2.5G/Ts speed.  D2F4 RxE2[2:0] when PE3 in 5.0G/Ts speed. | LKL0SE\_ |  | vcc | x | x | x |
| 11:10 | RO  ((RW)) | NA | 11b | **Active State Link PM (ASPM) Support**  11b: L0s and L1 supported.  ((For Internal Reference: RW when D0F5 RxF0[0] is set to 1.)) | LKAPMS\_ |  | vcc | 11b | x | x |
| 9 | RO  ((RW)) | NA | 0 | **Maximum Link Width Bit 5** | LKMLW\_5 |  | vcc | 0 | x | x |
| 8 | RO  ((RW)) | NA | 0 | **Maximum Link Width Bit 4** | LKMLW\_4 |  | vcc | 0 | x | x |
| 7 | RO  ((RW)) | NA | 0 | **Maximum Link Width Bit 3** | LKMLW\_3 |  | vcc | 0 | x | x |
| 6 | RO  ((RW)) | NA | 1b | **Maximum Link Width Bit 2** | LKMLW\_2 |  | vcc | 1b | x | x |
| 5 | RO  ((RW)) | NA | 0 | **Maximum Link Width Bit 1** | LKMLW\_1 |  | vcc | x | x | x |
| 4 | RO  ((RW)) | NA | 0 | **Maximum Link Width Bit 0** | LKMLW\_0 |  | vcc | x | x | x |
| 3 | RO  ((RW)) | NA | 0 | **Max Link Speed Bit 3**  Max Link Speeds – This field indicates the supported maximum Link speed(s) of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed.  Defined encodings are:  0001b: Supported Link Speeds Vector field bit 0.  0010b: Supported Link Speeds Vector field bit 1.  0011b: Supported Link Speeds Vector field bit 2.  0100b: Supported Link Speeds Vector field bit 3.  0101b: Supported Link Speeds Vector field bit 4.  0110b: Supported Link Speeds Vector field bit 5.  0111b: Supported Link Speeds Vector field bit 6. | LKMAXLS\_ 3 |  | vcc | 0 | x | x |
| 2 | RO  ((RW)) | NA | 0 | **Max Link Speed Bit 2** | LKMAXLS\_ 2 |  | vcc | 0 | x | x |
| 1 | RO  ((RW)) | NA | 0b | **Max Link Speed Bit 1** | LKMAXLS\_ 1 |  | vcc | 0b | x | x |
| 0 | RO  ((RW)) | NA | 1b | **Max Link Speed Bit 0** | LKMAXLS\_ 0 |  | vcc | 1b | x | x |

Offset Address: 51-50h (D0F2)   
Link Control 1 Default Value: 0040h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:12 | RO | NA | 0 | **Reserved** | rsv\_32 |  | vcc | R | x | x |
| 11 | RW | NA | 0 | **Enable Link Autonomous Bandwidth Interrupt**  0: Disable.  1: Enable the generation of an interrupt to indicate that the autonomous bandwidth status bit (Rx53[7] (RLATNMBW) ) has been set.  ((For internal verify reference: @((#TOGGLE=1)) )) | RLABITEN |  | vcc | 0 | x | x |
| 10 | RW | NA | 0 | **Enable Link Bandwidth Management Interrupt**  0: Disable.  1: Enable the generation of an interrupt to indicate that the link bandwidth management status bit (Rx53[6] (RLBWMNGT) ) has been set.  ((For internal verify reference: @((#TOGGLE=1)) )) | RLBMITEN |  | vcc | 0 | x | x |
| 9 | RW | NA | 0 | **Hardware Autonomous Width Control**  0: Hardware can change the link width because of correcting unreliable link operations or power saving issue.  1: Hardware can change the link width only because of correcting unreliable link operations. | RHATNMWD |  | vcc | 0 | x | 0 |
| 8 | RO | NA | 0 | **Enable Clock Power Management**  0: Disable 1: Enable | RLCOCPMEN |  | vcc | 0 | x | x |
| 7 | RW | NA | 0 | **Extended Synch**  0: FCU timer limit is 30us.  No. of FTS ordered set to be transmitted from L0s to L0 is N\_FTS.  No. of TS1 to be transmitted in Recovery.RcvrLock is not limited.  1: FCU timer limit is 120us.  No. of FTS ordered set to be transmitted from L0s to L0 is 4096.  No. of TS1 to be transmitted in Recovery.RcvrLock is at least 1024. | LCES |  | vcc | 0 | 0 | x |
| 6 | RW | NA | 1b | **Common Clock Configuration**  0: Indicates that this port and the component on the opposite end of the link are operating with asynchronous reference clock.  1: Indicates that this port and the component on the opposite end of the link are operating with a distributed common reference clock. | LCCCC |  | vcc | x | x | x |
| 5 | RO | NA | 0 | **Retrain Link**  Link retrain is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state. Hardware will clear this bit to 0 when complete. | LCRL |  | vcc | 0 | x | x |
| 4 | RW | NA | 0 | **Link Disable**  0: Enable the link 1: Disable the link | LCLD |  | vcc | 0 | x | x |
| 3 | RO  ((RW)) | NA | 0 | **Read Completion Boundary**  0: 64 bytes 1: 128 bytes  ((For Internal Reference: RO/RW through D0F5 RxF0[0].)) | LCRCB |  | vcc | 0 | x | x |
| 2 | RO | NA | 0 | **Reserved** | rsv\_33 |  | vcc | R | x | x |
| 1:0 | RW | NA | 00b | **Link Active State PM (ASPM) Control**  00: Disable  01: Enable L0s entry  10: Enable L1 entry  11: Enable L0s and L1 entry | LCAPMS\_ |  | vcc | 00b | 00b | 00b |

Offset Address: 53-52h (D0F2)   
Link Status 1 Default Value: 1000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15 | RO | NA | 0 | **Link Autonomous Bandwidth Status**  This bit is set to 1b to indicate that hardware has autonomously changed link speed or width, without the port transitioning through DL\_Down status, for reasons other than attempt to correct unreliable link operation. | \*RLATNMBW |  | vcc | 0 | x | x |
| 14 | RO | NA | 0 | **Link Bandwidth Management Status**  This bit is asserted when:  1) LTSSM transits from Recovery to L0.  2) Link speed is changed.  3) Link width is changed. | RLBWMNGT |  | vcc | 0 | x | x |
| 13 | RO | NA | 0 | **Data Link Layer Link Active**  0: Inactive 1: Active | \*DL\_ACTIVE |  | vcc | x | x | x |
| 12 | RO  ((RW)) | NA | 1b | **Slot Clock Configuration**  0: Use an independent clock irrespective of the presence of a reference on the connector.  1: Use the same physical reference clock that the platform provides on the connector.  ((For Internal Reference: RO/RW through D0F5RxF0[0].)) | LSSCC |  | vcc | x | x | x |
| 11 | RO | NA | 0 | **Link Training**  This bit indicate that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or the Retrain Link bit is set but Link training has not yet begun. Hardware clears this bit once Link training is complete. | LSLT |  | vcc | 0 | x | x |
| 10 | RO | NA | 0 | **Training Error**  Set when a Link training error occurs. Cleared by hardware upon successfully training of the Link to the L0 Link state. | LSTE |  | vcc | 0 | x | x |
| 9 | RO | NA | 0 | **Negotiated Link Width Bit 5**  Hardwired to 0. | tbd\_28 |  | vcc | 0 | x | x |
| 8:4 | RO((RW)) | NA | 0 | **Negotiated Link Width Bits[4:0]**  Default value set by hardware initial.  00001: x1 00010: x2  00100: x4 01000: x8  01000: x16  Others: Reserved | LSNLW\_ |  | vcc | 0 | x | x |
| 3:0 | RO((RW)) | NA | 0 | **Current Link Speed**  Current Link Speed – This field indicates the negotiated Link speed of the given PCI Express Link.  The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed.  Defined encodings are:  0001: Supported Link Speeds Vector field bit 0.  0010: Supported Link Speeds Vector field bit 1.  0011: Supported Link Speeds Vector field bit 2.  0100: Supported Link Speeds Vector field bit 3.  0101: Supported Link Speeds Vector field bit 4.  0110: Supported Link Speeds Vector field bit 5.  0111: Supported Link Speeds Vector field bit 6.  All other encodings are Reserved.  The value in this field is undefined when the Link is not up. | LSLS\_ |  | vcc | 0 | x | x |

Offset Address: 57-54h (D0F2)   
Slot Capabilities 1 Default Value: 0000 0020h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:19 | RO  ((RW)) | NA | 0 | **Physical Slot Number; Reserved**  Physical slot number attached to the port.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].)) | SLPSN\_ |  | vcc | 0 | x | x |
| 18 | RO  ((RW)) | NA | 0 | **No Command Completed Support**  0: Not supported 1: Supported  ((For Internal Reference: This bit will be write-able when D0F5 RxF0[0] is programmed to 1.)) | RSCANCCS |  | vcc | 0 | x | x |
| 17 | RO  ((RW)) | NA | 0 | **Electromechanical Interlock Present**  0: Not present 1: Present  ((For Internal Reference: This bit will be write-able when D0F5 RxF0[0] is programmed to 1.)) | RSCAEMIP |  | vcc | 0 | x | x |
| 16:15 | RO  ((RW)) | NA | 00b | **Slot Power Limit Scale**  Specify the scale used for the Slot Power Limit Value.  Range of values:  00: 1.0x 01: 0.1x  10: 0.01x 11: 0.001x  This register must be implemented if the Slot Implemented bit is set.  ((For Internal Reference: Write to the field causes the Port to send the Set\_Slot\_Power\_Limit message. RO/RW through D0F5 RxF0[0].)) | RSPLS\_ |  | vcc | 0 | x | x |
| 14:7 | RO  ((RW)) | NA | 0 | **Slot Power Limit Value**  In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.  This register must be implemented if the Slot Implemented bit is set.  ((For Internal Reference: Write to the field causes the Port to send the Set\_Slot\_Power\_Limit message. RO/RW through D0F5 RxF0[0].)) | RSPLV\_ |  | vcc | 0 | x | x |
| 6 | RO  ((RW)) | NA | 0 | **Hot-Plug Capable**  1b indicates that this slot is capable of supporting hot-plug operations.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].))  ((For internal verify reference: @((#TOGGLE=1)) )) | SCHP\_CAP |  | vcc | 0 | x | x |
| 5 | RO  ((RW)) | NA | 1b | **Hot-Plug Surprise**  1b indicates that an adapter present in this slot may be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow such removal without impact on successive software operation.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].))  ((For internal verify reference: @((#TOGGLE=1)) )) | SCHPS |  | vcc | 1 | x | x |
| 4 | RO  ((RW)) | NA | 0 | **Power Indicator Present**  When set to 1b, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].))  ((For internal verify reference: @((#TOGGLE=1)) )) | SCPIP |  | vcc | 0 | x | x |
| 3 | RO  ((RW)) | NA | 0 | **Attention Indicator Present**  When set to 1b, this bit indicates that an Attention Indicator is electrically controlled by the chassis.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].))  ((For internal verify reference: @((#TOGGLE=1)) )) | SCAIP |  | vcc | 0 | x | x |
| 2 | RO | NA | 0 | **MRL Sensor Present**  Reserved | rsv\_36 |  | vcc | 0 | x | x |
| 1 | RO | NA | 0 | **Power Controller Present**  Reserved | rsv\_37 |  | vcc | 0 | x | x |
| 0 | RO  ((RW)) | NA | 0 | **Attention Button Present**  When set to 1b, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].))  ((For internal verify reference: @((#TOGGLE=1)) )) | SCABP |  | vcc | 0 | x | x |

Offset Address: 59-58h (D0F2)   
Slot Control 1 Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:13 | RO | NA | 0 | **Reserved** | rsv\_39 |  | vcc | R | x | x |
| 12 | RW | NA | 0 | **Enable Data Link Layer State Change**  0: Disable 1: Enable  If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed.  ((For internal verify reference: @((#TOGGLE=1)) )) | RDLSCHGEN |  | vcc | 0 | x | x |
| 11 | RO | NA | 0 | **Electromechanical Interlock Control**  0: Disable 1: Enable | RSCOEMIC |  | vcc | 0 | x | x |
| 10 | RW | NA | 0 | **Power Controller Control**  0: Power on 1: Power off  If a power controller is implemented, this bit when written sets the power state of the slot per the defined encodings.  If the Power Controller Implemented field in the Slot Capabilities register is set to 0b, then writes to this field have no effect and the read value of this field is undefined. | SCPCC |  | vcc | 0 | x | x |
| 9:8 | RO/RW | NA | 00b | **Power Indicator Control**  If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state.  Reads of this field must reflect the value from the latest write,even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined.  Defined encodings are:  00: Reserved 01: On  10: Blink 11: Off  This bit is RW when D0F2 Rx54[4] is set to 1.  Note: The default value of this field must be one of the non-Reserved values.  @((guardbit = SCPIP D0F2 RX54[4]))  ((For Internal Reference:  00: Reserved 01: On  10: Blink 11: Off  Writes to this field cause the port to send the appropriate POWER\_INDICATOR\_\* Message.)) | SCPIC\_ |  | vcc | 0 | x | x |
| 7:6 | RO/RW | NA | 00b | **Attention Indicator Control**  If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state.  Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined.  Defined encodings are:  00: Reserved 01: On  10: Blink 11: Off  This bit is RW when D0F2 Rx54[3] is set to 1.  Note: The default value of this field must be one of the non-Reserved values.  @((guardbit = SCAIP D0F2 RX54[3]))  ((For Internal Reference:  00: Reserved 01: On  10: Blink 11: Off  Writes to this field cause the ort to send the appropriate ATTENTION\_INDICATOR\_\* Message.)) | SCAIC\_ |  | vcc | 0 | x | x |
| 5 | RO/RW | NA | 0 | **Enable Hot-Plug Interrupt**  0: If the Hot Plug Capable field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.  1: When set to 1b, this bit enables generation of an interrupt on enabled hot-plug events.  This bit is RW when D0F2 Rx54[6] is set to 1.  @((guardbit = SCHP\_CAP D0F2 RX54[6]))  ((For Internal Reference:  0: Disable 1: Enable  his bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.)) | SCHPIE |  | vcc | 0 | x | x |
| 4 | RW | NA | 0 | **Enable Command Completed Interrupt**  0: If Command Completed notification is not supported, this bit must be hardwired to 0b.  1: When set to 1b, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller.  ((For Internal Reference:  0: Disable 1: Enable  This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.)) | SCCCIE |  | vcc | 0 | x | x |
| 3 | RW | NA | 0 | **Enable Presence Detect Change**  When set to 1b, this bit enables software notification on a presence detect changed event.  ((For Internal Reference:  0: Disable 1: Enable  This bit when set enables the generation of Hot-Plug interrupt or WakeuPEvent on a presence detect changed event.)) | SCPDCE |  | vcc | 0 | x | x |
| 2 | RO | NA | 0 | **Enable MRL Sensor Change**  Reserved  ((For Internal Reference:  0: Disable 1: Enable )) | rsv\_40 |  | vcc | 0 | x | x |
| 1 | RO | NA | 0 | **Enable Power Fault Detected**  Reserved  ((For Internal Reference:  0: Disable 1: Enable )) | rsv\_41 |  | vcc | 0 | x | x |
| 0 | RO/RW | NA | 0 | **Enable Attention Button Pressed**  When set to 1b, this bit enables software notification on an attention button pressed event. This bit is RW when D0F2 Rx54[0] is set to 1.  ((For Internal Reference:  0: Disable 1: Enable  This bit when set enables the generation of Hot-Plug interrupt or WakeuPEvent on an Attention Button pressed event.))  @((guardbit = SCABP D0F2 Rx54[0])) | SCABPE |  | vcc | 0 | x | x |

Offset Address: 5B-5Ah (D0F2)   
Slot Status 1 Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:9 | RO | NA | 0 | **Reserved** | rsv\_42 |  | vcc | R | x | x |
| 8 | RO | NA | 0 | **Data Link Layer State Changed**  0: No state changed 1: State changed | RDLSCHG |  | vcc | 0 | x | x |
| 7 | RO | NA | 0 | **Electromechanical Interlock Status** | RSSEMIS |  | vcc | 0 | x | x |
| 6 | RO | NA | 0 | **Presence Detect State**  0: Slot empty  1: Card present in slot | SPDCST |  | vcc | 0 | x | x |
| 5 | RO | NA | 0 | **MRL (Manually Operated Retention Latch) Sensor State**  Reserved | rsv\_43 |  | vcc | 0 | x | x |
| 4 | RO | NA | 0 | **Command Completed**  0: Not completed 1: Completed | SSCC |  | vcc | 0 | x | x |
| 3 | RO | NA | 0 | **Presence Detect Change**  0: Not changed 1: Changed | SPDC |  | vcc | 0 | x | x |
| 2 | RO | NA | 0 | **MRL Sensor Change**  0: Not changed 1: Changed | tbd\_29 |  | vcc | 0 | x | x |
| 1 | RO | NA | 0 | **Power Fault Detected**  0: Not changed 1: Changed | tbd\_30 |  | vcc | 0 | x | x |
| 0 | RO | NA | 0 | **Attention Button Pressed**  0: No state changed 1: State changed | SSABP |  | vcc | 0 | x | x |

Offset Address: 5D-5Ch (D0F2)   
Root Control Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:5 | RO | NA | 0 | **Reserved** | Rsv\_5c\_5 |  | vcc | R | x | x |
| 4 | RW | NA | 0 | **Enable CRS Software Visibility**  0: Disable.  1: Enable the root port to return Configuration Request Retry Status (CRS) completion status to software.  ((For internal verify reference: @((#TOGGLE=1)) )) | RCCRSSVE |  | vcc | 0 | x | x |
| 3 | RW | NA | 0 | **Enable PME Interrupt**  0: Disable.  1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state. | RCPMEIE |  | vcc | 0 | x | x |
| 2 | RW | NA | 0 | **Enable System Error on Fatal Error**  0: Disable.  1: Enable generation of a System Error if a Fatal Error (ERR\_FATAL) is reported by any of the devices in the hierarchy associated with the root port, or by the root Port itself. | RCSEFEE |  | vcc | 0 | x | x |
| 1 | RW | NA | 0 | **Enable System Error on Non-Fatal Error**  0: Disable.  1: Enable generation of a System Error if a Non-Fatal Error (ERR\_NONFATAL) is reported by any of the devices in the hierarchy associated with the root port, or by the root port itself. | RCSENFEE |  | vcc | 0 | x | x |
| 0 | RW | NA | 0 | **Enable System Error on Correctable Error**  0: Disable.  1: Enable generation of a System Error if a Correctable Error (ERR\_COR) is reported by any of the devices in the hierarchy associated with the root port, or by the root port itself. | RCSECEE |  | vcc | 0 | x | x |

Offset Address: 5F-5Eh (D0F2)   
Root Capabilities Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:1 | RO | NA | 0 | **Reserved** | rsv\_44\_5e |  | vcc | R | x | x |
| 0 | RO  ((RW)) | NA | 0 | **Configuration Request Retry Status (CRS) Software Visibility**  0: Disable. The Root Port cannot return CRS completion status to software.  1: Enable. The Root Port will return CRS completion status to software.  ((For Internal Reference: RO/RW through D0F5 RxF0[0].))  ((For internal verify reference: @((#TOGGLE=1)) )) | RSCRSSFV |  | vcc | 0 | x | x |

Offset Address: 63-60h (D0F2)   
Root Status Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:18 | RO | NA | 0 | **Reserved** | rsv\_45 |  | vcc | R | x | x |
| 17 | RO | NA | 0 | **PME Pending**  0: No pending PME.  1: Indicates another PME is pending when the PME Status (bit 16) is set. | RSPP |  | vcc | 0 | x | x |
| 16 | RO | NA | 0 | **PME Status**  Indicates that the PME is asserted by the Requestor ID indicated in PME Requestor ID (bits[15:0]). | RSPS |  | vcc | 0 | x | x |
| 15:0 | RO | NA | 0 | **PME Requester ID**  The Requestor ID of the last PME Requestor. | RSPRID\_ |  | vcc | 0 | x | x |

Offset Address: 67-64h (D0F2)   
Device Capabilities 2 Default Value: 0000 0010h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:20 | RO | NA | 0 | **Reserved** | Rsv\_64\_6 |  | vcc | R | x | x |
| 19:18 | RO  ((RW)) | NA | 0 | **OBFF Supported**  00: OBFF not supported.  01: OBFF supported using Message signaling only.  10: OBFF supported using WAKE# signaling only.  11: OBFF supported using WAKE# and Message signaling. | ROBFFSP\_ |  | vcc | 0 | x | x |
| 17:12 | RO | NA | 0 | **Reserved** | Rsv\_64\_12 |  | vcc | R | x | x |
| 11 | RO  ((RW)) | NA | 0 | **LTR Mechanism Supported**  A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. | RLTRSP |  | vcc | 0 | x | x |
| 10:6 | RO | NA | 0 | **Reserved** | Rsv\_64\_10 |  | vcc | x | x | x |
| 5 | RO  ((RW)) | NA | 0 | **Alternative Routing-ID Interpretation (ARI) Forwarding Supported**  0: Not supported 1: Supported  ARI is used to increase the number of functions supported by single device. | RARISP |  | vcc | 0 | x | x |
| 4 | RO  ((RW)) | NA | 1b | **Completion Timeout Disable Supported**  0: Not support Completion Timeout Disable.  1: Support Completion Timeout Disable.  ((For Internal Reference: This bit will be write-able when D0F5 RxF0[0] is programmed to 1.)) | tbd\_31 |  | vcc | 1 | x | x |
| 3:0 | RO | NA | 0 | **Completion Timeout Ranges Supported**  0: Not supported 1: Supported  ((For Internal Reference: The timeout value is in the range from 50us to 50ms, compliant with PCIe 1.1)) | tbd\_32 |  | vcc | 0 | x | x |

Offset Address: 69-68h (D0F2)   
Device Control 2 Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15 | RO | NA | 0 | **Reserved** | rsv\_46 |  | vcc | R | x | x |
| 14:13 | RW | NA | 0 | **OBFF Enable**  00: Disabled  01: Enabled using Message signaling [Variation A]  10: Enabled using Message signaling [Variation B]  11: Enabled using WAKE# signaling | ROBFFEN\_ |  | vcc | 0 | x | x |
| 12:11 | RO | NA | 0 | **Reserved** | Rsv\_68\_11 |  | vcc | R | x | x |
| 10 | RW | NA | 0 | **LTR Mechanism Enable**  When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism | RLTREN |  | vcc | 0 | x | x |
| 9:6 | RO | NA | 0 | **Reserved** | Rsv\_68\_6 |  | vcc | R | x | x |
| 5 | RO/RW | NA | 0 | **Enable ARI Forwarding**  0: Disable. Check device number being 0 when turning downstream Type1 configuration to Type 0 configuration.  1: Enable. Never check device number when turning downstream Type1 configuration to Type 0 configuration.  This bit is RW when D0F2 Rx64[5] is set to 1.  ((For Internal Reference: Internal design guideline  Default value of this bit is 0b. Must be hardwired to 0b if the ARI Forwarding Supported bit (D0F2 Rx64[5]) is 0b.))  @((guardbit=RARISP D0F2 RX64[5])) | RARIEN |  | vcc | 0 | x | x |
| 4 | RW | NA | 0 | **Completion Timeout Disable Control**  0: Enable completion timeout function.  1: Disable completion timeout function. | \*RDISCPLTM |  | vcc | 0 | 0 | x |
| 3:0 | RO | NA | 0 | **Completion Timeout Value**  ((For Internal Reference: Not support completion timeout programmability then hardwire this field to 0000b.)) | tbd\_33 |  | vcc | 0 | x | x |

Offset Address: 6B-6Ah (D0F2)   
Device Status 2 Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:0 | RO | NA | 0 | **Reserved** | rsv\_47 |  | vcc | R | x | x |

Offset Address: 6F-6Ch (D0F2)   
Link Capabilities 2 Default Value: 0001 0202h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:19 | RO | NA | 0 | **Reserved** | rsv\_6c\_31 |  | vcc | R | x | x |
| 18 | RO  ((RW)) | NA | 0 | **Lower SKP OS Reception Supported Speeds Vector**  If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS.  Bit definitions within this field are:  Bit 0: 2.5 GT/s Bit 1: 5.0 GT/s  Bit 2: 8.0 GT/s Bits 6:3: RsvdP | RLOW\_SKP\_REC\_SUPPORT\_2 |  | vcc | x | x | X |
| 17 | RO  ((RW)) | NA | 0 | **Lower SKP OS Reception Supported Speeds Vector** | RLOW\_SKP\_REC\_SUPPORT\_1 |  | vcc | x | x | X |
| 16 | RO  ((RW)) | NA | 1b | **Lower SKP OS Reception Supported Speeds Vector** | RLOW\_SKP\_REC\_SUPPORT\_0 |  | vcc | x | x | X |
| 15:12 | RO | NA | 0 | **Reserved** | rsv\_6c\_15 |  | vcc | R | x | x |
| 11 | RO  ((RW)) | NA | 0 | **Lower SKP OS Generation Supported Speeds Vector**  If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate.  Bit definitions within this field are:  Bit 0: 2.5 GT/s Bit 1: 5.0 GT/s  Bit 2: 8.0 GT/s | RLOW\_SKP\_GEN\_SUPPORT\_2 |  | vcc | x | x | x |
| 10 | RO  ((RW)) | NA | 0 | **Lower SKP OS Generation Supported Speeds Vector** | RLOW\_SKP\_GEN\_SUPPORT\_1 |  | vcc | x | x | X |
| 9 | RO  ((RW)) | NA | 1b | **Lower SKP OS Generation Supported Speeds Vector** | RLOW\_SKP\_GEN\_SUPPORT\_0 |  | vcc | x | x | X |
| 8 | RO | NA | 0 | **CrossLink Supported**  0 indicates the RP does not support CrossLink. | Rsv\_6c\_8 |  | vcc | 0 | x | x |
| 7 | RO | NA | 0 | **Supported Link Speed Vector Bit 6**  Reserved | LKMLS\_ 6 |  | vcc | 0 | x | x |
| 6 | RO | NA | 0 | **Supported Link Speed Vector Bit 5**  Reserved | LKMLS\_ 5 |  | vcc | 0 | x | x |
| 5 | RO | NA | 0 | **Supported Link Speed Vector Bit 4**  Reserved | LKMLS\_ 4 |  | vcc | 0 | x | x |
| 4 | RO | NA | 0 | **Supported Link Speed Vector Bit 3**  Reserved | LKMLS\_ 3 |  | vcc | 0 | x | x |
| 3 | RO  ((RW)) | NA | 0 | **Supported Link Speed Vector Bit 2, 8.0GT/s** | LKMLS\_2 |  | vcc | 0 | x | x |
| 2 | RO  ((RW)) | NA | 0 | **Supported Link Speed Vector Bit 1, 5.0GT/s** | LKMLS\_1 |  | vcc | 0b | x | x |
| 1 | RO  ((RW)) | NA | 1b | **Supported Link Speed Vector Bit 0, 2.5 GT/s** | LKMLS\_ 0 |  | vcc | 1b | x | x |
| 0 | RO | NA | 0 | **Reserved** | rsv\_6c\_0 |  | vcc | R | x | x |

Offset Address: 71-70h (D0F2)   
Link Control 2 Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:12 | RW | NA | 0 | **Compliance Preset / De-emphasis**  For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b.  For 5.0 GT/s Data Rate: This bit field sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b.  Defined Encodings are:  0001b: -3.5 dB  0000b: -6 dB | CMPPSDEEMPHS\_ |  | vcc | 0 | x | x |
| 11 | RW | NA | 0 | **SKP Ordered Set (SOS) Transmission between Compliance Patterns**  0: No SOS is sending between the (modified) compliance patterns.  1: The LTSSM is sending SOS periodically in between the (modified) compliance patterns. | RCMPSOS |  | vcc | 0 | x | x |
| 10 | RW | NA | 0 | **Modified Compliance Pattern Set Bit**  0: Device transmits normal compliance pattern if LTSSM enters Polling.Compliance state.  1: Device transmits modified compliance pattern if LTSSM enters Polling.Compliance state. | PMDCMPSET |  | vcc | 0 | x | x |
| 9 | RW | NA | 0 | **Transmit Voltage Margin Setting**  Bits [9:7]  000: Normal operating range.  001: 800-1200 mV for full swing and 400-700 mV for half-swing.  010 ~ (n-1): Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200-400 mV for full-swing and 100-200 mV for half-swing.  n ~ 111: Reserved. | TXMGN \_2 |  | vcc | 0 | x | x |
| 8 | RW | NA | 0 | **Transmit Voltage Margin Setting**  Bits [9:7]  000: Normal operating range.  001: 800-1200 mV for full swing and 400-700 mV for half-swing.  010 ~ (n-1): Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200-400 mV for full-swing and 100-200 mV for half-swing.  n ~ 111: Reserved. | TXMGN\_1 |  | vcc | 0 | x | x |
| 7 | RW | NA | 0 | **Transmit Voltage Margin Setting**  Bits [9:7]  000: Normal operating range.  001: 800-1200 mV for full swing and 400-700 mV for half-swing.  010 ~ (n-1): Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200-400 mV for full-swing and 100-200 mV for half-swing.  n ~ 111: Reserved. | TXMGN\_0 |  | vcc | 0 | x | x |
| 6 | RO  ((RW)) | NA | 0 | **Selectable De-emphasis**  0: -6 db 1: -3.5db  When the link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an upstream component. | SELDEEMPHS |  | vcc | 0 | x | x |
| 5 | RW | NA | 0 | **Disable Hardware Autonomous Speed**  0: Enable hardware autonomous speed negotiation.  1: Disable hardware autonomous speed negotiation. | RHATNMSD |  | vcc | 0 | x | 0 |
| 4 | RW | NA | 0 | **Enter Compliance**  0: Normal negotiation.  1: Force to polling.compliance. | PCMPSET |  | vcc | 0 | x | x |
| 3 | RW | NA | 0 | **Target Link Speed Bit 3** | LKTGLS\_3 |  | vcc | 0 | 0 | 0 |
| 2 | RW | NA | 0 | **Target Link Speed Bit 2** | LKTGLS\_ 2 |  | vcc | 0 | 0 | 0 |
| 1 | RW | NA | 0 | **Target Link Speed Bit 1** | LKTGLS\_ 1 |  | vcc | 0 | 0 | 0 |
| 0 | RW | NA | 0 | **Target Link Speed Bit 0** | LKTGLS\_ 0 |  | vcc | 0 | 0 | 0 |

Offset Address: 73-72h (D0F2)   
Link Status 2 Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:6 | RO | NA | 0 | **Reserved** | rsv\_49 |  | vcc | R | x | x |
| 5 | RO | NA | 0 | **Request the Link Equalization Process**  This bit is Set to 1 by hardware to request the Link equalization process to be performed on the Link. | EQREQ |  | vcc | x | x | x |
| 4 | RO | NA | 0 | **Transmitter Equalization Procedure Completed -Phase 3**  1: Phase 3 of the Transmitter Equalization procedure has successfully completed. | EQCOMPLE3 |  | vcc | x | x | x |
| 3 | RO | NA | 0 | **Transmitter Equalization Procedure Completed -Phase 2**  1: Phase 2 of the Transmitter Equalization procedure has successfully completed. | EQCOMPLE2 |  | vcc | x | x | x |
| 2 | RO | NA | 0 | **Transmitter Equalization Procedure Completed -Phase 1**  1: Phase 1 of the Transmitter Equalization procedure has successfully completed. | EQCOMPLE1 |  | vcc | x | x | x |
| 1 | RO | NA | 0 | **Transmitter Equalization Procedure Completed**  1: Transmitter Equalization procedure has completed. | EQCOMPLE |  | vcc | x | x | x |
| 0 | RO | NA | 0 | **Current Link De-emphasis Level**  0: -6 db 1: -3.5db | CURDEEMPHS |  | vcc | x | x | x |

Offset Address: 74-7Fh (D0F2) – Reserved

Reserved for PCIe Slot Capabilities 2, Slot Control 2 and Slot Status 2 Register

### Reserved for PCI Power Management Capability Structure Registers (80-87h)

Offset Address: 83-80h (D0F2)   
Power Management Capabilities Default Value: C822 0001h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:27 | RO  ((RW)) | NA | 11001b | **PME Support**  0: Not supported 1: Supported  Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).  ((For Internal Reference: RW when D0F5 RxF0[0]=1.)) | PMCPME\_ |  | vcc | 19h | x | x |
| 26 | RO  ((RW)) | NA | 0 | **D2 Support**  0: Not supported 1: Supported  ((For Internal Reference: RW when D0F5 RxF0[0]=1.)) | PMCD2S |  | vcc | 0 | x | x |
| 25 | RO  ((RW)) | NA | 0 | **D1 Support**  0: Not supported 1: Supported  ((For Internal Reference: RW when D0F5 RxF0[0]=1.)) | PMCD1S |  | vcc | 0 | x | x |
| 24:22 | RO  ((RW)) | NA | 0 | **AUX Current**  ((For Internal Reference: This bit will be write-able when D0F5 RxF0[0] is programmed to 1.)) | PMCAUXC\_ |  | vcc | 0 | x | x |
| 21 | RO  ((RW)) | NA | 1b | **Device Specific Initialization**  Do not program.  ((For Internal Reference: RW when D0F5 RxF0[0]=1.)) | PMCDSI |  | vcc | 1 | x | x |
| 20:19 | RO | NA | 0 | **Reserved** | rsv\_53 |  | vcc | R | x | x |
| 18:16 | RO | NA | 010b | **Version** | tbd\_34 |  | vcc | 010b | x | x |
| 15:8 | RO((RW)) | NA | 00h | **Next Capability Pointer** | tbd\_35 |  | vcc | 00h | x | x |
| 7:0 | RO | NA | 01h | **Capability ID**  01h indicates extended capability ID for the advanced error reporting capability. | tbd\_36 |  | vcc | 01h | x | x |

Offset Address: 87-84h (D0F2)   
Power Management Status / Control Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:24 | RO | NA | 0 | **Power Management Data** | tbd\_37 |  | vcc | R | x | x |
| 23 | RO  ((RW)) | NA | 0 | **Enable Bus Power / Clock Control**  0: Disable 1: Enable  ((For Internal Reference: RO/RW through D0F5 RxF0[0].)) | tbd\_38 |  | vcc | x | x | x |
| 22 | RO  ((RW)) | NA | 0 | **B2 / B3 Support**  ((For Internal Reference: RO/RW through D0F5 RxF0[0].)) | tbd\_39 |  | vcc | x | x | x |
| 21:16 | RO | NA | 0 | **Reserved** | rsv\_54 |  | vcc | R | x | x |
| 15 | RO | NA | 0 | **PME Status**  This bit’s setting is not modified by hot, warm or cold reset. | PMESD |  | vcc | 0 | x | x |
| 14:13 | RO | NA | 0 | **Data Scale** | tbd\_40 |  | vcc | 0 | x | x |
| 12:9 | RO | NA | 0 | **Data Select** | tbd\_41 |  | vcc | 0 | x | x |
| 8 | RW | NA | 0 | **PME Enable**  0: Disable 1: Enable  This bit’s setting is not modified by hot, warm or cold reset.  ((For internal verify reference: @((#TOGGLE=1)) )) | PMEEN |  | vcc | 0 | x | x |
| 7:2 | RO | NA | 0 | **Reserved** | rsv\_55 |  | vcc | R | x | x |
| 1:0 | RW | NA | 00b | **Power State**  00: D0 01: D1  10: D2 11: D3 hot | PWSD\_ |  | vcc | 0 | x | x |

### Reserved Registers (88-8Fh)

Offset Address: 8B-88h (D0F2)  
Reserved ((Internal-RW)) Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RW | NA | 0 | **Reserved**  ((Writing 1 or 0 to these bits does not change any behavior of this chip.)) | Rx88[31:0] |  | vcc | 0 | x | x |

Offset Address: 8F-8Ch (D0F2)  
Reserved ((Internal-RW)) Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:0 | RW | NA | 0 | **Reserved**  ((Writing 1 or 0 to these bits does not change any behavior of this chip.)) | Rx8C[31:0] |  | vcc | 0 | x | x |

@((REG\_GROUP (System SVADDVAD Control): RANGE=(90h,3FFh)))























































































































































































































































































































































































































































































































































































































































































SVADLimit = highest SVAD limit address

* + SVAD limit address = N \* 256M  - 1

MemLimit +1 = highest SVAD limit target to memory(RTOPA)

* + MemLimit +1 = N \* 256M

B4GMemLimit +1 = Below 4G highest memory limit(RLOWTOPA)

* + B4GMemLimit +1 = N \* 256M

B4GMMIOBase = min(MMIOB2G,MMIO2T4G)

### MMIOB2G Decode (90-B7h)

Offset Address: 93-90h (D0F2)  
MMIOCFG decoder Default Value: 0nnn nn00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **RDID\_RID\_LOCK\_D0F2**  ((For Internal Reference: DID\_RID\_lock\_bit  0: DeviceID, RevisionID and RDID\_RID\_LOCK\_D0F2 is RW;  1: DeviceID, RevisionID and RDID\_RID\_LOCK\_D0F2 is RO;  @((#control\_lock = lock\_port RDID\_RID\_LOCK\_D0F2))   )) | RDID\_RID\_LOCK\_D0F2 |  | vcc | 0 | x | x |
| 30 | RWL | RO | 0 | **RSVAD\_LOCK**  This is a lock bit for the related register “SVAD”:  1: When this ((Lock\_bit)) is set to 1, the SVAD related register is RO.  0: When this ((Lock\_bit)) is set to 0, the SVAD related regisrer is RW  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK))  @((#control\_txt\_lock = LOCK\_SMRAM))  @((#control\_txt\_unlock = UNLOCK\_SMRAM))   ))  ((For Internal Reference: @((#USER=HIF))  )) | RSVAD\_LOCK |  | vcc | x | x | x |
| 29 | RWL | RO | 0 | **RVID\_DID\_LOCK\_D0F2**  ((For Internal Reference: VID\_DID\_lock\_bit  0: VendorID and RVID\_DID\_LOCK\_D0F2 is RW;  1: VendorID and RVID\_DID\_LOCK\_D0F2 is RO;  @((#control\_lock = lock\_port RVID\_DID\_LOCK\_D0F2))  @((#control\_default = NB\_VID\_DID\_LOCK))  )) | RVID\_DID\_LOCK\_D0F2 |  | vcc | x | x | x |
| 28 | RWL | RO | 0 | **C2M\_Tseg\_range \_LOCK\_D0F2**  0: C2M Tseg range control is RW;  1: C2M Tseg range Protection control  is RO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [28] is set to 0. @((#control\_lock=lock\_port RSVAD\_TSEGLOCK )) ))  ((For Internal Reference: The register is for SVAD.)) ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_TSEGLOCK |  | vcc | x | x | x |
| 27:8 | RWL | RO | ROMSIP | **MMIOCFG base**  This 20 bits are MMIOCFG base address  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[59:40]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFGBASE[45:26] |  | vcc | x | x | x |
| 7:3 | RO | NA | 0 | **Reserved** | Rx90[7:3] |  | vcc | R | x | x |
| 2 | RWL | RO | 0 | **RCLASS\_CODE\_LOCK\_D0F2**  ((For Internal Reference: ClassCode\_lock\_bit  0: ClassCode and RCLASS\_CODE\_LOCK\_D0F2 is RW;  1: ClassCode and RCLASS\_CODE\_LOCK\_D0F2 is RO;  @((#control\_lock = lock\_port RCLASS\_CODE\_LOCK\_D0F2))   )) | RCLASS\_CODE\_LOCK\_D0F2 |  | vcc | x | x | x |
| 1 | RWL | RO | 0 | **C2M\_CDEFseg\_range\_LOCK\_D0F2**  0: C2M CDEFGseg range control is RW;  1: C2M CDEFseg range Protection control  is RO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0. @((#control\_lock=lock\_port RSVAD\_CDEFSEGLOCK )) ))  ((For Internal Reference: The register is for SVAD.)) ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_CDEFSEGLOCK |  | vcc | x | x | x |
| 0 | RO | NA | 0 | **Reserved** | Rx90[0] |  | vcc | R | x | x |

Offset Address: 97-94h (D0F2)  
MMIOCFG limit address Default Value:nnnn nnnnh

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:29 | RO | NA | 0 | **Reserved** | Rx94[31:29] |  | vcc | R | x | x |
| 28:24 | RWL | RO | ROMSIP | **MMIOCFG SN3 bus number limit**  This 5 bits are sub node3 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[24:20]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N3\_LIMIT [27:23] |  | vcc | x | x | x |
| 23:21 | RO | NA | 0 | **Reserved** | Rx94[23:21] |  | vcc | R | x | x |
| 20:16 | RWL | RO | ROMSIP | **MMIOCFG SN2 bus number limit**  This 5 bits are sub node2 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[29:25]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N2\_LIMIT [27:23] |  | vcc | x | x | x |
| 15:13 | RO | NA | 0 | **Reserved** | Rx94[15:13] |  | vcc | R | x | x |
| 12:8 | RWL | RO | ROMSIP | **MMIOCFG SN1 bus number limit**  This 5 bits are sub node1 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[34:30]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N1\_LIMIT[27:23] |  | vcc | x | x | x |
| 7:5 | RO | NA | 0 | **Reserved** | Rx94[7:5] |  | vcc | R | x | x |
| 4:0 | RWL | RO | ROMSIP | **MMIOCFG SN0 bus number limit**  This 5 bits are sub node0 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[39:35])) ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N0\_LIMIT[27:23] |  | vcc | x | x | x |

Offset Address: 9B-98h (D0F2)  
MMIOCFG limit address Default Value: nnnn nnnnh

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:29 | RO | NA | 0 | **Reserved** | Rx98[31:29] |  | vcc | R | x | x |
| 28:24 | RWL | RO | ROMSIP | **MMIOCFG SN7 bus number limit**  This 5 bits are sub node7 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[4:0]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N7\_LIMIT [27:23] |  | vcc | x | x | x |
| 23:21 | RO | NA | 0 | **Reserved** | Rx98[23:21] |  | vcc | R | x | x |
| 20:16 | RWL | RO | ROMSIP | **MMIOCFG SN6 bus number limit**  This 5 bits are sub node6 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[9:5]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N6\_LIMIT [27:23] |  | vcc | x | x | x |
| 15:13 | RO | NA | 0 | **Reserved** | Rx98[15:13] |  | vcc | R | x | x |
| 12:8 | RWL | RO | ROMSIP | **MMIOCFG SN5 bus number limit**  This 5 bits are sub node5 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[14:10]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N5\_LIMIT[27:23] |  | vcc | x | x | x |
| 7:5 | RO | NA | 0 | **Reserved** | Rx98[7:5] |  | vcc | R | x | x |
| 4:0 | RWL | RO | ROMSIP | **MMIOCFG SN4 bus number limit**  This 5 bits are sub node4 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP1, HW\_DATA = ROMSIP\_VKCFG\_DATA[19:15]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N4\_LIMIT[27:23] |  | vcc | x | x | x |

Offset Address: 9F-9Ch (D0F2)  
MMIOCFG limit address Default Value: nnnn nnnnh

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:29 | RO | NA | 0 | **Reserved** | Rx9C[31:29] |  | vcc | R | x | x |
| 28:24 | RWL | RO | ROMSIP | **MMIOCFG SN11 bus number limit**  This 5 bits are sub node11 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[48:44]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N11\_LIMIT [27:23] |  | vcc | x | x | x |
| 23:21 | RO | NA | 0 | **Reserved** | Rx9C[23:21] |  | vcc | R | x | x |
| 20:16 | RWL | RO | ROMSIP | **MMIOCFG SN10 bus number limit**  This 5 bits are sub node10 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[53:49]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N10\_LIMIT [27:23] |  | vcc | x | x | x |
| 15:13 | RO | NA | 0 | **Reserved** | Rx9C[15:13] |  | vcc | R | x | x |
| 12:8 | RWL | RO | ROMSIP | **MMIOCFG SN9 bus number limit**  This 5 bits are sub node9 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[58:54]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N9\_LIMIT[27:23] |  | vcc | x | x | x |
| 7:5 | RO | NA | 0 | **Reserved** | Rx9C[7:5] |  | vcc | R | x | x |
| 4:0 | RWL | RO | ROMSIP | **MMIOCFG SN8 bus number limit**  This 5 bits are sub node8 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[63:59]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N8\_LIMIT[27:23] |  | vcc | x | x | x |

Offset Address: A3-A0h (D0F2)   
MMIOCFG limit address Default Value: nnnn nnnnh

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:29 | RO | NA | 0 | **Reserved** | RxA0[31:29] |  | vcc | R | x | x |
| 28:24 | RWL | RO | ROMSIP | **MMIOCFG SN15 bus number limit**  This 5 bits are sub node15 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[28:24]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N15\_LIMIT [27:23] |  | vcc | x | x | x |
| 23:21 | RO | NA | 0 | **Reserved** | RxA0[23:21] |  | vcc | R | x | x |
| 20:16 | RWL | RO | ROMSIP | **MMIOCFG SN14 bus number limit**  This 5 bits are sub node14 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[33:29]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N14\_LIMIT [27:23] |  | vcc | x | x | x |
| 15:13 | RO | NA | 0 | **Reserved** | RxA0[15:13] |  | vcc | R | x | x |
| 12:8 | RWL | RO | ROMSIP | **MMIOCFG SN13 bus number limit**  This 5 bits are sub node13 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[38:34]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N13\_LIMIT[27:23] |  | vcc | x | x | x |
| 7:5 | RO | NA | 0 | **Reserved** | RxA0[7:5] |  | vcc | R | x | x |
| 4:0 | RWL | RO | ROMSIP | **MMIOCFG SN12 bus number limit**  This 5 bits are sub node12 MMIOCFG bus number limit.  ((For Internal ROMSIP handling: HW\_EN = SELSIP2, HW\_DATA = ROMSIP\_VKCFG\_DATA[43:39]))  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOCFG\_N12\_LIMIT[27:23] |  | vcc | x | x | x |

Offset Address: A7-A4h (D0F2)   
MMIOB2G decoder Default Value:0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:4 | RO | NA | 0 | **Reserved** | RxA4[31:4] |  | vcc | R | x | x |
| 3:1 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) base address** MMIOB2G base address, A[39:32] are fixed to 0, A[31] is fixed to 0, A[30:28] are programmable, A[27:0] are fixed to 0. MMIOB2G Limit address is fixed to 2G-1, when MMIOB2G is valid, any address X hit MMIOB2G range( MMIOB2G\_base <= X <=MMIOB2G\_Limit) is claimed by MMIO decoder. ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0. @((#control\_lock=lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.)) ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GBASE[30:28] |  | vcc | x | x | x |
| 0 | RWL | RO | 0 | **MMIO Below 2G disable**  **1: MMIO Below 2G is invalid**  **0: MMIO Below 2G is valid**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2G\_DIS |  | vcc | x | x | x |

Offset Address: AB-A8h (D0F2)   
MMIOB2G decoder Default Value:0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry7 target node**  A[30:26]==5’d7: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry6 target node**  A[30:26]==5’d6: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry5 target node**  A[30:26]==5’d5: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry4 target node**  A[30:26]==5’d4: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry3 target node**  A[30:26]==5’d3: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry2 target node**  A[30:26]==5’d2: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry1 target node**  A[30:26]==5’d1: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry0 target node**  A[30:26]==5’d0: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ0[3:0] |  | vcc | x | x | x |

Offset Address: AF-ACh (D0F2)   
MMIOB2G decoder Default Value:0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry15 target node**  A[30:26]==5’d15: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry14 target node**  A[30:26]==5’d14: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry13 target node**  A[30:26]==5’d13: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry12 target node**  A[30:26]==5’d12: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry11 target node**  A[30:26]==5’d11: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry10 target node**  A[30:26]==5’d10: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry9 target node**  A[30:26]==5’d9: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry8 target node**  A[30:26]==5’d8: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ8[3:0] |  | vcc | x | x | x |

Offset Address: B3-B0h (D0F2)   
MMIOB2G decoder Default Value:0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry23 target node**  A[30:26]==5’d23: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ23[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry22 target node**  A[30:26]==5’d22: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ22[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry21 target node**  A[30:26]==5’d21: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ21[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry20 target node**  A[30:26]==5’d20: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ20[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry19 target node**  A[30:26]==5’d19: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ19[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry18 target node**  A[30:26]==5’d18: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ18[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry17 target node**  A[30:26]==5’d17: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ17[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry16 target node**  A[30:26]==5’d16: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ16[3:0] |  | vcc | x | x | x |

Offset Address: B7-B4h (D0F2)   
MMIOB2G decoder Default Value:0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry31 target node**  A[30:26]==5’d31: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ31[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry30 target node**  A[30:26]==5’d30: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ30[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry29 target node**  A[30:26]==5’d29: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ29[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry28 target node**  A[30:26]==5’d28: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ28[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry27 target node**  A[30:26]==5’d27: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ27[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry26 target node**  A[30:26]==5’d26: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ26[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry25 target node**  A[30:26]==5’d25: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ25[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MMIO Below 2G (MMIOB2G) entry24 target node**  A[30:26]==5’d24: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIOB2GTMVEQ24[3:0] |  | vcc | x | x | x |

### MMIO2T4G Decode (B8-CBh)

Offset Address: BB-B8h (D0F2)   
MMIO2T4G decoder Default Value:0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:3 | RO | NA | 0 | **Reserved** | RxB8[31:3] |  | vcc | x | x | x |
| 2:0 | RWL | RO | 0 | **MMIO 2 to 4G (MMIO2T4G) base address** MMIO2T4G base address, A[39:32] are fixed to 0, A[31] is fixed to 1, A[30:28] are programmable, A[27:0] are fixed to 0. MMIO2T4G Limit address is fixed to 4G-1, any address X hit MMIO2T4G range( MMIO2T4G\_base <= X <=MMIO2T4G\_Limit) is claimed by MMIO decoder. ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0. @((#control\_lock=lock\_port RSVAD\_LOCK)) )) ((For Internal Reference: The register is for SVAD.)) ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GBASE[30:28] |  | vcc | x | x | x |

Offset Address: BF-BCh (D0F2)   
MMIO2T4G decode Default Value:0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry7 target node**  A[30:26]==5’d7: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry6 target node**  A[30:26]==5’d6: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry5 target node**  A[30:26]==5’d5: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry4 target node**  A[30:26]==5’d4: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry3 target node**  A[30:26]==5’d3: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry2 target node**  A[30:26]==5’d2: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry1 target node**  A[30:26]==5’d1: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry0 target node**  A[30:26]==5’d0: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ0[3:0] |  | vcc | x | x | x |

Offset Address: C3-C0h (D0F2)   
MMIO2T4G decoder Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry15 target node**  A[30:26]==5’d15: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry14 target node**  A[30:26]==5’d14: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry13 target node**  A[30:26]==5’d13: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry12 target node**  A[30:26]==5’d12: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry11 target node**  A[30:26]==5’d11: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry10 target node**  A[30:26]==5’d10: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry9 target node**  A[30:26]==5’d9: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry8 target node**  A[30:26]==5’d8: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ8[3:0] |  | vcc | x | x | x |

Offset Address: C7-C4h (D0F2)   
MMIO2T4G decoder Default Value: 0000 0000h

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| Bit | Attribute | HW Property | Default | Description | Mnemonic | ChipRev | PwrDm | S | P | E |
| 31:28 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry23 target node  A[30:26]==5’d23: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ23[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry22 target node  A[30:26]==5’d22: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ22[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry21 target node  A[30:26]==5’d21: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ21[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry20 target node  A[30:26]==5’d20: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ20[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry19 target node  A[30:26]==5’d19: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ19[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry18 target node  A[30:26]==5’d18: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ18[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry17 target node  A[30:26]==5’d17: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ17[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | MMIO 2 To 4G (MMIO2T4G) entry16 target node  A[30:26]==5’d16: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ16[3:0] |  | vcc | x | x | x |

Offset Address: CB-C8h (D0F2)   
MMIO2T4G decoder Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry31 target node**  A[30:26]==5’d31: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ31[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry30 target node**  A[30:26]==5’d30: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ30[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry29 target node**  A[30:26]==5’d29: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ29[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry28 target node**  A[30:26]==5’d28: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ28[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry27 target node**  A[30:26]==5’d27: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ27[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry26 target node**  A[30:26]==5’d26: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ26[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry25 target node**  A[30:26]==5’d25: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ25[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MMIO 2 To 4G (MMIO2T4G) entry24 target node**  A[30:26]==5’d24: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_MMIO2T4GTMVEQ24[3:0] |  | vcc | x | x | x |

### ABSEG (CC-D3h)

Offset Address: CF-CCh (D0F2)   
ABSEG Default Value: 0000 0000h

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| Bit | Attribute | HW Property | Default | **Description** | Mnemonic | ChipRev | PwrDm | S | P | E |
| 31:8 | RO | NA | 0 | **Reserved** | RxC8[31:8] |  | vcc | R | x | x |
| 7 | RWL | NA | 0 | **C2M Tseg range Protection control**  When this bit set to 1 then C2M Tseg range protection is removed. This bit is valid only when RxCC[2,1] = [0,0], please reference table 1 for detail. Note: The DMA protection is always enabled, do not effect by this bit.  1: disable C2M Tseg range protection  0: enable C2M Tseg range protection  Please reference table 1  ((For Internal Reference: This bit is RW when D0F2 Rx90 [28] is set to 0.  @((#control\_lock = lock\_port RSVAD\_TSEGLOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_TSEGPRTDIS |  | vcc | x | x | x |
| 6:3 | RWL | RO | 0 | **A/B SEG(VGA memory) decode for target to MMIO  - for memory address range in A0000h to BFFFFh**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ABSEG\_MMIO\_TGT |  | vcc | x | x | x |
| 2:1 | RWL | RO | 0 | **A/B & T SEG access control to system memory or MMIO Reference table1**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ABSEG\_SEL |  | vcc | x | x | x |
| 0 | RO | NA | 0 | **Reserved** | RxBC[0] |  | vcc | R | x | x |

table1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| RxCC[2] | RxCC[1] | **RxCC[7]** | Cycle  Type | Code Read  Target | Data Access  Target |
| 0 | 0 | 0 | Normal | MMIO \*1 | MMIO \*1 |
| 0 | 0 | 0 | SMM | System Memory \*2 | System Memory \*2 |
| 0 | 0 | 1 | Normal | A/B Seg ->MMIO \*1  T Seg -> System Memory \*3 | A/B Seg ->MMIO \*1  T Seg -> System Memory \*3 |
| 0 | 0 | 1 | SMM | System Memory \*2 | System Memory \*2 |
| - | 1 | x | Normal/SMM | System Memory \*2 | System Memory \*2 |
| 1 | 0 | x | Normal | MMIO \*1 | MMIO \*1 |
| 1 | 0 | x | SMM | System Memory \*2 | MMIO \*1 |

Chipset base on the request from CPU is in normal/SMM mode and RxCC[2:1] to re-direct the cycle to MMIO or System memory.

Note 1: For target to MMIO and in A/B SEG range, chipset also reference RxCC[2:1] to re-direct the cycle to sub node. In Tseg range, chipset always forward the cycle to local sub node.

Note 2: For target to System Memory, chipset also reference SVAD entries to re-direct the cycle to master/slave socket.

Note 3: For target to System Memory in T seg range, it is used for CPU SMRR enable with WB cache mode only.

DMA protection:

Note 1: Chipset always protect A0000h~FFFFFh range. The DMA cycle issue by PCI or PCIE device target to this range then will be abored by Chipset: for write, discard the request and data; for read: give back all ‘1” data to device.

Note 2. When RTSMMEN = 1 then chipset protect the DMA cycle target to T SEG range.

-          T SEG range start from “RLOWTOPA – T SEG size(in SM\_SIZE[1:0])” to “RLOWTOPA – 1”

Note 3. When Memory Hole enable then chipset forward the cycle to PCI.

Note 4. When DPR enable, then chipset protect the DMA cycle target to DPR range.

Offset Address: D3-D0h (D0F2)   
C/D/E/F SEG Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **C/D/E/F SEG decode control when target to MMIO controlled by RxD0[25:0]**  The value is the target sub node number;  This register control all C/D/E/F segment**.**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) ))  Note: when target to system memory, chipset base on SVAD to select to target socket. | RSVAD\_CDEFSEG\_MMIO\_TGT |  | vcc | x | x | x |
| 27:26 | RO | NA | 0 | **Reserved** | RxCC[27:26] |  | vcc | x | x | x |
| 25:24 | RWL | RO | 0 | **F0000-FFFFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENFF[1:0] |  | vcc | x | x | x |
| 23:22 | RWL | RO | 0 | **E0000-E3FFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENE0[1:0] |  | vcc | x | x | x |
| 21:20 | RWL | RO | 0 | **E4000-E7FFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENE4[1:0] |  | vcc | x | x | x |
| 19:18 | RWL | RO | 0 | **E8000-EBFFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENE8[1:0] |  | vcc | x | x | x |
| 17:16 | RWL | RO | 0 | **EC000-EFFFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENEC[1:0] |  | vcc | x | x | x |
| 15:14 | RWL | RO | 0 | **D0000-D3FFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SEND0[1:0] |  | vcc | x | x | x |
| 13:12 | RWL | RO | 0 | **D4000-D7FFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SEND4[1:0] |  | vcc | x | x | x |
| 11:10 | RWL | RO | 0 | **D8000-DBFFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SEND8[1:0] |  | vcc | x | x | x |
| 9:8 | RWL | RO | 0 | **DC000-DFFFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENDC[1:0] |  | vcc | x | x | x |
| 7:6 | RWL | RO | 0 | **C0000-C3FFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENC0[1:0] |  | vcc | x | x | x |
| 5:4 | RWL | RO | 0 | **C4000-C7FFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENC4[1:0] |  | vcc | x | x | x |
| 3:2 | RWL | RO | 0 | **C8000-CBFFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENC8[1:0] |  | vcc | x | x | x |
| 1:0 | RWL | RO | 0 | **CC000-CFFFFh Memory Space Access Control**  00b: Read / Write disable;  01b: Write enable;  10b: Read enable;  11b: Read / Write enable  ((For Internal Reference: This bit is RW when D0F2 Rx90 [1] is set to 0.  @((#control\_lock = lock\_port RSVAD\_CDEFSEGLOCK)) )) | SENCC[1:0] |  | vcc | x | x | x |

### MMIO VGA IO and Legacy IO Decode (D4-10Fh)

Offset Address: D7-D4h (D0F2)   
MMIO and VGA IO decoder Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:30 | RWL | RO | 0 | **Memory Hole**  00: None  01: 512K ~ 640K  10: 15M ~ 16M (1M)  11: 14M ~ 16M (2M)  Limitation: always forward to master socket MMIO space(PCI) when hit memory hole range.  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RHOLE[1:0] |  | vcc | x | x | x |
| 29 | RWL | RO | 0 | **Top SM Memory Enable**  This bit is the enable bit for the SM Memory at the top of the memory below 4G to be activated. When this bit is enabled, the memory with size defined by bits [1:0] will be deducted from the top of the system memory and be used for SM mode. Top SM Memory range : B4GMemLimit(RLOWTOPA)+1 - SM\_SIZE <= X <= B4GMemLimit 0: Disabled.1: Enabled.  ((For Internal Reference: This bit is RW when D0F2 Rx90 [28] is set to 0.  @((#control\_lock = lock\_port RSVAD\_TSEGLOCK)) )) | RTSMMEN |  | vcc | x | x | x |
| 28:27 | RWL | RO | 0 | **Top SM Memory Size** For SM mode, these two bits defined the size of the memory at the top of the memory below 4G. They are activated only when bit-2 is 1.  00: 4M.  01: 8M. 10: 16M.  11: 32M.  ((For Internal Reference: This bit is RW when D0F2 Rx90 [28] is set to 0.  @((#control\_lock = lock\_port RSVAD\_TSEGLOCK)) )) | SM\_SIZE[1:0] |  | vcc | x | x | x |
| 26:5 | RO | NA | 0 | **Reserved** | RxD0[26:5] |  | vcc | R | x | x |
| 4:1 | RWL | RO | 0 | **Legacy VGA IO target select – in IO range 3B0h-3BBh, 3C0h-3DFh**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_VGA\_TGT[3:0] |  | vcc | x | x | x |
| 0 | RO | NA | 0 | **Reserved** | RxD0[0] |  | vcc | R | x | x |

Offset Address: DB-D8h (D0F2)   
legacy IO decoder Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **Legacy IO entry7 target node**  A[15:11]==5’d7: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **Legacy IO entry6 target node**  A[15:11]==5’d6: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **Legacy IO entry5 target node**  A[15:11]==5’d5: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **Legacy IO entry4 target node**  A[15:11]==5’d4: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **Legacy IO entry3 target node**  A[15:11]==5’d3: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **Legacy IO entry2 target node**  A[15:11]==5’d2: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **Legacy IO entry1 target node**  A[15:11]==5’d1: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **Legacy IO entry0 target node**  A[15:11]==5’d0: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT0[3:0] |  | vcc | x | x | x |

Offset Address: DF-DCh (D0F2)   
legacy IO decoder Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **Legacy IO entry15 target node**  A[15:11]==5’d7: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **Legacy IO entry14 target node**  A[15:11]==5’d14: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **Legacy IO entry13 target node**  A[15:11]==5’d13: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **Legacy IO entry12 target node**  A[15:11]==5’d12: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **Legacy IO entry11 target node**  A[15:11]==5’d11: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **Legacy IO entry10 target node**  A[15:11]==5’d10: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **Legacy IO entry9 target node**  A[15:11]==5’d9: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **Legacy IO entry8 target node**  A[15:11]==5’d8: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT8[3:0] |  | vcc | x | x | x |

Offset Address: E3-E0h (D0F2)   
legacy IO decoder Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **Legacy IO entry23 target node**  A[15:11]==5’d23: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT23[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **Legacy IO entry22 target node**  A[15:11]==5’d22: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT22[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **Legacy IO entry21 target node**  A[15:11]==5’d21: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT21[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **Legacy IO entry20 target node**  A[15:11]==5’d20: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT20[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **Legacy IO entry19 target node**  A[15:11]==5’d19: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT19[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **Legacy IO entry18 target node**  A[15:11]==5’d18: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT18[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **Legacy IO entry17 target node**  A[15:11]==5’d17: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT17[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **Legacy IO entry16 target node**  A[15:11]==5’d16: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT16[3:0] |  | vcc | x | x | x |

Offset Address: E7-E4h (D0F2)   
legacy IO decoder Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **Legacy IO entry31 target node**  A[15:11]==5’d31: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT31[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **Legacy IO entry30 target node**  A[15:11]==5’d30: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT30[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **Legacy IO entry29 target node**  A[15:11]==5’d29: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT29[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **Legacy IO entry28 target node**  A[15:11]==5’d28: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT28[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **Legacy IO entry27 target node**  A[15:11]==5’d27: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT27[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **Legacy IO entry26 target node**  A[15:11]==5’d26: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT26[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **Legacy IO entry25 target node**  A[15:11]==5’d25: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT25[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **Legacy IO entry24 target node**  A[15:11]==5’d24: the request is routed to the node indicated by this register value  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_IO\_TGT\_SEL\_ENT24[3:0] |  | vcc | x | x | x |

Offset Address: E9-E8h (D0F2)   
Multi-die link ready Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:1 | RO | NA | 0 | **Reserved** | RxE8[15:1] |  | vcc | R | x | x |
| 0 | RWL | RO | 0 | **This bit indicate all ZPI/OPI link of the platform initial done.**  1 means ZPI/OPI link ready  0 means ZPI/OPI not ready  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) )) | MULTI\_DIE\_ALL\_LINK\_READY |  | vcc | x | x | x |

Offset Address: EA-10Fh (D0F2) – Reserved

### MEM ENTRY (110-34Fh)

Offset Address: 113-110h (D0F2)   
MEM\_ENT0 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry0 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry0 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry0 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry0 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry0 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry0 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry0 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry0 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 117-114h (D0F2)   
MEM\_ENT0 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry0 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry0 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry0 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry0 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry0 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry0 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry0 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry0 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 11B-118h (D0F2)   
MEM\_ENT0 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry0 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry0 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry0 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME0ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx118[11:0] |  | vcc | x | x | x |

Note1: The SVAD entry 0 base address = 0, SVAD entry 0 Limit address must not 0.

Note 2: For SVAD entry 1 to 47,  the SVAD entry N base address =  SVAD entry N-1 Limit address +1;  This SVAD entry is invalid if SVAD entry N Limit address = SVAD entry N-1 Limit address.

programming rule: Software should update Limit address from entry 47 to 0 to avoid some corner case cause decode fail.

Offset Address: 11F-11Ch (D0F2)   
MEM\_ENT1 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry1 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry1 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry1 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry1 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry1 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry1 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry1 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry1 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 123-120h (D0F2)   
MEM\_ENT1 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry1 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry1 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry1 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry1 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry1 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry1 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry1 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry1 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 127-124h (D0F2)   
MEM\_ENT1 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry1 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry1 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry1 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME1ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx124[10:0] |  | vcc | x | x | x |

Offset Address: 12B-128h (D0F2)   
MEM\_ENT2 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry2 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry2 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry2 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry2 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry2 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry2 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry2 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry2 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:12F-12Ch (D0F2)   
MEM\_ENT2 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry2 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry2 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry2 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry2 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry2 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry2 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry2 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry2 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:133-130h (D0F2)   
MEM\_ENT2 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry2 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry2 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry2 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME2ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx130[10:0] |  | vcc | x | x | x |

Offset Address: 137-134h (D0F2)   
MEM\_ENT3 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry3 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry3 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry3 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry3 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry3 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry3 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry3 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry3 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 13B-138h (D0F2)   
MEM\_ENT3 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry3 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry3 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry3 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry3 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry3 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry3 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry3 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry3 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 13F-13Ch (D0F2)   
MEM\_ENT3 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry3 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry3 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry3 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME3ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx13C[11:0] |  | vcc | x | x | x |

Offset Address: 143-140h (D0F2)   
MEM\_ENT4 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry4 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry4 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry4 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry4 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry4 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry4 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry4 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry4 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 147-144h (D0F2)   
MEM\_ENT4 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry4 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry4 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry4 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry4 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry4 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry4 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry4 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry4 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 14B-148h (D0F2)   
MEM\_ENT4 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry4 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry4 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry4 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME4ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx148[10:0] |  | vcc | x | x | x |

Offset Address: 14F-14Ch (D0F2)   
MEM\_ENT5 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry5 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry5 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry5 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry5 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry5 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry5 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry5 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry5 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:153-150h (D0F2)   
MEM\_ENT5 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry5 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry5 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry5 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry5 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry5 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry5 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry5 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry5 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:157-154h (D0F2)   
MEM\_ENT5 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry5 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry5 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry5 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME5ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx154[10:0] |  | vcc | x | x | x |

Offset Address: 15B-158h (D0F2)   
MEM\_ENT6 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry6 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry6 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry6 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry6 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry6 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry6 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry6 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry6 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 15F-15Ch (D0F2)   
MEM\_ENT6 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry6 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry6 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry6 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry6 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry6 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry6 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry6 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry6 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 163-160h (D0F2)   
MEM\_ENT6 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry6 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry6 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry6 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME6ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx160[11:0] |  | vcc | x | x | x |

Offset Address: 167-164h (D0F2)   
MEM\_ENT7 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry7 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry7 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry7 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry7 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry7 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry7 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry7 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry7 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 16B-168h (D0F2)   
MEM\_ENT7 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry7 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry7 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry7 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry7 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry7 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry7 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry7 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry7 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 16F-16Ch (D0F2)   
MEM\_ENT7 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry7 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry7 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry7 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME7ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx16C[10:0] |  | vcc | x | x | x |

Offset Address: 173-170h (D0F2)   
MEM\_ENT8 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry8 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry8 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry8 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry8 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry8 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry8 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry8 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry8 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:177-174h (D0F2)   
MEM\_ENT8 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry8 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry8 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry8 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry8 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry8 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry8 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry8 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry8 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:17B-178h (D0F2)   
MEM\_ENT8 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry8 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry8 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry8 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME8ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx178[10:0] |  | vcc | x | x | x |

Offset Address: 17F-17Ch (D0F2)   
MEM\_ENT9 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry9 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry9 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry9 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry9 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry9 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry9 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry9 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry9 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 183-180h (D0F2)   
MEM\_ENT9 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry9 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry9 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry9 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry9 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry9 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry9 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry9 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry9 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 187-184h (D0F2)   
MEM\_ENT9 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry9 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry9 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry9 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME9ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx184[11:0] |  | vcc | x | x | x |

Offset Address: 18B-188h (D0F2)   
MEM\_ENT10 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry10 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry10 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry10 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry10 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry10 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry10 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry10 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry10 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 18F-18Ch (D0F2)   
MEM\_ENT10 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry10 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry10 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry10 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry10 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry10 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry10 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry10 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry10 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 193-190h (D0F2)   
MEM\_ENT10 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry10 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry10 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry10 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME10ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx190[10:0] |  | vcc | x | x | x |

Offset Address: 197-194h (D0F2)   
MEM\_ENT11 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry11 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry11 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry11 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry11 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry11 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry11 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry11 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry11 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:19B-198h (D0F2)   
MEM\_ENT11 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry11 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry11 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry11 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry11 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry11 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry11 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry11 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry11 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:19F-19Ch (D0F2)   
MEM\_ENT11 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry11 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry11 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry11 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME11ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx19C[10:0] |  | vcc | x | x | x |

Offset Address: 1A3-1A0h (D0F2)   
MEM\_ENT12 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry12 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry12 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry12 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry12 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry12 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry12 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry12 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry12 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 1A7-1A4h (D0F2)   
MEM\_ENT12 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry12 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry12 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry12 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry12 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry12 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry12 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry12 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry12 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 1AB-1A8h (D0F2)   
MEM\_ENT12 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry12 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry12 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry12 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME12ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1A8[11:0] |  | vcc | x | x | x |

Offset Address: 1AF-1ACh (D0F2)   
MEM\_ENT13 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry13 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry13 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry13 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry13 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry13 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry13 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry13 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry13 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 1B3-1B0h (D0F2)   
MEM\_ENT13 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry13 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry13 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry13 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry13 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry13 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry13 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry13 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry13 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13TARGET\_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 1B7-1B4h (D0F2)   
MEM\_ENT13 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry13 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry13 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry13 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME13ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1B4[10:0] |  | vcc | x | x | x |

Offset Address: 1BB-1B8h (D0F2)   
MEM\_ENT14 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry14 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry14 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry14 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry14 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry14 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry14 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry14 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry14 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:1BF-1BCh (D0F2)   
MEM\_ENT14 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry14 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry14 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry14 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry14 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry14 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry14 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry14 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry14 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:1C3-1C0h (D0F2)   
MEM\_ENT14 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry14 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry14 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry14 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME14ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1C0[10:0] |  | vcc | x | x | x |

Offset Address: 1C7-1C4h (D0F2)   
MEM\_ENT15 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry15 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry15 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry15 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry15 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry15 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry15 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry15 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry15 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 1CB-1C8h (D0F2)   
MEM\_ENT15 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry15 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry15 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry15 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry15 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry15 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry15 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry15 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry15 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 1CF-1CCh (D0F2)   
MEM\_ENT15 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry15 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry15 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry15 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME15ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1CC[11:0] |  | vcc | x | x | x |

Offset Address: 1D3-1D0h (D0F2)   
MEM\_ENT16 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry16 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry16 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry16 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry16 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry16 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry16 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry16 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry16 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 1D7-1D4h (D0F2)   
MEM\_ENT16 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry16 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry16 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry16 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry16 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry16 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry16 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry16 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry16 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 1DB-1D8h (D0F2)   
MEM\_ENT16 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry16 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry16 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry16 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME16ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1D8[10:0] |  | vcc | x | x | x |

Offset Address: 1DF-1DCh (D0F2)   
MEM\_ENT17 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry17 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry17 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry17 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry17 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry17 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry17 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry17 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry17 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:1E3-1E0h (D0F2)   
MEM\_ENT17 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry17 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry17 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry17 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry17 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry17 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry17 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry17 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry17 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:1E7-1E4h (D0F2)   
MEM\_ENT17 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry17 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry17 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry17 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME17ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1E4[10:0] |  | vcc | x | x | x |

Offset Address: 1EB-1E8h (D0F2)   
MEM\_ENT18 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry18 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry18 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry18 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry18 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry18 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry18 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry18 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry18 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 1EF-1ECh (D0F2)   
MEM\_ENT18 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry18 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry18 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry18 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry18 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry18 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry18 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry18 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry18 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 1F3-1F0h (D0F2)   
MEM\_ENT18 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry18 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry18 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry18 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME18ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1F0[11:0] |  | vcc | x | x | x |

Offset Address: 1F7-1F4h (D0F2)   
MEM\_ENT19 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry19 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry19 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry19 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry19 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry19 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry19 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry19 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry19 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 1FB-1F8h (D0F2)   
MEM\_ENT19 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry19 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry19 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry19 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry19 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry19 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry19 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry19 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry19 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 1FF-1FCh (D0F2)   
MEM\_ENT19 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry19 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry19 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry19 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME19ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx1FC[10:0] |  | vcc | x | x | x |

Offset Address: 203-200h (D0F2)   
MEM\_ENT20 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry20 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry20 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry20 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry20 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry20 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry20 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry20 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry20 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:207-204h (D0F2)   
MEM\_ENT20 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry20 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry20 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry20 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry20 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry20 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry20 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry20 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry20 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:20B-208h (D0F2)   
MEM\_ENT20 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry20 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry20 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry20 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME20ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx208[10:0] |  | vcc | x | x | x |

Offset Address: 20F-20Ch (D0F2)   
MEM\_ENT21 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry21 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry21 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry21 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry21 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry21 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry21 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry21 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry21 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 213-210h (D0F2)   
MEM\_ENT21 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry21 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry21 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry21 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry21 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry21 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry21 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry21 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry21 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 217-214h (D0F2)   
MEM\_ENT21 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry21 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry21 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry21 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME21ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx214[11:0] |  | vcc | x | x | x |

Offset Address: 21B-218h (D0F2)   
MEM\_ENT22 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry22 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry22 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry22 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry22 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry22 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry22 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry22 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry22 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 21F-21Ch (D0F2)   
MEM\_ENT22 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry22 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry22 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry22 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry22 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry22 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry22 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry22 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry22 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 223-220h (D0F2)   
MEM\_ENT22 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry22 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry22 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry22 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME22ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx220[10:0] |  | vcc | x | x | x |

Offset Address: 227-224h (D0F2)   
MEM\_ENT23 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry23 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry23 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry23 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry23 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry23 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry23 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry23 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry23 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:22B-228h (D0F2)   
MEM\_ENT23 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry23 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry23 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry23 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry23 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry23 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry23 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry23 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry23 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:22F-22Ch (D0F2)   
MEM\_ENT23 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry23 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry23 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry23 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME23ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx22C[10:0] |  | vcc | x | x | x |

Offset Address: 233-230h (D0F2)   
MEM\_ENT24 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry24 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry24 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry24 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry24 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry24 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry24 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry24 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry24 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 237-234h (D0F2)   
MEM\_ENT24 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry24 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry24 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry24 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry24 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry24 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry24 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry24 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry24 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 23B-238h (D0F2)   
MEM\_ENT24 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry24 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry24 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry24 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME24ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx238[11:0] |  | vcc | x | x | x |

Offset Address: 23F-23Ch (D0F2)   
MEM\_ENT25 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry1 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry1 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry1 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry1 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry1 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry1 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry1 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry1 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 243-240h (D0F2)   
MEM\_ENT25 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry1 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry1 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry1 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry1 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry1 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry1 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry1 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry1 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 247-244h (D0F2)   
MEM\_ENT25 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry1 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry1 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry1 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME25ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx244[10:0] |  | vcc | x | x | x |

Offset Address: 24B-248h (D0F2)   
MEM\_ENT26 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry2 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry2 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry2 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry2 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry2 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry2 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry2 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry2 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:24F-24Ch (D0F2)   
MEM\_ENT26 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry2 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry2 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry2 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry2 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry2 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry2 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry2 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry2 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:253-250h (D0F2)   
MEM\_ENT26 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry2 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry2 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry2 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME26ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx250[10:0] |  | vcc | x | x | x |

Offset Address: 257-254h (D0F2)   
MEM\_ENT27 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry27 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry27 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry27 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry27 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry27 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry27 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry27 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry27 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 25B-258h (D0F2)   
MEM\_ENT27 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry27 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry27 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry27 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry27 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry27 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry27 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry27 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry27 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 25F-25Ch (D0F2)   
MEM\_ENT27 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry27 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry27 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry27 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME27ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx25C[11:0] |  | vcc | x | x | x |

Offset Address: 263-260h (D0F2)   
MEM\_ENT28 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry28 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry28 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry28 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry28 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry28 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry28 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry28 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry28 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 267-264h (D0F2)   
MEM\_ENT28 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry28 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry28 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry28 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry28 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry28 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry28 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry28 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry28 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 26B-268h (D0F2)   
MEM\_ENT28 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry28 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry28 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry28 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME28ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx268[10:0] |  | vcc | x | x | x |

Offset Address: 26F-26Ch (D0F2)   
MEM\_ENT29 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry29 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry29 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry29 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry29 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry29 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry29 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry29 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry29 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:273-270h (D0F2)   
MEM\_ENT29 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry29 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry29 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry29 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry29 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry29 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry29 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry29 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry29 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:277-274h (D0F2)   
MEM\_ENT29 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry29 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry29 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry29 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME29ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx274[10:0] |  | vcc | x | x | x |

Offset Address: 27B-278h (D0F2)   
MEM\_ENT30 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry30 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry30 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry30 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry30 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry30 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry30 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry30 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry30 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 27F-27Ch (D0F2)   
MEM\_ENT30 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry30 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry30 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry30 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry30 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry30 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry30 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry30 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry30 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 283-280h (D0F2)   
MEM\_ENT30 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry30 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry30 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry30 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME30ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx280[11:0] |  | vcc | x | x | x |

Offset Address: 287-284h (D0F2)   
MEM\_ENT31 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry31 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry31 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry31 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry31 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry31 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry31 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry31 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry31 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 28B-288h (D0F2)   
MEM\_ENT31 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry31 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry31 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry31 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry31 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry31 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry31 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry31 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry31 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 28F-28Ch (D0F2)   
MEM\_ENT31 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry31 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry31 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry31 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME31ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx28C[10:0] |  | vcc | x | x | x |

Offset Address: 293-290h (D0F2)   
MEM\_ENT32 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry32 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry32 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry32 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry32 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry32 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry32 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry32 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry32 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:297-294h (D0F2)   
MEM\_ENT32 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry32 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry32 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry32 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry32 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry32 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry32 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry32 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry32 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:29B-298h (D0F2)   
MEM\_ENT32 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry32 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry32 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry32 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME32ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx298[10:0] |  | vcc | x | x | x |

Offset Address: 29F-29Ch (D0F2)   
MEM\_ENT33 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry33 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry33 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry33 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry33 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry33 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry33 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry33 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry33 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 2A3-2A0h (D0F2)   
MEM\_ENT33 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry33 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry33 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry33 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry33 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry33 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry33 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry33 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry33 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 2A7-2A4h (D0F2)   
MEM\_ENT33 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry33 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry33 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry33 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME33ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx2A4[11:0] |  | vcc | x | x | x |

Offset Address: 2AB-2A8h (D0F2)   
MEM\_ENT34 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry34 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry34 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry34 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry34 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry34 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry34 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry34 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry34 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 2AF-2ACh (D0F2)   
MEM\_ENT34 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry34 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry34 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry34 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry34 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry34 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry34 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry34 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry34 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 2B3-2B0h (D0F2)   
MEM\_ENT34 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry34 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry34 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry34 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME34ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx2B0[10:0] |  | vcc | x | x | x |

Offset Address: 2B7-2B4h (D0F2)   
MEM\_ENT35 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry35 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry35 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry35 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry35 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry35 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry35 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry35 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry35 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:2BB-2B8h (D0F2)   
MEM\_ENT35 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry35 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry35 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry35 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry35 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry35 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry35 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry35 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry35 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:2BF-2BCh (D0F2)   
MEM\_ENT35 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry35 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry35 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry35 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME35ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx2BC[10:0] |  | vcc | x | x | x |

Offset Address: 2C3-2C0h (D0F2)   
MEM\_ENT36 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry36 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry36 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry36 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry36 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry36 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry36 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry36 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry36 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 2C7-2C4h (D0F2)   
MEM\_ENT36 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry36 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry36 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry36 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry36 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry36 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry36 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry36 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry36 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 2CB-2C8h (D0F2)   
MEM\_ENT36 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry36 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry36 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry36 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME36ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx2C8[11:0] |  | vcc | x | x | x |

Offset Address: 2CF-2CCh (D0F2)   
MEM\_ENT37 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry37 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry37 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry37 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry37 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry37 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry37 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry37 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry37 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 2D3-2D0h (D0F2)   
MEM\_ENT37 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry37 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry37 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry37 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry37 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry37 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry37 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry37 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry37 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37TARGET\_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 2D7-2D4h (D0F2)   
MEM\_ENT37 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry37 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry37 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry37 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME37ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx2D4[10:0] |  | vcc | x | x | x |

Offset Address: 2DB-2D8h (D0F2)   
MEM\_ENT38 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry38 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry38 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry38 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry38 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry38 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry38 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry38 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry38 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:2DF-2DCh (D0F2)   
MEM\_ENT38 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry38 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry38 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry38 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry38 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry38 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry38 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry38 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry38 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:2E3-2E0h (D0F2)   
MEM\_ENT38 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry38 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry38 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry38 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME38ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx2E0[10:0] |  | vcc | x | x | x |

Offset Address: 2E7-2E4h (D0F2)   
MEM\_ENT39 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry39 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry39 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry39 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry39 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry39 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry39 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry39 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry39 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 2EB-2E8h (D0F2)   
MEM\_ENT39 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry39 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry39 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry39 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry39 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry39 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry39 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry39 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry39 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 2EF-2ECh (D0F2)   
MEM\_ENT39 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry39 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry39 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry39 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME39ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx2EC[11:0] |  | vcc | x | x | x |

Offset Address: 2F3-2F0h (D0F2)   
MEM\_ENT40 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry40 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry40 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry40 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry40 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry40 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry40 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry40 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry40 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 2F7-2F4h (D0F2)   
MEM\_ENT40 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry40 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry40 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry40 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry40 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry40 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry40 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry40 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry40 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 2FB-2F8h (D0F2)   
MEM\_ENT40 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry40 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry40 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry40 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME40ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx12F8[10:0] |  | vcc | x | x | x |

Offset Address: 2FF-2FCh (D0F2)   
MEM\_ENT41 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry41 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry41 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry41 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry41 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry41 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry41 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry41 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry41 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:303-300h (D0F2)   
MEM\_ENT41 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry41 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry41 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry41 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry41 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry41 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry41 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry41 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry41 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:307-304h (D0F2)   
MEM\_ENT41 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry41 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry41 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry41 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME41ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx304[10:0] |  | vcc | x | x | x |

Offset Address: 30B-308h (D0F2)   
MEM\_ENT42 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry42 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry42 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry42 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry42 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry42 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry42 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry42 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry42 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 30F-30Ch (D0F2)   
MEM\_ENT42 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry42 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry42 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry42 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry42 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry42 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry42 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry42 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry42 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 313-310h (D0F2)   
MEM\_ENT42 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry42 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry42 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry42 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME42ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx310[11:0] |  | vcc | x | x | x |

Offset Address: 317-314h (D0F2)   
MEM\_ENT43 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry43 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry43 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry43 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry43 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry43 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry43 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry43 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry43 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 31B-318h (D0F2)   
MEM\_ENT43 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry43 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry43 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry43 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry43 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry43 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry43 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry43 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry43 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 31F-31Ch (D0F2)   
MEM\_ENT43 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry43 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry43 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry43 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME43ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx31C[10:0] |  | vcc | x | x | x |

Offset Address: 323-320h (D0F2)   
MEM\_ENT44 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry44 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry44 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry44 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry44 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry44 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry44 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry44 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry44 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:327-324h (D0F2)   
MEM\_ENT44 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry44 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry44 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry44 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry44 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry44 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry44 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry44 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry44 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:32B-328h (D0F2)   
MEM\_ENT44 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry44 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry44 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry44 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME44ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx328[10:0] |  | vcc | x | x | x |

Offset Address: 32F-32Ch (D0F2)   
MEM\_ENT45 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry45 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry45 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry45 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry45 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry45 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry45 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry45 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry45 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 333-330h (D0F2)   
MEM\_ENT45 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry45 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry45 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry45 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry45 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry45 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry45 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry45 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry45 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 337-334h (D0F2)   
MEM\_ENT45 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry45 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry45 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry45 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME45ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx334[11:0] |  | vcc | x | x | x |

Offset Address: 33B-338h (D0F2)   
MEM\_ENT46 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry46 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry46 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry46 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry46 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry46 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET \_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry46 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry46 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry46 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address: 33F-33ch (D0F2)   
MEM\_ENT46 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry46 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry46 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry46 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry46 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry46 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry46 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry46 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry46 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address: 343-340h (D0F2)   
MEM\_ENT46 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry46 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry46 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry46 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME46ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx340[10:0] |  | vcc | x | x | x |

Offset Address: 347-344h (D0F2)   
MEM\_ENT47 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry47 TARGET LIST7 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST7[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry47 TARGET LIST6 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST6[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry47 TARGET LIST5 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST5[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry47 TARGET LIST4 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST4[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry47 TARGET LIST3 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST3[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry47 TARGET LIST2 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST2[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry47 TARGET LIST1 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST1[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry47 TARGET LIST0 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST0[3:0] |  | vcc | x | x | x |

Offset Address:34B-348h (D0F2)   
MEM\_ENT47 Default Value: 0000 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:28 | RWL | RO | 0 | **MEM entry47 TARGET LIST15 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST15[3:0] |  | vcc | x | x | x |
| 27:24 | RWL | RO | 0 | **MEM entry47 TARGET LIST14 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST14[3:0] |  | vcc | x | x | x |
| 23:20 | RWL | RO | 0 | **MEM entry47 TARGET LIST13 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST13[3:0] |  | vcc | x | x | x |
| 19:16 | RWL | RO | 0 | **MEM entry47 TARGET LIST12 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST12[3:0] |  | vcc | x | x | x |
| 15:12 | RWL | RO | 0 | **MEM entry47 TARGET LIST11 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST11[3:0] |  | vcc | x | x | x |
| 11:8 | RWL | RO | 0 | **MEM entry47 TARGET LIST10 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST10[3:0] |  | vcc | x | x | x |
| 7:4 | RWL | RO | 0 | **MEM entry47 TARGET LIST9 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET\_LIST9[3:0] |  | vcc | x | x | x |
| 3:0 | RWL | RO | 0 | **MEM entry47 TARGET LIST8 for target decode**  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47TARGET \_LIST8[3:0] |  | vcc | x | x | x |

Offset Address:34F-34Ch (D0F2)   
MEM\_ENT47 Default Value: 7FFF E000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31 | RWL | RO | 0 | **MEM entry47 attr**  Indicate the region's memory attribute.  1'b0: Memory;  1'b1: MMIO;  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47ATTR |  | vcc | x | x | x |
| 30:13 | RWL | RO | 3FFFFh | **MEM entry47 limit addr**  Memory decoder entry address limit, unit of 256M bytes.  0: means address limit = 256M -1 bytes  1: means address limit =  (1+1)x256M – 1 bytes  N: means  address limit = (N+1)x256M – 1 bytes  For an address X, When Base address <= X <= limit address then hit this entry  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47LADDR[45:28] |  | vcc | x | x | x |
| 12:11 | RWL | RO | 0 | **MEM entry47 interleave addr bit sel**  2’b00: A[9:6] 2’b01:A[10:7] 2’b10:A[11:8]  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) ))  ((For Internal Reference: The register is for SVAD.))  ((For Internal Reference: @((#USER=HIF)) )) | RSVAD\_ME47ADDR\_SEL\_11\_9 |  | vcc | x | x | x |
| 10:0 | RO | NA | 0 | **Reserved** | Rx34C[10:0] |  | vcc | x | x | x |

### RTopA and LowTopA (350-3FFh)

Offset Address: 353-350h (D0F2)   
Highest SVAD limit target to memory (DRAM limit address over 4G) Default Value: FFFF FFC0h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 31:6 | RWL | RO | 3FFFFFFh | **TOP of System memory address over 4G**  these bits defined the TOP address space over 4G that the system can use as the system memory.  The address X of “4G<=X<RTOPA” is the DRAM address.  BIOS should set RTOPA = 1000h if no system memory above 4G address  This register is used for traffic controller to decode target of the upstream cycle to memory or MMIO(PCI) for P2P  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) )) | RTOPA[45:20] |  | vcc | x | x | x |
| 5:0 | RO | NA | 0 | **Reserved** | Rx318[3:0] |  | vcc | x | x | x |

Offset Address: 355-354h (D0F2)   
Below 4G highest memory limit(DRAM limit address below 4G) Default Value: FF00h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:4 | RWL | RO | FF0h | **TOP of System memory address below 4G**  these bits defined the TOP address space below 4G that the system can use as the system memory.  Note: BIOS MUST set Below 4G MMIO Base address  = RLOWTOPA = min value of {MMIOB2G, MMIO2T4G}  The address X of “X < RLOWTOPA”is the DRAM address.  HW use the RLOWTOPA to decode the P2C cycle target to DRAM or MMIO.  ((For Internal Reference: This bit is RW when D0F2 Rx90 [30] is set to 0.  @((#control\_lock = lock\_port RSVAD\_LOCK)) )) | RLOWTOPA[31:20] |  | vcc | x | x | x |
| 3:0 | RO | NA | 0 | **Reserved** | Rx354[3:0] |  | vcc | x | x | x |

Offset Address: 356-3FFh (D0F2) – Reserved

### TPR Control (400-40Fh)

Offset Address: 400-40Bh (D0F2) – Reserved

Offset Address: 40D-40Ch (D0F2)   
Reserved Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:0 | RO | NA | 0 | **Reserved** | Rxcc[15:0] |  | vcc | x | x | x |

Offset Address: 40F-40Eh (D0F2)  
TPR Control Default Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:5 | RO | NA | 0 | **Reserved** | Rxce[15:5] |  | vcc | x | x | x |
| 4 | RW | RO | 0 | **APIC Round-Robin Mode Select**  When enable the round-robin mechanism (RAPICROEN=1), There are two modes to control round-robin method  0: Round-Robin base on each core’s TPR value and select target core  1: Treat all cores as same TPR value and round-robin to select target core, in this case, ignore all TPR value configured from TPR cycle.  ((For Internal Reference: @((#TOGGLE=1))  )) | RAPICROMODESEL |  | vcc | 0 | x | x |
| 3 | RW | NA | 0 | **Reserved**  ((For Internal Reference:  APIC Cluster Model Select There are two ways to decide HIF is in APIC Cluster Model (Note 1) or not.  One is auto mode, in this way, HIF will decide whether or not it is in Cluster model according to APIC\_CM\_EN (Note 2) which is set by CPU’s TPR cycle; the other way is SW control mode, in this way, HIF will decide whether or not it is in Cluster mode according to Register RAPICCMSWEN.  0: Auto mode  1: Software control mode  Notes:  1. In logical destination mode, CPU support flat model and Cluster model. Controlled by Destination Format Register in local apic. in Flat model, CPU bit match with Destination field of MSI with Logical APIC ID field in Logical Destination Register of local APIC. The Flat model  support up to 8 cores. In Cluster model, the bit [7:4] in Logical APIC ID field is Cluster ID and bit [3:0]  in Logical APIC ID field bit match for target cpu cores in this cluster. It support Cluster ID from 0h to Eh, total 15 Cluster ID and support 4 cores in each Cluster ID. Total support 15x4 = 60 cores in Cluster model.  2. When CPU in Cluster model, it will issue TPR cycle with APIC\_CM\_EN=1.  3. When Cluster ID = Fh, Means broadcast Cluster ID, all CPU treat it as Cluster ID hit.  )) | RAPICCMS |  | vcc | 0 | x | x |
| 2 | RW | NA | 0 | **Reserved**  ((For Internal Reference:  APIC Round-Robin Mechanism Enable  When enable the round-robin mechanism, if there are two cores which have the same priority, HIF will not always choose the core which core number is little, but choose the two cores in turn.  0: Disable 1: Enable  ))  ((For Internal Reference: @((#TOGGLE=1)) )) | RAPICROEN |  | vcc | 0 | x | x |
| 1 | RW | NA | 0 | **Reserved**  ((For Internal Reference:  APIC Cluster Model Software Enable  0: Disable APIC Cluster Model  1: Enable APIC Cluster Model  )) | RAPICCMSWEN |  | vcc | 0 | x | x |
| 0 | RW | NA | 0 | **Reserved**  ((For Internal Reference:  Redirect Lowest Priority MSI Requests to CPU Core0  For supporting the FSB interrupt delivery, this chip is able to redirect the coming in MSI cycle to the CPU with least task priority. This register is used to redirect the Lowest Priority MSI Request cycle to the CPU core0 (CPU0 is treated as the lowest priority processor).  0: Disable. The Lowest Priority MSI Request will be redirected to lowest priority CPU core according to TPR Table record.  1: Enable. The Lowest Priority MSI Request will be always redirected to CPU core0.  )) | RAPIC0 |  | vcc | 0 | 0 | x |

Interrupt Message Address Format

|  |  |
| --- | --- |
| Bit | Description |
| 31:20 | always be 0xFEE |
| 19:12 | Destination ID |
| 11:4 | will always be 0 |
| 3 | Redirection Hint |
| 2 | Destination Mode |
| 1:0 | always be 00 |

Interrupt Message Data Format

|  |  |
| --- | --- |
| Bit | Description |
| 31:16 | always be 0000h |
| 15 | Trigger Mode |
| 14 | Delivery Status |
| 13:12 | always be 00 |
| 11 | always be 0 |
| 10:8 | Delivery mode |
| 7:0 | Vector |

### DMA Protection Control (410-41Fh)

Offset Address: 411-410h (D0F2)   
DMA Protection ControlDefault Value: 0000h

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| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | ChipRev | **PwrDm** | **S** | **P** | **E** |
| 15:12 | RW | RO | 0 | **Reserved** | Rx410[15:12] |  | vcc | 0 | x | x |
| 11:4 | RWL | RO | 0 | **This is the Size of DPR Region in MB**  It can be locked by Rx410[0]  ((For Internal Reference: This bit is RW when D0F2 DPR\_LOCK is set to 0.  @((#control\_lock = lock\_port DPR\_LOCK)) )) | DPR\_SIZE[7:0] |  | vcc | \* | x | x |
| 3 | RW | RO | 0 | **Reserved** | Rx410[3] |  | vcc | 0 | x | x |
| 2 | RWL | RO | 0 | **DPR Enable**  0: Disable DPR 1: Enable DPR  ((For Internal Reference: This bit is RW when D0F2 DPR\_LOCK is set to 0.  @((#control\_lock = lock\_port DPR\_LOCK)) )) | DPR\_EN |  | vcc | \* | x | x |
| 1 | RO | NA | 0 | **Reserved** | DPR\_STS |  | vcc | 0 | x | x |
| 0 | RWL | RO | 0 | **Lock Bit to Lock DMA Protection Control**  0: No effect  1: Bits 11:0 will be locked down in this register.  ((For Internal Reference: This bit is RW when D0F2 DPR\_LOCK is set to 0.  @((#control\_lock = lock\_port DPR\_LOCK)) )) | DPR\_LOCK |  | vcc | 0 | x | x |

Offset Address: 413-412h (D0F2)  
Reserved Default Value: 0000h

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit | **Attribute** | **HW Property** | **Default** | **Description** | Mnemonic | **ChipRev** | **PwrDm** | **S** | **P** | **E** |
| 15:0 | RO | NA | 0 | **Reserved** | Rx412[15:0] |  | vcc | 0 | x | x |

Offset Address: 414-41Fh (D0F2) – Reserved

([TIC Question 1. End of questions. Thanks!])