

## 14.0 Ballout and Package Information

The Intel® Atom™ Processor E6xx Series comes in an 22 mm x 22 mm Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 676 solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Refer to the *Intel® Atom™ Processor E6xx Series Thermal and Mechanical Design Guidelines* for details on package mechanical dimensions and tolerance, as well as other key package attributes.

### Dimensions:

- Package parameters: 22 mm x 22 mm
- Ball Count: 676
- Land metal diameter: 500 microns
- Solder resist opening: 430 microns

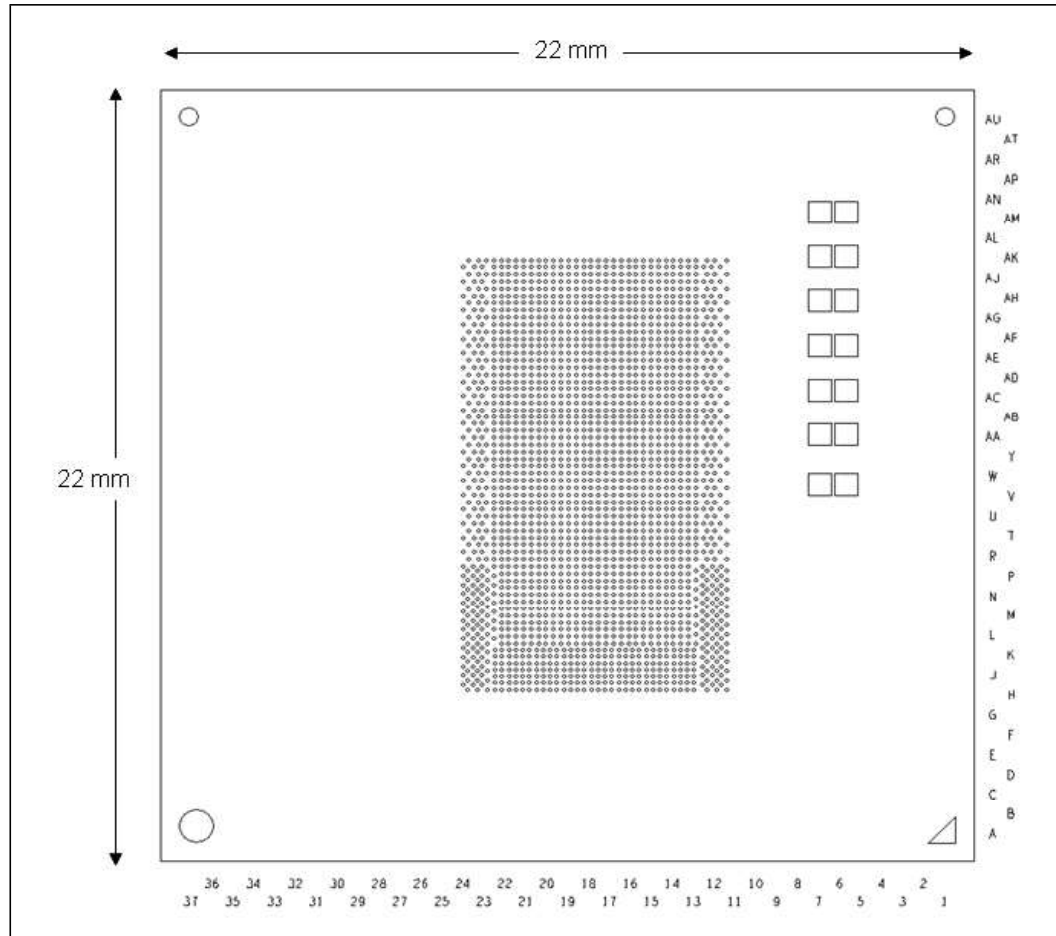
### Tolerances:

- .X -  $\pm 0.1$
- .XX -  $\pm 0.05$
- Angles -  $\pm 1.0$  degrees



## 14.1 Package Diagrams

Figure 10. Intel® Atom™ Processor E6xx Series Silicon and Die Side Capacitor (Top View)



SYMBOL	MILLIMETERS	COMMENTS
A	2.997	2.35
A <sub>1</sub>	0.32	0.32
A <sub>2</sub>	0.905	1.045
b	0.45	0.45
C <sub>1</sub>	1.51	
C <sub>2</sub>	12.79	
D	21.95	22.05
D <sub>1</sub>	20.316	BASIC
e	0.8	BASIC
E	21.95	22.05
F	0.75	
F <sub>1</sub>	20.316	BASIC
H <sub>1</sub>	16.188	BASIC
H <sub>2</sub>	16.188	BASIC
N	675	



## 14.2 Ballout Definition and Signal Locations

Figure 12 provides the ballout as viewed from the top of the package. Table 407 lists the ballout alphabetically by signal name.

**Figure 12. Intel® Atom™ Processor E6xx Series Package Ball Pattern**

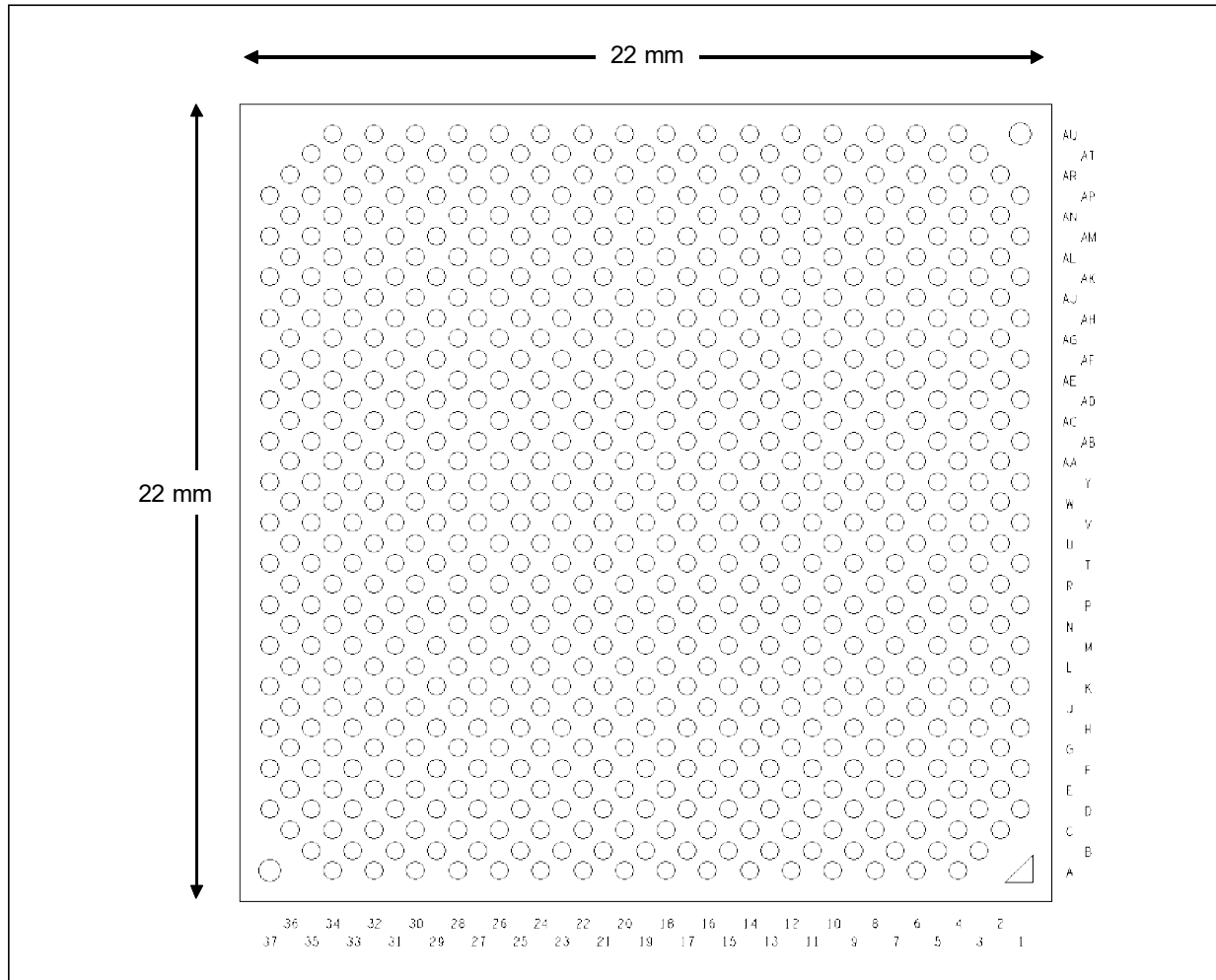




Figure 13. Intel® Atom™ Processor E6xx Series Ball Map (Sheet 1 of 5)

	9	8	7	6	5	4	3	2	1
AU		M_CKP		M_DQ[8]		VSS			
AT	M_SRFWEN		M_CKN		M_DQS[1]		VSS		
AR		VSS		VSS		M_DQ[10]		VSS	
AP	M_DQ[25]		M_MA[5]		M_DQ[13]		VSS		VSS
AN		M_DQ[24]		VSS		M_MA[2]		M_MA[4]	
AM	VSS		M_CKE[1]		M_DQ[14]		VSS		M_BS[1]
AL		NC		VSS		M_DQ[9]		M_BS[2]	
AK	VSS		M_CKE[0]		M_DQ[12]		VSS		M_DQ[0]
AJ		M_MA[14]		VSS		M_DQ[11]		M_DQ[2]	
AH	VCC180		M_MA[6]		M_DQ[15]		VSS		M_DQ[3]
AG		M_MA[11]		VSS		M_DQ[4]		M_DM[0]	
AF	VSS		M_MA[9]		M_DM[1]		VSS		M_DQ[1]
AE		M_RCOMPOUT		VSS		M_DQ[5]		VSS	
AD	VSS		M_RCVENOUT		M_MA[12]		VSS		IO_TDO
AC		M_RCVENIN		VSS		M_DQ[7]		IO_TDI	
AB	VSS		M_MA[8]		M_BS[0]		VSS		IO_TMS
AA		M_MA[0]		VSS		M_DQ[6]		RTCRST_B	
Y	VSS		M_MA[3]		M_DQS[0]		VSS		PWROK
W		M_MA[7]		VSS		HPLL_REFCLK_N		HIGHZ_B	
V	VSS		VSS		HPLL_REFCLK_P		VSS		RSMRST_B
U		VSS		VSS		IO_RX_CVREF		IO_RX_GVREF	
T	VSS		VSS		IOCOMP1[0]		VSS		IO_TCK
R		VSS		IOCOMP1[1]		NC		IO_TRST_N	
P	VSS		VSS		VSS		VSS		GPIO_SUS[2]
N		VSS		VSS		GPIO_SUS[1]		GPE_B	
M	VSS		RTCX2		SLPMODE		GPIO_SUS[3]		GPIO_SUS[5]
L		RTCX1		VSS		RSTWARN		GPIO_SUS[6]	
K	VSS		RSTRDY_B		RESET_B		VSS		SLPRDY_B
J		CLK14		VSS		GPIO_SUS[7]		SUSCLK	
H	VSS		SMI_B		SPI_CS_B		TEST_B		GPIO_SUS[8]
G		LPC_AD[2]		VSS		NC		SPKR	
F	VSS		SMB_ALERT_B		SPI_SCK		VSS		SPI_MOSI
E		LPC_SERIRQ		GPIO[0]		SMB_CLK		SPI_MISO	
D	LPC_CLKOUT[1]		LPC_CLKRUN_B		GPIO[3]		LPC_AD[1]		VSS
C		VSS		VSS		GPIO[1]		VSS	
B	NC		SDVO_CTRLDATA		GPIO[4]		VSS		
A		NC		GPIO[2]		VSS			



Figure 14. Intel® Atom™ Processor E6xx Series Ball Map (Sheet 2 of 5)

	16	15	14	13	12	11	10
AU	M_DQ[16]		M_DQS[3]		M_DQ[26]		M_MA[13]
AT		M_DQ[31]		M_WEB		M_DQ[27]	
AR	VSS		VSS		VSS		VSS
AP		M_DQS[2]		M_DM[3]		M_DQ[28]	
AN	TDI		M_CSB[0]		M_ODT[1]		M_DQ[29]
AM		VSS		VSS		VSS	
AL	TMS		TRST_B		VSS		M_DQ[30]
AK		VCCP		VCC180		M_ODT[0]	
AJ	VCCPQ		VCC180		M_CSB[1]		M_RASB
AH		VCC180		VCC180		VCC180	
AG	VSS		VSS		VCC180		VSS
AF		VSS		VCCPDDR		VSS	
AE	VSS		VSS		VCCPDDR		VSS
AD		VCC180		VSS		VSS	
AC	VSS		VCCA		VCCPDDR		VSS
AB		VSS		VCC180SR		VSS	
AA	VCC180		VSS		VSS		M_MA[1]
Y		VCC180		VSS		VSS	
W	VCC180		VSS		VCCPDDR		M_MA[10]
V		VSS		VCCPDDR		VSS	
U	VCC180		VCC180		VSS		VSS
T		VCC180		VCC180		VSS	
R	VCC180		VSS		VSS		VSS
P		VCCP		VSS		VCCQ	
N	VSS		VSS		VCCPSUS		VSS
M		VCCSFRHPLL		VCC33RTC		VSS	
L	VSS		VSS		VCCRTCEXT		GPIO_SUS[0]
K		VCCDSUS		VCCP33SUS		GPIO_SUS[4]	
J	VCCP33		VSS		VSS		VSS
H		VSS		VSS		WAKE_B	
G	VSS		SMB_DATA		LPC_AD[3]		THRM_B
F		VSS		VSS		VSS	
E	NC		SDVO_CTRLCLK		LPC_CLKOUT[0]		LPC_CLKOUT[2]
D		NC		LPC_AD[0]		LPC_FRAME_B	
C	VSS		VSS		VSS		VSS
B		SDVO_TVCLKINP		SDVO_CLKP		SDVO_REFCLKP	
A	SDVO_REDN		SDVO_TVCLKINN		SDVO_CLKN		SDVO_REFCLKN



Figure 15. Intel® Atom™ Processor E6xx Series Ball Map (Sheet 3 of 5)

	23	22	21	20	19	18	17
AU		M_DQ[20]		M_DM[2]		M_DQ[17]	
AT	M_DQ[21]		M_DQ[19]		M_DQ[22]		M_DQ[18]
AR		VSS		VSS		VSS	
AP	GTLVREF		BSEL[1]		GPIO_B		M_CASB
AN		TCK		VSS		TDO	
AM	VSS		VSS		VSS		VSS
AL		NCTDI		NC		NC	
AK	PWRMODE[0]		NC		NC		NC
AJ		VCCSENSE		VCCA		VNN	
AH	VSS		VCC_VSSSENSE		VSS		VSS
AG		VCC		VNNSENSE		VNN	
AF	VSS		VSS		VSS		VSS
AE		VCC		VNN		VNN	
AD	VSS		VSS		VSS		VSS
AC		VCC		VNN		VNN	
AB	VSS		VSS		VSS		VSS
AA		VCC		VNN		VNN	
Y	VSS		VSS		VSS		VSS
W		VCC		VNN		VNN	
V	VSS		VSS		VSS		VSS
U		VCC		VNN		VNN	
T	VMM		VSS		VSS		VSS
R		VCC		VNN		VNN	
P	VSS		VSS		VCCFHV		VCC180
N		VCCD		VCCDSENSE		VCCQHPLL	
M	VSS		VSS		VCCD_VSSSENSE		VSS
L		VCCD		VCCD		VCCD	
K	VCCA_PEG		VCCA_PEG		VCCD_DPL		VCCP33
J		VCCA_PEG		VCCA_PEG		VCCA_PEG	
H	VSS		VSS		VCCSFR_EXP		VCCSFRDPLL
G		VSS		VSS		VSS	
F	VSS		VSS		VSS		VSS
E		PCIE_RBIAS		SDVO_STALLP		SDVO_BLUEP	
D	NC		NC		SDVO_STALLN		SDVO_BLUEN
C		VSS		VSS		VSS	
B	PCIE_ICOMPI		SDVO_INTP		SDVO_GREENN		SDVO_REDP
A		NC		SDVO_INTN		SDVO_GREENP	

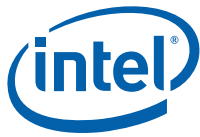


Figure 16. Intel® Atom™ Processor E6xx Series Ball Map (Sheet 4 of 5)

	30	29	28	27	26	25	24
AU	NCTDO		THERMTRIP_B		BCLKN		M_DQ[23]
AT		VID[1]		PROCHOT_B		BCLKP	
AR	VSS		VSS		VSS		VSS
AP		VID[3]		NCTMS		BSEL[2]	
AN	NC		NCTCK		PWRMODE[1]		NC
AM		VSS		VSS		VCCF	
AL	GTLPREF		VID[2]		VIDEN[1]		PWRMODE[2]
AK		VSS		VIDEN[0]		VCCPA	
AJ	COMP0[0]		VSS		VCCP		VSS
AH		VSS		VSS		VSS	
AG	NC		VSS		VCCP		VCC
AF		VSS		VCCQ		VSS	
AE	NC		VSS		VSS		VCC
AD		VSS		VSS		VSS	
AC	NC		VSS		VCCP		VCC
AB		VSS		VSS		VCCA	
AA	NC		VSS		VSS		VCC
Y		VSS		VSS		VSS	
W	NC		VSS		VCCP		VCC
V		VSS		VSS		VSS	
U	LVD_DATAP_1		VSS		VCCPA		VCC
T		VSS		VCCA180		VCCD180	
R	LVD_IBG		VSS		VCCP		VCC
P		VSS		VSS		VCCP33	
N	IOCOMP0[0]		VSS		VCCQ		VCCD
M		VSS		VSS		VCCD	
L	VSS		VSS		VCCP		VCCD
K		VSS		VSS		VSS	
J	VSS		VSS		VSS		VCCA_PEG
H		VSS		VSS		VCCA_PEG	
G	VSS		VSS		VSS		VSS
F		VSS		VSS		VSS	
E	PCIE_PERN[1]		PCIE_PETN[1]		PCIE_PETN[0]		NC
D		PCIE_PERP[1]		PCIE_PETP[1]		PCIE_PETP[0]	
C	VSS		VSS		VSS		VSS
B		NC		PCIE_CLKINP		PCIE_ICOMPO	
A	PCIE_PERP[0]		NC		PCIE_CLKINN		PCIE_RCOMPO





Figure 17. Intel® Atom™ Processor E6xx Series Ball Map (Sheet 5 of 5)

	37	36	35	34	33	32	31
AU			VSS		VID[0]		
AT		VSS		VID[5]		VID[6]	
AR			VID[4]		VSS		
AP	VSS	BPM_B[1]		BPM_B[0]		NC	
AN		BPM_B[3]		BPM_B[2]	VSS		
AM	PREQ_B		VSS	PRDY_B		BSEL[0]	
AL		NC		COMP0[1]	VSS		
AK	NC		NC		NC		NC
AJ		NC		NC		VSS	
AH	GTLREF		VSS		NC		NC
AG		CMREF		NC		VSS	
AF	NC		NC		NC		NC
AE		NC		NC		VSS	
AD	NC		VSS		NC		NC
AC		NC		DLIOCMREF		VSS	
AB	DLIOGTLREF		COMP1[0]		COMP1[1]		NC
AA		NC		NC		VSS	
Y	NC		VSS		NC		NC
W		NC		NC		VSS	
V	NC		NC		LVD_DATAP_0		LVD_DATAN_1
U		LVD_CLKP		LVD_DATAN_0		VSS	
T	LVD_CLKN		VSS		LVD_DATAP_3		LVD_VBG
R		LVD_DATAN_2		LVD_DATAN_3		VSS	
P	LVD_DATAP_2		VSS		THRMDA		HDA_RST_B
N		LVD_VREFL		THRMDC		HDA_SDI[0]	
M	LVD_VREFH		VSS		VSS		VSS
L		NC		IOCOMP0[1]		VSS	
K	NC		VSS		IOGTLREF		VSS
J		HDA_SDO		IOCMREF		VSS	
H	RCOMP		VSS		VSS		PCIE_PETP[3]
G		HDA_SDI[1]		VSS		PCIE_PETN[3]	
F	HDA_DOCKEN_B		HDA_SYNC		VSS		VSS
E		HDA_CLK		NC		PCIE_PETN[2]	
D	VSS		HDA_DOCKRST_B		PCIE_PERP[3]		PCIE_PETP[2]
C		VSS		PCIE_PERN[3]		VSS	
B			VSS		PCIE_PERN[2]		PCIE_PERN[0]
A			VSS			PCIE_PERP[2]	



Table 407. Pin List

Pin Name	Ball#
BCLKP	AT25
BCLKN	AU26
BPM_B[0]	AP33
BPM_B[1]	AP35
BPM_B[2]	AN34
BPM_B[3]	AN36
BSEL[0]	AM31
BSEL[1]	AP21
BSEL[2]	AP25
CLK14	J8
CMREF	AG36
COMP0[0]	AJ30
COMP0[1]	AL34
COMP1[0]	AB35
COMP1[1]	AB33
DLIOCMREF	AC34
DLIOGTLREF	AB37
GPE_B	N2
GPIO[0]	E6
GPIO[1]	C4
GPIO[2]	A6
GPIO[3]	D5
GPIO[4]	B5
GPIO_SUS[0]	L10
GPIO_SUS[1]	N4
GPIO_SUS[2]	P1
GPIO_SUS[3]	M3
GPIO_SUS[4]	K11
GPIO_SUS[5]	M1
GPIO_SUS[6]	L2
GPIO_SUS[7]	J4
GPIO_SUS[8]	H1
GPIO_B	AP19
GTLREF	AL30
GTLVREF	AH37
HDA_CLK	AP23
HDA_DOCKEN_B	E36
HDA_DOCKRST_B	F37
HDA_RST_B	D35
HDA_SDI[0]	P31
HDA_SDI[1]	N32
HDA_SDO	G36
HDA_SYNC	J36
	F35

Table 407. Pin List

Pin Name	Ball#
HIGHZ_B	W2
HPLL_REFCLK_N	W4
HPLL_REFCLK_P	V5
IO_RX_CVREF	U4
IO_RX_GVREF	U2
IO_TCK	T1
IO_TDI	AC2
IO_TDO	AD1
IO_TMS	AB1
IO_TRST_B	R2
IOCMREF	J34
IOCOMP0[0]	N30
IOCOMP0[1]	L34
IOCOMP1[0]	T5
IOCOMP1[1]	R6
IOGTLREF	K33
LPC_AD[0]	D13
LPC_AD[1]	D3
LPC_AD[2]	G8
LPC_AD[3]	G12
LPC_CLKOUT[0]	E12
LPC_CLKOUT[1]	D9
LPC_CLKOUT[2]	E10
LPC_CLKRUN_B	D7
LPC_FRAME_B	D11
LPC_SERIRQ	E8
LVD_CLKN	T37
LVD_CLKP	U36
LVD_DATAN_0	U34
LVD_DATAN_1	V31
LVD_DATAN_2	R36
LVD_DATAN_3	R34
LVD_DATAP_0	V33
LVD_DATAP_1	U30
LVD_DATAP_2	P37
LVD_DATAP_3	T33
LVD_IBG	R30
LVD_VBG	T31
LVD_VREFH	M37
LVD_VREFL	N36
M_BS[0]	AB5
M_BS[1]	AM1
M_BS[2]	AL2
M_CASB	AP17
M_CKP	AU8

Table 407. Pin List

Pin Name	Ball#
M_CKN	AT7
M_CKE[0]	AK7
M_CKE[1]	AM7
M_CSB[0]	AN14
M_CSB[1]	AJ12
M_DM[0]	AG2
M_DM[1]	AF5
M_DM[2]	AU20
M_DM[3]	AP13
M_DQ[0]	AK1
M_DQ[1]	AF1
M_DQ[10]	AR4
M_DQ[11]	AJ4
M_DQ[12]	AK5
M_DQ[13]	AP5
M_DQ[14]	AM5
M_DQ[15]	AH5
M_DQ[16]	AU16
M_DQ[17]	AU18
M_DQ[18]	AT17
M_DQ[19]	AT21
M_DQ[2]	AJ2
M_DQ[20]	AU22
M_DQ[21]	AT23
M_DQ[22]	AT19
M_DQ[23]	AU24
M_DQ[24]	AN8
M_DQ[25]	AP9
M_DQ[26]	AU12
M_DQ[27]	AT11
M_DQ[28]	AP11
M_DQ[29]	AN10
M_DQ[3]	AH1
M_DQ[30]	AL10
M_DQ[31]	AT15
M_DQ[4]	AG4
M_DQ[5]	AE4
M_DQ[6]	AA4
M_DQ[7]	AC4
M_DQ[8]	AU6
M_DQ[9]	AL4
M_DQS[0]	Y5
M_DQS[1]	AT5
M_DQS[2]	AP15
M_DQS[3]	AU14

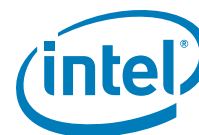


Table 407. Pin List

Pin Name	Ball#
M_MA[0]	AA8
M_MA[1]	AA10
M_MA[10]	W10
M_MA[11]	AG8
M_MA[12]	AD5
M_MA[13]	AU10
M_MA[14]	AJ8
M_MA[2]	AN4
M_MA[3]	Y7
M_MA[4]	AN2
M_MA[5]	AP7
M_MA[6]	AH7
M_MA[7]	W8
M_MA[8]	AB7
M_MA[9]	AF7
M_ODT[0]	AK11
M_ODT[1]	AN12
M_RASB	AJ10
M_RCOMPOUT	AE8
M_RCVENIN	AC8
M_RCVENOUT	AD7
M_SRFWEN	AT9
M_WEB	AT13
NCTCK	AN28
NCTDI	AL22
NCTDO	AU30
NCTMS	AP27
PCIE_CLKINN	A26
PCIE_CLKINP	B27
PCIE_ICOMPI	B23
PCIE_ICOMPO	B25
PCIE_PERN[0]	B31
PCIE_PERN[1]	E30
PCIE_PERN[2]	B33
PCIE_PERN[3]	C34
PCIE_PERP[0]	A30
PCIE_PERP[1]	D29
PCIE_PERP[2]	A32
PCIE_PERP[3]	D33
PCIE_PETN[0]	E26
PCIE_PETN[1]	E28
PCIE_PETN[2]	E32
PCIE_PETN[3]	G32
PCIE_PETP[0]	D25

Table 407. Pin List

Pin Name	Ball#
PCIE_PETP[1]	D27
PCIE_PETP[2]	D31
PCIE_PETP[3]	H31
PCIE_RBIA5	E22
PCIE_RCOMPO	A24
PRDY_B	AM33
PREQ_B	AM37
PROCHOT_B	AT27
PWRMODE[0]	AK23
PWRMODE[1]	AN26
PWRMODE[2]	AL24
PWROK	Y1
RCOMP	H37
RESET_B	K5
RSMRST_B	V1
RSTRDY_B	K7
RSTWARN	L4
RTCRST_B	AA2
RTCX1	L8
RTCX2	M7
SDVO_BLUEN	D17
SDVO_BLUEP	E18
SDVO_CLKN	A12
SDVO_CLKP	B13
SDVO_CTRLCLK	E14
SDVO_CTRLDATA	B7
SDVO_GREENN	B19
SDVO_GREENP	A18
SDVO_INTN	A20
SDVO_INTP	B21
SDVO_REDN	A16
SDVO_REDP	B17
SDVO_REFCLKN	A10
SDVO_REFCLKP	B11
SDVO_STALLN	D19
SDVO_STALLP	E20
SDVO_TVCLKINN	A14
SDVO_TVCLKINP	B15
SLPMODE	M5
SLPRDY_B	K1
SMB_ALERT_B	F7
SMB_CLK	E4
SMB_DATA	G14
SMI_B	H7

Table 407. Pin List

Pin Name	Ball#
SPI_CS_B	H5
SPI_MISO	E2
SPI_MOSI	F1
SPI_SCK	F5
SPKR	G2
SUSCLK	J2
TCK	AN22
TDI	AN16
TDO	AN18
TEST_B	H3
THERMTRIP_B	AU28
THRM_B	G10
THRMADA	P33
THRMDC	N34
TMS	AL16
TRST_B	AL14
VCC	R22
VCC	R24
VCC	U22
VCC	U24
VCC	W22
VCC	W24
VCC	AA22
VCC	AA24
VCC	AC22
VCC	AC24
VCC	AE22
VCC	AE24
VCC	AG22
VCC	AG24
VCC180	P17
VCC180	R16
VCC180	T13
VCC180	T15
VCC180	U14
VCC180	U16
VCC180	W16
VCC180	Y15
VCC180	AA16
VCC180	AD15
VCC180	AG12
VCC180	AH9
VCC180	AH11
VCC180	AH13

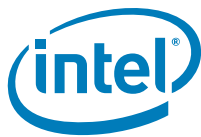


Table 407. Pin List

Pin Name	Ball#
VCC180	AH15
VCC180	AJ14
VCC180	AK13
VCC180SR	AB13
VCC33RTC	M13
VCCA	AB25
VCCA	AC14
VCCA	AJ20
VCCA_PEG	H25
VCCA_PEG	J18
VCCA_PEG	J20
VCCA_PEG	J22
VCCA_PEG	J24
VCCA_PEG	K21
VCCA_PEG	K23
VCCA180	T27
VCCD	L18
VCCD	L20
VCCD	L22
VCCD	L24
VCCD	M25
VCCD	N22
VCCD	N24
VCCD_DPL	K19
VCCD180	T25
VCCDSENSE	N20
VCCDSUS	K15
VCCF	AM25
VCCFHV	P19
VCCP	L26
VCCP	P15
VCCP	R26
VCCP	W26
VCCP	AC26
VCCP	AG26
VCCP	AJ26
VCCP	AK15
VCCP33	J16
VCCP33	K17
VCCP33	P25
VCCP33SUS	K13
VCCPA	U26
VCCPA	AK25
VCCPDDR	V13

Table 407. Pin List

Pin Name	Ball#
VCCPDDR	W12
VCCPDDR	AC12
VCCPDDR	AE12
VCCPDDR	AF13
VCCPQ	AJ16
VCCPSUS	N12
VCCQ	N26
VCCQ	P11
VCCQ	AF27
VCCQHPLL	N18
VCCRTCEXT	L12
VCCSENSE	AJ22
VCCSFR_EXP	H19
VCCSFRDPLL	H17
VCCSFRHPLL	M15
VID[0]	AU32
VID[1]	AT29
VID[2]	AL28
VID[3]	AP29
VID[4]	AR34
VID[5]	AT33
VID[6]	AT31
VIDEN[0]	AK27
VIDEN[1]	AL26
VMM	T23
VNN	R18
VNN	R20
VNN	U18
VNN	U20
VNN	W18
VNN	W20
VNN	AA18
VNN	AA20
VNN	AC18
VNN	AC20
VNN	AE18
VNN	AE20
VNN	AG18
VNN	AJ18
VNNSENSE	AG20
VSS	A4
VSS	A34
VSS	B3
VSS	B35

Table 407. Pin List

Pin Name	Ball#
VSS	C2
VSS	C6
VSS	C8
VSS	C10
VSS	C12
VSS	C14
VSS	C16
VSS	C18
VSS	C20
VSS	C22
VSS	C24
VSS	C26
VSS	C28
VSS	C30
VSS	C32
VSS	C36
VSS	D1
VSS	D37
VSS	F3
VSS	F9
VSS	F11
VSS	F13
VSS	F15
VSS	F17
VSS	F19
VSS	F21
VSS	F23
VSS	F25
VSS	F27
VSS	F29
VSS	F31
VSS	F33
VSS	G6
VSS	G16
VSS	G18
VSS	G20
VSS	G22
VSS	G24
VSS	G26
VSS	G28
VSS	G30
VSS	G34
VSS	H9
VSS	H13

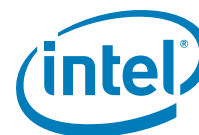


Table 407. Pin List

Pin Name	Ball#
VSS	H15
VSS	H21
VSS	H23
VSS	H27
VSS	H29
VSS	H33
VSS	H35
VSS	J6
VSS	J10
VSS	J12
VSS	J14
VSS	J26
VSS	J28
VSS	J30
VSS	J32
VSS	K3
VSS	K9
VSS	K25
VSS	K27
VSS	K29
VSS	K31
VSS	K35
VSS	L6
VSS	L14
VSS	L16
VSS	L28
VSS	L30
VSS	L32
VSS	M9
VSS	M11
VSS	M17
VSS	M21
VSS	M23
VSS	M27
VSS	M29
VSS	M31
VSS	M33
VSS	M35
VSS	N6
VSS	N8
VSS	N10
VSS	N14
VSS	N16
VSS	N28

Table 407. Pin List

Pin Name	Ball#
VSS	P3
VSS	P5
VSS	P7
VSS	P9
VSS	P13
VSS	P21
VSS	P23
VSS	P27
VSS	P29
VSS	P35
VSS	R8
VSS	R10
VSS	R12
VSS	R14
VSS	R28
VSS	R32
VSS	T3
VSS	T7
VSS	T9
VSS	T11
VSS	T17
VSS	T19
VSS	T21
VSS	T29
VSS	T35
VSS	U6
VSS	U8
VSS	U10
VSS	U12
VSS	U28
VSS	U32
VSS	V3
VSS	V7
VSS	V9
VSS	V11
VSS	V15
VSS	V17
VSS	V19
VSS	V21
VSS	V23
VSS	V25
VSS	V27
VSS	V29
VSS	W6
VSS	W14

Table 407. Pin List

Pin Name	Ball#
VSS	W28
VSS	W32
VSS	Y3
VSS	Y9
VSS	Y11
VSS	Y13
VSS	Y17
VSS	Y19
VSS	Y21
VSS	Y23
VSS	Y25
VSS	Y27
VSS	Y29
VSS	Y35
VSS	AA6
VSS	AA12
VSS	AA14
VSS	AA26
VSS	AA28
VSS	AA32
VSS	AB3
VSS	AB9
VSS	AB11
VSS	AB15
VSS	AB17
VSS	AB19
VSS	AB21
VSS	AB23
VSS	AB27
VSS	AB29
VSS	AC6
VSS	AC10
VSS	AC16
VSS	AC28
VSS	AC32
VSS	AD3
VSS	AD9
VSS	AD11
VSS	AD13
VSS	AD17
VSS	AD19
VSS	AD21
VSS	AD23
VSS	AD25
VSS	AD27

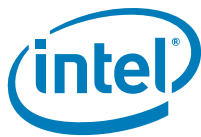


Table 407. Pin List

Pin Name	Ball#
VSS	AD29
VSS	AD35
VSS	AE2
VSS	AE6
VSS	AE10
VSS	AE14
VSS	AE16
VSS	AE26
VSS	AE28
VSS	AE32
VSS	AF3
VSS	AF9
VSS	AF11
VSS	AF15
VSS	AF17
VSS	AF19
VSS	AF21
VSS	AF23
VSS	AF25
VSS	AF29
VSS	AG6
VSS	AG10
VSS	AG14
VSS	AG16
VSS	AG28
VSS	AG32
VSS	AH3
VSS	AH17
VSS	AH19
VSS	AH23
VSS	AH25
VSS	AH27
VSS	AH29
VSS	AH35
VSS	AJ6
VSS	AJ24
VSS	AJ28
VSS	AJ32
VSS	AK3
VSS	AK9
VSS	AK29
VSS	AL6
VSS	AL12
VSS	AL32
VSS	AM3
VSS	AM9
VSS	AM11
VSS	AM13
VSS	AM15

Table 407. Pin List

Pin Name	Ball#
VSS	AM17
VSS	AM19
VSS	AM21
VSS	AM23
VSS	AM27
VSS	AM29
VSS	AM35
VSS	AN6
VSS	AN20
VSS	AN32
VSS	AP1
VSS	AP3
VSS	AP37
VSS	AR2
VSS	AR6
VSS	AR8
VSS	AR10
VSS	AR12
VSS	AR14
VSS	AR16
VSS	AR18
VSS	AR20
VSS	AR22
VSS	AR24
VSS	AR26
VSS	AR28
VSS	AR30
VSS	AR32
VSS	AR36
VSS	AT3
VSS	AT35
VSS	AU4
VSS	AU34
VCCD_VSSSENSE	M19
VCC_VSSSENSE	AH21
WAKE_B	H11
NC	A8
NC	A22
NC	A28
NC	B9
NC	B29
NC	D15
NC	D21
NC	D23
NC	E16
NC	E24

Table 407. Pin List

Pin Name	Ball#
NC	E34
NC	G4
NC	K37
NC	L36
NC	R4
NC	V35
NC	V37
NC	W30
NC	W34
NC	W36
NC	Y31
NC	Y33
NC	Y37
NC	AA30
NC	AA34
NC	AA36
NC	AB31
NC	AC30
NC	AC36
NC	AD31
NC	AD33
NC	AD37
NC	AE30
NC	AE34
NC	AE36
NC	AF31
NC	AF33
NC	AF35
NC	AF37
NC	AG30
NC	AG34
NC	AH31
NC	AH33
NC	AJ34
NC	AJ36
NC	AK17
NC	AK19
NC	AK21
NC	AK31
NC	AK33
NC	AK35
NC	AK37
NC	AL8
NC	AL18
NC	AL20
NC	AL36
NC	AN24
NC	AN30
NC	AP31

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