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**Question 1 - Harvard Architecture**

In Harvard Architecture, the instruction memory and data memory are two different units that use different buses to communicate with the control unit of the CPU.

Advantages:

1. Two separate memories allow for parallel access to both instructions and data. Therefore, it reduces the number of structural hazards, which results in faster execution.
2. Data memory and instruction memory can use different sizes for words/address space.
3. More secure (potentially) – programs cannot overwrite their own or other programs' instructions, maliciously or by mistake.

Disadvantages:

1. Design complexity, area and cost - Designing a CPU with multiple buses and multiple memory components is more complex, requires more space and ultimately more expensive.
2. Reduces memory utilization - instruction memory cannot be used for data and vice versa.

Since we wish to maximize the performance gain from pipelining, we think that Harvard architecture is a good choice.

In addition, for our DMA to work, we must have a different bus for the instruction memory. Therefore, if we use the Von Neuman Architecture would result in the bus being busy every cycle and the DMA will be suffering from starvation.

**Question 2 - Structural and Data Hazards**

There are three main types of hazards:

1. Structural hazard - occurs when two different instructions require access to the same resource simultaneously. In our case, such hazards happen when there is an LD instruction that immediately follows an ST instruction (resulting in reading and writing to memory in the same cycle).

Our solution is to compare the load and store registers of the instructions and stall one of the instructions (depending on the one that should complete second). This stall costs us one clock cycle.

The original timing diagram that shows the hazard:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| ST | F0 | F1 | D0 | D1 | E0 | E1 |  |  |
| LD |  | F0 | F1 | D0 | D1 | E0 | E1 |  |

After adding a stall:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| ST | F0 | F1 | D0 | D1 | E0 | E1 |  |  |
| LD |  | F0 | F1 | D0 | D1 | stall | E0 | E1 |

1. Data hazard – occurs when there is a dependency between two adjacent instructions. In our single core architecture, this is possible when an instruction reads data from the same location a previous instruction writes to, and the updated value is not yet available at the time of execution (read-after-write hazard).  
   Our solution is to check if the source registers are the destination registers of the previous instructions that weren't already updated. If so, we use forwarding from E1 to D1 or E0.

The original timing diagram that shows the hazard:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| ADD r5, r3, r4,0 | F0 | F1 | D0 | D1 | E0 | E1 |  |  |
| ADD r6, r6, r5,0 |  | F0 | F1 | D0 | D1 | E0 | E1 |  |
| ADD r7, r6, r5,0 |  |  | F0 | F1 | D0 | D1 | E0 | E1 |

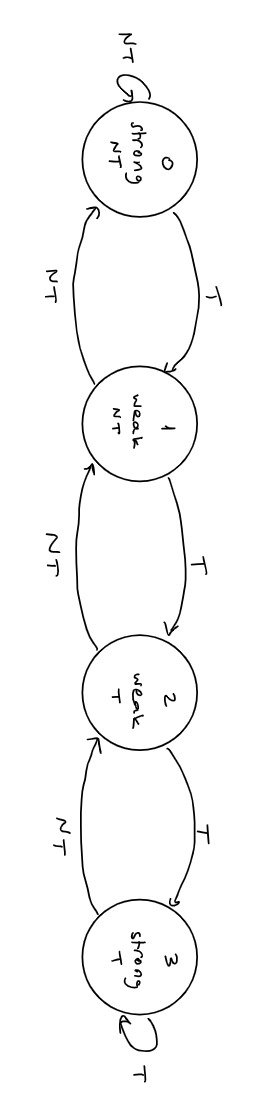
After adding forwarding:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| ADD r5, r3, r4,0 | F0 | F1 | D0 | D1 | E0 | E1 |  |  |
| ADD r6, r6, r5,0 |  | F0 | F1 | D0 | D1 | E0 | E1 |  |
| ADD r7, r6, r5,0 |  |  | F0 | F1 | D0 | D1 | E0 | E1 |

1. Control hazard - Occurs due to the usage of branch instructions. When we need to jump to a different instruction, the pipeline can continue executing instructions that won't execute because of the jump.   
   Our solution contains branch prediction (detailed in the next question) and flushes the pipeline as necessary.

**Question 3 - Branches and branch prediction**

For our branch prediction, we used a branch history table of size 10 with a 2-bit predictor. The scheme of the predicator is as followed:



In DEC0 stage - if we had a branch operation, we checked in the history table at index PC % 10, and if the prediction showed that the branch should be taken (value of 2 or 3), we flush the pipeline.

In EXEC1 stage - if we had a branch operation we updated the table according to the state machine above. We also calculated the next PC and flushed if needed.

We will illustrate the flush using an example when the first branch is taken and the prediction says it's taken. The next instruction will be flushed from the pipeline.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| JLT r0, r1, r2 12 | F0 | F1 | D0 | D1 | E0 | E1 |  |  |
| ADD r6, r6, r5, 0 |  | ~~F0~~ | ~~F1~~ |  |  |  |  |  |

Another example is when the first branch is taken and the prediction says it's not taken but we understand in EXEC1 that it is taken:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| JLT r0, r1, r2 12 | F0 | F1 | D0 | D1 | E0 | E1 |  |  |
| ADD r6, r6, r5, 0 |  | ~~F0~~ | ~~F1~~ | ~~D0~~ | ~~D1~~ | ~~E0~~ |  |  |

**Question 4 - Low level simulator pipeline implementation**

The required files are attached.

**Question 5 - Low level testing**

We verified that the outputs are the same as the previous labs.

The required files are attached.

**Question 6 - Speedup comparison, next generation improvements**

1.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
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|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

2. CPI is not 1. This is not surprising because the pipeline has new hazards like branch instructions. The average CPI is higher than 1, but it is getting closer to it.

3.

a. better branch prediction mechanism (avoids flushes).

1. b. Add cache (prevent structural hazards like LD after ST).
2. c. Add more cores (allows work in parallel).

**Question 7 - DMA testing in a pipeline environment**

We used the same test from lab 2.

Screenshot ?