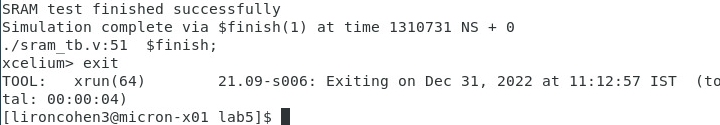
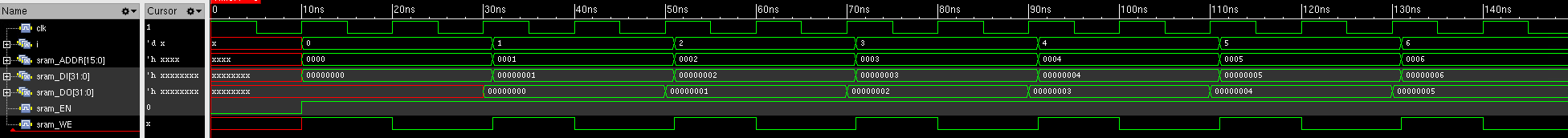
**Lab5 Report**Liron Cohen 207481268  
Yuval Mor 209011543

**Question 1 - SRAM verification**

We filled the missing code in the sram.v module and the sram\_tb.v module.

We ran the xrun command the simulation finished successfully:



The waveform is:

As we can see, on the clock rises and the integer 1 is written to address 0001 (shows in ) and on the clock rises and the output data that is read from address 0001 is the value 1 (shows in ), so the read after write is working and the simulation succeeded.

**Question 2 - processor implementation (no DMA)**

We filled the missing code in the alu.v module, sp.v module and ctl.v module.

The required files are attached.

**Question 3 - verification #1: example.bin**