MACRO PIXEL ASIC (MPA):
The readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC

Davide Ceresa

PH-ESE, CERN

on behalf of the *CMS Tracker Phase II electronics team*

PH-ESE seminar, 10th March, 2015
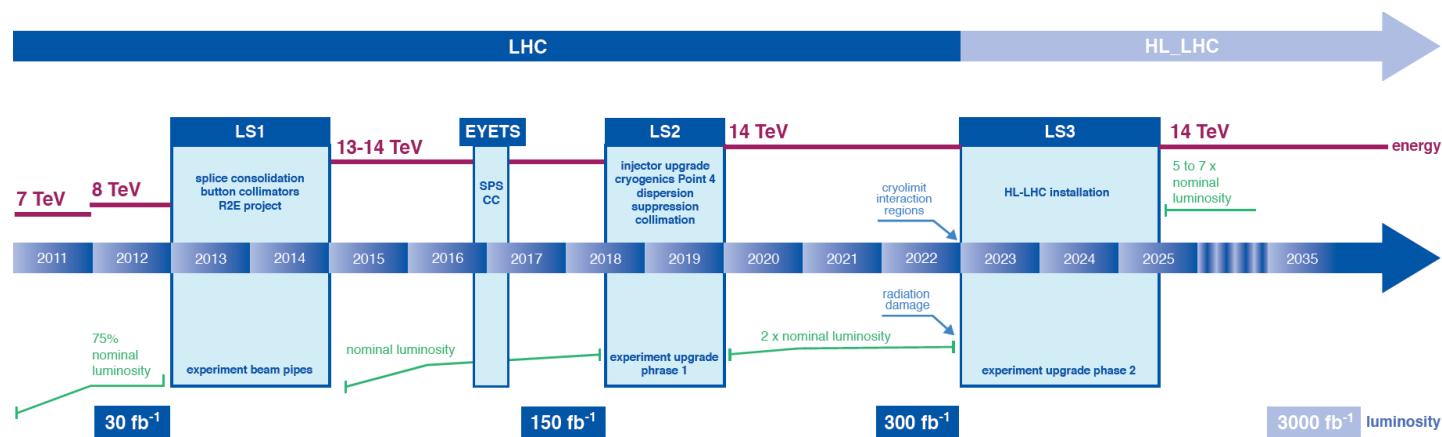
# CMS Tracker will be upgraded during Phase II

HL-LHC will operate at *14 TeV* centre of mass energy with a peak luminosity of *5x10^34cm-2s-1*

*To exploit the very high interaction rate and integrated luminosity, reaching 3000 fb-1, **major upgrades to CMS are necessary***

New Requirements for HL-LHC CMS Tracker

**High granularity** *for efficient track reconstruction* **beyond 140 Pile Up**

Pixelated sensors.
Only in the inner part of the CMS tracker

Improved material budget

Limited power *budget*

Provides **high pT information**, *called* **stubs,** *to the Level-1 Trigger*


Thanks to 3.8 T magnetic field

Two sensors *Pt - modules*

Level 1 Tracking

1 milion of interesting events can be fully readout per second

L1 rate
500 kHz – 1 MHz
Fixed Latency = 10 us

Level-1 accept

Full data

Stubs only

40 MHz

Readout → Track Find → CMS Level-1

CMS DAQ

Outer Tracker Front-end

Tracker Back-end

CMS
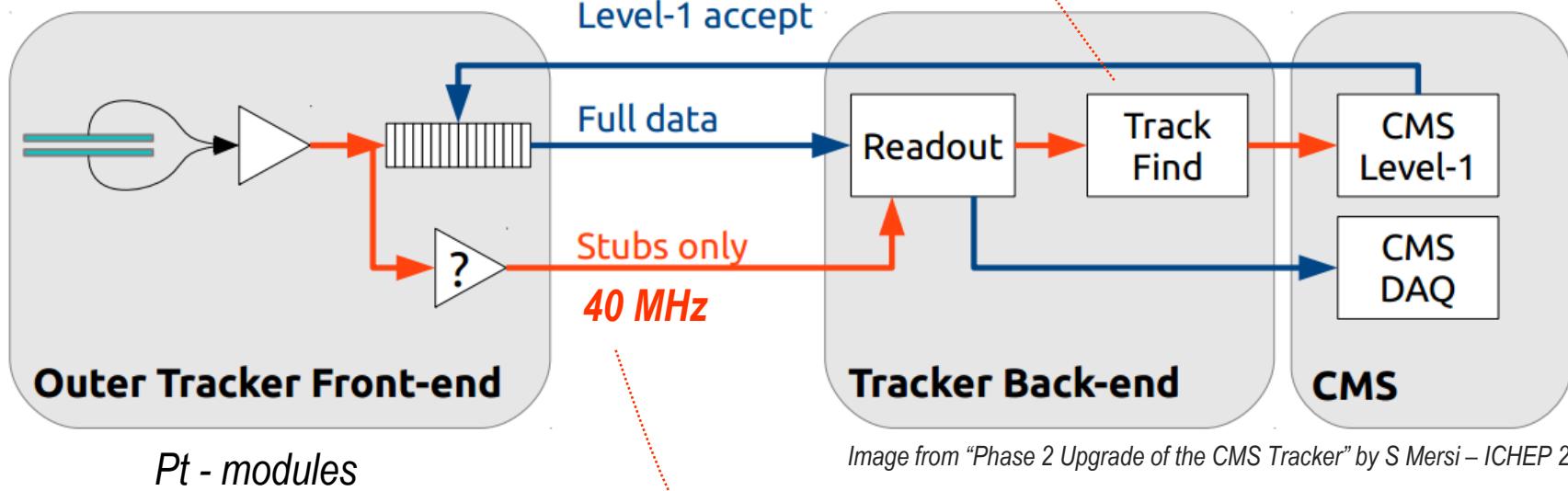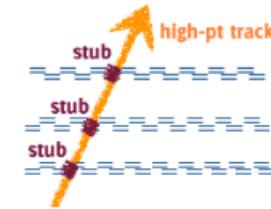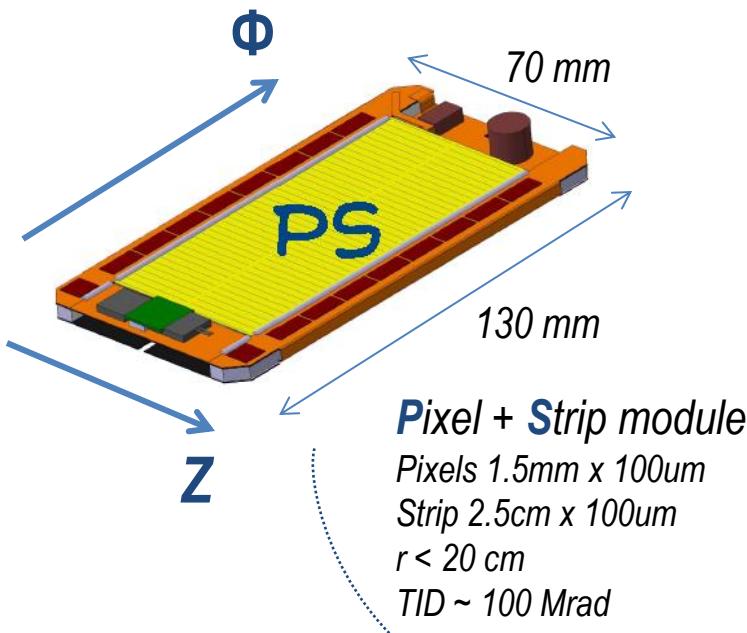
Pt - modules

Image from "Phase 2 Upgrade of the CMS Tracker" by S Mersi – ICHEP 2014"

Bunch crossing frequency
Ship all data @40 MHz is impossible
due to bandwidth limitation.

Pt modules and Pixels compose the Tracker

Φ

70 mm

PS

Z

130 mm

Pixel + **S**trip module
Pixels 1.5mm x 100um
Strip 2.5cm x 100um
r < 20 cm
TID ~ 100 Mrad

140 mm

2S

130 mm

2 Strip module
Strips 5 cm x 90 um
r > 40 cm
TID ~ 40 Mrad
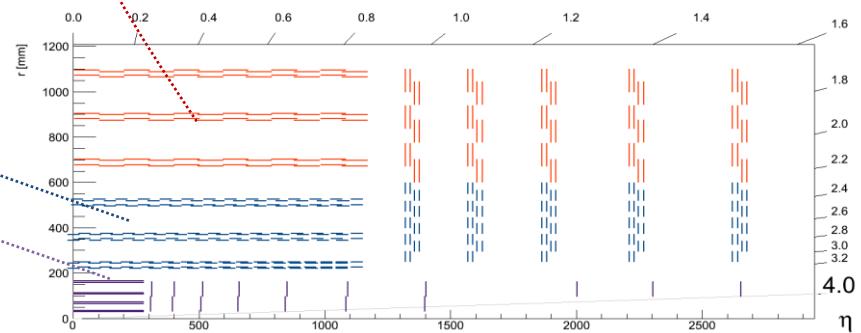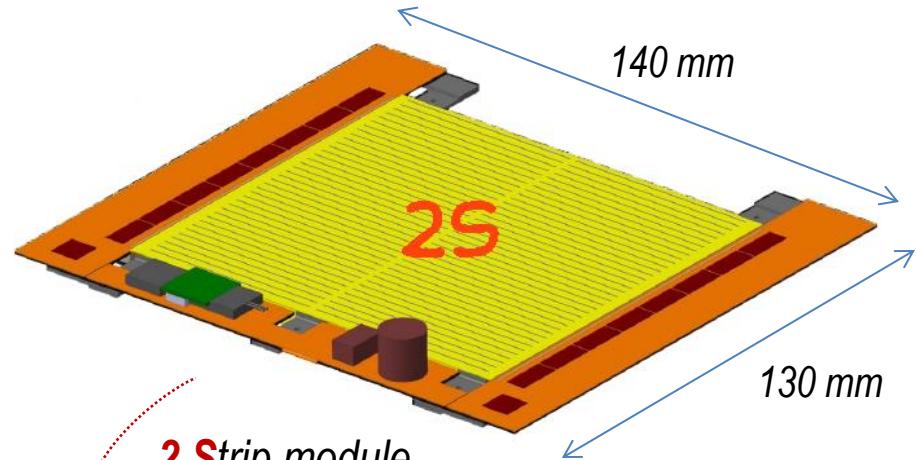
Pixel Detector (RD53)
Pixels 50um x 50um or 100um x 100um
r < 20 cm
*TID ~ **1 Grad***
No high-pT information
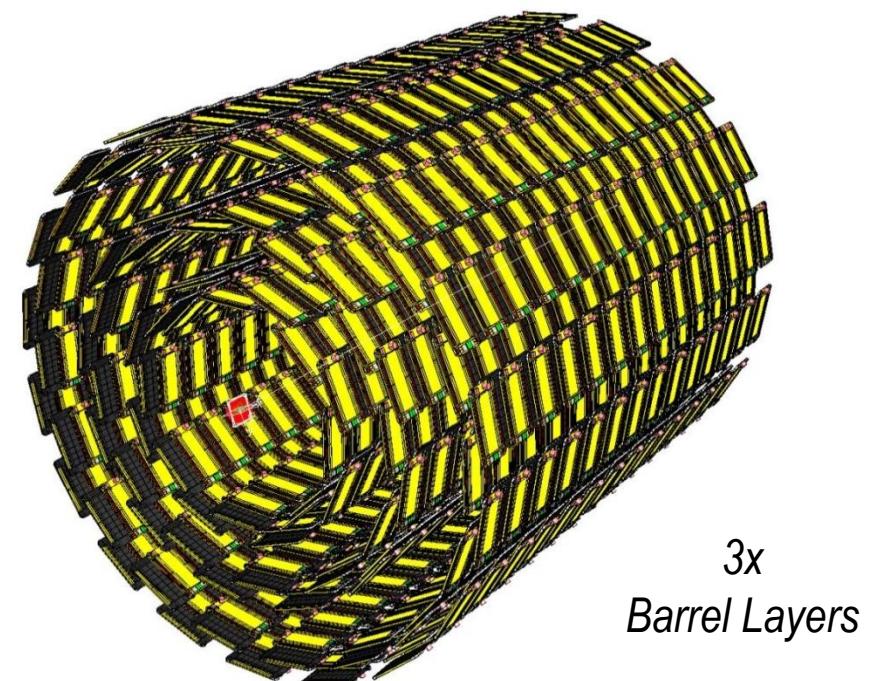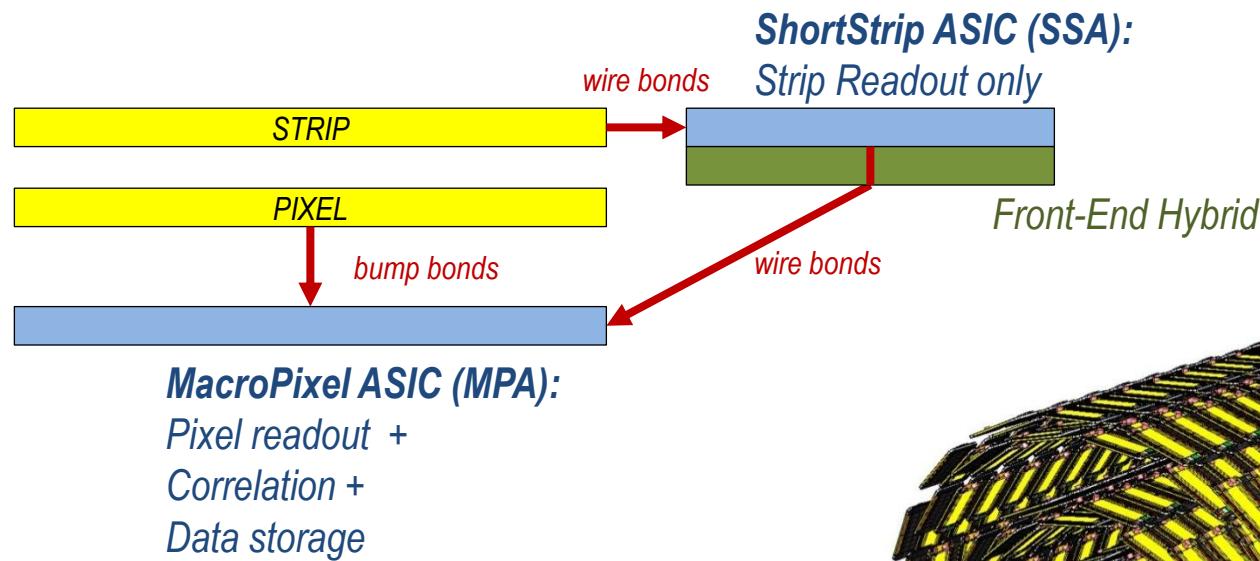
Tracker Layout by G.Bianchi, N.De Maio and S.Mersi

PIXEL STRIP MODULE
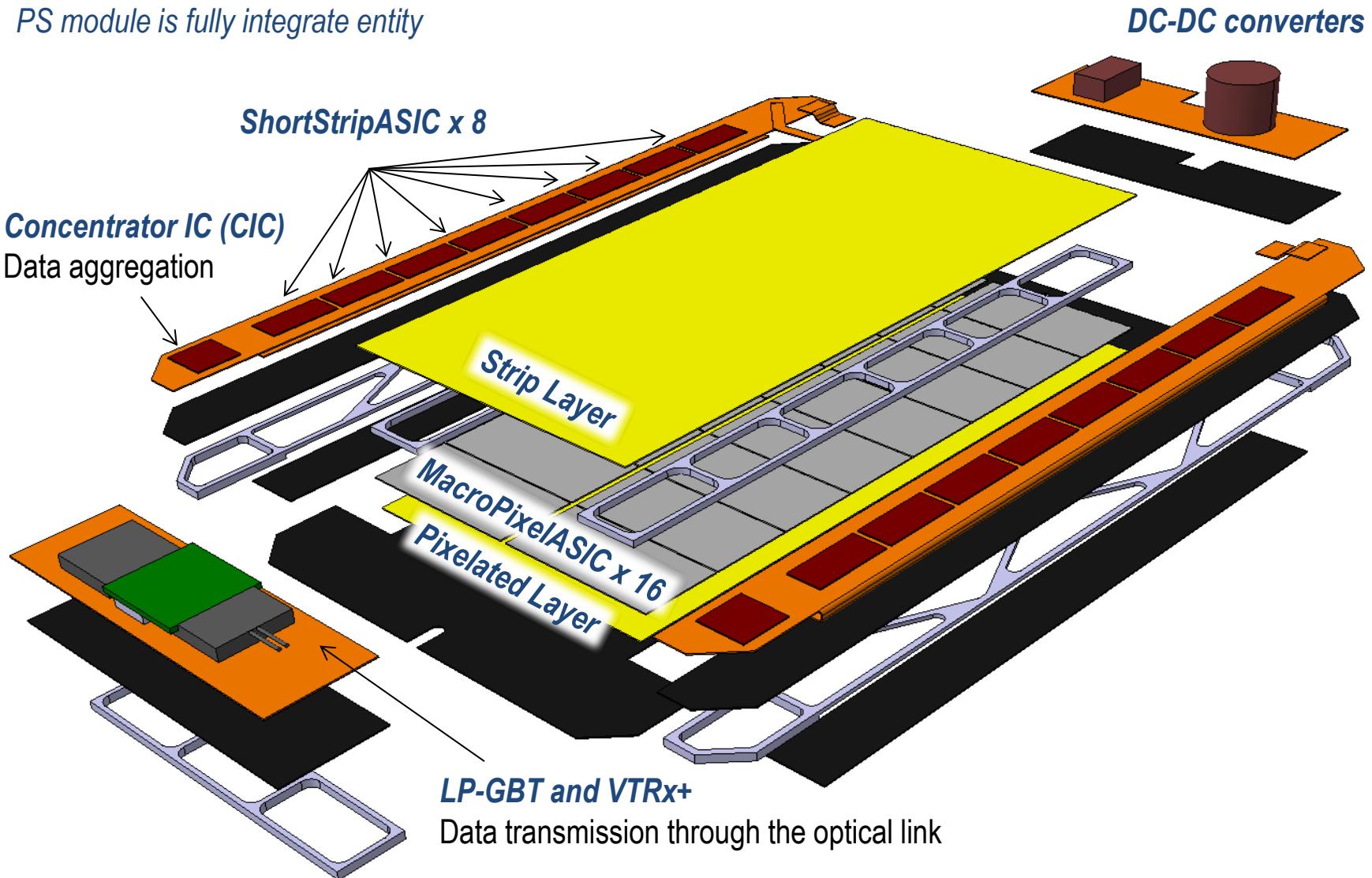
The Pixelated Pt-Module

# **P**ixel + **S**trip module readout scheme

ShortStrip ASIC (SSA):
Strip Readout only

STRIP

wire bonds

PIXEL

Front-End Hybrid

bump bonds

wire bonds

MacroPixel ASIC (MPA):
Pixel readout +
Correlation +
Data storage

3x
Barrel Layers
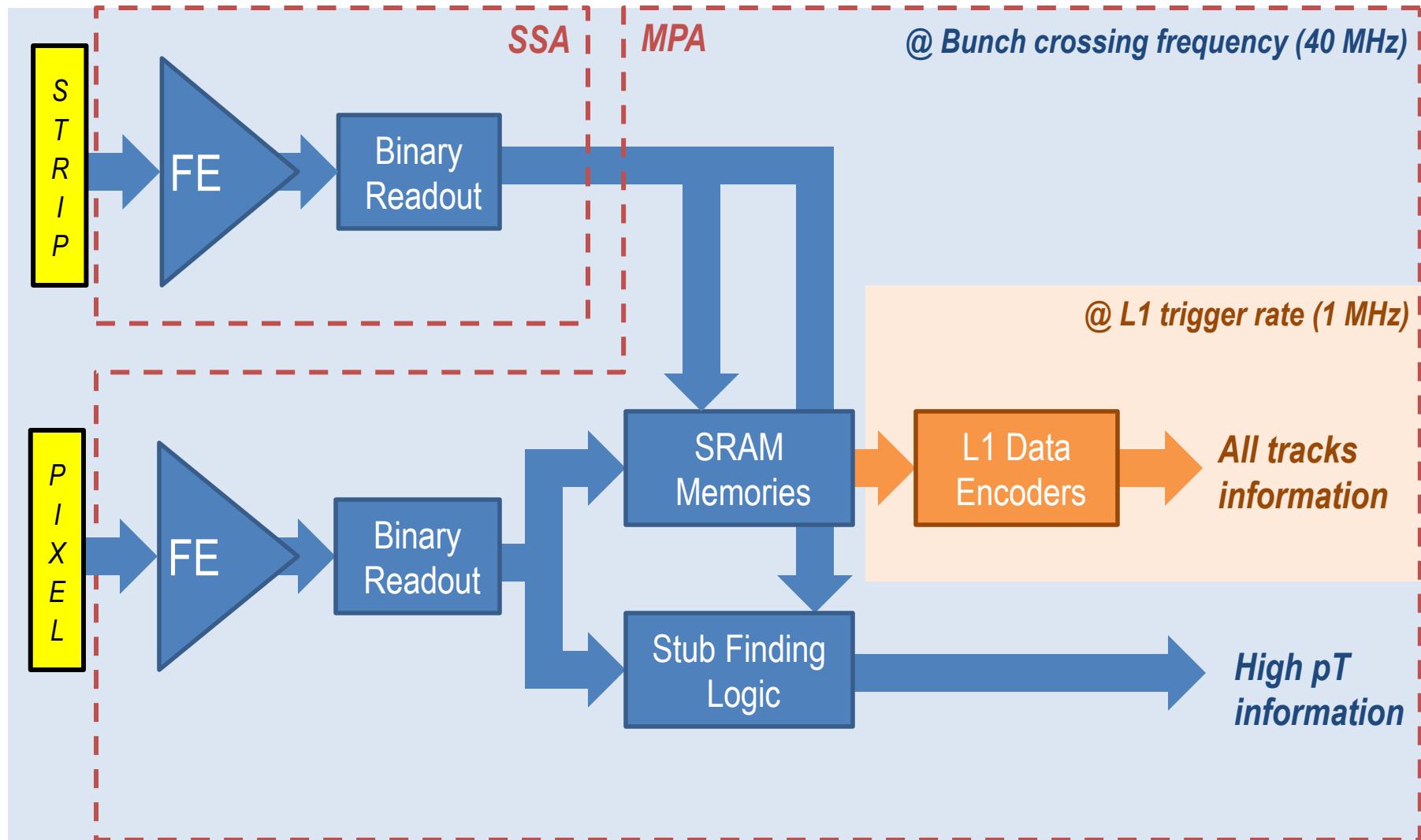
Pixel + **S**trip module exploded view
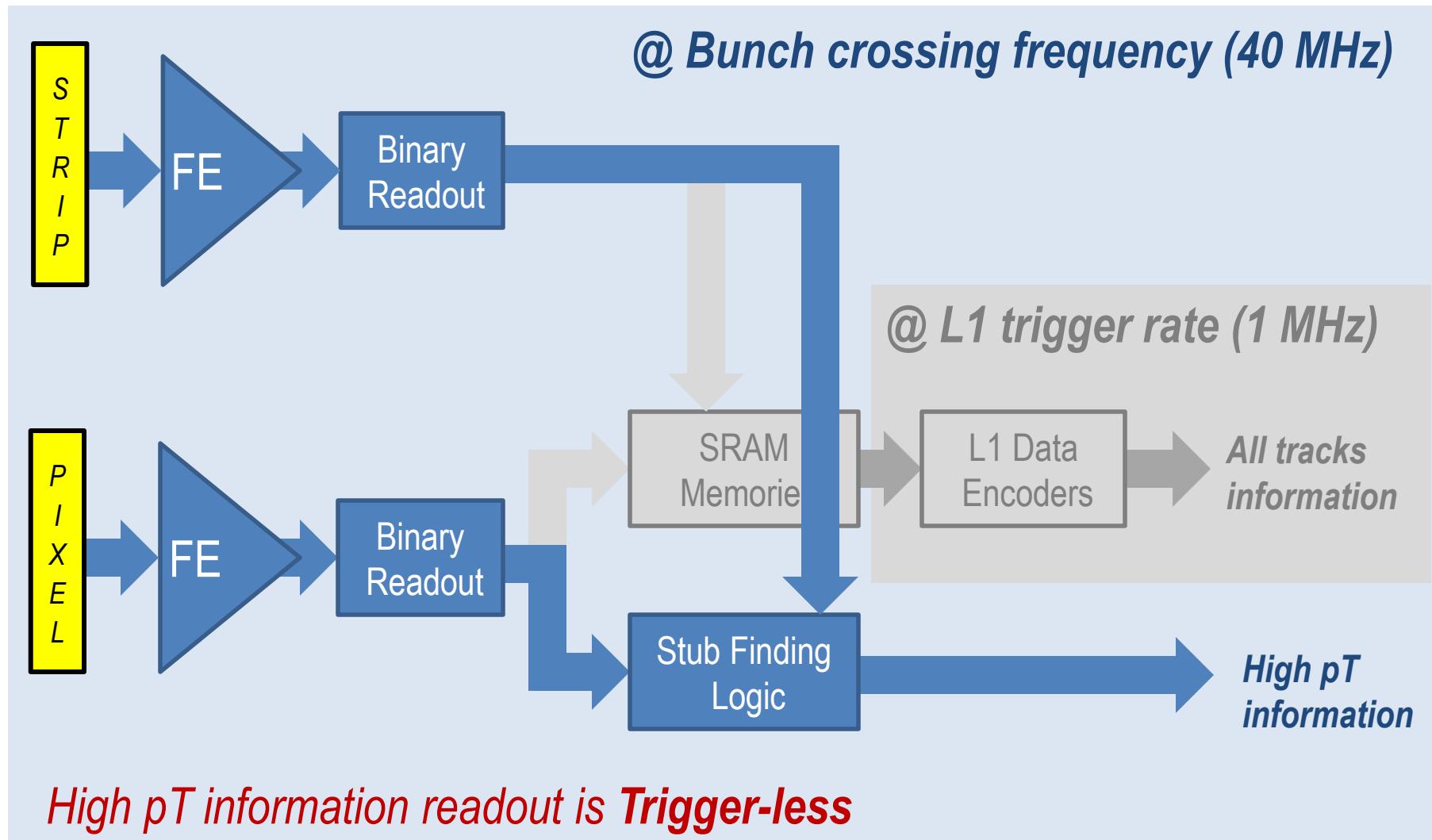
PS module is fully integrate entity

DC-DC converters

ShortStripASIC x 8

Concentrator IC (CIC)
Data aggregation

Strip Layer

MacroPixelASIC x 16

Pixelated Layer

LP-GBT and VTRx+
Data transmission through the optical link
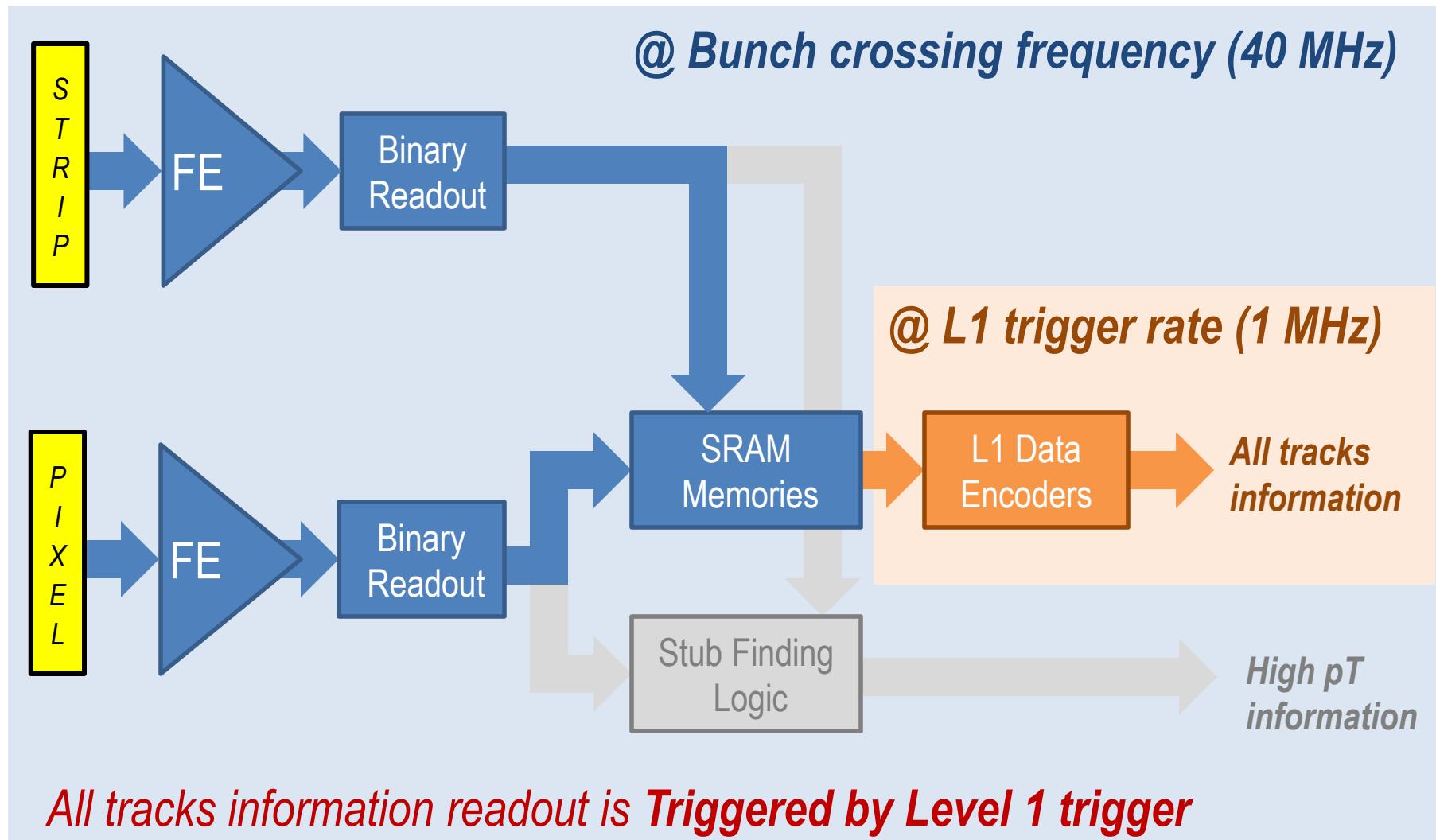
Data Readout block diagram of SSA + MPA

Data Readout block diagram of SSA + MPA

@ *Bunch crossing frequency (40 MHz)*

@ *L1 trigger rate (1 MHz)*

STRIP

FE

Binary Readout

PIXEL

FE

Binary Readout

SRAM Memorie

L1 Data Encoders

All tracks information

Stub Finding Logic

High pT information

*High pT information readout is **Trigger-less***

Data Readout block diagram of SSA + MPA

@ Bunch crossing frequency (40 MHz)

STRIP → FE → Binary Readout

PIXEL → FE → Binary Readout → SRAM Memories

@ L1 trigger rate (1 MHz)

SRAM Memories → L1 Data Encoders → *All tracks information*

Stub Finding Logic → *High pT information*

*All tracks information readout is **Triggered by Level 1 trigger***

Tracker Back-end data transmission optimization

Data transmission frequency **320 MHz with differential lines**

Tracker Back-end **data transmission**

simulation and studies by S.Viret

TRG size (in bits)	Bend coding	Stub losses (in %)					
		All stubs			Good stubs		
		TOB 1	TOB 2	TOB 3	TOB 1	TOB 2	TOB 3
256	5	15.3	1.9	0.6	19.4	2.2	0.3
	3	12.3	1.3	0.5	15.9	1.4	0.2
	0	7.2	0.7	0.5	9.8	0.7	0.1
288	5	10.7	1.1	0.5	14.2	1.2	0.2
	3	8.2	0.8	0.5	11.1	0.8	
	0	4.6	0.5	0.4	6.3	0.4	
312	5	8.2	0.8	0.5	11.1	0.8	
	3	6.1	0.6	0.5	8.4	0.5	0.1
	0	3.3	0.4	0.4	4.6	0.3	
320	5	7.4	0.7	0.5	10.1	0.7	
	3	5.6	0.5	0.4	7.7	0.5	
	0	3.0	0.4	0.1	4.1	0.3	

	MPA/CBC bend bits	Proportion of PU4T (in%)	Stub losses (in %)	
			Good stubs (pT>2/IP<1)	
			TRG/RAW repartition (in bits)	
			After CONC	
			TIB 1 10G-LEC 768b/128b	TIB 2 LP-LEC 384b/64b
PU140/T2-SB	4/4	10		
	3/3	10	0.2+/-0.4	0.0+/-0.5
PU140/T3-SB	4/4	10		
	3/3	10	0.1+/-0.5	0.0+/-0.5
PU200/T2-SB	4/4	10		
	3/3	10	0.5+/-0.3	0.3+/-0.4
PU200/T3-SB	4/4	10		
	3/3	10	0.2+/-0.4	0.1+/-0.4

Stub transmission to tracker back-end is clearly critical for the first barrel layer

Reduced thanks to: Bend bits reduction Tight Stub threshold **Different LP-GBT transmission mode**

Good stub losses lower than 0.5% in all the tracker at Pile Up 200
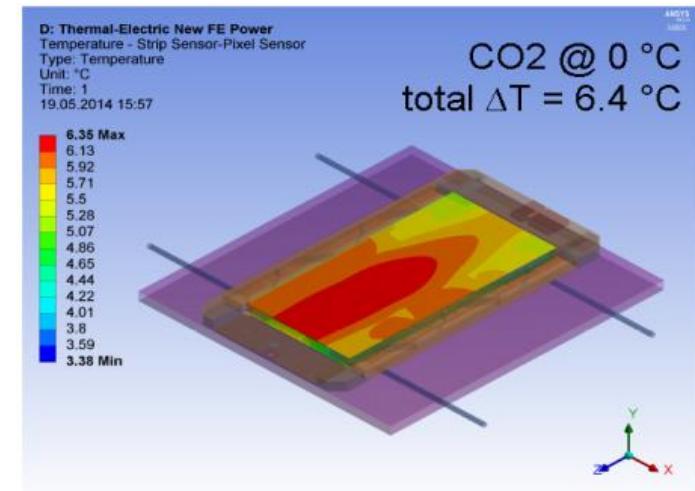
Power budget inside the tracker is *limited*

Total Power Allocated per 16 MPAs and SSAs: *4W*

Total Power Allocated per MPA + SSA: *250 mW*
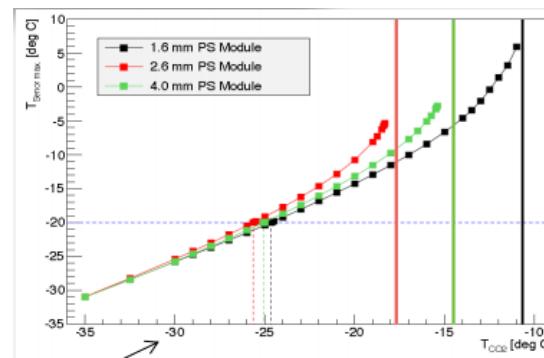
Rough Power Estimation:

Analog	70 mW	
L1 Memory	70 mW	
SSA	40 mW	
Remaining	*70 mW*	

I/O
Clock Distribution
Data Transport
Stub Finding Logic
L1 Data Logic
Output Interface

D: Thermal-Electric New FE Power
Temperature - Strip Sensor-Pixel Sensor
Type: Temperature
Unit: °C
Time: 1
19.05.2014 15:57

CO_2 @ 0 °C
total ΔT = 6.4 °C

6.35 Max
6.13
5.92
5.71
5.5
5.28
5.07
4.86
4.65
4.44
4.22
4.01
3.8
3.59
3.38 Min

PS Module Masses

1.6 mm		2.6 mm		4.0 mm	
AL-C V2-4	2.70	AL-C V2-4	4.39	AL-C V2-4	6.26
CFRP	4.41	CFRP	4.41	CFRP	4.41
Glue	2.17	Glue	2.19	Glue	2.18
Hybrid	1.76	Hybrid	1.82	Hybrid	1.90
Parylene	0.10	Parylene	0.10	Parylene	0.10
Sensors	4.54	Sensors	4.54	Sensors	4.54
Chips	2.70	Chips	2.70	Chips	2.70
GBT/DCDC	0.75	GBT/DCDC	0.75	GBT/DCDC	0.75
	19.13		20.90		22.84

+ 1.75 g → + 1.95 g →

all masses are in grams
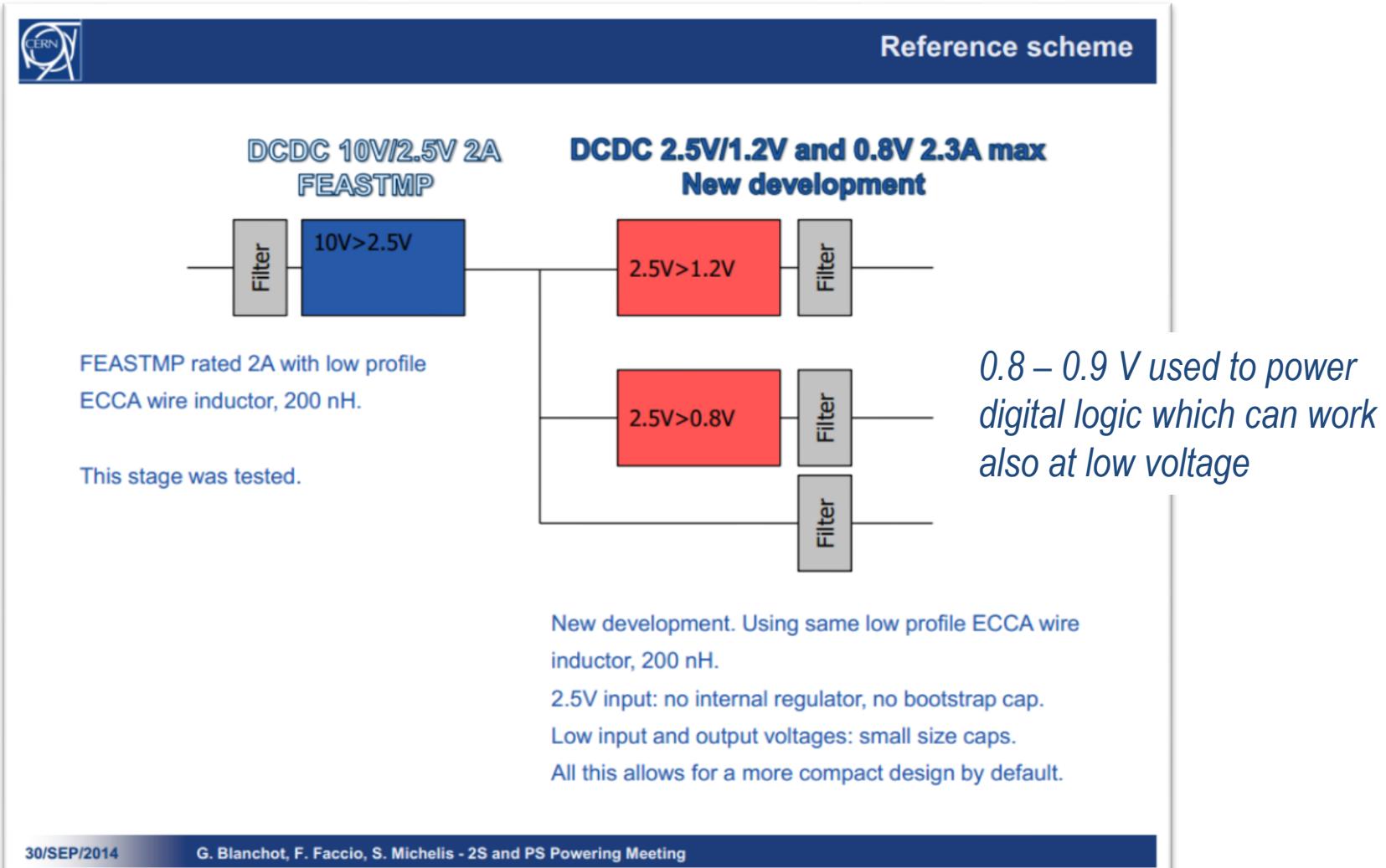
PS module	CO_2 temperature @ working point [°C]	thermal runaway [°C]
1.6 mm	-24.7	-10.8
2.6 mm	-25.6	-17.5
4.0 mm	-25.1	-14.5

Working temperature cooling: ~ -30C

Powering reference scheme

slide and studies from G. Blanchot, F. Faccio and S.Michelis
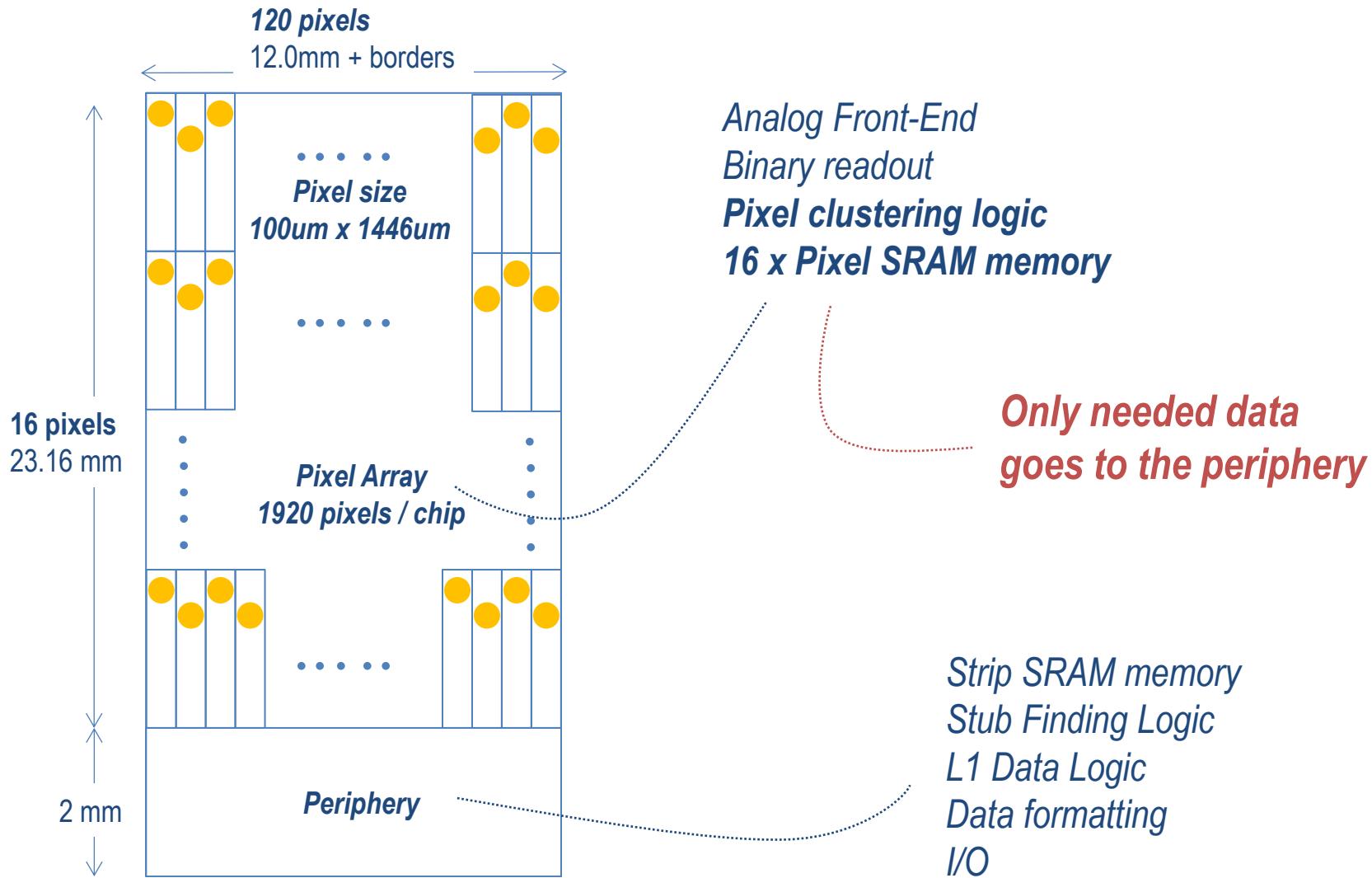
# THE MACRO PIXEL ASIC

The Readout chip for the Pixel-Strip module
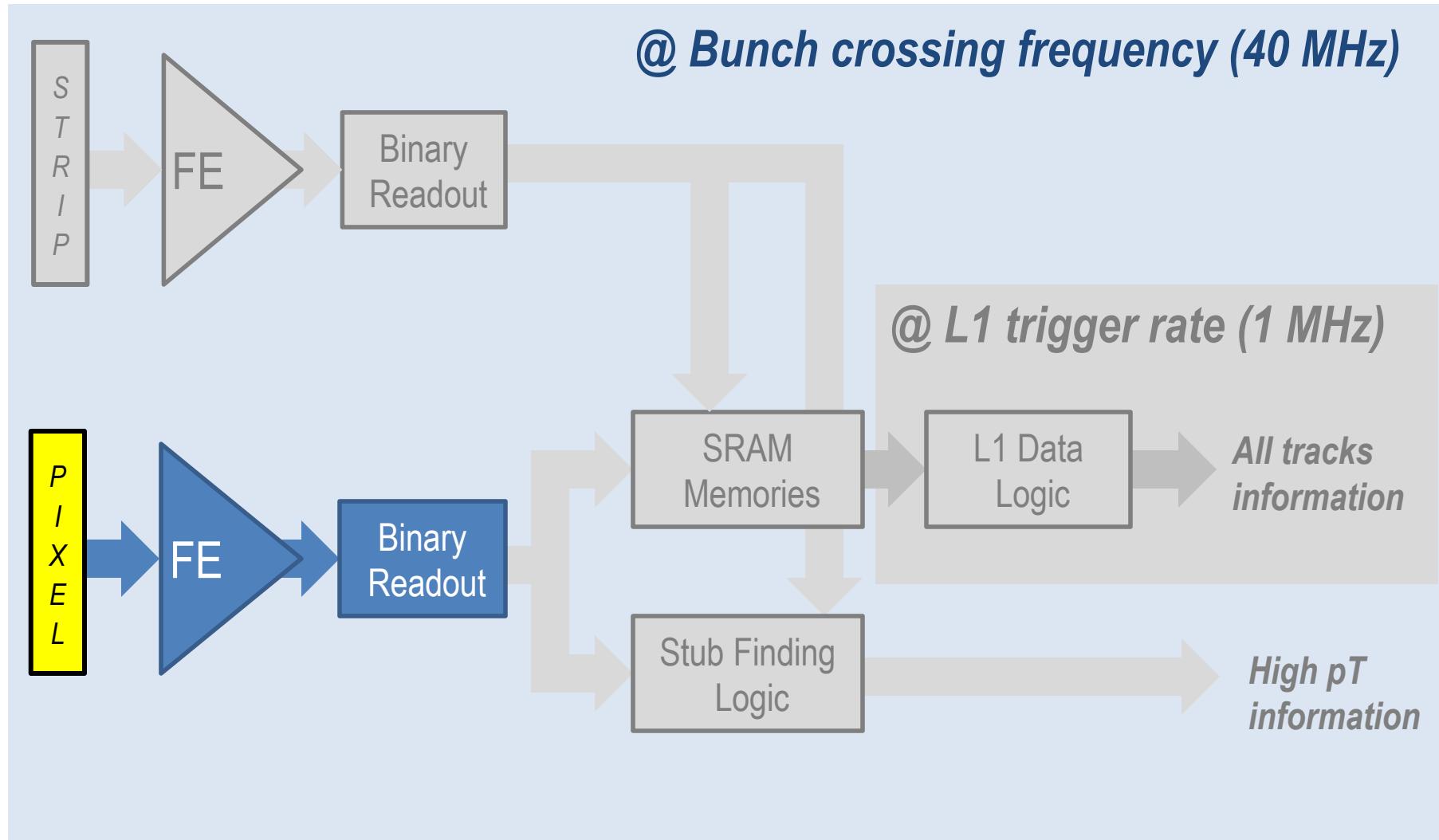
Macro Pixel ASIC specifications

|	
Pixel Arrangement	120 x 16 = 1920 pixels
Macro Pixel Size	100 um x 1446 um
Silicon Detector type	n- on p+ of 200 um (~280 fF), DC coupled
Nominal signal	15000 e-
Technology	65 nm with 8-metals stack
Acquisition Type	Continuous
Acquisition Mode	Binary readout
Data types	1) Encoded cluster position and width 2) Encoded stubs position
Readout types	1) Triggered for full frame 2) Trigger-Less for high-pT information
Data storage	Pixel frame + strip frame for 10 us
Output data port	12 x sLVS @ 320 Mbps
Power budget	220 mW

MacroPixel ASIC **Floorplan**

120 pixels
12.0mm + borders

Pixel size
100um x 1446um

16 pixels
23.16 mm

Pixel Array
1920 pixels / chip

2 mm

Periphery

Analog Front-End
Binary readout
Pixel clustering logic
16 x Pixel SRAM memory

Only needed data
goes to the periphery

Strip SRAM memory
Stub Finding Logic
L1 Data Logic
Data formatting
I/O
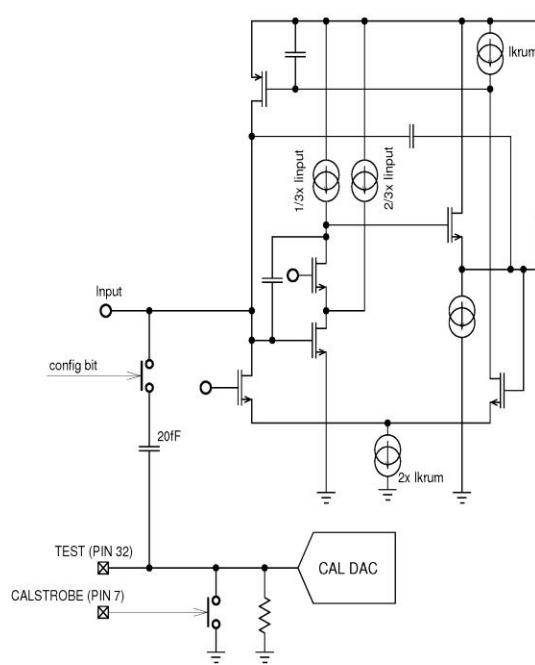
Data Readout block diagram of SSA + MPA

Analog Front-End schematic
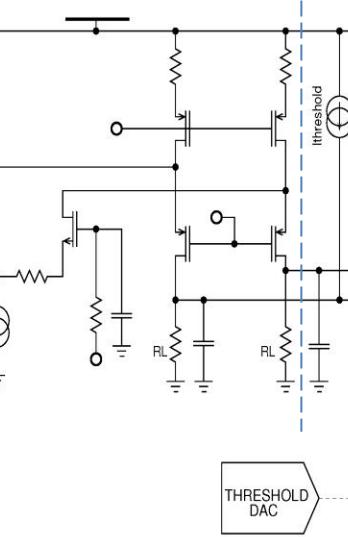
designed by J. Kaplon

Preamplifier · *Shaper* · *Discriminator*
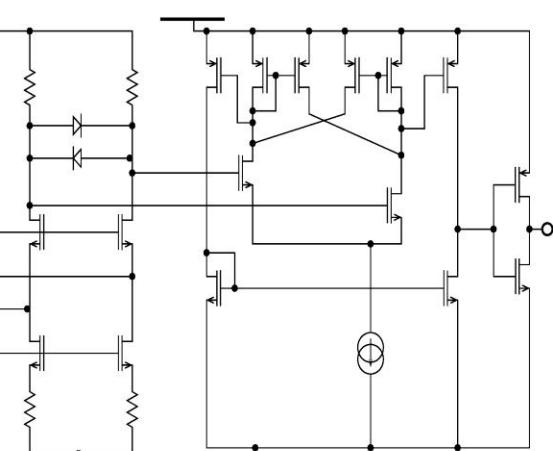
Transimpedance Preamplifier with Krummenacher feedback leakage compensation for n+ on p- detectors

*Single-ended to differential folded cascode stage with resistive load*
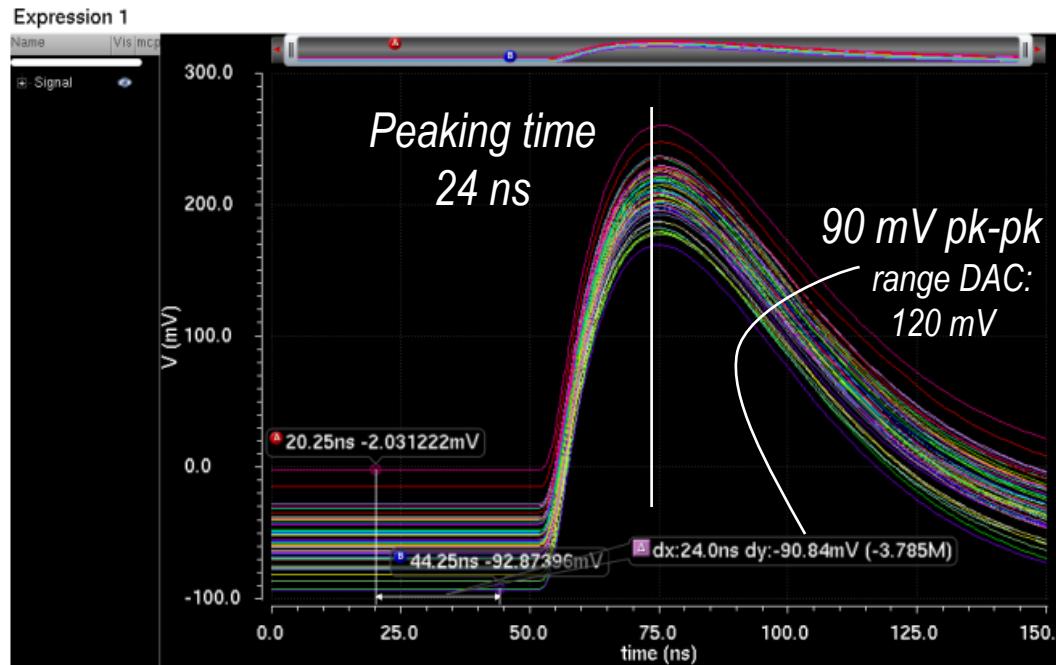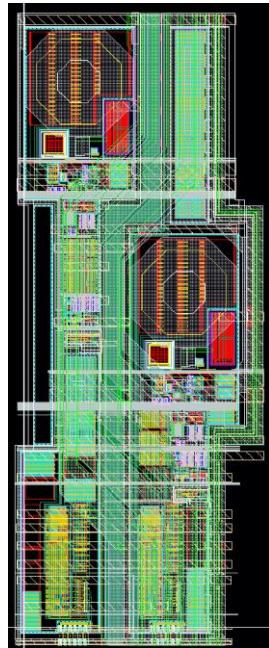
Discriminator with:
- *PMOS folded cascode input*
- *Swing limiter based on PMOS working in diode configuration*
- *Second stage with hysteresis (6mV)*

# Montecarlo simulations 100 runs for 2.5 fC

designed by J. Kaplon

Other simulation results:

|	
Gain from S curves:	85 mV/fC
Time walk :	< 14 ns with threshold at 0.5 fC and signal from 0.75 to 12 fC
PSRR (Worst case):	> 10 dB
Noise(Worst case):	< 200 e- (SNR >> 20)
INL	< 2 %
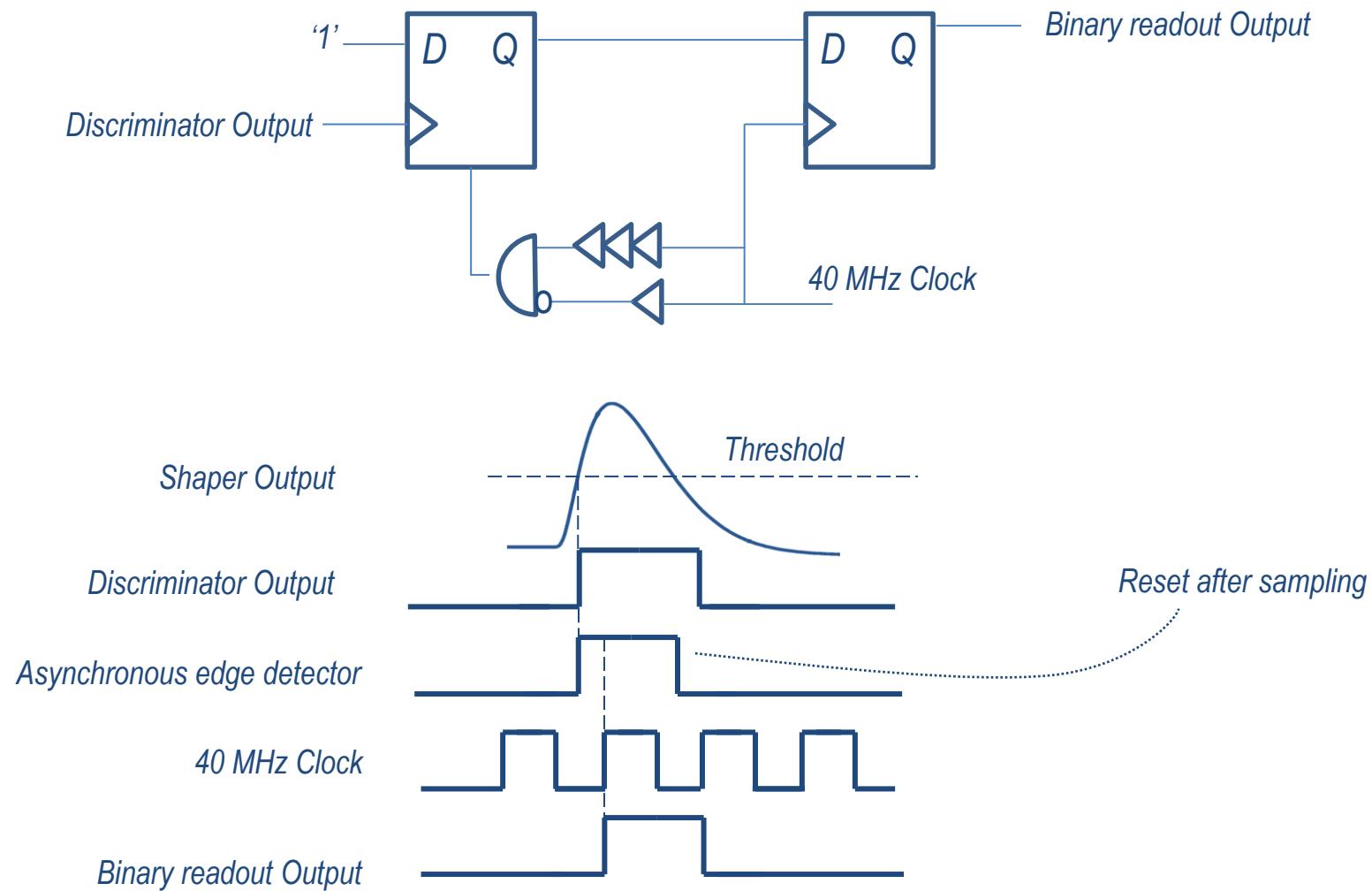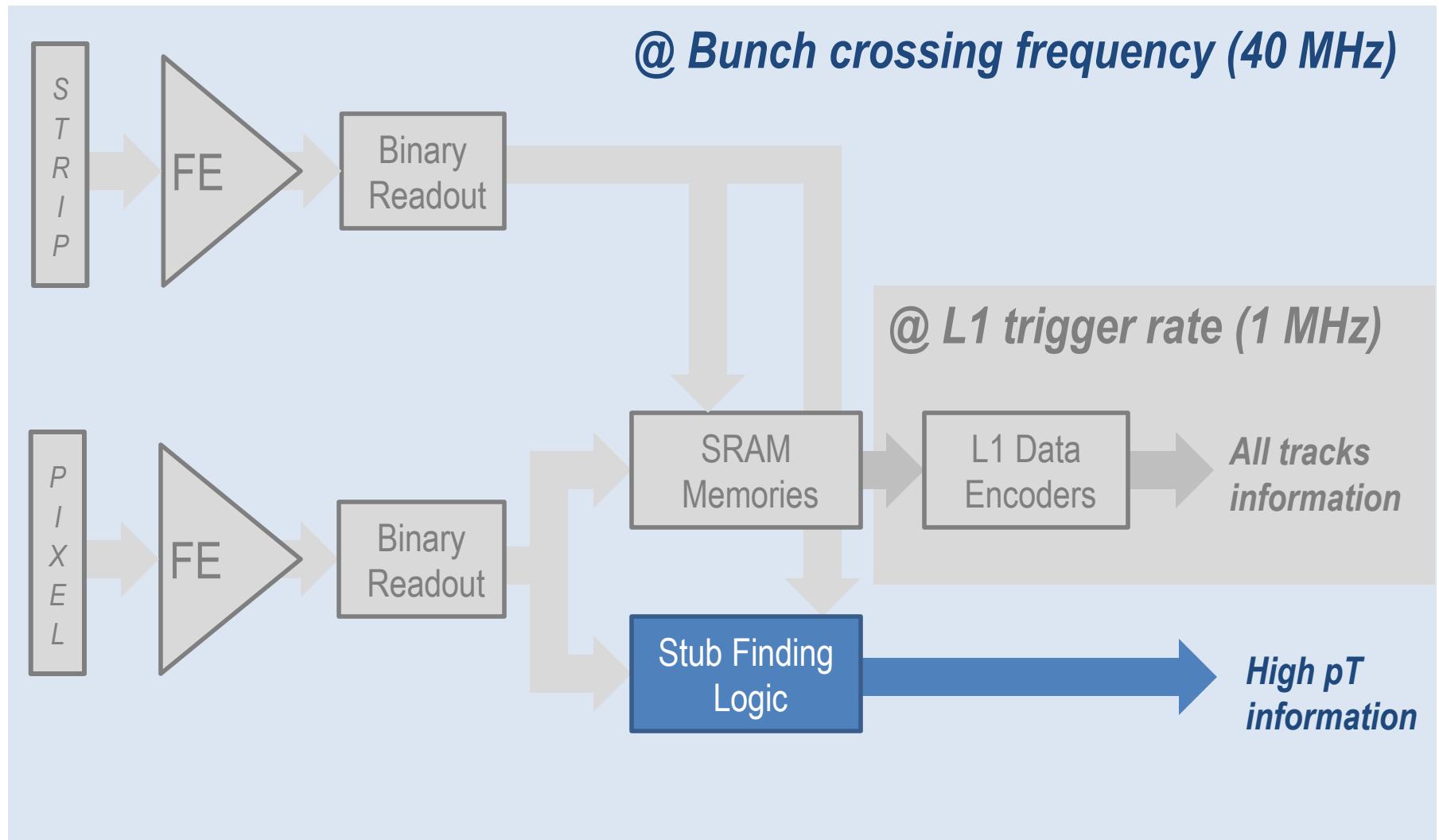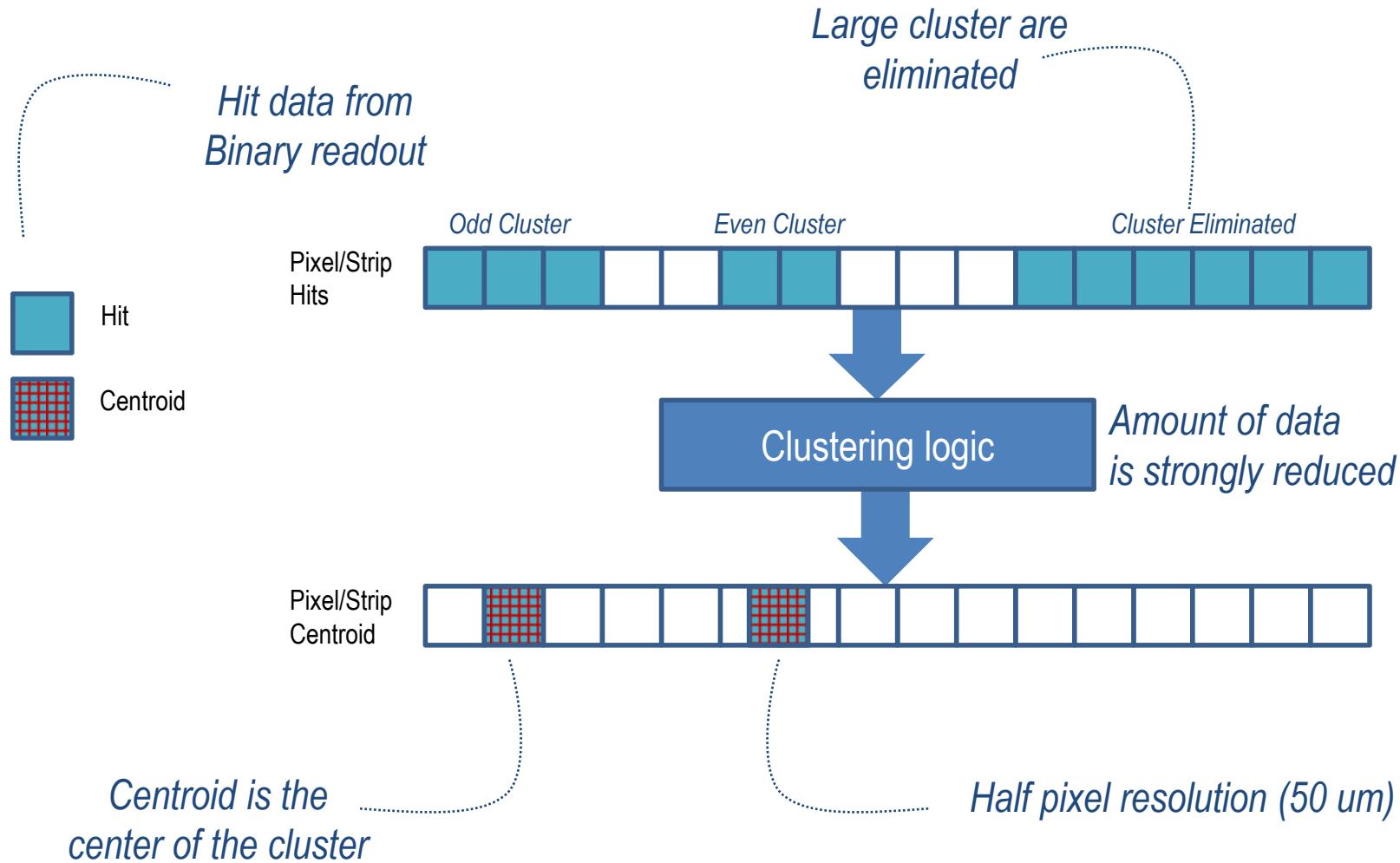
Binary readout system

Data Readout block diagram of SSA + MPA

@ **Bunch crossing frequency (40 MHz)**

@ **L1 trigger rate (1 MHz)**

STRIP → FE → Binary Readout

PIXEL → FE → Binary Readout

SRAM Memories → L1 Data Encoders → *All tracks information*

Stub Finding Logic → *High pT information*
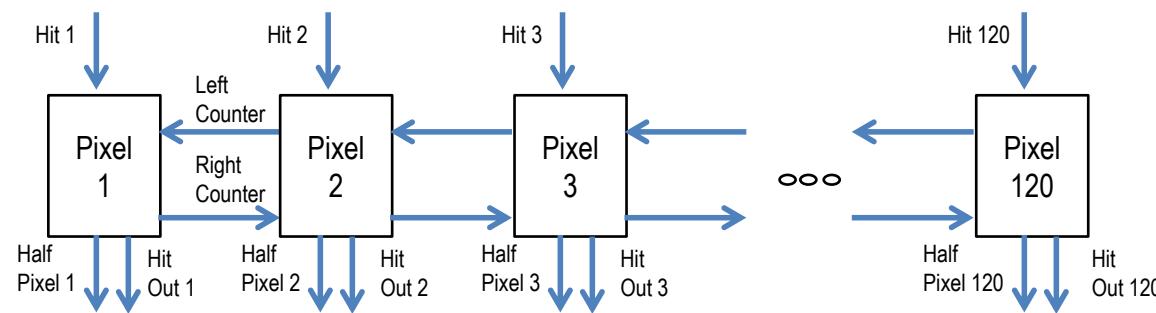
Cluster elimination and centroids extraction

Large cluster are eliminated

Hit data from Binary readout

Odd Cluster   *Even Cluster*   *Cluster Eliminated*

Pixel/Strip Hits

Hit

Centroid

Clustering logic

Amount of data is strongly reduced

Pixel/Strip Centroid

Centroid is the center of the cluster

Half pixel resolution (50 um)

Row Pixel Clustering

Avoids OR-ing of pixel columns → Higher efficiency

	Hit 1		Hit 2		Hit 3		Hit 120

Pixel 1 — Left Counter / Right Counter — Pixel 2 — Pixel 3 — ∘∘∘ — Pixel 120

Half Pixel 1 / Hit Out 1
Half Pixel 2 / Hit Out 2
Half Pixel 3 / Hit Out 3
Half Pixel 120 / Hit Out 120
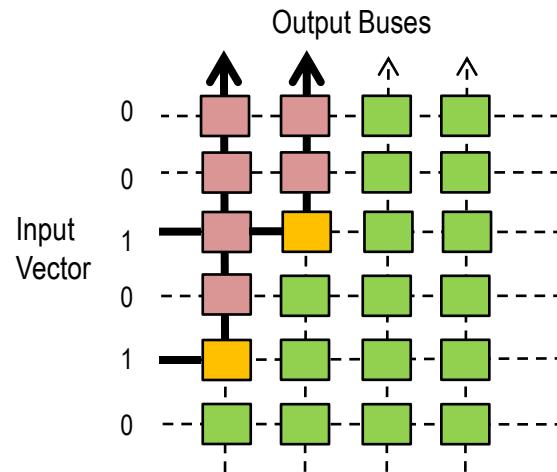
Input:	0	*1*	0	*1*	*1*	*1*	*1*	*1*	0	*1*	*1*	0	*1*	*1*	*1*	0	*1*	*1*	*1*	*1*	0
Count R:	0	1	0	1	2	3	4	5	0	1	2	0	1	2	3	0	1	2	3	4	0
Count L:	0	1	0	5	4	3	2	1	0	2	1	0	3	2	1	0	4	3	2	1	0
Centroid:	0	*1*	0	0	0	0	0	0	0	*1*	0	0	*1*	0	0	0	*1*	0	0	0	
Half Pixel:	0	0	0	0	0	0	0	0	0	*1*	0	0	0	0	0	0	*1*	0	0	0	

Large cluster are eliminated locally

Centroid position encoding is the second step

Output Buses

Input Vector

(a) SCAN   (b) BACKPROPAGATION

Priority Encoder:
Encodes up to 6 coordinate/ 25ns of a 128 bits vector.
Used for:

   Strip centroid position
       Pixel centroid row position
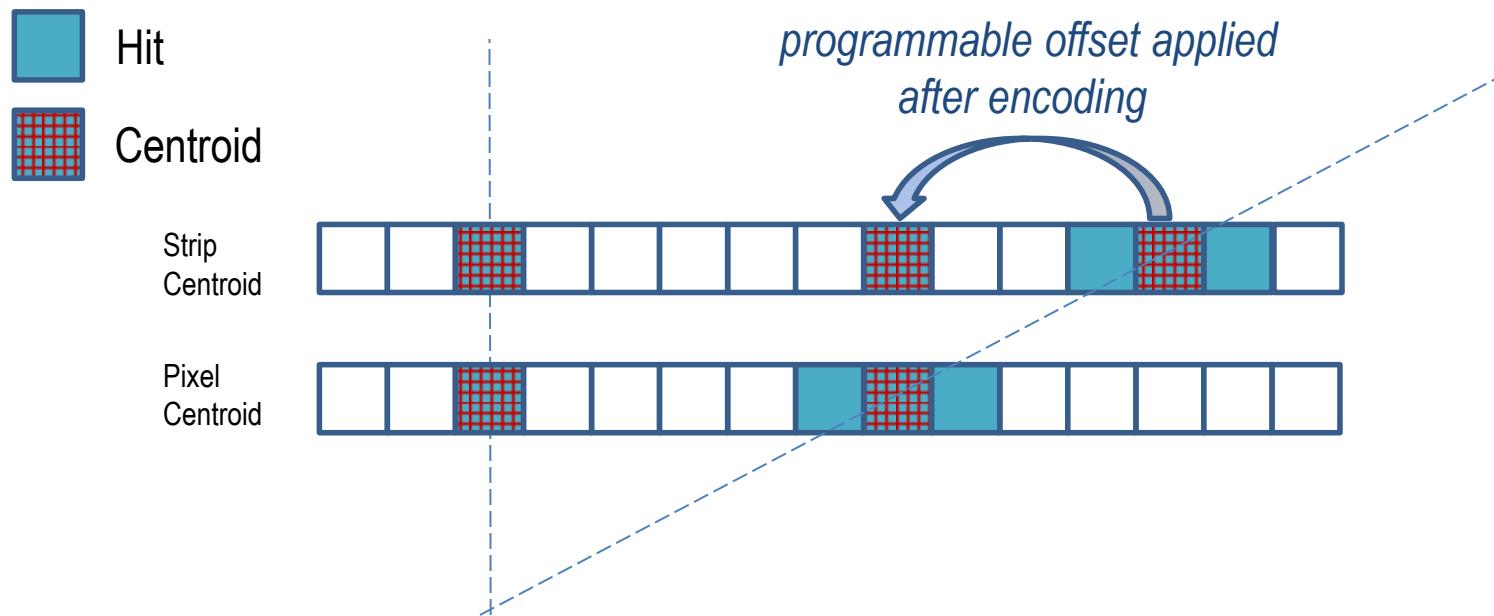
Mephisto Encoder:
Encodes up to 2 coordinate/25ns cycle but low power.
Used for **Pixel centroid column position encoder** (x16 rows)

Parallax correction on encoded positions

Ps module
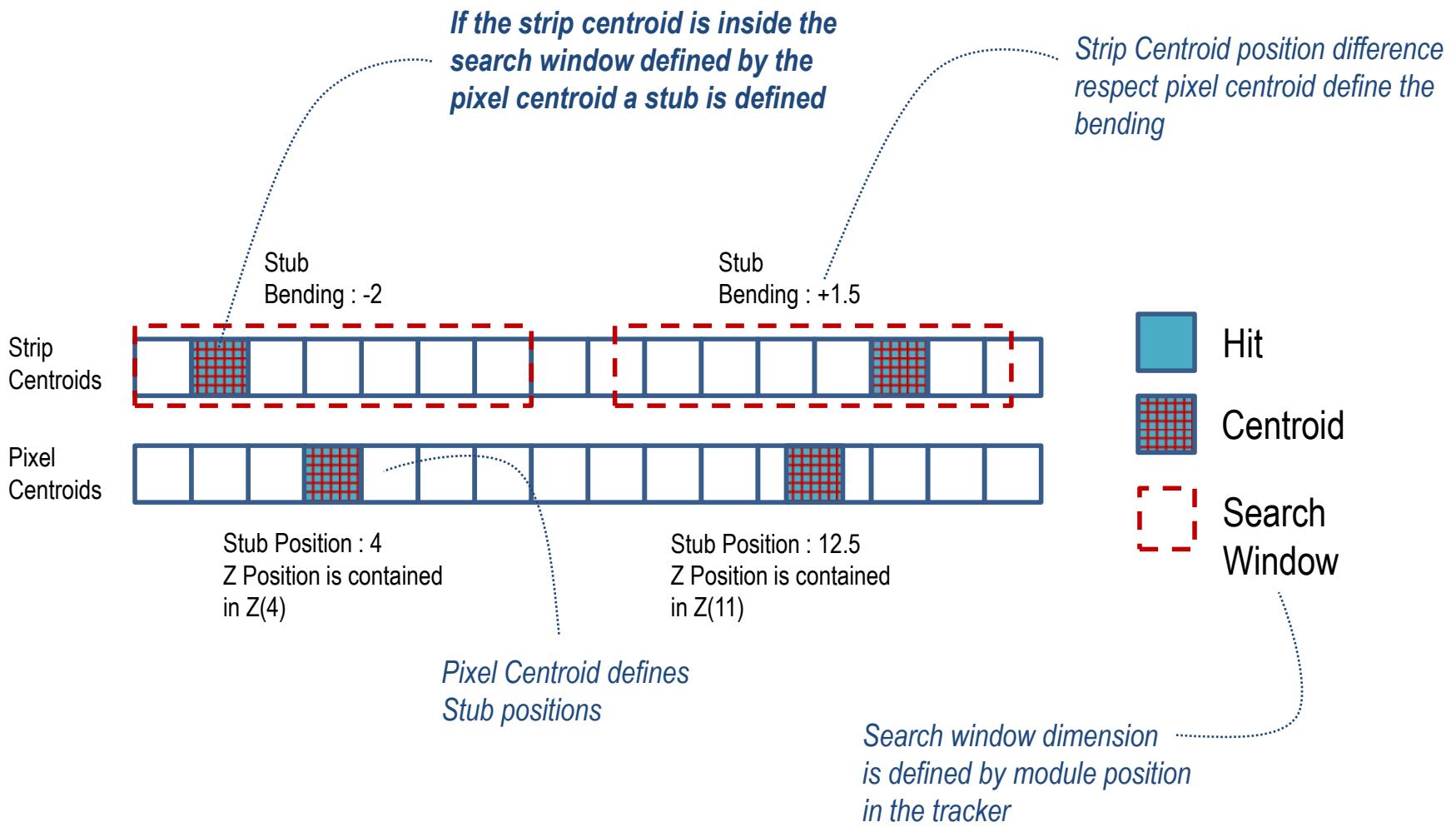
Collision Point

*The shift is needed to compensate the **relative position between the chip and the collision point:***

*Strip parallax correction = **+/- 400 um** with a precision of **+/- 50 um***

Hit

Centroid

programmable offset applied after encoding

Strip Centroid

Pixel Centroid

Correlation logic select matching hits

If the strip centroid is inside the search window defined by the pixel centroid a stub is defined

Strip Centroid position difference respect pixel centroid define the bending

Stub
Bending : -2

Stub
Bending : +1.5

Strip
Centroids

Pixel
Centroids

Hit

Centroid

Search
Window

Stub Position : 4
Z Position is contained
in Z(4)

Stub Position : 12.5
Z Position is contained
in Z(11)

*Pixel Centroid defines
Stub positions*

*Search window dimension
is defined by module position
in the tracker*

Correlation logic select matching hits

- Input:
  - Strip Centroid List = 8 elements
  - Pixel Centroid List = 8 elements
  - Search Window = +/- 3 (7 strip around the Pixel Centroid)

- Pseudo-code:

  Difference = Pixel Phi – Strip Phi

  if (|Difference| =< Search window)

  Generate Stub!

  Stub Position = Pixel Phi

  Stub Bending = Difference

  Stub Z = Pixel Z

Pixel Centroid

Strip Centroid

Stub Found

Correlation logic select matching hits
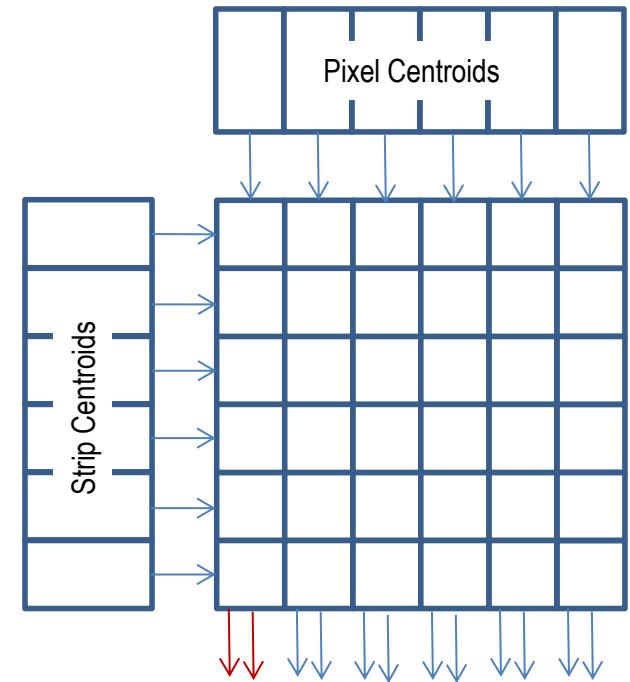
- Input:
  - Strip Centroid List = 8 elements
  - Pixel Centroid List = 8 elements
  - Search Window = +/- 3 (7 strip around the Pixel Centroid)

- Pseudo-code:

  For (Pixel Centroid List)

  For (Strip Centroid List)

  > *Difference = Pixel Phi – Strip Phi*
  >
  > *if (|Difference| =< Search window)*
  >
  > **Generate Stub!**
  >
  > *Stub Position = Pixel Phi*
  >
  > *Stub Bending = Difference*
  >
  > *Stub Z = Pixel Z*

- Loop Unrolling is necessary to implement this code in HW.

Pixel Centroids

Strip Centroids

Limit: 2 stubs for each
Pixel Centroid:
- *Strip/Pixel Centroid = n.*
- *Output Bus = 2n.*
- *ECM Cell = n^2.*
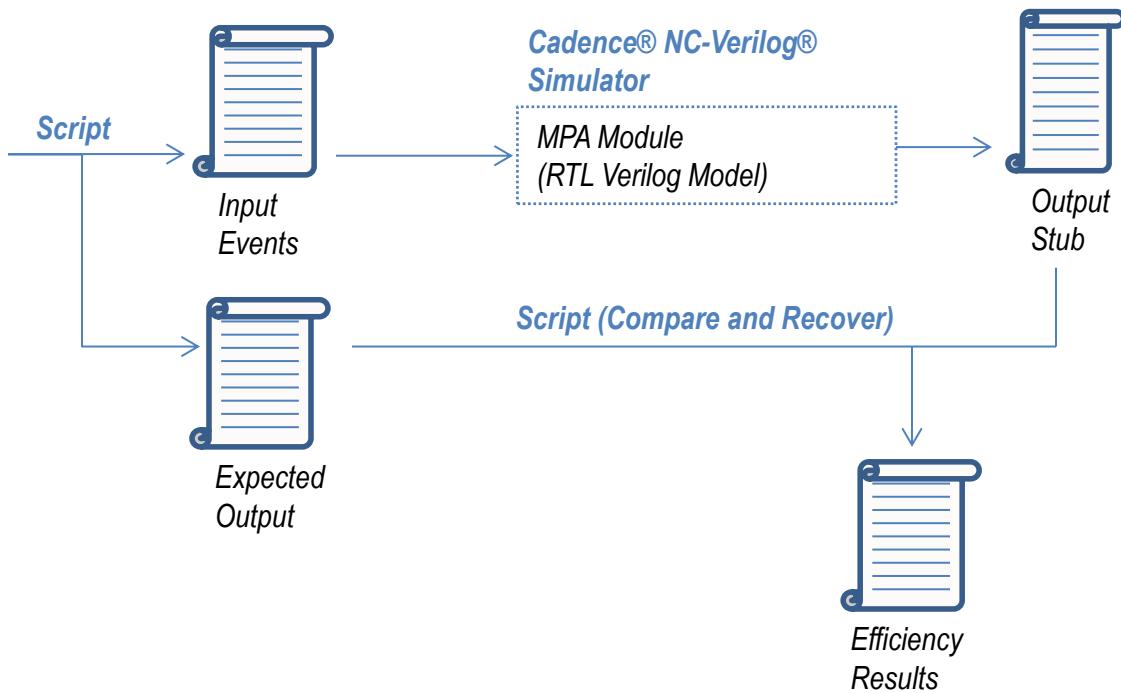
Efficiency using Montecarlo events

Input from Montecarlo generated events are used to calculate and compare the different Stub finding architectures efficiencies.
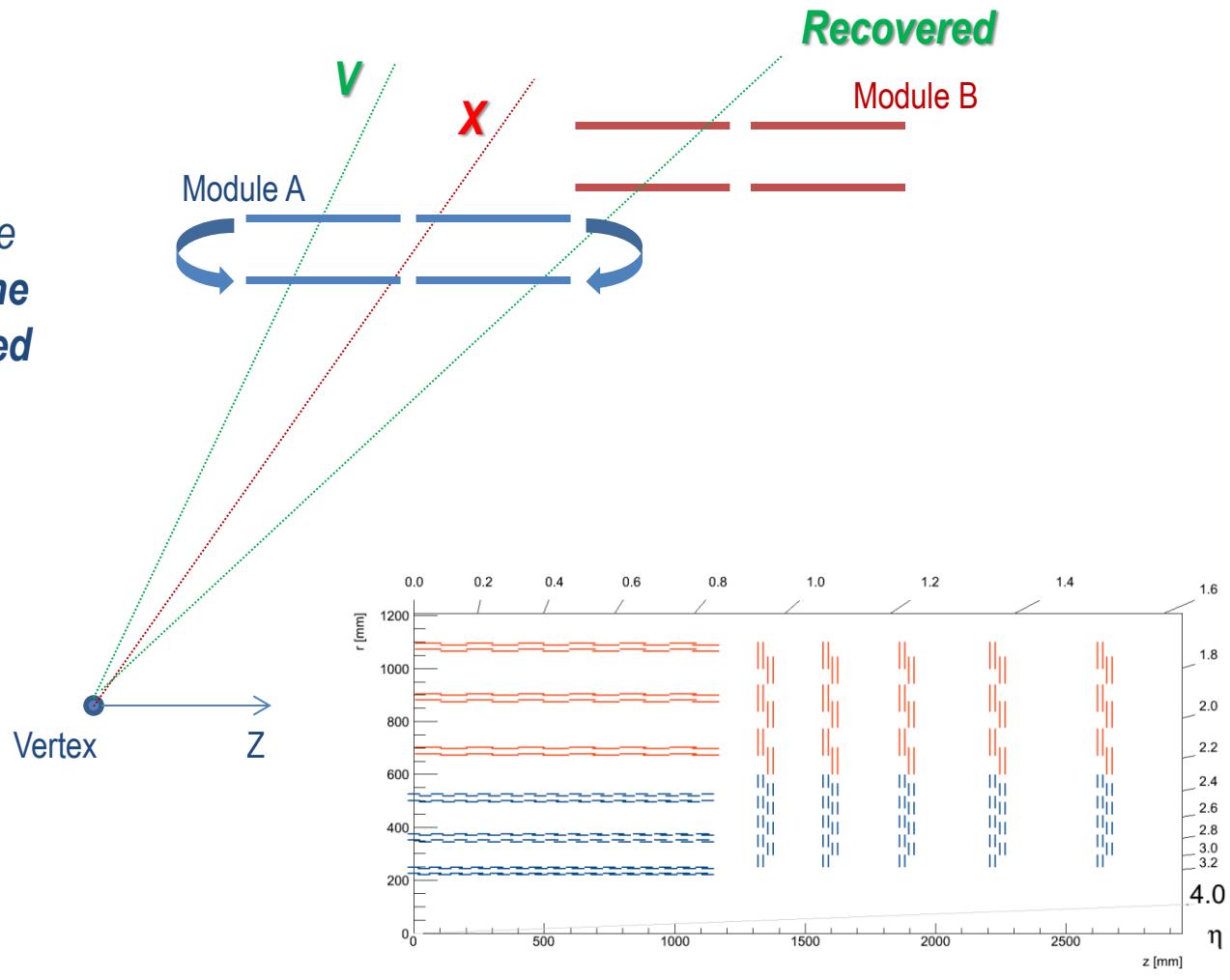
500 Montecarlo Events from S.Viret:

```
##########################################
#
# Event  0
# NPU  = 122

_____
Module 1 1 1
pixeldigi 15 7 // 0 0.06 22.40 // 0.21 22.46 -111.46
pixeldigi 769 30 // 0 0.17 10.06 // -0.13 22.16 -114.78
pixeldigi 770 30 // 0 0.17 10.06 // -0.13 22.16 -114.78
pixeldigi 775 30 // 1 2.17 0.06 // -0.13 22.17 -114.78
pixeldigi 917 3 // 0 0.29 0.00 // -0.20 22.40 -110.88
stripdigi 8 0 // 0 0.06 22.40 // 0.21 22.73 -111.53
stripdigi 79 0 // 0 0.38 57.29 // 0.18 22.59 -111.53
stripdigi 80 0 // 0 0.38 57.29 // 0.18 22.59 -111.53
stub: 15.0 -1.5
…
```

Script

Input Events

Cadence® NC-Verilog® Simulator

MPA Module
(RTL Verilog Model)

Output Stub

Expected Output

Script (Compare and Recover)

Efficiency Results
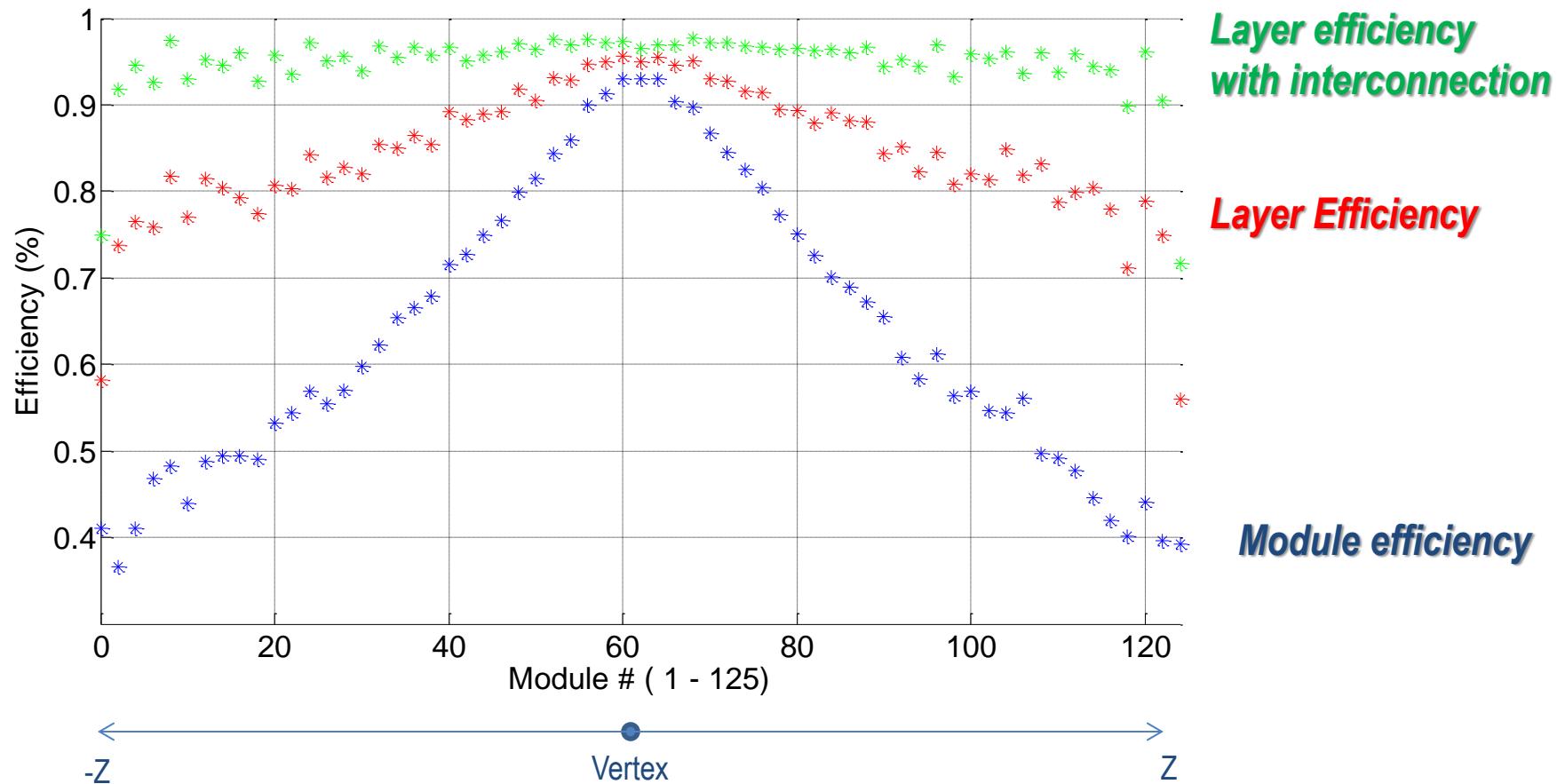
Stub Finding logic efficiency results

*Without an **interconnect technology** (ex: TSV) between the two sides of the module, **tracks crossing the middle will not be identified as stubs***

Recovered

V

X

Module B

Module A

Vertex

Z
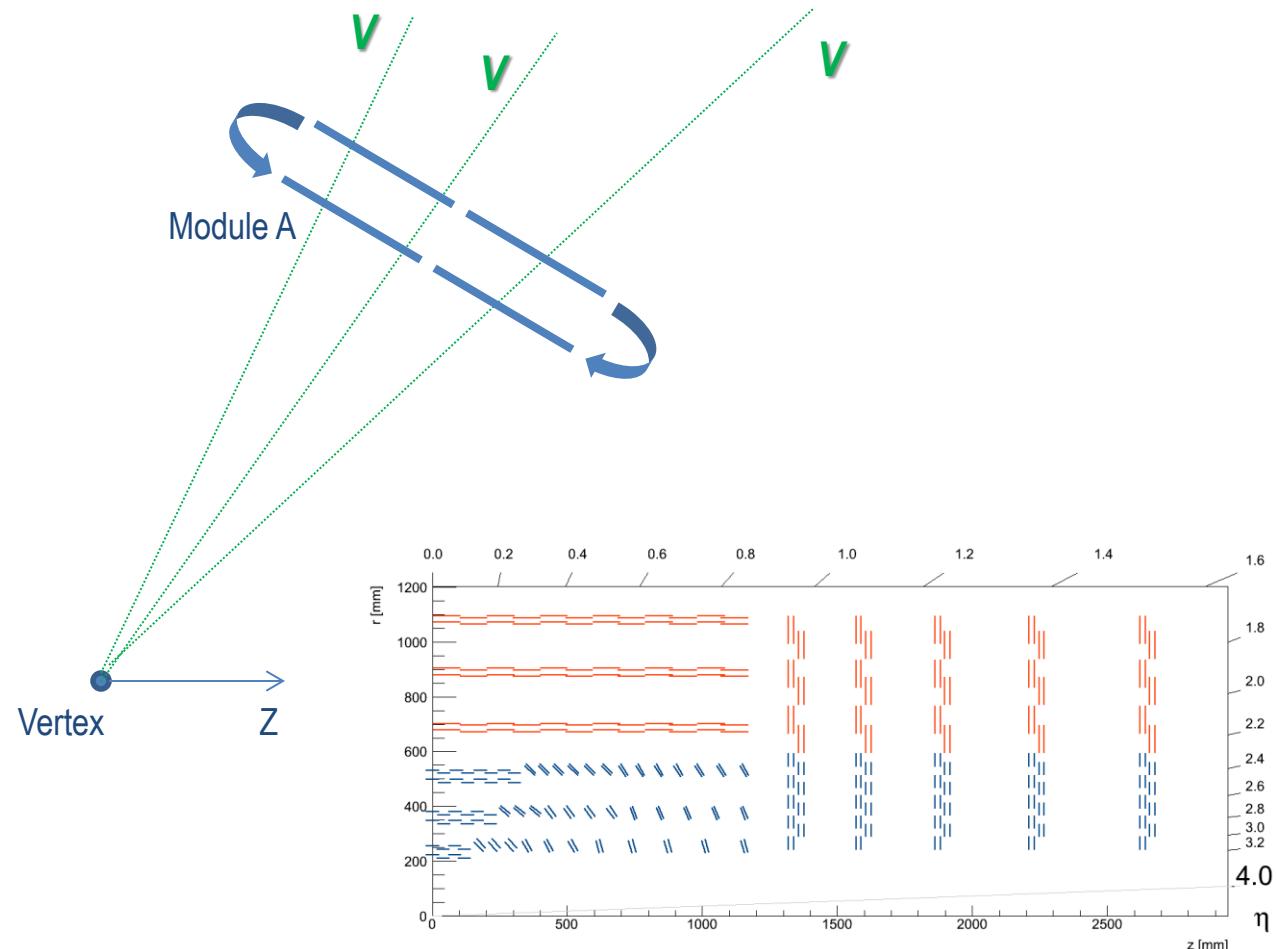
Tracker Layout by G.Bianchi, N.De Maio and S.Mersi

Stub Finding logic efficiency results
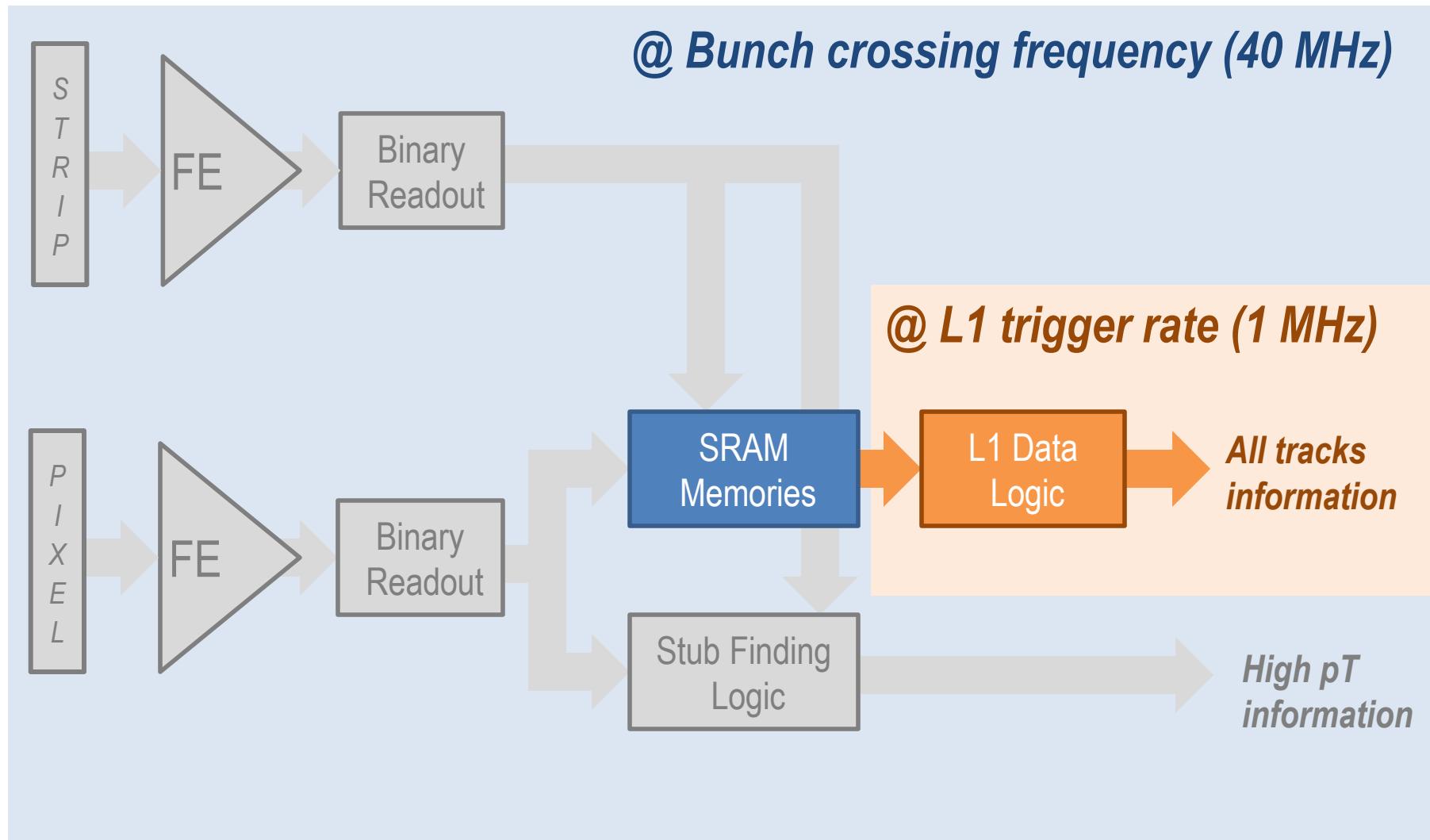
Stub Finding logic efficiency results

Tilted layout solves the problem and decrease the number of modules, but complicates mechanics

V   *V*   *V*

Module A

Vertex   Z

Tracker Layout by G.Bianchi, N.De Maio and S.Mersi

Data Readout block diagram of SSA + MPA

@ *Bunch crossing frequency (40 MHz)*

@ *L1 trigger rate (1 MHz)*

STRIP

FE

Binary Readout

PIXEL

FE

Binary Readout

SRAM Memories

L1 Data Logic

All tracks information

Stub Finding Logic

High pT information

Development of SRAM IP block
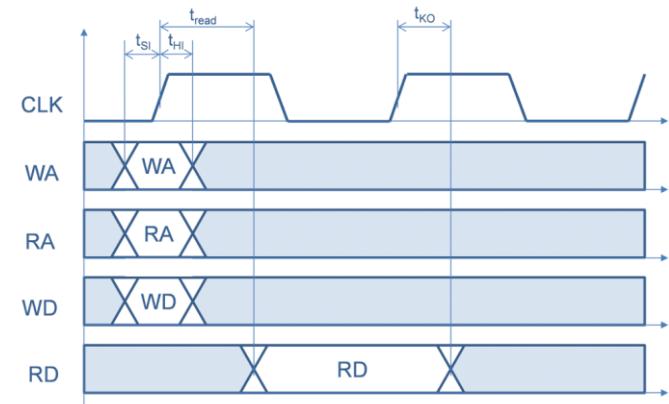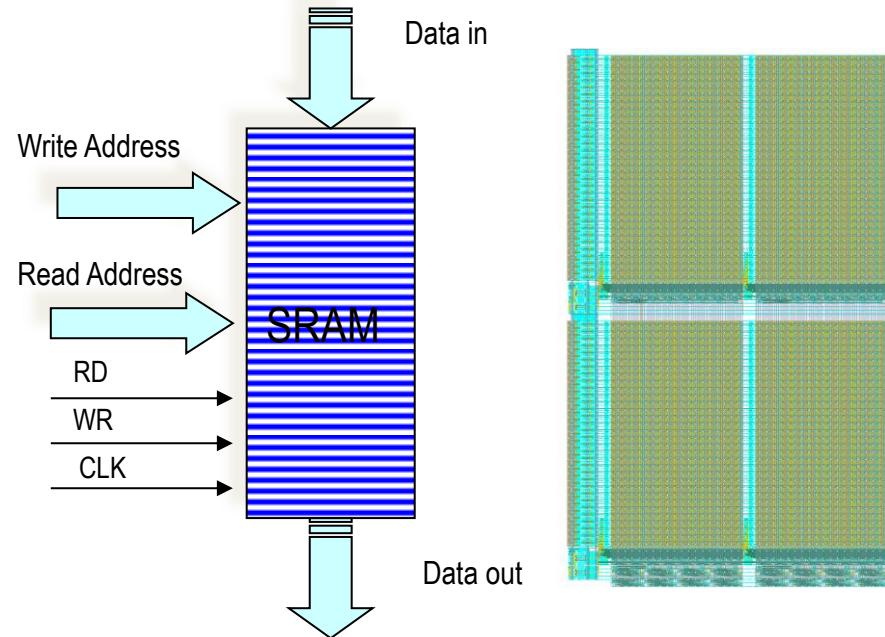
S. Bonacini, I. Kremastotis, K.Kloukinas,

Memory Compiler specifications
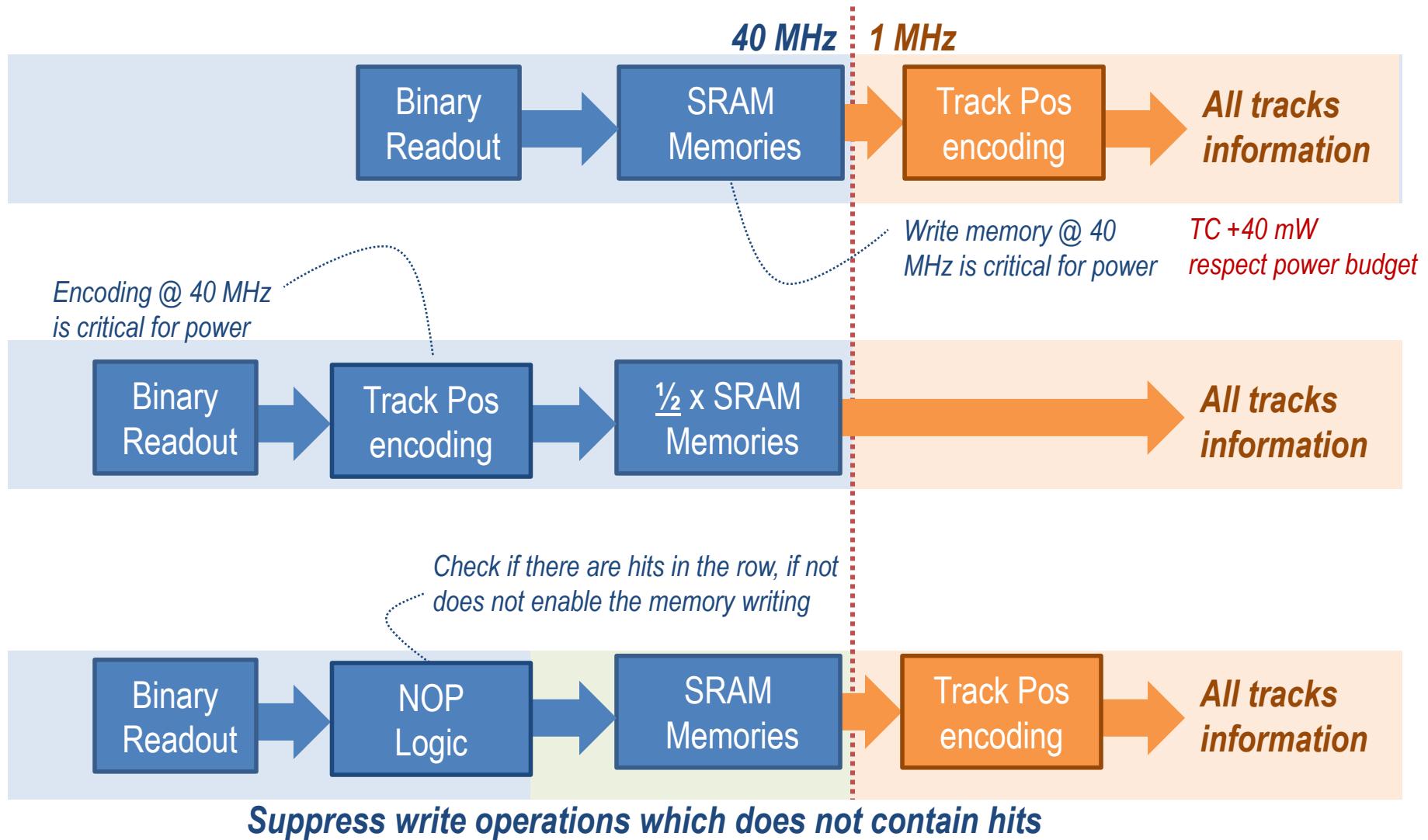
- Clock synchronous, pseudo dual-port memory
  - Write/Read operation @ same clock cycle
- Operating speed: 80 MHz @ 1.2 V
- Compatible with the 65nm CMOS
  - Only lower 4 metal levels used in the SRAM block
  - Only Standard-Vt transistors
  - Special design techniques for *radiation tolerance*
- Memory Compiler specifications:
  - Minimum size: 128 words of 8 bit
  - Max size: 1k words of 256 bits
- Development work is outsourced

MPA Memory specifications:

17 SRAMs of 512 words x 128 bits
power dissipation more than 1/3 of total budget

Data in

Write Address

Read Address

SRAM

RD

WR

CLK

Data out

Different architectures under study for L1 logic

40 MHz | **1 MHz**

Binary Readout → SRAM Memories → Track Pos encoding → *All tracks information*

Write memory @ 40 MHz is critical for power

TC +40 mW respect power budget

Encoding @ 40 MHz is critical for power

Binary Readout → Track Pos encoding → ½ x SRAM Memories → *All tracks information*

Check if there are hits in the row, if not does not enable the memory writing

Binary Readout → NOP Logic → SRAM Memories → Track Pos encoding → *All tracks information*

Suppress write operations which does not contain hits

THE MPA-LIGHT

The Macro Pixel ASIC demonstrator

MPA prototyping requires three ASICs
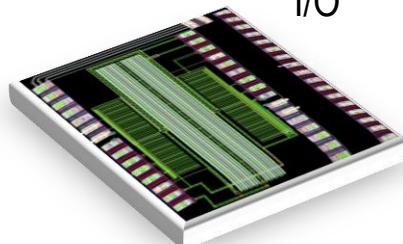
MPA-Light
Analog FE circuitry
Digital Pixel Logic
Stub Finding Logic
Sensor Readout ASIC
MaPSA Assembly
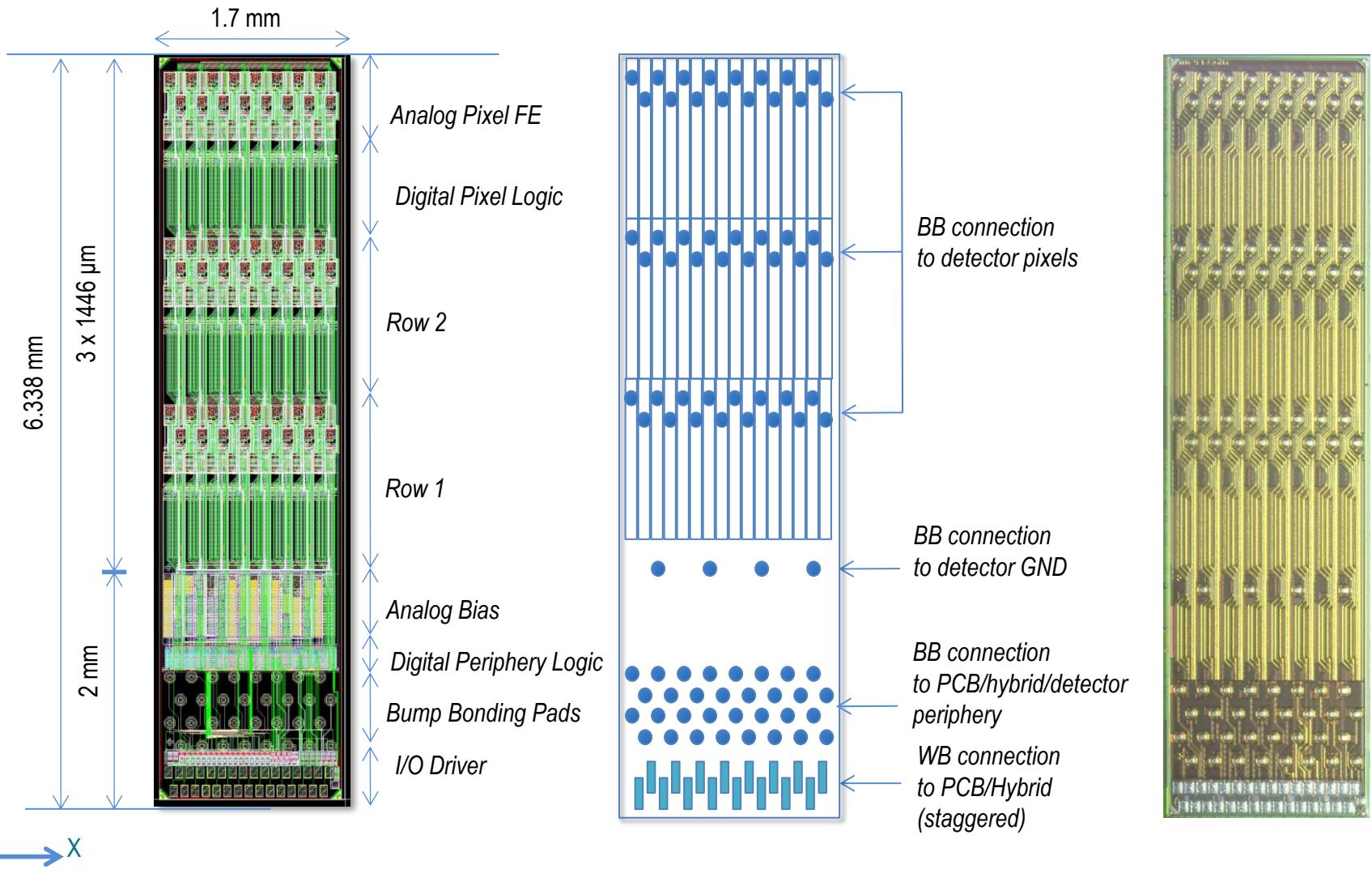
SRAM test
L1 Memory

Clock and SLVS structure
Clock Distribution
I/O
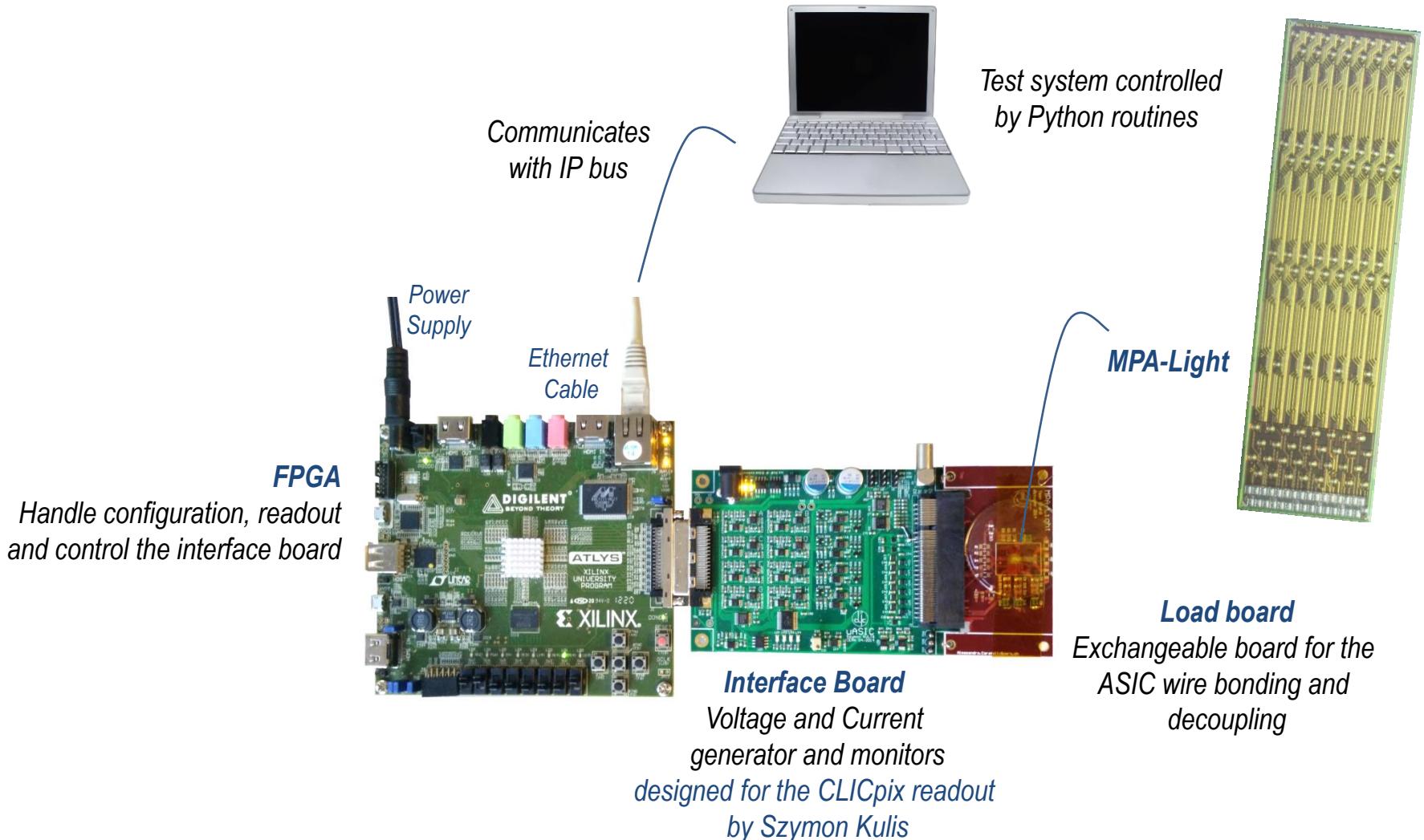
MPA-Light designed by J.Kaplon, D.Ceresa and R. De Olivera
Clock and SLVS structure designed by G.Traversi and L.Gaioni
*SRAM test designed by external company, S.Bonacini and I. Kremastotis*

MPA-Light ASIC floorplan

1.7 mm

6.338 mm

3 x 1446 µm

2 mm

Analog Pixel FE

Digital Pixel Logic

Row 2

Row 1

Analog Bias

Digital Periphery Logic

Bump Bonding Pads

I/O Driver

BB connection
to detector pixels

BB connection
to detector GND

BB connection
to PCB/hybrid/detector
periphery

WB connection
to PCB/Hybrid
(staggered)

z

X
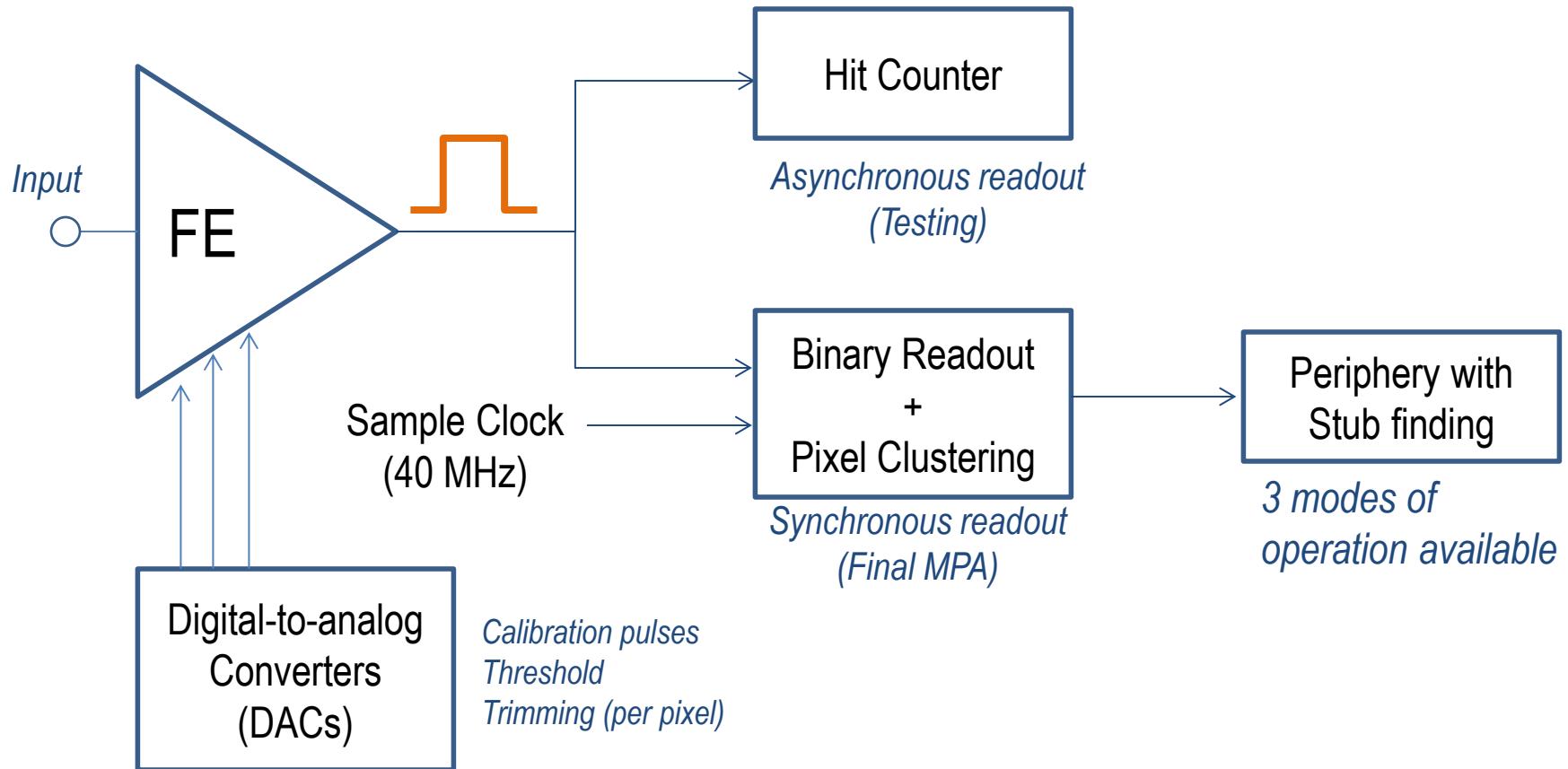
MPA-Light test system overview
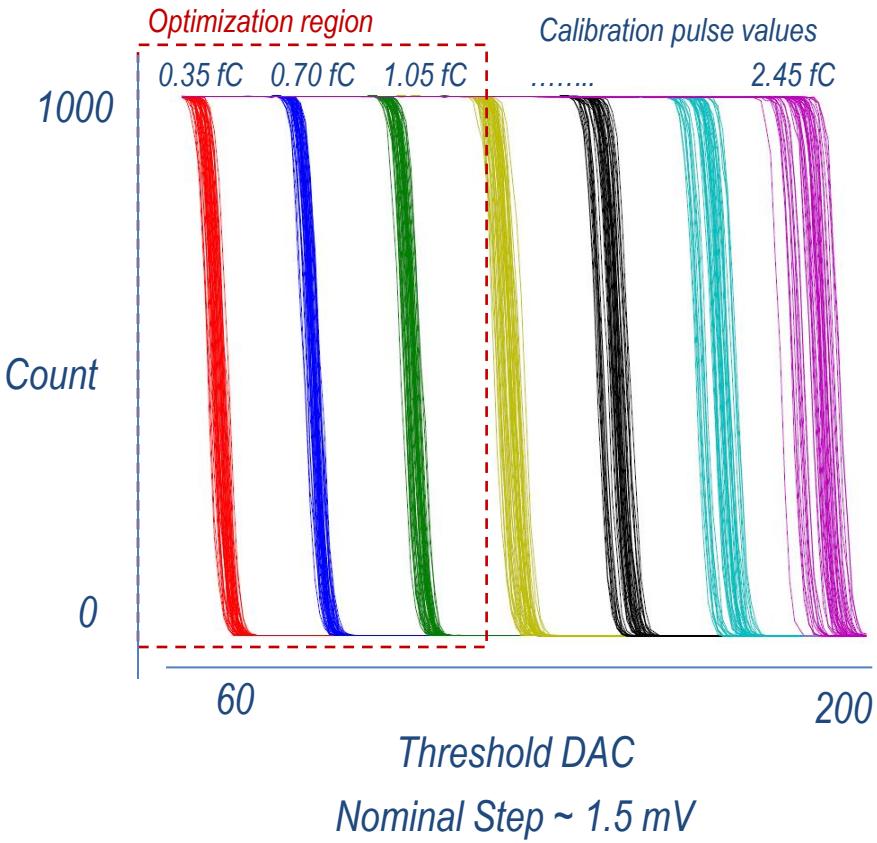
developed by A. Caratelli

Communicates
with IP bus

Test system controlled
by Python routines

Power
Supply

Ethernet
Cable

MPA-Light

FPGA
*Handle configuration, readout
and control the interface board*

Load board
*Exchangeable board for the
ASIC wire bonding and
decoupling*

Interface Board
*Voltage and Current
generator and monitors*
*designed for the CLICpix readout
by Szymon Kulis*

Synchronous and Asynchronous acquisition are available
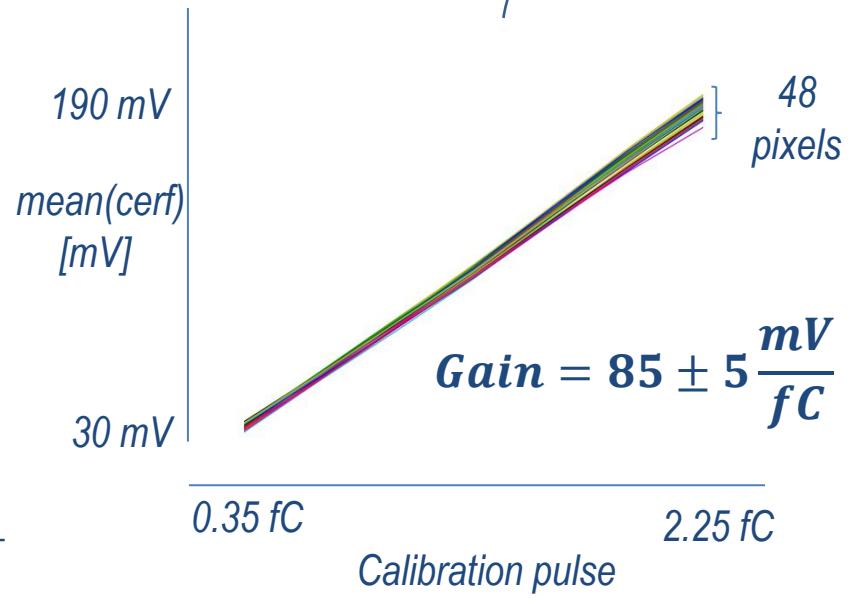
Gain measures confirms specifications

Optimization region

Calibration pulse values

0.35 fC   0.70 fC   1.05 fC

....

2.45 fC

1000

Count

0

60

200

Threshold DAC

Nominal Step ~ 1.5 mV

For every pixel, the gain is extracted with
the complementary error function fitting

190 mV

mean(cerf)
[mV]

30 mV

48
pixels

$Gain = 85 \pm 5 \dfrac{mV}{fC}$

0.35 fC

2.25 fC

Calibration pulse
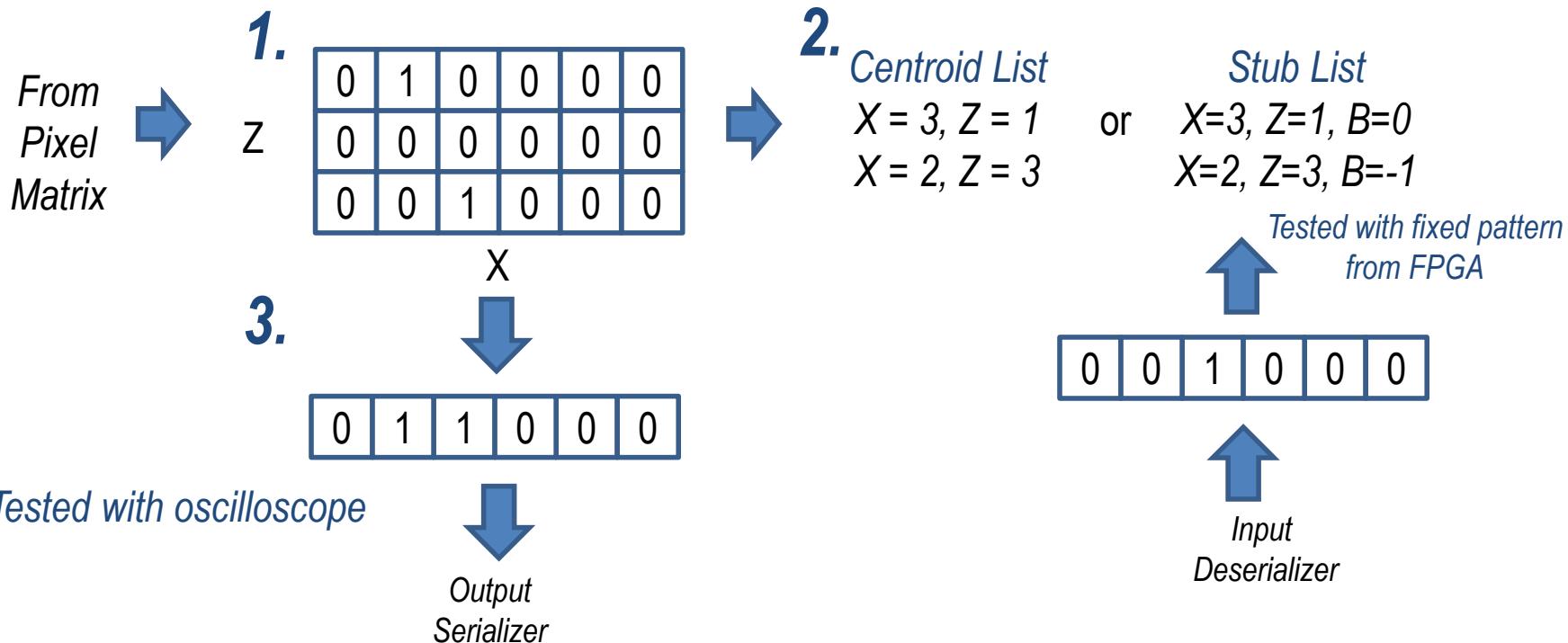
sigma(cerf) = Eq. Noise Charge = $276\ e^- \pm 27 e^-$
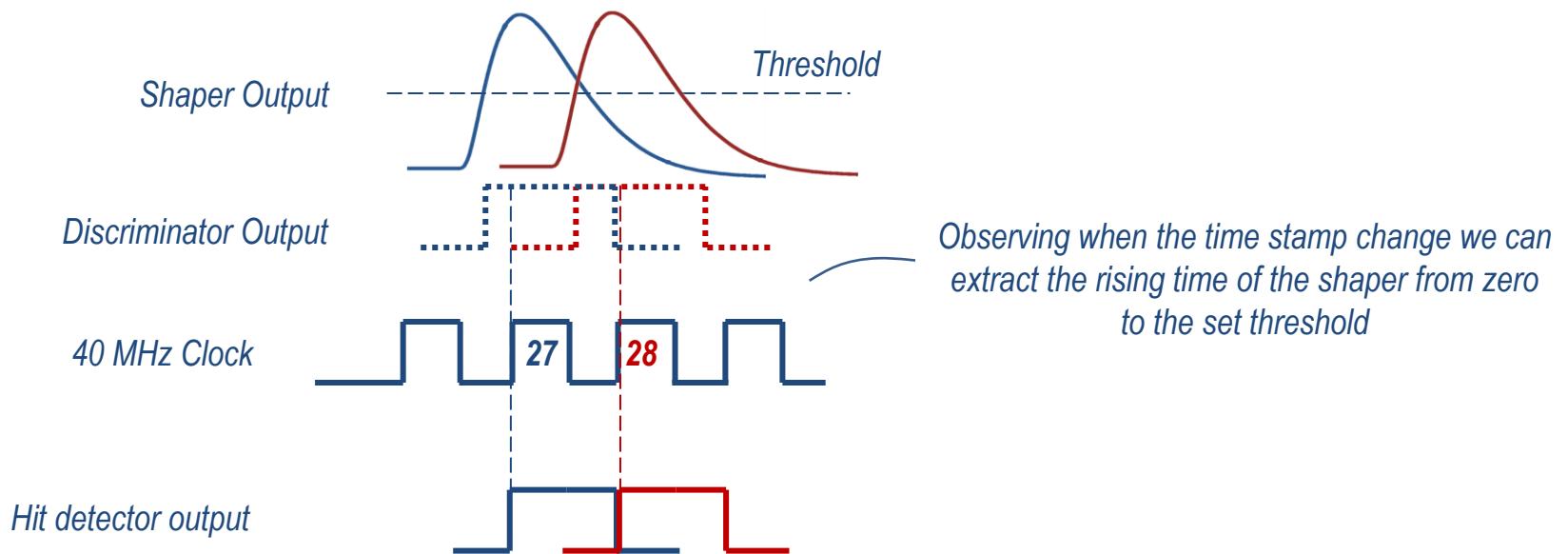
High pT information logic is working

1.

From Pixel Matrix →

Z

0	1	0	0	0	0
0	0	0	0	0	0
0	0	1	0	0	0

X

2.

Centroid List
X = 3, Z = 1
X = 2, Z = 3

or

Stub List
X=3, Z=1, B=0
X=2, Z=3, B=-1

Tested with fixed pattern from FPGA

↑

0	0	1	0	0	0

↑

Input Deserializer

3.

↓

0	1	1	0	0	0

Tested with oscilloscope

↓

Output Serializer

1. No processing → Save in memory all the data from Pixel Matrix
2. With Data Reduction → Generate and save in memory Centroid or Stubs
3. Strip Emulator → OR the Pixel Column and send the data in output
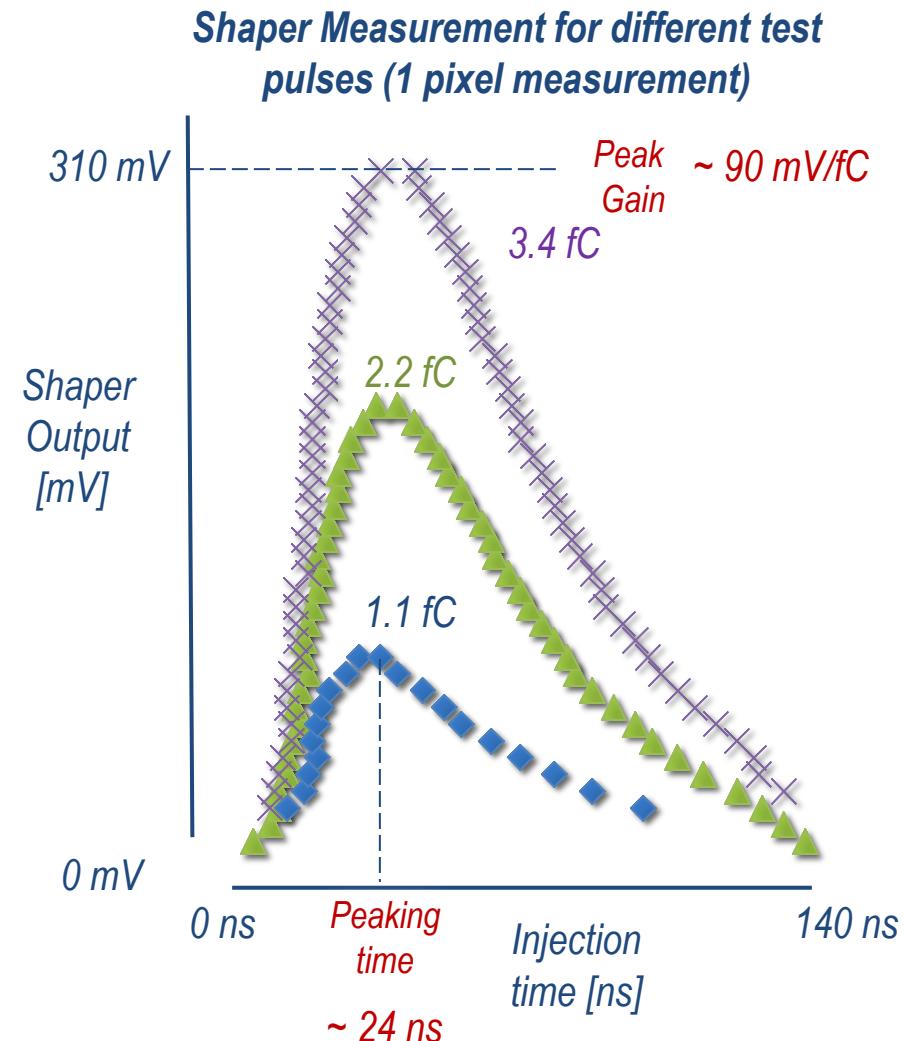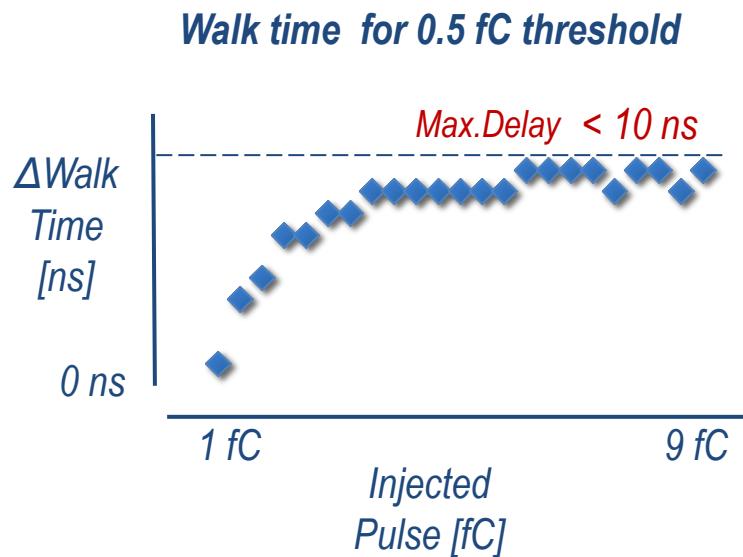
Synchronous readout allows additional FE studies

Changing the calibration injection point and using the synchronous readout we can characterize the shaper of the analog FE

Threshold

Shaper Output

Discriminator Output

Observing when the time stamp change we can extract the rising time of the shaper from zero to the set threshold

40 MHz Clock   27   28

Hit detector output
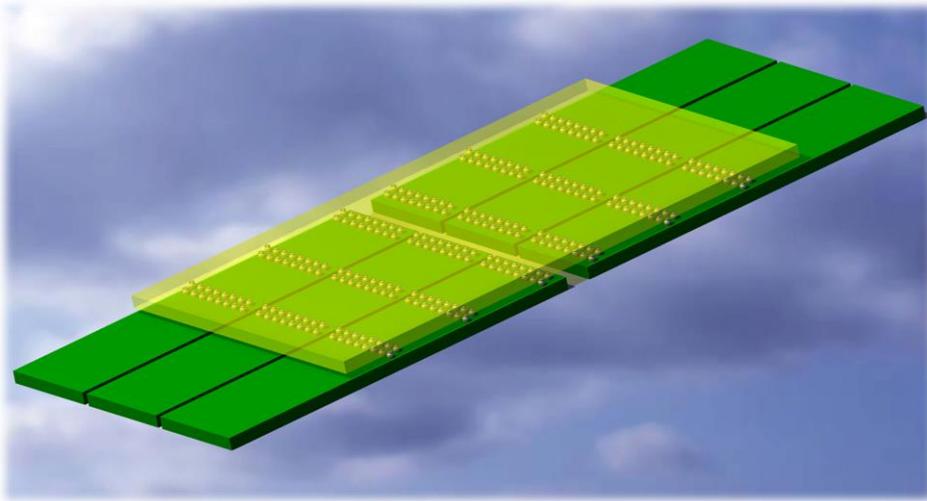
Shaper measurement for different pulses

The measurement allows peaking time, peak gain and walk time measurement which are in agreement with the simulation.

Shaper Measurement for different test pulses (1 pixel measurement)

310 mV — Peak Gain ~ 90 mV/fC

3.4 fC

2.2 fC

1.1 fC

Shaper Output [mV]

0 mV

0 ns — Peaking time ~ 24 ns — Injection time [ns] — 140 ns

Walk time for 0.5 fC threshold

Max.Delay < 10 ns

ΔWalk Time [ns]

0 ns

1 fC — 9 fC

Injected Pulse [fC]
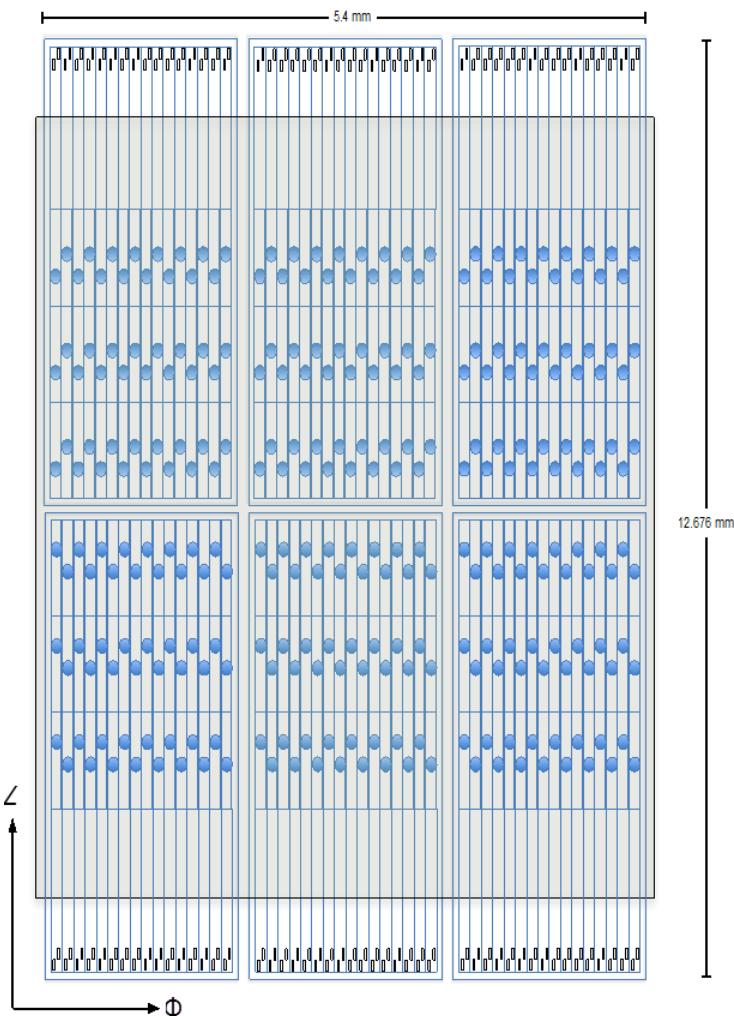
MaPSA-Light = 6 x MPA-Light + Pixel sensor

Design by G.Blanchot, et Al.

- **MA**cro **P**ixel **S**ub **A**ssembly (MAPSA) light

- *Objective is to assemble a module of
  3 x 2 MPA-light chips for a total of 288 pixels*

Conclusions

- ***MPA-Light:***

  - All measurement without sensor indicate that the ASIC is fully functional

  - Assembly with the sensor is foreseen in the next months

    - Sensor Characterization
    - Module assembly first prototype

- ***Full Macro Pixel ASIC project:***

  - Analog performance confirmed in 65 nm technology

  - Macro Pixel ASIC and Short Strip ASIC final development can start

Thanks to all the
CMS TRACKER PHASE II ELECTRONICS TEAM

Davide Ceresa

PH-ESE, CERN
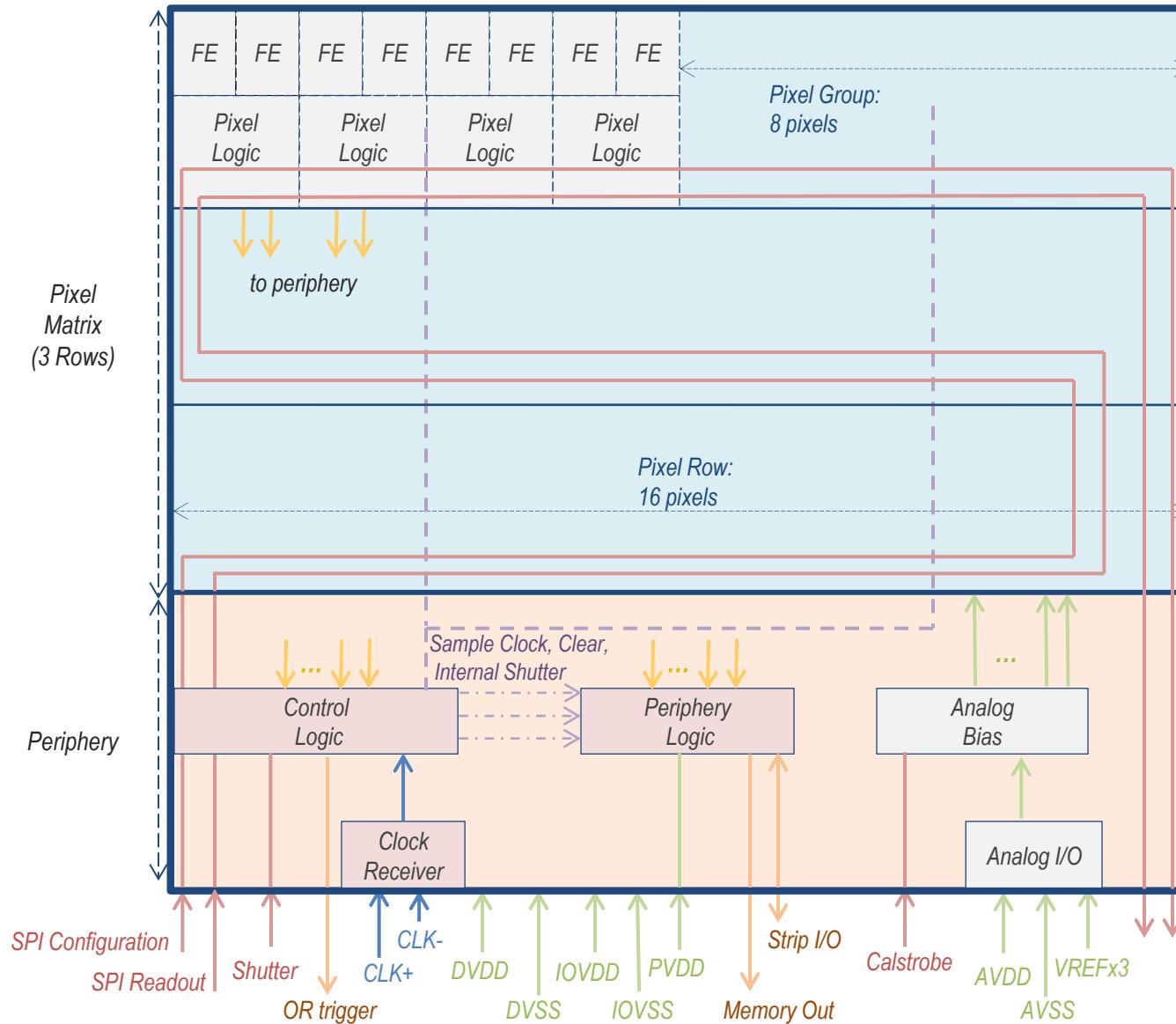
on behalf of the *CMS Tracker Phase II electronics team*

PH-ESE seminar, 10th March, 2015
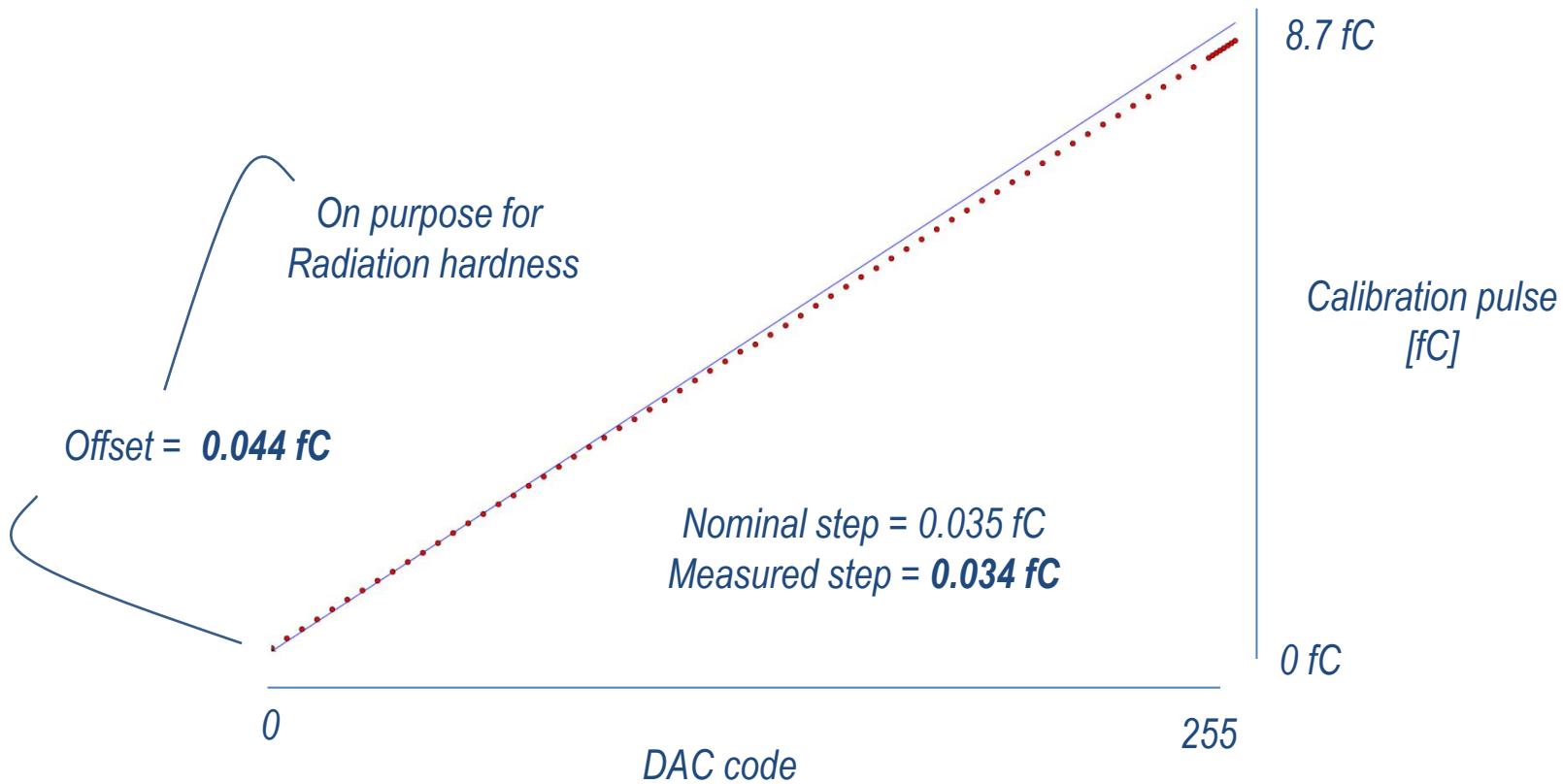
SPARE SLIDES

MPA-Light Building Blocks
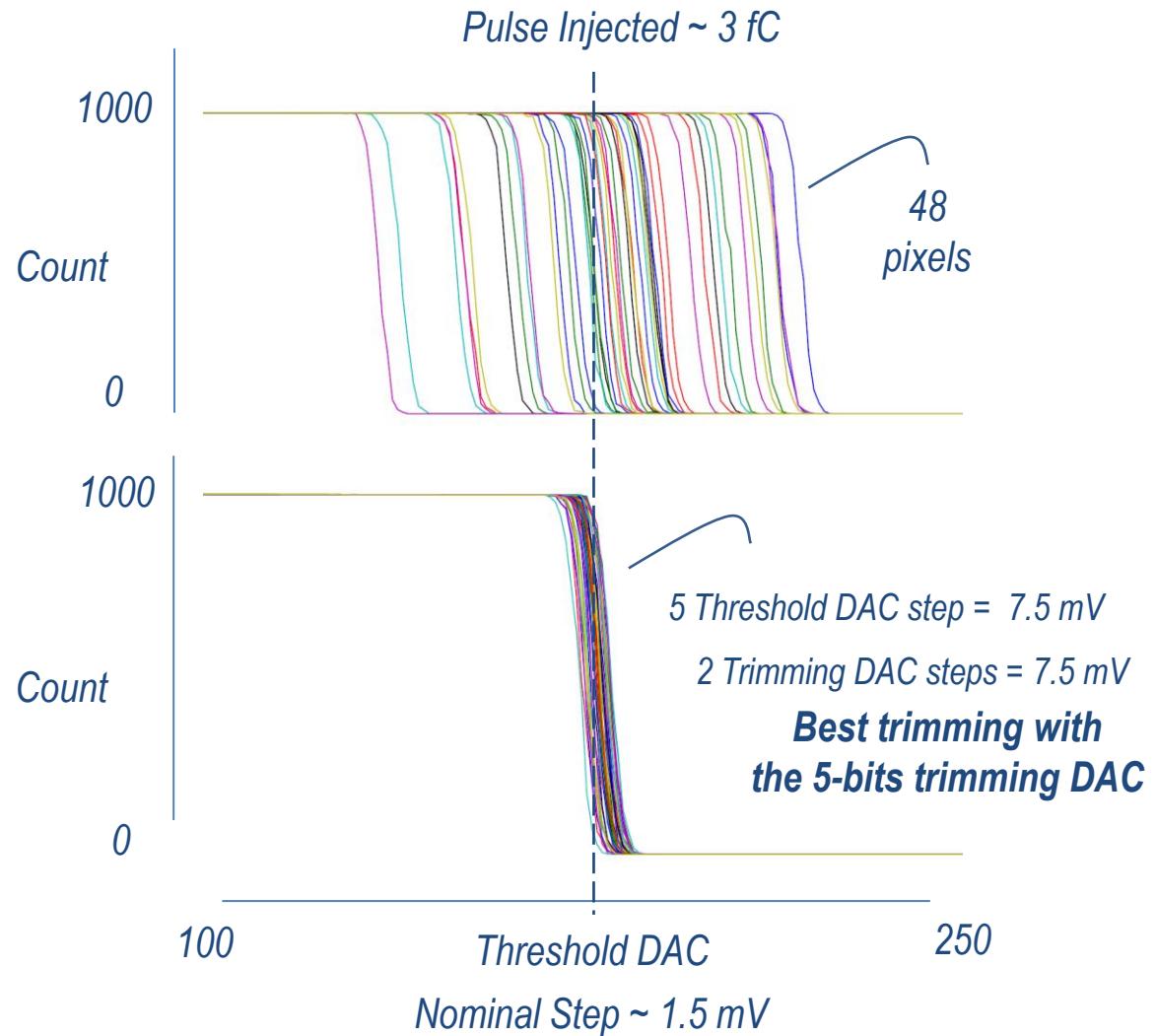
Calibration DAC measurement

Calibration DAC is the only DAC we can measure directly the voltage.

8.7 fC

On purpose for Radiation hardness

Calibration pulse [fC]

*Offset = **0.044 fC***

Nominal step = 0.035 fC
*Measured step = **0.034 fC***

0 fC

0   255

DAC code
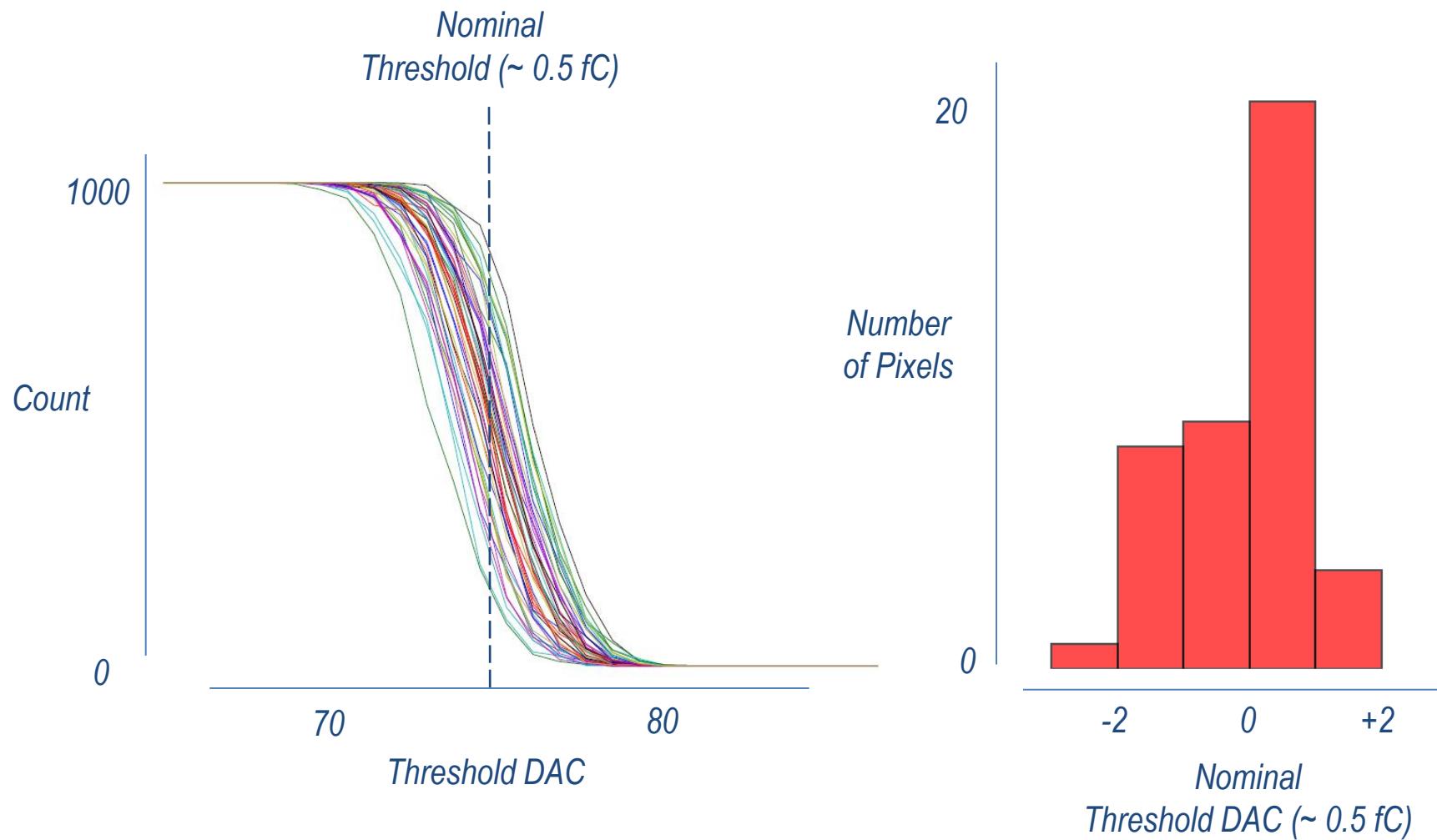
S-curve with trimming procedures

Trimming allows to correct for the threshold variation along the pixel array and to set the same threshold for all the pixels

Pulse Injected ~ 3 fC

1000

Count

0

48 pixels

1000

Count

0

5 Threshold DAC step = 7.5 mV

2 Trimming DAC steps = 7.5 mV

Best trimming with the 5-bits trimming DAC

100

Threshold DAC

Nominal Step ~ 1.5 mV

250
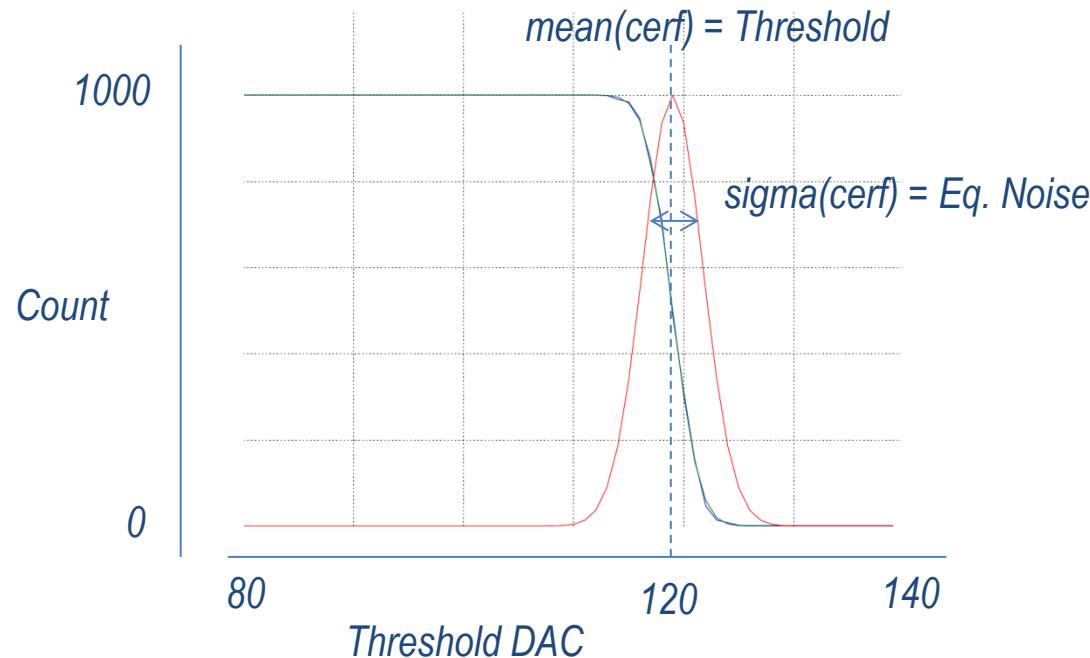
Iterative trimming at nominal threshold

Allows optimization around the operative point

Nominal
Threshold (~ 0.5 fC)

1000

Count

0

70   80

Threshold DAC

20

Number
of Pixels

0

-2   0   +2

Nominal
Threshold DAC (~ 0.5 fC)
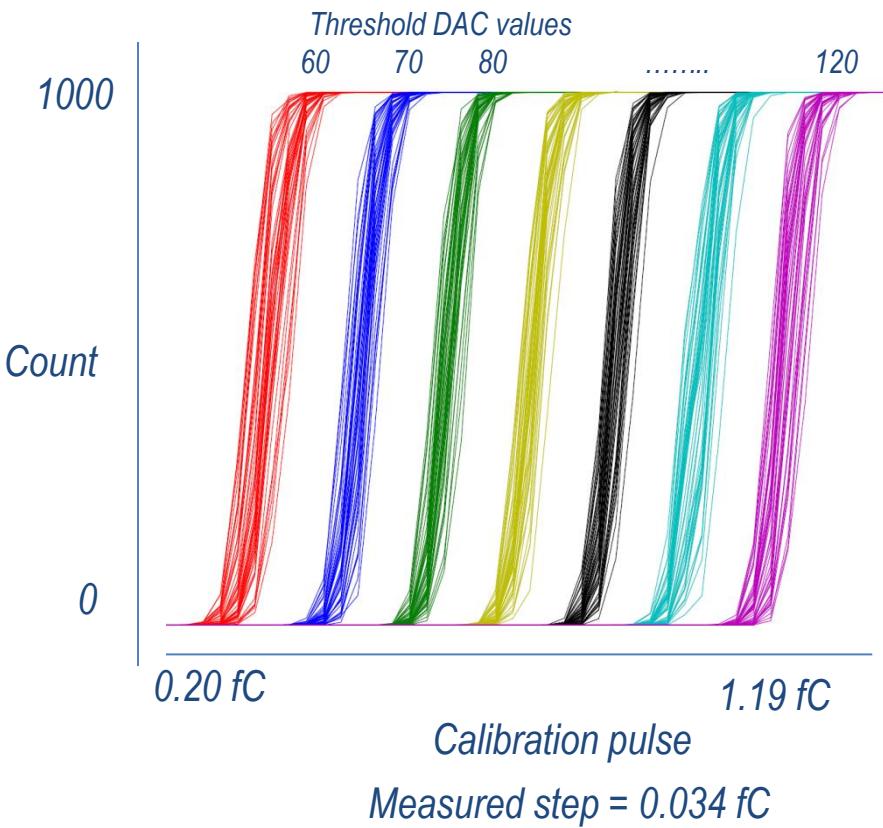
S-curve fitting with error functions

The error function and its complementary allows the extraction of the Analog Front-End parameters from the S-curves obtained from the hit counters
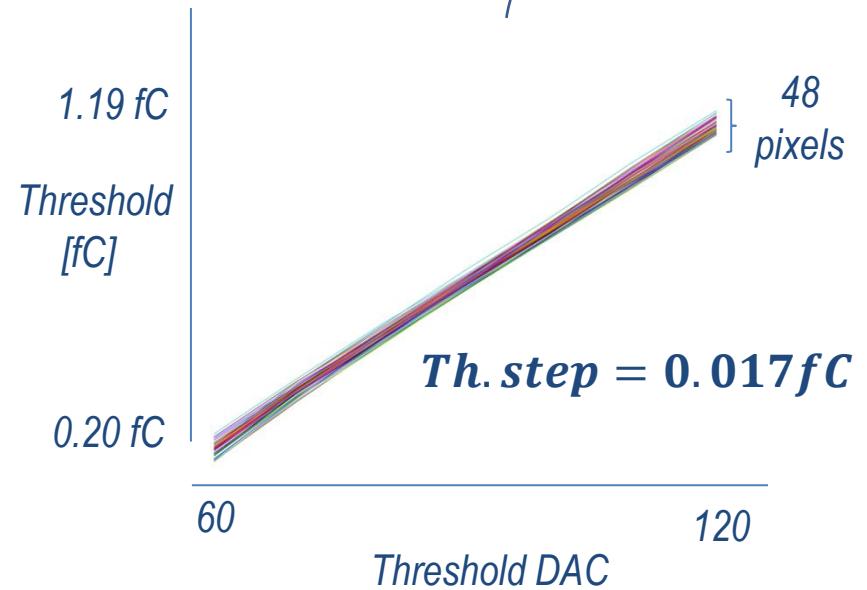
The fitting of a threshold S-curves provides threshold and noise information about the pixel

Threshold DAC measured with calibration pulses

Threshold DAC values
60   70   80   ……..   120

1000

Count

0

0.20 fC   *1.19 fC*

Calibration pulse

Measured step = 0.034 fC

For every pixel, the threshold is extracted with the error function fitting

1.19 fC

Threshold [fC]

48 pixels

$$Th. step = 0.017 fC$$

0.20 fC

60   *120*

Threshold DAC
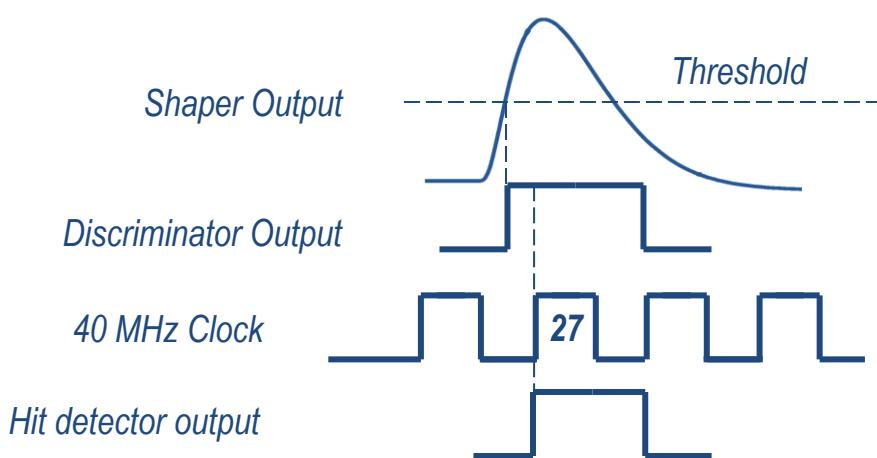
Hit detector and No processing mode

```
>>> conf.ModifyPixel(range(1,3), 'SR', 1)
>>> conf.Upload()
>>> daq.SendCalibrationStrobe(3, 4, 40, 40)
>>> (BX, hit) = daq.ReadMemory ()
>>> BX

            [27, 38, 49]

>>> hit

            ['1111000000000000000000000000000000000000000000000',
             '1111000000000000000000000000000000000000000000000',
             '1111000000000000000000000000000000000000000000000']
```

Synchronous readout active in pixel from 1 to 4.

3 test pulses

Readout the memory and save the data in two variables

Time stamp (Bunch crossing number when the memory is written)

Pixel hits in BX = 27

Pixel hits in BX = 38

Pixel hits in BX = 49

Shaper Output

Threshold

Discriminator Output

40 MHz Clock   **27**

Hit detector output
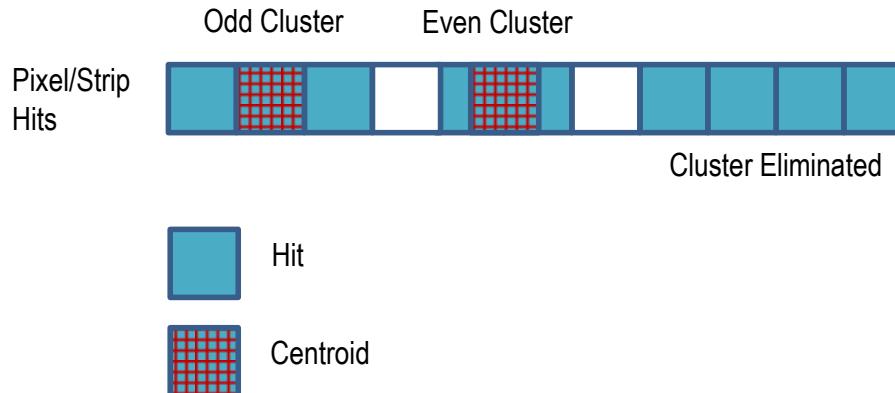
Pixel clustering finds the center of the cluster

```
>>> conf.ModifyPixel(range(1,3), 'CW', 3)
>>> conf.Upload()
>>> daq.SendCalibrationStrobe(3, 4, 40, 40)
>>> (BX, hit) = daq.ReadMemory (3)
>>> BX
            [27, 38, 49]
>>> hit
```

*Pixel Clustering active (accepted cluster width 5)
in pixel from 1 to 4.*

['0100000000000000000000000000000000000000000000000', *Centroid in BX = 27*
 '0100000000000000000000000000000000000000000000000', *Centroid in BX = 38*
 '0100000000000000000000000000000000000000000000000'] *Centroid in BX = 49*

Odd Cluster   Even Cluster

Pixel/Strip Hits

Cluster Eliminated

Hit

Centroid

Centroid extraction encodes cluster positions

```
>>> conf.ModifyPeriphery('OM', 2)
>>> conf.Upload()
>>> daq. SendCalibrationStrobe(3, 4, 40, 40)
>>> (BX, centroids) = daq.ReadMemory (2)
>>> BX
          [27, 38, 49]
>>> centroids
          [[2.5, 2.5, 2.5], [1, 1, 1]]
```

Operative mode is set to Centroid extraction

Read memory mode is set to Centroid extraction
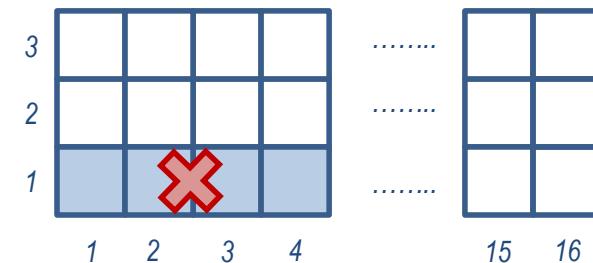
Column coordinate   *Row coordinate*
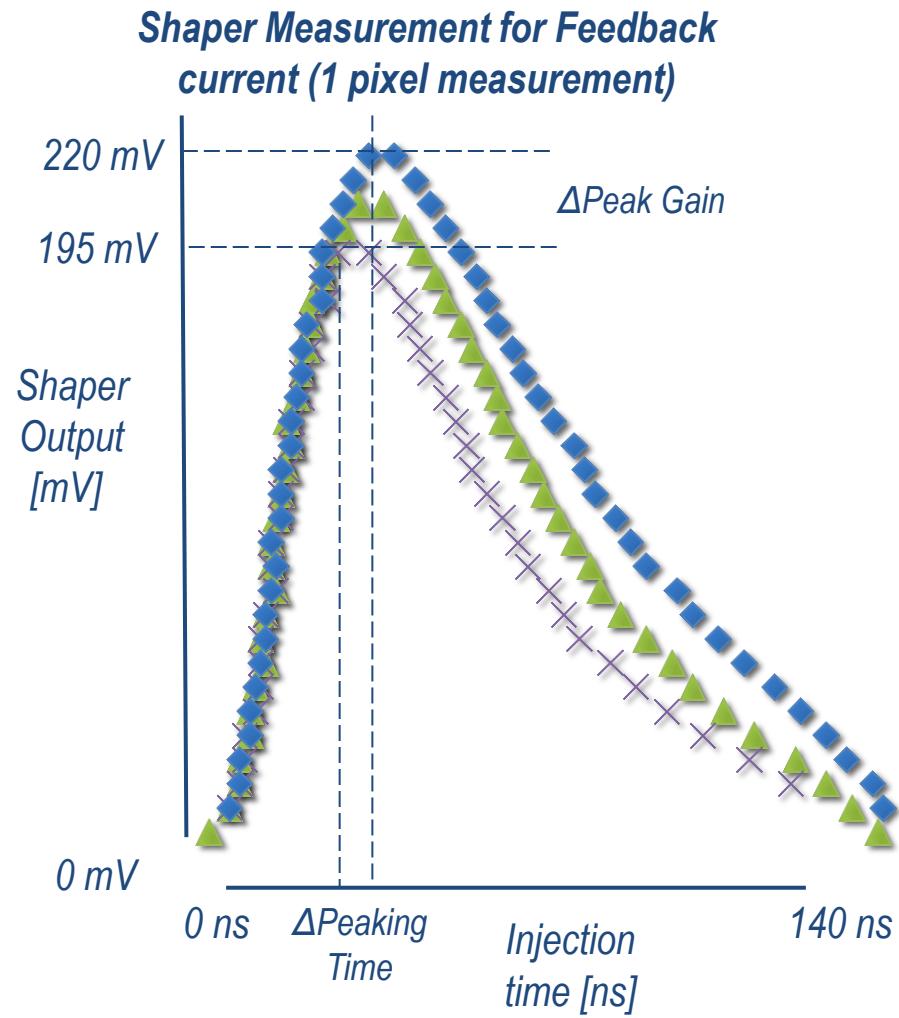
Shaper measurement for different biases
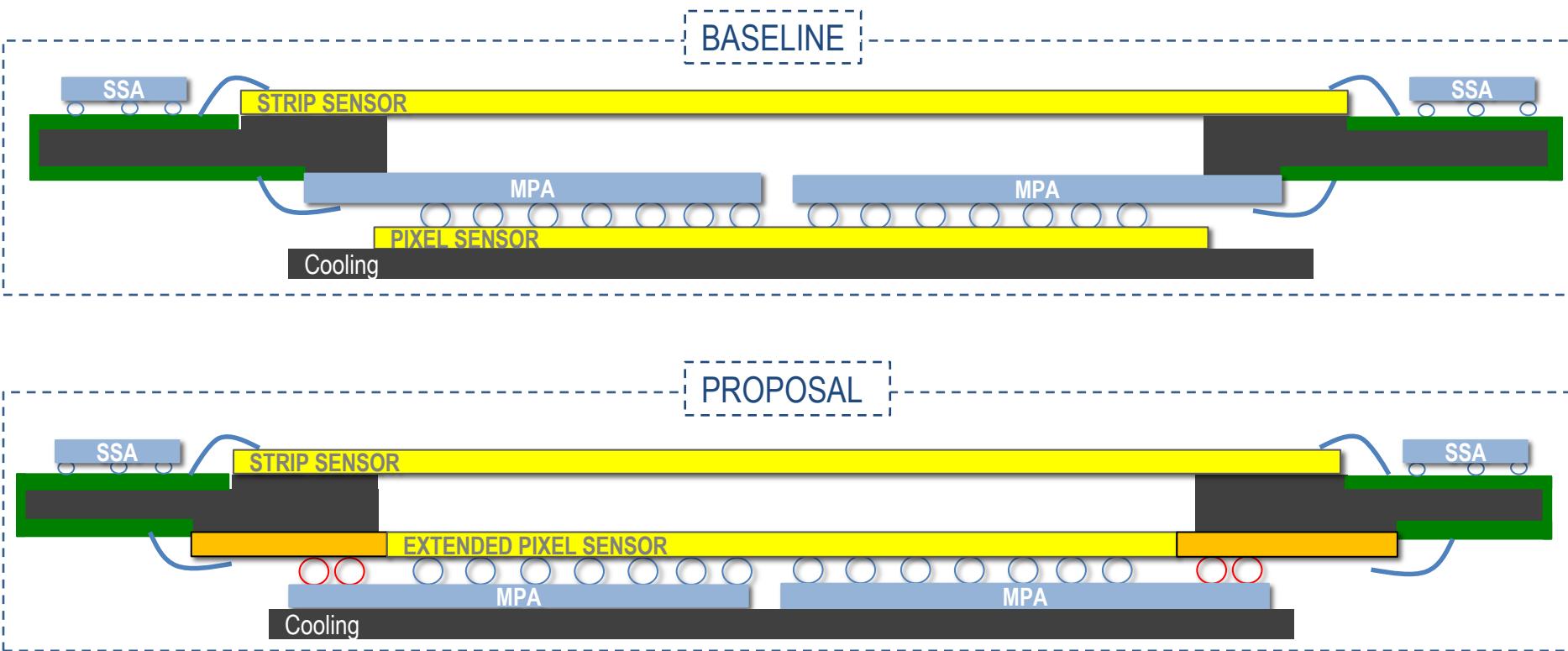
Current and voltage reference for the Analog front-end can be tuned through three external voltage reference:

Bias Voltage

Feedback Voltage

Pre Amplifier Voltage

The three references can undergo a variation of +/- 25% and we can measure the effect on the shaper output with injection time sweep

Shaper Measurement for Feedback current (1 pixel measurement)

220 mV

195 mV

ΔPeak Gain

Shaper Output [mV]

0 mV

0 ns

ΔPeaking Time

Injection time [ns]

140 ns

MPA-Light ASIC allows two assemblies

BASELINE

SSA
STRIP SENSOR
SSA
MPA
MPA
PIXEL SENSOR
Cooling

PROPOSAL

SSA
STRIP SENSOR
SSA
EXTENDED PIXEL SENSOR
MPA
MPA
Cooling
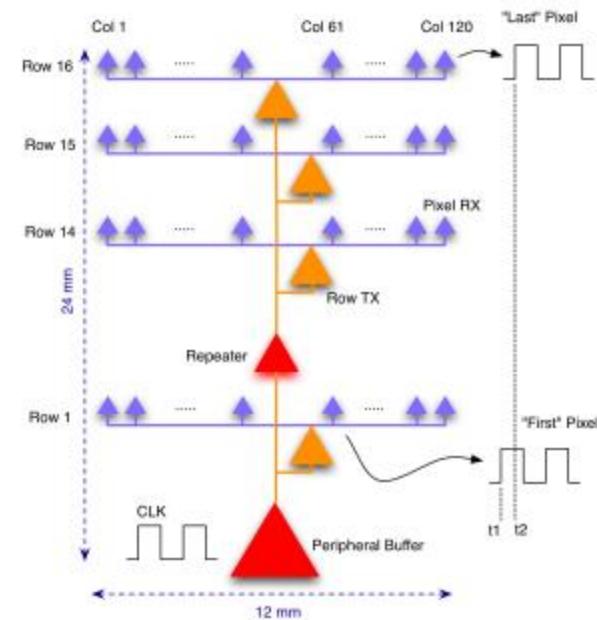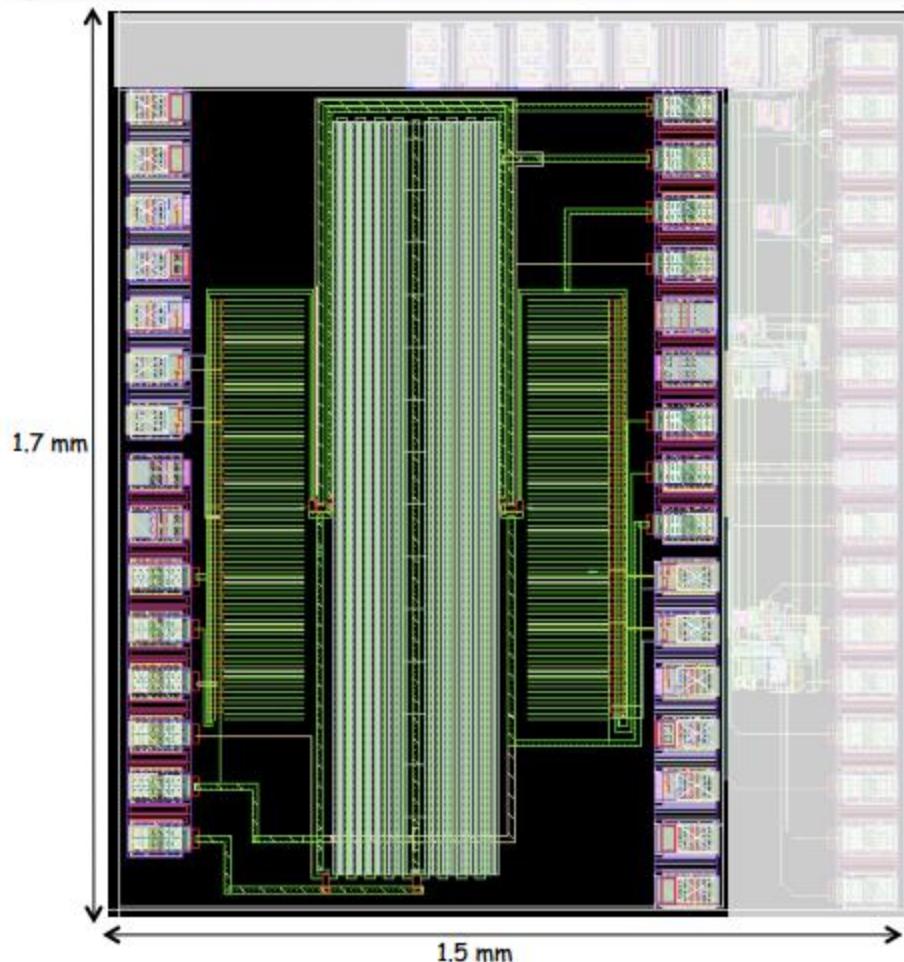
- Only bump bonding in MPA design
- No extra material between strip and pixel sensors
- Better cooling of MPA
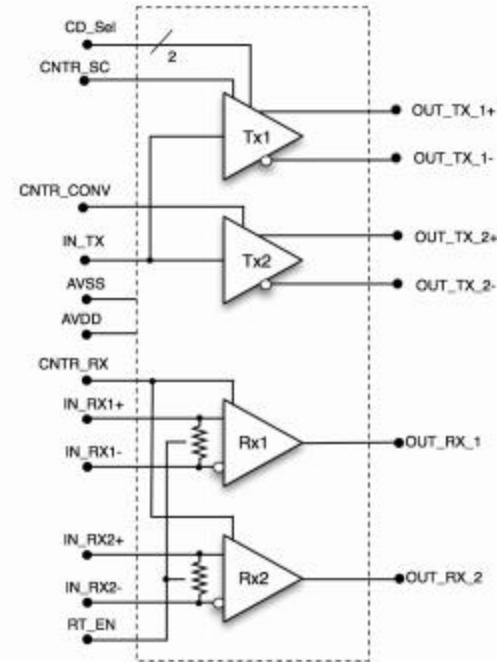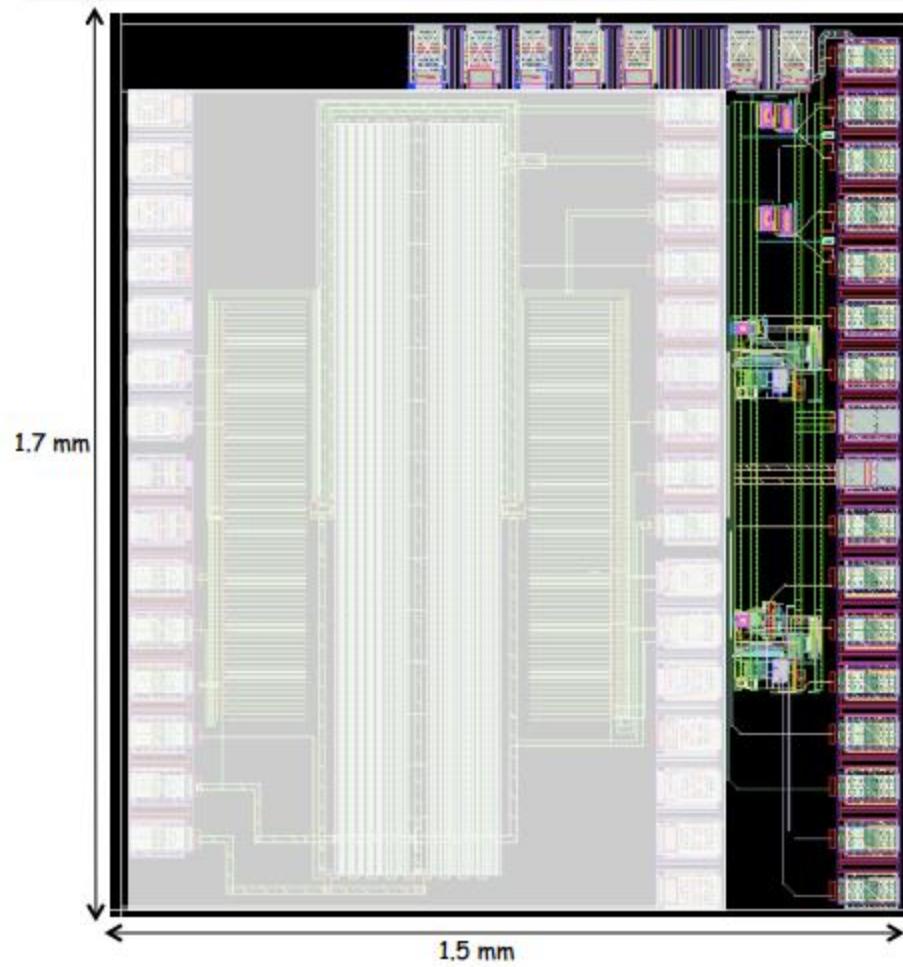
- Digital IO through sensor periphery
- Temperature gradient across the sensor surface can be critical
- Larger sensor can create problem in final design production
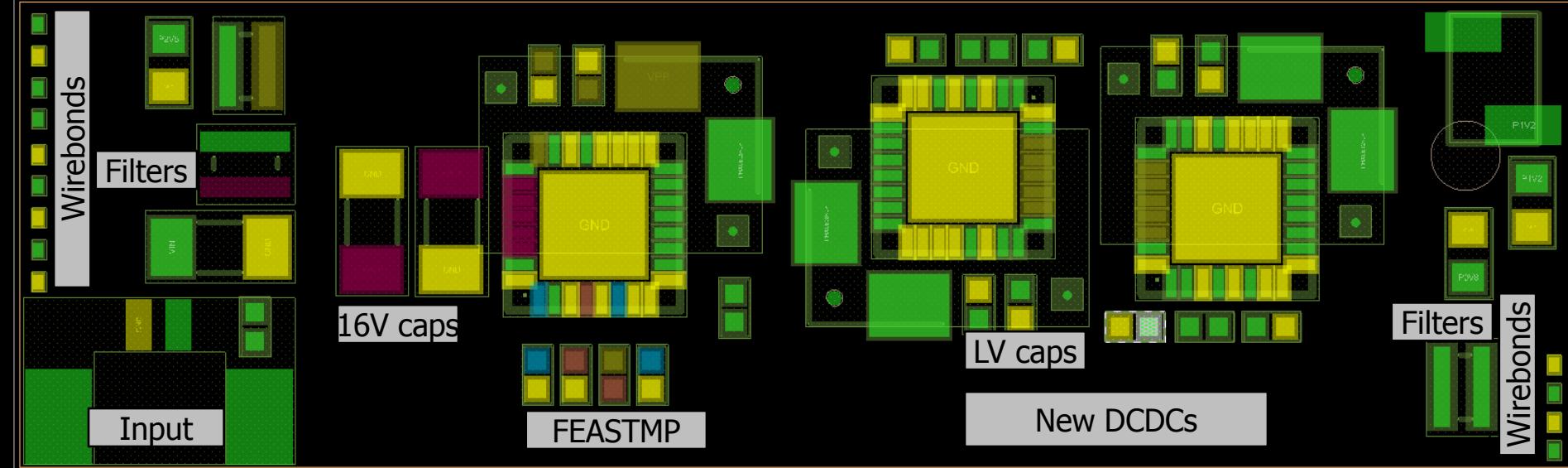
Chip Layout (clock distribution)

Chip Layout (sLVDS drivers and receivers)

Input power: low profile Molex Picoblade 2 poles connector (stands our current rating).
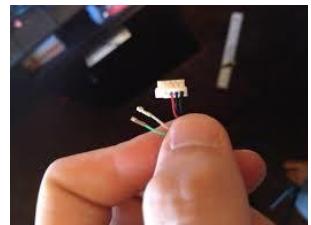
The filters will stay out of the shield area, must be on sides.
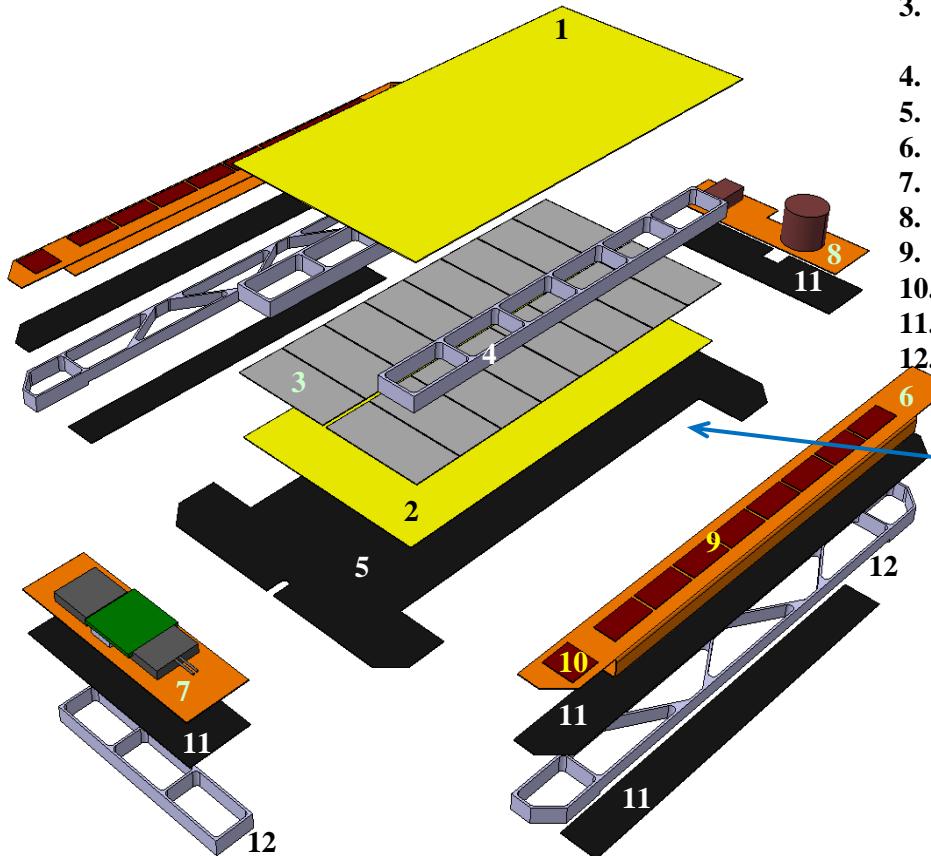
Wirebond based IO implemented so far.

The same low mass ECCA based coil is used for the 3 converters.
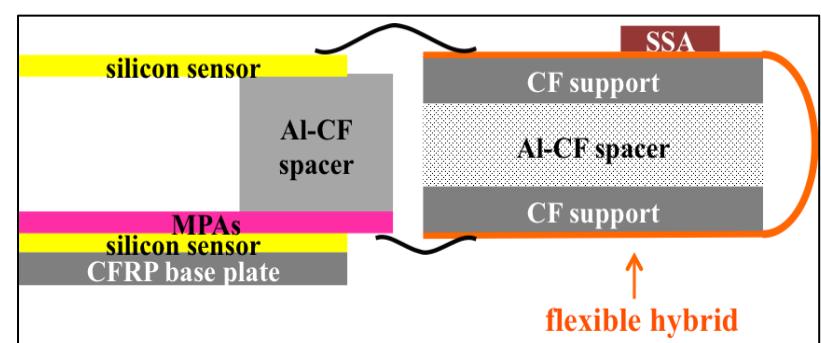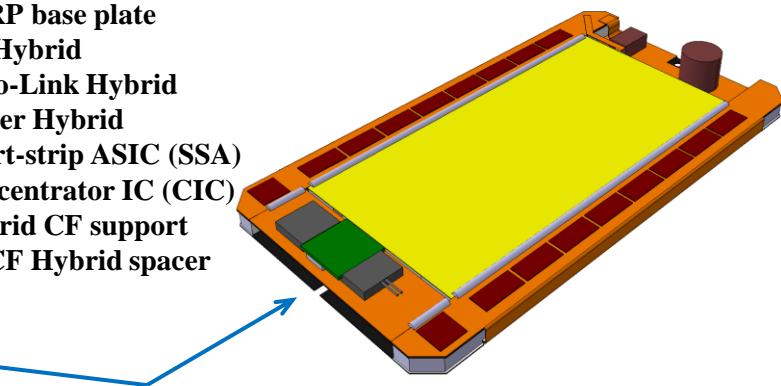
The new LV DCDCs still based on teh FEASTMP geometry. However we can consider a smaller package for this chip.

The 3 DCDC stages can be fitted in the available board space without excessive compromise.
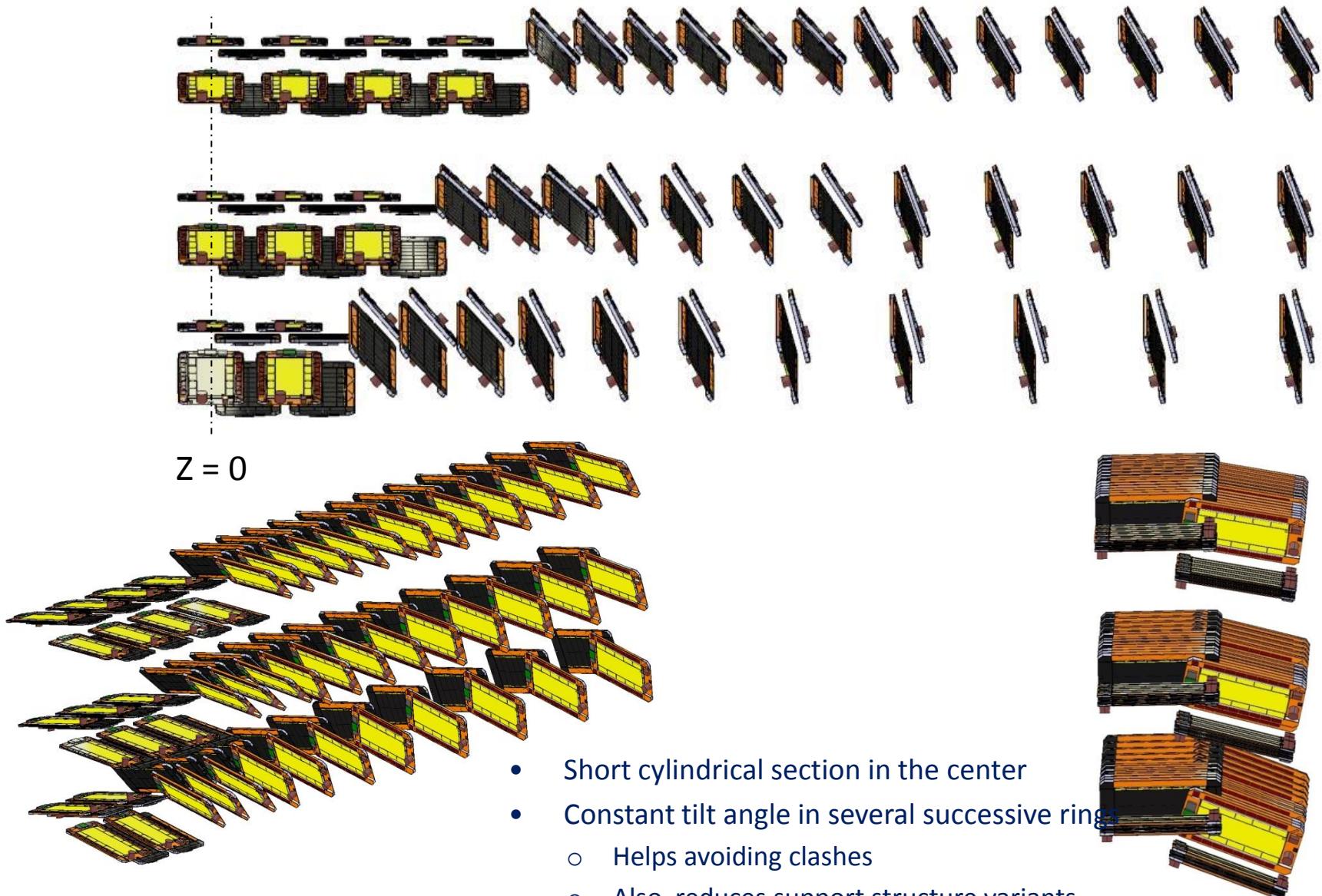
1. Silicon strip sensor
2. Silicon pixel sensor
3. Macro-Pixel ASIC (MPA)
4. Al-CF sensor spacer
5. CFRP base plate
6. FE Hybrid
7. Opto-Link Hybrid
8. Power Hybrid
9. Short-strip ASIC (SSA)
10. Concentrator IC (CIC)
11. Hybrid CF support
12. Al-CF Hybrid spacer
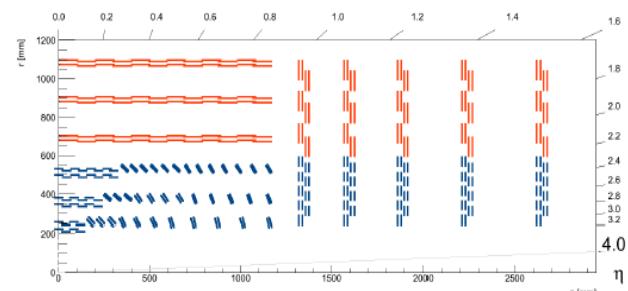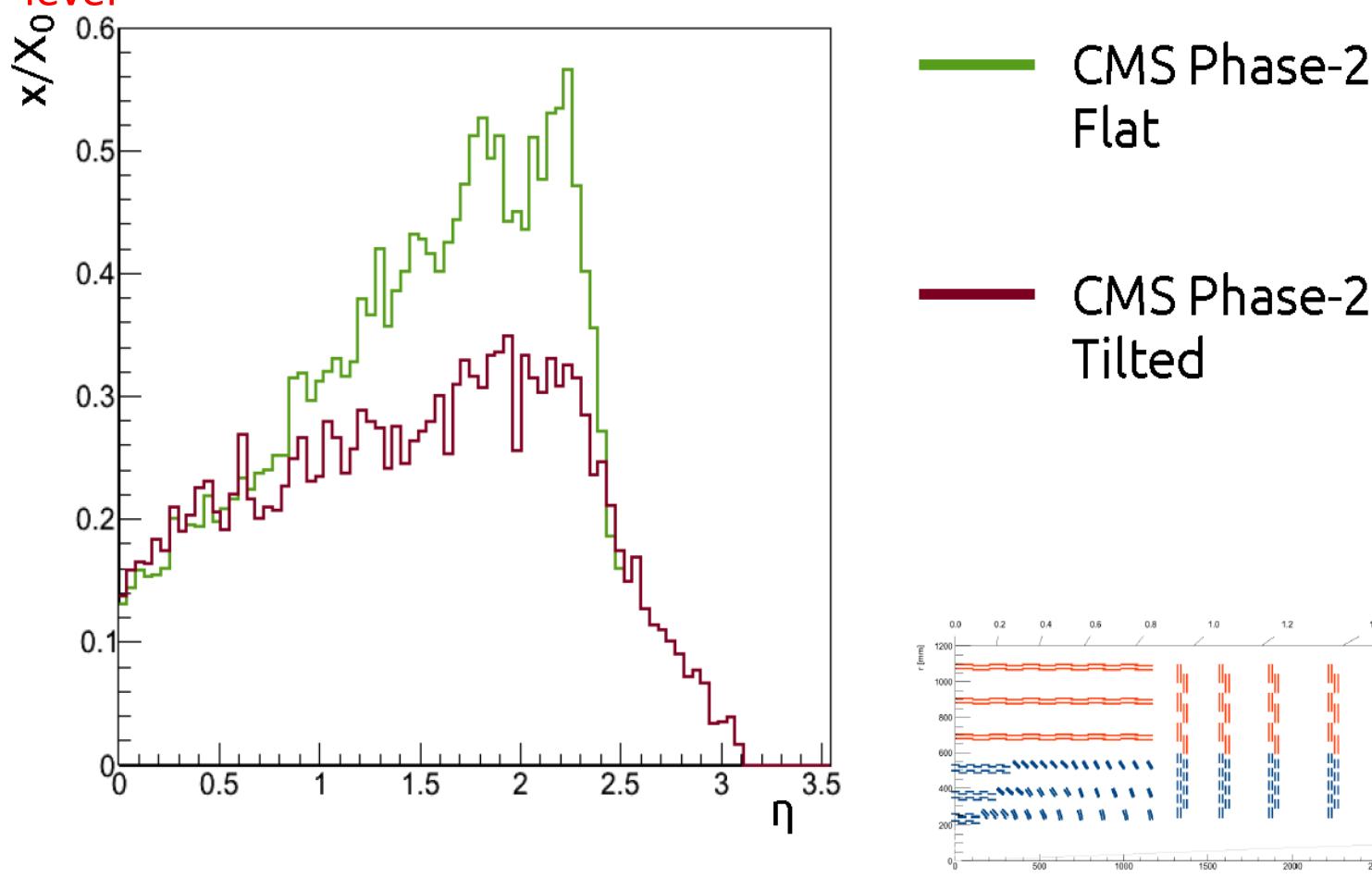
**Support and cooling
via a large-area base plate**

Z = 0

- Short cylindrical section in the center
- Constant tilt angle in several successive rings
  - Helps avoiding clashes
  - Also, reduces support structure variants.
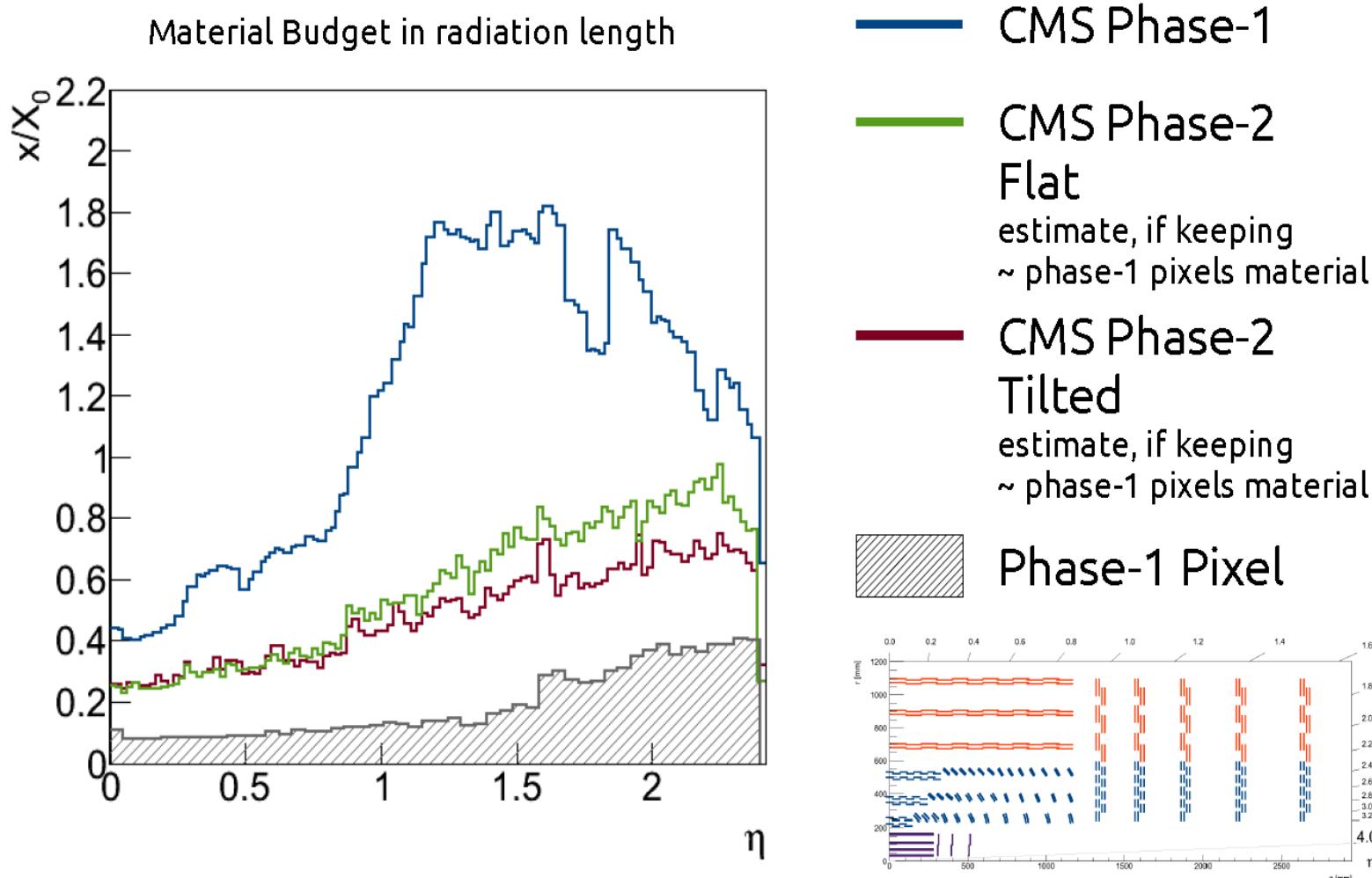
S. Mersi at al., Performance of Tilted Inner Barrel, CMS Upgrade Workshop 1 April 2014

The gain by the Tilted inner section is clearly visible even at the full Tracker level
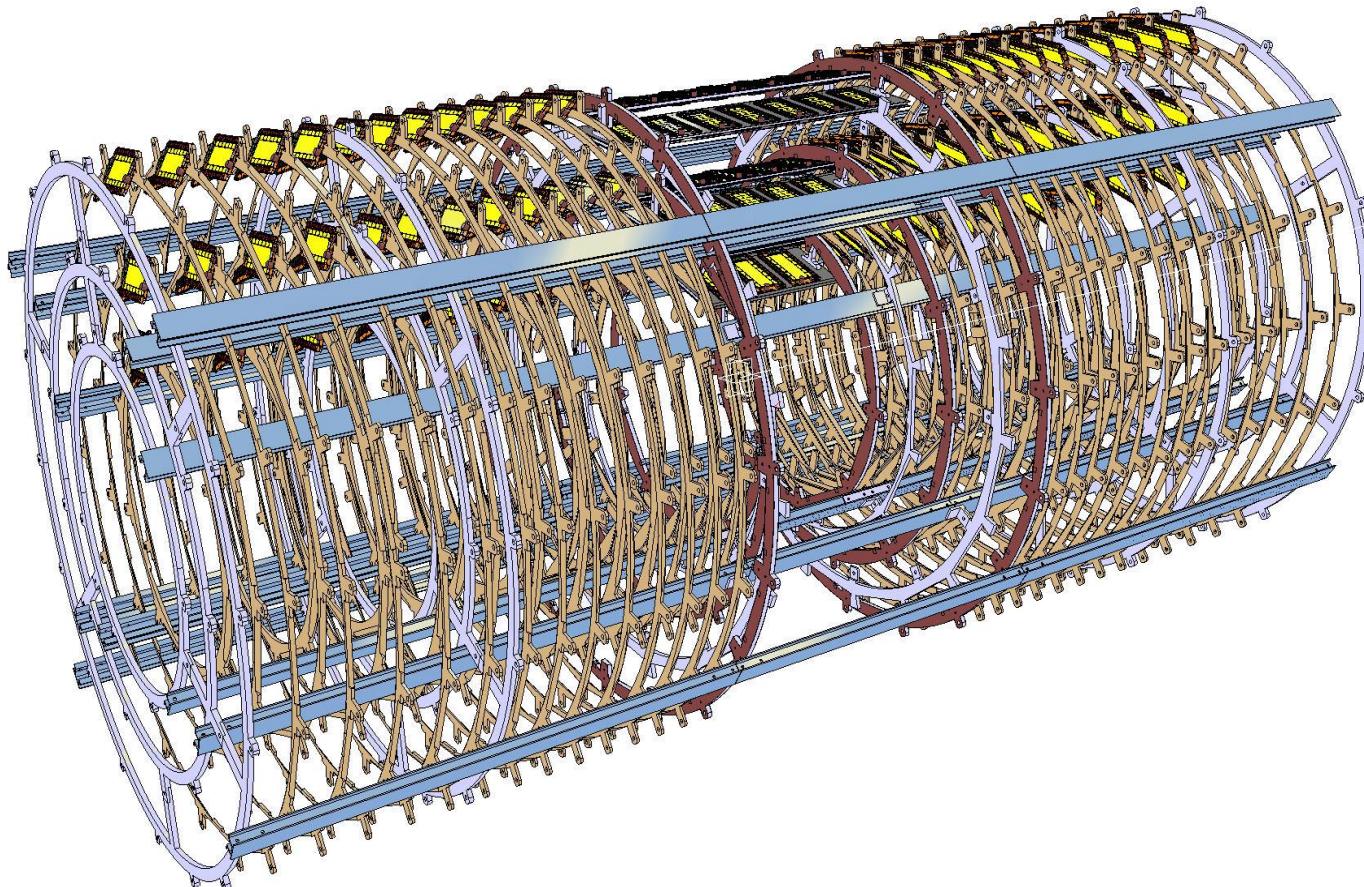
Material budget full tracker

Material Budget in radiation length

CMS Phase-1

CMS Phase-2 Flat
estimate, if keeping ~ phase-1 pixels material

CMS Phase-2 Tilted
estimate, if keeping ~ phase-1 pixels material

Phase-1 Pixel

This design still misses a few 'details':
- Most of the modules (on purpose to keep CAD model size reasonable).
- Power wire and optofibres and their handling during various assy stages
- Cooling pipe manifolding, supply lines and connections

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