Front-end hybrids for the CMS Outer Tracker Phase 2 Upgrade

EP-ESE Seminar

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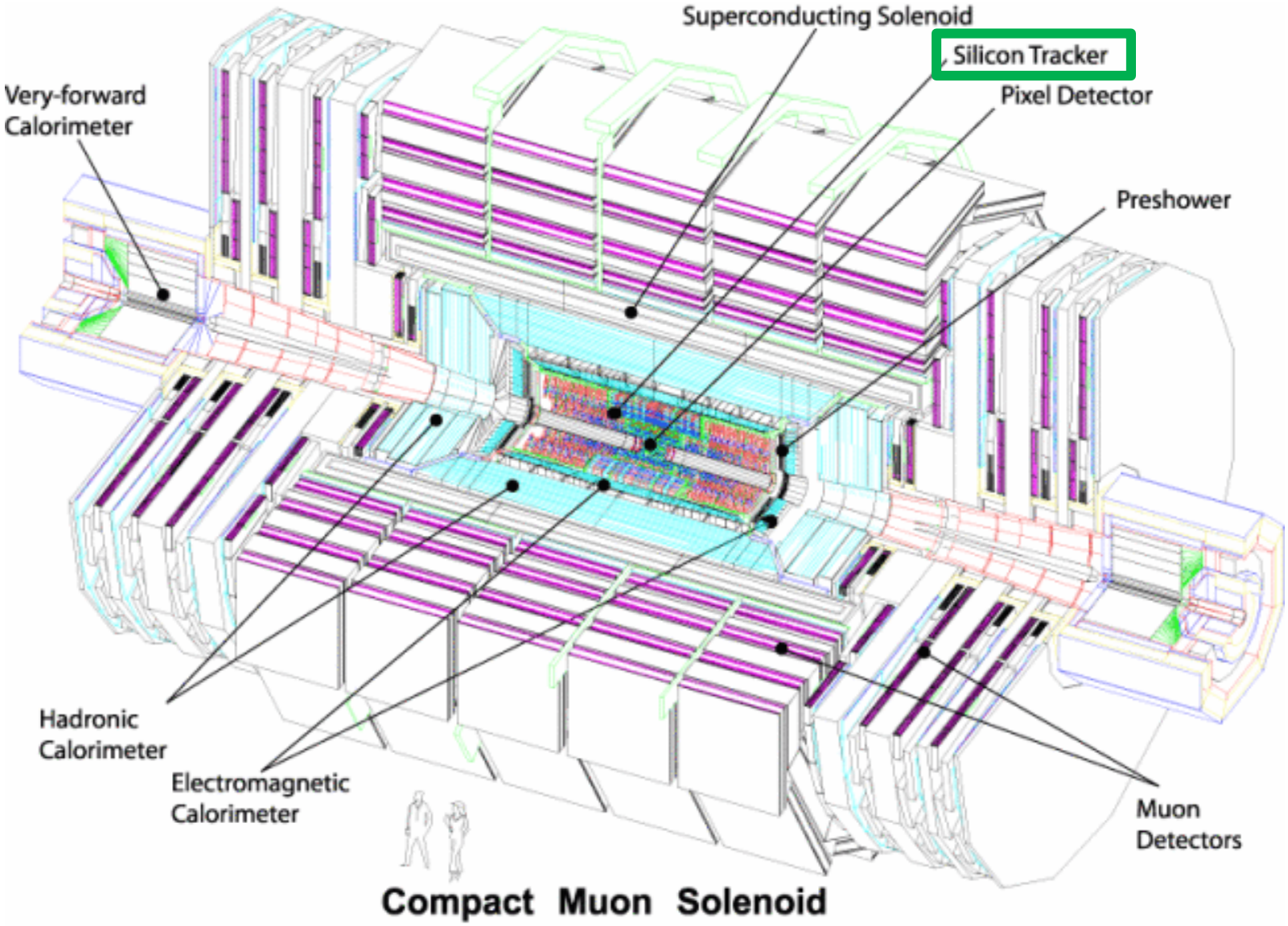
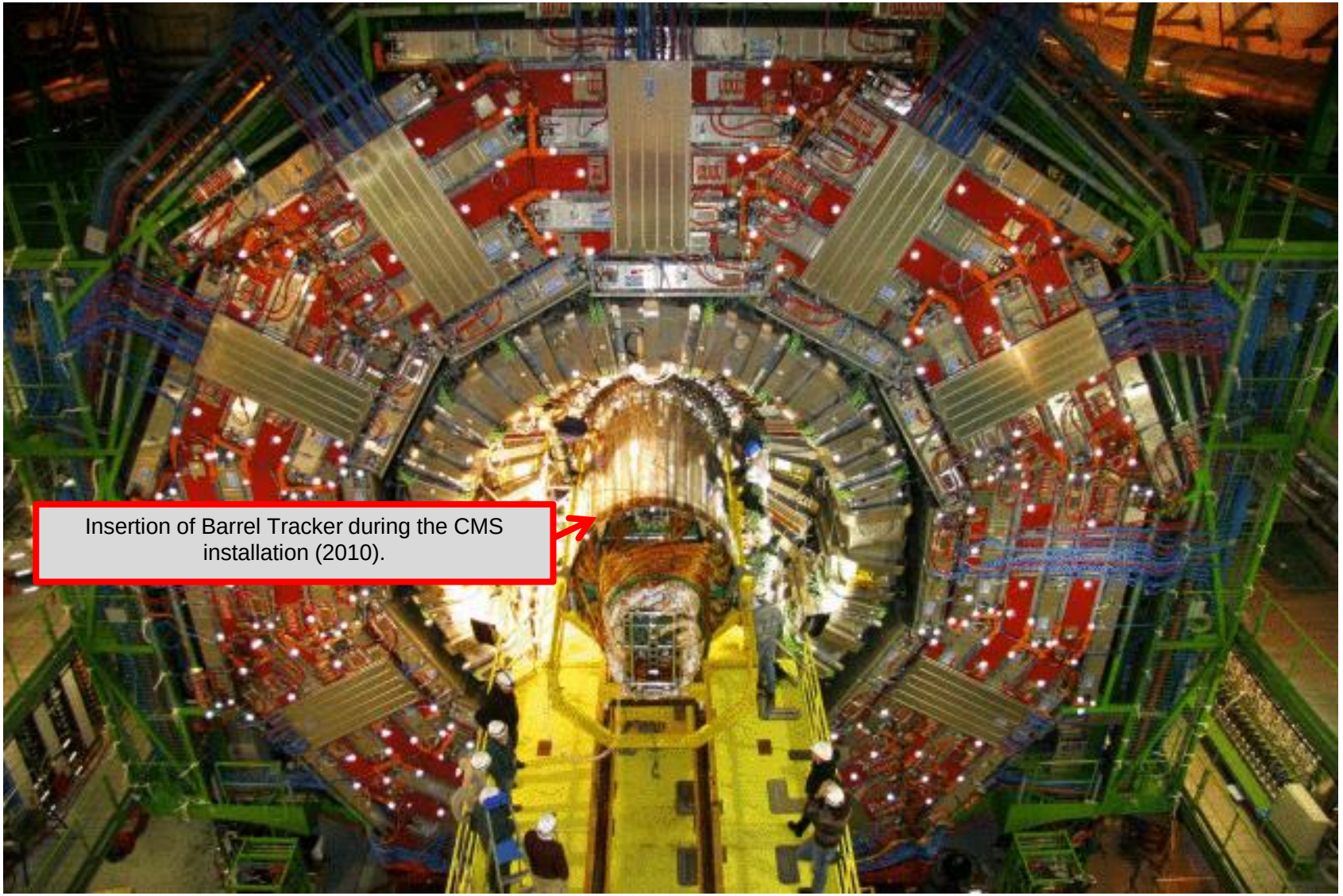
- Introduction of the Phase-2 tracker upgrade.
- Module topologies.
- Front-end hybrids variants.
- Carbon-fibre stiffeners and the stiffener test.
- Introduction of test coupons.
- The reliability test system.
- Test results.
- The hybrid production scale test system.
- Future plans and conclusion.

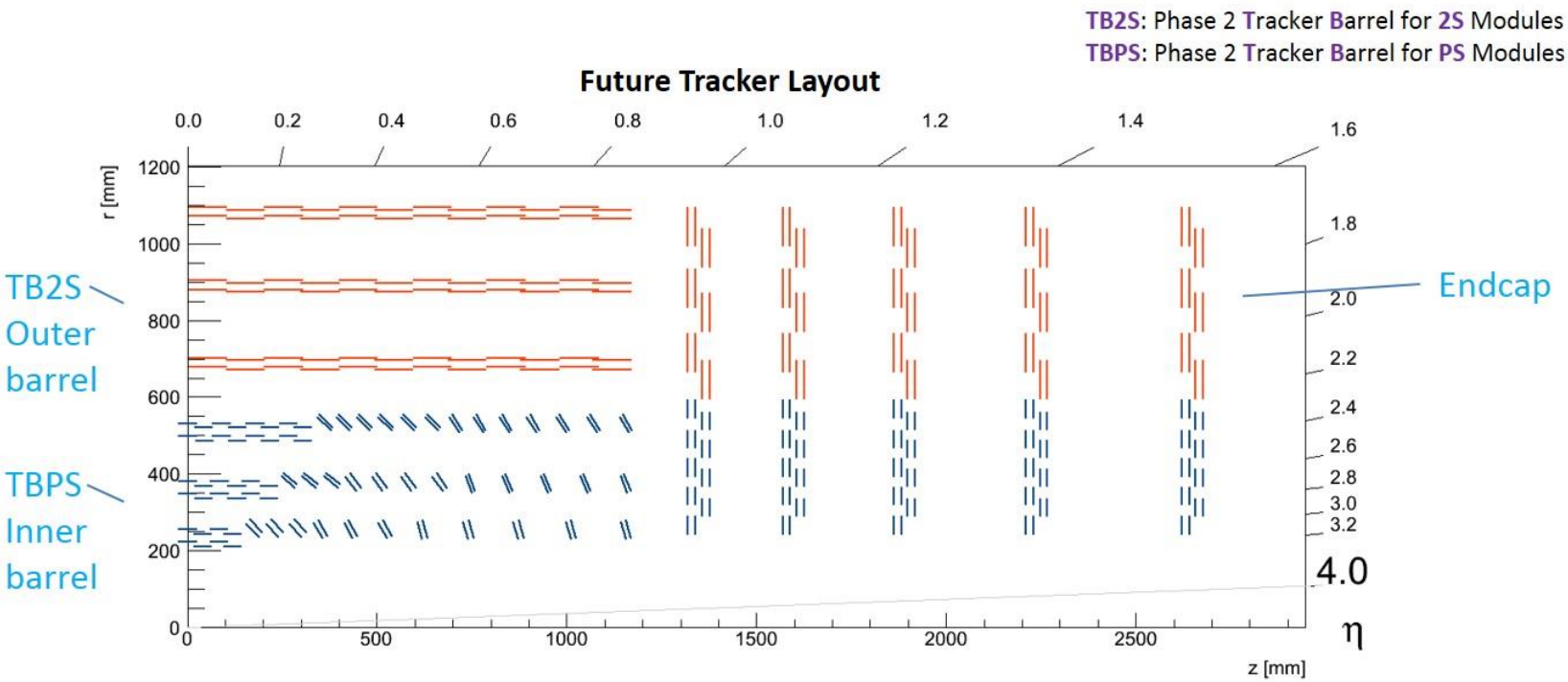

Superconducting Solenoid
Silicon Tracker
Pixel Detector
Very-forward
Calorimeter
Preshower
Hadronic
Calorimeter
Electromagnetic
Calorimeter
Muon
Detectors
Compact Muon Solenoid


Insertion of Barrel Tracker during the CMS installation (2010).

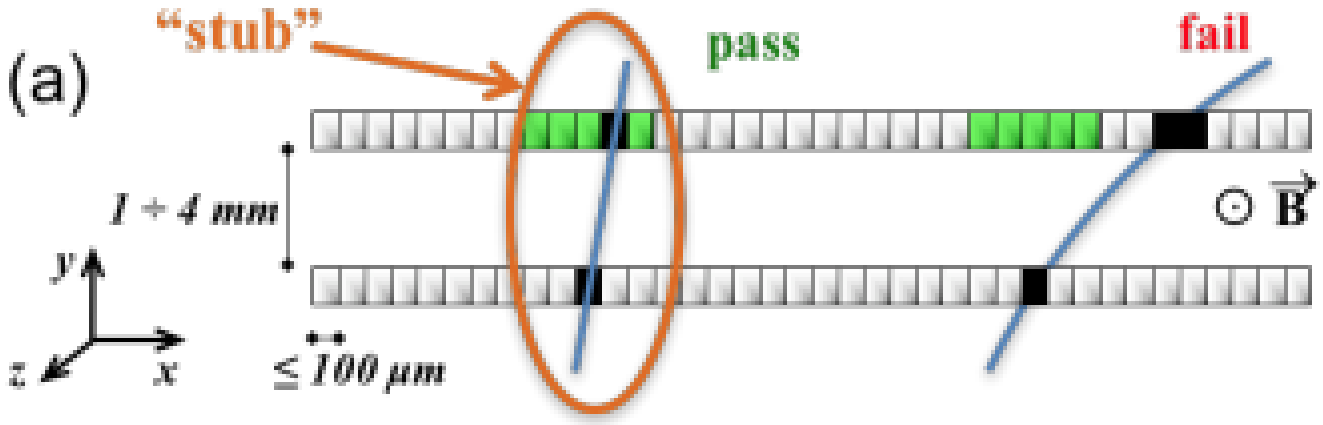
- **The CMS experiment has been operative from 2010 until now.**
  - Large amount of physics data collected.
- **The LHC is going through different upgrades.**
  - Hardware facility improvement to provide higher beam luminosity.
  - Increased energy during beam collisions.
  - Long Shutdown 3 (LS3) to release the Phase 2 Upgrade scheduled by 2023.
- **The CMS Tracker will require a full upgrade to cope with the new HL-LHC constraints:**
  - Increased granularity: to cope with higher rate of events.
  - Improved radiation hardness: to cope with increased luminosity.
  - Reduction of mass: to obtain the required resolution.
  - Provide L1 tracking information: to reduce the data volume.

- R&D for the future upgrade of the CMS tracker started in 2013, and is the scope of the hybrid circuits developments presented here.

New Tracker Geometry and Low Momentum Rejection



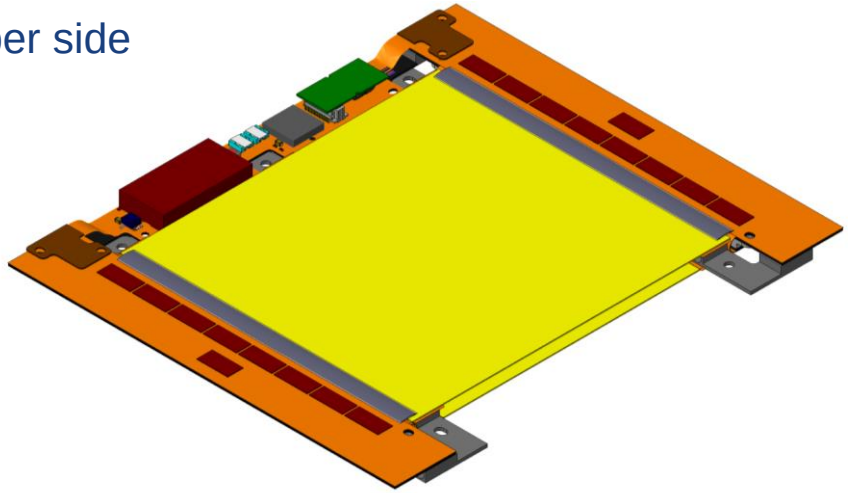
- Tracks of interest must be selected to cope with the higher rate of events.
- Focus only on high momentum tracks.
- Two parallel sensors provide the momentum information.
- The inner barrel adds also Z axis resolution.
- Stubs are formed from the high momentum tracks. They are used for L1 triggering construction at the back-end.



- Stubs defined as a track coordinate + angle based on tracking window on parallel sensor.
- Spacing between sensors must be adjusted depending on tracker location.
- At small track angles, endcaps are preferred and sensor spacing is increased.

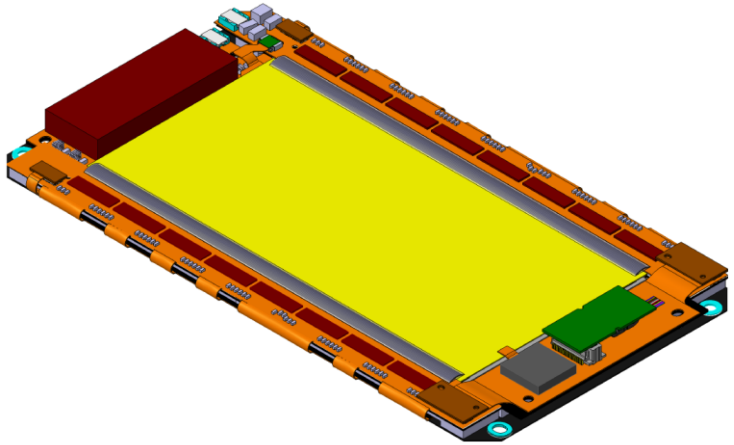
2S Modules

- 2 Strip Sensors: 2 × 1016 strips 5cm × 90 µm per side
- 90 cm^2 active area
- For R > 60 cm
- Spacing 1.8 mm and 4.0 mm
- Two front-end hybrids and one service hybrid (opto + power).
- Total 2S modules needed: 8424

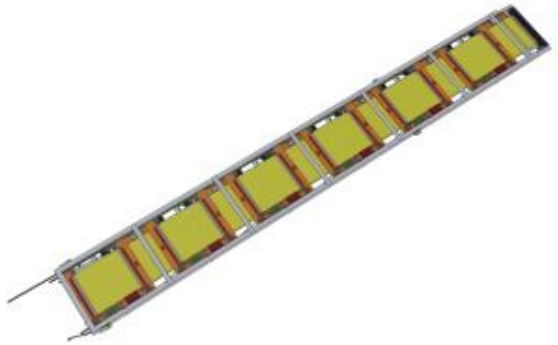


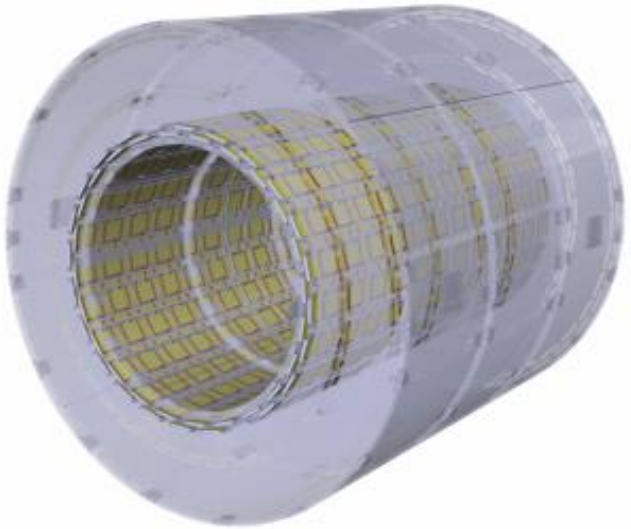
PS Modules

- Pixel + Strip Sensors
- 2 × 960 Strips 2.5 cm × 100 µm
- 32 ×960 macro-pixels 1.5 mm × 100 µm
- 45 cm^2 active area
- For R > 20 cm
- Spacing 1.6 mm, 2.6 mm and 4.0 mm
- Total 2S modules needed: 5708

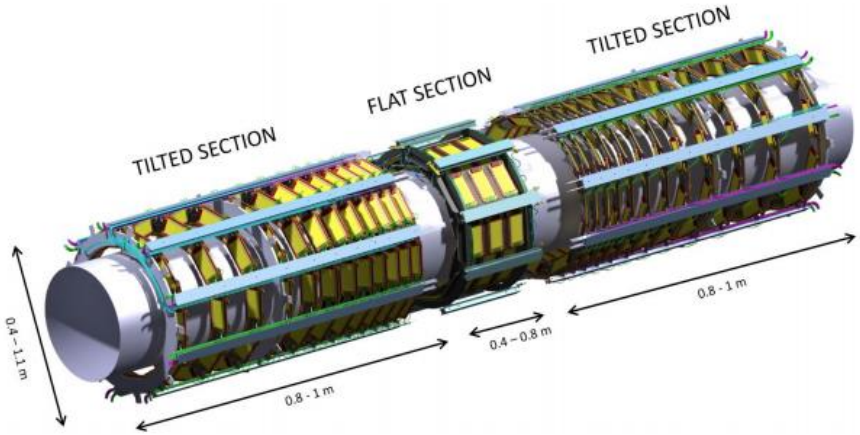


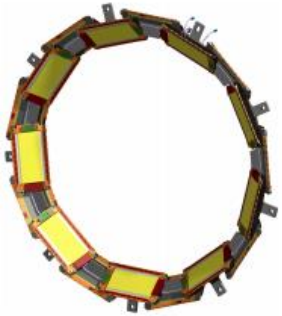
- **2S barrel modules are organized in staves.**
- Staves arranged to form 3 coaxial barrels.

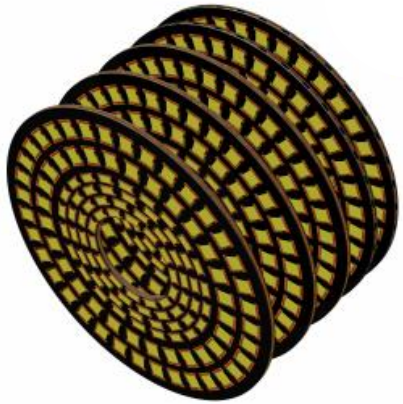




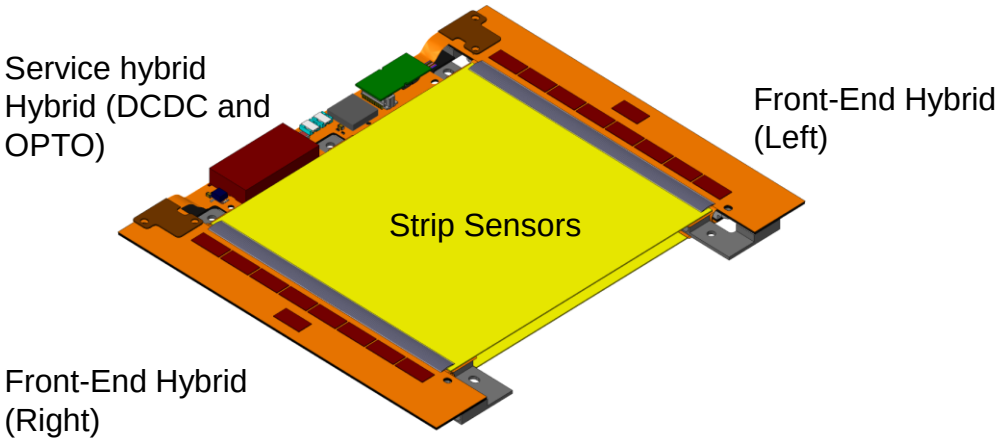
- **PS modules are organized in flat planks and with tilted section rings**



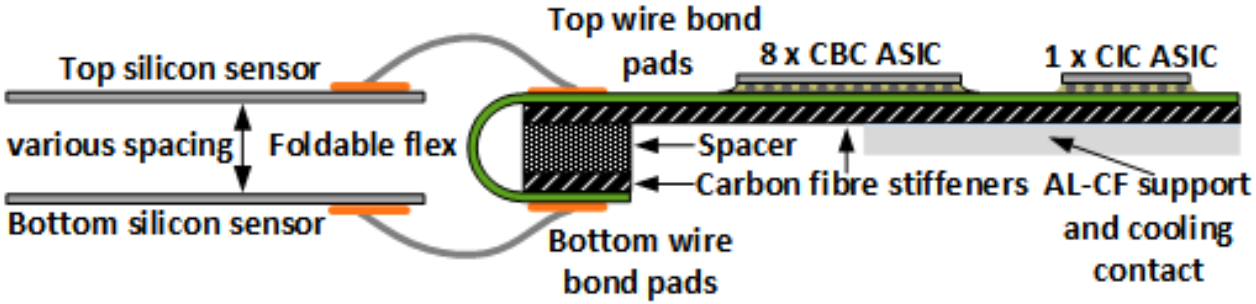




- **Endcaps are organized as discs.**



- 2S front-end hybrids contain eight CBC3 front-end ASICs, feeding a Concentrator ASIC
- The Concentrator ASICs transmits high speed data to a lpGBT transmitter on the service hybrid.
- All the system is powered by DCDC converters on the service hybrid.

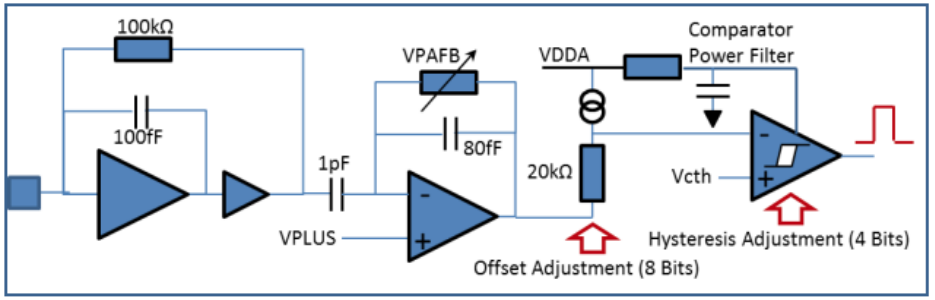


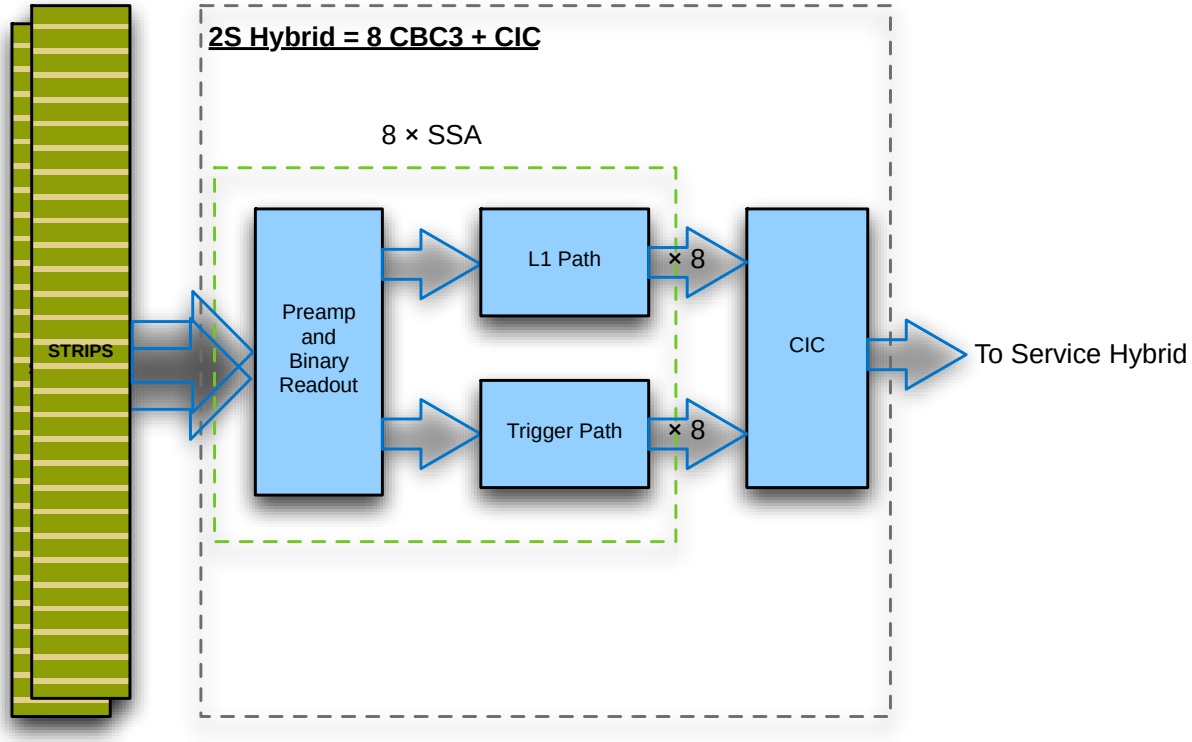
- The front-end hybrid is a high density interconnect flexible circuit folded around a carbon fibre structure.
- Two sensors processed by single chip enable low momentum tracks rejection and creation of stubs for L1 triggering.

- Preamplifier and shaper with offset control.
- Discriminator with programmable threshold and hysteresis.
- Hit detection.

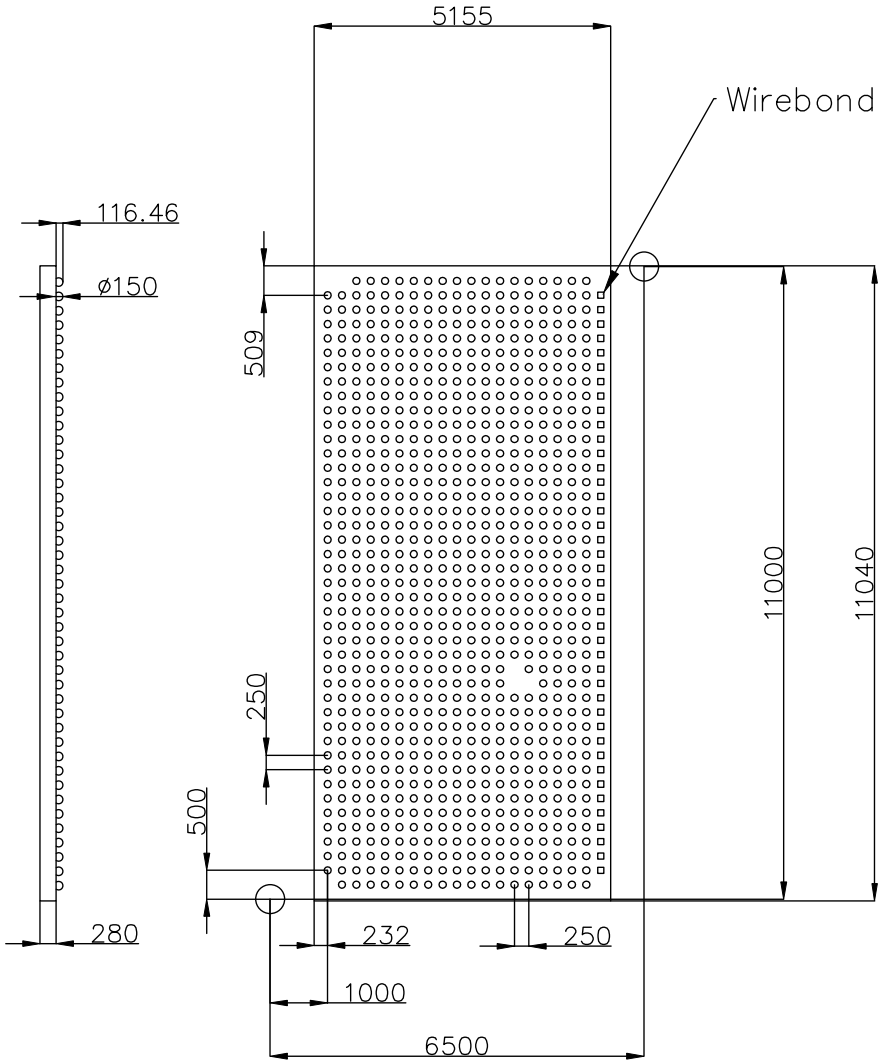
- Hits pushed into pipeline awaiting for L1 trigger.
- Hits pushed in stubs gathering logic.

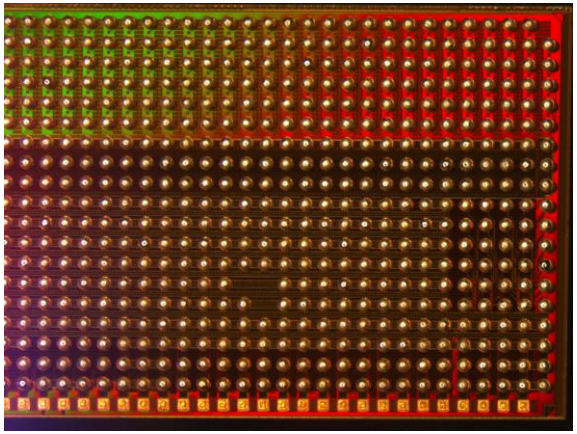
- Stubs and triggered data extracted from pipeline are transmitted at LHC BC rate.



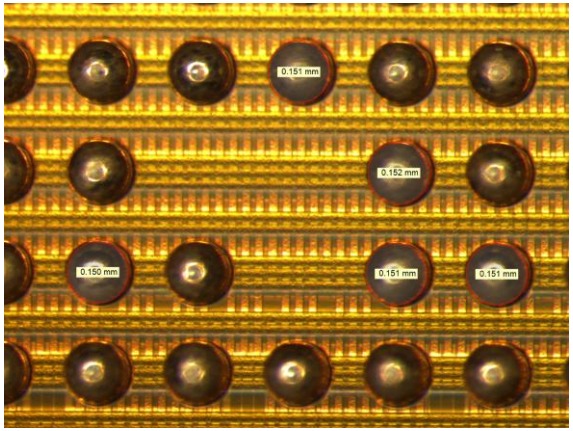


CBC3 is a bare flip-chip die: 811 bumps SAC305 (lead free)





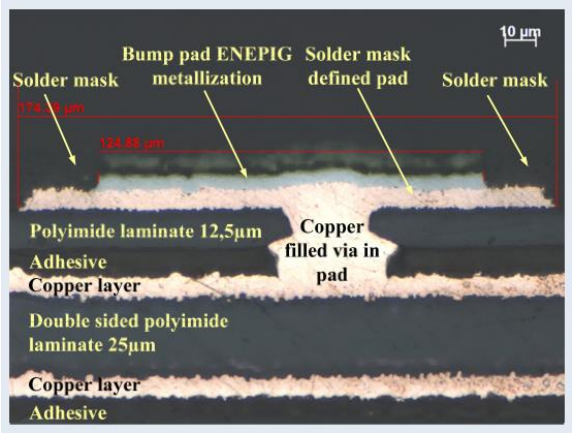
Pitch: 250 µm (X and Y)

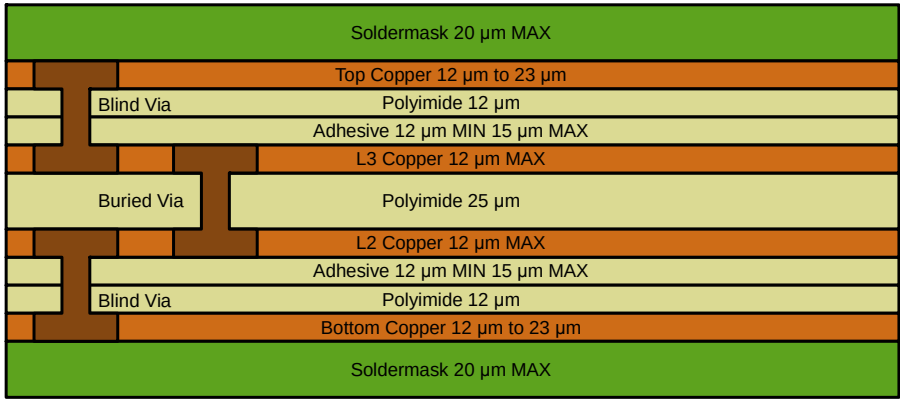


Diameter: 125 to 150 µm

Typical hybrid Design

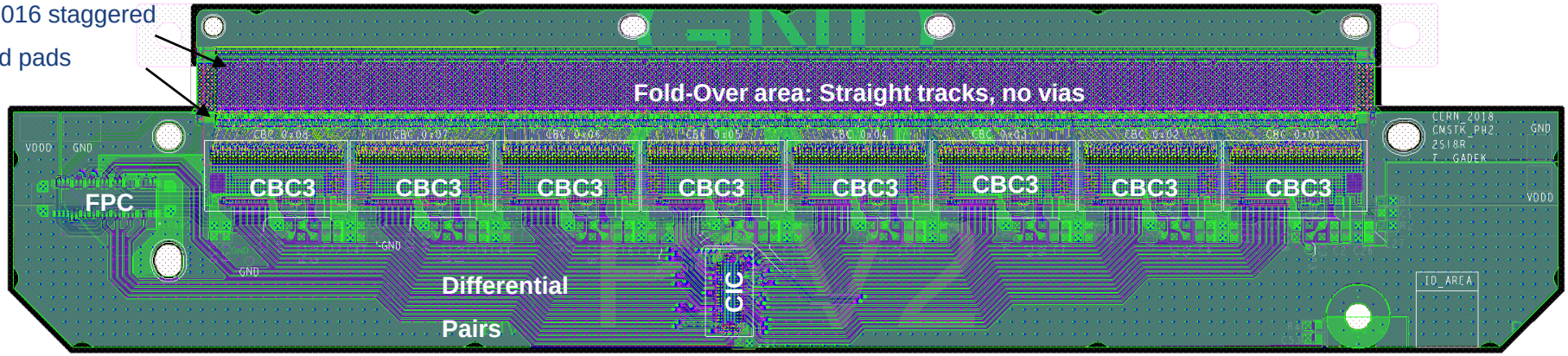
- Build-up: 150 µm thick HDI Kapton in 4 layers, with more than 18.000 blind and buried vias.
- The more than 6500 flip-chip pads are copper-filled via-in-pad microvias, using drill diameters of 25 to 50 µm.
- Copper tracks: 42.5 µm width and spacing are mandatory to fan out the flip-chip bump patterns and to obtain the correct impedance at differential pairs with this thin polyimide stack-up.



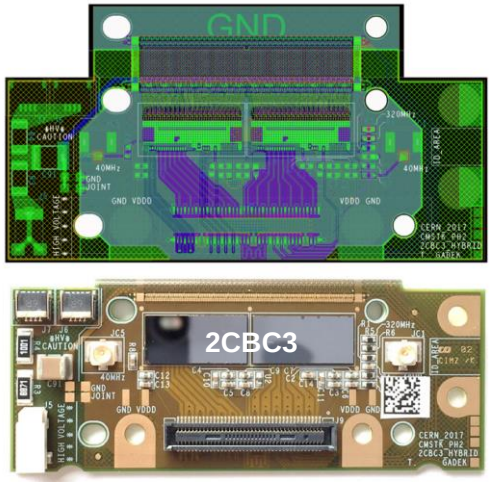


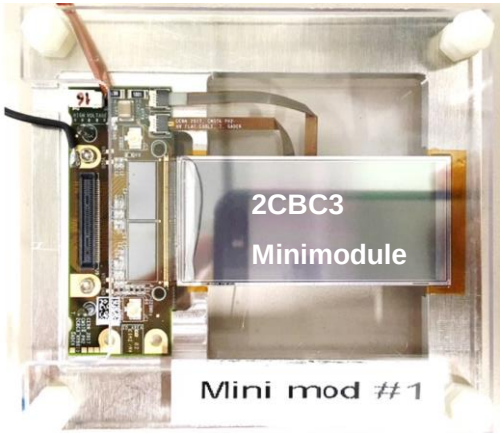
Wirebond pad arrays:

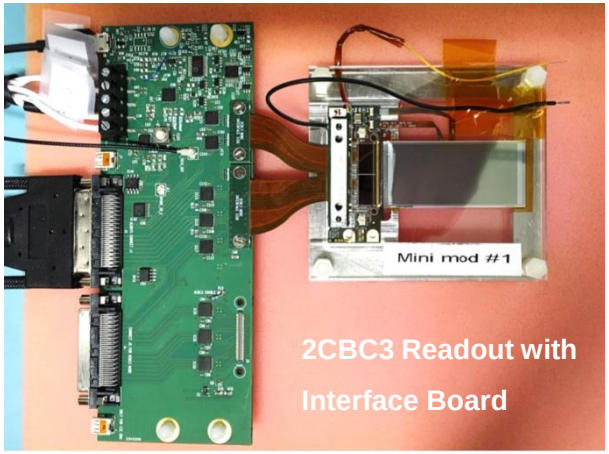
2X1016 staggered bond pads

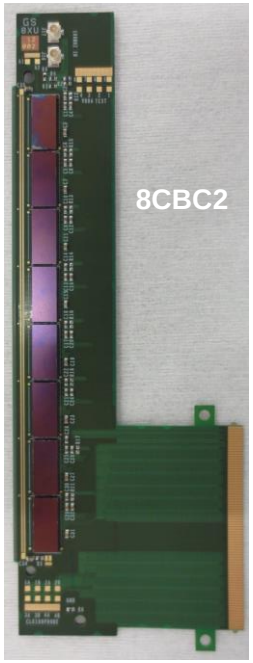


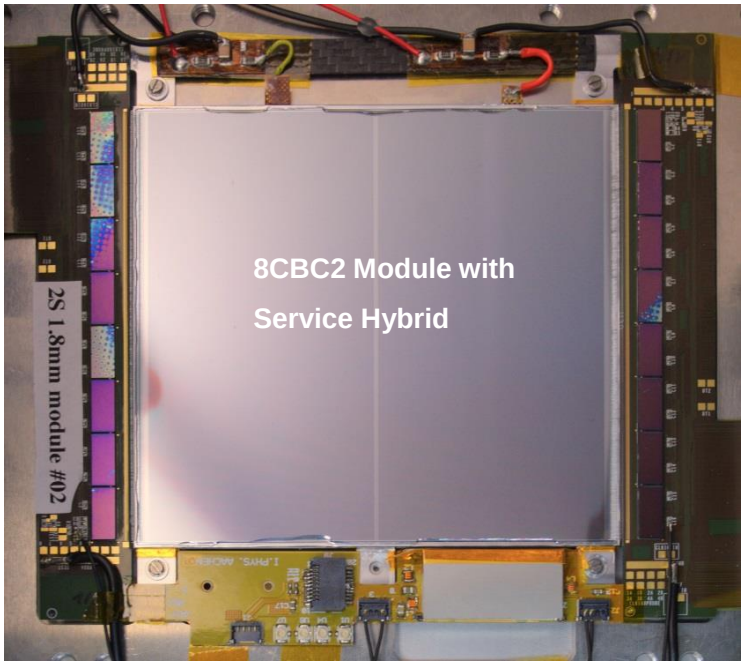
2S Type Hybrids produced



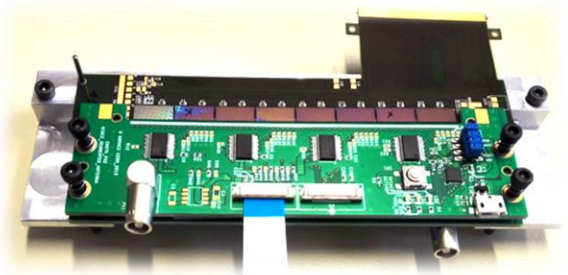


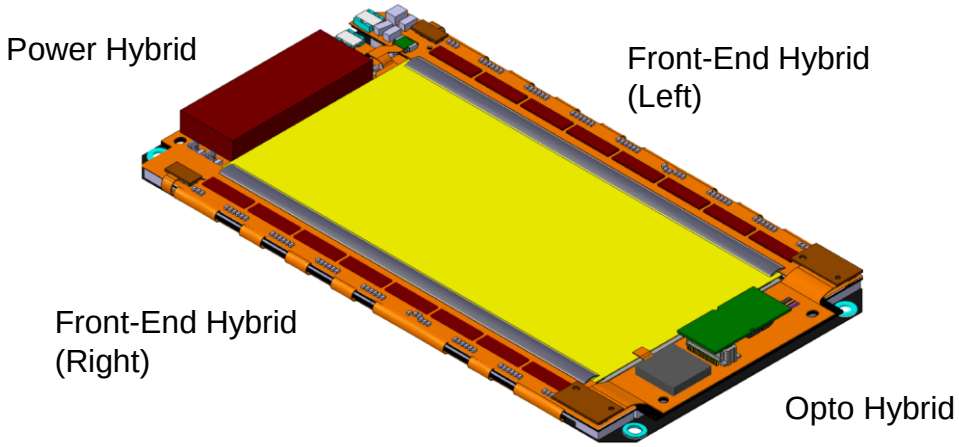




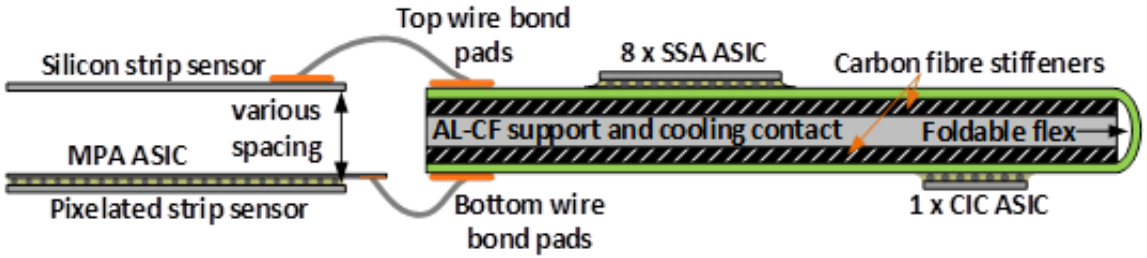


8CBC2 Test System

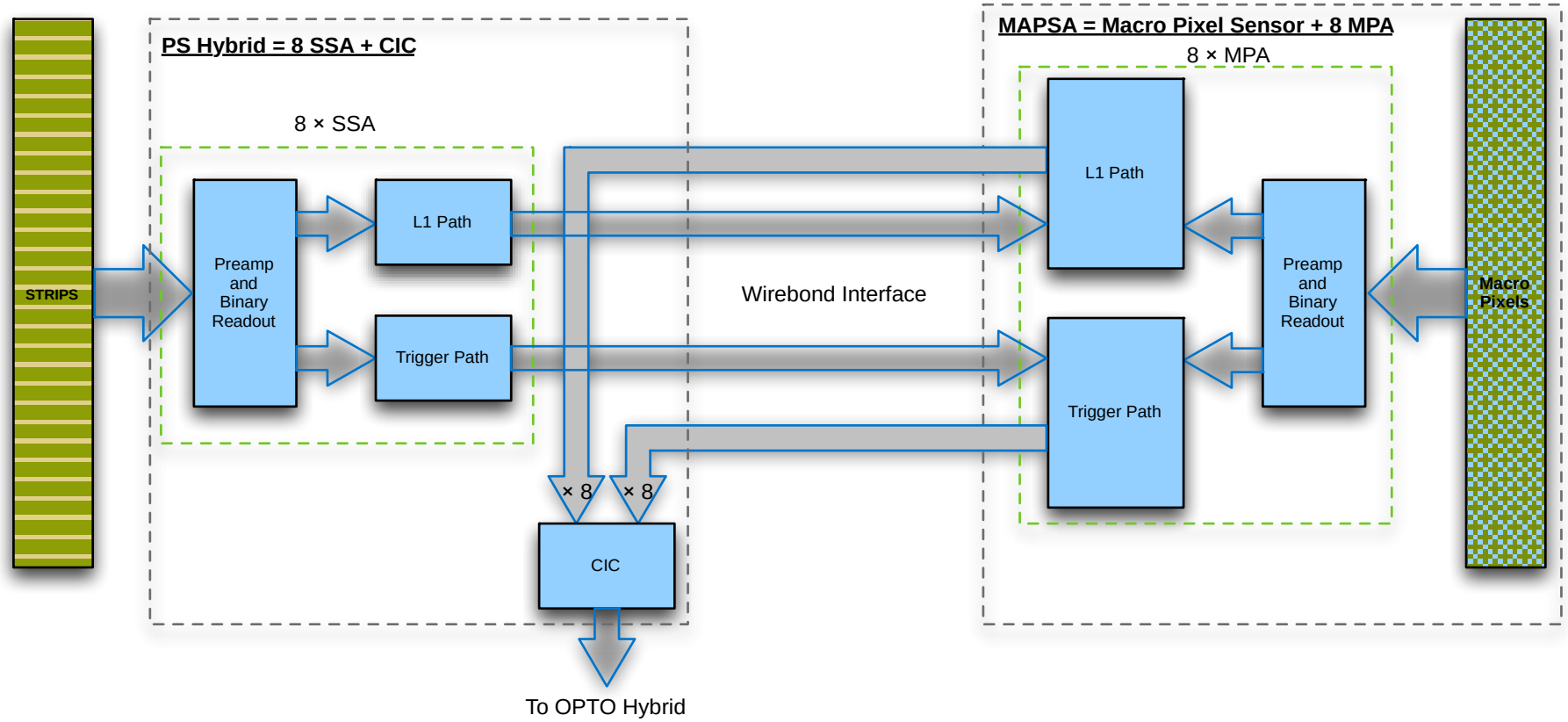




- PS front-end hybrids contain eight SSA front-end ASICs and one Concentrator (CIC).
- The front-end hybrid is a high density interconnect flexible circuit folded around a carbon fibre structure, 10 mm wide, 125 mm long approximately.
- The hybrid is wirebonded to a strip sensor and to a macro pixel sensor.
  - The sensor is bonded to its macro pixel front-end chips that is therefore external from the hybrid.

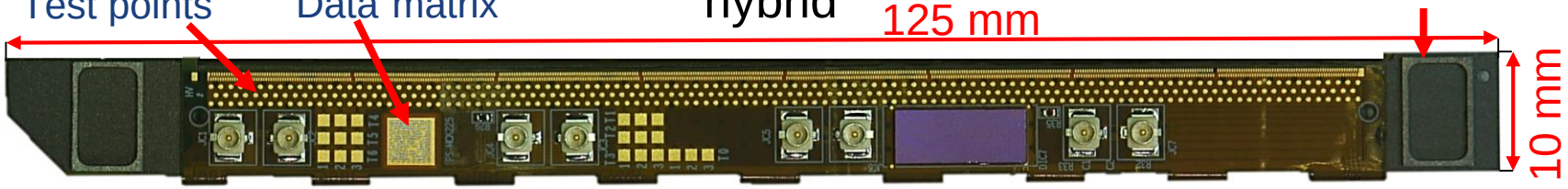


PS Block Diagram



- PS front-end hybrids contain eight SSA front-end ASICs, feeding the off-hybrid MPA front-end ASIC bonded to the macro-pixel sensor.
- The MPA chips combines its data with the SSA data to format stubs and sends it back to the hybrid.
- The formatted data is finally sent to the Concentrator (same as on 2S hybrids), forwarding serialized data towards the Opto hybrid containing the lpGBT and VL+.

Top view of the PS-MCK hybrid



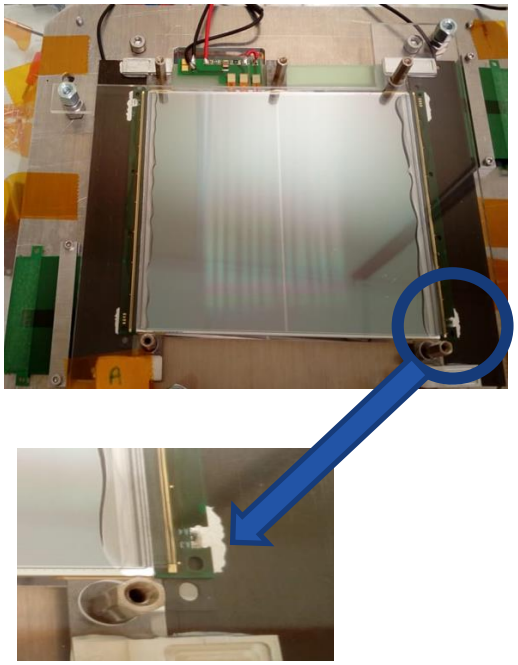
Bottom view of the PS-MCK

- Lack of CIC and SSA chips limited development to a dummy circuit only, used 2 CBC2.
- PS representative geometry and constraints solved by our three contractors, although one required major design modifications.
- Typical difficulties: fold-over without breaking tracks, control of cleanliness, flatness of Al-CF spacers.
- Major difficulty: delamination of flex from stiffeners during reflow. Problem was observed also on the second production batch of 8CBC2 hybrids.

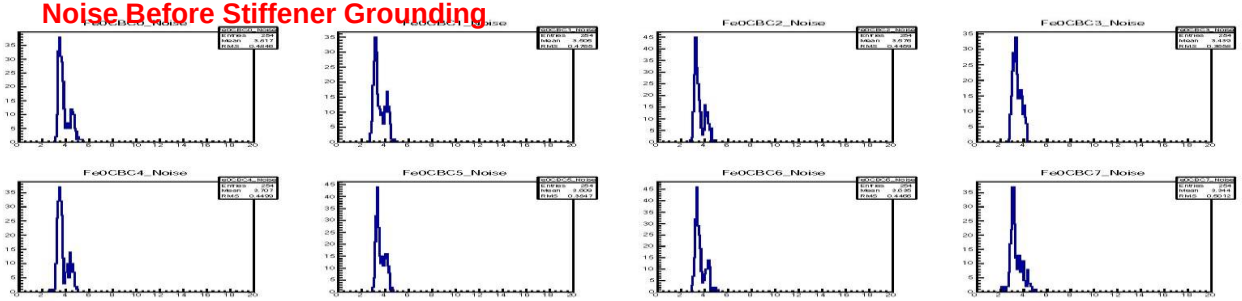
2S Hybrids			
Item	**Description**	**Quantities**	**Prototyped**
2S-FEH-18-L	1.8mm spacing, Left side	8750	--
2S-FEH-18-R	1.8mm spacing, Right side	8750	2CBC2, 8CBC2-P1, 8CBC2-P2, 2CBC3, 8CBC3 (now)
2S-FEH-40-L	4.0mm spacing, Left side	1125	--
2S-FEH-40-R	4.0mm spacing, Right side	1125	8CBC2-4MM

PS Hybrids			
Item	**Description**	**Quantities**	**Prototyped**
PS-FEH-16-L	1.6mm spacing, Left side	990	--
PS-FEH-16-R	1.6mm spacing, Right side	990	3 × PS-MCK (Dummy)
PS-FEH-26-L	2.6mm spacing, Left side	1840	--
PS-FEH-26-L	2.6mm spacing, Right side	1840	--
PS-FEH-40-L	4.0mm spacing, Left side	3650	--
PS-FEH-40-R	4.0mm spacing, Right side	3650	--

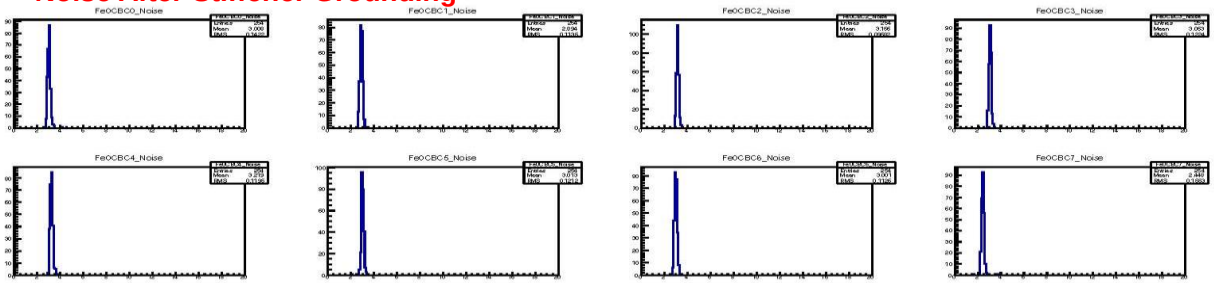
- **Floating carbon fibre material propagates digital noise towards analog inputs**
  - At origin of double trigger effect, then fake hits.
  - Grounding carbon fibre cancels the coupling.
  - Measurements made so far with conductive silver loaded paint succesfull, but paint not easily applicable.



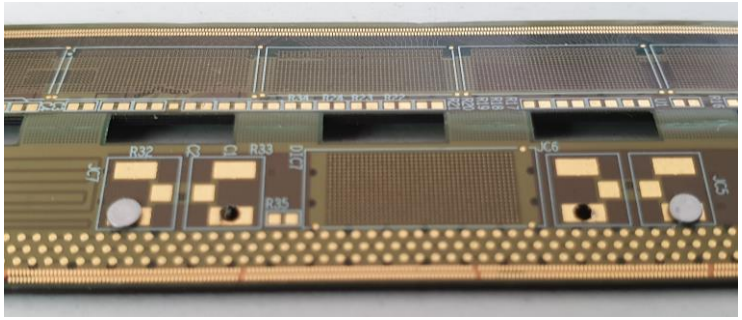
Noise Before Stiffener Grounding

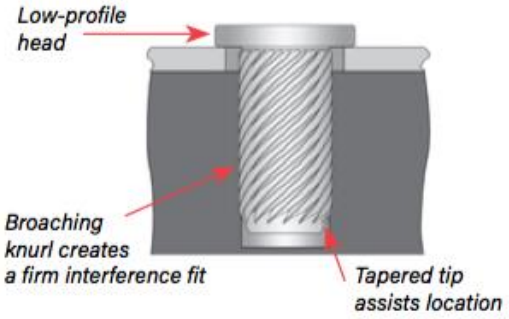


Noise After Stiffener Grounding



- **Proposed alternatives**
  - Silver loaded paint not applicable as is: gets activated, unclear long-term reliability.
  - Co-cured stiffeners: copper mesh embedded into carbon fiber at lamination, most complex solution, difficulty to set a contact between the mesh and the hybrids ground plane.
  - Screw (down to 1.6 mm) with toothed washer is the simplest but large footprint.
  - Press fit micro Inserts, 1.2mm head and 1mm pin diameter is the most compact solution.
- **Integration in 8CBC3**
  - 8CBC3 prepared for screw grounding.
  - Micro inserts are being evaluated on samples.

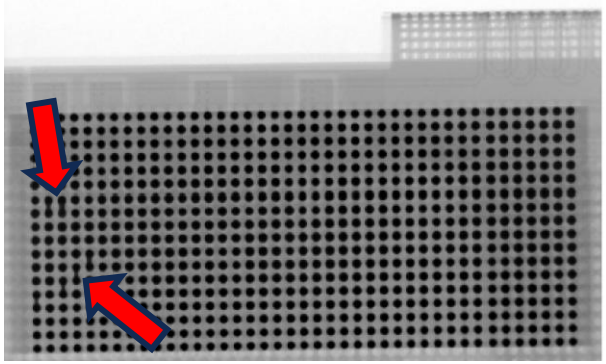




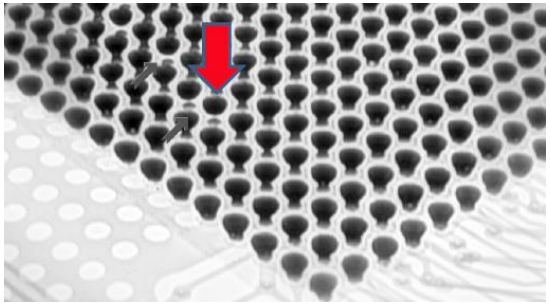
Module's yield depends directly from hybrids production yield

- 2S modules yield → (Hybrids yield)^3
- PS modules yield → (Hybrids yield)^4
- Hybrids yield = 95% implies:
  - 2S module yield of 86% or 13% losses at module assembly if hybrids not screened.
  - PS module yield of 81% or 19% losses at module assembly if hybrids no screened.
  - We need to target more than 98% hybrids yield to contain modules losses below 5%.

Different quality concerns can affect the hybrids



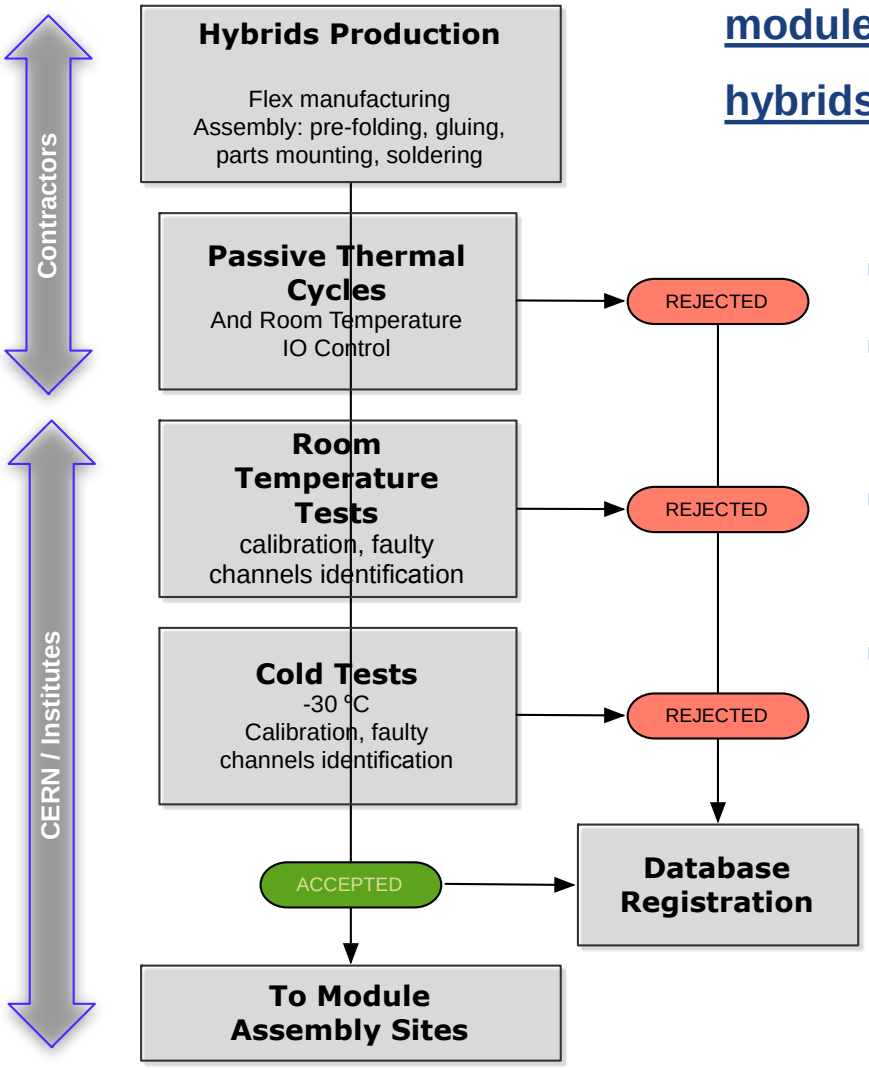
- Non functional dies.
- Damages to flex: broken tracks or vias
- Long term reliability concerns on vias and soldering.
- Non flatness of flex compromising the bump bonding of dies.
- Non flatness of flex compromising the wire bonding to sensors.
- Contamination of bond pads compromising the wire bondability.
- Incorrectly glued spacers compromising the hybrid gluing into modules.



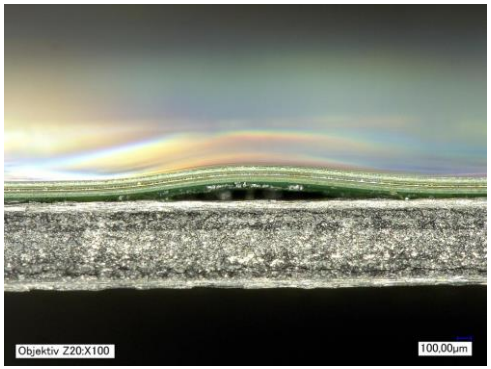
Mandatory qualification of processes

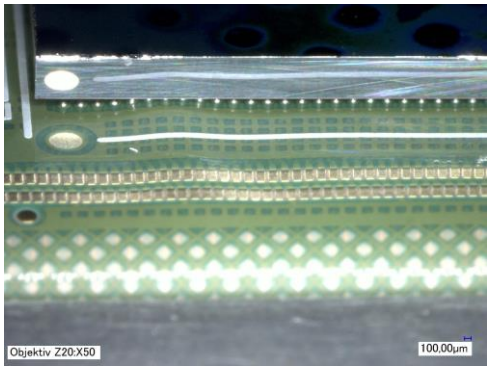
- Assembly procedures must be qualified.
- Hybrids need to be exhaustively tested.

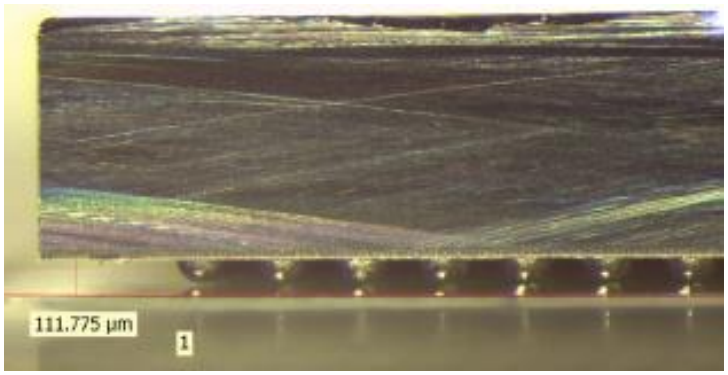
Non functional hybrids can result in high losses at module assembly because of integration of several hybrids per module



- Functional screening at assembly contractor
- Systematic room temperature and cold tests at CERN and collaborating institutes.
- Tracking of power parameters, disconnected, shorted or grounded channels.
- Recording in database for correct tracking at module assembly sites.





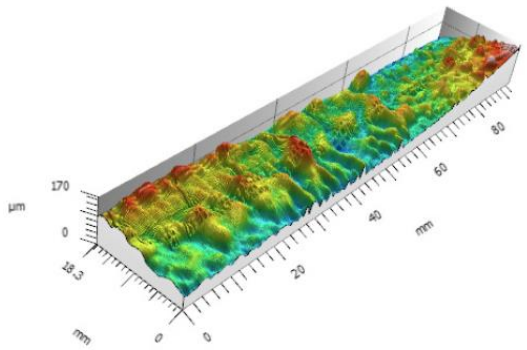


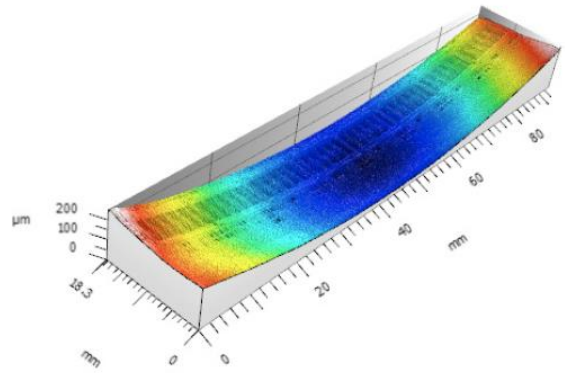
Recent 2S and PS hybrids suffer from warpage and/or bow during assembly process:

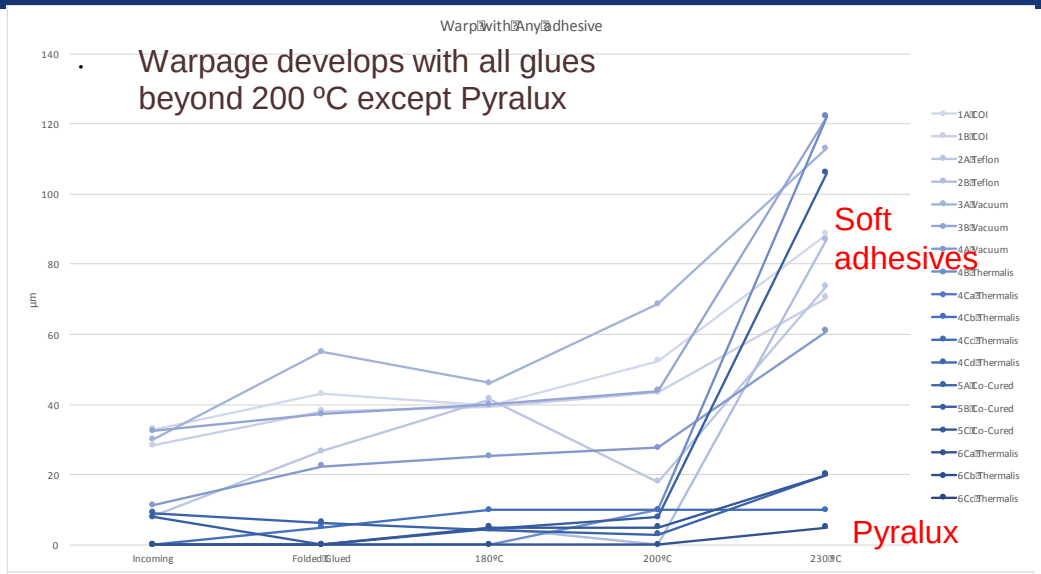
- Reported on latest prototypes: 8CBC2, PS-MCK, by all contractors.
- Related to CTE mismatches (Cu, Kapton, CF)
- Also, soft adhesives used so far are not standing reflow temperatures, but we need to stand lead-free soldering temperatures for ASIC bump compatibility.
- Consequences: the delamination of flex from stiffeners form waves on flex that compromise the soldering of dies and the wire bondability of hybrids.

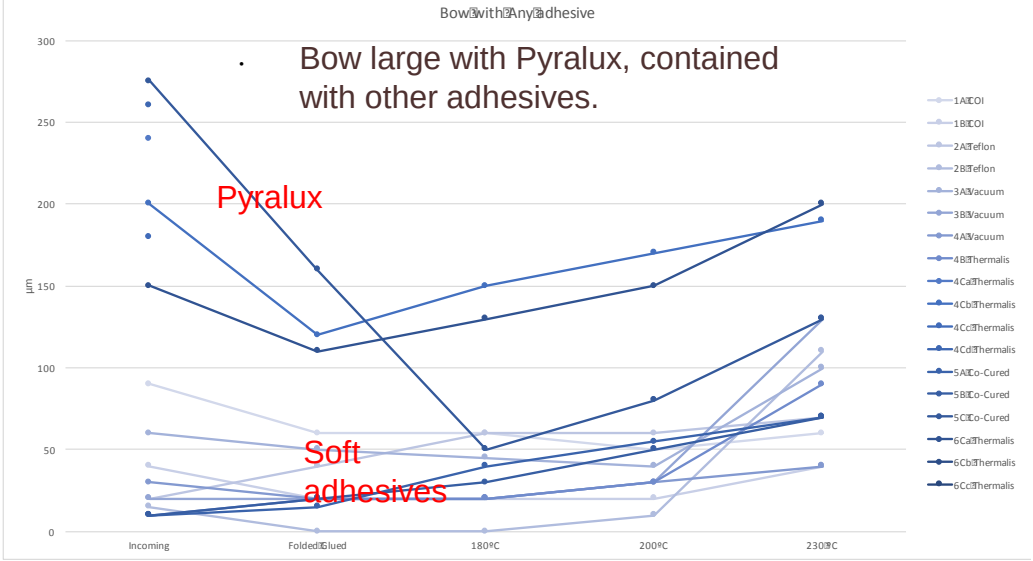
- Specific R&D on lamination process is now ongoing: **Stiffener Test Plan**.

Bow versus Warpage



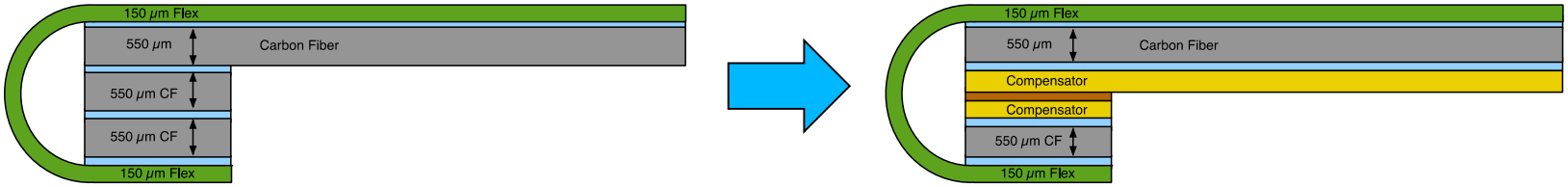






Pyralux = hard acrylic adhesive stands short term 400 ºC.
Soft adhesives = different double sided tapes stand short term 260 ºC max.

- **Influence of stiffener material:**
  - No relevant difference between materials was found between different carbon fibre stiffeners.
- **Influence of adhesive**
  - Pyralux leads to bow but contains very well the warpage : 20 µm max warp.
  - Bow is easier to handle for module assembly: can tolerate up to 100 µm of bow.
  - Warpage compromises the wire bonding and the flip chip bonding: it must be very well contained.
- **Outcome summary from discussions with contractors**
  - First R&D Path:
    - Evaluation of new soft adhesives more suitable to stand high temperatures.
    - Apply plasma etching on soldermask to improve adherence.
  - Second R&D Path: Pyralux and a CTE compensator.



  - FR4 compensator of adequate thickness (thickness, CTE and Young's modules tuning) will balance the CTE mismatch around the flex and make it flat at all temperatures.

- **At this point, few contractors able to cope with HDI layout requirements.**
  - Can manufacture the flex.
  - Can glue stiffeners and do the fold.
  - Can mount the dies.
- **Several hybrids were produced:**
  - Several 2S variant types produced: 2CBC2, 2CBC3, 8CBC2, 8CBC3, enabled studies of the assembly process and the verification of front-end chip performance.
- **Quality is a major topic:**
  - Ongoing studies of stiffener gluing to be compatible with reflow, this combines adhesive material, stack-up and reflow profiles.
  - Many other topics are being addressed also: see Mark's section here after.
    - Long term reliability of flex construction.
    - Integration of test features within the hybrid: integrated antenna.
    - Detection of opened, shorted and grounded input channels.
    - Preparation for full hybrids testing during production.

Reliability and quality check of hybrids and interconnect structures

M. Kovacs, B. Allongue, F. Andre, G. Blanchot, T. Gadek, R. Gajanec

Contact: mark.istvan.kovacs@cern.ch

The long term reliability of the hybrid assemblies and the modules is an important concern. Flip-chip ASICs and high density interconnect flex circuits were not used in the detectors before, therefore it is important to test the reliability of these structures.

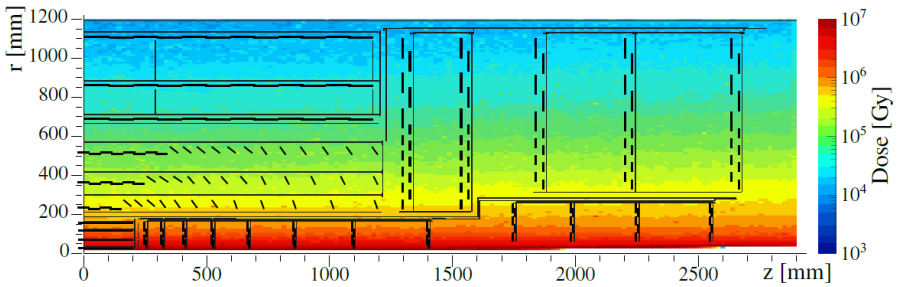
Test coupons were added to several hybrid production panel:

- 8CBC2 4mm (#1).
- 8CBC2 1.6mm (#3).
- PS-MCK all three versions (#2).
- Connector test coupons were manufactured separately.

The Tracker environment where the hybrids will operate:

- Controlled low humidity.
- Coolant temperature at around -35 °C, operation temperature at around -20 °C.
- A few shutdowns of the cooling plant per year, a few power cycles per year.
- High radiation dose for PS modules, lower for 2S modules (56 Mrad max [1]).
- Operation in a strong static magnetic field.

The planned lifetime of the electronics is **15 years**. The modules must remain fully operational during this period.

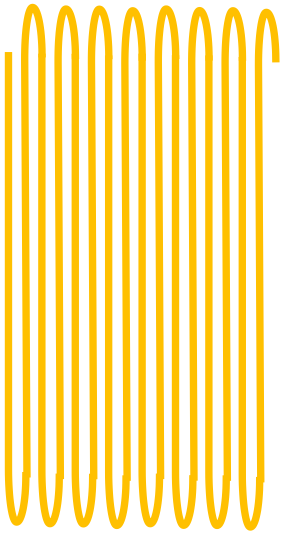


Expected radiation levels in the CMS PH-2 tracker [1].

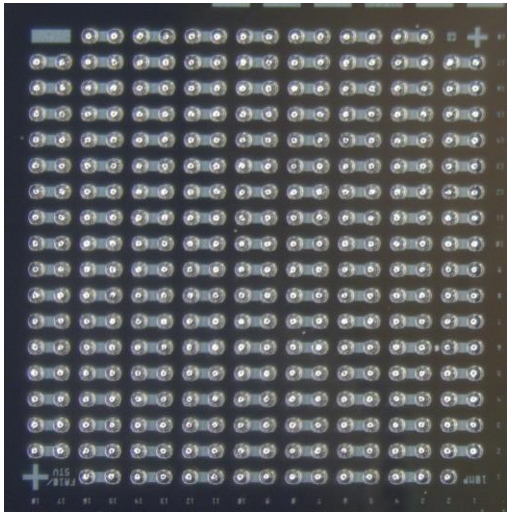
[1]: The Phase-2 Upgrade of the CMS Tracker Technical Design Report CMS-TDR-17-001

Parts of the circuits where failure might occur:

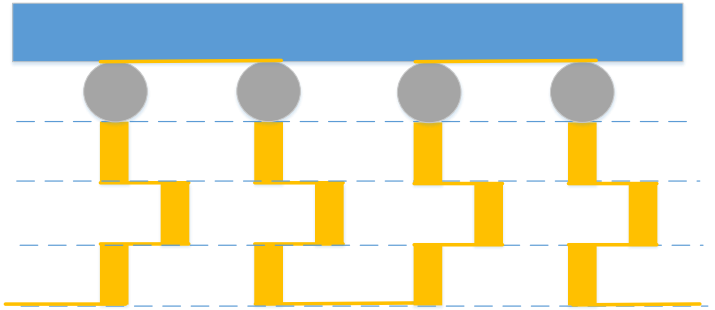
- Solder connections of surface mount components (~6500 bump bonds / hybrid).
- Via structures (~18000 microvias / hybrid).
- Fine traces (down to 40 µm).



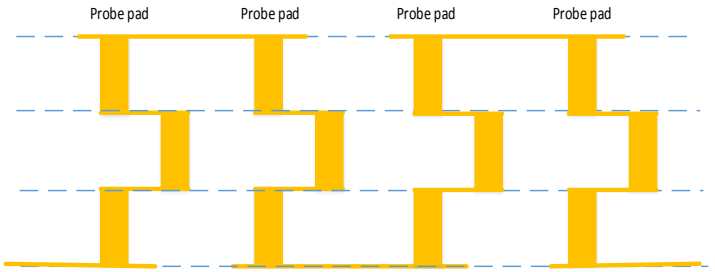
Fine line test structure with 45 µm lines.



Daisy-chain test flip-chip with 254 µm pitch.



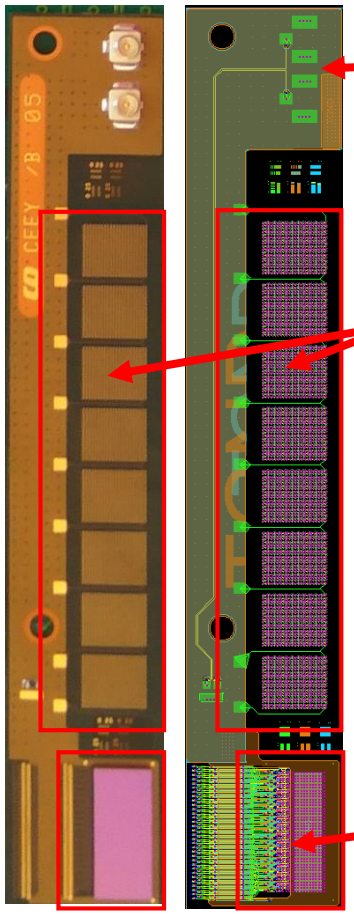
Flip-chip test daisy-chain with via-in-pad structure.



Via daisy-chain test structure.

Test coupons – Design of the different coupons

Coupon #1 only one manufacturer.



Impedance test (not used in the test).

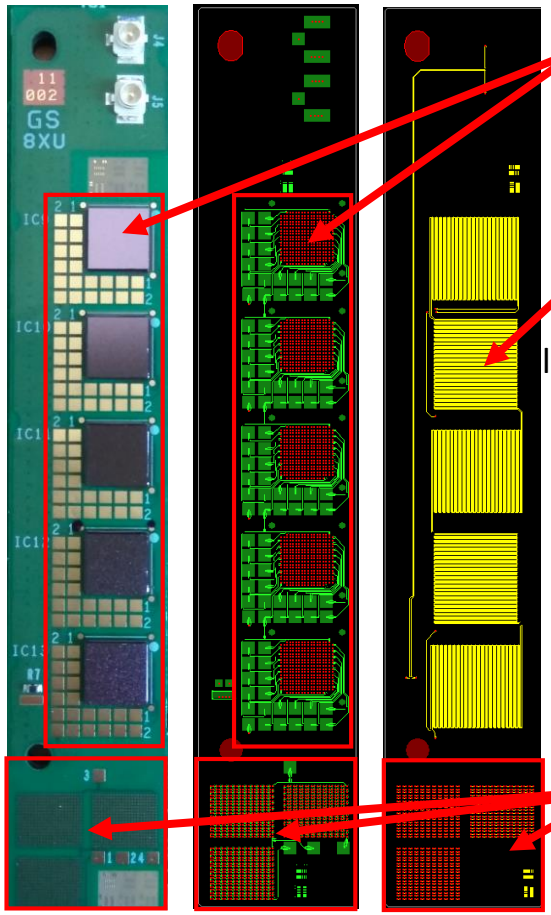
Via daisy-chain structures with 9504 vias staggered.

Dummy flip-chip for assembly test.

Instance Design

Some were irradiated @ 1MGy.

Coupon #3 only one manufacturer.



Flip-chip daisy-chain structure with 5 x 317 bumps.

Fine line test structure with two parallel nets and 45µm/50µm linewidth/spacing 1.6m total length.

Via daisy-chain structures with 3564 vias staggered.

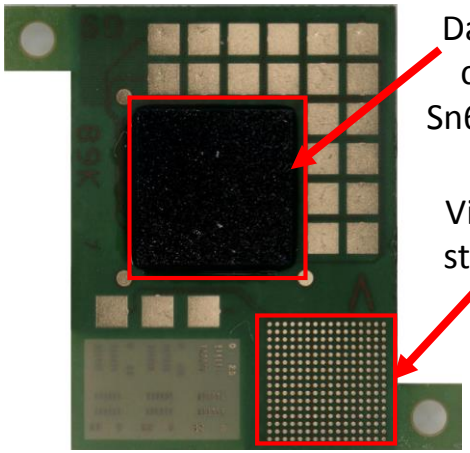
Instance Design top layer Design bott. layer

Flip-chips with SAC305 bumps.

Test coupons designed by M. Kovacs.

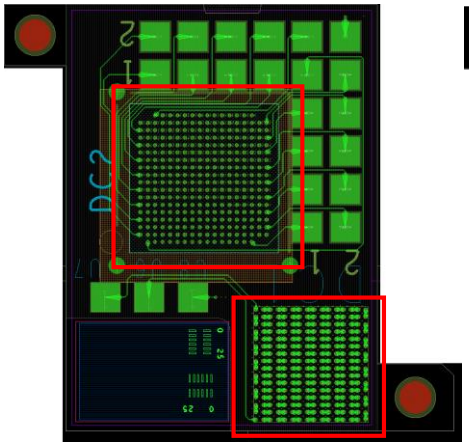
Test coupons – Design of the different coupons

Coupon #2 from three different manufacturers.

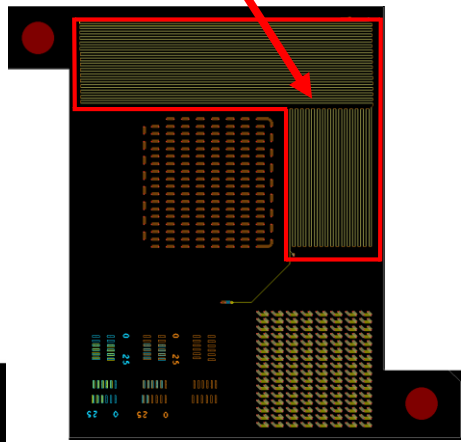


#2 Type test coupon instance

1.4m long fine line test structure is under the probe pads.



Top layer design of all #2 type coupons.



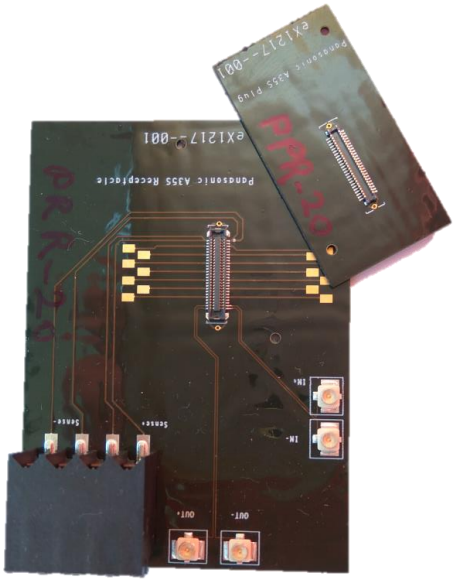
Inner layer design of all #2 type coupons.

- Three different circuit manufacturers and assemblers.
- Flip-chips with eutectic Sn63Pb37 balls.
- 2 sets manufactured with solder-mask defined pads.
- 1 set manufactured with copper defined pads.
- The flip-chip assembly on the #2 V coupons failed.

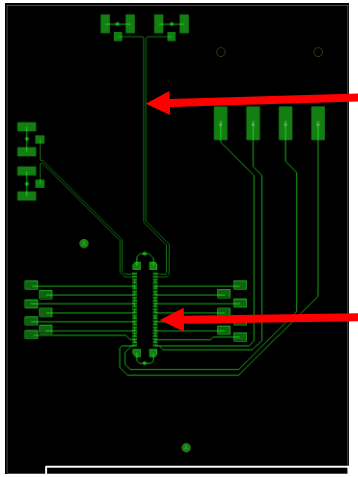
Test coupons designed by M. Kovacs.

The Panasonic A35S connector family is planned to be used for the service hybrid to front-end hybrid data connection.

Connector test coupon from one manufacturer.



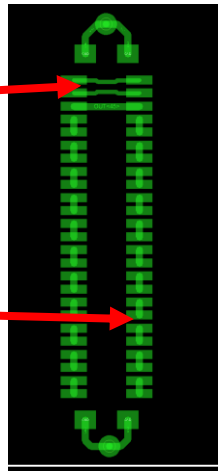
Connector test coupons.



Socket design.

Effect on differential signals measured.

44 contact pairs daisy-chained.



Plug design.

- 10 coupons were irradiated with 1MGy Gamma ray.
- 10 coupons were not irradiated.
- 5 coupons from each group had 5 connect-disconnect cycles before the tests.

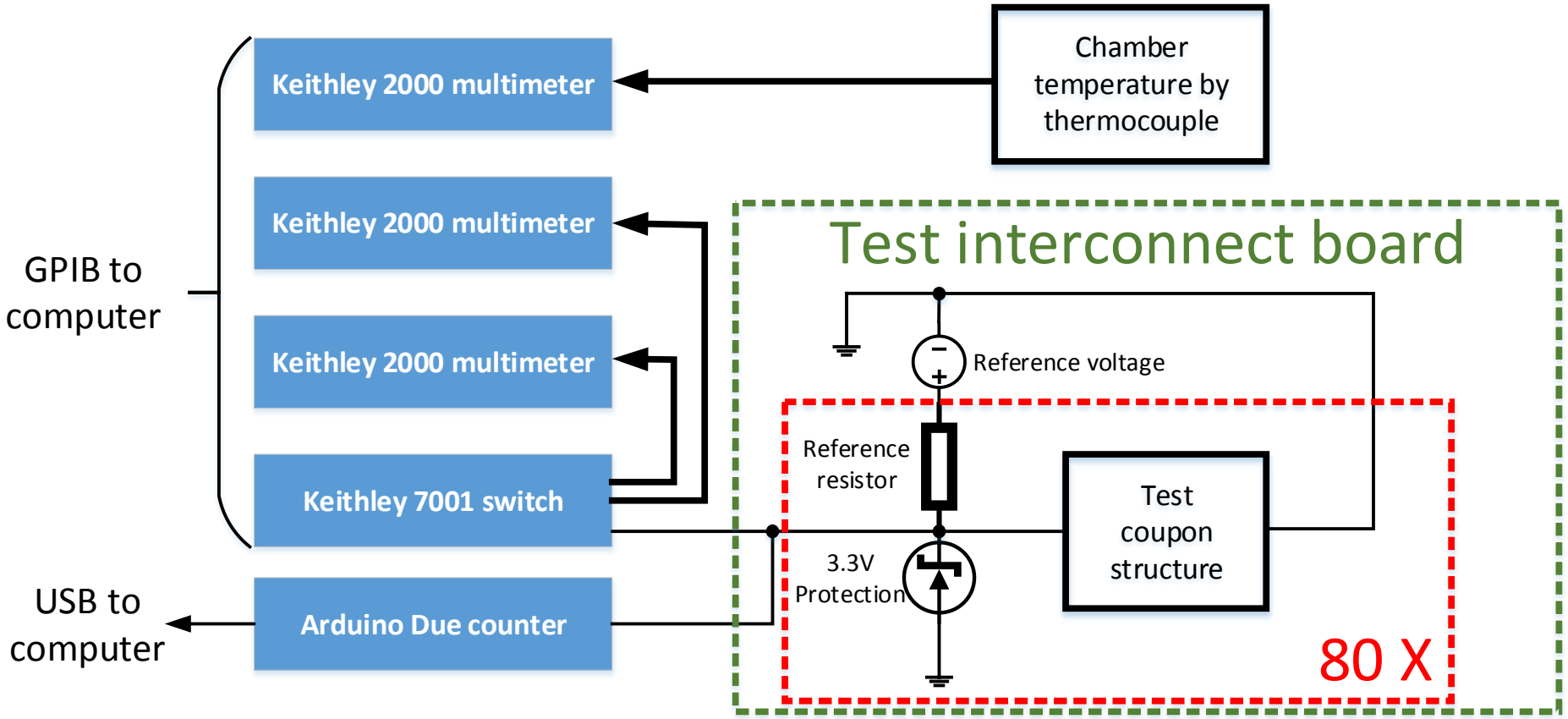
Test coupon designed by B. Allongue.

Test coupons – Summary of test objects

Coupon type	Flip-chip DC	Via DC	Fine line	Other	Pieces
Coupon #1	No	Yes	No	Irradiated	3
Coupon #1	No	Yes	No	-	4
Coupon #2V	No	Yes	Yes	SnPb, SM defined	11
Coupon #2E	Yes	Yes	Yes	SnPb, Cu defined	8
Coupon #2E	No	Yes	Yes	SnPb, Cu defined	6
Coupon #2A	Yes	Yes	Yes	SnPb, SM defined	14
Coupon #3	Yes	Yes	Yes	SAC305*, SM defined	17
Coupon #3	No	Yes	Yes	-	11
Conn. coup.	-	-	-	Irradiated, 5 cycles	5
Conn. coup.	-	-	-	Irradiated, no cycles	4
Conn. coup.	-	-	-	5 cycles	5
Conn. coup.	-	-	-	no cycles	5

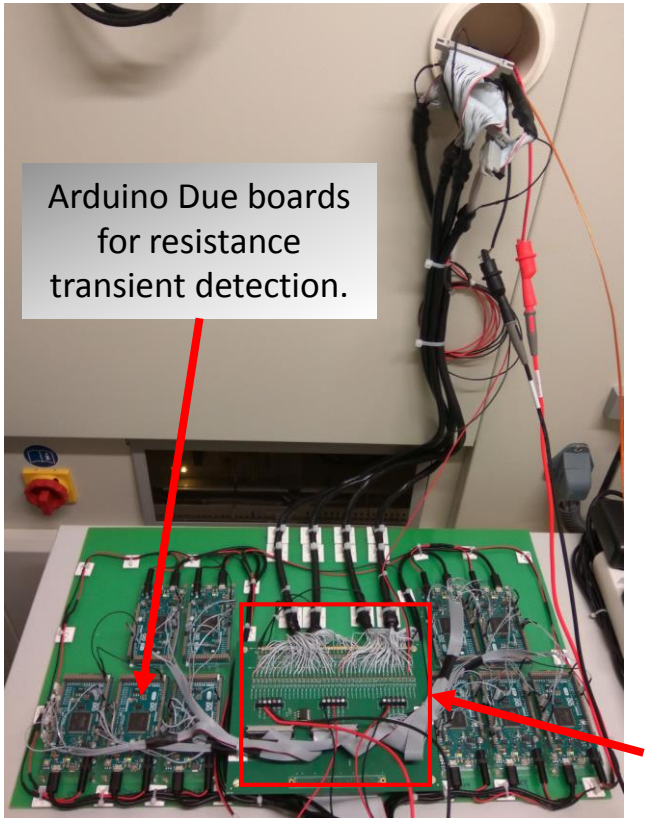
*SnPb solder alloy was applied during assembly for the following coupons: (2005,3005,7007,13007).

The test system has two functional parts. A static resistance measurement and a dynamic resistance measurement system. The dynamic system uses Arduino Due boards to count the duration of resistance transients above 60 Ω. The static system uses Keithley multimeters and a switch to measure the resistance of 80 channels.

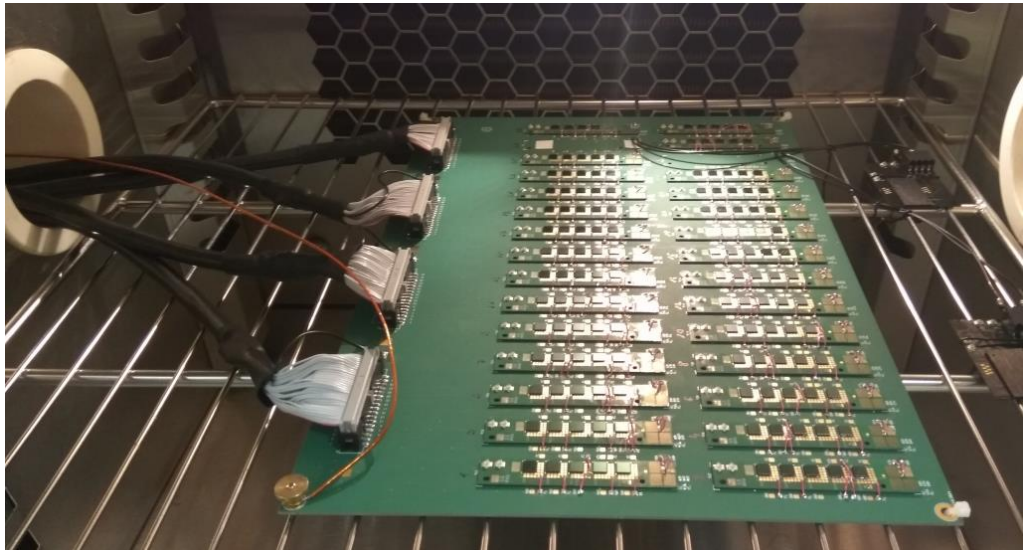


Hardware design by M. Kovacs, software development by F. Andre

In order to be compatible with different test coupon runs, an interconnect board was designed which is compatible with all the test coupons. Shielded 34 pin ribbon cables with IDC connectors interconnect the test chamber's inner part to the system.



Reliability test system.



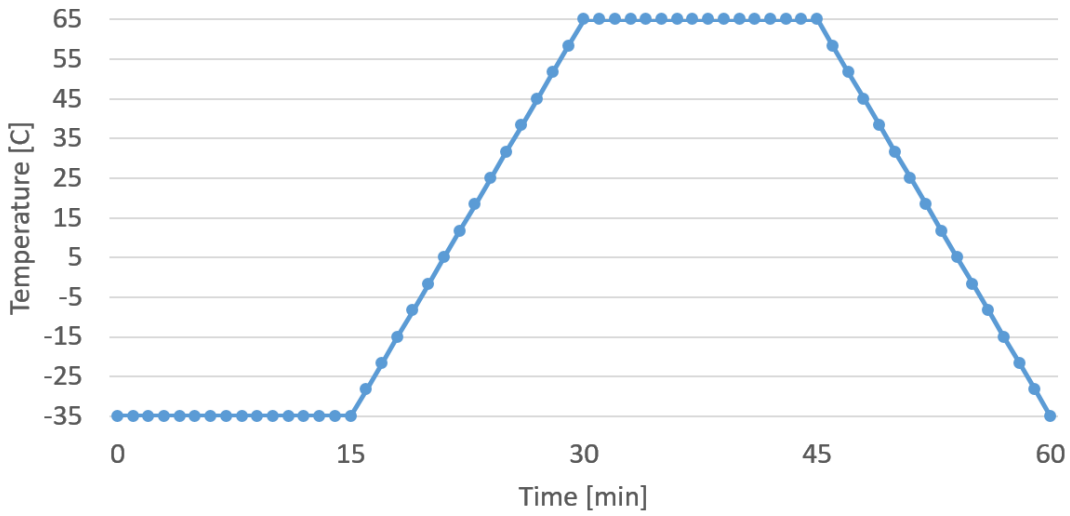
Test coupon interconnect board.

Reference voltage is generated on-board and reference resistors are mounted for each channel. The reference voltage and the coupon voltage drop is measured by the Keithley 2000 multimeters.

Test coupon interconnect board designed by R. Gajanec.

The test thermal cycle is chosen to run from -35 °C to 65 °C with 15 minutes dwell time and ~7 °C / min temperature ramp. The thermal chamber used for the tests is a Climats Excal model. Dry air injection was activated to avoid condensation on the test specimens. The test system and the thermal cycle was set up using the guidelines from IPC-SM-785.

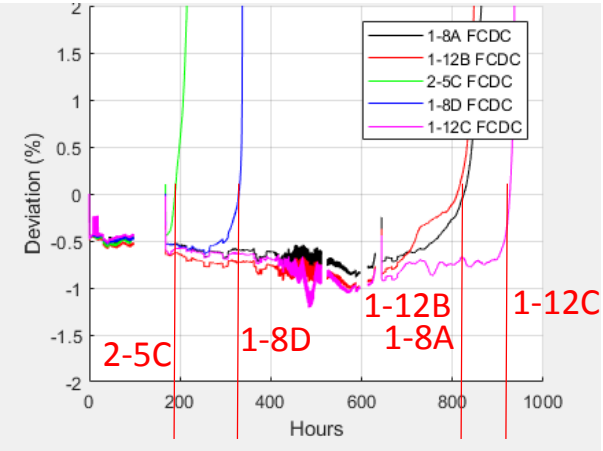
Similar climatic chamber to the one used for the tests [2]



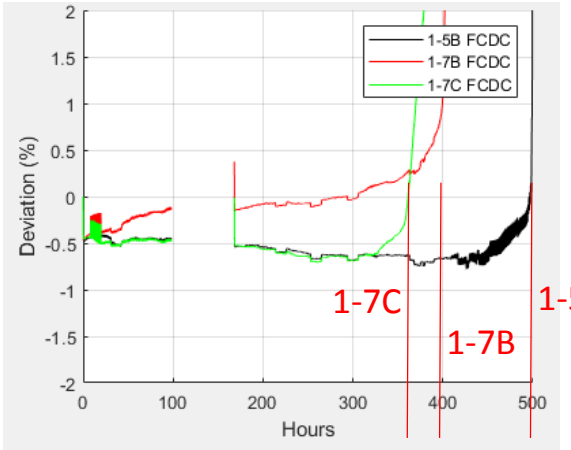
Temperature profile of one thermal cycle.

[2] Source: www.climats-tec.com

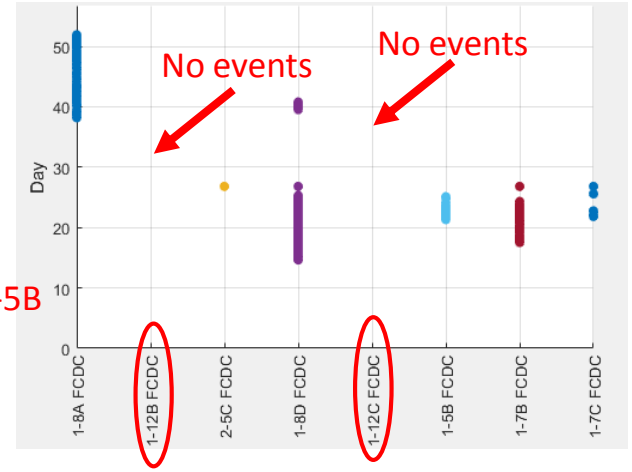
Static resistance deviation coupons #2 E



Static resistance deviation coupons #2 E

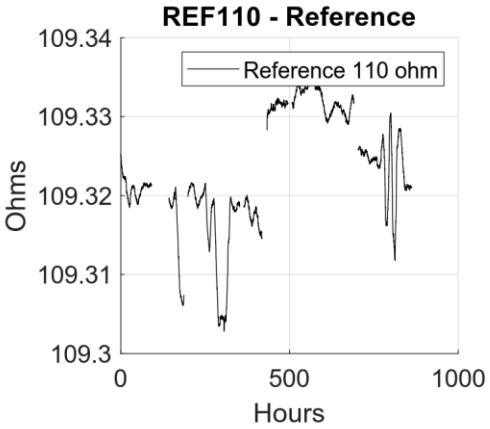


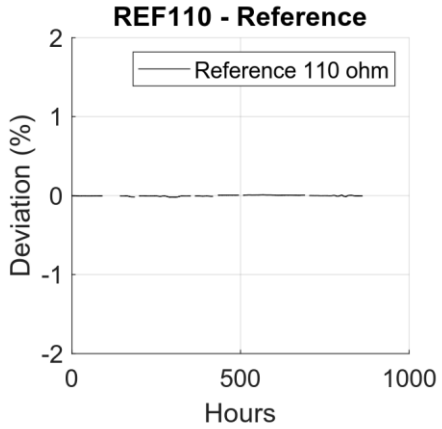
Resistance transients > 1µs coupons #2 E



The resistance transient detection did not indicate failures before they were visible by the static measurement. Some failures were not indicated.

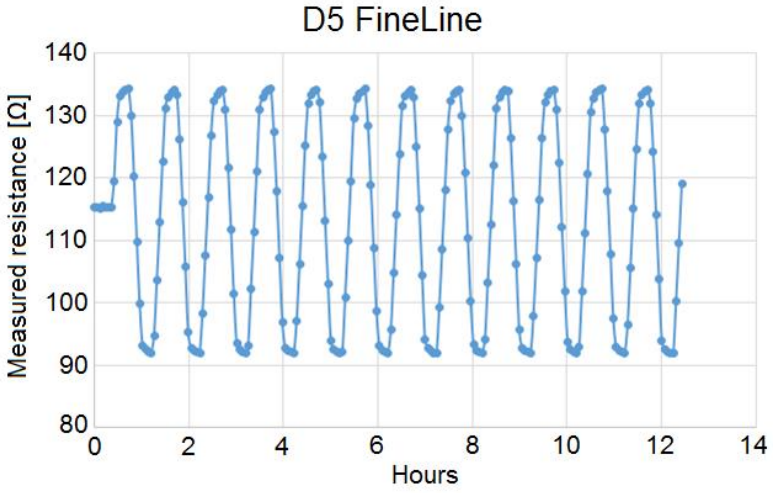
The test system is equipped with three reference channels with 110 Ω reference resistors. The relative resistance measurement was very precise, less than 0.1% deviation was observed (air-conditioned room).



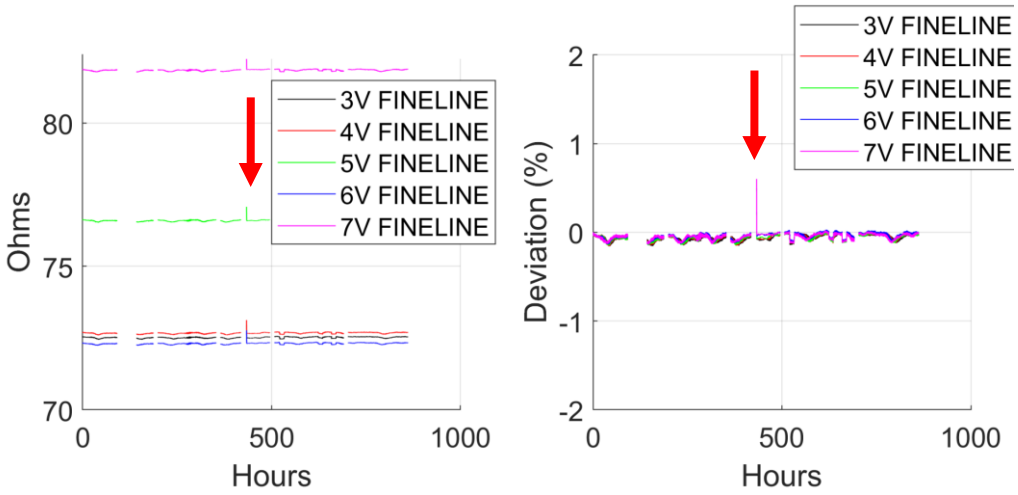


Resistance of reference is recorded for the full test duration.

The test system saves the data in CSV files. It measures the resistance of all 80 channels every 5 minutes. During 1000 thermal cycles it generates ~1 million measurement points. A Matlab script was created to load, sort and plot the data.



Resistance fluctuation caused by the temperature change.



Small deviation caused by the absolute temperature change.

As the resistance of the test coupons is changing in function of the temperature, the resistance is averaged based on 144 measurement points. This averaging method relies on the absolute temperature of the cycles and it can drift with the absolute temperature of the chamber.

Test software design by G. Blanchot.

Test results summary

Via test structures	Failed at start	Failed after 100 cycles	300 cycles	500 cycles	700 cycles	1000 cycles	Note
Coupon #1	0/5	0/5	0/5	0/5	0/5	0/5	
Coupon #1 Irradiated	0/3	0/3	0/3	0/3	0/3	0/3	
Coupon #2A	1/14	1/14	2/14	2/14	2/14	2/14	
Coupon #2V	0/11	0/11	0/11	0/11	0/11	0/11	15V slight incr. (4%)
Coupon #2E	0/14	0/14	0/14	0/14	1/14	1/14	
Coupon #3	1/28	2/28	2/28	2/28	2/28	2/28	
Fine line test structures	**Failed at start**	**Failed after 100 cycles**	**300 cycles**	**500 cycles**	**700 cycles**	**1000 cycles**	**Note**
Coupon #2A	1/14	1/14	2/14	2/14	2/14	2/14	
Coupon #2V	0/11	0/11	0/11	0/11	0/11	0/11	
Coupon #2E	1/14	1/14	1/14	1/14	1/14	2/14	
Coupon #3	0/28	0/28	0/28	0/28	0/28	0/28	
Flip-chip test structures	**Failed at start**	**Failed after 100 cycles**	**300 cycles**	**500 cycles**	**700 cycles**	**1000 cycles**	**Note**
Coupon #2A	0/14	0/14	0/14	0/14	0/14	0/14	Sn63Pb37 bumps SM-def.
Coupon #2E	0/8	0/8	1/8	5/8	5/8	8/8	Sn63Pb37 bumps Cu-def.
Coupon #2V	14/14	-	-	-	-	-	Assembly failed.
Coupon #3	2/17	5/17	8/17	10/17	11/17	11/17	SAC305, mixed paste
Connector test coupons	**Failed at start**	**Failed after 100 cycles**	**300 cycles**	**500 cycles**	**700 cycles**	**1000 cycles**	**Note**
Conn A35S IRR 5CYC	0/5	0/5	0/5	0/5	0/5	0/5	
Conn A35S IRR No CYC	0/4	0/4	0/4	0/4	0/4	0/4	1 slightly increased
Conn A35S 5CYC	0/4	0/4	0/4	0/4	0/4	0/4	
Conn A35S No CYC	0/5	0/5	0/5	0/5	0/5	0/5	2 slightly increased

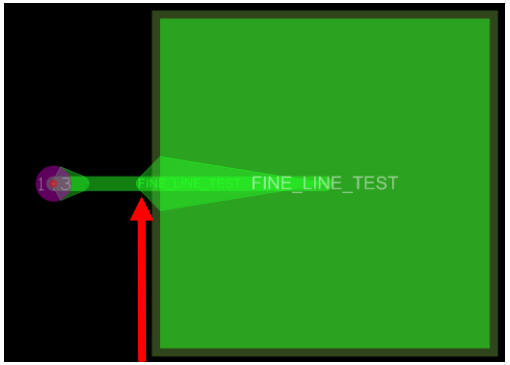
When a test structure is considered as broken/failed, it is important to analyze the failure method. Based on the nature of the failures, they can be grouped in four categories:

- Design problem.
- PCB manufacturing problem.
- Assembly problem.
- Via metallization or solder joint fatigue.

Design, PCB manufacturing and assembly problems can be fixed in the future if they are found during the reliability tests. Fatigue failures are related to the applied technology and materials and they determine the expected product lifetime. For lifetime analysis only fatigue failures can be considered.

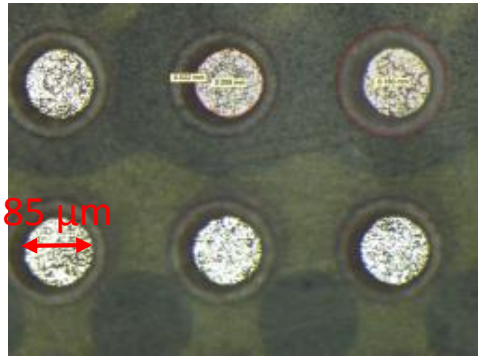
Types of failures found

Design problem

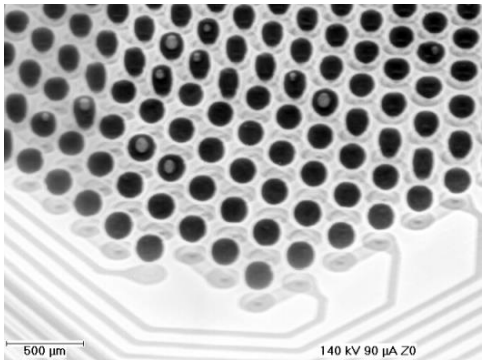


The fine trace can crack close to the solder pad.

PCB manufacturing problem

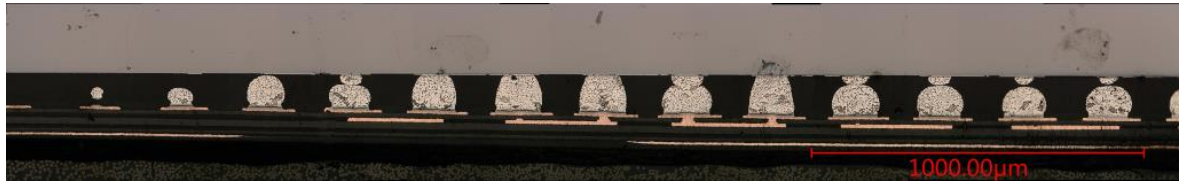


Soldermask opening was not tuned to SM thickness.

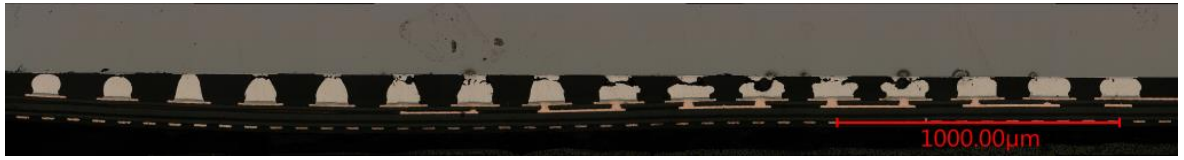


Solder joints could not form between the PCB and ASIC.

Assembly and design problem



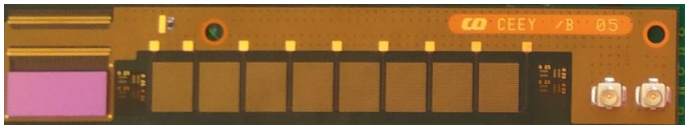
SnPb solder paste was used to assemble ASICs with SAC305 bumps.



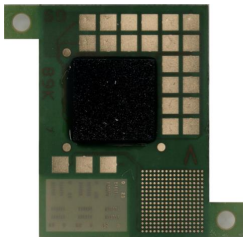
Substrate warps due to CTE mismatch during reflow.

Types of failures found

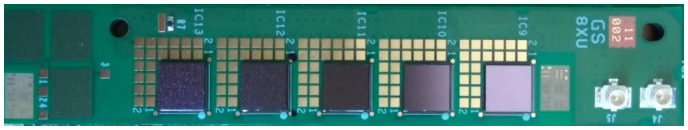
Coupon #1



Coupon #2



Coupon #3



Coupon type	Solder pad fine trace crack	Too small soldermask opening	Warpage issue during assembly	Not yet investigated/ unknown
Coupon #2A via daisy-chain	2			
Coupon #2E via daisy-chain	1			
Coupon #3 via daisy-chain	2			
Coupon #2A fine line	2			
Coupon #2E fine line	2			
Coupon #2V flip-chip daisy-chain		14		
Coupon #2E flip-chip daisy-chain				8
Coupon #3 flip-chip daisy-chain			11	

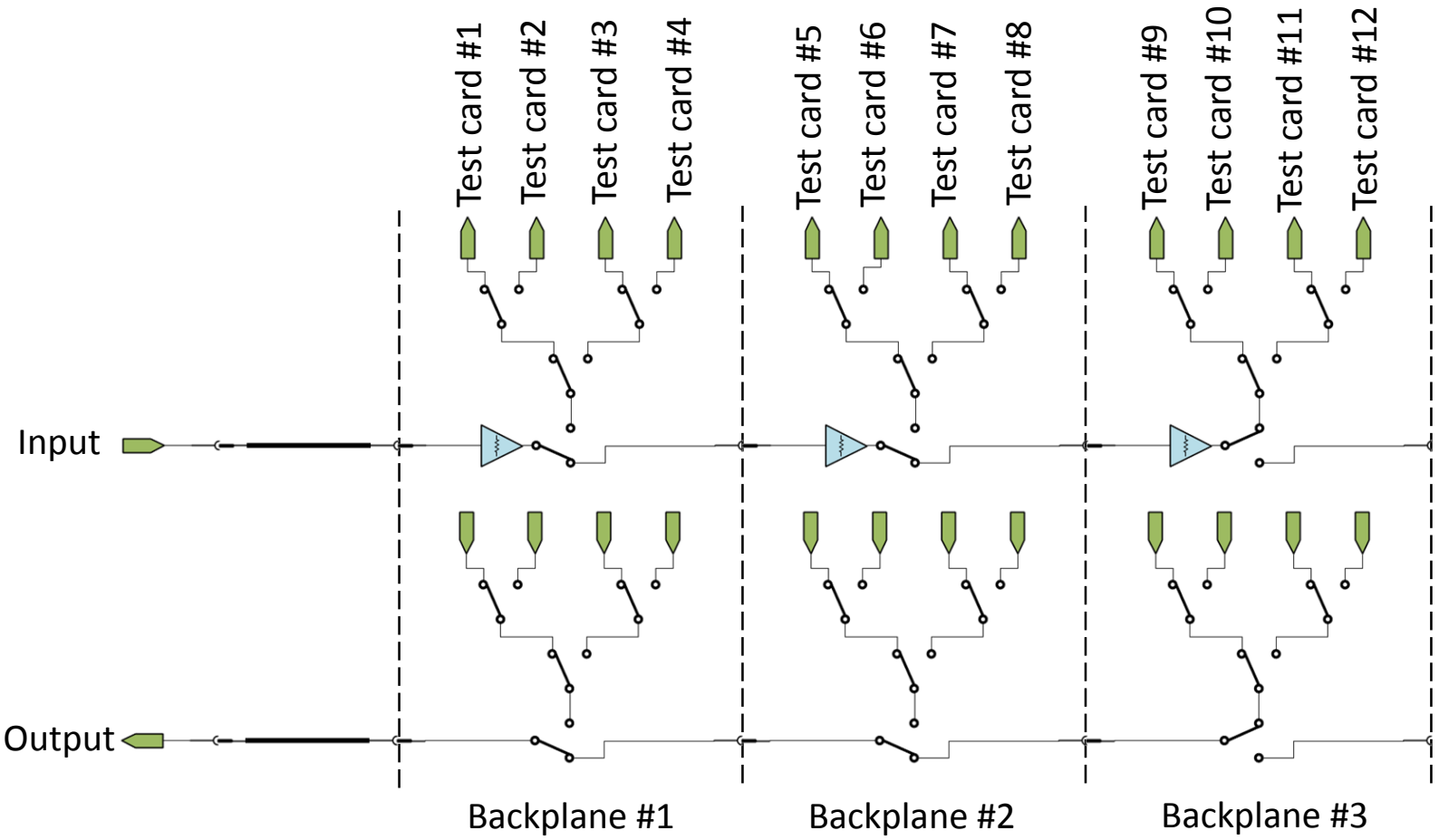
The reliability testing of test coupons will be one part of the production quality check. Production-scale functional testing is also required for the front-end hybrids. A test system is under development to allow for large scale testing of:

- The bump bonding connectivity of the ASICs.
- The functionality of the hybrids from -35°C to +65°C.
- Early failures occurring during the thermal cycles.

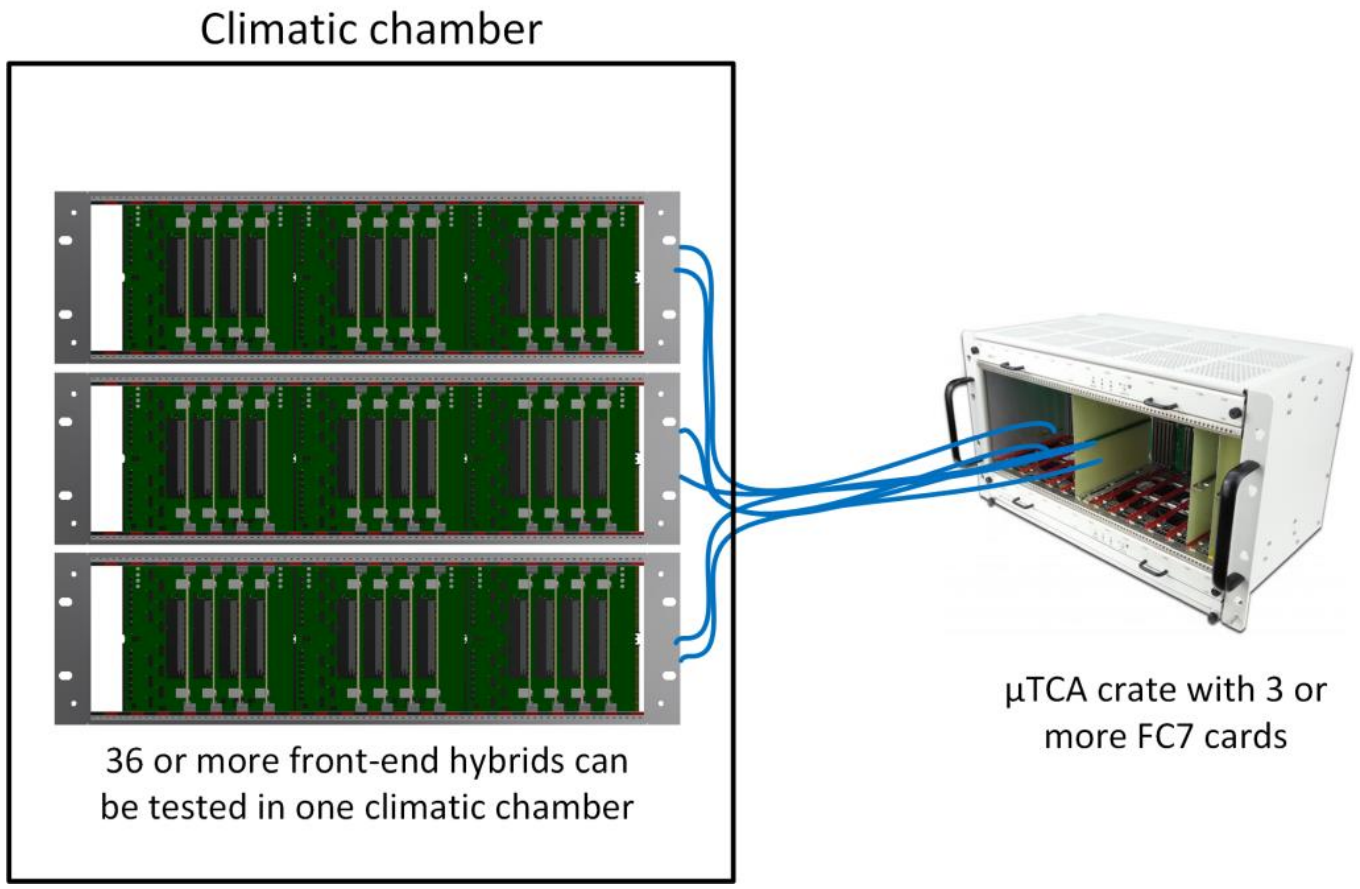
The system is designed to be:

- **Modular** – Allow for low volume testing at collaborating institutes.
- **Universal** – Enable the testing of all the hybrids foreseen for the Phase-2 upgrade.
- **Compatible** – With already developed testing infrastructure (FC7 and µDTC).

Only one test card is powered at the time. When the test sequence is finished on the given card another card can be activated.

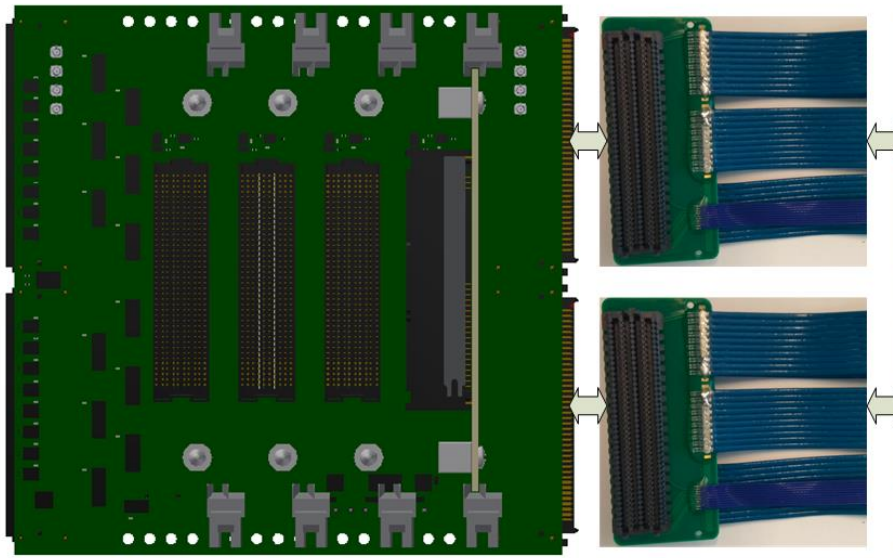


Three backplane cards form a full 19” crate compatible backplane. One individual backplane card can be operated with up to four plug-in cards. The full system can host 36 or more (with more crates) hybrids at the same time.



Backplane design by R. Gajanec

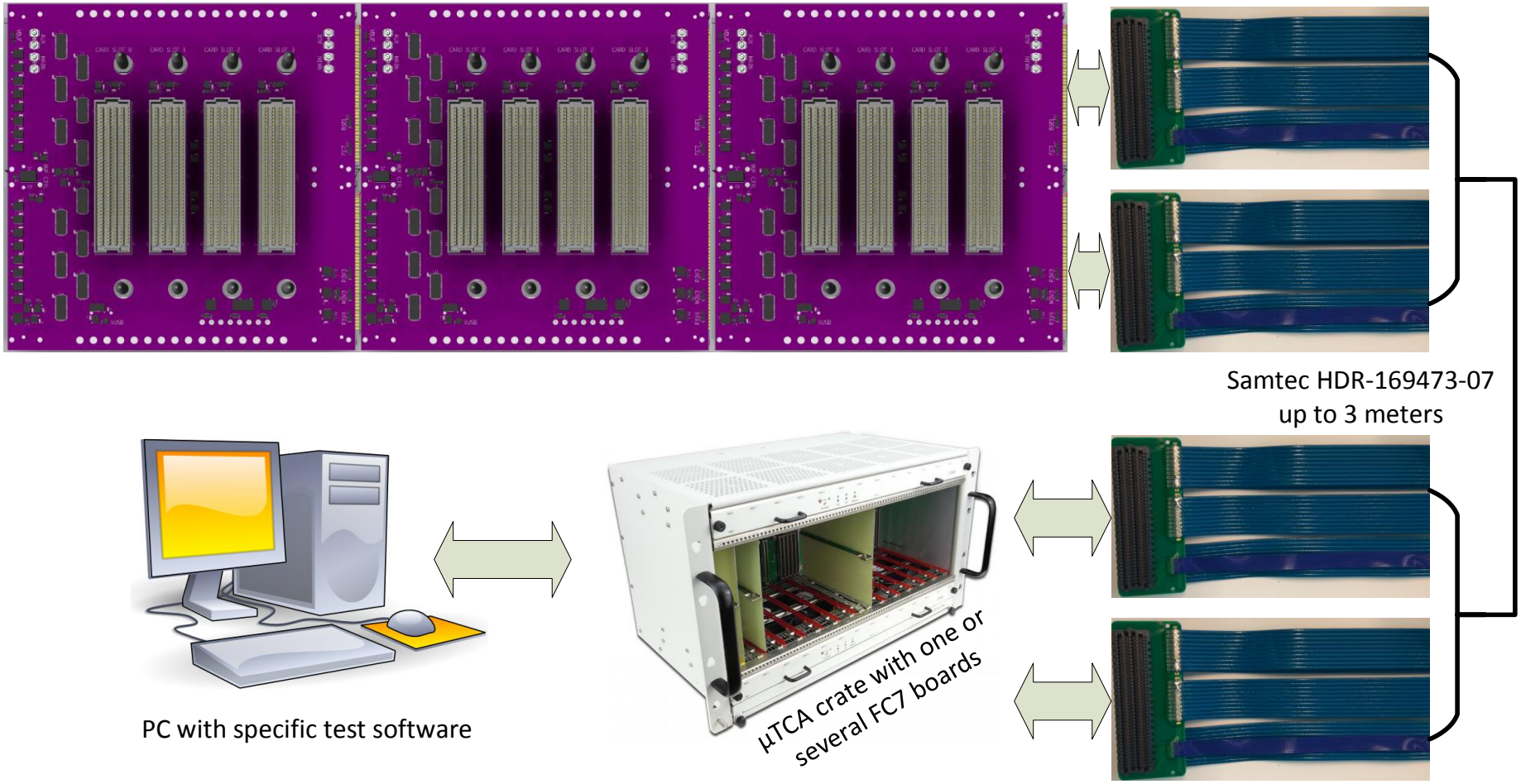
The backplane card can be operated in standalone mode with even only one test card plugged. The FC7 can be operated in a benchtop mode as well.



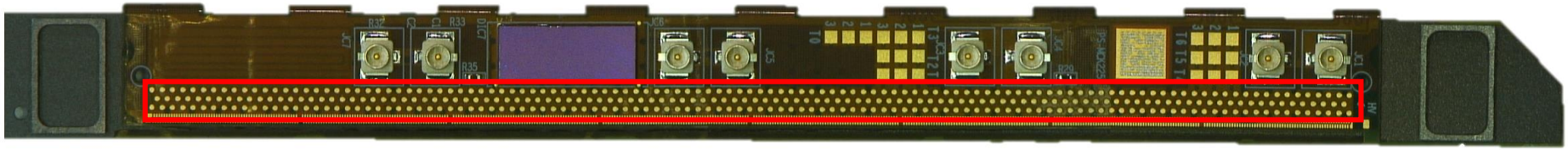
Standalone
backplane card

Plugged to an FC7 operated in
“benchtop” mode

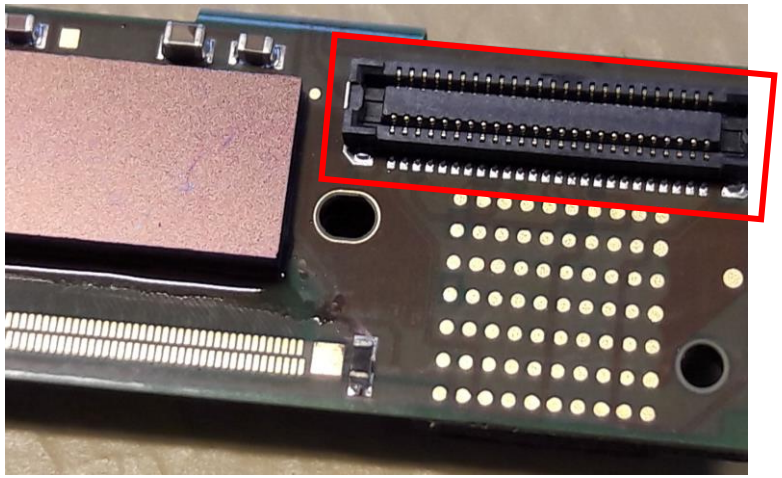
To form a complete 19” crate compatible backplane, three cards need to be interconnected. The system is compatible with the FMC LPC pinout defined in the VITA 57.1 standard. The main target is the FC7 board.



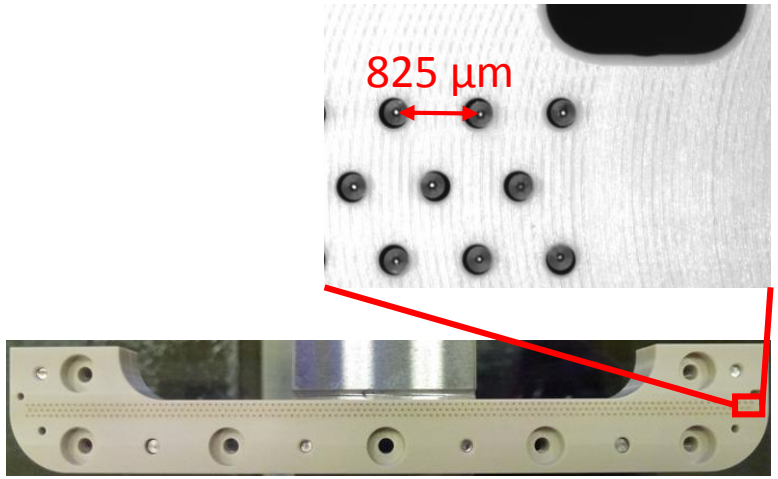
The test interconnection to the PS hybrids is using the data connector on the top side and POGO probe points on the bottom side. The reliability of the POGO interconnection was tested with the PS-MCK in the climatic chamber. The interconnection to the 2S hybrids is using only the data connectors.



POGO probe points on the bottom side of the PS-MCK hybrid.

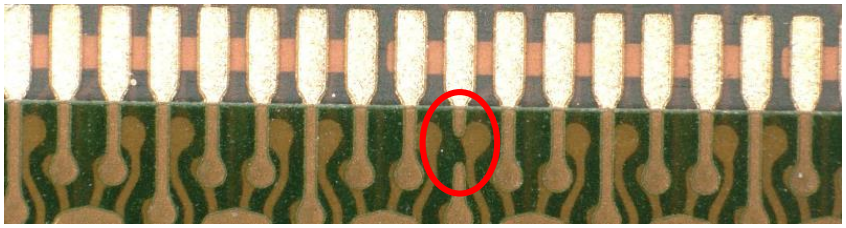


PS-MCK top side A35S series data connector.

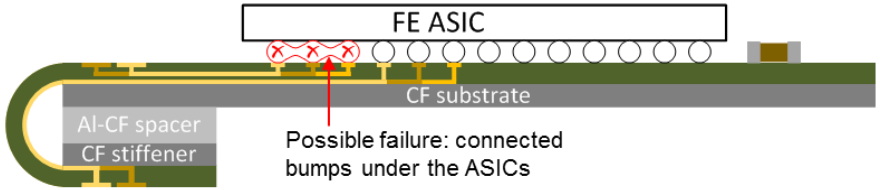


PS-MCK compatible POGO test socket.

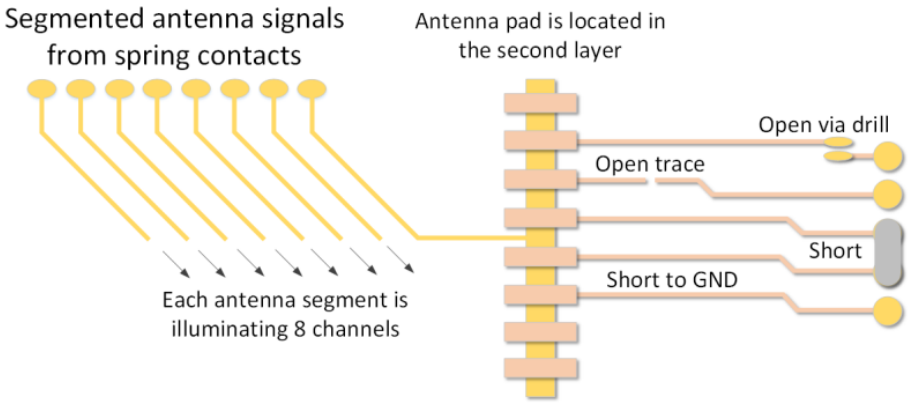
During the first functional test, the hybrids have no sensors interconnected. An embedded charge injection system was developed to test the interconnection from the hybrid wire-bond pads to the flip-chips (opens). A short finding algorithm was developed in parallel to find the shorted connections.



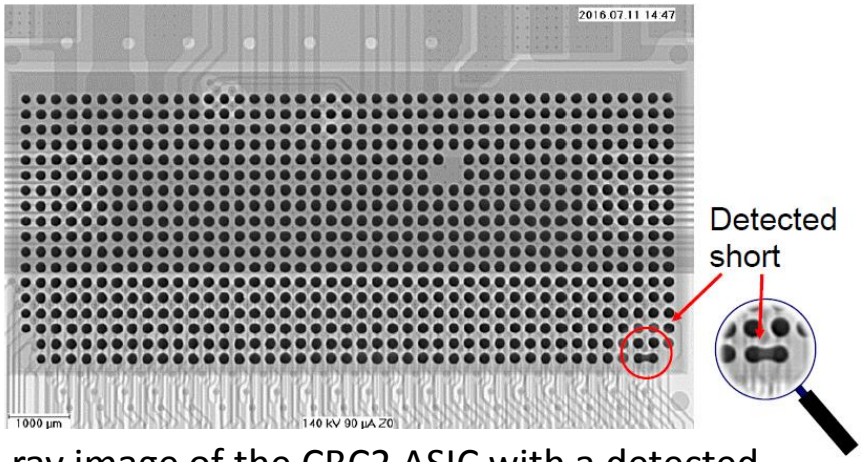
Intentionally created open circuit failure next to the wire-bond pads of the PS-MCK.



A cross-section sketch of a folded 8CBC2 hybrid with shorted bumps.



Schematic figure of the integrated charge injection system.



X-ray image of the CBC2 ASIC with a detected short.

Test algorithms developed by T. Gadek

Conclusions

- A few contractors can deal with the complexity of the hybrids and several prototypes have been manufactured and tested.
- Good surface flatness is a key point to achieve a reliable flip-chip assembly. The warpage problems need to be solved. Different solutions are being explored.
- The PCBs tested so far showed good reliability. No via structures failed due to via fatigue, no fine line structures formed shorts or broke.
- The connector test coupons showed good reliability even after irradiation and 5 plug-unplug cycles.
- The reliability test system can be operated reliably for the long duration tests.
- The analysis shows when the failures developed during the test.
- The test system can find the manufacturing/design/assembly failures.
- The reliability of the different flip-chip assemblies cannot be compared due to the assembly problems, lifetime analysis is not possible for the flip-chip bonding.
- The production scale hybrid test system is under development, prototypes of the backplane will be available this year.

- Solve flex warpage problem due to the CTE mismatch of stiffener and PCB.
- Finish the design of all the hybrid variants and prepare prototype runs.
- Produce test system prototype, design the hybrid test cards, test the system.
- Continue thermal cycling of the samples which did not show failures.
- Analyze the failure methods of the coupon #2 E flip-chip daisy-chain (ongoing).
- Test coupons will be added to every new design. Thin connection to solder pad will be improved.
- Prepare lifetime analysis when fatigue failures are found.
- Compare the reliability of different assemblies and technologies.
- Estimate expected lifetime in the tracker environment.

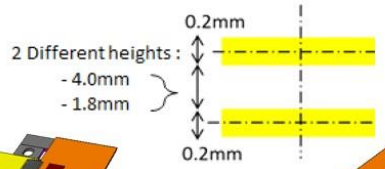
Acknowledgement

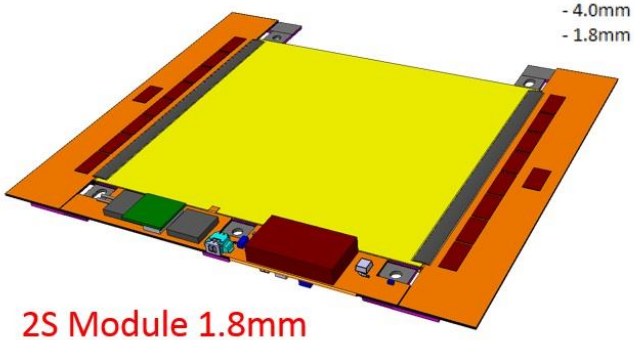
I would like to thank for the contribution of all the colleagues involved in the hybrid development and the reliability testing.

Thank you for your attention.

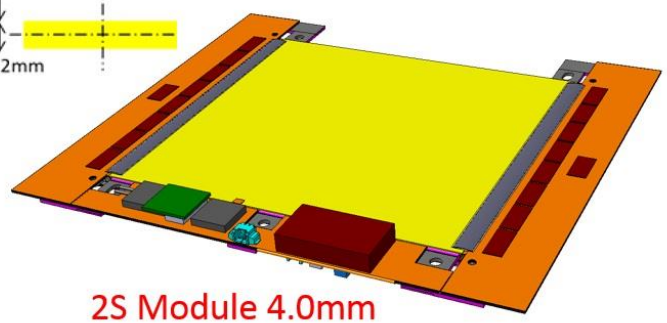
Backup Slides

2S : Strip-Strip Module





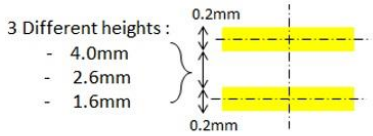
2S Module 1.8mm

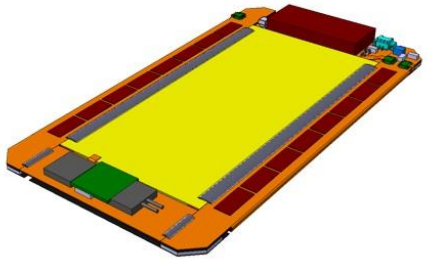


2S Module 4.0mm

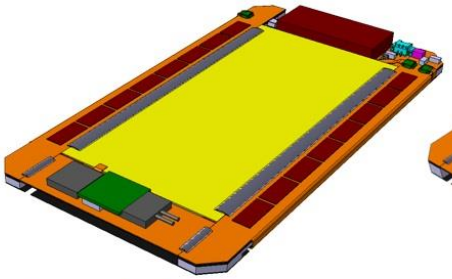
4,064 5-centimeter long silicon strips per module

PS : Pixel-Strip Module

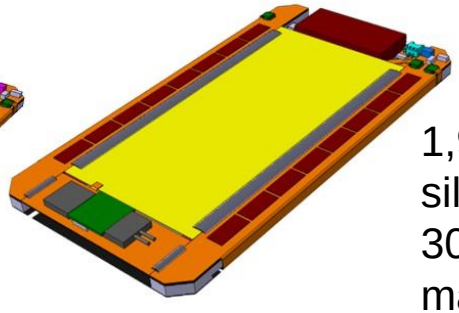




PS Module 1.6mm

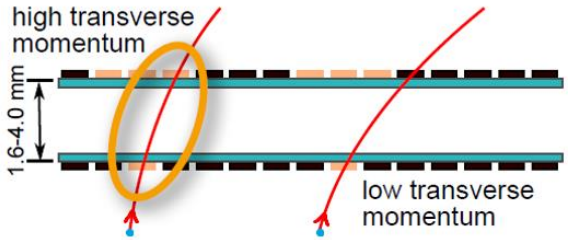


PS Module 2.6mm



PS Module 4.0mm

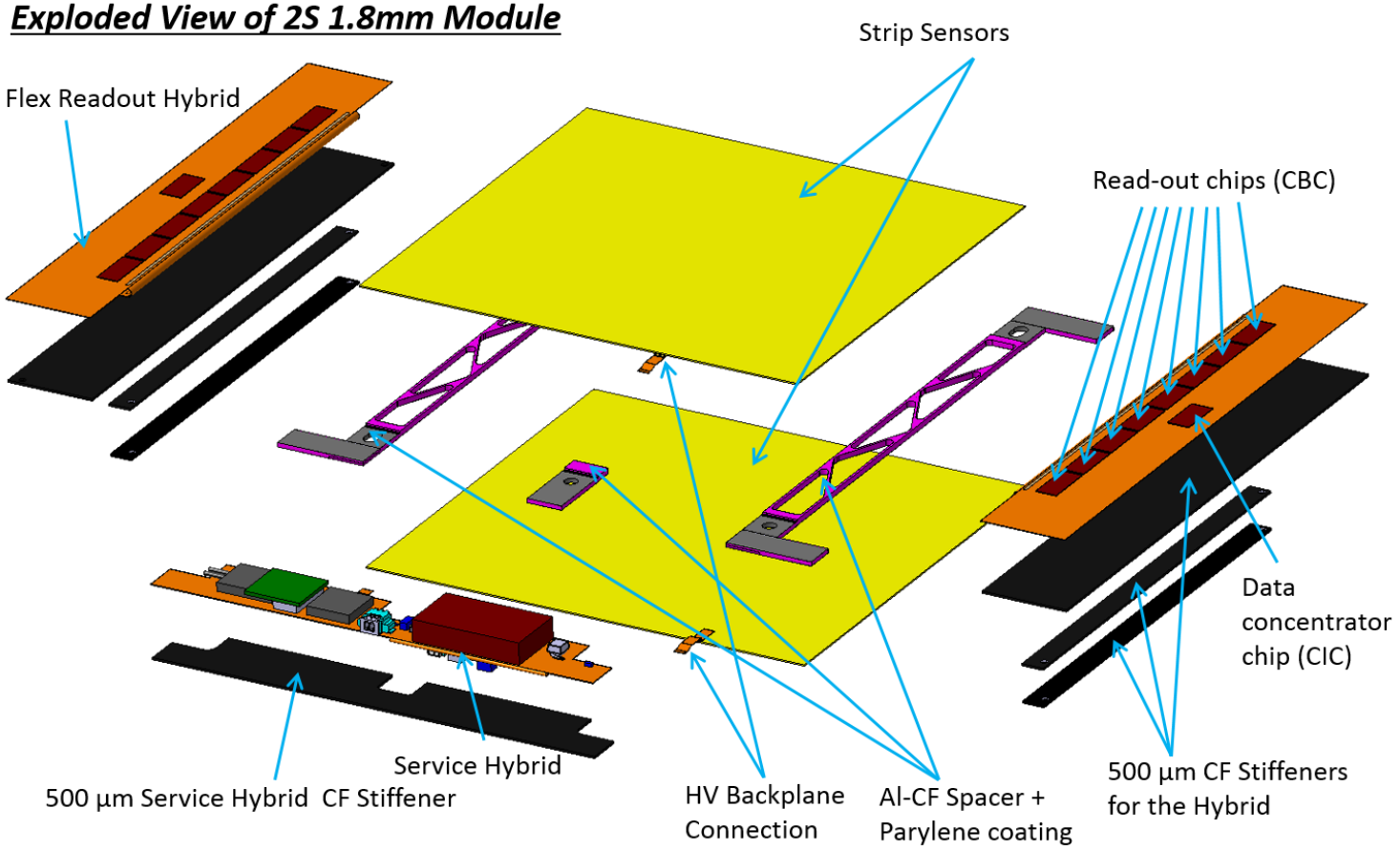
1,920 2.5-centimeter long silicon strips
30,720 1.4-millimeter long macro pixels per module

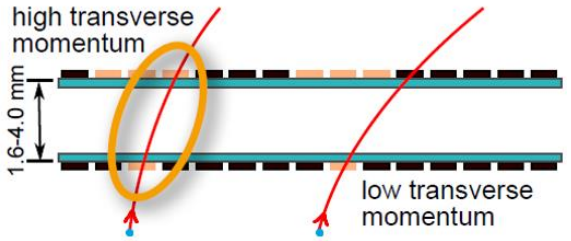


	2S Modules		PS Modules		
	1.8mm	4.0mm	1.6mm	2.6mm	4.0mm
TBPS	.	.	888	1516	504
TB2S	4464	.	.	.	.
Endcap	2976	984	.	.	2800

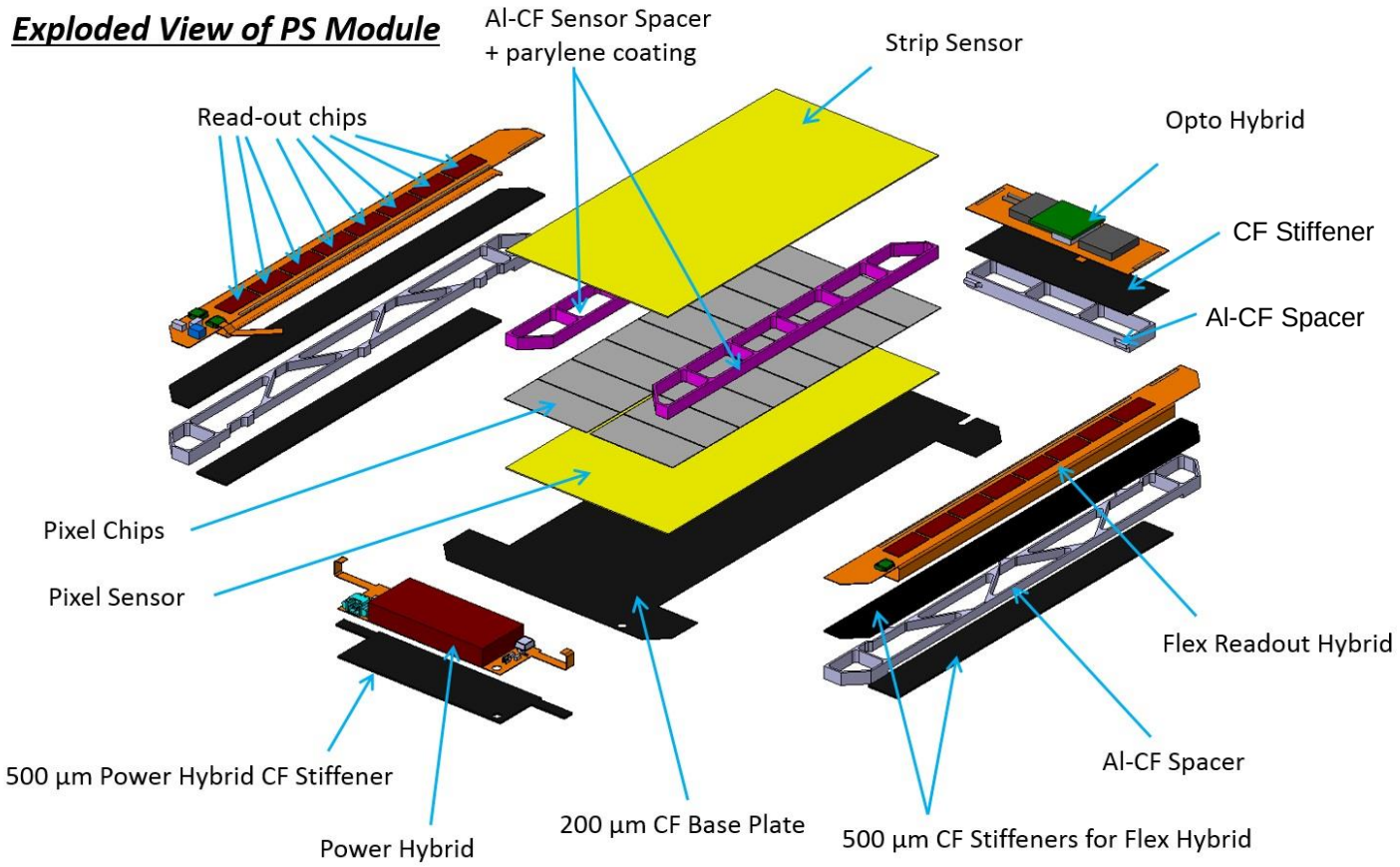
Total 2S Modules	**8424**
Total PS Modules	**5708**

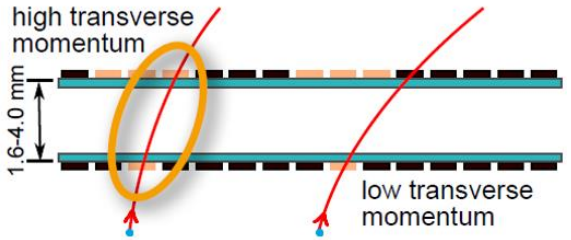
Total Modules	**14132**
Total Hybrids	**28264**





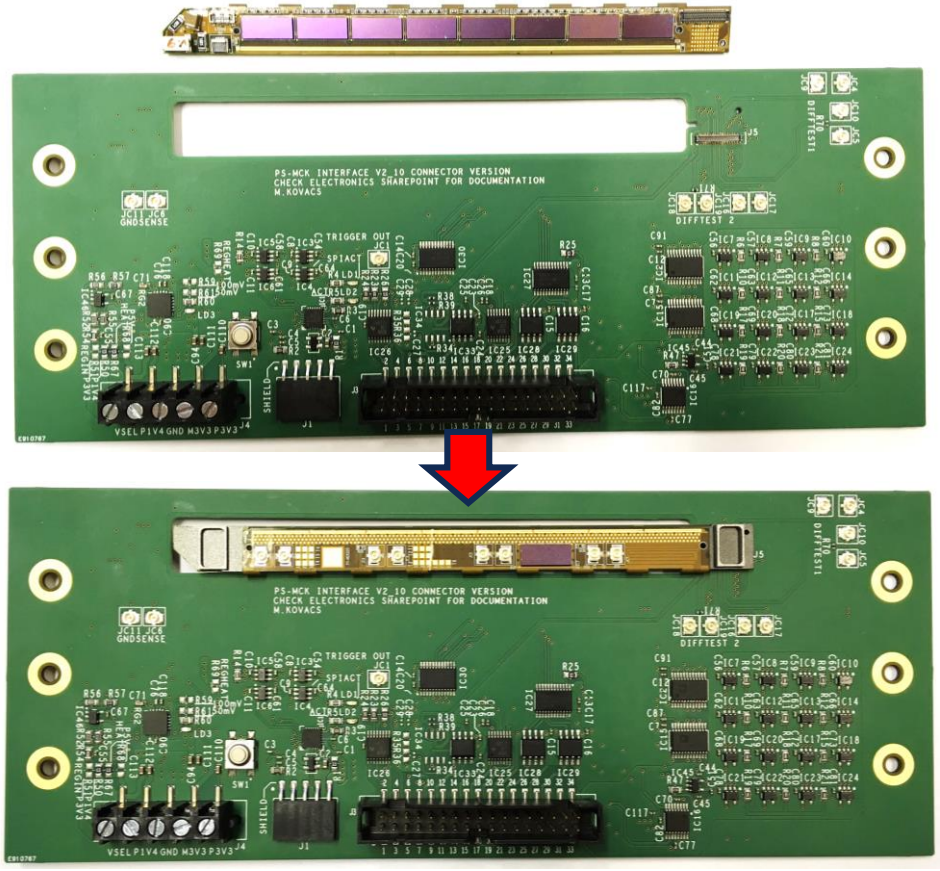
G. Blanchot, T. Gadek, R. Gajanec , M. Kovacs


Exploded View of PS Module
Al-CF Sensor Spacer
+ parylene coating
Strip Sensor
Read-out chips
Opto Hybrid
CF Stiffener
Al-CF Spacer
Pixel Chips
Pixel Sensor
Flex Readout Hybrid
Al-CF Spacer
500 µm Power Hybrid CF Stiffener
Power Hybrid
200 µm CF Base Plate
500 µm CF Stiffeners for Flex Hybrid


high transverse
momentum
1.6-4.0 mm
low transverse
momentum

Two types of interface card were produced:

- 1 for the bench top use with a mezzanine connector,
- 1 for the cold box use with a spring loaded pins socket,
- Conversion of signals from a hybrid to an FPGA-based readout,
- Software controlled charge injection and trigger generation circuit on board.

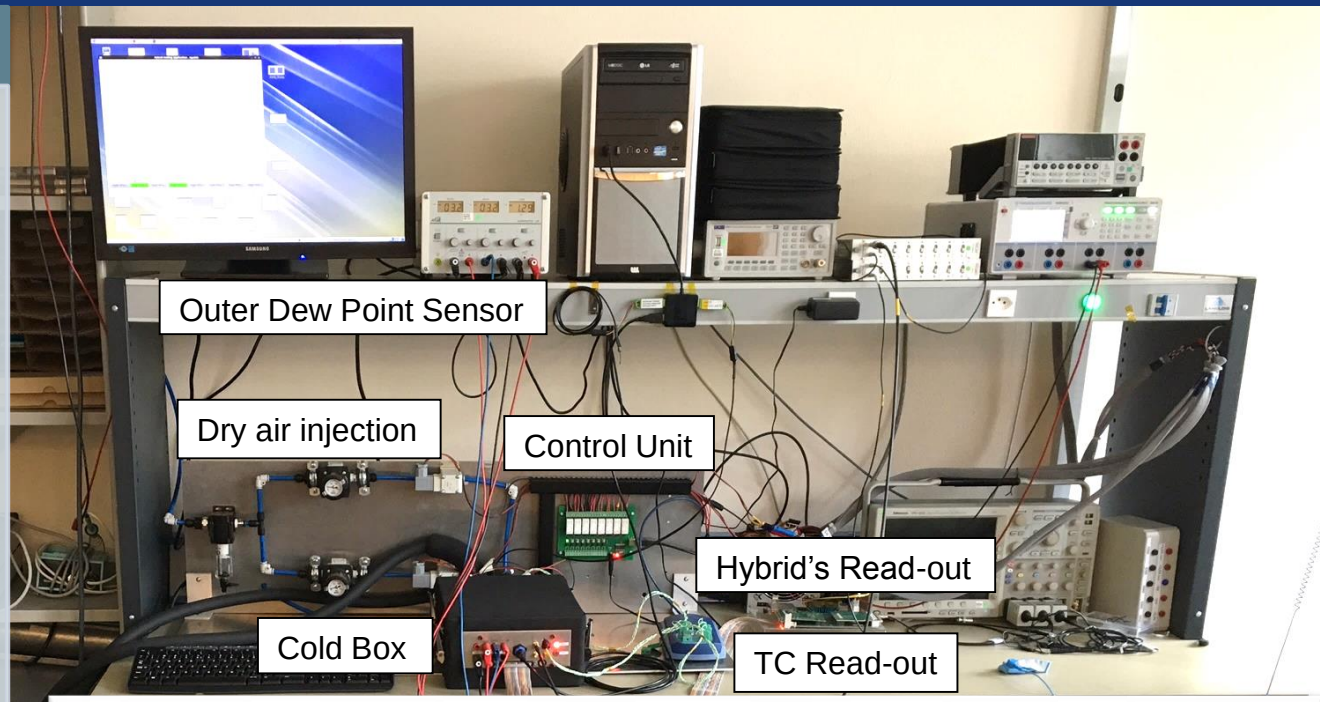


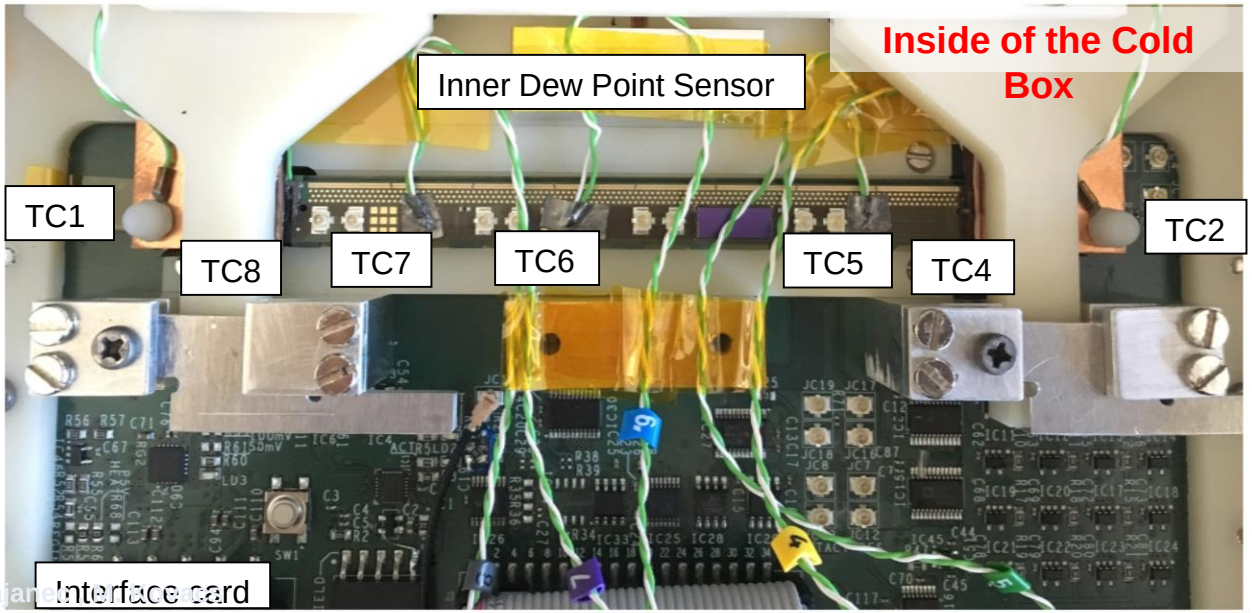
Interface card for a bench top

Cold Test Setup

Re-test in cold:

- Hybrid's operation at planned coolant temperature in the detector (-35°C),
- Validation of test methods at low temperature,
- Study on the impact of the temperature on the detectability of defects.





Example of shorts detection

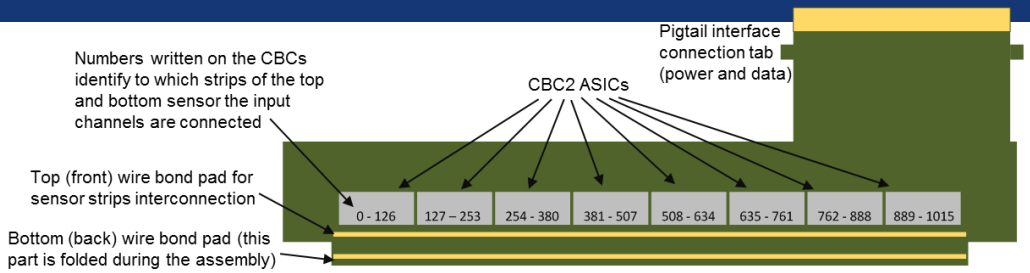


Figure: An explanatory sketch of an unfolded 8CBC2 hybrid components

Example of use - 8CBC2 prototype (a short between bumps under CBC)

```
Shorted channels searching procedure
Sides: Front - 0  Back - 1 (Channel numbering starts from 0)

 Side   | Channel_ID   | Group_ID     | Shorted_With_Group_ID
-------------------------------------------------------------
   0    |       886    |       4      |       1
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
   0    |       883    |       1      |       4
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
```

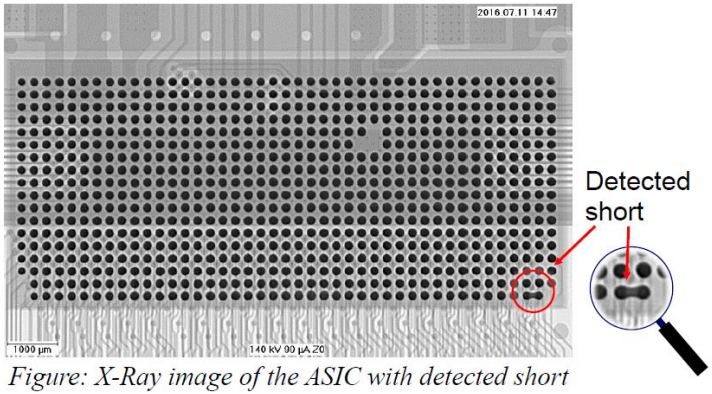


Figure: X-Ray image of the ASIC with detected short

Example of use – 2S module prototype number 3 (a short between wire-bond pads on the sensor)

```
Shorted channels searching procedure
Sides: Front - 0  Back - 1 (Channel numbering starts from 0)

 Side   | Channel_ID   | Group_ID     | Shorted_With_Group_ID
-------------------------------------------------------------
-------------------------------------------------------------
   1    |       1012   |       3      |       2
-------------------------------------------------------------
   1    |       1011   |       2      |       3
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
```

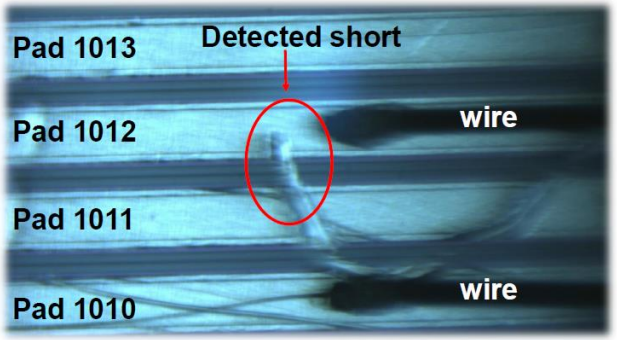


Figure: A microscope image of the short between pads on the silicon sensor detected by the algorithm