Characterization of the CBC2 readout ASIC for the CMS Strip-Tracker HL upgrade

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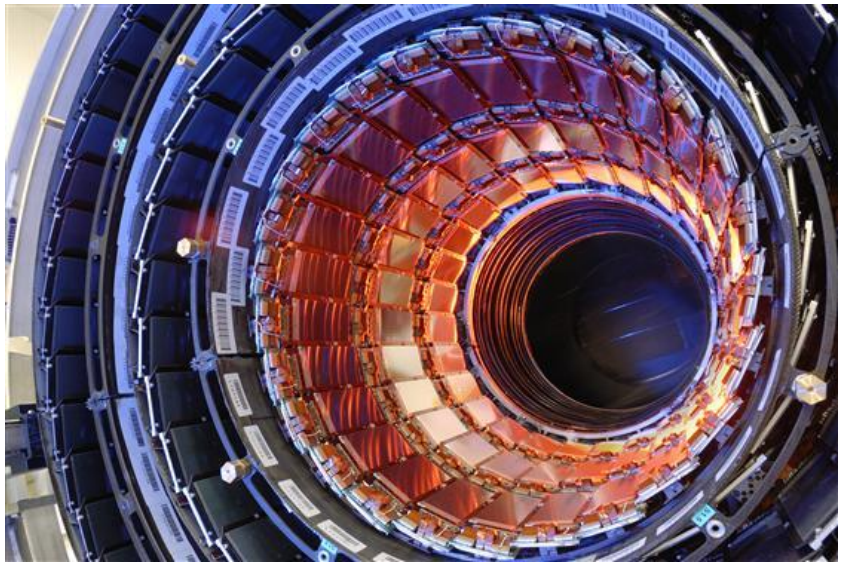
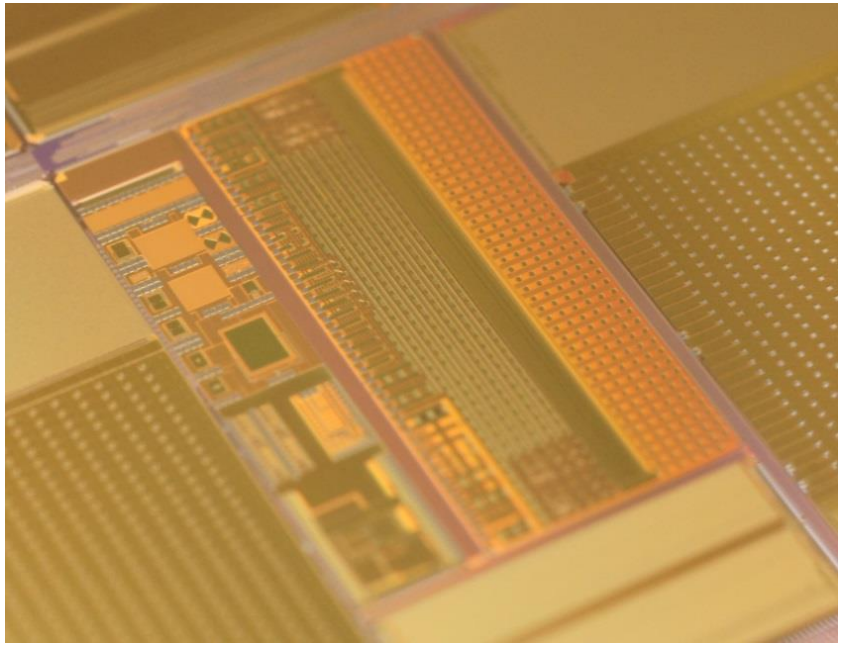
Imperial College London

Science & Technology Facilities Council

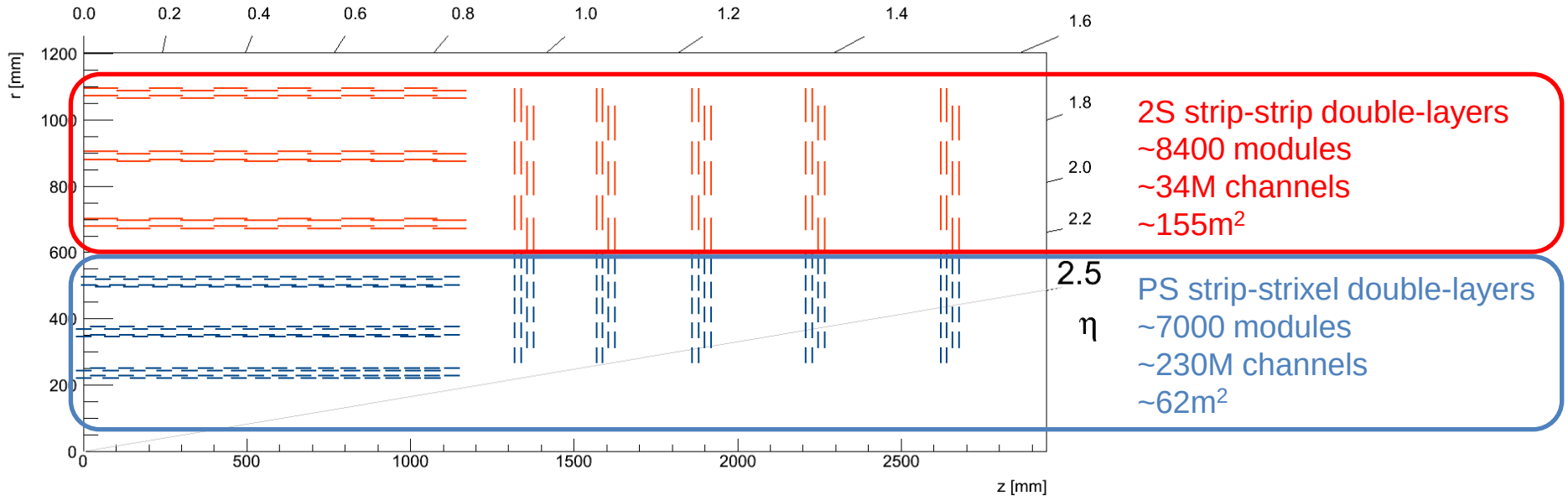




Outline

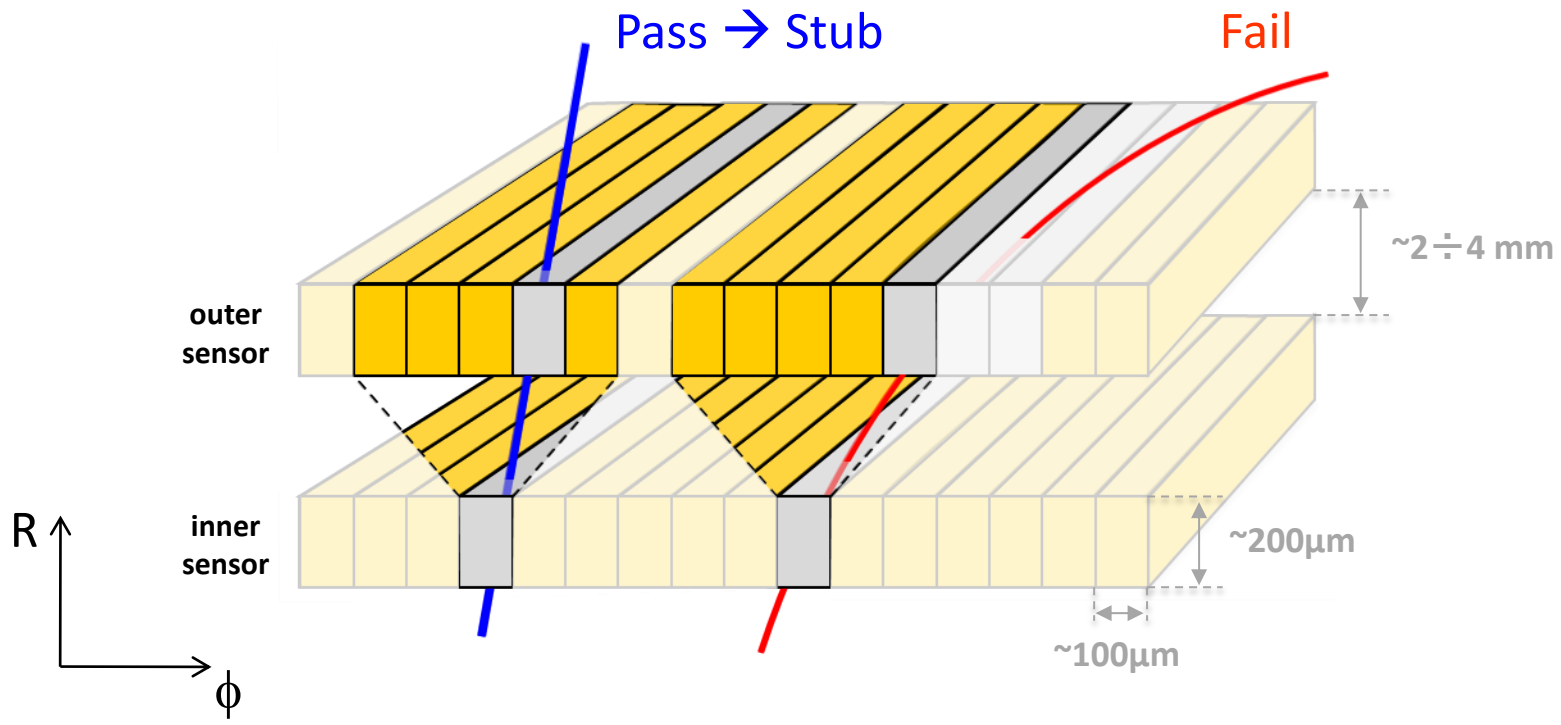
- Tracker upgrade & detector module
- The CBC (CMS Binary Chip) v.1 & 2
- CBC2: architecture & performance
  - Front end
  - Coincidence logic
  - Power elements
- Dual-CBC2 module
- Future plans and conclusions

Phase II upgrade of the CMS Strip Tracker



- Baseline design: Barrel+5Endcaps
- Contribute to L1 trigger to contain rate to 100 kHz
- Possible objective of L1 readout up to 1 MHz/10-20μs latency

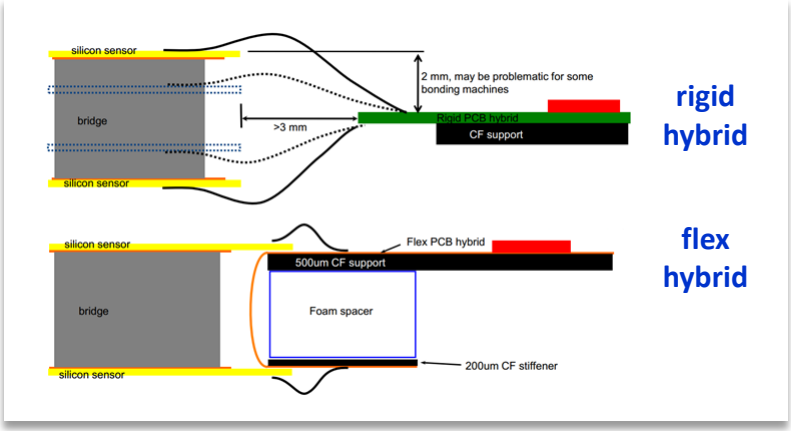
Basic trigger module concept

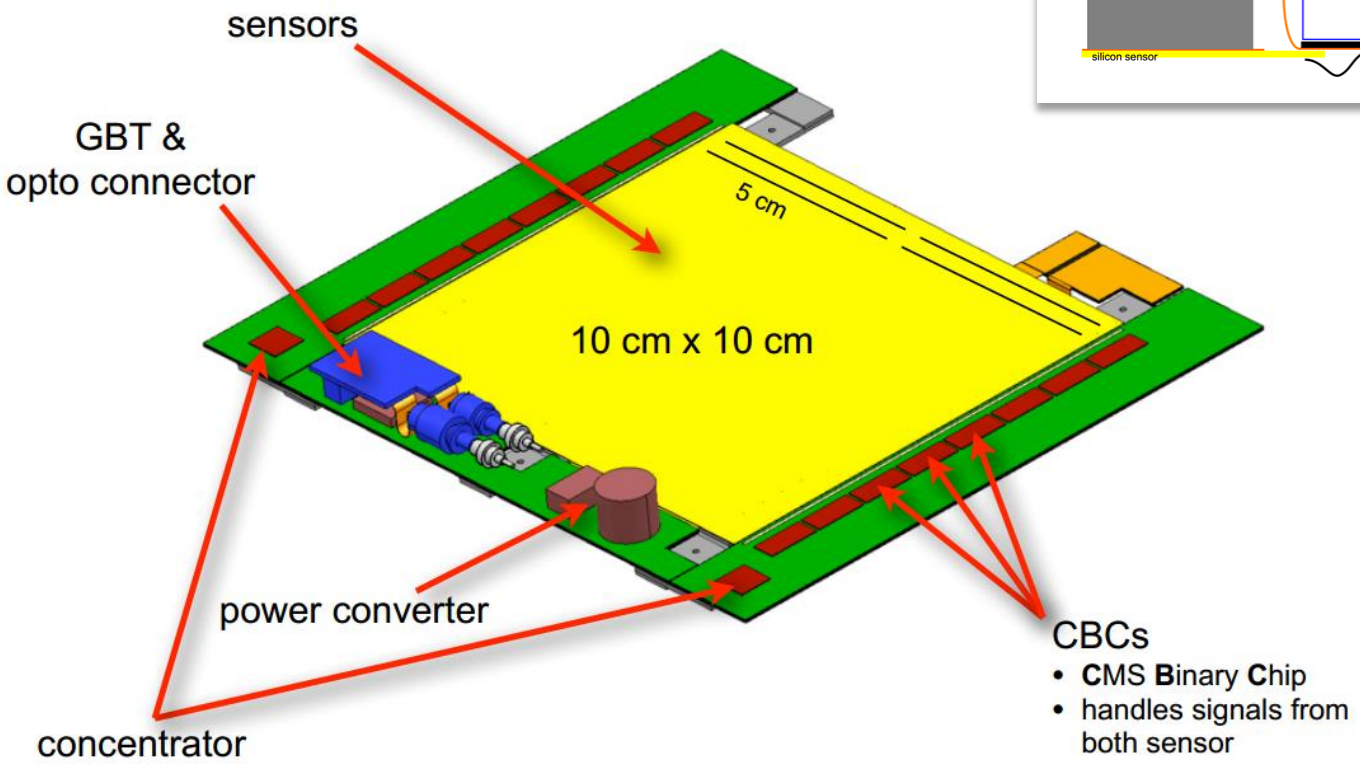


High-P_T tracks (stubs) can be identified if cluster centre in top layer lies within a search window in R-Φ (rows)

2S PT module with CBC2

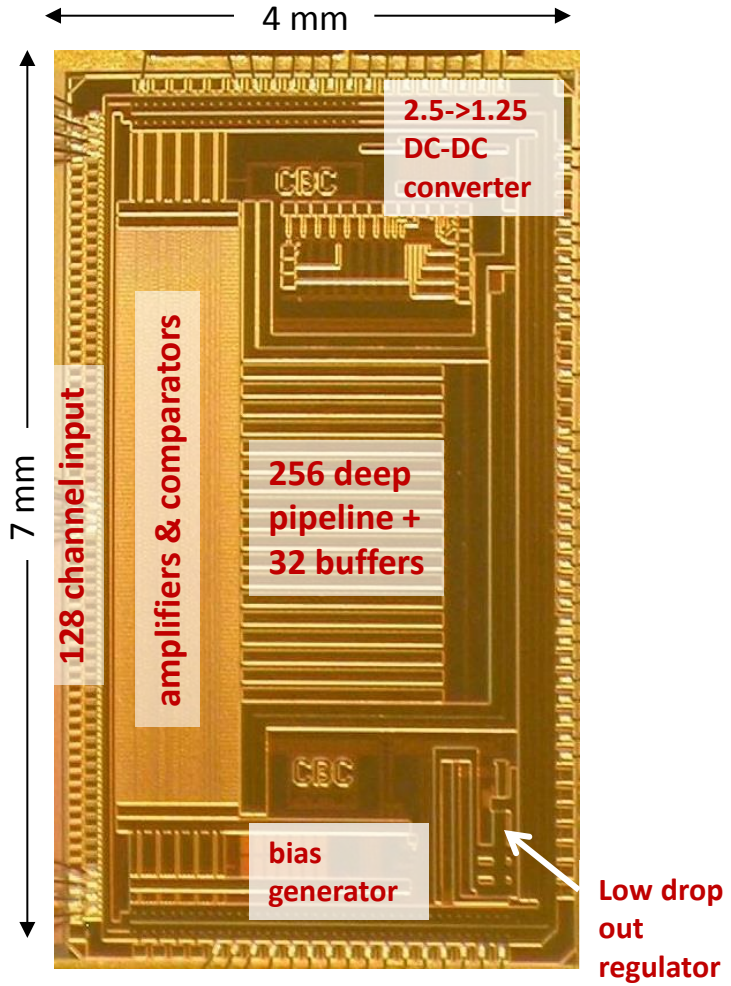
- **Commercial assembly**
- **2x8 CBC bump bonded for commercial assembly**
  → designed for rapid assembly on large scale
- **Only one flavour (except for sensors separation)**





First version: CBC main features

- IBM 130nm CMOS process
- binary, unsparsified architecture
  - retains chip and system simplicity
  - but no pulse height data
- designed for ~2.5 - 5cm µstrips < ~ 10 pF
- 128 channels, 50 µm pitch wire-bond
  - either polarity input signal
- **not contributing** to L1 trigger
- powering test features:
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analogue FE
- fast (SLVS) and slow (I2C) control interfaces



CBC(1) Test Results

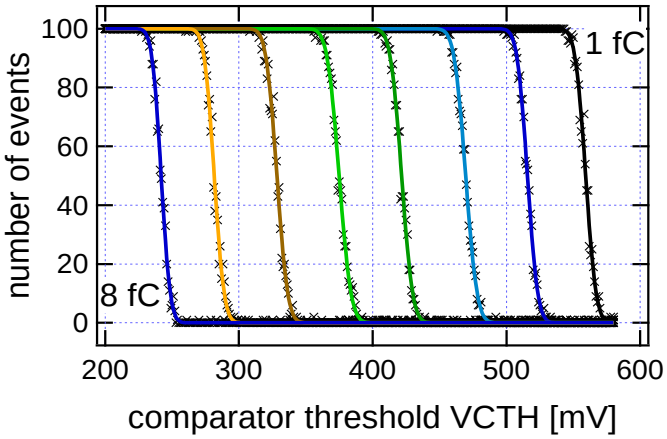
e.g. for 5pF input capacitance:

noise: ~ 800 e_{RMS}

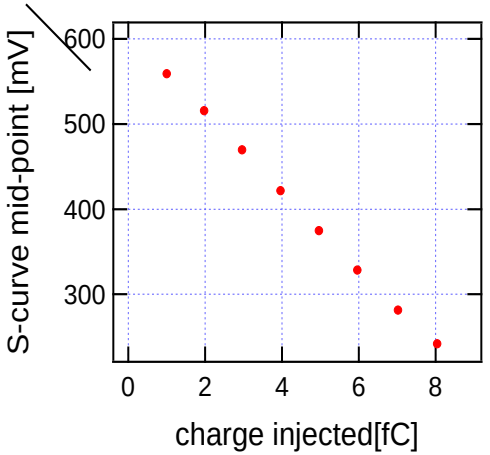
total power: < 300 µW/channel

see: "M.Raymond et al 2012 JINST 7 C01033"
"W.Ferguson et al 2012 JINST 7 C08006"

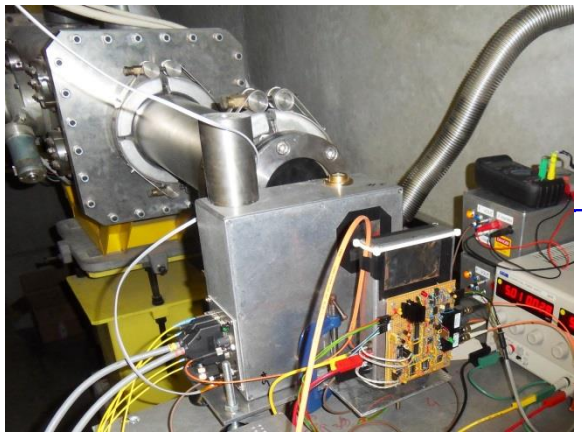
S-curves

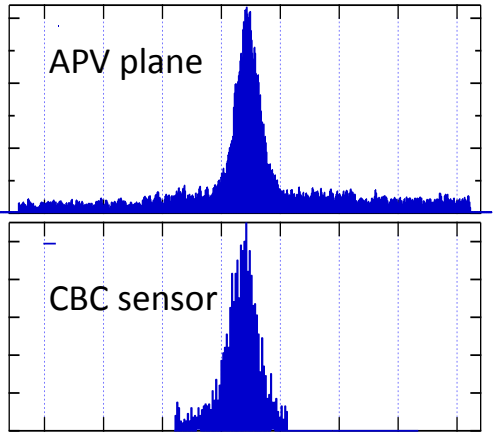


gain

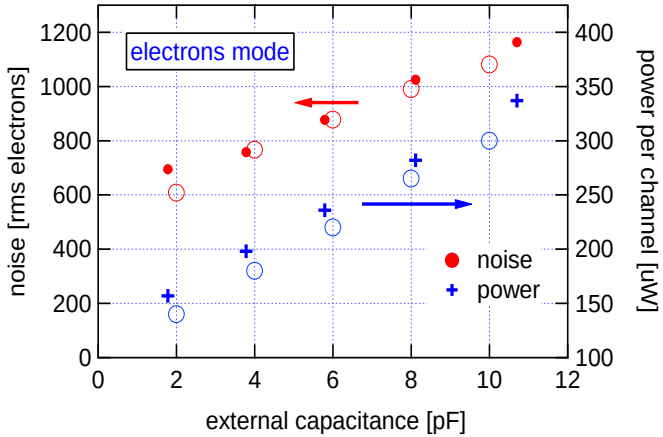


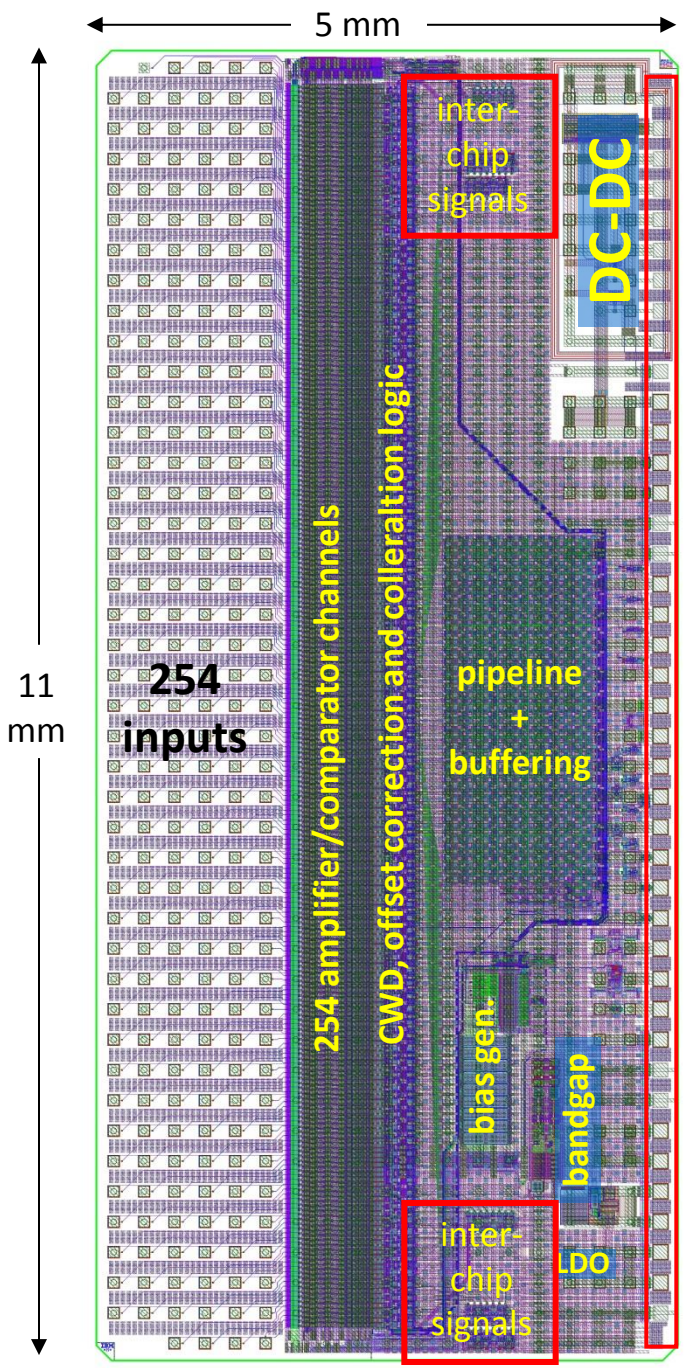
beam profile





noise/power



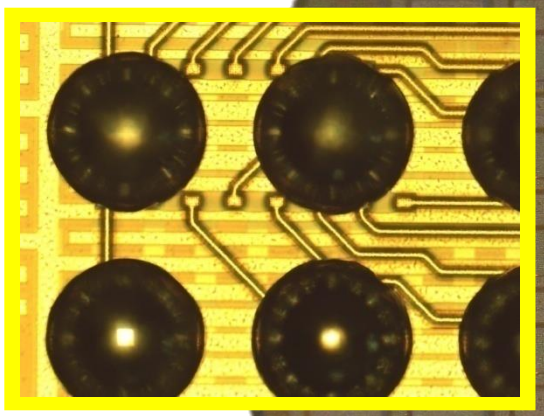


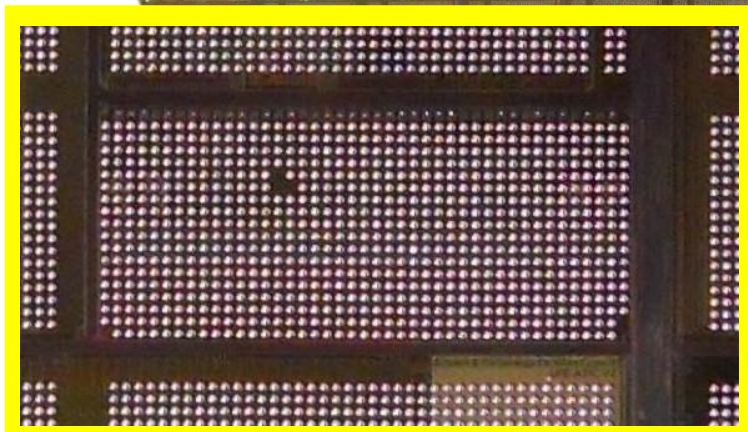
CBC → CBC2: New Features

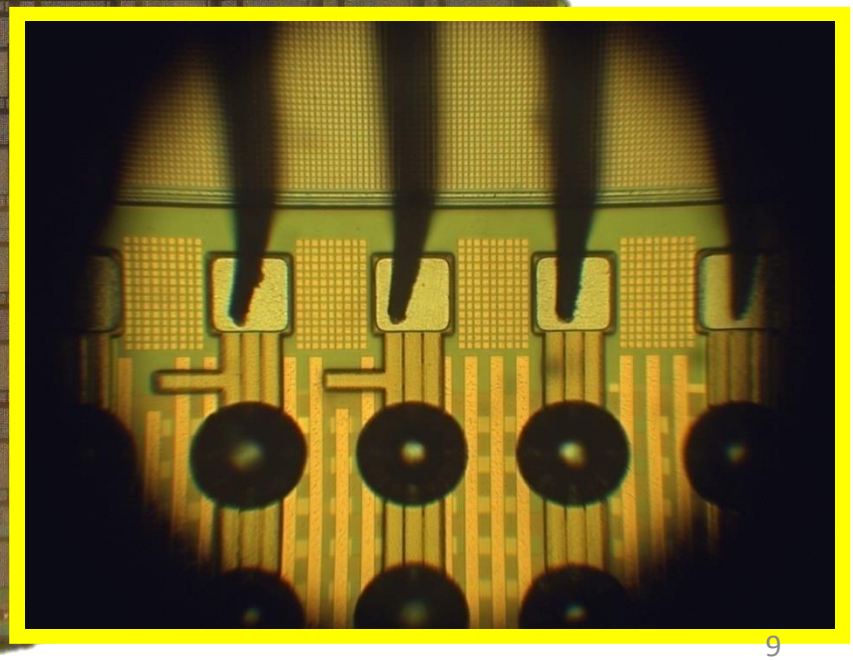
- 250µm pitch C4 layout
  for commercially assembled module
  back edge wire-bond pads for wafer probe
- 254 channels for 127 + 127 strips
- correlation logic for stub formation
  between top & bottom strips
  vetoes wide clusters
- Test pulse & other minor circuit improvements
- Improved DC-DC (CERN)
- received Jan 2013 – fully functional

CBC2 C4 wafers

(shared with RAL LPD ASIC)







CBC2

reticle

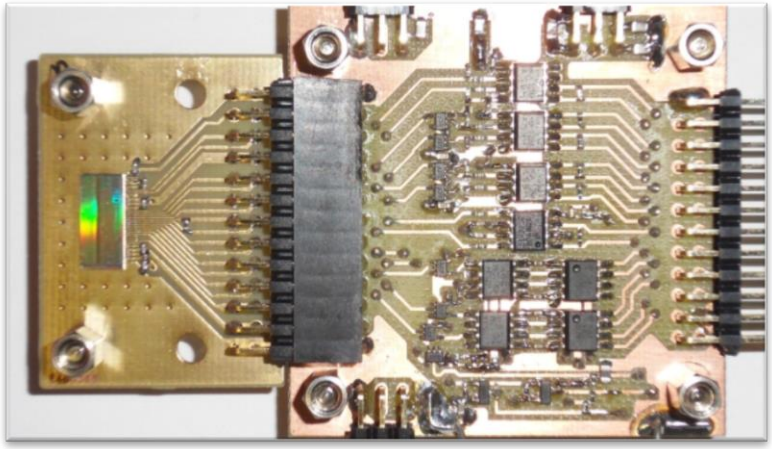
>97% yield

So far 2 out of 8 wafers probed (220 chips)

CBC2 testing activities

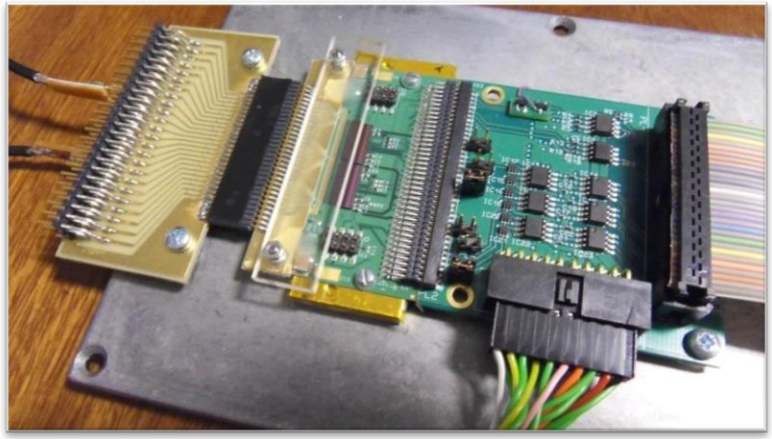
Wire-bond CBC2

- To develop wafer probe procedures
- Next: x-rays TID testing



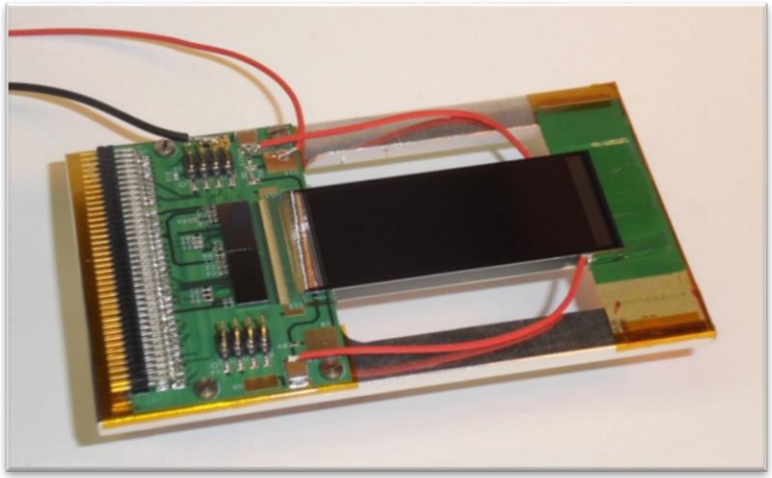
2xCBC2 hybrid

- Hybrid characterization and chip integration
- Bump-bonded ASICs
- Inter-chip links & logic



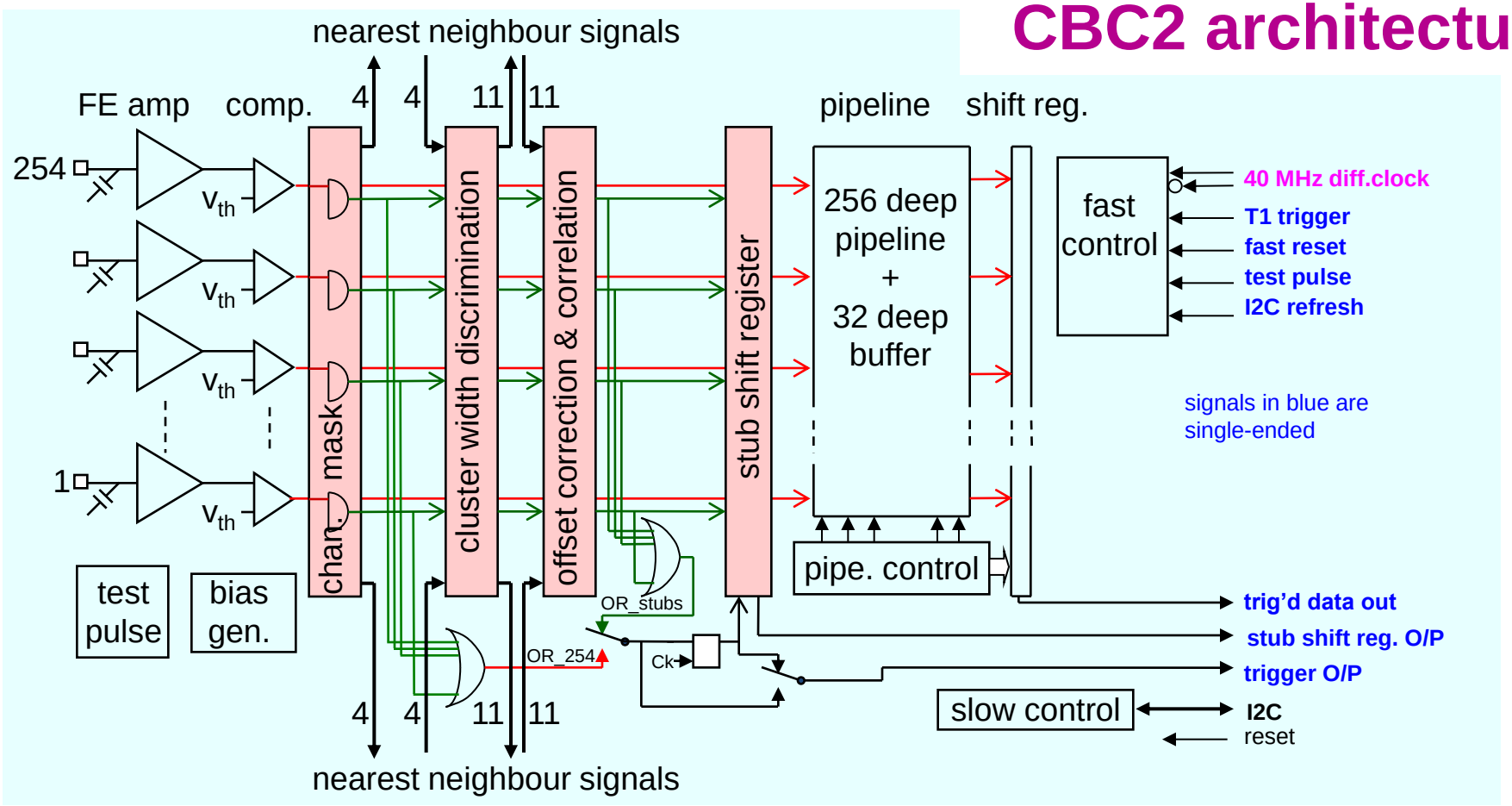
2xCBC2 mini-module + sensor

- Sr-90 source
- Cosmics
- Next: test beam → Pt stubs performance



see Georges' talk: "Hybrid circuit prototypes for the CMS Tracker upgrade front-end electronics"

CBC2 architecture



front end, pipeline, L1 triggered readout, biasing

~ same as prototype (some bug fixes) twice as many channels

new blocks associated with Pt stub generation

channel mask: block problem channels (not from L1 pipeline)

cluster width discrimination: exclude wide clusters > 3

offset correction and correlation: correct for phi offset across module and correlate between layers

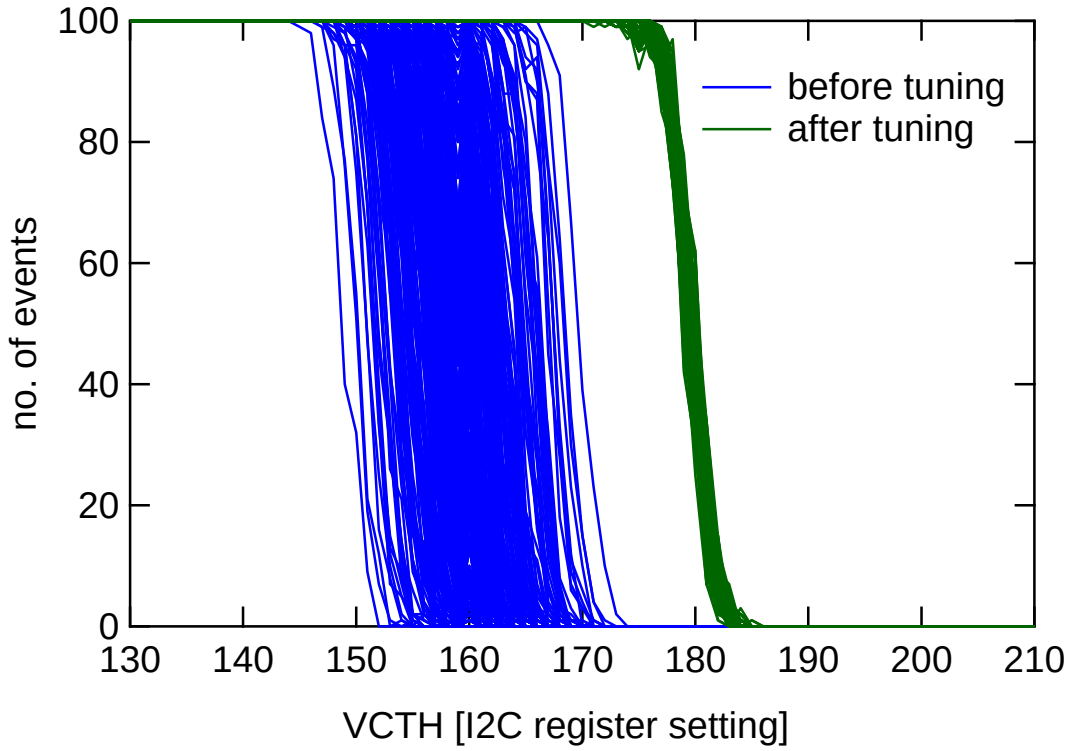
stub shift register: test feature - shift out result of correlation operation at 40 MHz

trigger O/P: in normal operation 1 bit per BX indicates presence of high Pt stub

test pulse

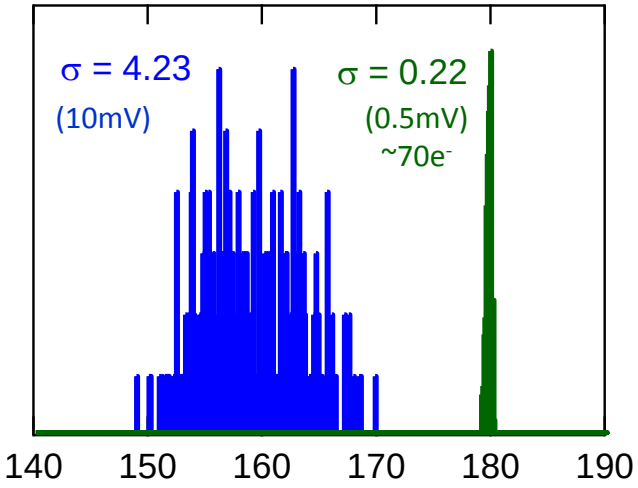
charge injection to all channels (8 groups of ~32), programmable timing and amplitude

S-curves and tuning

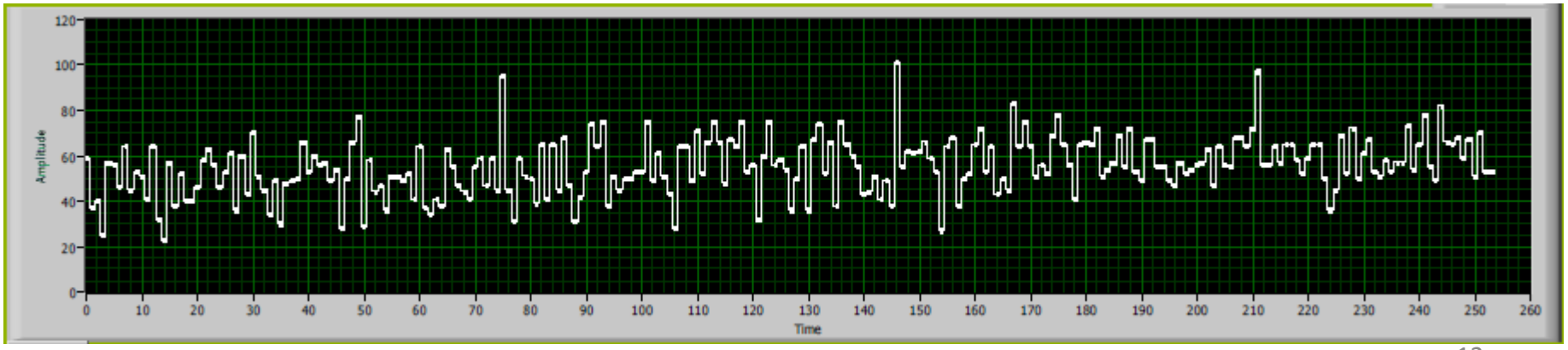


254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to ~mV level



254 offset values after tuning



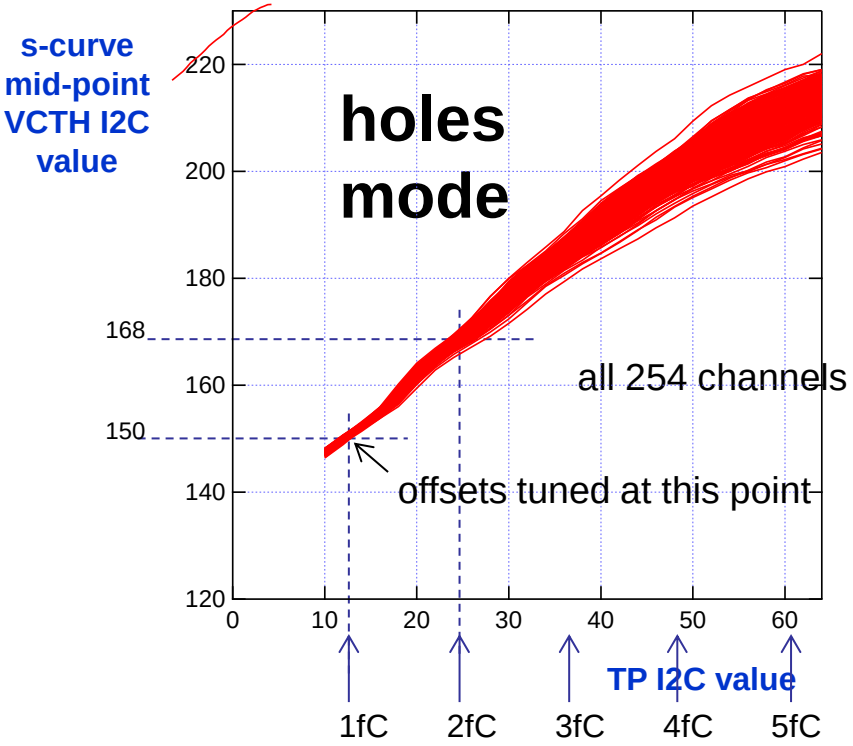
Gain measurements

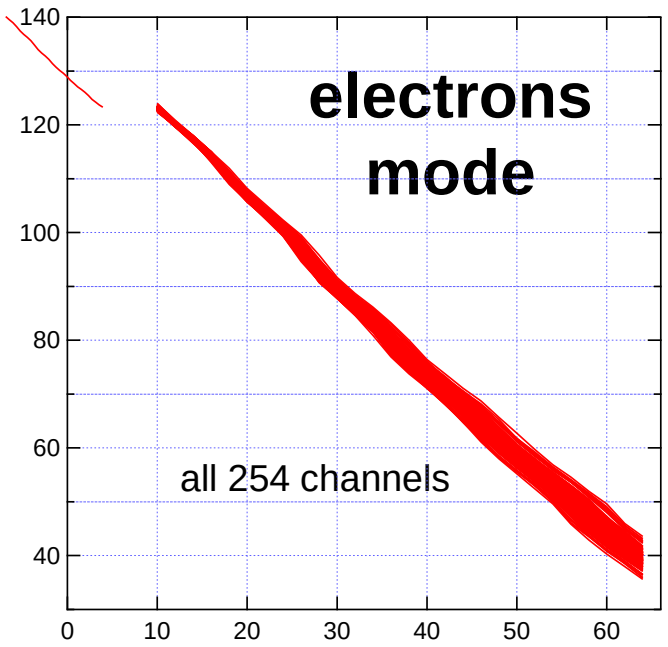
sweep global comparator threshold VCTH
to get s-curves for range of test pulse amplitudes

plot s-curve mid-points vs. TP amp

rough calculation in 1÷2fC region
(assumes TP value of 12 / fC)

(168 - 150) x 2.5 mV* = 45 mV/fC





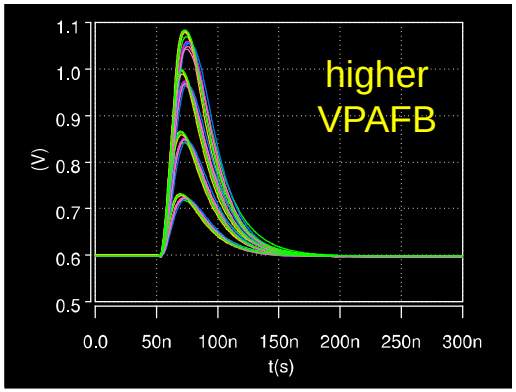
(* from VCTH bias sweep measurements)

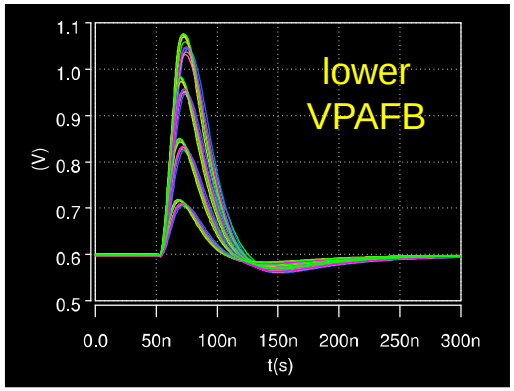
Post-amp feedback resistor control

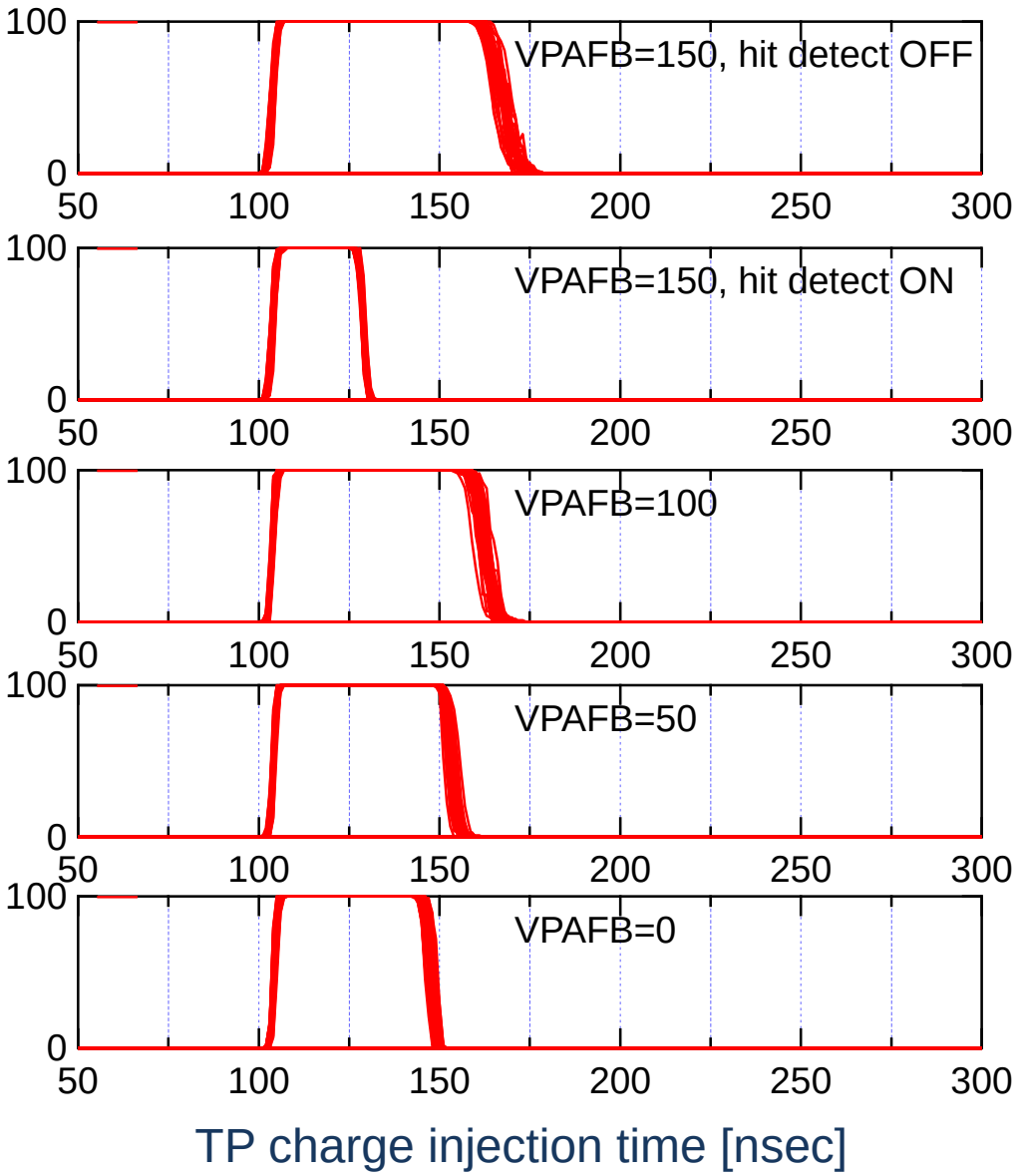
can see effect of VPAFB using test pulse sweep - smaller values give shorter pulse length

hit detect circuit works - only single hit in pipeline irrespective of how long comp O/P stays high

~ 2 fC signal
1 fC comp. thresh







Stub finding logic

cluster width discrimination (CWD) logic

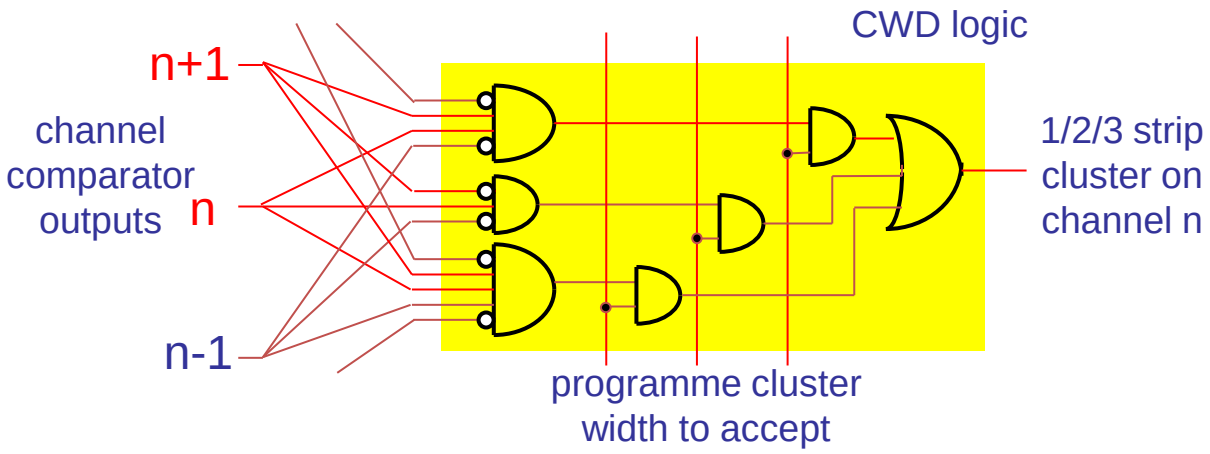
exclude clusters with hits in >3 neighbouring channels
wide clusters not consistent with high pT track

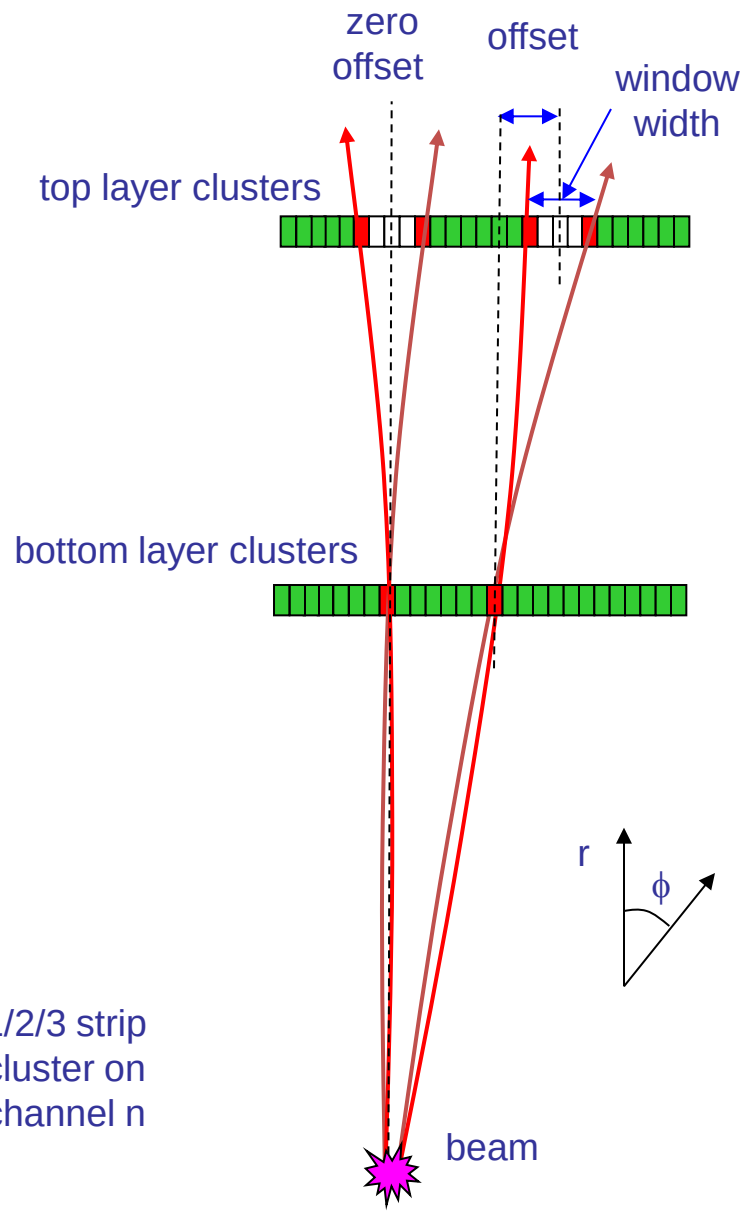
offset correction & correlation logic

for a cluster in bottom layer, look for correlating cluster occurring in window in top layer

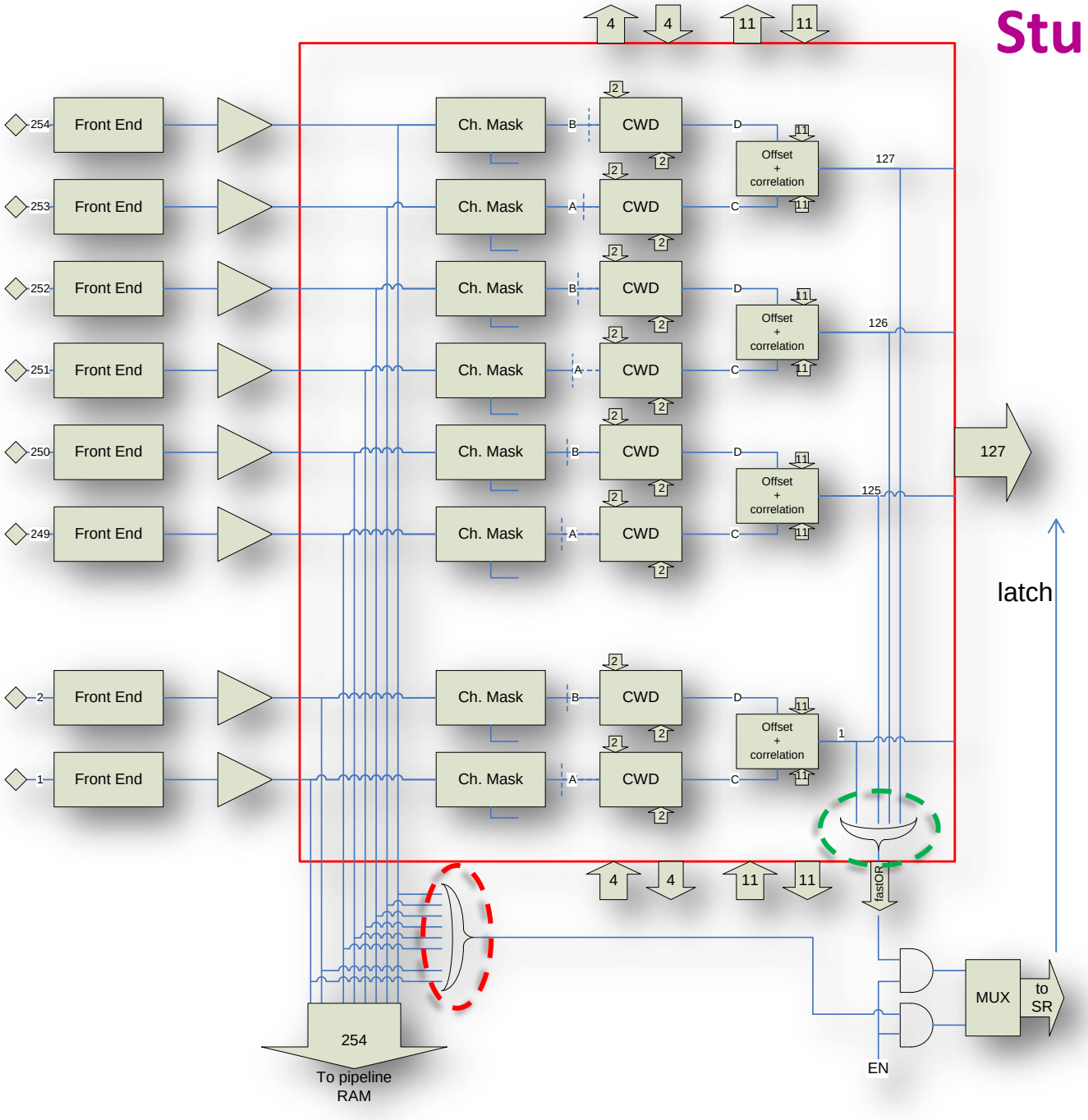
window width controls pT cut
stub found if cluster in bottom layer corresponds to cluster within window in top layer
window width programmable up to **± 8** channels

offset defines lateral displacement of window across chip
programmable up to **± 3** channels





Stub finding Logic



Individual mask for noisy channels
→254b from I2C reg.
(can be also used to inhibit coincidence logic)

Need to be able to inhibit stub shift register operation
→1b EN from I2C reg.

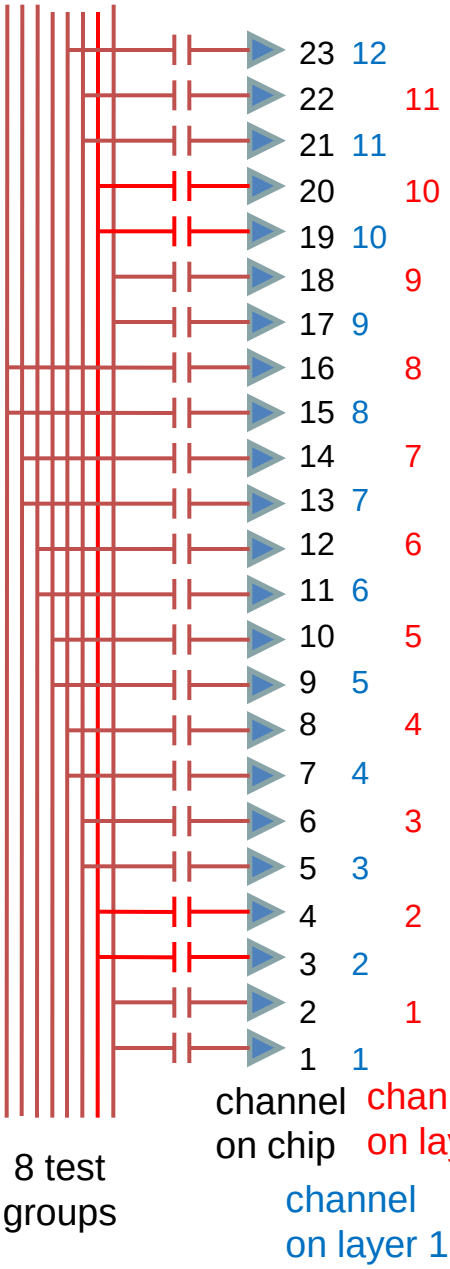
254-OR of channel outputs to signal any activity on chip

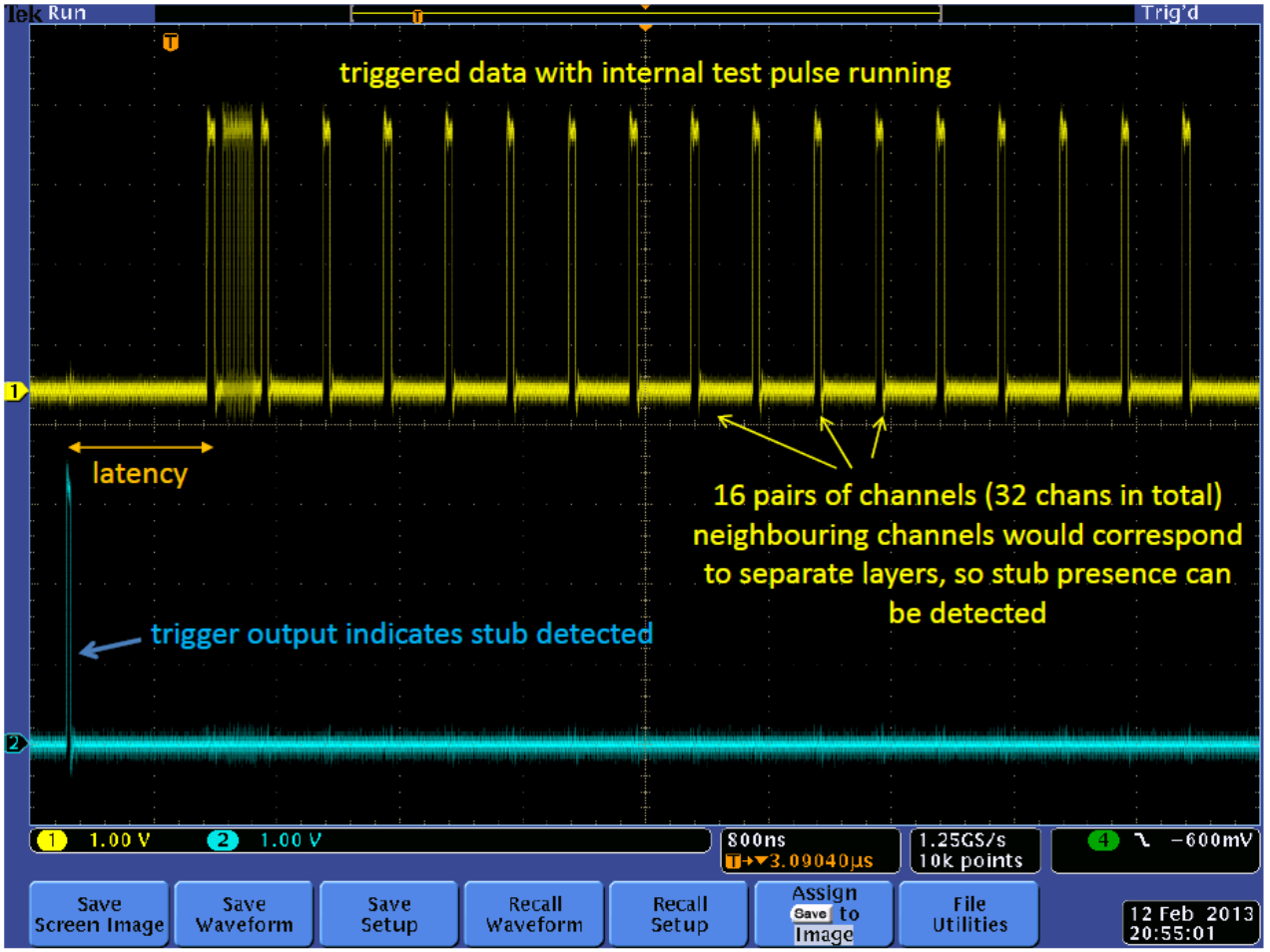
127-OR of stubs to signal stub activity and control the stubs SR readout

(→ CBC2 can be used as self-triggered chip)

@40MHz

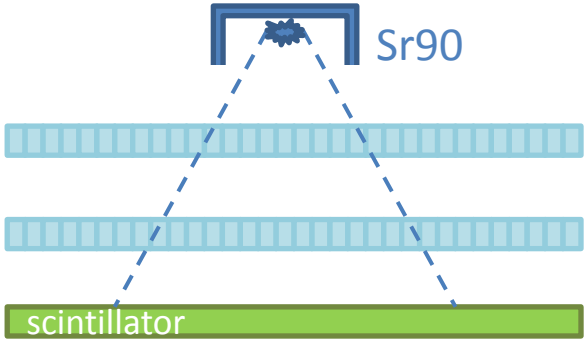
Results with test pulse

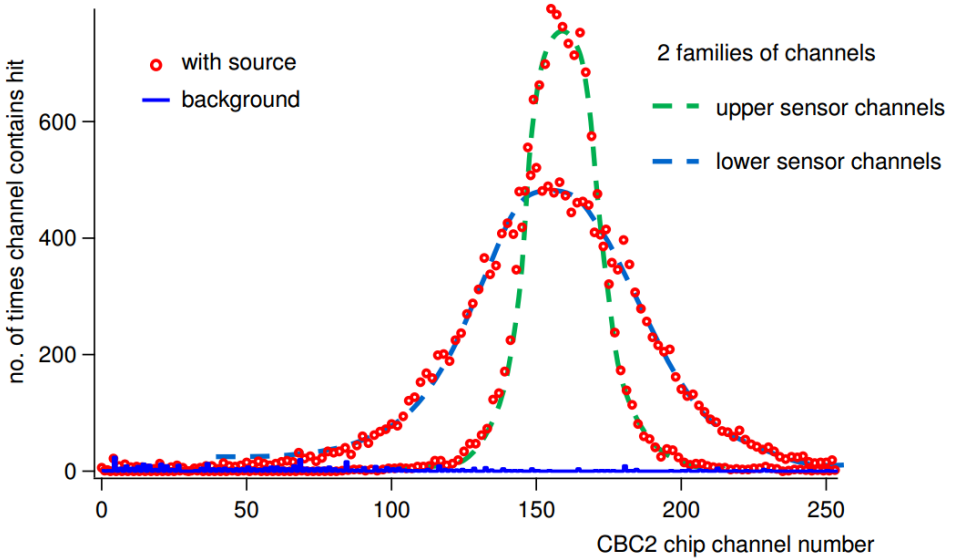


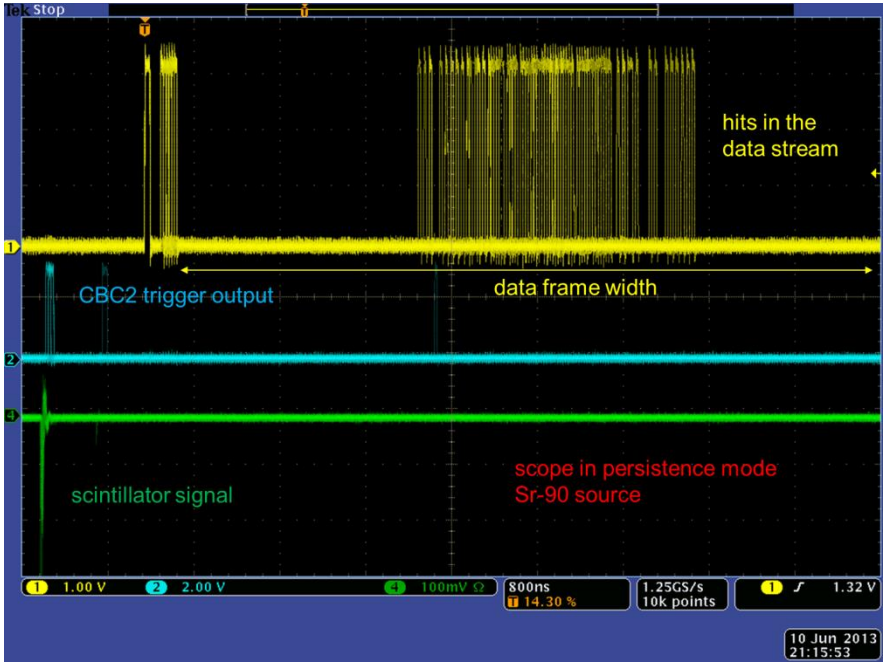


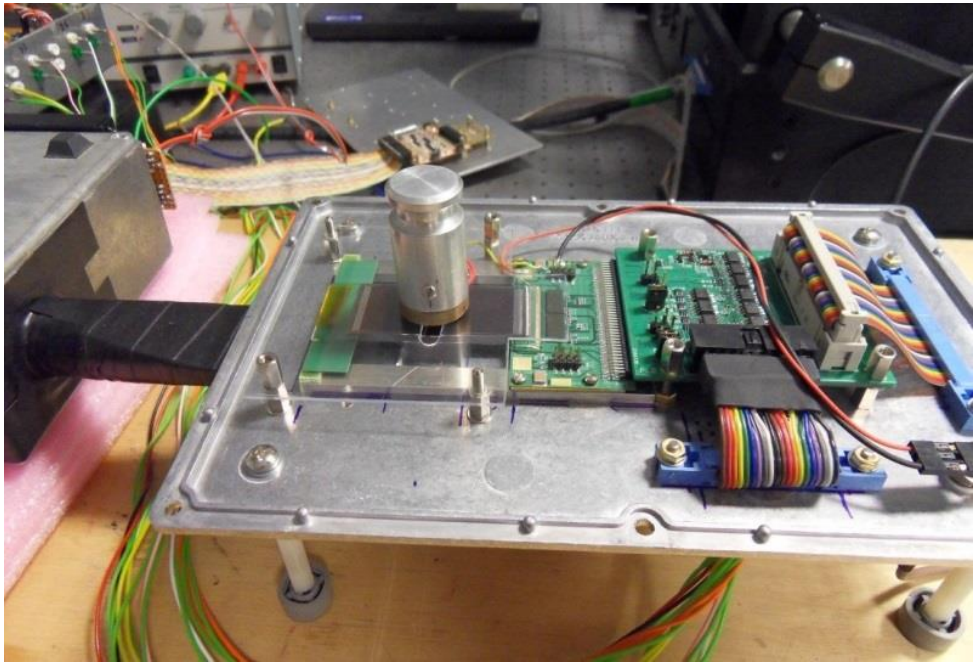
→ Test pulse together with individually-programmable channel masks can be used to fully exercise the coincidence logic

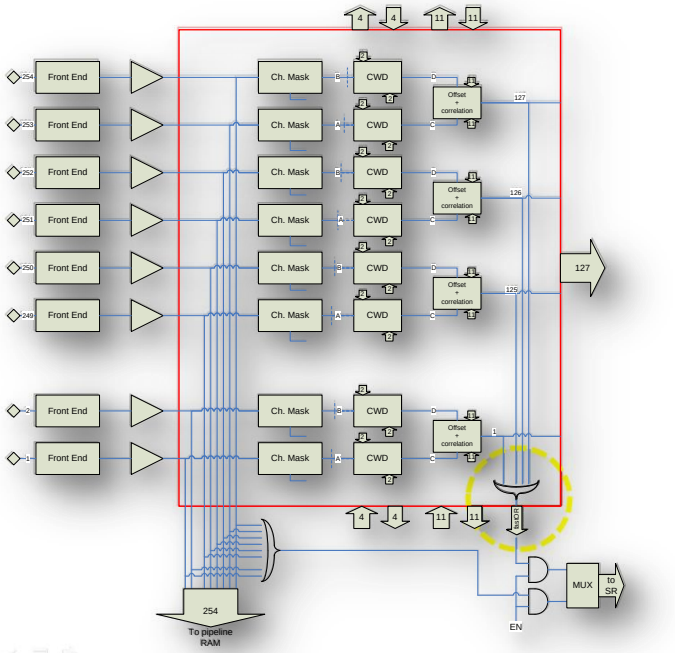
Logic tests using beta source

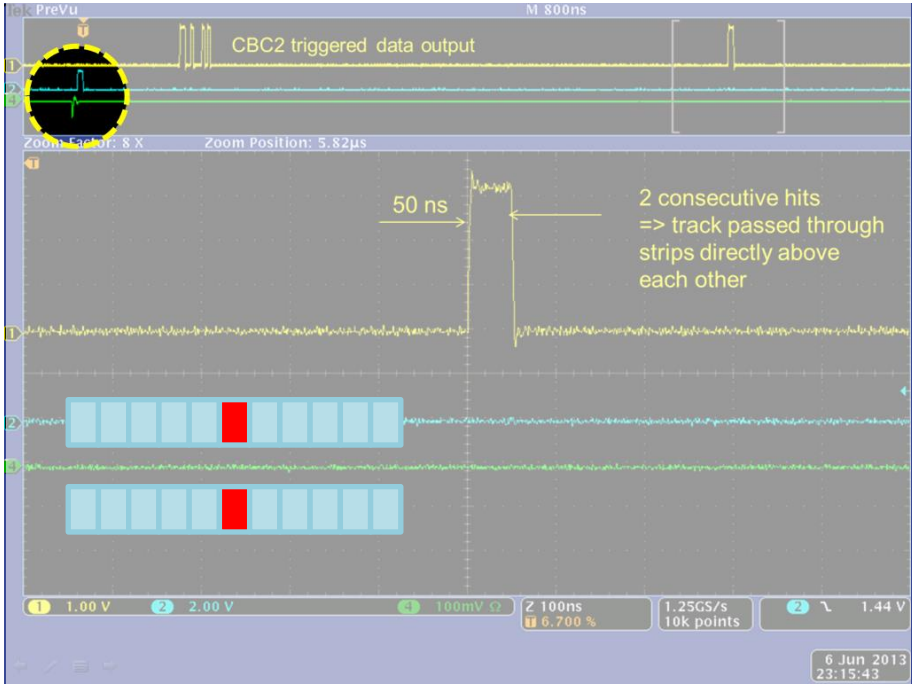


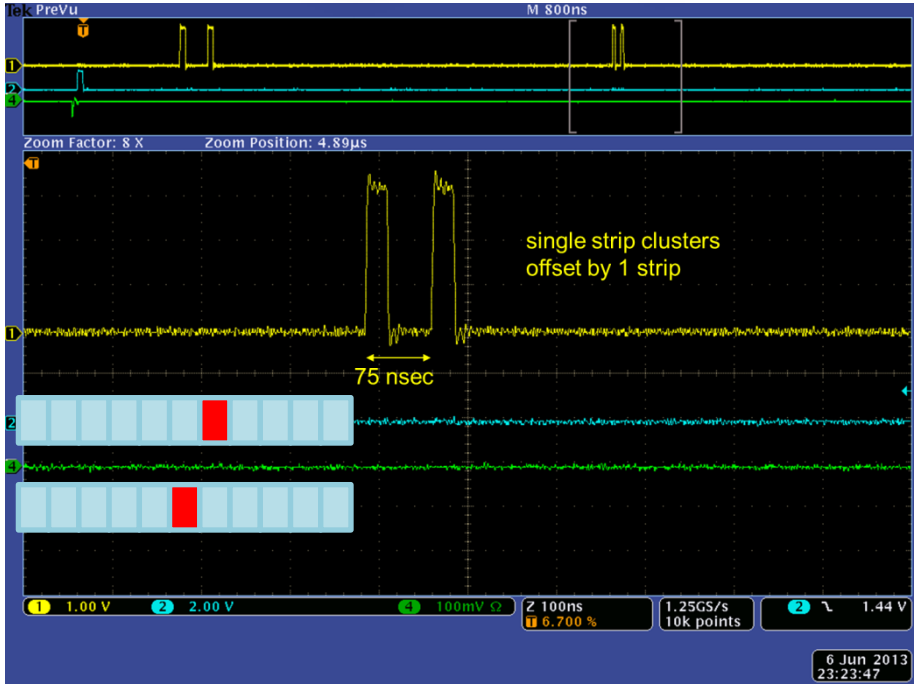


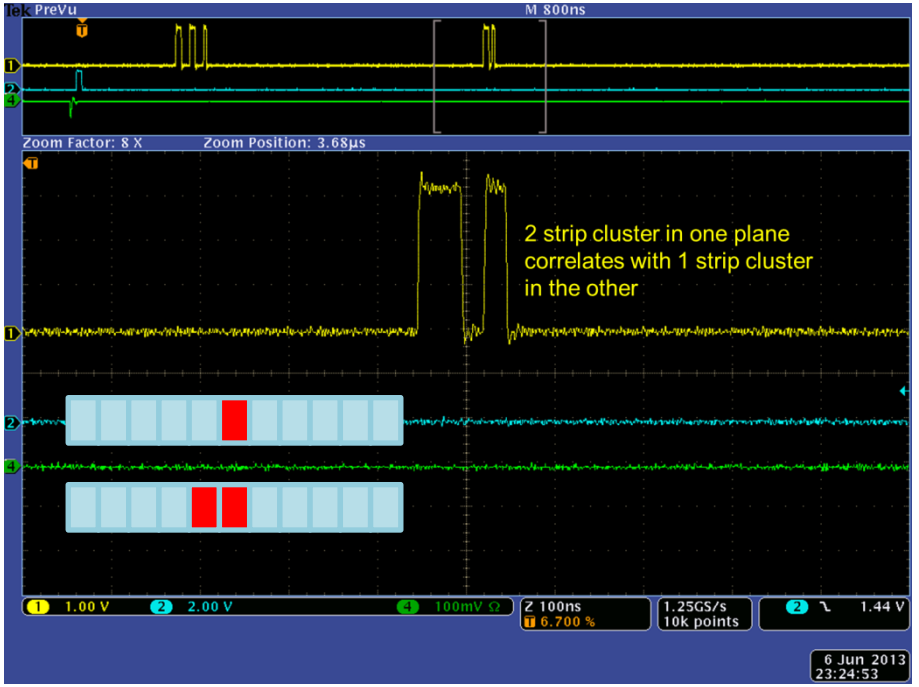





Front End
Ch. Mask
CWD
Offset + correlation
127
126
125
MUX
to SR
254
To pipeline RAM
EN

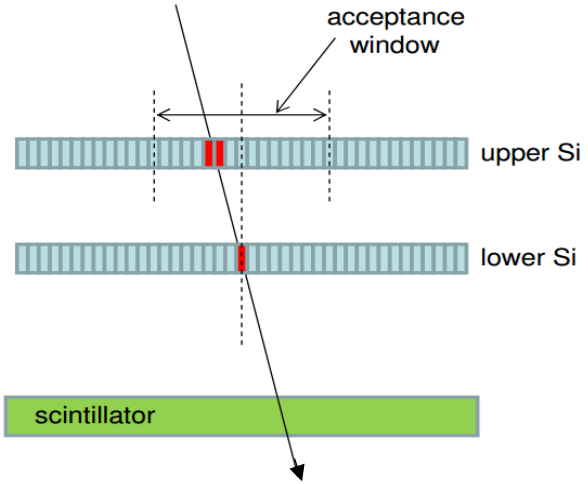

Tek PreVu
M 800ns
CBC2 triggered data output
Zoom Factor: 8 X
Zoom Position: 5.82µs
50 ns
2 consecutive hits
=> track passed through
strips directly above
each other
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:15:43

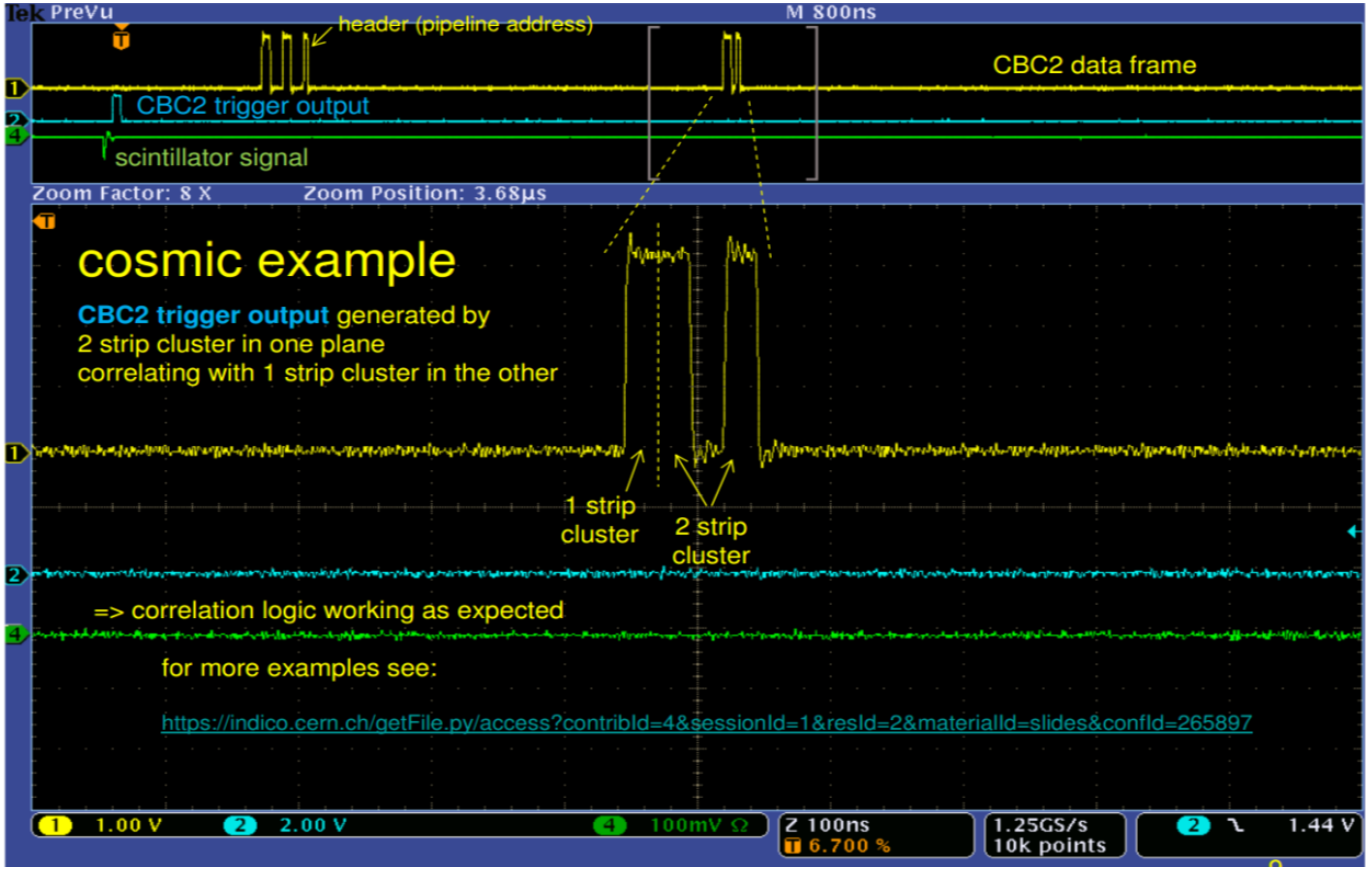

Tek PreVu
M 800ns
Zoom Factor: 8 X
Zoom Position: 4.89µs
single strip clusters
offset by 1 strip
75 nsec
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:23:47


Tek PreVu
M 800ns
Zoom Factor: 8 X
Zoom Position: 3.68µs
2 strip cluster in one plane
correlates with 1 strip cluster
in the other
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:24:53

Logic tests using cosmics

NB: very low rate (<<1Hz) even with maximum coincidence window in upper sensor



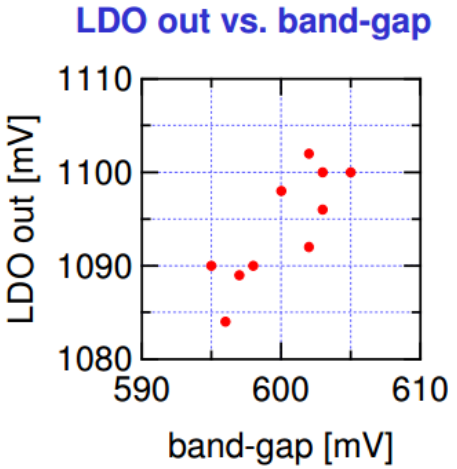


Power elements

Low-dropout linear regulator

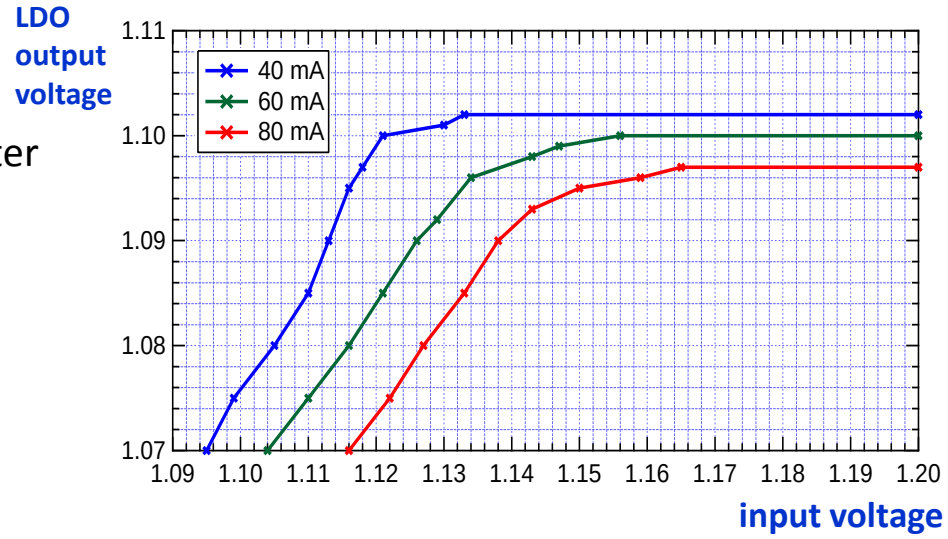
- provides clean, regulated rail to analog FE (uses CERN bandgap) ~ 1.2 Vin, 1.1 Vout
- load currents 40, 60, 80 mA
- dropouts ~ 30, 55, 70 mV (approx.)

DC shift due to series resistance (measured on wire-bonded chip)

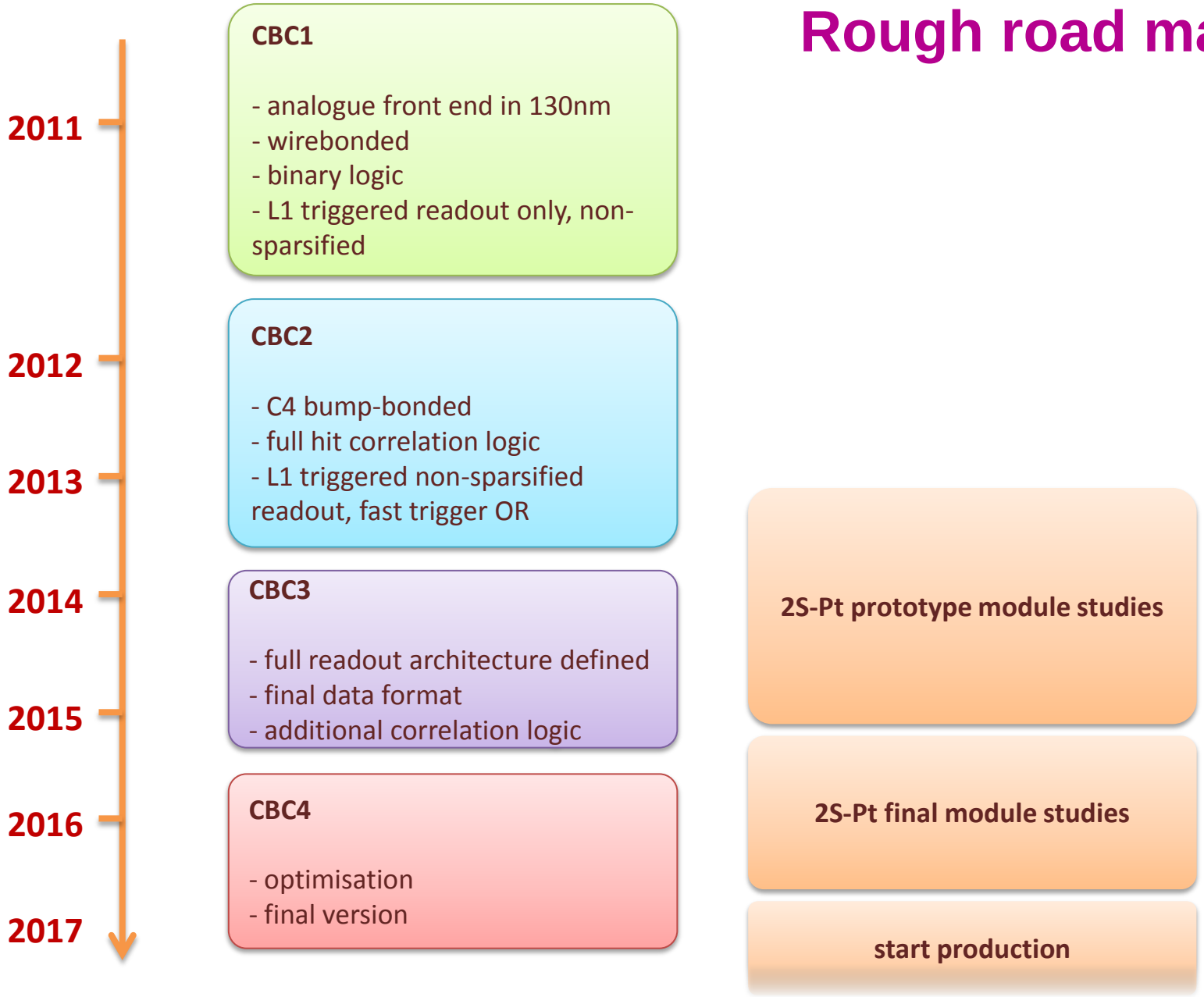


DC-DC:

- CERN on-chip switched capacitor converter
- 2.5V → ~1.2V Can be used to power the CBC2
- Improved version wrt CBC1
- Working but not yet characterized



Rough road map



CBC3 – the “final prototype”

- **final choices for front end**

  Optimized for 5cm strips (possibly longer), AC coupled, n-on-p

- **stub data definition**

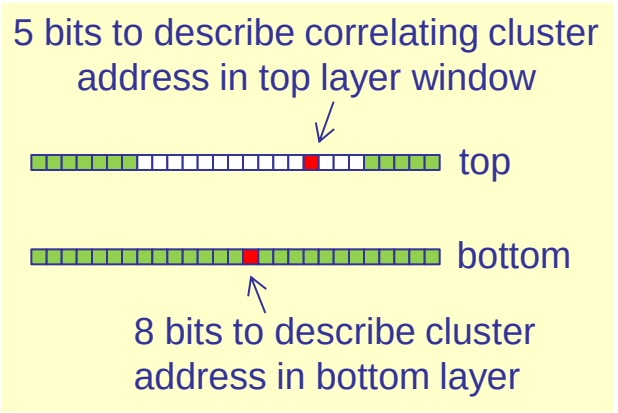
  ½ strip cluster resolution
  Increased max acceptance width from 3 to 4strip clusters
  8b address (for ½ strip resolution) of cluster in bottom layer
  5b for stub bend information (rough Pt)

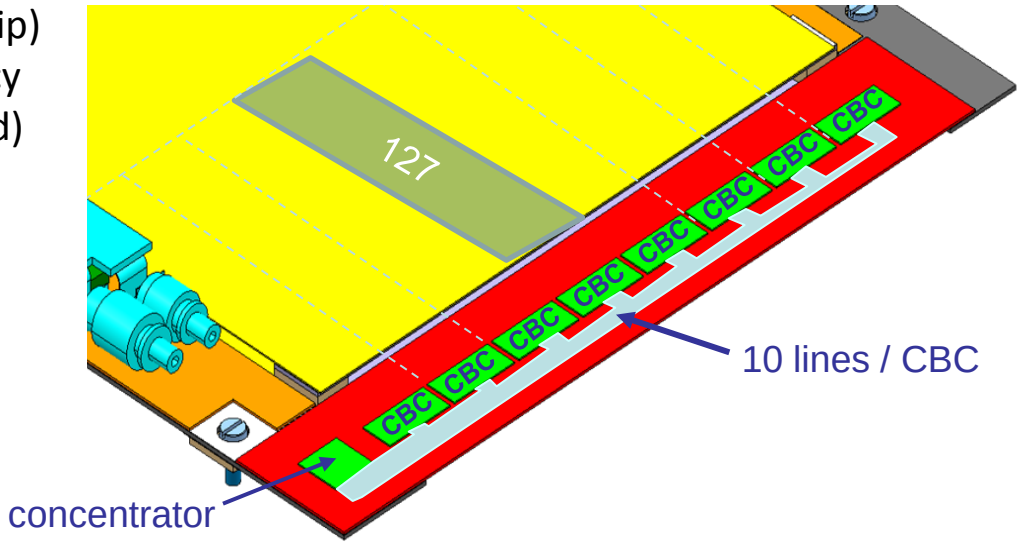
- **stub data formatting & transmission**

  13b/stub, up to 3 stubs/BX => 39 bits
  +1 bit unsparsified L1 triggered readout data
  => 40 bits / 25 nsec
  e.g. 10 lines at 160 Mbps (per chip)
  Designed for final trigger rate & latency
  Priority encoding of Pt stubs (if desired)

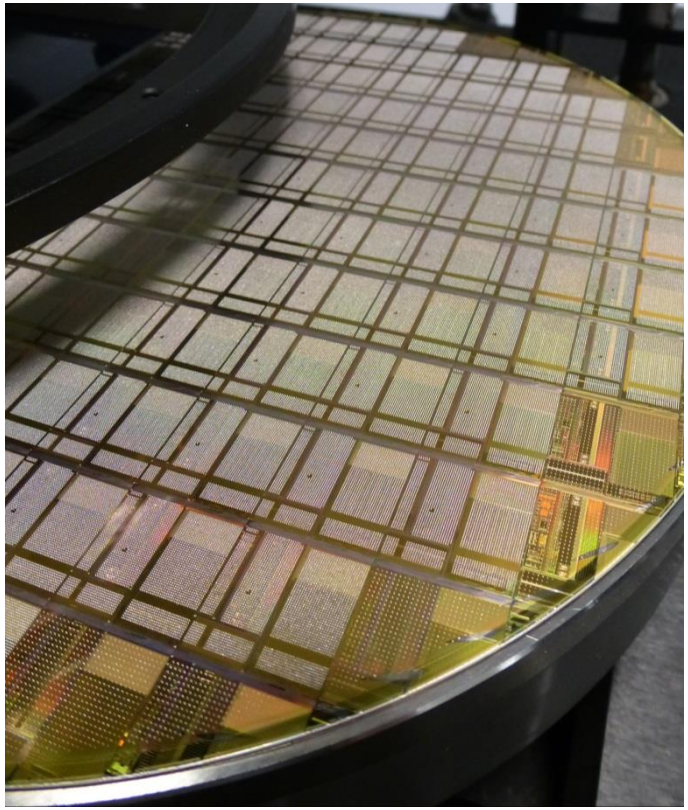
- **other useful features**

  e.g. slow ADC to monitor bias levels
  …





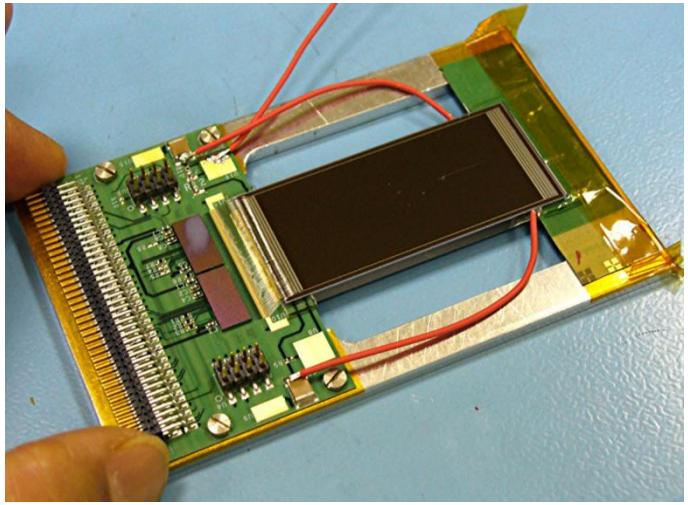
Summary & Conclusions



Two successful full-size prototypes of new Outer Tracker ASIC

- ✓ CBC2 working to specs
- ✓ Some front-end improvements over CBC1
- ✓ Stub finding logic functioning
- ✓ Power features (LDO & DC-DC) operational

First prototype version of 2S module in hand



- ✓ First demonstration of bump-bonded ASIC for strip readout
- ✓ Ready to be distributed to collaborating institutes
- ✓ First beam test foreseen for December 2013
  followed by ionizing radiation and SEU studies