06/02/2023 – Architetture dei Sistemi di Elaborazione C

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Domanda 3

Considerando il programma precedente e l'architettura del processore superscalare descritto in seguito; completare la tabella relativa alle prime 3 iterazioni.
Processor architecture:

- Issue 2 instructions per clock cycle
- jump instructions require 1 issue
- handle 2 instructions commit per clock cycle
- timing facts for the following separate functional units:
  i. 1 Memory address 1 clock cycle
  ii. 1 Integer ALU 1 clock cycle
  iii. 1 Jump unit 1 clock cycle
  iv. 1 FP multiplier unit, which is not pipelined: 6 stages OCCHIO
  v. 1 FP divider unit, which is not pipelined: 6 clock cycles
  vi. 1 FP Arithmetic unit, which is pipelined: 4 stages
- Branch prediction is always correct
- There are no cache misses
- There are 2 CDB (Common Data Bus).

# iteration		Issue	EXE	MEM	CDB x2	COMMIT x2
1	l.d f1,v1(r1)	1	2m	3	4	5
1	l.d f2,v2(r1)	1	3m	4	5	6
1	mul.d f4,f1,f2	2	6x		12	13
1	l.d f3,v3(r1)	2	4m	5	6	13
1	mul.d f4,f4,f3	3	18x		24	25
1	s.d f4,v4(r1)	3	5m			25
1	daddi r2,r2,-1	4	5i		6	26
1	daddui r1,r1,8	4	6i		7	26
1	bnez r2,loop	5	7j			27
2	l.d f1,v1(r1)	6	8m	9	10	27
2	l.d f2,v2(r1)	6	9m	10	11	28
2	mul.d f4,f1,f2	7	12x		18	28
2	l.d f3,v3(r1)	7	10m	11	12	29
2	mul.d f4,f4,f3	8	24x		30	31
2	s.d f4,v4(r1)	8	11m			31
2	daddi r2,r2,-1	9	10i		11	32
2	daddui r1,r1,8	9	11i		13	32
2	bnez r2,loop	10	12j			33
3	l.d f1,v1(r1)	11	14m	15	16	33
3	l.d f2,v2(r1)	11	15m	16	17	34
3	mul.d f4,f1,f2	12	30x		36	37
3	l.d f3,v3(r1)	12	16m	17	18	37
3	mul.d f4,f4,f3	13	37x		43	44
3	s.d f4,v4(r1)	13	17m			44
3	daddi r2,r2,-1	14	15i		16	45
3	daddui r1,r1,8	14	16i		17	45
3	bnez r2,loop	15	17j			46