Circuits Lab 07: MOS Differential Pair

Lisa Joëlle Hachmann, Brenna Manning

April 6, 2016

1 Introduction

In this lab, we examined the current-voltage characteristic of a MOS differential pair, which is widely used as an input stage in operational amplifiers and used in many other types of circuits. This circuit has a relatively large response to change in the difference between its two input voltages, but a relatively small response to change in the average value of its two input voltages.

This lab consisted of one experiment in which we measured the current-voltage characteristics of a differential pair for different values of the common-mode input voltage and as a function of the bias current level. We also examined the behavior of the common-source node voltage. We constructed our circuit from transistors on an ALD1106 quad nMOS transistor array. To establish the proper bulk voltage of the chip, we connected ground to pin 4 and Vdd, 5V, to pin 11.

2 Experiment 1: Differential Pair Current-Voltage Characteristics

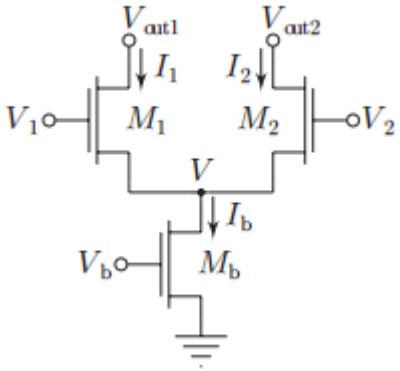

Figure 1: Differential Pair made from nMOS transitors

We constructed an nMOS differential pair from nMOS transistors as shown above. We set the bias voltage, V_b, to 0.6V, so that the bias current was just around threshold, and initially set V_2 to 2V, sufficiently far from the supply rail so that the bias transistor was saturated. With the full power supply across the differential pair, we measured each of the output currents, I_1 and I_2, and the common-source node voltage, V, while sweeping V_1 from a few tenths of a volt below V_2 to a few tenths of a volt above V_2.

We repeated these measurements for $V_2 = 1.5V$ and $V_2 = 2.5V$.

The plot below shows I_1, I_2, I_1-I_2, and $I_1 + I_2$, as a function of V_1-V_2 for all three values of V_2 that we used.

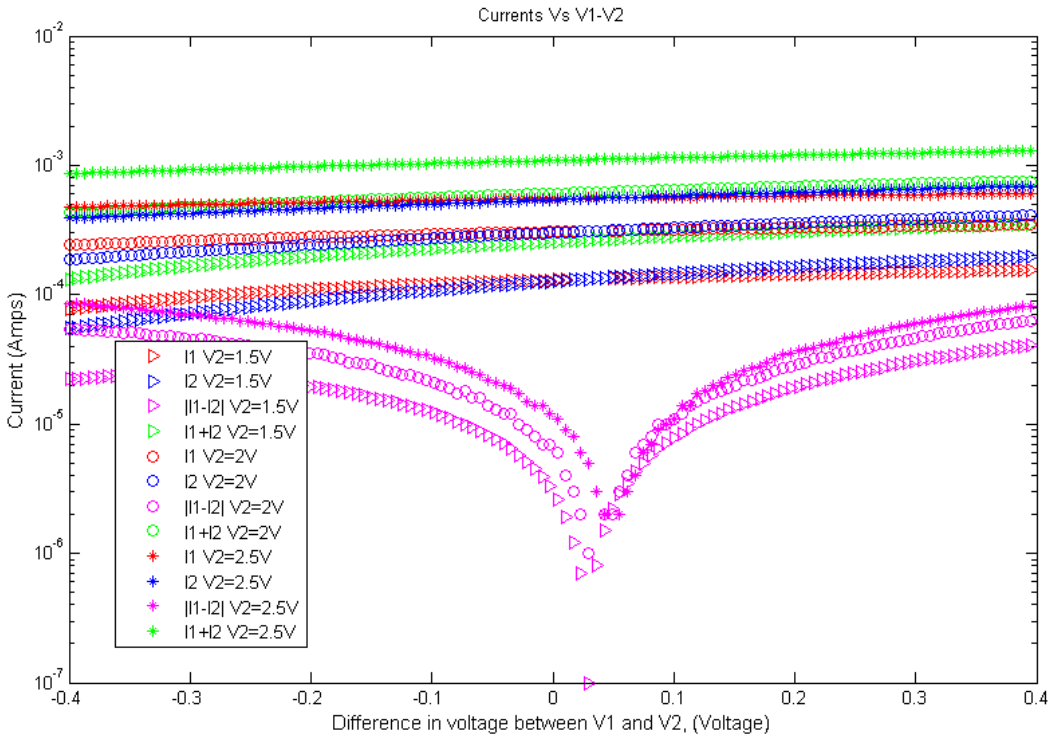

Figure 2: The current characteristics for each transistor (I1 and I2), the sum of the transistor currents and the difference between the transistor currents, for three values of V2.

A lower V2 corresponds to noticeably lower currents I_1 and I_2 than a higher V2, but they each have a similar shape and follow the same behavior. As V2 increases, the current for each transistor, the sum and the difference all increase. They change in significance of about half an order of magnitude with 0.5V increase, consistently. I_1 and I_2 of each transistor cross at around 0V difference between V_1 and V_2. This is clearly shown by the absolute value of $I_1 - I_2$, which decreases as the difference between V_1 and V_2 approaches 0V.

The plot below shows the common-source node voltage, V, as a function of $V_1 - V_2$ for all three values of V_2.

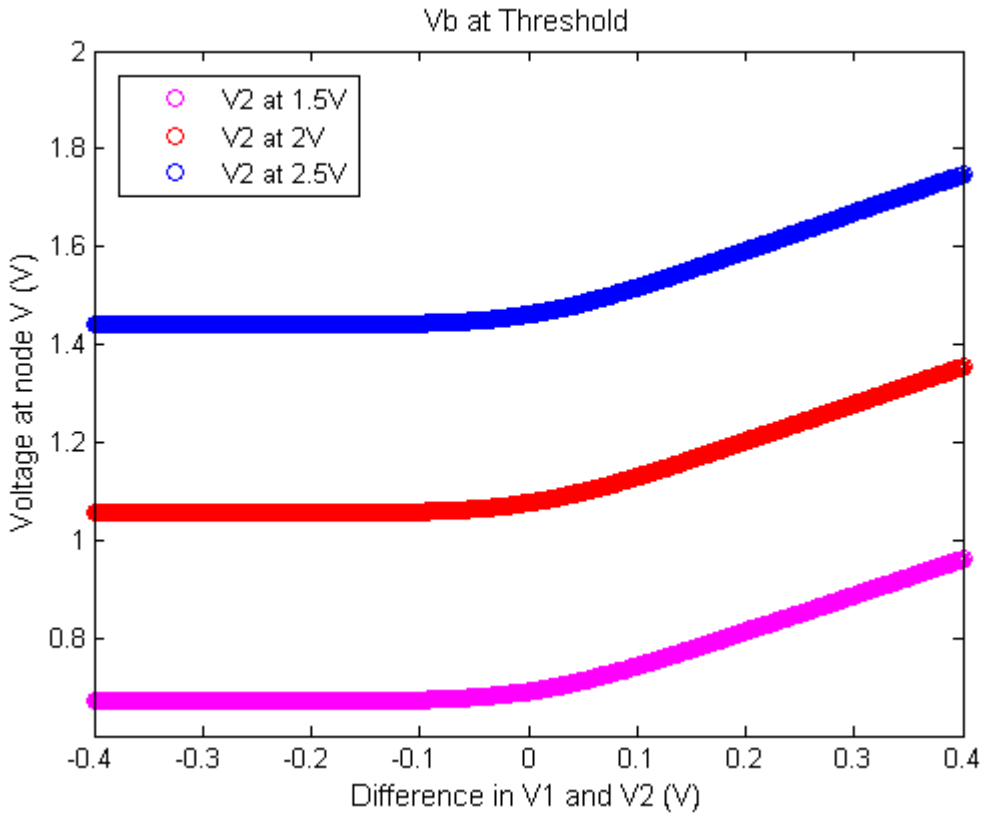

Figure 3: Common Source Node Voltage as a function of the difference between V_1 and V_2.

V does not change as V increases from below V_2 until V_1 approaches the point at which $V_1 = V_2$. Where the difference between V1 and V2 increases after the equilibrium point, where V1 is increasingly greater than V2, the voltage at node V increases.

As seen in the plot below, for each of the three values of V_2 that we used, we fit a straight line to the plot of $I_1 - I_2$ as a function of $V_1 - V_2$ around the region where $V_1 \approx V_2 or (V_1 - V_2 \approx 0)$.

The theoretical fit lines are here:

$$\text{When Vb} = 0.6\text{V and V2} = 1.5\text{V: } (I_1 - I_2) = 1.0e-04(V1 - V2) - 2.6e-06 \quad (1)$$

$$\text{When Vb} = 0.6\text{V and V2} = 1.5\text{V: } (I_1 - I_2) = 1.6e-04(V1 - V2) - 5.3e-06 \quad (2)$$

$$\text{When Vb} = 0.6\text{V and V2} = 1.5\text{V: } (I_1 - I_2) = 2.2e-04(V1 - V2)1.1e-05 \quad (3)$$

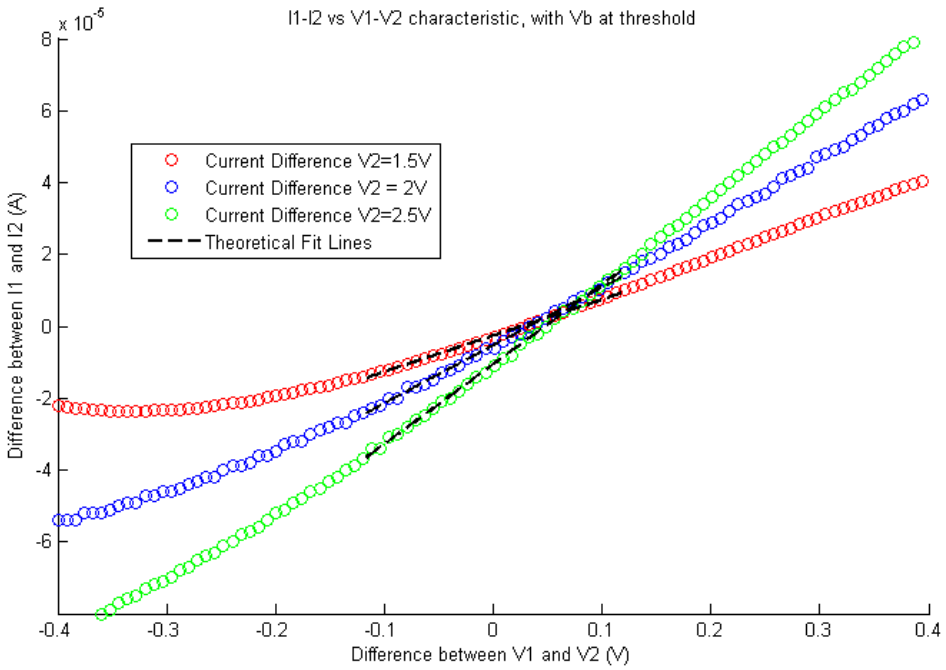

Figure 4: The I_{dm} and V_{dm} graph shows the levels of difference in current with 3 values of V2. As V2 increases, the slope of its characteristics grows steeper. These measurements were done with the bias transistor's gate voltage at threshold voltage (Vb at threshold)

The slope of these lines are approximately equal to the (incremental) differential-mode transconductance gains of each differential pair. The equation for differential mode transconductance gain of a differential pair is:

$$G_{dm} = \frac{\partial(I_{dm})}{\partial(V_{dm})}\bigg|_{V_{dm}=0} = \frac{\partial(I_1 I_2)}{\partial(V_1 V_2)}\bigg|_{V_1=V_2} \tag{4}$$

	Differential mode Transconductance Gain	**Slope of the fit line**
With V2 = 1.5V, Vb = 0.6V	7.913e-5	1e-4
With V2 = 2V, Vb = 0.6V	1.475e-4	1.6e-4
With V2 = 2.5V, Vb = 0.6V	2.125e-4	2.2e-4

Table 1: Comparison of transconductance gain and the slope of the fit line for the difference between V1 and V2 and the difference between I1 and I2

As V_2 changes within a few millivolts, the value of the differential-mode transconductance gain does not change very much, and the slope of the fit line is very consistent. However, at the corners of graph, it hints that V2 is about to flatten out, and then the slope would significantly change.

Next, we set the bias voltage, Vb, to 2V, so that the bias current was above threshold. We performed the same measurements as above for the same three values of V2.

The plot below shows I_1, I_2, I_1-I_2, and $I_1 + I_2$, as a function of V_1-V_2 for all three values of V_2 that we used, when $V_b = 2V$.

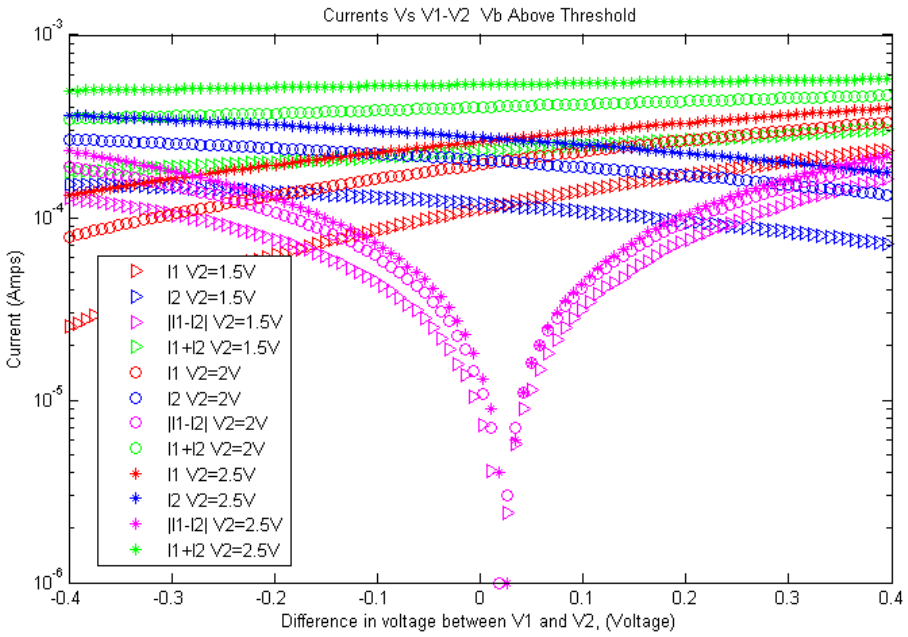

Figure 5: The current characteristics for each transistor (I1 and I2), the sum of the transistor currents and the absolute value of the difference between the transistor currents, for three values of V2, where Vb is above threshold, Vb = 2V.

As seen in figure 5, values of I_1 for each transistor increase as $(V_1 - V_2)$ sweeps from -0.4 to 0.4. The values of I_2 decrease as $(V_1 - V_2)$ sweeps from -0.4 to 0.4, crossing I_1 at a difference in voltage of approximately 0V. The absolute value of the difference between I_1 and I_2 approaches 0 as the difference between V_1 and V_2 approaches 0, and the sums of I_1 and I_2 do not change much as the difference between V_1 and V_2 varies over this range.

A lower V2 corresponds to noticeably lower currents I_1 and I_2 than a higher V2, but they each have a similar shape and follow the same behavior. For $1.5V$ increase in V2, the current level stays within 1 order of magnitude of each other, meaning that the change in V2 has less of an effect on the current level.

The plot below shows the common-source node voltage, V, as a function of $V_1 - V_2$ for all three values of V_2.

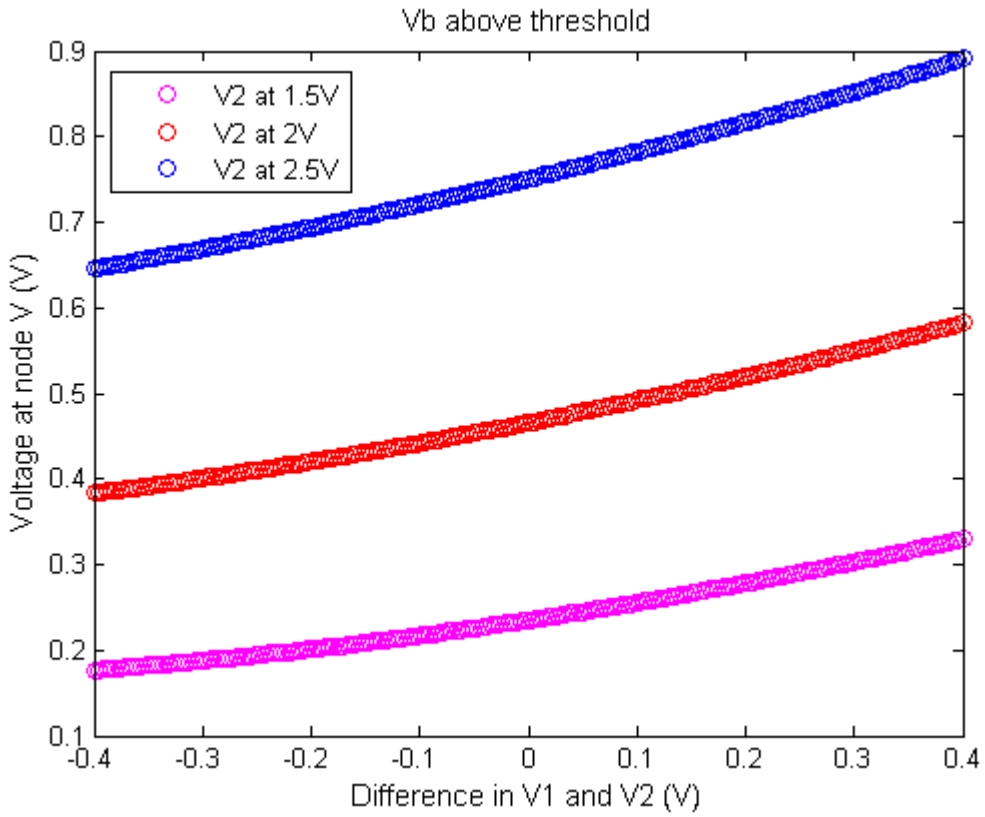

Figure 6: Common Source Node Voltage as a function of the difference between V1 and V2 for Vb above threshold.

The value of V, shown in the plot above, increases as $(V_1 - V_2)$ increases.

As seen in the plot below, for each of the three values of V_2 that we used, we fit a straight line to the plot of $I_1 - I_2$ as a function of $V_1 - V_2$ around the region where $V_1 \approx V_2 or (V_1 - V_2 \approx 0)$.

The theoretical fit lines are:

$$\text{When Vb} = 2\text{V and V2} = 1.5\text{V: } (I_1 - I_2) = 3.8e-04(V1 - V2) - 7.2e-06 \quad (5)$$

$$\text{When Vb} = 2\text{V and V2} = 2\text{V: } (I_1 - I_2) = 5.1e-04(V1 - V2) - 1.1e-05 \quad (6)$$

$$\text{When Vb} = 2\text{V and V2} = 2.5\text{V: } (I_1 - I_2) = 5.8e-04(V1 - V2) - 1.4e-05 \quad (7)$$

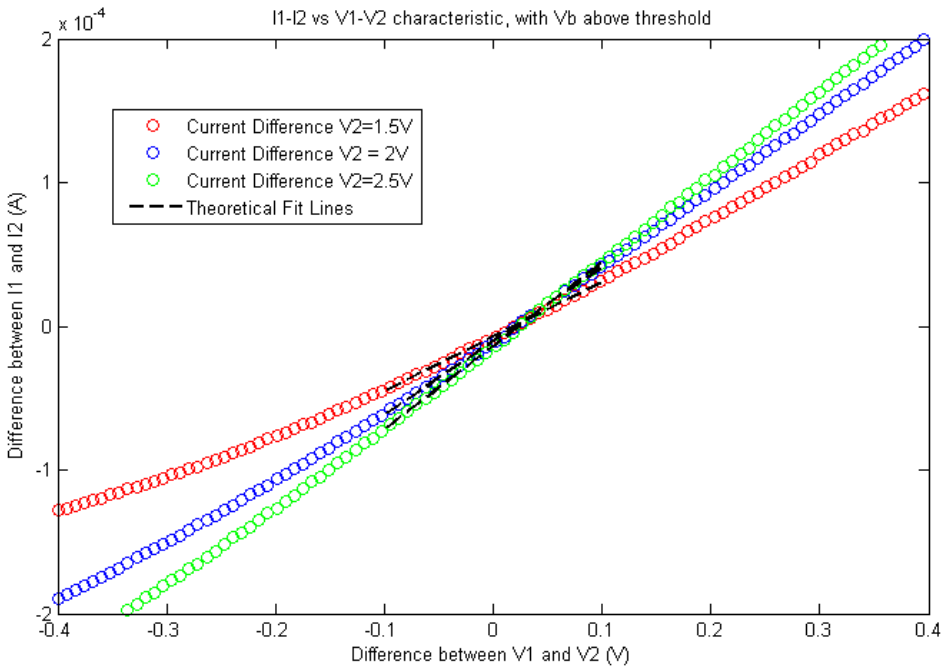

Figure 7: The I_{dm} and V_{dm} graph shows the levels of difference in current with 3 values of V2. As V2 increases, the slope of its characteristics grows steeper. These measurements were done with the bias transistor's gate voltage at threshold voltage (Vb above threshold)

	Differential mode Transconductance Gain	**Slope of the fit line**
With V2 = 1.5V, Vb = 2V	8.664e-5	3.8e-4
With V2 = 2V, Vb = 2V	3.769e-4	5.1e-4
With V2 = 2.5V, Vb = 2V	3.971e-4	5.8e-4

Table 2: Comparison of transconductance gain and the slope of the fit line for the difference between V1 and V2 and the difference between I1 and I2

The transconductance gains are still similar to the slope of the lines at around $V1 \approx V2$, however they are also very similar to the values found for when the bias voltage is at threshold.

The circuit behaves significantly differently when bias current is in strong inversion rather than weak inversion. When the bias voltage is increased so the bias current is in strong inversion, the bias current level increases, increasing the node voltage (the source voltage of both M1 and M2), and decreasing the current levels of both M1 and M2.

When the bias current is in the weak/moderate inversion changing V_2 causes a greater change in current. For example, in comparing Figure 2 and Figure 5, we see that when Vb is below threshold, the sum of the output currents for a V2 of 2.5 is a whole order of magnitude greater than the sum of the output currents for a V2 of 1.5. This difference is much less when Vb is above threshold.

The circuit also differs in the values of the voltage at node V as V1-V2 varies. Comparing Figures 3 and 6, we can see that when in weak/moderate inversion, the voltage at node V does not even start increasing until V1-V2 is positive, while in strong inversion, when Vb is above threshold,

the voltage at node V was increasing throughout the entire sweep.

A difference in behavior between weak/moderate and strong inversion is visible when comparing Figures 4 and 7, the difference in currents as a function of the difference in voltage. We see again that when bias current is in weak/moderate inversion, the difference in currents is smaller than when it is in strong inversion. Additionally, within the range of voltage differences we swept, as the difference between V1 and V2 increases, the rate of change of the current difference decreases sooner and more visibly when in weak/moderate inversion than in strong inversion.