Final Project: **Building & Analyzing SR Latch**

Lisa Hachmann and Brenna Manning

We plan to use transistors to construct 2-3 different SR Latches of varying complexity, and compare their behavior. We have found example schematics (shown below) of SR-Latches made up of as few as six and as many as twelve transistors.

We would like to look into how well the simpler SR Latch works as well as explore in what ways the more complex SR-Latches perform either differently or better.

Things to explore for each latch:

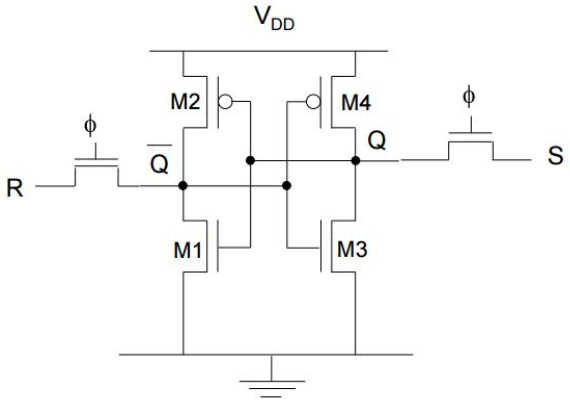
What minimum voltage counts as high?
What is the delay when changing from high to low or vice versa?

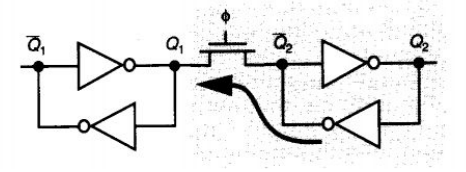
Stretch Goal:
What is the distribution of time to leave the metastable state? (S and R both high) Does it appear to be random?

Relevant resources:
Memory and Latch circuits by University of Puerto Rico, Mayaguez
http://www.ece.uprm.edu/~mtoledo/4207/F2011/set8
Sequential Logic by Purdue University
https://engineering.purdue.edu/~vlsi/ECE559_Fall09/Notes/SequentialLogic.pdf
Sequential CMOS Logic Circuits by Western Engineering
http://www.engga.uwo.ca/people/adounavis/courses/ece480a/notes/ece480_chap5.pdf
Metastability by University of Southern California
http://www-classes.usc.edu/engr/ee-s/552/coursematerials/ee552-G1.pdf

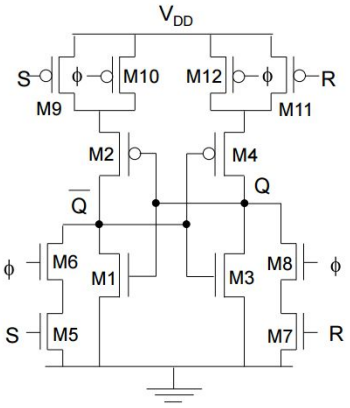
Schematics:

6-Transistor SR Flip-Flop





Complementary CMOS SR Flip-Flop



Eliminates pseudo-NMOS inverters
⇒ Faster switching and smaller transient current

CMOS Clocked SR Flip-Flop