Circuits Lab 08: A Simple MOS Differential Amplifier

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1 Introduction

In this lab, we examined the voltage transfer characteristics and output-voltage swing of a simple MOS differential amplifier comprising an nMOS differential pair and a simple pMOS current mirror (schematic shown below). We also measured its incremental voltage gain, its incremental transconductance gain, and its output incremental output resistance. We also examined the voltage transfer characteristics of our amplifier configured as a unity-gain follower.

This lab consisted of three experiments. In the first experiment, we examined the behavior of the differential amplifier in response to changes in the common-mode input voltage and the differential-mode input voltage. In the second experiment, we measured the incremental output resistance of the differential amplifier and its incremental transconductance gain. We also computed the differential-mode voltage gain of the circuit in two different ways. In the third experiment, we examined the voltage transfer characteristic of our amplifier configured as a unity-gain follower.

We constructed each of our circuits from transistors on an ALD1106 quad nMOS transistor array and transistors from an ALD1107 quad pMOS transistor array. Because MOS transistors are four-terminal devices, we connected ground to pin 4 and Vdd to pin 11 on both the ALD1106 and the ALD1107 to maintain proper bulk voltages.

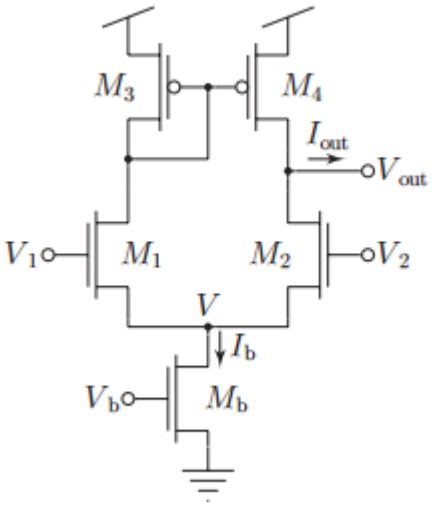

Figure 1: A simple MOS differential amplifier

2 Experiment 1: Voltage Transfer Characteristics

For this experiment, we constructed a differential amplifier with an nMOS differential pair and a pMOS current mirror. We set the bias voltage to 0.6V so that the bias current was just at threshold. We connected V2 to a constant voltage source, set to 2.5V using a potentiometer and swept V1 rail to rail from 0V to 5V while meauring Vout. We repeated this sweep for two more values of V2: 3.5V and 4.5V. The plot below shows all of these voltage transfer characteristics.

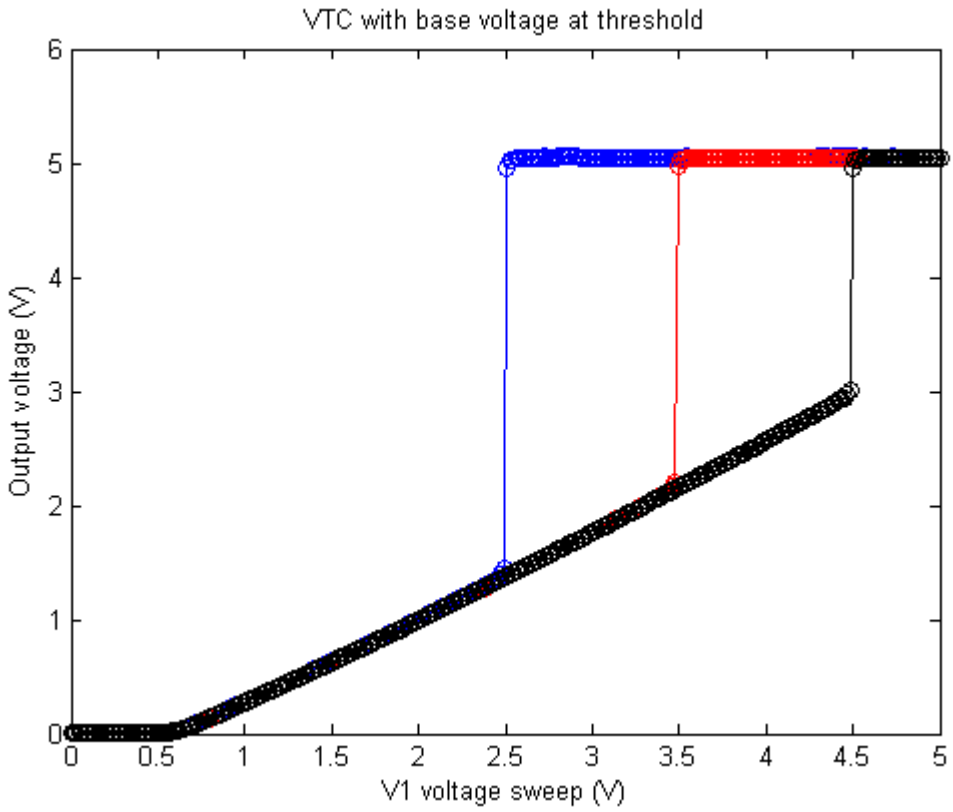

Figure 2: Plot showing all three voltage transfer characteristics with bias voltage at threshold. Blue: V2=2.5, Red: V2=3.5, Black: V2=4.5

Next, we repeated this same experiment for an above-threshold bias current of 1.5V. The plot below shows the voltage transfer characteristics found when $V_b = 1.5V$.

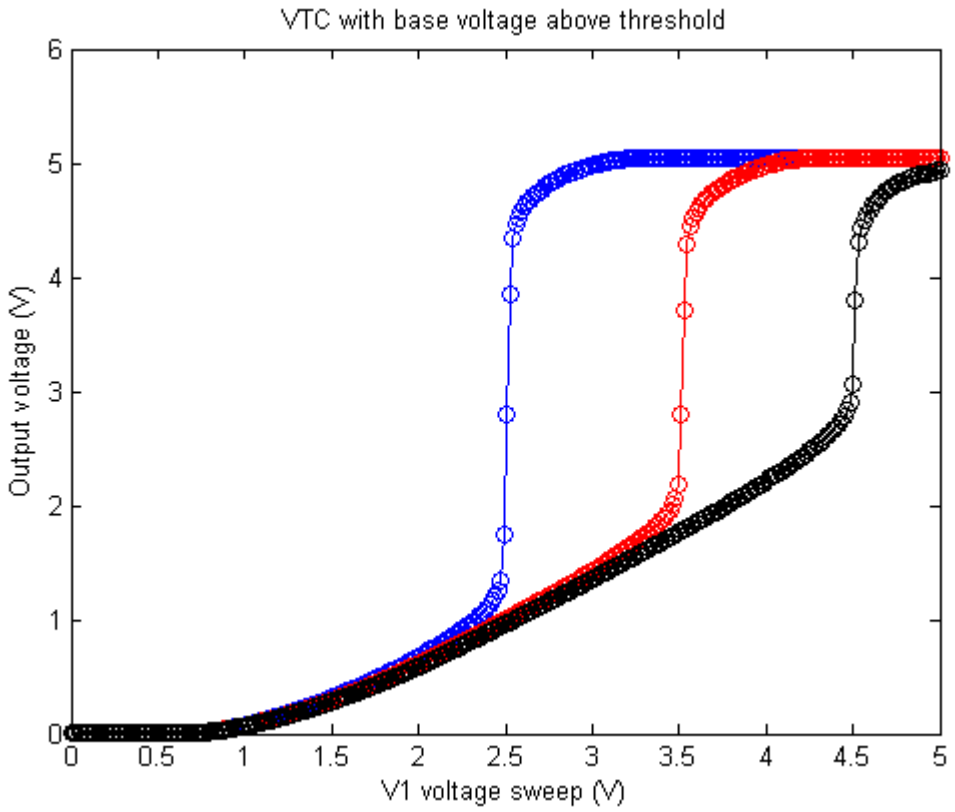

Figure 3: Plot showing all three voltage transfer characteristics with bias voltage above threshold. Blue: V2=2.5, Red: V2=3.5, Black: V2=4.5

The behavior of the circuit does differ substantially when biased in strong inversion compared to when it is in weak or moderate inversion. When biased in strong inversion, the slope, while still close to vertical, is less steep than in weak inversion.. Also, what appears to be an immediate change when the circuit is biased in weak/moderate inversion, is more gradual, and curves can be seen in the shape of the plot for strong inversion.

3 Experiment 2: Transconductance, Output Resistance and Gain

In this experiment, for $V_2 = 2.5V$, we swept V1 around V2 in fine increments while measuring Vout. As seen below, we fit a straight line to the steep part of the curve. The slope of this best-fit line was used to determine the differential-mode voltage gain of our circuit.

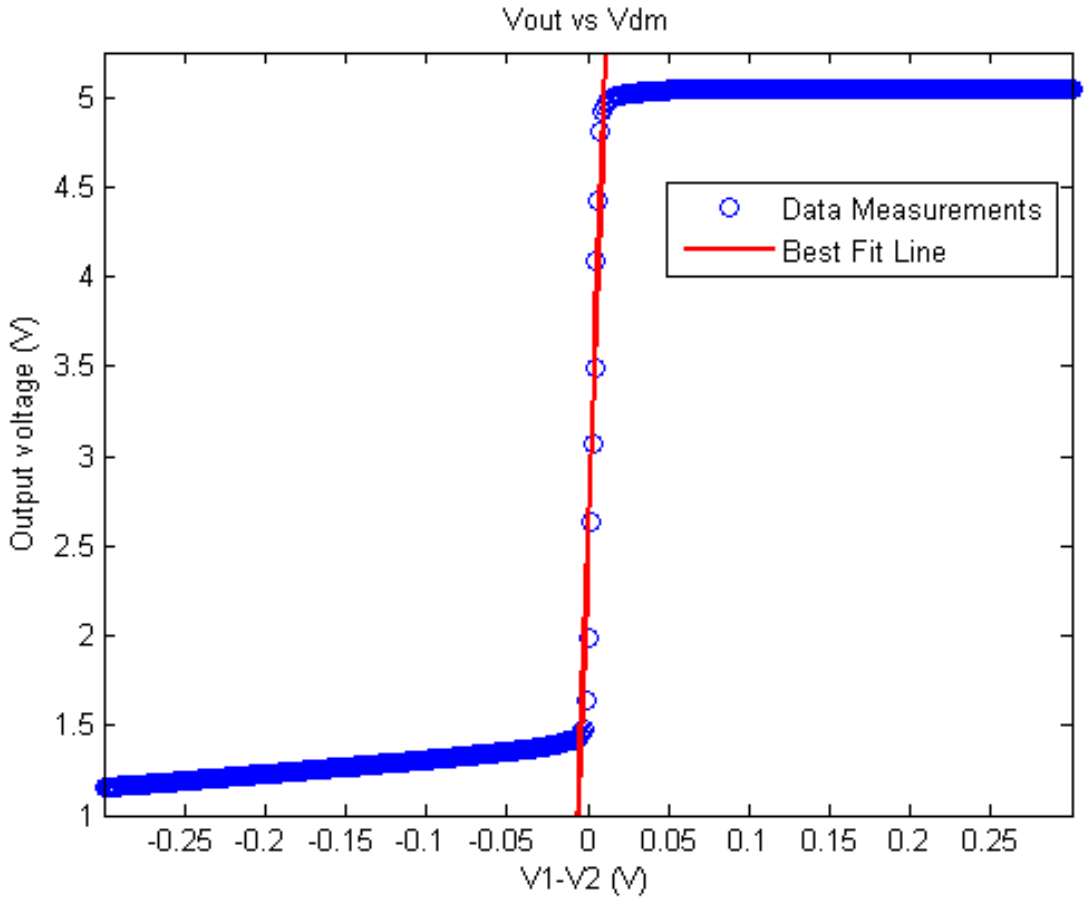

Figure 4: Plot showing Vout vs Vdm along with the best fit line

The theoretical best fit line is:

$$y = 250.326 \cdot x + 2.4143 \tag{1}$$

The differential-mode voltage gain is the slope of the line in figure 4.

$$A_{dm} = \frac{V_{out}}{V_{dm}} \tag{2}$$

$$A_{dm} = 250 \tag{3}$$

Next, we set the differential-mode input voltage to zero and measured the current flowing into the output of the amplifier as we swept Vout from one rail to the other. As seen below, we fit a straight line to the shallow part of this output current-voltage characteristic. This shallow range corresponds to the range of output voltages over which the gain of the circuit is large. From the slope of this line, we determined the incremental output resistance of the circuit.

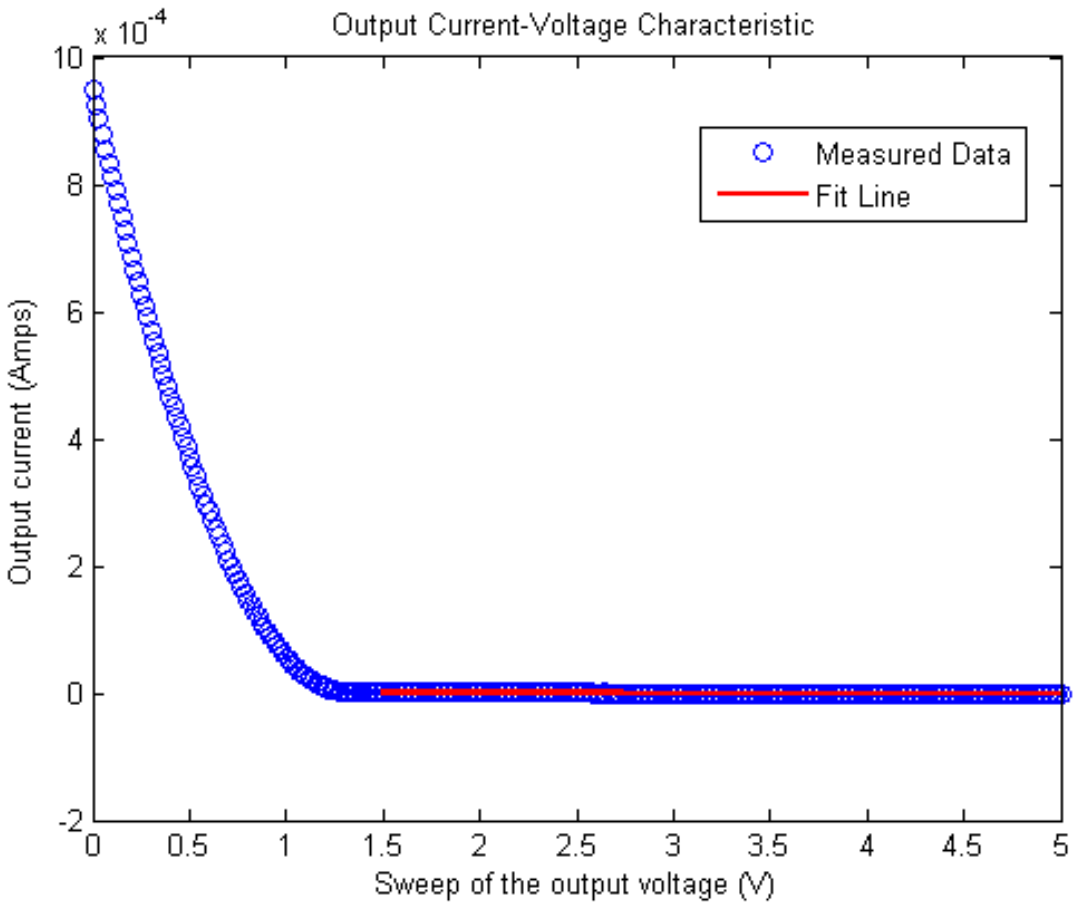

Figure 5: Plot showing output current-voltage characteristic along with the best-fit line

The theoretical best fit line is:

$$y = -1.129 \cdot 10^{-8} \cdot x + 3.081 \cdot 10^{-8} \tag{4}$$

The slope of the data in figure 5 is $\frac{I_{out}}{V_{out}}$, which would correspond to $\frac{1}{R_{out}}$, so flipping this, we find that the incremental output resistance is:

$$R_{out} \approx -8.9 \cdot 10^{7} \tag{5}$$

Next, we fixed the output voltage to be 2V, so that it would be in the middle of the range of output voltages for which the current's gain is large. We measured the current flowing out of the amplifier as we swept V1 around V2. We fit a straight line to the curve around where V1 = V2, and we extracted a value of the incremental transconductance gain of the circuit with the output voltage fixed.

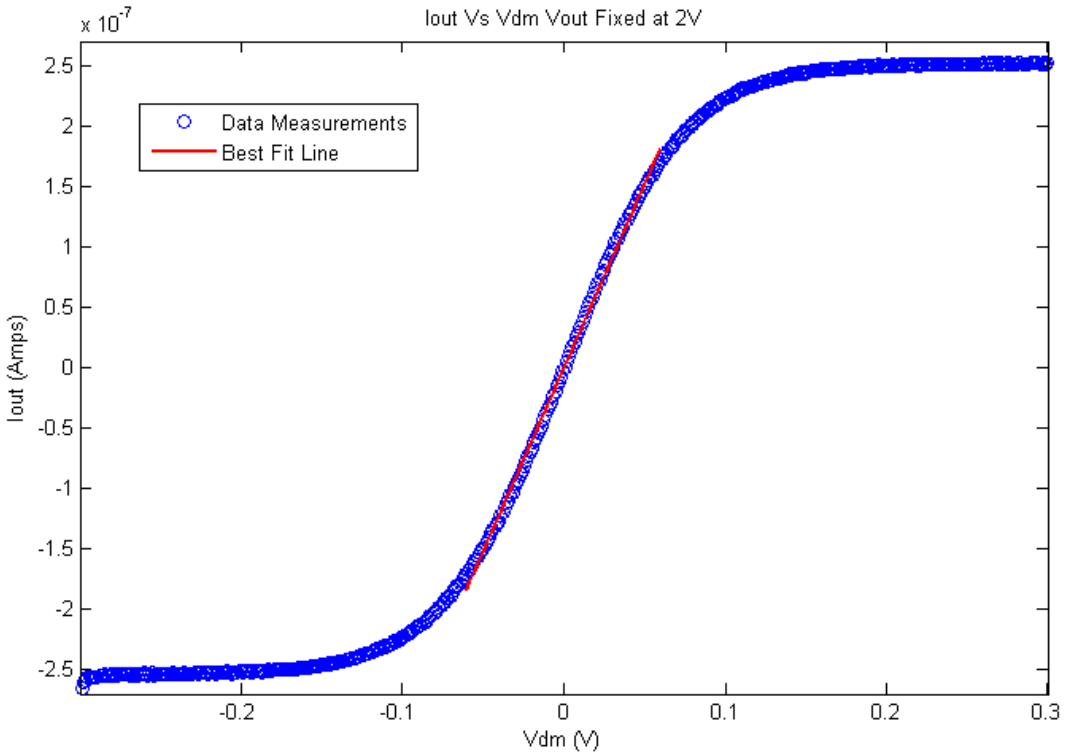

Figure 6: Plot showing Iout vs Vdm along with the best-fit line

The theoretical fit line is:

$$y = 3.036 \cdot 10^{-6} \cdot x - 1.43 \cdot 10^{-10} \tag{6}$$

Incremental transconductance gain with output voltage fixed is the slope of the line around where $V1 \approx V2$:

$$G_m = 3.036 \cdot 10^{-6} \tag{7}$$

The equation for the incremental differential-mode voltage gain of the circuit can be written as:

$$A_{dm} = \frac{\partial V_{out}}{\partial V_{dm}} = \frac{\partial V_{out}}{\partial I_{out}} \cdot \frac{\partial I_{out}}{\partial V_{dm}} = R_{out} \cdot G_m \tag{8}$$

From our incremental output resistance and our incremental transconductance gain, we computed the differential-mode voltage gain of our circuit.

$$A_{dm} = R_{out} \cdot G_m \tag{9}$$

$$Rout = 8.9 \cdot 10^7 \Omega \tag{10}$$

$$G_m = 3.036 \cdot 10^{-6} \mho \tag{11}$$

$$A_{dm} = 271 \tag{12}$$

The value of the calculated differential-mode gain (271) is very similar to the value of the differential-mode gain found from the slope of the VTC (250).

4 Experiment 3: Unity-Gain Follower

For this experiment, we configured our amplifier as a unity-gain follower by connecting the output to the inverting input terminal. We measured Vout as we swept Vin from one rail to the other. As shown below, we fit a straight line to the VTC obtained from this sweep.

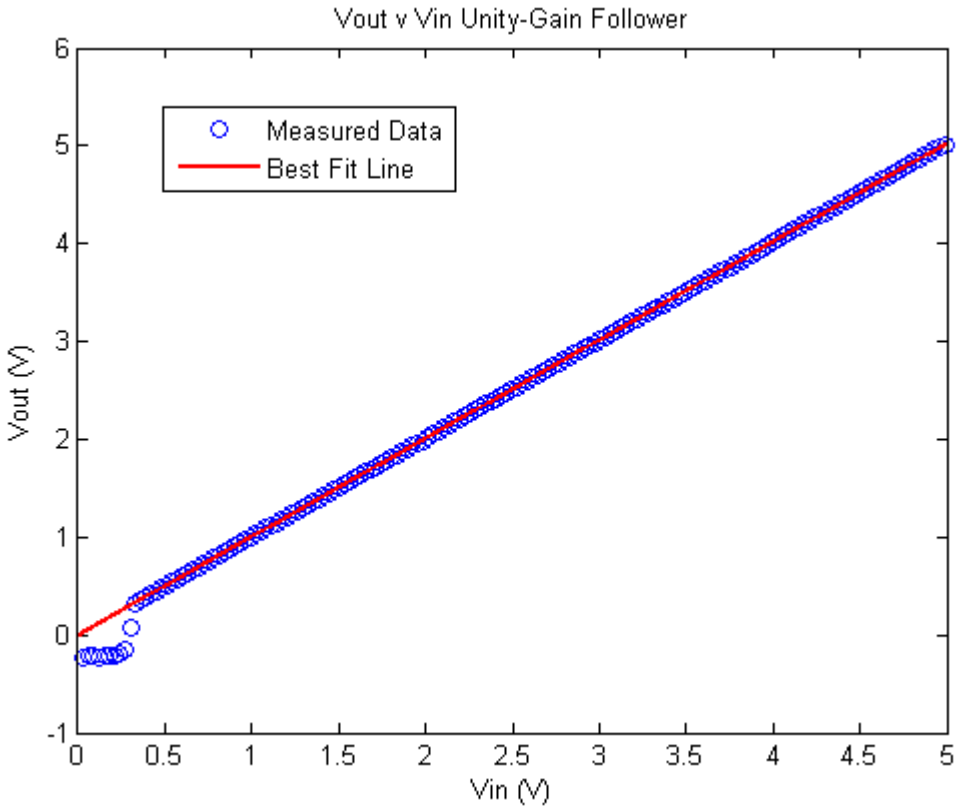

Figure 7: Plot showing Vout vs Vin along with the best fit line

The incremental gain is close to unity, as the slope of the best fit line = 1.005.

Finally, we repeated the sweep of the input voltage while measuring offset voltage (the difference between the output and input voltages) directly.

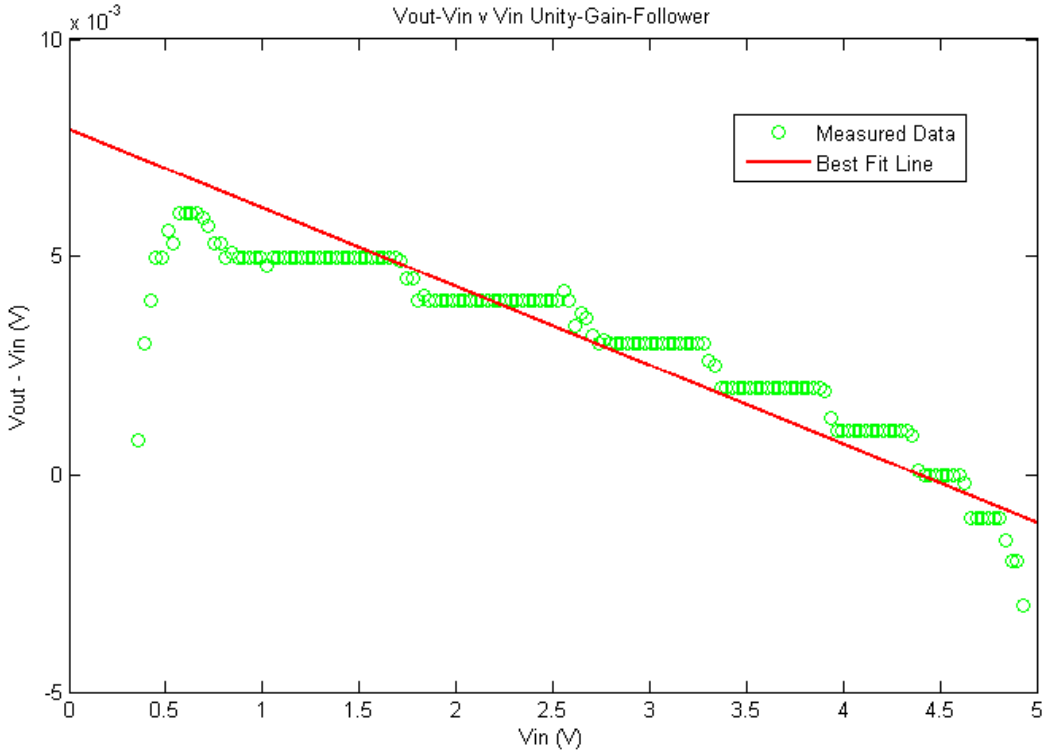

Figure 8: Plot showing Vout-Vin vs Vin along with the best fit line

Figure 8 represents the offset voltage of our amplifier. As the input voltage increases, the offset voltage decreases to no difference. The data taken before the input voltage is 0.7, the offset voltage isn't significant because the transistors are cutoff and not yet passing current. The steps seen in the figure are a result of the resolution of the measuring unit, and not of the data. We believe that the data would look more like the best fit line if measured with a measuring unit with finer resolution. Note that the largest offset voltage (when $V_{in} \approx 1V$) is only ≈ 5 mV.