Circuits Lab 06: Series/Parallel MOS Networks and MOS Current Dividers

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1 Introduction

In this lab we examined the characteristics of closely matched MOS transistors connected in series and in parallel, and we examined the characteristics of simple MOS current divider circuits made from closely matched MOS transistors. This lab consisted of three experiments. In the first experiment we examined the current-voltage characteristics of each of the four transistors on our ALD1106 quad nMOS transistor chip to see how well their characteristics match. In the second experiment, we examined the current-voltage characteristics of pairs of matched transistors in series and in parallel in various operating regimes. In the third experiment we constructed current dividers out of MOS transistors and examined their current transfer characteristics.

In the following experiments, we constructed each of these circuits from transistors on an ALD1106 quad nMOS transistor array. In each experiment, pin 4 of the ALD1106 was connected to ground and pin 11 was connected to Vdd, 5V, in order to establish proper bulk voltage for the chip.

2 Experiment 1: Transistor Matching

For each of the four transistors on our ALD1106 chip, we measured channel current as a function of gate voltage with the source voltage at ground and the drain voltage at Vdd.

We fit the EKV model to each of these characteristics and extracted a value of Is, κ, and VT0 for each transistor. These values are shown in the table below.

Transistor	Kappa (κ)	Specific current (Is) (A)	Threshold voltage (Vt) (V)
M1	0.5562	1.9649e-6	0.517
M2	0.6243	1.881e-6	0.635
M3	0.6469	1.8841e-6	0.6487
M4	0.6749	1.7388e-6	0.6474

Table 1: Extracted parameters of the EKV fit for all 4 transistors

The semilog plot below shows the current-voltage characteristics for all four transistors on the array along with their theoretical EKV fits.

The EKV fits were as follows:

$$I_{Q1} = Is1 * log(1 + e^{(\kappa_1(Q1_{Vg} - Q1_{V_t})/2U_t)2} \quad (1)$$

$$I_{Q2} = Is1 * log(1 + e^{(\kappa_2(Q2_{Vg} - Q2_{V_t})/2U_t)2} \quad (2)$$

$$I_{Q3} = Is1 * log(1 + e^{(\kappa_3(Q2_{Vg} - Q3V_t)/2U_t)2} \quad (3)$$

$$I_{Q4} = Is1 * log(1 + e^{(\kappa_4(Q2_{Vg} - Q4_{V_t})/2U_t)2} \quad (4)$$

The EKV model fits the measurements incredibly well, although it is easy to see that M1's parameters and fit are very different from the rest of the transistors. The theoretical fit lines for M2, M3 and M4 were nearly identical, as were the measurements, and they overlay themselves on the graph.

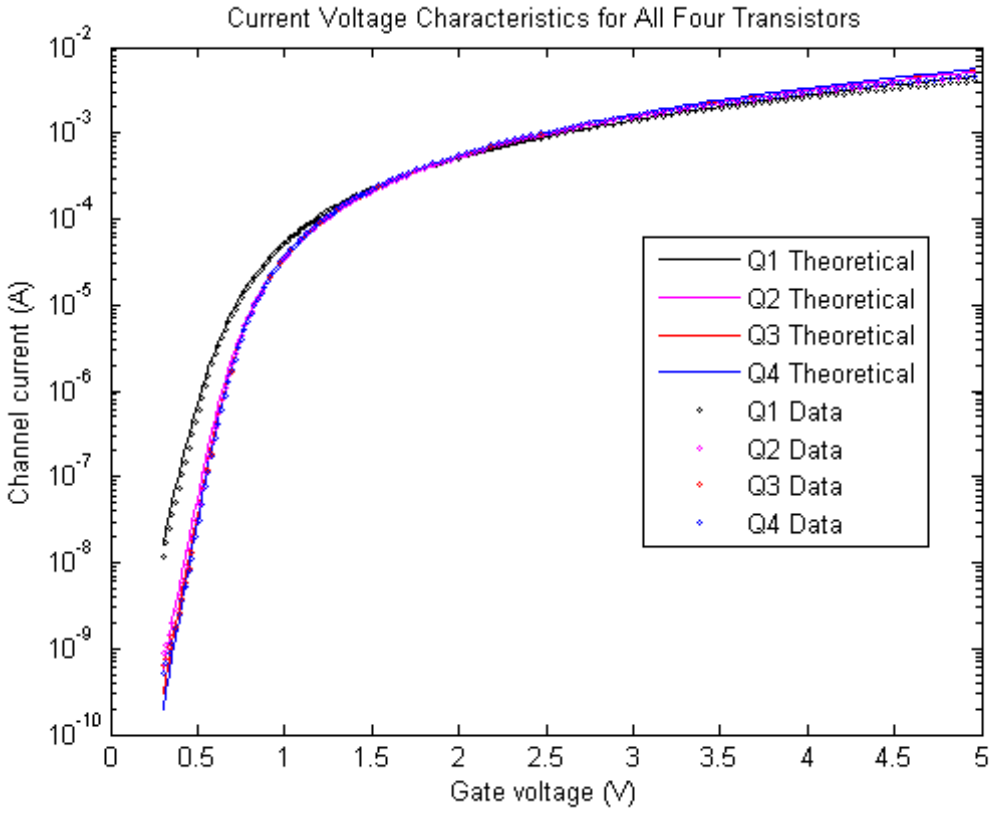

Figure 1: A single semilog plot showing all four current-voltage characteristics along with their fits.

The semilog plot below shows the percentage difference between the channel currents for each transistor and the mean value of all four channel currents as a function of the mean value of all four channel currents. We saw that M1, the first transistor we collected data from in the array, was not matched nearly as well as the others. Because of this, in later experiments we chose not to use M1.

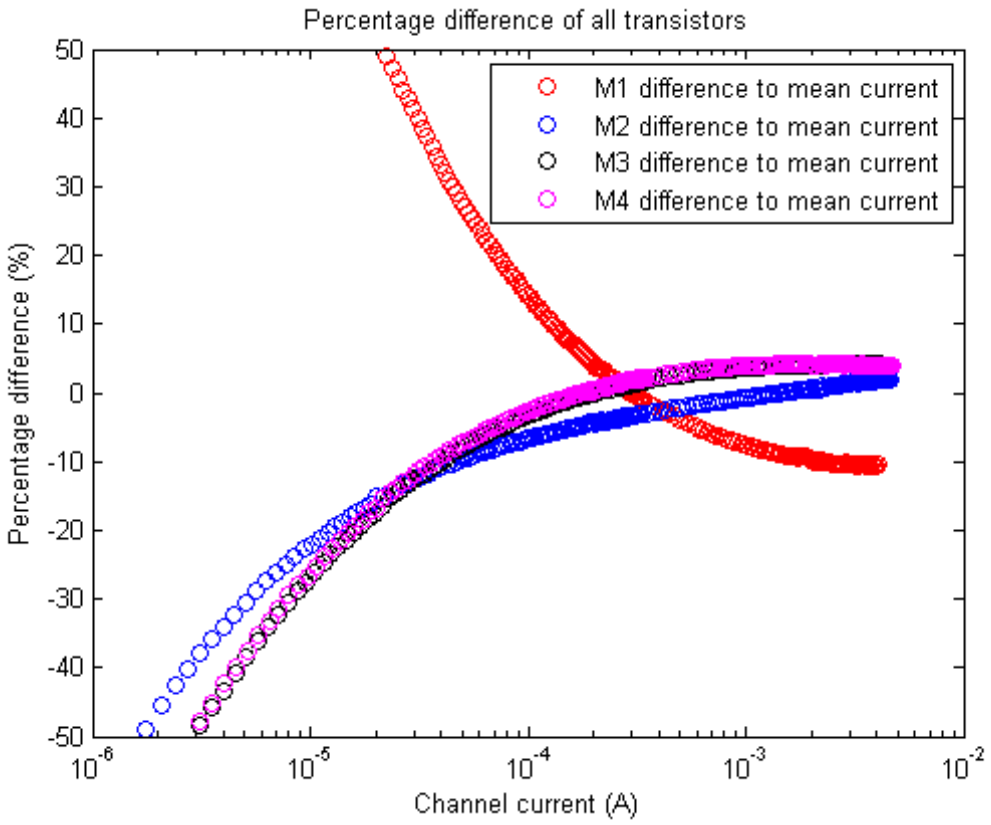

Figure 2: Semilog plot showing the percentage difference between each transistor's channel current and the mean value of all four channel currents as a function of the mean value of all four channel currents.

We have also shown the percentage difference of the other three transistors when they are not being compared to the one that did not match. The semilog plot below shows the percentage difference between the channel currents for transistors M2, M3, and M4, and the mean value of the three channel currents as a function of the mean value of all three channel currents.

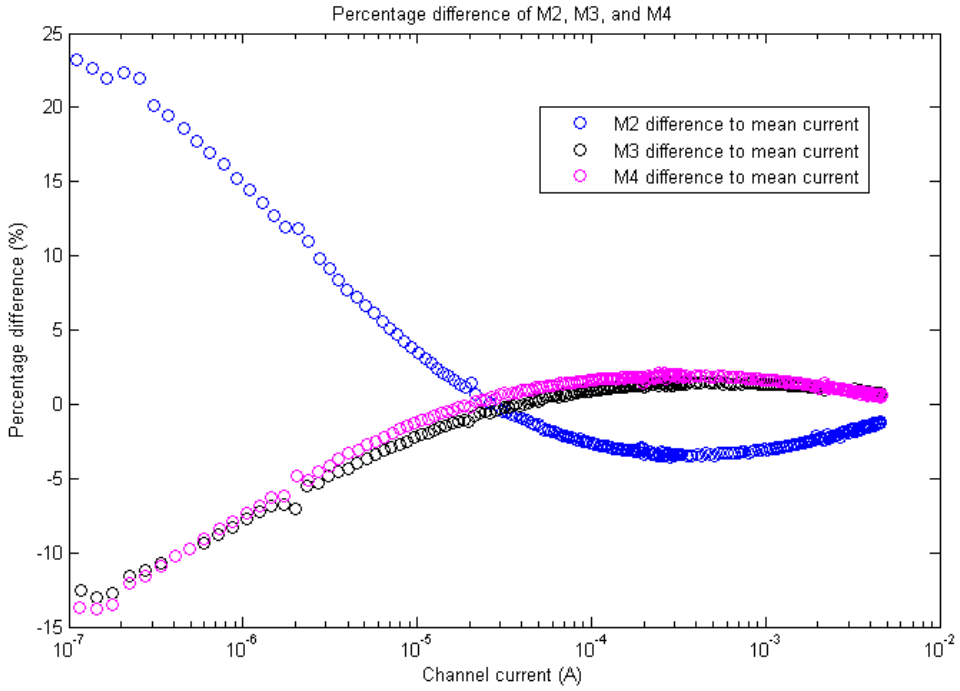

Figure 3: Semilog plot showing the percentage difference between M2, M3, and M4 transistors' channel current and the mean value of all three channel currents as a function of the mean value of all three channel currents.

We found the percent difference by taking:

$$I_{diff} = \frac{I_n - I_{avg}}{\frac{I_n + I_{avg}}{2}} * 100 \tag{5}$$

This equation was for each transistor, and with the plot that only includes M2, M3, M4, the average included only these three values.

Some transistors certainly matched better than others. The first transistor did not match well at all, especially compared to the others. The other three, however, generally seem to match each other well enough, with transistors M_3 and M_4 matching the best.

3 Experiment 2: MOS Transistors in Series and Parallel

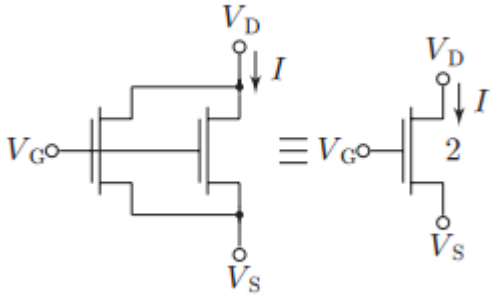

Figure 4: Two matched nMOS transistors connected with their channels connected in parallel. The parallel connection behaves just as if it were a single nMOS transistor whose current is twice as large as either of the individual devices. The same is true for pMOS devices.

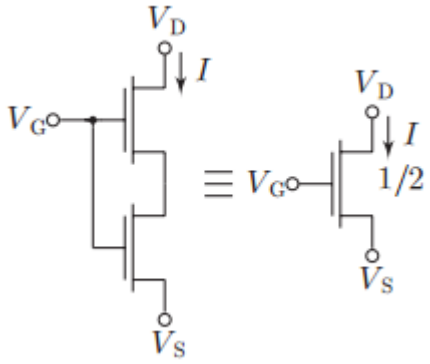

Figure 5: Two matched nMOS transistors connected with their channels connected in Series. The series connection behaves just as if it were a single nMOS transistor with half the current of either device. The same is true for pMOS transistors

For a single nMOS transistor, we measured channel current as a function of gate voltage both for VDS = 10 mV and for VDS = Vdd.

Next, we connected a matched pair of nMOS transistors in parallel with each other, as shown in Fig. 4, and repeated the measurements that we just did one of the devices by itself of this circuit.

Next, we connected the same pair of transistors in series with each other, as shown in Fig. 5, and repeated the same set of measurements.

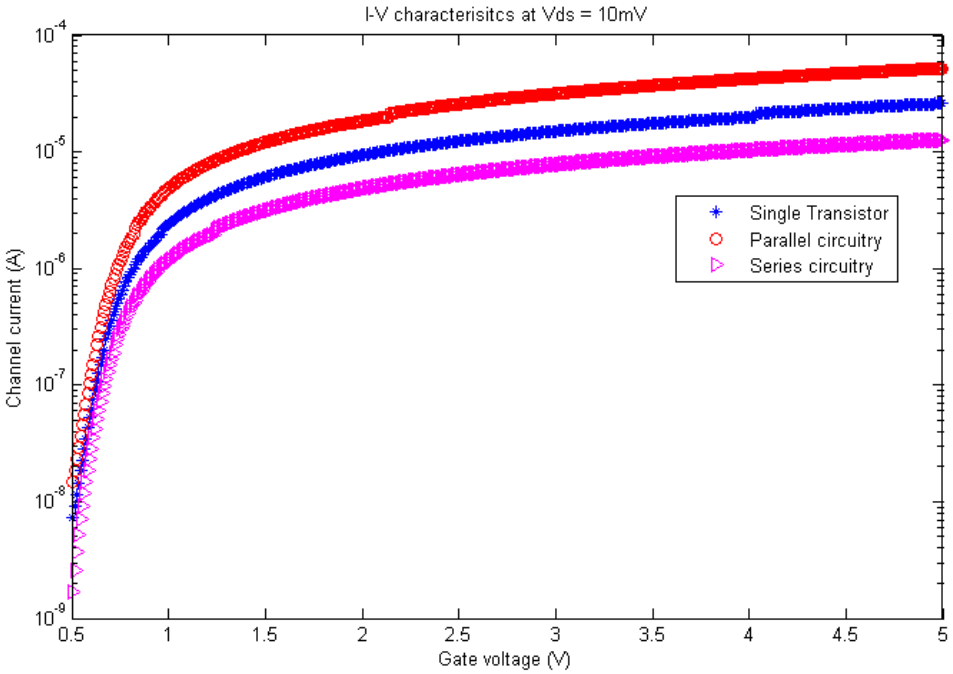

Figure 6: The current characteristics as a function of gate voltage for transistors in series, transistors in parallel and individual transistors when the drain voltage is set to 10 mV.

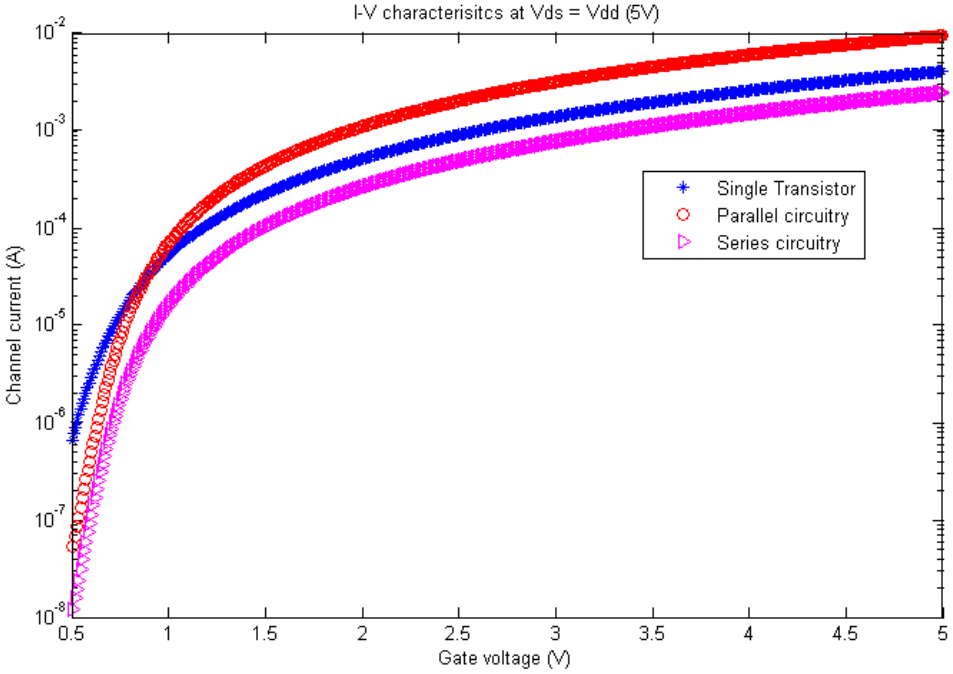

Figure 7: The current characteristics as a function of gate voltage for transistors in series, transistors in parallel and individual transistors when the drain voltage is set to 5V.

Figures 6 and 7 both show that the single transistor has twice the current of the series circuitry and half the current of parallel transistors.

To see how the channel currents of the series connected transistors and parallel connected transistors relate to the channel current of the single transistor, we have plotted the ratios below.

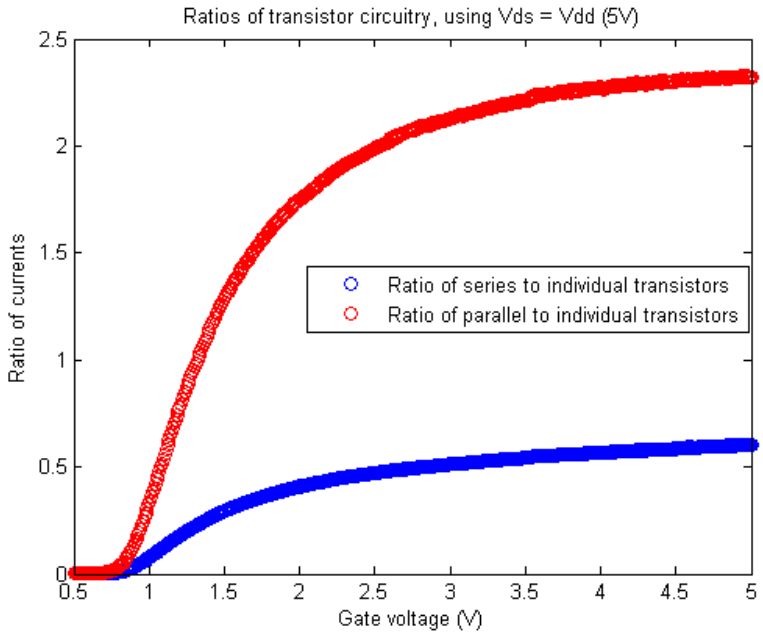

Figure 8: The ratio of the current of transistors in parallel to the current of an individual transistor (red) and the ratio of the current of transistors in series to the current of an individual transistor (blue), as a function of gate voltage when V_{ds} = Vdd.

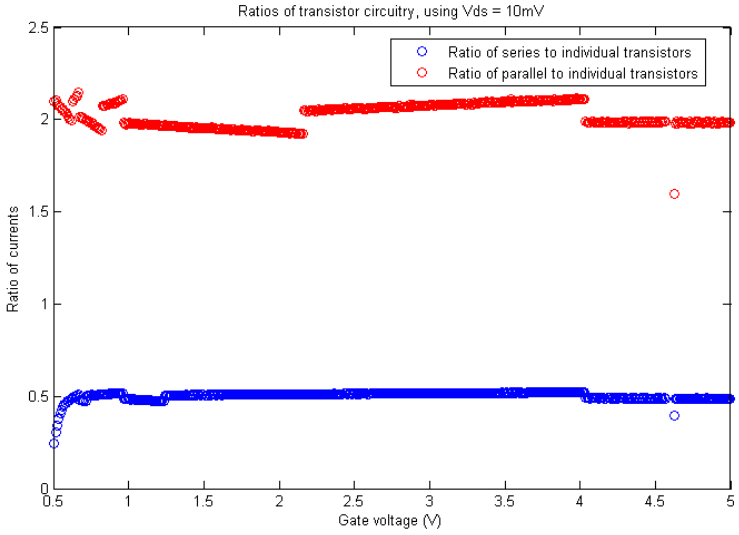

Figure 9: The ratio of the current of transistors in parallel to the current of an individual transistor (red) and the ratio of the current of transistors in series to the current of an individual transistor (blue), as a function of gate voltage when $V_{ds} = 10_{mV}$.

In general, the ratio for the series connected transistors is around 1/2, as expected, and the ratio for the parallel connected transistors is around 2, as expected.

We noticed that when V_{ds} was set to 10mV, the ratios seen were much noisier than when it was set to Vdd. Additionally, when V_{ds} was set to Vdd, we saw the current ratios increasing from 0 until they reached either 2 (for parallel) or 0.5 (for series), while when it was set to 10_{mV}, current ratios reached those points much quicker.

Overall, the series/parallel equivalences work decently well for MOS transistors. They do not work so well in the weak inversion, but they do in the strong inversion. We found the ratio of our parallel transistors to the single transistor leveled off at slightly higher than double when Vdd was set to 5V, but in each case they seem to reach close to the expected values of 0.5 and 2, especially once they reach the strong inversion.

4 Experiment 3: MOS Current Dividers

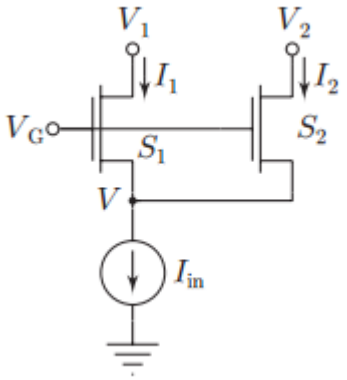

Figure 10: Two-way current dividers made from two nMOS transistors in which the input current is sunk from their sources and the output currents are taken at their drains.

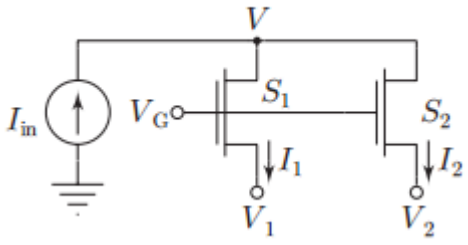

Figure 11: Two-way current dividers made from two nMOS transistors in which the input current is sourced into their drains and the output currents are taken at their sources.

We constructed the two-way current divider of Fig. 10 in which the divider ratio is a ratio of two small integers from the nMOS transistors in our ALD1106 array. We used one channel of the SMU to apply an input current to the divider, and we used the other channel of the SMU to measure

one of the output currents. We set the Gate Voltage to Vdd, 5V, and we set the drain voltage to Vdd so that drain voltage would be high enough to guarantee that the transistors were saturated.

We measured output current as a function of input current, and fit a straight line to the divider's current transfer characteristic. From here we were able to extract the value of the divider ratio. The plot below shows both the measured data and the theoretical fit with the extracted value of the divider ratio.

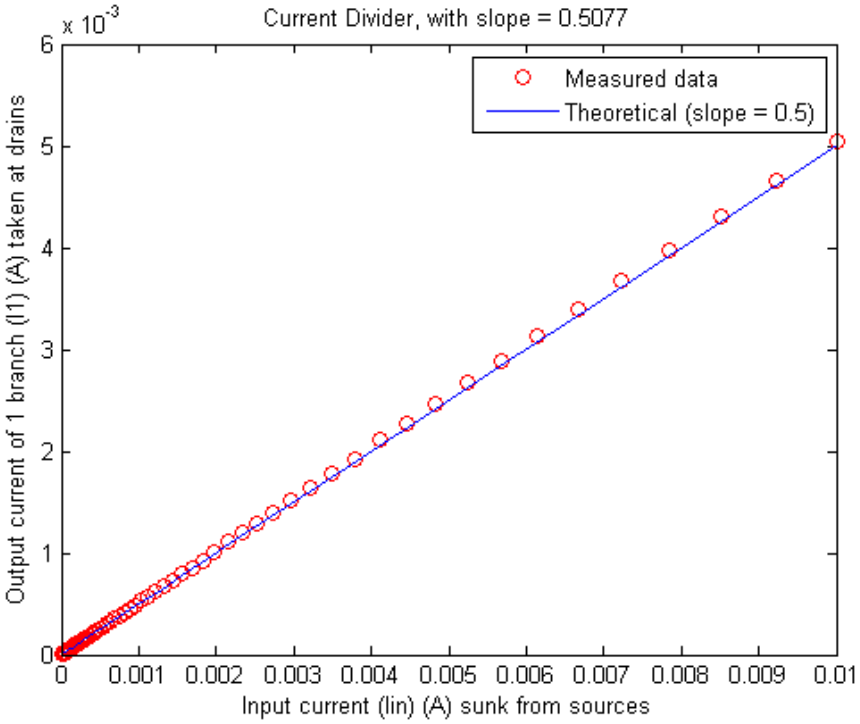

Figure 12: Current divider where current is sunk from sources and output currents are taken at drains. Current divider ratio = 0.5077

Next, we constructed the two-way current divider of Fig. 11 from the nMOS transistors in our ALD1106 array. With one channel of the SMU we applied an input current to the divider, and with the other channel we measured one of the output currents. We set the gate voltage to Vdd, 5V,and we set the source voltages to ground and the drain voltages to Vdd. Gate voltage was set sufficiently high that the transistors were able to accommodate the maximum input current that we used in our sweep.

We measured the output current as a function of input current, and once again we fit a straight line to the divider's current transfer characteristic. We extracted the value of the divider ratio as 0.5 for both circuits, figures 10 and 11 . The plot below shows both the measured data and the theoretical fits along with the extracted values of the divider ratio.

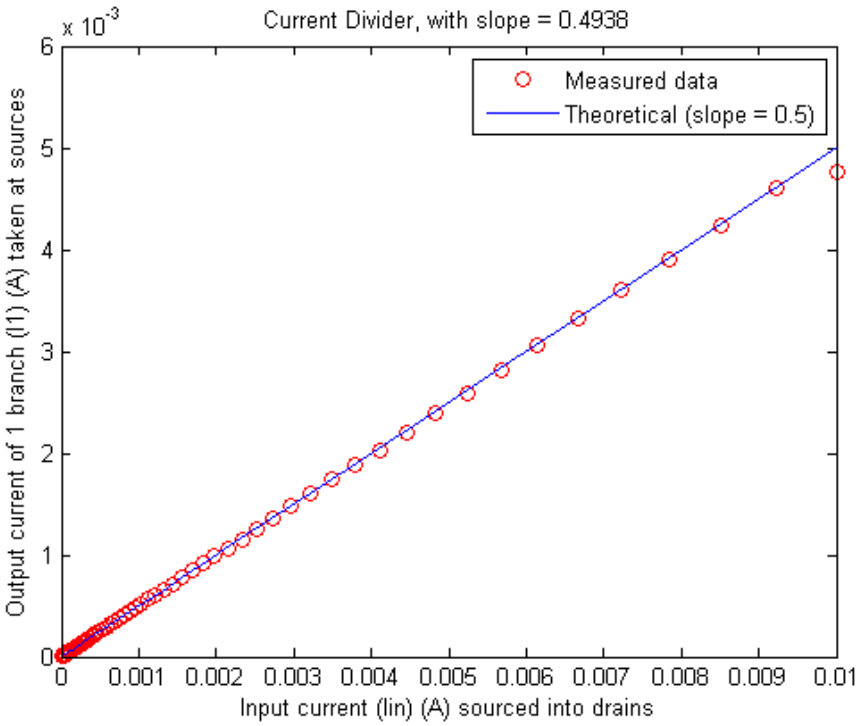

Figure 13: Current divider where current is sunk from drains and output currents are taken at sources. Current divider ratio = 0.4938

The divider ratios from each current divider, 0.5077 and 0.4938, are both very close to the expected theoretical value of 0.5.

5 Conclusion

In conclusion, we have seen in practice that twice transistors in parallel have twice the current output as one transistor, and transistors in series have half of the current output of one transistor. This knowledge is useful because it can be applied to the creation of current dividers.