Circuits Lab 05: MOS Transistor Characteristics

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1 Introduction

This lab consists of three experiments. First, we measured channel current as a function of gate voltage for both an nMOS and a pMOS transistor. In the second experiment we measured channel current as a function of source voltage, again for both an nMOS and a pMOS transistor. Finally, in the third experiment, we measured channel current as a function of drain voltage for both an nMOS and a pMOS transistor. The nMOS transistor used in these experiments is on an ALD1106 quad nMOS transistor array, and the pMOS transistor used in these experiments is on an ALD1107 quad pMOS transistor array. To establish proper bulk voltage for each chip, pin 4 of each tranistor array was connected to Vdd (5V) and pin 11 of each transistor array was connected to ground. In these experiments, measurements of the nMOS transistor were relative to ground, and measurements of the pMOS transistor were relative to Vdd, which was equal to +5V.

The gate, source and drain characteristics were in reference to the following symbols for N and P channel mosfets:

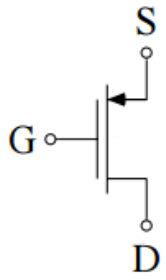

Figure 1: nMOS transistor schematic symbol

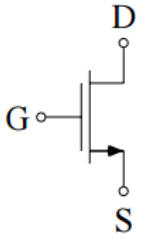

Figure 2: pMOS transistor schematic symbol

2 Experiments

2.1 Experiment 1: Gate Characteristics

For this experiment, we first measured channel current as a function of the gate voltage of an nMOS transistor from the ALD1106 nMOS transistor array, with the source voltage at ground at the drain voltage at 5V. The drain voltage was set to 5V so that it would be far enough above ground to guarantee that the transistor would remain in saturation.

Because current can be assumed to be in saturation, the theoretical fit for the nMOS transistor shown below follows the equations:

$$I = I_f A \tag{1}$$

$$I = I_{sat} = I_s \log(1 + e^{(\kappa(V_{gb} - V_t) - V_{sb})/Ut})^2 A \tag{2}$$

Where the values of κ, I_s, and V_t were found using the EKV fit shown below, and Ut is assumed equal 0.025V.

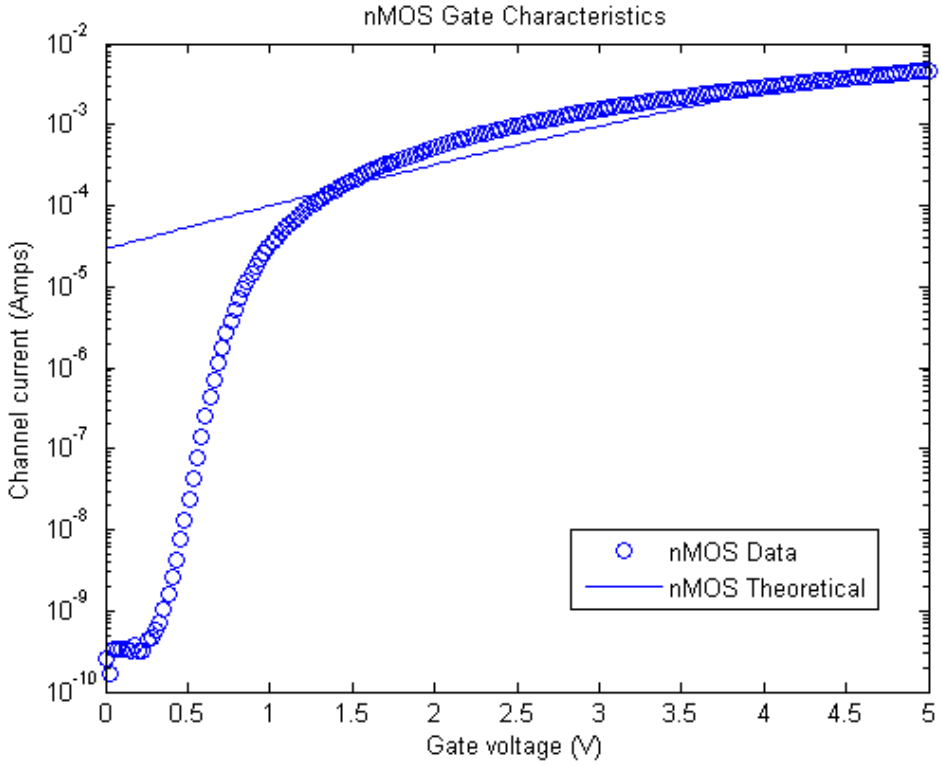

Figure 3: Channel current as a function of gate voltage for an nMOS transistor.

Next, we measured channel current as a function of gate voltage of a pMOS transistor from the AL1107 transistor array. Here, the source voltage was set to Vdd, which was 5V, and the drain voltage was set to ground, so that it would be far enough below Vdd to guarantee that the transistor would remain in saturation.

Because current can be assumed to be in saturation, the theoretical fit for the pMOS transistor shown below follows the equations:

$$I = I_f A \tag{3}$$

$$I = I_{sat} = I_s \log(1 + e^{(\kappa(V_{bg} - V_t) - V_{bs})/Ut})^2 A \tag{4}$$

Where the values of κ, I_s, and V_t were found using the EKV fit shown below, and Ut is assumed equal 0.025V.

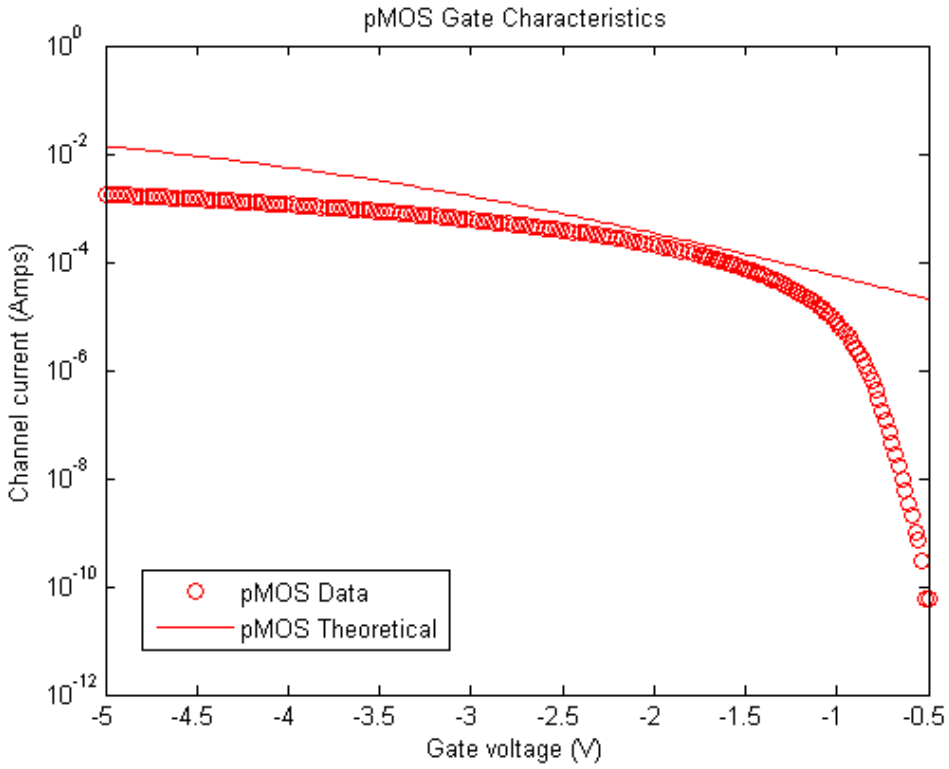

Figure 4: Channel current as a function of gate voltage for a pMOS transistor

The semilog plot below shows both the pMOS and nMOS transistor data together, along with their theoretical fits. Again, theoretical fits for both of the transistors shown below follow the equations:
nMOS:

$$I = (I_s \log(1 + e^{(\kappa(V_{gb} - V_t) - V_{sb})/Ut})^2) A \tag{5}$$

pMOS:

$$I = (I_s \log(1 + e^{(\kappa(V_{bg} - V_t) - V_{bs})/Ut})^2) A \tag{6}$$

Where for nMOS $V_{sb} = 0$V and $V_{db} = 5$V, while for pMOS, $V_{bs} = 5$V and $V_{bd} = 0$V. The values of κ, I_s, and V_t were found using the EKV fit shown below, and Ut is assumed equal 0.025V.

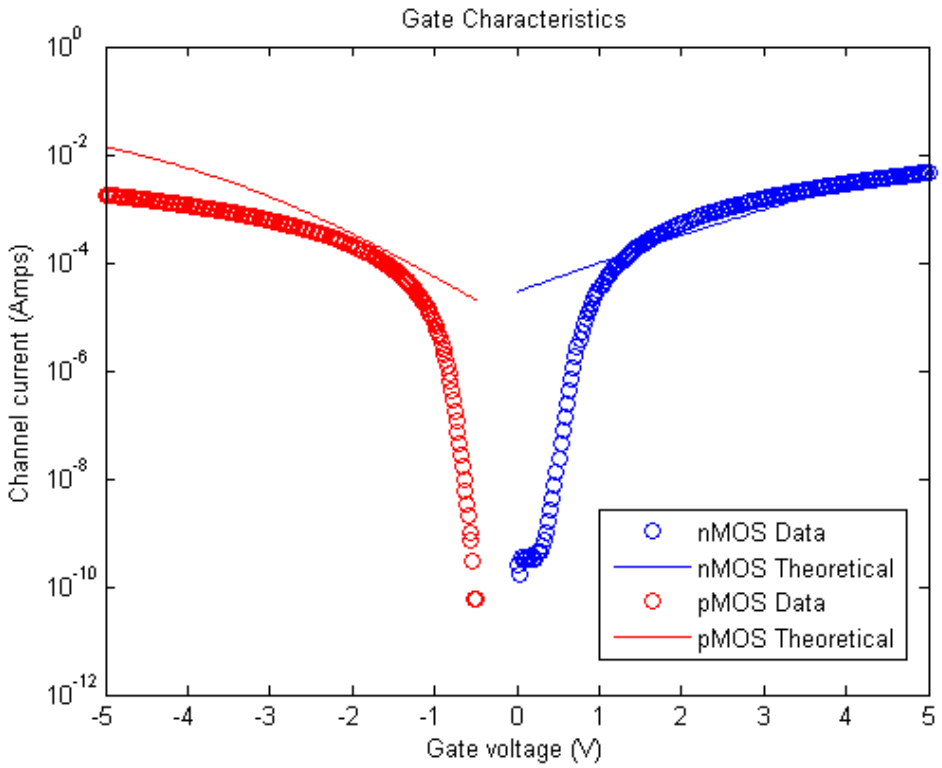

Figure 5: Channel current as a function of gate voltage for both an nMOS transistor and a pMOS transistor

If you take the absolute value of the gate voltage for the pMOS transistor and plot the gate characteristic, the nMOS and pMOS are nearly identical.

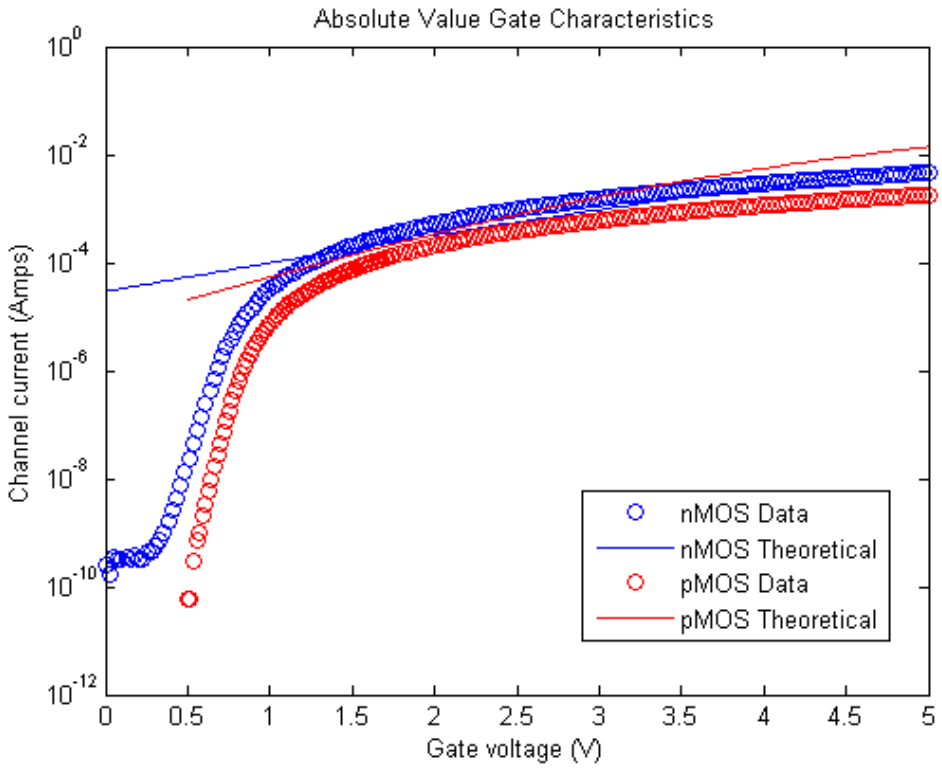

Figure 6: Taking the absolute value of the pMOS gate voltage makes the nMOS and pMOS data line up.

The gate characteristics were matched with an EKV fit through a provided matlab script.

The nMOS theoretical fit was found using the EKV model, listed below. It is assumed that the saturation current is approximately the channel current.

$$I_{sat} = I_s \log(1 + e^{\kappa(V_{gb} - V_t) - V_{sb}/2Ut})^2 A \tag{7}$$

$$\kappa = 0.6452 \tag{8}$$
$$I_s = 1.941e^{-6} A \tag{9}$$
$$V_t = 0.6748V \tag{10}$$

The pMOS theoretical fit was also found using the EKV model, listed below. It is assumed that the saturation current is approximately the channel current.

$$I_{sat} = I_s \log(1 + e^{\kappa(V_{bg} - V_t) - V_{bs}/2Ut})^2 A \tag{11}$$

$$\kappa = 1.03384 \tag{12}$$
$$I_s = 2.544e^{-7} A \tag{13}$$
$$V_t = 0.7335V \tag{14}$$

To analyze the gate characteristics, we looked at transconductance gain of both the nMOS and pMOS transistors.

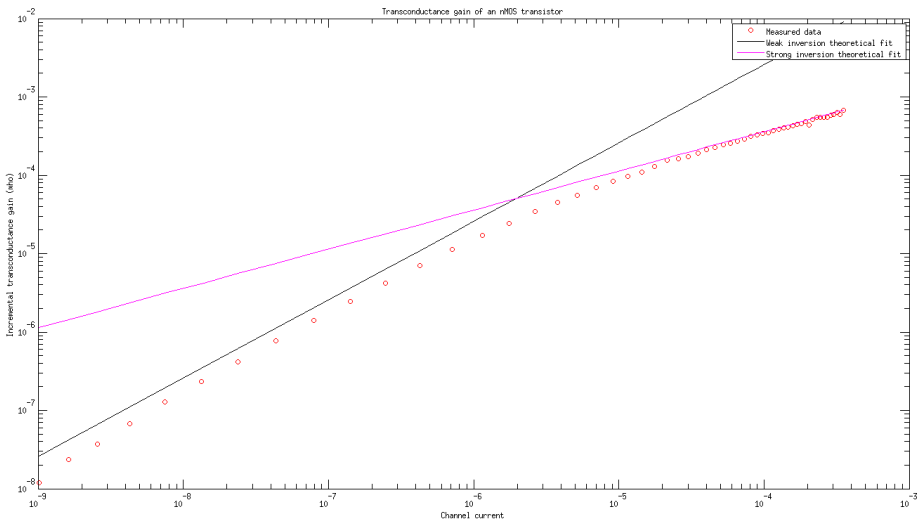

Figure 7: Transconductance of an nMOS transistor in saturation. The theoretical fit lines are described below.

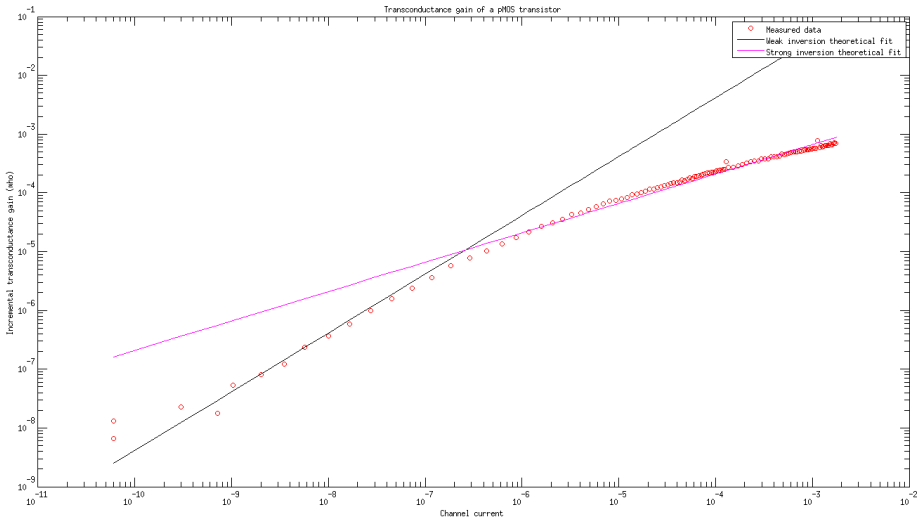

Figure 8: Transconductance of a pMOS transistor in saturation. The theoretical fit lines are described below.

The theoretical fit lines of the weak inversion region for both nMOS and pMOS were found using:

$$g_m = \kappa * \frac{I_{sat}}{U}\mho \tag{15}$$

The theoretical fit lines of the strong inversion regions were found using:

$$g_m = \kappa \frac{\sqrt{I_s I_{sat}}}{U_t} \upsilon \tag{16}$$

While the data taken from the previous graphs was used to calculate the transconductance gain using:

$$g_m = \frac{I_{sat}}{V_g} \tag{17}$$

Each have U_t being valued at 0.025V and use the κ and channel current found previously as the saturation current for each transistor.

In figures 7 and 8, the fit lines fit rather well. However, they fit better for the strong inversion for both transistors. We believe that this is due to the small magnitude of the weak inversion region. The strong inversion region, which also has more data points, fits incredibly well with both transistors, and acts as expected.

2.2 Experiment 2: Source Characteristics

For this experiment, we first measured channel current as a function of source voltage on an nMOS transistor with the gate and drain voltages both set at Vdd, 5V. Next, for the pMOS transistor, we measured channel current as a function of source voltage with the gate and drain voltage both set at ground.

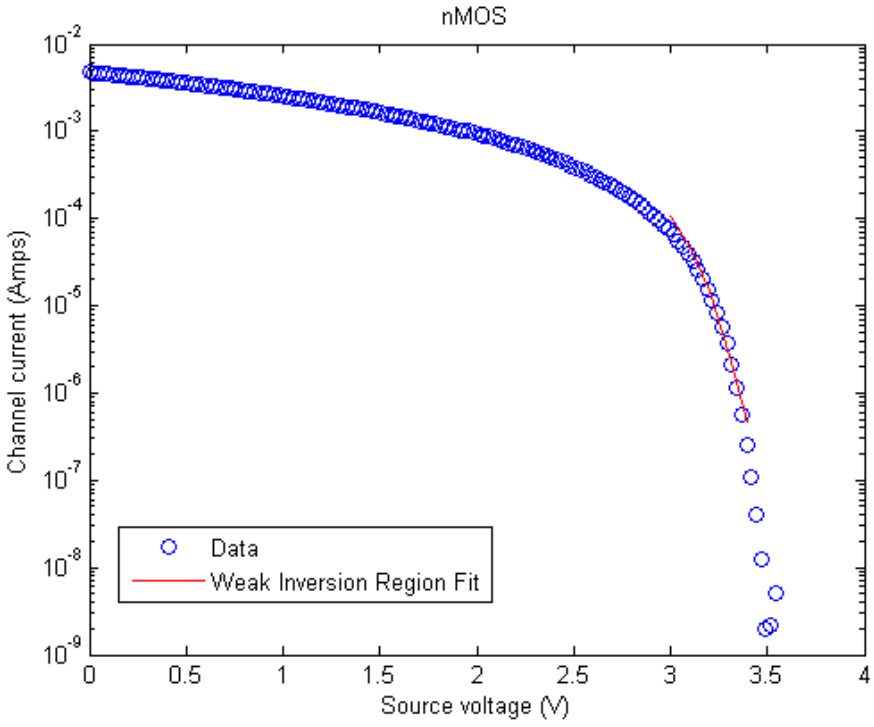

Figure 9: nMOS Source Characteristic. Exponential Slope of Weak Inversion $= -0.0848 * e^{-03}$ This was found using a linear fit of (Vs, log(I))

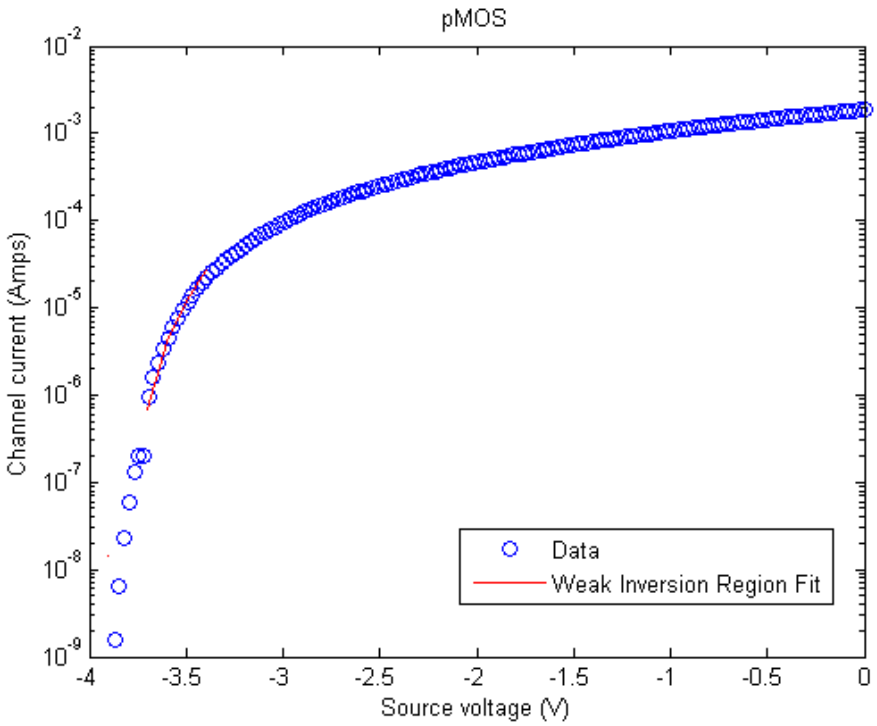

Figure 10: pMOS Source Characteristic. Exponential Slope of Weak Inversion $= 0.1479 * e^{-04}$. This was found using a linear fit of (Vs, log(I))

Note that the current drops off at around 3.5V at the source for both the nMOS and pMOS. For the nMOS, that is because the source voltage needs to be lower than the drain and gate, and there is a certain relationship between the threshold and source voltage, shown below.

$$\kappa * (V_g - V_t) - V_s = 0 \tag{18}$$
$$0.7 * (5 - 0.7) - V_s = 0 \tag{19}$$
$$Vs = \ 3.5 \tag{20}$$

With example values for gate voltage, threshold voltage and kappa for an nMOS transistor, we can see that the source voltage will be around 3.5 when reaching the threshold of activity. There is a similar version of this for pMOS, but with different references.

The incremental source conductance of both the nMOS and pMOS transistors was characterized in figures 11 and 12.

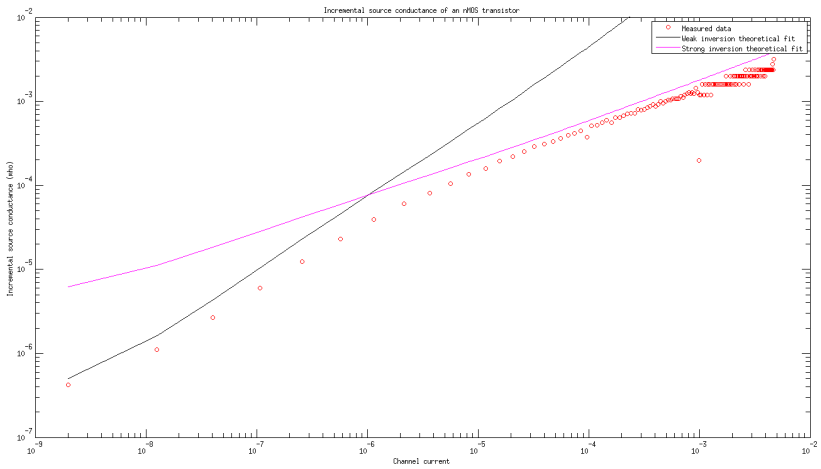

Figure 11: Incremental source conductance of an nMOS transistor

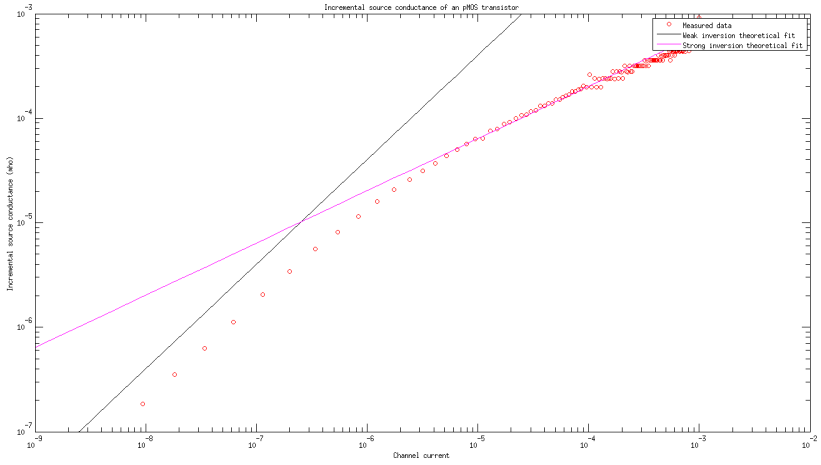

Figure 12: Incremental source conductance of a pMOS transistor

The theoretical fit lines of the weak inversion region for both nMOS and pMOS transistors were found using:

$$g_s = \frac{I_{sat}}{U}\mho \tag{21}$$

The theoretical fit lines of the strong inversion region for both nMOS and pMOS transistors were found using:

$$g_s = \frac{\sqrt{I_s I_{sat}}}{U_t}\mho \tag{22}$$

While the data taken from the previous graphs was used to calculate the transconductance gain using:

$$\frac{I_{sat}}{V_s} \tag{23}$$

Each have U_t being valued at 0.025V and use the channel current found previously (in Experiment 1) as the saturation current. Neither fit line for nMOS or pMOS in the weak inversion is perfect, and again we think it is because of the small magnitude of the weak inversion current, and the data is less than one magnitude off. The data points of the strong inversion are much more dense, and the fit line also fits better for the strong inversion for each transistor.

2.3 Experiment 3: Drain Characteristics

For this final experiment, on an nMOS transistor we measured channel current as a function of drain voltage for three values of gate voltage: below the threshold voltage (weak inversion), the threshold voltage (moderate inversion), and Vdd (strong inversion). The exact voltages used were 0.5V for weak inversion, 0.7V for moderate inversion, and 5V for strong inversion.The source voltage was set to ground for each of these sweeps.

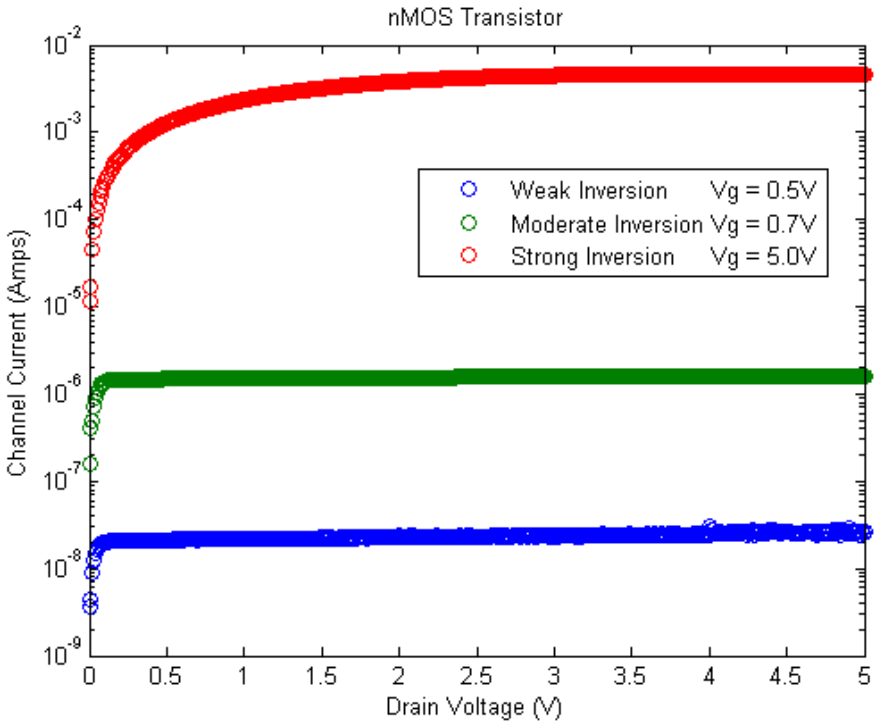

Figure 13: Channel current as a function of drain voltage for three different gate voltages for an nMOS transistor.

On a pMOS transistor, we measured channel current as a function of drain voltage for the same three values of gate voltage. For each of these sweeps the source voltage was set to 5V, Vdd.

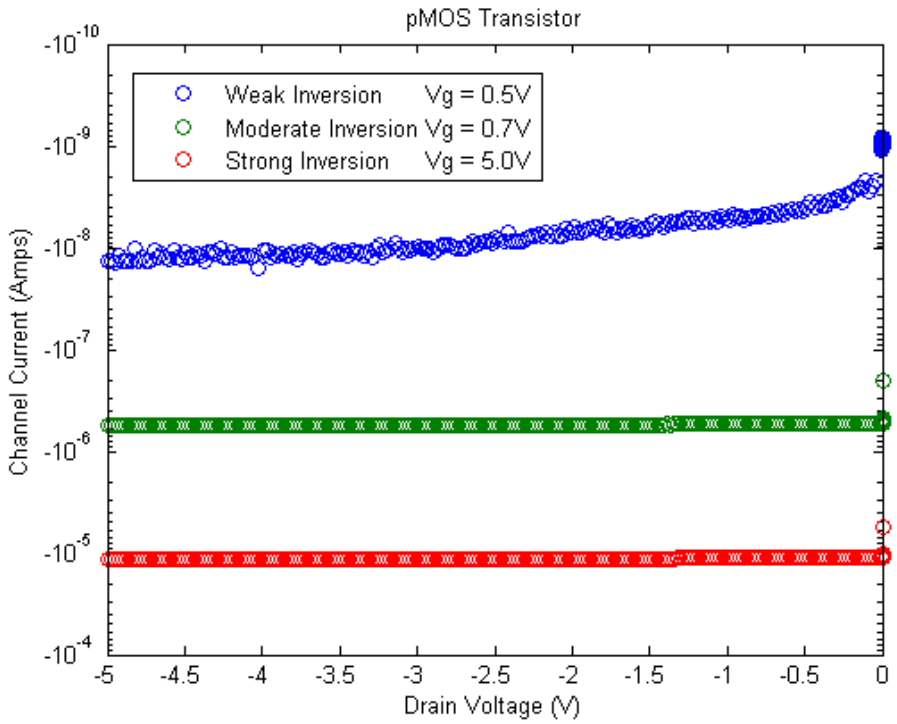

Figure 14: Channel current as a function of drain voltage for three different gate voltages for a pMOS transistor.

From here, the early voltages can be found by extrapolating the slopes of each drain characteristic, and finding the absolute value of the x intercept. Each value of I_{sat} is equal to the corresponding y-intercept of the same extrapolated lines. The graph below shows the early voltages (V_a) as a function of the saturation currents (I_{sat}).

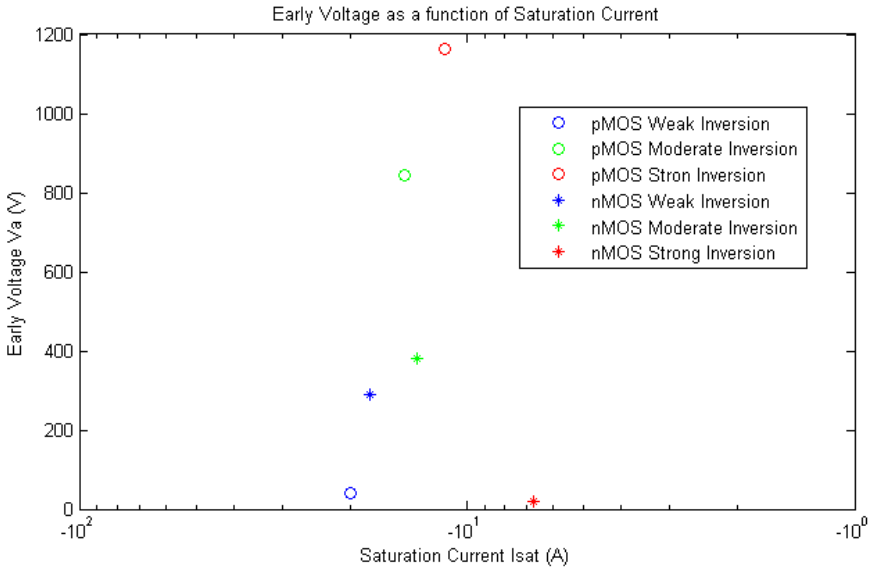

Figure 15: Semilog plot showing Early Voltage V_a (V) as a function of I_{sat} (A)

The inverse of the slope of the drain characteristic is equal to ro, and gs is equal to $\frac{I_{sat}}{Ut}$, so gsro is equal to $\frac{I_{sat}}{Ut}$ multiplied by the inverse of the drain characteristic slopes. Because in figure 14 the slopes of the pMOS moderate and strong inversions are so horizontal, the 1/slope (ro) found is extremely high. The nMOS data collected also had horizontal slopes in the weak and moderate inversions, their numbers are also higher than expected. The typical early voltages expected are around 15-150V. We are not sure why the drain characteristics of figures 16 and 14 are so flat in their slopes, but that is morphing our early voltage calculations.

A loglog plot of Intrinsic gain vs saturation current is shown below.

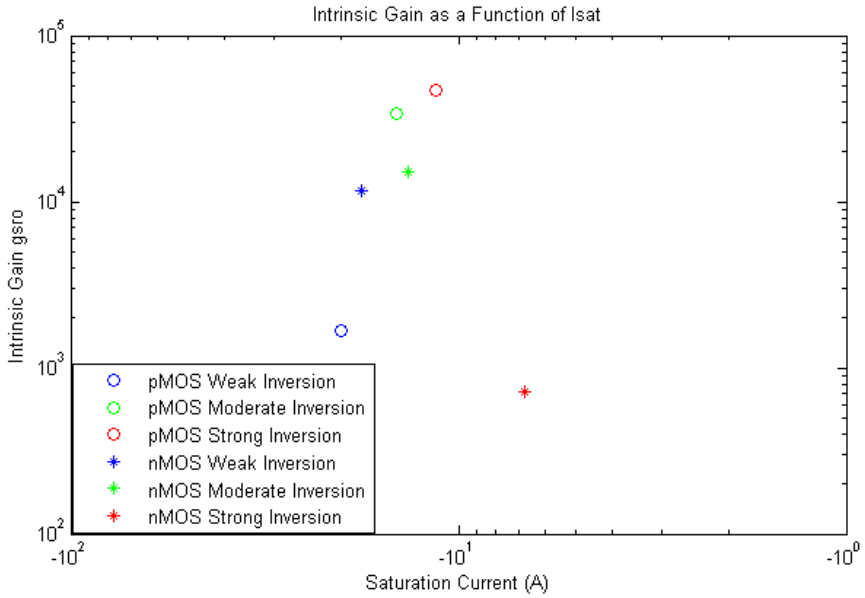

Figure 16: Loglog plot showing Intrinsic Gain gsro as a function of I_{sat} (A)

In many incremental analyses of CMOS circuits, it is useful to invoke several kinds of approximations that are based on the assumption that a transistor's intrinsic gain is much larger than unity. From our experimental measurements, we have found that this is generally a good assumption. The intrinsic gains we found were consistently significantly above unity, even with the reasonable values for early voltage. We also know that gmro is proportional to the intrinsic gains we extracted, because $gmro = gsro * \kappa$. The κ's found in experiment 1 for the transistors were around 0.5-1.