This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

An Overview of Nonvolatile Emerging Memories—Spintronics for Working Memories

Tetsuo Endoh, *Member, IEEE*, Hiroki Koike, *Member, IEEE*, Shoji Ikeda, Takahiro Hanyu, *Senior Member, IEEE*, and Hideo Ohno, *Member, IEEE*

***Abstract*—This paper reviews emerging nonvolatile random access memories (RAM) in recent years. It first benchmarks ferroelectric RAM (FeRAM), phase change RAM (PCRAM), resistive RAM (ReRAM), and spin-torque-transfer magnetic RAM (STT-MRAM), discussing each RAM's features and its applications. Then current status of spintronics developments including not only STT-MRAM but also nonvolatile logic LSI is described, which are particularly suitable for working memory applications.**

***Index Terms*—CMOS, ferroelectric RAM (FeRAM), memory, nonvolatile, phase change RAM (PCRAM), resistive RAM (ReRAM), spin-transfer-torque magnetic RAM (STT-MRAM).**

I. Introduction

IN INFORMATION and communication technology (ICT) equipment indispensable for modern society, semiconductor memory large scale integrated circuits (LSIs) occupy a main position in areas of silicon storage, working memories, and logic blocks. Semiconductor memories in ICT equipment normally constitute a pyramid-like structure as shown in Fig. 1 [1]–[3]. It consists of, from top to bottom, a processing core, cache memory by static random access memory (SRAM), main memory by dynamic random access memory (DRAM), and storage memory by solid-state disk (SSD), or hard disk drive (HDD). Located closer to the processing core, the faster the operating speed is required, whereas more distant from the core, larger density is required. In the processing core, even higher speed is required but with smaller capacity like flip-flops or registers. In recent years, in a large number of equipment, only semiconductor LSIs using NAND-flash storage instead of HDD are employed.

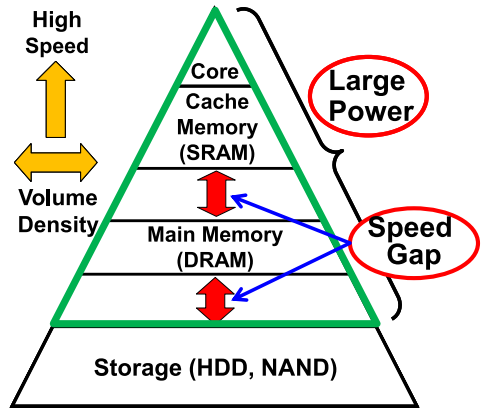


Fig. 1. Example of memory hierarchy in an ICT system. Speed gaps and large power are big issues for improving the system performance [1]–[3].

In the memory hierarchy in Fig. 1, cache memory and main memory are the working memories that are closer to the core. SRAM and DRAM have conventionally been adopted to the working memory. There are two key issues in such current semiconductor memory LSIs: 1) speed gap between different levels of the memory hierarchy and 2) rapid increase in the power consumption due to the increased density.

Issue 1 stems from the fact that DRAM is becoming a bottleneck of speed performance improvement. This is because DRAM must inevitably have several clocks of latency owing to its operating principle [4], [5], while the core processor and cache SRAM are able to operate with the frequency of 3 GHz or more, using the state-of-the-art process technology [6]–[9]. Also, there are essential speed gap between main memory and storage due again to the operating principle of NAND flash; it takes μs $\sim$ ms for write/erase [10], [11].

Regarding issue 2, the major factor is that the stand-by power to retain the information can no longer be ignored compared to the operating power to perform information processing, because of the characteristic of miniaturized transistors [12]. As for DRAM, in particular, the number of memory cells which must be refreshed simultaneously has reached the maximum limit from the viewpoint of the refresh current. This fact not only causes large power dissipation but has also become the obstruction of miniaturization.

In order for ICT technology to keep contributing to the world society under the situation, where the more energy-saving

Manuscript received July 07, 2015; revised August 28, 2015; accepted September 29, 2015, and October 16, 2015. This work was supported in part by CIES's Industrial Affiliation on STT -MRAM Program , R&D Subsidiary Program for promotion of Academia -Industrial Cooperation of METI , R&D Project for ICT Key Technology of MEXT , ImPACT Program of CSTI , and ACCEL Program under JST . This work was recommended by Guest Editor S. Ghosh.

T. Endoh is with the Graduate School of Engineering, the Center for Spintronics Integrated Systems, and the Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai 980-0845, Japan (e-mail: tetsuo.endoh@cies.tohoku.ac.jp).

H. Koike is with the Center for Spintronics Integrated Systems, Tohoku University, Sendai 980-8577, Japan (e-mail: h-koike@cies.tohoku.ac.jp).

S. Ikeda is with the Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai 980-0845, Japan (e-mail: sikeda@riec.tohoku.ac.jp).

T. Hanyu and H. Ohno are with the Research Institute of Electrical Communication, the Center for Spintronics Integrated Systems, and the Center for Innovative Integrated Electronic Systems, Tohoku University, Sendai 980-8577, Japan (e-mail: hanyu@riec.tohoku.ac.jp; ohno@riec.tohoku.ac.jp).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JETCAS.2016.2547704

2156-3357 © 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

TABLE I
BENCHMARK OF EMERGING NONVOLATILE MEMORIES

Performance index	FeRAM	PCRAM	ReRAM	STT-MRAM	NAND flash	SRAM
Cell size (SLC*)	15 ~ 35F^2	4 ~ 19F^2	6 ~ 10F^2	6 ~ 14F^2	4F^2	160 ~ 280F^2
Operation voltage	~ 1.8 V	1.5 ~ 1.8 V	3.3 ~ 6.5 V	0.8 ~ 1.8 V	~ 20 V	0.6 ~ 1.1 V
Write current	~ 10^{-6} A**	~ 10^{-4} A	~ 10^{-4} A	~ 10^{-5} A	~ 10^{-7} A	~ 10^{-5} A
Write time	< 10 ns	~ 100 ns	~ 50 ns	< 10 ns	~ 1 ms	≤ 2 ns
Read time	< 5 ns	< 5 ns	< 5 ns	< 5 ns	~ 100 µs	≤ 2 ns
Retention	> 10 yrs	> 10 yrs	> 10 yrs	> 10 yrs	> 10 yrs	(volatile)
Endurance	10^{13}	10^9 ~ 10^{12}	~ 10^6	10^{15}	~ 10^5	10^{15}

* SLC: Single-level cell. (In this table, only physical cell size is written. Multi-level cell and multi-layer cell is out of consideration.)
** Capacitive switching (no static current required).

is strongly required, it is essential to develop and commercialize LSIs which achieve both reduction of power dissipation and enhancement of speed performance. Currently many research institutions and manufacturers have actively been involved in research and development (R&D) for "emerging nonvolatile memory". These R&D activities are based on the idea that emerging nonvolatile memory using new materials can be a promising candidate technology to break through the above speed gap and power consumption problems for conventional SRAM and DRAM. As examples of emerging nonvolatile memory, there are ferroelectric RAM (FeRAM), phase change RAM (PCRAM), resistive RAM (ReRAM), and spin-transfer-torque magnetic RAM (STT-MRAM).

In the following, we first benchmark emerging nonvolatile memories, and discuss what application would be most suitable for each type of emerging memory. Second, we particularly focus on STT-MRAM, which we consider the most optimal device for working memory in computer systems. Recent development results about STT-MRAM are summarized based on our recent effort in this direction.

II. BENCHMARK FOR EMERGING NONVOLATILE RAMS

Development of emerging nonvolatile memories with silicon CMOS technology started from early or mid 1980s. They use special materials having a bi-stable state in their electronic characteristics without power supply. The examples are FeRAMs [13]–[17], PCRAMs [18]–[23], ReRAMs [24]–[32], and STT-MRAMs [33]–[40]. The performance benchmark for each emerging memory is summarized in Table I. For reference purpose, NAND flash [76]–[79] and SRAM [80]–[83] are added to Table I. These will help us compare current status of each emerging memory and the existing working/storage memory.

Emerging nonvolatile memories generally have the structure like Fig. 2, in which the case of magnetic-tunnel-junction (MTJ)-based STT-MRAM is shown as an example. In Fig. 2, nonvolatile devices (MTJs) are fabricated directly on the CMOS circuit. Because of the close connection between the logic circuit and the memory compared to the conventional logic circuit with SRAM, the MTJ-based nonvolatile logic

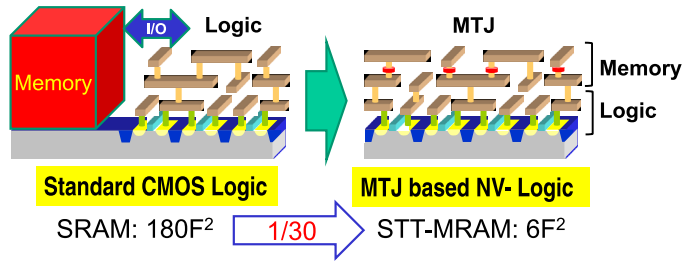


Fig. 2. Advantage of emerging nonvolatile memory, compared to a conventional standard CMOS logic with SRAM.

achieves not only drastic area and I/O power reduction but also improvement of data transfer speed.

The idea of FeRAM cell was first reported in 1987 [13], subsequently in the next year a 256-bit FeRAM was reported [14]. This early emerging nonvolatile memory used ferroelectric capacitors as a nonvolatile device combined with a CMOS circuit. However, FeRAM has a difficulty in scaling of its memory cell size: because it is not straightforward to process the ferroelectric materials, e.g., lead-zirconate-titanate (PZT), and the electrode materials, which are usually noble metals, e.g., platinum (Pt), iridium (Ir), without having reaction between the two. As a result of this, at the present moment, the most suitable applications for FeRAM are somewhat limited, to smart IC cards and small scale microcontrollers with a small storage capacity.

PCRAM is a nonvolatile memory using the chalcogenide material, which is widely used in storage media such as CD-ROM and DVD. The advantage of this device is its small storage element size. Due to this feature, PCRAM is suitable for the application area of program storage, where NOR flash memory has been traditionally used. And if further integration is achieved, storage class memory will also be covered as its application target. However, it has a significant difficulty in operation stability or reliability by temperature cross-talk between adjacent memory cells as the technology scales down, because it uses phase transition phenomenon by applying Joule heat as the nonvolatile operation principle. If the endurance of 10^{15} order were achieved, it could replace DRAM. However, it remains to be seen how it overcomes the technology issue of chalcogenide material property.

ReRAM is relatively a new face among the emerging nonvolatile memories. It was first reported around early 2000s. Since the recent researches have revealed that the redox reaction (oxidation-reduction reaction) of metals plays a major role in ReRAM, it is nowadays often referred to as the abbreviation of "Redox RAM", instead of conventional "Resistive RAM". There are several types of storage principle for ReRAM, which can be categorized into two types. One is conductive bridge RAM (CBRAM), and the other is oxide RAM (OxRAM). Both CBRAM and OxRAM use redox reaction in their operational principle [32], [75]. The principal advantage of the ReRAM is its simple device structure. In particular, if the device formation into the via hole and/or the multi-layer [29], [30] is achieved, it may be able to cover the storage application area where NAND flash currently occupies. It is also important to develop multi-level memory cell [28] utilizing the high on/off ratio of a redox material.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

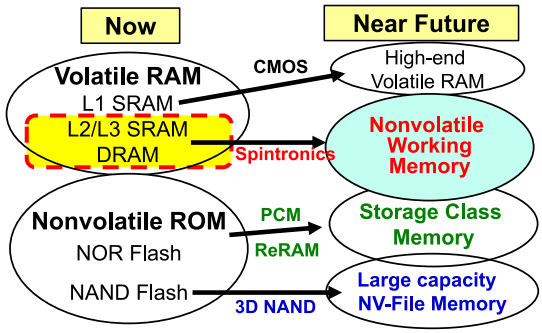


Fig. 3. Segmentation of each kind of emerging nonvolatile memories (conventional SRAM, Spintronics, PCRAM, ReRAM, and 3D NAND). Spintronics includes not only STT-MRAM but also nonvolatile logic using spintronics device.

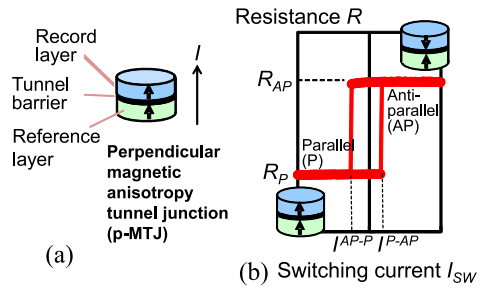


Fig. 4. Schematic views of MTJ device. (a) Structure of p-MTJ. (b) Resistance versus switching current characteristics.

MRAM initially adopted the data write scheme that used current-induced magnetic fields [67], [68]. However, the scheme had a serious problem in that write current increases inversely-proportional to the device feature size [40] and hence it has an early limit in scaling. By employing spin-transfer-torque operation principle [69], [70], which utilizes spin-torque transfer of spin-polarized current that induces magnetization switching, MRAM (STT-MRAM) overcame the scaling difficulty of the first generation MRAM. Remaining challenges to further scaling of STT-MRAM will be reducing switching current, stable data retention, obtaining low resistance and wider operational margin (increasing *MR ratio*). Since there are tradeoffs among these issues, clever arbitration will also be required. STT-MRAM will then become the most promising candidate of nonvolatile working memory owing to the MTJ's native virtues of low-voltage, high-speed, and practically infinite endurance.

Fig. 3 illustrates the segmentation of the above emerging nonvolatile memories for individual applications in the near future. Conventional SRAM may remain in the level-1 cache which is very close to MPU. STT-MRAM will be able to occupy the position of the level-2 cache and lower hierarchy level high-density working memory. In storage class memory, PCRAM and/or ReRAM, especially high-density memory with multi-layer or multi-level techniques is promising. For the application areas that require extremely large capacity, 3D-NAND will still be most appropriate.

III. Spintronics: Material and Device Technology

This chapter through the next chapter reviews our recent development results for spintronics technology in detail. This chapter describes mainly material and device technology including the basics of MTJ device, and the next chapter concerns circuit and system technology.

A. Basics of MTJ Device

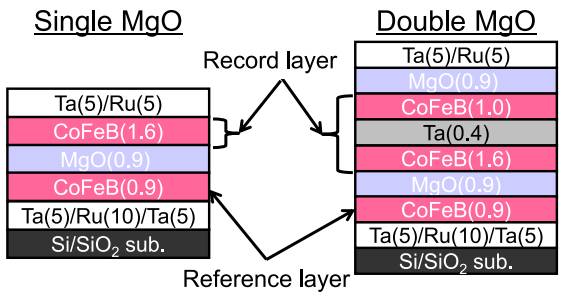
Fig. 4 illustrates schematic views of MTJ structure (a) and electronic characteristics (b) [41]. Here we take up perpendicular anisotropy MTJ (p-MTJ) as a typical example of MTJ devices. As shown in Fig. 4(a), MTJ has a structure with a thin tunnel barrier film composed of several atomic layers, sandwiched by two ferromagnetic layers. The upper ferromagnetic layer in Fig. 4(a) is the recording layer, in which the magnetization direction can be flipped upward or downward. On the other hand, the lower layer is the reference layer, in which the magnetization direction is fixed [upward in Fig. 4(a)]. The resistance across the MTJ device has a different value according to whether the magnetization direction for the recording layer is parallel to that for the reference layer or not. We define R_P as the resistance for the parallel (P) state, and R_{AP} for the anti-parallel (AP) state. R_{AP} is normally larger than R_P. This phenomenon is so-called tunnel-magneto-resistance (TMR) effect [42].

The MTJ resistance can be changed by flipping the magnetization direction of the recording layer. Spin-transfer-torque switching by spin-polarized current is usually chosen for the way to invert the magnetization direction. The spin-transfer-torque is a phenomenon that spin-torque, generated by exchanging the angular momentum between spin-polarized conduction electrons and the magnetization of the recording layer, makes the magnetization flipped. Using the spin-transfer-torque, the MTJ resistance state can be changed by applying the switching current (I_{SW}) to the MTJ, as shown in Fig. 4(b). There is the threshold current where the MTJ resistance is changed (shown as I^{AP-P}, I^{P-AP} in the figure).

The magnitude of the TMR effect can be usually measured by the *MR ratio*, which is defined as $(R_{AP} - R_P)/R_P$. The larger the *MR ratio* is, the larger the difference between R_P and R_{AP}. Hence for an MTJ with a large *MR ratio*, it is easy for the sensing circuit to distinguish which resistance state the MTJ is in. This is an advantage of the STT-MRAM operation. The *MR ratio* is often used as an index indicating the operational margin of STT-MRAM. In the past, typical *MR ratio* was less than several percent, but after the magnesium oxide (MgO)–CoFe(B) system was discovered, large *MR ratio* of more than 100% was able to be obtained [43]–[47].

There is another important index, thermal-stability factor Δ, which indicates the stability of data retention. Δ is defined as E/k_BT, where E is the energy barrier between P-state and AP-state, k_B is Boltzmann constant, and T is the junction temperature in Kelvin. The larger the Δ, the MTJ is more tolerant against the thermal disturbance, i.e., the MTJ's data retention is more stable. For example, reference [48] reported that the Δ of more than 67 was required for guaranteeing the nonvolatility of 32 Mbit STT-MRAM.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.



Note: Numerals in () stand for film thickness [nm]

(70 nmϕ)	Single	Double
Δ (E/k_BT)	51	95
I_{C0} (μA)	125	123

Fig. 5. Improvement of thermal stability factor Δ by applying double MgO structure. Δ was improved without increasing the switching current I_{C0} [51].

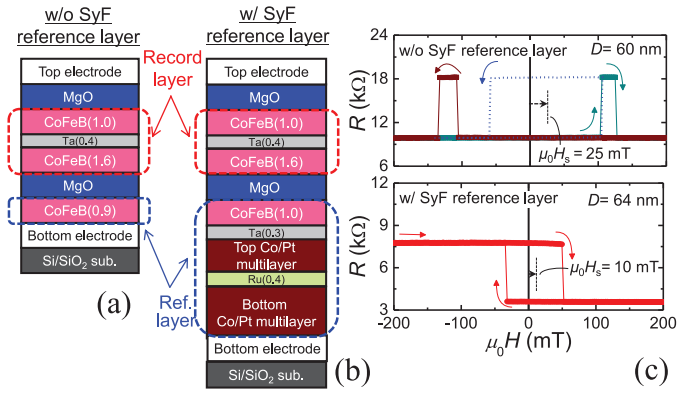


Fig. 6. Development of synthetic ferrimagnetic (SyF) reference structure which consists of a top [Co/Pt]/Ta/CoFeB multilayer and a bottom Co/Pt multilayer antiparallel-coupled by a Ru layer. The shift (H_s) of resistance versus magnetic field was reduced by applying SyF reference structure [52]–[54].

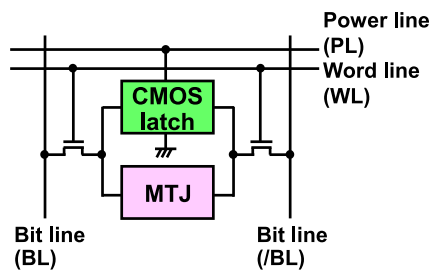


Fig. 7. Conceptual diagram of differential type STT-MRAM cell.

B. Recent Development of MTJ

After the first demonstration of the interfacial perpendicular anisotropy between the ferromagnetic electrodes (CoFeB) and the tunnel barrier (MgO) of MTJ [49], we have continued to pursue more miniaturization, higher performance, and higher reliability for p-MTJ.

Further improvement of thermal-stability factor Δ is strongly required for achieving Mbit class high density memory LSI. To tackle this issue, we focused on the fact that Δ is proportional to the thickness of the CoFeB recording layer [50]. Based on this fact, it was found that forming the double MgO structure, in which the CoFeB/Ta/CoFeB recording layer is sandwiched by two tunnel barrier MgO films, can increase the recording layer thickness by almost a factor of two [51]. The experimental result is summarized in Fig. 5, together with the result for the conventional single MgO structure as a reference. The MTJ size was 70 nmϕ. As expected, Δ for the double MgO structure was 1.9 times larger than that for a single MgO. Moreover it was achieved without increasing the switching current I_{C0}.

The fringing magnetic field from the reference layer causes the asymmetry of Δ for P-state and AP-state, resulting in degradation of total thermal stability of MTJ. To solve this problem, we developed a synthetic ferrimagnetic (SyF) reference layer [52]–[54]. Fig. 6 summarizes the experimental result, together with the result of the reference sample. By applying an SyF structure to the Co/Pt multilayer based reference layer, the shift of the resistance-magnetic field curve was suppressed, thus the higher thermal stability of antiparallel magnetization configuration was obtained compared to that without a SyF structure. Moreover, the *MR ratio* of 120% at 8 Ωμm^2 in the 10-nm-diameter p-MTJ with this stack structure using 300 mm Si wafer sputtering system showed almost no degradation after annealing at 400 °C [55], [56], indicating its high-temperature tolerance. The developed MTJ has a good affinity, with a capability to withstand the thermal budget of typical back-end-of-line (BEOL) process.

IV. Spintronics: Application to LSIs

In this chapter, recent development results of spintronics LSIs are reviewed. First we discuss STT-MRAM including the fast differential type and the high-density 1T1MTJ type, and then move on to spintronics logic LSIs.

A. High-Speed Differential Type STT-MRAM

In order to reduce the operating power of computer systems, it is effective to make working memory nonvolatile, and to cut off the power of memory area in stand-by. From the viewpoint of operation factors such as speed, write endurance, and low-voltage operability, STT-MRAM is at present the most probable candidate for nonvolatile working memory. By using a differential type memory cell, which combines a CMOS latch and MTJ devices as shown in Fig. 7, high-speed STT-MRAM comparable to SRAM was demonstrated [57].

However, the switching speed of MTJ is not fast enough to be applied to cache memory requiring several hundred MHz frequency or more. Since MTJ switching is related to write operation, write speed limits the STT-MRAM operation speed.

To solve this problem, a novel circuit technique, the background write scheme, has been developed [57]. This technique achieves high-speed write operation by "hiding" the MTJ switching time from the STT-MRAM operation. Fig. 8 shows the concept of this scheme and the diagram of 6 transistor(T)-2MTJ type STT-MRAM cell to realize this background write scheme. In this scheme, each STT-MRAM cell is configured with a normal 6T SRAM cell and a couple of MTJs. High speed write is carried out by the CMOS latch in the SRAM operation frequency, and nonvolatile write from the CMOS latch to the MTJ pair (called "backup to MTJ") is subsequently performed apart from the SRAM frequency. For the backup to MTJ operation, 6T-2MTJ type STT-MRAM cell

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

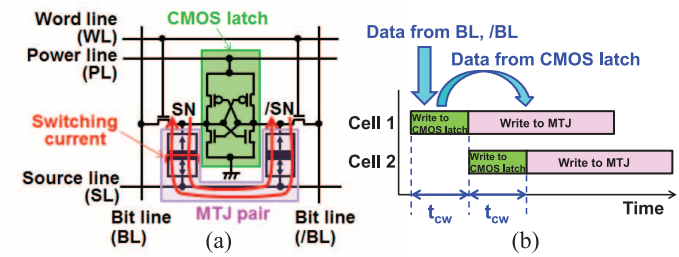
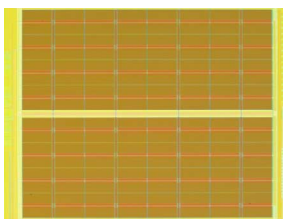


Fig. 8. 6T-2MTJ differential STT-MRAM with background write scheme [57].



Process	90nm CMOS + 100nm MTJ
Cell Size	1.13×3.06=3.46μm^2
Macro Size/Mb	5.14mm^2
Cell Efficiency	70.5%
Supply Voltage	1.3V
Organization	64k word x 16bit
Grain Size	64bit
Functioin	Asynchronous SRAM
Random Read Cycle	1.5ns
Random Write Cycle	2.1ns

(a) (b)

Fig. 9. 1 Mbit 6T-2MTJ STT-MRAM prototype with background write scheme. (a) Chip photo. (b) Chip features [57].

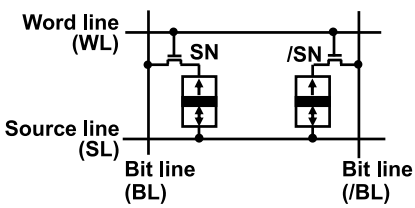
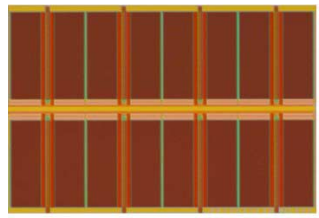


Fig. 10. 2T-2MTJ (Twin 1T-1MTJ) memory cell.

is the most suitable, because the write to MTJ can be done only by setting the source line (SL) to floating. The internal nodes of CMOS latch (SN, /SN) have a voltage difference. When the SL is set to floating, the voltage difference between SN and /SN makes current flow to the MTJ pair, by which the MTJ switching is automatically performed as shown in Fig. 8(a). This operation is apart from the CMOS latch operation, so it maintains the SRAM speed and also achieves nonvolatile write. 1 Mbit STT-MRAM prototype with this scheme was designed and fabricated using 90 nm standard CMOS and an additional 100 nm MTJ process technology. Fig. 9 summarizes the result. Read/write of 1.5 ns/2.1 ns has been realized, which is sufficient for cache memory application. Note that the write speed to MTJs are relaxed to the time sufficient to be switched ($\sim$ 7 ns [57]), by using the developed "background write scheme" previously explained in Fig. 8.

The smallest cell for the differential type STT-MRAM cell is 2T-2MTJ (or "twin 1T-1MTJ" in a sense of a combination of two 1T-1MTJ cells). The 2T-2MTJ cell is illustrated in Fig. 10 [58]. This cell has a simple structure, which consists of only selecting transistors and MTJs, removing a CMOS latch, compared to the fundamental differential type STT-MRAM cell in Fig. 7. This results in the minimum cell area among differential type memory cells. When this memory cell is applied to STT-MRAM, however, the degradation of operating speed may be concerned due to removing the CMOS latch, which provides high-speed operability equivalent to SRAM. According to an



	1Mb twin 1T1MTJ STT-MRAM
Process	90nm CMOS (Lg=100nm) + MTJ
Cell size	0.88μm^2
Macro size	1.40mm^2/1Mb
Cell efficiency	66%
Supply voltage	1.0V
Organization	64k word x 16bit
Access time	500ps (V_{dd}=1.0V,RT)
Read current	52mA (V_{dd}=1.0V, 2ns cycle)
Write current	23mA (V_{dd}=1.0V, 5ns cycle)

(a) (b)

Fig. 11. 1 Mbit twin 1T-1MTJ STT-MRAM. (a) Chip photo. (b) Chip features [58].

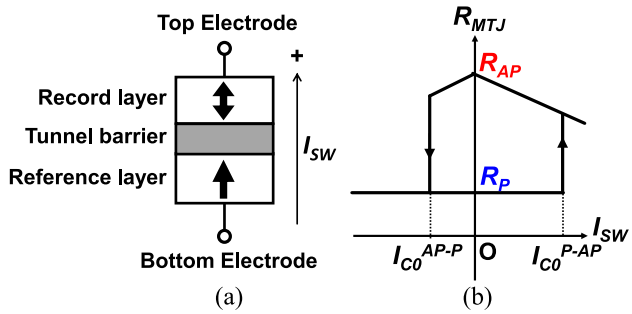


Fig. 12. Asymmetry of resistance-current characteristics of MTJ.

analysis using circuit simulation, a prospect for achieving the read latency of 500 ps by using a feedback type sense amplifier and optimizing the memory cell array configuration [58] has been shown. A fabrication result of 1 Mbit twin 1T-1MTJ STT-MRAM is shown in Fig. 11. The cell size for the twin 1T-1MTJ is 1/4 (0.88 μm^2) compared to 3.46 μm^2 of the 6T-2MTJ STT-MRAM in Fig. 10. The cell area efficiency is almost equal for both cells, thus the macro size per 1 Mbit is also 1/4 (1.40 mm^2 for twin 1T-1MTJ, 5.14 mm^2 for 6T-2MTJ).

B. High-Density Single MTJ Type STT-MRAM

The 1T-1MTJ memory cell, which consists of 1-transistor and 1-MTJ, is the most suitable for main memory application due to its small cell size. There have been issues in circuit design and device/process technology, in order to take full advantage of the 1T-1MTJ memory cell.

Fig. 12 illustrates typical resistance—current (R-I) characteristics of an MTJ, together with a schematic MTJ structure for reference purpose. The switching current generally has an asymmetry that the value of the switching current is different depending on its switching direction [59], [60]. The forward current (I_{C0}^{P-AP}), which inverts the MTJ's magnetization direction from the R_P state to the R_{AP} state, is normally larger than the reverse current (I_{C0}^{AP-P}), which is opposite to the forward current. On the other hand, the memory cell transistor also has an asymmetry in the amount of cell current by its direction because of transistor's body effect, etc. Thus it is important to arbitrate between the two asymmetries so as to avoid causing a mismatch between the current required for MTJ switching and the current allowed to pass the memory cell. This is essential for enlarging the operational margin of scaled 1T-1MTJ memory [61].

Fig. 13 lists the possible combination of the MTJ structure and the cell transistor for a 1T-1MTJ memory cell. The structure of MTJ has two options depending on the longitudinal position

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

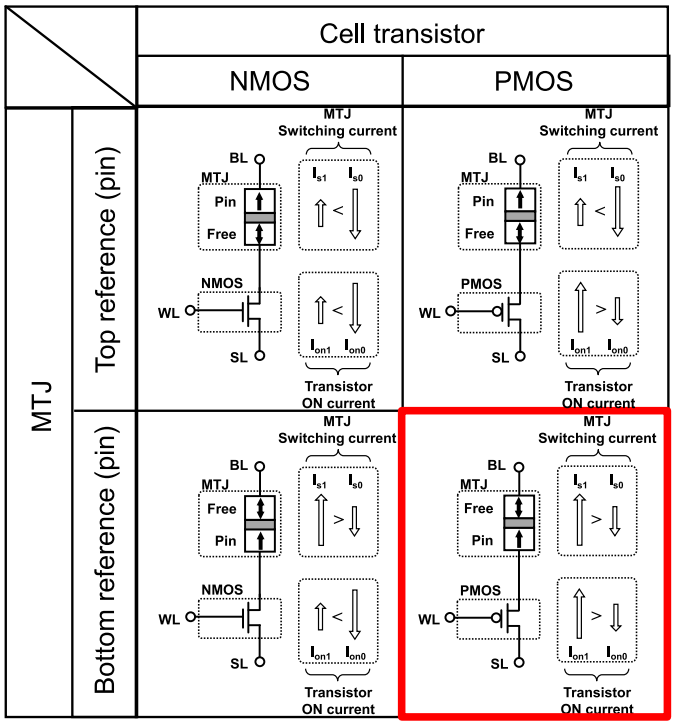


Fig. 13. Possible structure matrix for 1T-1MTJ memory cell. MTJ. The combination of a PMOS FET and a top-pin MTJ has been analyzed in [61].

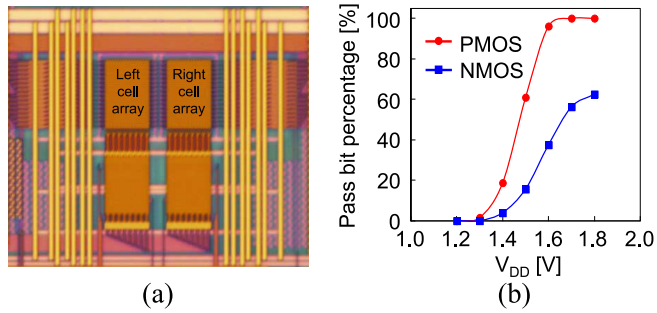


Fig. 14. 1 kbit 1T-1MTJ STT-MRAM test chip for evaluating PMOS—bottom reference structure. (a) Chip photo. (b) Experimental result [61].

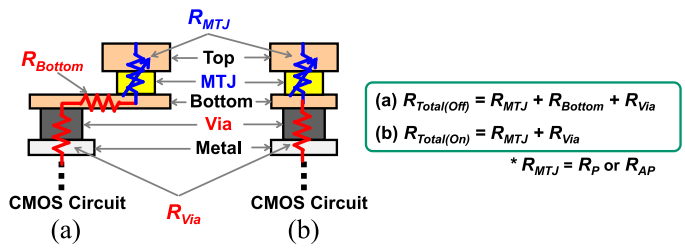


Fig. 15. MTJ film formation: (a) off via, (b) on via. Parasitic resistances and their impact to the *MR ratio* are described.

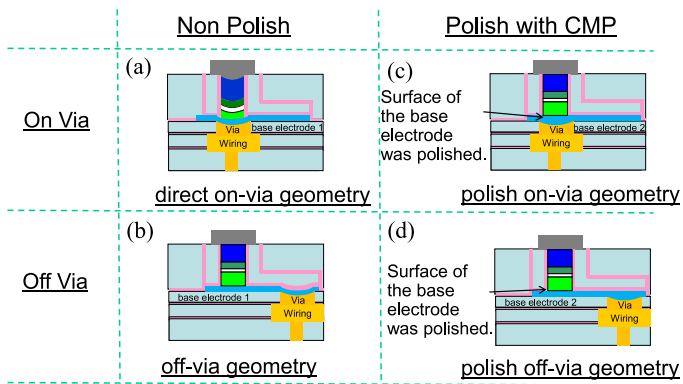


Fig. 16. Experimental conditions to establish MTJ formation process on a via hole [62].

of the reference layer, one is top reference layer and the other is bottom reference layer. The memory cell transistor can be an NMOS FET or a PMOS FET. In this figure, both directions for the current required from MTJ switching and for the current allowed to pass the cell transistor are respectively shown at the right side of each component. The length of each arrow represents their relative magnitudes.

From the viewpoint of current matching, it will be sufficient to consider only two cases, the NMOS – top reference and the PMOS—bottom reference. Several literatures have reported trials for top reference structure [71]–[73], but currently they still have some difficulties in attaining reliable MTJ characteristics.

We focused on PMOS—bottom reference structure. In order to evaluate the PMOS—bottom reference structure, a 1 kbit 1T-1MTJ STT-MRAM test chip was designed and fabricated using 90 nm standard CMOS and 100 nm MTJ process technology. Not only the PMOS cell but also the NMOS cell were prepared. The test chip microphotograph and experimental result are shown in Fig. 14 [61]. As shown in Fig. 14(b), the pass bit percentage for the PMOS cell exceeds that for the NMOS cell. This is because the NMOS cell cannot supply the current enough to switch from P-state to AP-state due to the current matching effect. Particularly, as shown in Fig. 13 (NMOS—bottom reference), the switching current passing through the memory cell is limited by the NMOS transistor for P to AP switching (I_{on1}), while the PMOS cell can provide sufficient switching current. Thus, it was demonstrated that the PMOS—bottom reference structure was effective.

Another issue for realizing high-density 1T-1MTJ STT-MRAM is to establish a process technology achieving a small memory cell size. The formation of MTJ directly on the via hole is especially important because it can drastically shrink the memory cell size. In order to obtain satisfactory magnetic characteristics, roughness must be under a certain level before the deposition of MTJ films. Thus MTJs were formed not directly on the via hole (on-via), which connects the MTJ's electrode to the CMOS circuit, but on the position which is slightly apart from the via hole (off-via), as shown in Fig. 15. Obviously the on-via MTJ is preferable from the viewpoint of small cell area. But the on-via MTJ formation without characteristics degradation is usually difficult, because the surface of a via hole has a curved shape, so-called "dishing".

To realize on-via MTJ formation with satisfactory characteristics, the chemical-mechanical polishing (CMP) technique specifically aiming at this film stack was developed [62]. Fig. 16 lists the experimental condition matrix to verify the effects of with/without CMP and on/off-via. The measured electrical characteristic (*MR ratio*) distributions are shown in Fig. 17. In the

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

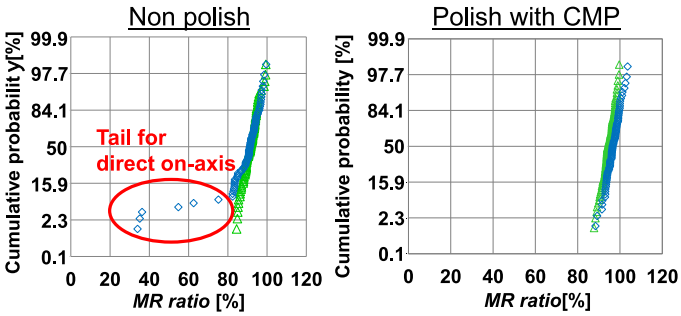


Fig. 17. Experimental result for on-via MTJ formation [62].

Low Power Tech.	Power State	VDD		Clock		MPU State	Cache	Idle Power	Entry/Exit Delay	Mode
		Core	Peri.	Core	Peri.					
N/A	C0	Full Supply	Full Supply	On	On	Keep	Full W/R	Large	No	Normal Operation
Clock Gating	C1	Full Supply	Full Supply	Off	On	Keep	Keep Data	Medium (But No Leak Reduction)	Negligibly Small	Halt
	C2	Full Supply	Full Supply	Off	Off	Keep	Keep Data	Medium (But No Leak Reduction)	Small	Clock Off
Power Gating	C3	Full Supply	Reduced	Off	Off	Lose	Flash Data	Small	Large	Sleep
	C4	Reduced	Reduced	Off	Off	Lose	Flash Data	Very Small	Very Large	Deep Sleep
	>C5	Further Reduced	Further Reduced	Off	Off	Lose	Flash Data	Negligible	Extremely Large	Deeper Sleep

Fig. 18. Example of an MPU's power state list.

case of on-via without CMP, many devices showed degraded *MR ratio*, enclosed by the red circle. On the other hand, with the developed CMP, no device revealed deteriorated *MR ratio*, even obtaining improved *MR ratio* because the parasitic resistance of the on-via with CMP was smaller than that of the off-via with CMP. This can be understood referring the difference of parasitic capacitance between off-via and on-via shown in Fig. 15. The total resistance of off-via device ($R_{\mathrm{Total(Off)}}$ in Fig. 15) is larger by the parasitic resistance of thin-film bottom electrode (R_{Bottom}) than that of on-via device ($R_{Total(On)}$). R_{Bottom} is constant regardless of R_{MTJ} value, and it reduces the total *MR ratio* of the MTJ device. For example, if $R_P/R_{AP} = 3\mathrm{k}/6\mathrm{k}\ \Omega$ (intrinsic $MR\ ratio = 100\%$) and $R_{\mathrm{Bottom}} = 50\ \Omega$, the total $MR\ ratio = 98\%$, about 2% less than intrinsic one. (R_{Via} is neglected here for simplicity.)

Hence the developed CMP technique was effective for the miniaturization of 1T-1MTJ STT-MRAM cell.

C. Spintronics Circuit for Logic LSIs

For realizing low power logic LSIs for future applications, we are focusing on mainly two technologies, 1) power-gating, and 2) logic-in-memory (LiM).

In current logic LSIs, e.g., microprocessors (MPUs) or microcontrollers (MCUs), various power reduction technologies, such as reduced voltage operation, clock gating, and power gating, have been applied. Such logic LSI operation is categorized into some modes that are represented by parameters for several stages, called the processor power states, which are ranked according to their power consumption [74]. Fig. 18 is an example of an MPU's power state list [63]. In general, there exists a tradeoff between the power reduction and the operation performance. In Fig. 18, while the effect of the power reduction is enhanced further as the value of "n" (in Cn)

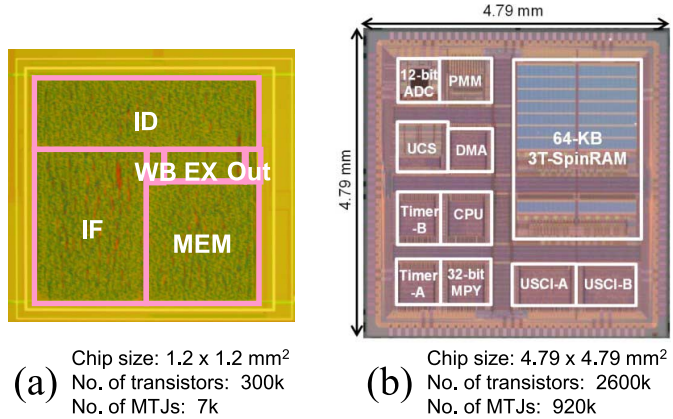
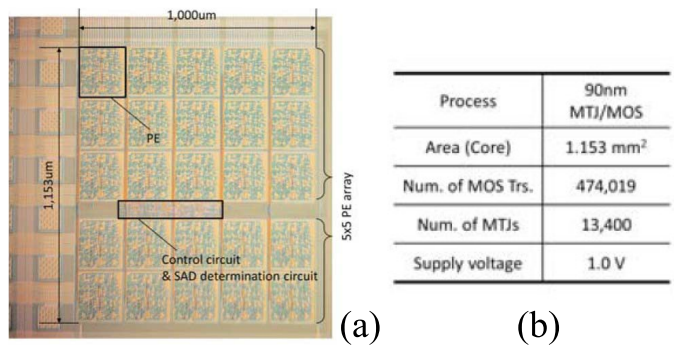


Fig. 19. Developed spintronic logic LSIs applying nonvolatile power-gating technology. (a) 32 bit MPU [63]. (b) 16 bit MCU [65].



Process	90nm MTJ/MOS
Area (Core)	1.153 mm²
Num. of MOS Trs.	474,019
Num. of MTJs	13,400
Supply voltage	1.0 V

Fig. 20. Spintronic LiM chip [66]. (a) chip photo. (b) Chip features.

increases, the penalty for using the mode, i.e., the delay time to enter-into/exit-from the mode (entry/exit delay), increases.

The great advantage of using spintronic nonvolatile flip-flop (NV-FF) [64] or STT-MRAM is to reduce the entry/exit delay drastically, due to fast store/recall operation to/from nonvolatile memories by spintronics. This feature will enable more frequent entry of power-gating mode, resulting in the reduction of total system power.

Logic LSI prototypes based on the above idea have been reported [63], [65], and the chip microphotographs are shown in Fig. 19. Fig. 19(a) is a 32 bit prototype MPU, whose registers and memories are all replaced to NV-FF or STT-MRAM [63]. It achieves 3 μs entry/exit delay, which is one order of magnitude faster than the conventional volatile-memory based deep power down mode. Fig. 19(b) is a 16 bit prototype MCU, which employs a typical set of peripheral circuits, including several kinds of I/O, timers, an A/D converter, etc. [65]. Its entry delay is especially fast, 120 ns, because the MCU's circuit module divided into an optimal size can be controlled for individual power-gating. Moreover, by adding the "dirty bit" memories to nonvolatile registers, which indicates whether memory contents have been changed or not, the frequency of write operation to nonvolatile devices can be restricted to a minimum necessary. This leads to reduce write power to NV-FFs.

Logic-in-memory (LiM) is the computer architecture, which enables the amount of global data transmission to minimize by localizing the data transmission between the memory and the logical operating unit. In this architecture, energy dissipation in

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

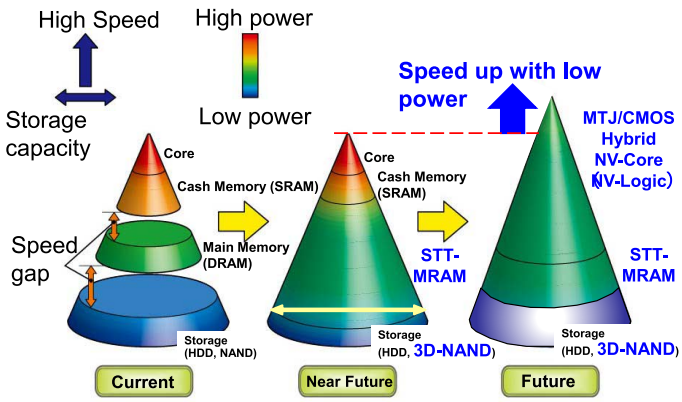


Fig. 21. Future vision of the memory hierarchy in computing system with spintronics technology.

data access can be minimized because the memory function and the logical operation function are compactly unified. This feature fits just to MTJ device, which has the excellent features such as low voltage operability (Table I), good endurance (Table I), and a CMOS compatible structure (Fig. 2) compared to the other kind of emerging memory devices. Also, since an MTJ functions as not only a memory device but also a variable resistor, it can be utilized for a part of logical operating unit by devising circuitry.

A LiM processor prototype based on the above idea is shown in Fig. 20 [66]. This processor is designed for image-processing like motion-vector prediction, realizing 75% leakage reduction compared to a conventional processor, by implementing the newly developed MTJ-based LiM circuit for logic components (full adder, etc.).

D. Future Vision of Spintronics Technology

Our vision for the memory hierarchy in computing system with spintronics technology is illustrated in Fig. 21. This illustration is drawn using a common pyramid manner like Fig. 1, and the additional color-coding which distinguishes the amount of each level's power dissipation.

Low power operation is being achieved in the near future by applying STT-MRAM to working memory. Subsequently further low power and high speed operation will be pursued by developing novel MTJ/CMOS hybrid nonvolatile core circuits.

V. Conclusion

Emerging memories, including Ferroelectric RAM, Phase change RAM, Resistive RAM, Spin-transfer-torque RAM, were reviewed and benchmarked, and their suitable applications were discussed. In particular, the recent developments for the application of spintronics technology to integrated circuits, which we currently focus on, were described in detail. Future energy-saving and high-performance electronics society will be opened by continuing integrating research and development for material/device through circuit/systems of emerging devices.

References

[1] H. Ohno, T. Endoh, T. Hanyu, N. Kasai, and S. Ikeda, "Magnetic tunnel junction for nonvolatile CMOS logic," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2010, pp. 218–221.
[2] T. Endoh, T. Ohsawa, H. Koike, T. Hanyu, and H. Ohno, "Restructuring of memory hierarchy in computing system with spintronics-based technologies," in *Proc. Symp. VLSI Technol. Dig. Tech. Papers*, 2012, pp. 89–90.
[3] T. Endoh, "Nonvolatile logic and memory devices based on spintronics," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2015, pp. 13–16.
[4] E. J. Fluhr *et al.*, "POWER8: A 12-core server-class processor in 22 nm SOI with 7.6 Tb/s off-chip bandwidth," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 96–97.
[5] N. Kurd *et al.*, "Haswell: A family of IA 22 nm processors," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 112–113.
[6] E. Karl *et al.*, "A 4.6 GHz 162 Mb SRAM design in 22 nm tri-gate CMOS technology with integrated active V_{MIN}-enhancing assist circuitry," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 230–231.
[7] H. Pilo *et al.*, "A 64 Mb SRAM in 22 nm SOI technology featuring fine-granularity power gating and low-energy power-supply-partition techniques for 37% leakage reduction," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 322–323.
[8] K. Lim *et al.*, "A 1.2 V 23 nm $6F^2$ 4 Gb DDR3 SDRAM with local-bit-line sense amplifier, hybrid LIO sense amplifier and dummy-less array architecture," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 42–43.
[9] T. Oh *et al.*, "A 3.2 Gbps/pin 8 Gbit 1.0 V LPDDR4 SDRAM with integrated ECC engine for sub-1 V DRAM core operation," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 178–190, Jan. 2015.
[10] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to flash memory," *Proc. IEEE*, vol. 91, no. 4, pp. 489–502, Apr. 2003.
[11] K. Kanda *et al.*, "A 19 nm 112.8 mm^2 64 Gb multi-level flash memory with 400 Mbit/sec/pin 1.8 V toggle mode interface," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 159–167, Jan. 2013.
[12] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Res.*, vol. 3, pp. 147–169, Mar. 2010.
[13] W. I. Kinney, W. Shepherd, W. Miller, J. Evans, and R. Womack, "A non-volatile memory cell based on ferroelectric storage capacitors," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 1987, pp. 850–851.
[14] S. S. Eaton, D. B. Butler, M. Parris, D. Wilson, and H. McNeillie, "A ferroelectric nonvolatile memory," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1988, pp. 130–131.
[15] H. Shiga *et al.*, "A 1.6 GB/s DDR2 128 Mb chain FeRAM with scalable octal bitline and sensing schemes," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 142–152, Jan. 2010.
[16] M. Qazi, M. Clinton, S. Bartling, and A. P. Chandrakasan, "A low-voltage 1 Mb FeRAM in 0.13 μm CMOS featuring time-to-digital sensing for expanded operating margin in scaled CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 208–209.
[17] N. Setter *et al.*, "Ferroelectric thin films: Review of materials, properties, and applications," *J. Appl. Phys.*, vol. 100, p. 051606, Sep. 2006.
[18] S. Lai and T. Lowrey, "OUM–A 180 nm nonvolatile memory cell element technology for stand alone and embedded applications," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2001, pp. 803–806.
[19] M. Gill, T. Lowrey, and J. Park, "Ovonic unified memory–A high-performance nonvolatile memory technology for stand-alone memory and embedded applications," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2002, pp. 202–203.
[20] K. Osada *et al.*, "Phase change RAM operated with 1.5-V CMOS as low cost embedded memory," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2005, pp. 431–434.
[21] S. H. Lee *et al.*, "Highly productive PCRAM technology platform and full chip operation: Based on $4F^2$ (84 nm pitch) cell scheme for 1 Gb and beyond," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2011, pp. 47–50.
[22] Y. Choi *et al.*, "A 20 nm 1.8 V 8 Gb PRAM with 40 MB/s program bandwidth," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 46–47.
[23] H.-S. P. Wong *et al.*, "Phase change memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, Dec. 2010.
[24] W. W. Zhuang *et al.*, "Novell colossal magnetoresistive thin film nonvolatile resistance random access memory (RRAM)," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2002, pp. 193–196.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[25] I. G. Baek *et al.*, "Highly scalable non-volatile resistive memory using simple binary oxide driven by asymmetric unipolar voltage pulses," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2004, pp. 587–590.

[26] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nat. Mater.*, vol. 6, pp. 833–840, Nov. 2007.

[27] H. Y. Lee *et al.*, "Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO_2 based RRAM," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2008, pp. 297–300.

[28] S. Sheu *et al.*, "A 4 Mb embedded SLC resistive-RAM macro with 7.2 ns read-write random-access time and 160 ns MLC-access capability," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 200–201.

[29] A. Kawahara *et al.*, "An 8 Mb multi-layered cross-point ReRAM macro with 443 MB/s write throughput," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 432–433.

[30] T. Liu *et al.*, "A 130.7-mm^2 2-layer 32-Gb ReRAM memory device in 24-nm technology," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 140–153, Jan. 2014.

[31] R. Fackenthal *et al.*, "A 16 Gb ReRAM with 200 MB/s write and 1 GB/s read in 27 nm technology," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 338–339.

[32] H.-S. P. Wong *et al.*, "Metal–oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012.

[33] M. Hosomi *et al.*, "A novel nonvolatile memory with spin torque transfer magnetization switching: Spin-RAM," in *Proc. Int. Electron Devices Meeting Tech. Dig.*, 2005, pp. 459–462.

[34] T. Kawahara *et al.*, "2 Mb SPRAM (SPin-Transfer Torque RAM) with bit-by-bit bi-directional current write and parallelizing-direction current read," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 109–120, Jan. 2008.

[35] K. Tsuchida *et al.*, "A 64 Mb MRAM with clamped-reference and adequate-reference schemes," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 258–259.

[36] S. C. Oh *et al.*, "On-axis scheme and novel MTJ structure for sub-30 nm Gb density STT-MRAM," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2010, pp. 300–303.

[37] S. Chung *et al.*, "Fully integrated 54 nm STT-RAM with the smallest bit cell dimension for high density memory application," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2010, pp. 304–307.

[38] E. Chen *et al.*, "Progress and prospects of spin transfer torque random access memory," *IEEE Trans. Magn.*, vol. 48, no. 11, pp. 3025–3030, Nov. 2012.

[39] N. D. Rizzo *et al.*, "A fully functional 64 Mb DDR3 ST-MRAM built on 90 nm CMOS technology," *IEEE Trans. Magn.*, vol. 49, no. 7, pp. 4441–4446, Jul. 2013.

[40] S. Ikeda *et al.*, "Magnetic tunnel junctions for spintronic memories and beyond," *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 991–1002, May 2007.

[41] S. Fukami *et al.*, "Advances in spintronics devices for microelectronics – from spin-transfer torque to spin-orbit torque," in *Proc. Asia South Pacific Design Automat. Conf.*, 2014, pp. 684–691.

[42] M. Julliere, "Tunneling between ferromagnetic films," *Phys. Lett.*, vol. 54A, no. 3, pp. 225–226, Sep. 1975.

[43] W. H. Butler, X.-G. Zhang, T. C. Schulthess, and J. M. MacLaren, "Spin-dependent tunneling conductance of $Fe|MgO|Fe$ sandwiches," *Phys. Rev. B*, vol. 63, no. 5, p. 054416, Jan. 2001.

[44] J. Mathon and A. Umerski, "Theory of tunneling magnetoresistance of an epitaxial Fe/MgO/Fe(001) junction," *Phys. Rev. B*, vol. 63, no. 22, p. 220403(R), May 2001.

[45] S. S. P. Parkin *et al.*, "Giant tunnelling magnetoresistance at room temperature with MgO (100) tunnel barriers," *Nature Mater.*, vol. 3, pp. 862–864, Dec. 2004.

[46] S. Yuasa, T. Nagahama, A. Fukushima, Y. Suzuki, and K. Ando, "Giant room-temperature magnetoresistance in single-crystal Fe/MgO/Fe magnetic tunnel junctions," *Nature Mater.*, vol. 3, pp. 868–871, Dec. 2004.

[47] S. Ikeda *et al.*, "Tunnel magnetoresistance of 604% at 300 K by suppression of Ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature," *Appl. Phys. Lett.*, vol. 93, no. 8, p. 082508, Aug. 2008.

[48] R. Takemura *et al.*, "A 32-Mb SPRAM with 2T1R memory cell, localized bi-directional write driver and '1'/'0' dual-array equalized reference scheme," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 869–879, Apr. 2010.

[49] S. Ikeda *et al.*, "A perpendicular-anisotropy CoFeB-MgO magnetic tunnel junction," *Nature Mater.*, vol. 9, pp. 721–724, Sep. 2010.

[50] H. Sato *et al.*, "CoFeB thickness dependence of thermal stability factor in CoFeB/MgO perpendicular magnetic tunnel junctions," *IEEE Magn. Lett.*, vol. 3, p. 3000204, Apr. 2012.

[51] H. Sato *et al.*, "Perpendicular-anisotropy CoFeB-MgO magnetic tunnel junctions with a MgO/CoFeB/Ta/CoFeB/MgO recording structure," *Appl. Phys. Lett.*, vol. 101, no. 2, p. 022414, Jul. 2012.

[52] H. Sato *et al.*, "MgO/CoFeB/Ta/CoFeB/MgO recording structure in magnetic tunnel junctions with perpendicular easy axis," *IEEE Trans. Magn.*, vol. 49, no. 7, pp. 4437–4440, Jul. 2013.

[53] H. Sato *et al.*, "Co/Pt multilayer based reference layers in magnetic tunnel junctions for nonvolatile spintronics VLSIs," *Jpn. J. Appl. Phys.*, vol. 53, p. 04EM02, Feb. 2014.

[54] H. Sato *et al.*, "Comprehensive study of CoFeB-MgO magnetic tunnel junction characteristics with single- and double-interface scaling down to 1X nm," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2013, pp. 60–63.

[55] S. Ikeda *et al.*, "Perpendicular-anisotropy CoFeB-MgO based magnetic tunnel junctions scaling down to 1X nm," in *Int. Electron Devices Meet. Tech. Dig.*, 2014, pp. 796–799.

[56] H. Honjo *et al.*, "10 $nm\phi$ perpendicular-anisotropy CoFeB-MgO magnetic tunnel junction with over 400° C high thermal tolerance by boron diffusion control," in *Symp. VLSI Technol. Dig. Tech. Papers*, 2015, pp. 160–161.

[57] T. Ohsawa *et al.*, "A 1.5 nsec/2.1 nsec random read/write cycle 1 Mb STT-RAM using 6T2MTJ cell with background write for nonvolatile e-memories," in *Symp. VLSI Technol. Dig. Tech. Papers*, 2013, pp. 110–111.

[58] T. Ohsawa *et al.*, "A 500 ps/8.5 ns array read/write latency 1 Mb twin 1T1MTJ STT-MRAM designed in 90 nm CMOS/40 nm MTJ process with novel positive feedback S/A circuit," in *Proc. Int. Conf. Solid State Devices Mater.*, 2014, pp. 458–459.

[59] Z. Diao *et al.*, "Spin transfer switching and spin polarization in magnetic tunnel junctions with MgO and AlOx barriers," *Appl. Phys. Lett.*, vol. 87, p. 232502, Dec. 2005.

[60] W. Zhu, H. Li, Y. Chen, and X. Wang, "Current switching in MgO-based magnetic tunneling junctions," *IEEE Trans. Magn.*, vol. 47, no. 1, pp. 156–160, Jan. 2011.

[61] H. Koike *et al.*, "Wide operational margin capability of 1 kbit spin-transfer-torque memory array chip with 1-PMOS and 1-bottom-pin-magnetic-tunnel-junction type cell," *Jpn. J. Appl. Phys.*, vol. 53, p. 04ED13, Mar. 2014.

[62] S. Miura *et al.*, "Properties of perpendicular-anisotropy magnetic tunnel junctions fabricated over the bottom electrode contact," *Jpn. J. Appl. Phys.*, vol. 54, p. 04DM06, Mar. 2015.

[63] H. Koike *et al.*, "A power-gated MPU with 3-microsecond entry/exit delay using MTJ-based nonvolatile flip-flop," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2013, pp. 317–320.

[64] T. Endoh *et al.*, "A 600 MHz MTJ-based nonvolatile latch making use of incubation time in MTJ switching," in *Proc. Int. Electron Devices Meet. Tech. Dig.*, 2011, pp. 75–78.

[65] N. Sakimura *et al.*, "A 90 nm 20 MHz fully nonvolatile microcontroller for standby-power-critical applications," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 184–185.

[66] M. Natsui *et al.*, "Nonvolatile logic-in-memory array processor in 90 nm MTJ/MOS achieving 75% leakage reduction using cycle-based power gating," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 194–195.

[67] R. Scheuerlein *et al.*, "A 10 ns read and write non-volatile memory array using a magnetic tunnel junction and FET switch in each cell," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2000, pp. 128–129.

[68] M. Durlam *et al.*, "Nonvolatile RAM based on magnetic tunnel junction elements," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2000, pp. 130–131.

[69] J. C. Slonczewski, "Current-driven excitation of magnetic multilayers," *J. Magn. Magn. Mater.*, vol. 159, no. 1/2, pp. L1–L7, Jun. 1996.

[70] L. Berger, "Emission of spin waves by a magnetic multilayer traversed by a current," *Phys. Rev. B, Condens. Matter*, vol. 54, no. 13, pp. 9353–9358, Jan. 1996.

[71] Y. M. Lee *et al.*, "Highly scalable STT-MRAM with MTJs of top-pinned structure in 1T/1MTJ cell," in *Symp. VLSI Technol. Dig. Tech. Papers*, 2010, pp. 49–50.

[72] C. Yoshida *et al.*, "Enhanced thermal stability in perpendicular top-pinned magnetic tunnel junction with synthetic antiferromagnetic free layers," *IEEE Trans. Magn.*, vol. 49, no. 7, pp. 4363–4366, Jul. 2013.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[73] Y. Iba *et al.*, "Top-pinned perpendicular MTJ structure with a counter bias magnetic field layer for suppressing a stray-field in highly scalable STT-MRAM," in *Symp. VLSI Technol. Dig. Tech. Papers*, 2013, pp. 136–137.
[74] Advanced configuration and power interface specification5.0 ed. 2011.
[75] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories–nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, pp. 2632–2663, Mar. 2009.
[76] G. Naso *et al.*, "A 128 Gb 3 b/cell NAND flash design using 20 nm planar-cell technology," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 218–219.
[77] K.-T. Park *et al.*, "Three-dimensional 128 Gb MLC vertical NAND flash memory with 24-WL stacked layers and 50 MB/s high-speed programming," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 204–213, Jan. 2015.
[78] K. Suzuki and S. Swanson, "A survey of trends in non-volatile memory technologies: 2000–2014," in *Proc. IEEE Int. Memory Workshop*, 2015, pp. 65–68.
[79] M. A. A. Sanvido, F. R. Chu, A. Kulkarni, and R. Selinger, "NAND flash memory and its role in storage architectures," *Proc. IEEE*, vol. 96, no. 11, pp. 1864–1874, Nov. 2008.
[80] J. D. Davis *et al.*, "7 GHz L1 cache SRAMs for the 32 nm zEnterprise™ EC12 processor," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 324–325.
[81] M.-F. Chang *et al.*, "A 28 nm 256 kb 6T-SRAM with 280 mV improvement in V_{MIN} using a dual-split-control assist scheme," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2015, pp. 314–315.
[82] Y.-H. Chen *et al.*, "A 16 nm 128 Mb SRAM in high-κ metal-gate FinFET technology with write-assist circuitry for low-VMIN applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 170–177, Jan. 2015.
[83] Y. Yang *et al.*, "SRAM design for 22-nm ETSOI technology: Selective cell current boosting and asymmetric back-gate write-assist circuit," *IEEE Trans. Circuit and Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1538–1545, Jun. 2015.

Tetsuo Endoh (M'89) received the B.S. degree in physics from the University of Tokyo, Tokyo, Japan, in 1987, and the Ph.D. degree in electronic engineering from Tohoku University, Sendai, Japan, in 1995.

He joined Toshiba Corporation in 1987, where he was engaged in research on NAND-type flash memory and advanced CMOS device design at ULSI Research Laboratories, the Research and Development Center, Toshiba Corporation, Kawasaki, Japan. He became a Lecturer with the Research Institute of Electrical Communication, Tohoku University, Sendai, Japan, in 1995, an Associate Professor in 1997, and a Professor in April 2008. He became a Professor with the Center for Interdisciplinary Research, Tohoku University, in May 2008. Currently, he has been a Professor with the Graduate School of Engineering, Tohoku University, since May 2012. He has also been the Deputy Director of the Center for Spintronics Integrated Systems, Tohoku University, since March 2010, and the Director of the Center for Innovative Integrated Electronic Systems, Tohoku University, since October 2012. He has been engaged in research on advanced CMOS device design (e.g., 3DMOS devices, vertical MOS devices, etc.), clean room technology, low-power and high-speed circuit technology and advanced memory (e.g., 3D memory and memory based on novel principles). He was a member of the "High-performance Low-power Consumption Spin Devices and Storage Systems" program as part of the Research and Development for Next-Generation Information Technology program of MEXT. He is currently engaged in the development of novel nano-LSI with hybrid technology between spin memory devices and extended CMOS technology. He has served as the research leader of the Research and Development of Vertical Body Channel MOSFET and Its Integration Process project as part of the Research of Innovative Material and Process for Creation of Next-generation Electronics Devices program of JST-CREST. He has also served as a research subleader of the Research and Development of Ultra-low Power Spintronics-based Logic VLSIs program as part of the Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program).

Dr. Endoh is a Fellow of the Japan Society of Applied Physics (JSAP) and a member of the Institute of Electronics, Information, and Communication Engineers (IEICE). He was the recipient of the LSI IP Design Award in 2001, the Japanese Journal of Applied Physics (JJAP) Paper Award in 2009, the 6th Fellow Award of the Japan Society of Applied Physics in 2012, and the 2012 International Conference on Solid State Devices and Materials (SSDM) Paper Award in 2012. He assumed an International Collaboration Fellow of Sendai city in 2012.

Hiroki Koike (M'99) received the B.S. degree in physics from the Tokyo Institute of Technology, Tokyo, Japan, in 1987, and a Doctoral degree in computer science from the Kyushu Institute of Technology, Kyushu, Japan, in 2006.

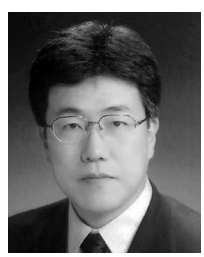
In 1987, he joined the NEC Corporation, where he was engaged in research and development for DRAM, FeRAM, and NOR Flash memories. Since 2010, he has been a Research Associate of the Center for Spintronics Integrated Systems, Tohoku University. His research interests mainly include the design of analog, digital, and memory circuits combined with emerging devices.

Dr. Koike is a member of the Japan Society of Applied Physics (JSAP), and the Institute of Electronics, Information and Communication Engineers (IEICE).

Shoji Ikeda received the B.S., M.S., and D.E. degrees from Muroran Institute of Technology, Muroran, Japan, in 1991, 1993, and 1996, respectively.

He was a Research Associate with the Department of Electrical and Electronic Engineering at the Muroran institute of Technology from 1996 to 1999. He joined Fujitsu Limited, Atsugi/Nagano, Japan from 1999 to 2003. In 2003, he joined Tohoku University, Sendai, Japan, where he was an Associate Professor at Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University from 2003 to 2014. He is currently Professor at Center for Innovative Integrated Electronic Systems, Tohoku University. His current research interests include magnetic metal devices with nanostructures and their application such as STT-MRAM.

Dr. Ikeda received the MSJ (Magnetics Society of Japan) Distinguished Paper Award (2003), APEX/JJAP Paper Award (2009), DPS Best Paper Award (2011), and SSDM Paper Award (2012).



Takahiro Hanyu (S'87–M'89–SM'12) received the B.E., M.E., and D.E. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1984, 1986, and 1989, respectively.

He is currently a Professor in the Research Institute of Electrical Communication, Tohoku University. His general research interests include nonvolatile logic circuits and their applications to ultra-low-power and/or highly dependable VLSI processors, and multiple-valued current-mode circuit and its application to power-aware asynchronous network-on-chip systems.

Dr. Hanyu received the Sakai Memorial Award from the Information Processing Society of Japan in 2000, the Judge's Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002, the Special Feature Award at the University LSI Design Contest from ASP-DAC in 2007, the APEX Paper Award of Japan Society of Applied Physics in 2009, the Excellent Paper Award of IEICE, Japan, in 2010, Ichimura Academic Award in 2010, the Best Paper Award of IEEE ISVLSI 2010, the Paper Award of SSDM 2012, the Best Paper Finalist of IEEE ASYNC 2014, and the Commendation for Science and Technology by MEXT, Japan in 2015.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

Hideo Ohno (M'82) received the Ph.D. degree from the University of Tokyo, Tokyo, Japan, in 1982.

He is Director of Research Institute of Electrical Communication, Tohoku University, Director of Center for Spintronics Integrated System, Tohoku University, Principal Investigator of WPI Advanced Institute for Materials Research, Tohoku University and Professor of Center for Innovative Integrated Electronic Systems, Tohoku University. He has published 500 papers in the field of spintronics and semiconductor science and technology, which have been cited over 30 000 times.

Prof. Ohno received the IBM Japan Science Award (1998), the IUPAP Magnetism Prize (2003), Japan Academy Prize (2005), Presidential Prize for Research Excellence, Tohoku University (2005), and the 2005 Agilent Technologies Europhysics Prize. He has been a Fellow of the Institute of Physics (IOP) since 2004, an honorary professor of Institute of Semiconductors, Chinese Academy of Sciences since 2006, a Fellow of the Japan Society of Applied Physics (JSAP) since 2007 and a fellow of American Physical Society (APS) since 2012. Tohoku University appointed him as a distinguished professor. IEEE Magnetics Society named him for the Distinguished Lecturer for 2009. He was awarded the Thomson Reuters Citation Laureate (2011), the JSAP Outstanding Achievement Award and IEEE David Sarnoff Award (2012), and JSAP Compound Semiconductor Electronics Achievement Award (2014).