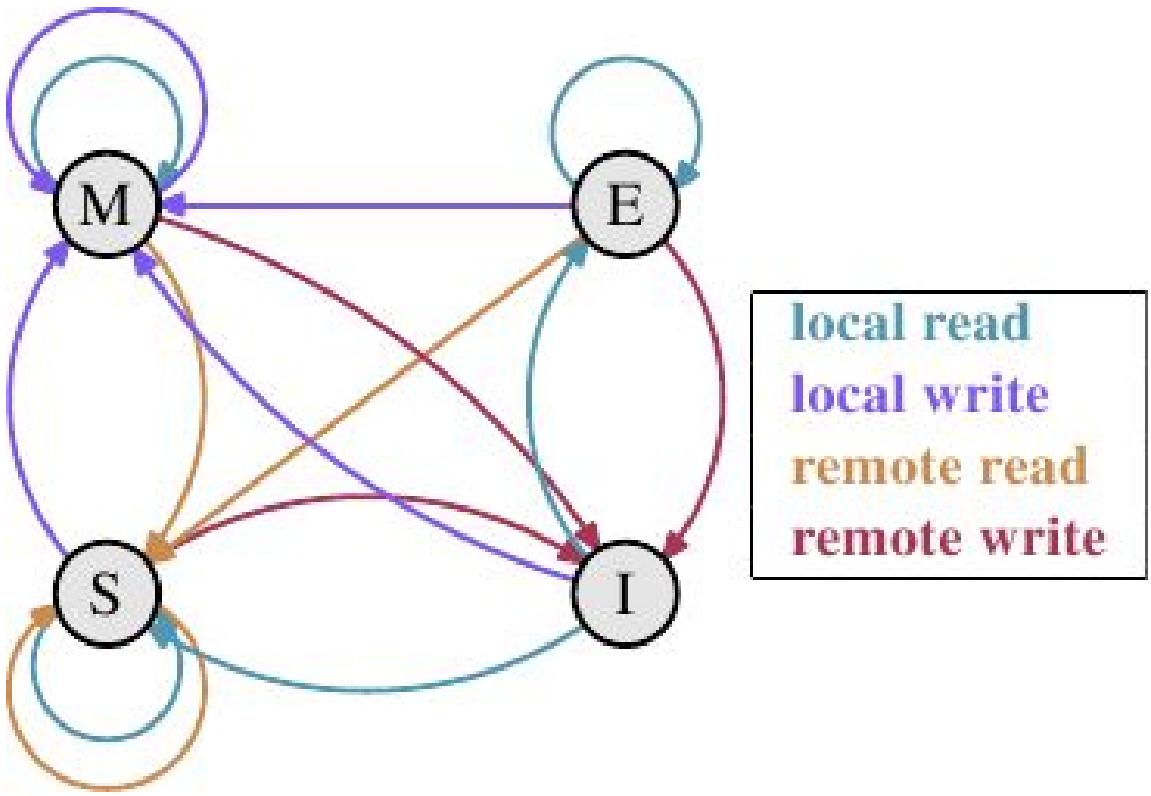
ECE6100 PROJECT 3

Cache Coherence Protocol



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Protocols Intro

1* MESI

State	Processor Request		Snoop Request		
	PrRd	PrWr	BusRd	BusWr	Data
M	M	M	S	I	~
E	E	M	S	I	~
S	S	SM	S	I	~
I	IS	IM	~	~	~
IM	~	~	~	~	M
IS	~	~	~	~	E/S
SM	~	~	~	IM	~

Here **SM is necessary** because still you have to have those who are in SM state **set_shared_line** for those who wants to read, since in their requests to write has not been handled so they are still in S state as in real-life implementation. SM just means that they have sent out request for writing.

2* MOSI

State	Processor Request		Snoop Request		
	PrRd	PrWr	BusRd	BusWr	Data
M	M	M	O	I	~
O	O	OM	O	I	~
S	S	SM	S	I	~
I	IS	IM	~	~	~
IM	~	~	~	~	M
IS	~	~	~	~	S

SM	~	~	~	IM	~
OM	~	~	~	IM	~

The difference of SM and OM is that OM, when receiving its own GETM on bus, turns to IM at the same time, it send data onto bus.

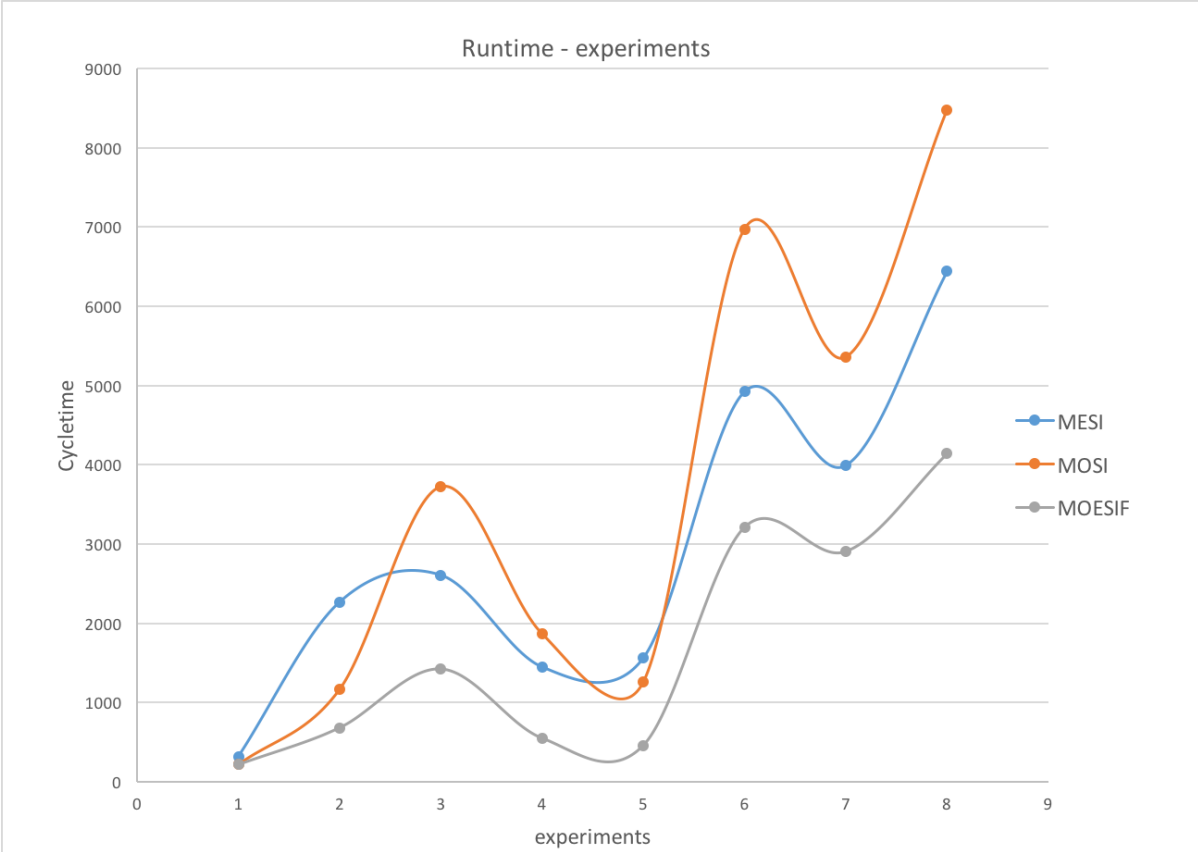
3* MOESIF

State	Processor Request		Snoop Request		
	PrRd	PrWr	BusRd	BusWr	Data
M	M	M	O	I	~
O	O	OM	O	I	~
E	E	M	F	I	~
S	S	SM	S	I	~
I	IS	IM	~	~	~
F	F	FM	F	I	~
IM	~	~	~	~	M
IS	~	~	~	~	E/S
SM	~	~	~	IM	~
OM	~	~	~	IM	~
FM	~	~	~	IM	~

In Red : set shared line
In Orange: send data on bus
In Blue: both

Experiments

1* Cycle Time



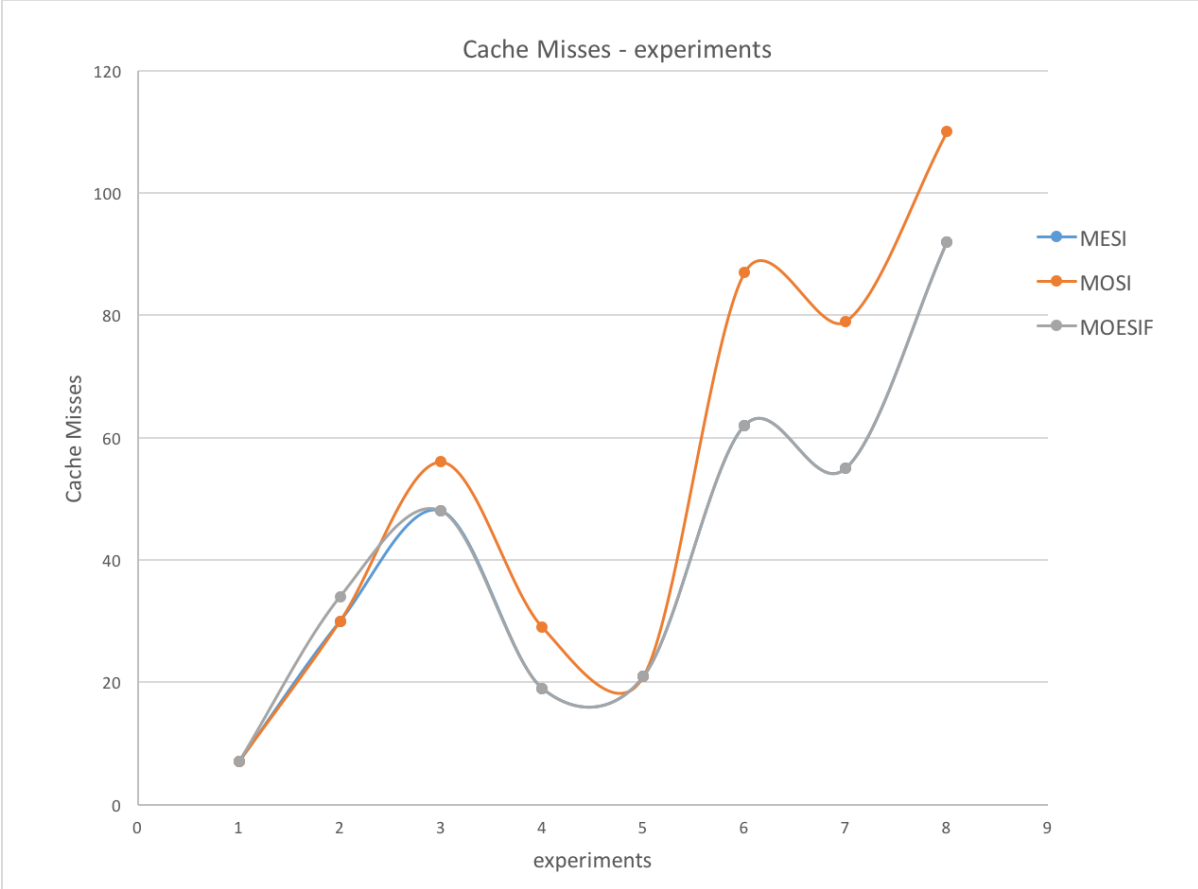
Conclusion:

- In terms of runtime, superiority:

  MOESIF > MESI > MOSI
- The advantage of E stage is that it can silently upgrades to M, which decreaes the bus traffic and the memory accesses (since in MOSI, S stage cache cannot forward data to I stage cache who wants to read, while an E stage cache can) .
- The advantage of O stage is that dirty blocks don't have to be written back to memory right now, instead it can stay in several caches and can be directly forwarded to an incoming I-stage cache who wants to read, which apparently decreases the memory accesses, thus decreasing the total runtime.
- MOESIF definitely avoids memory access to the most degree and therefore is the best protocol among the three.
- However, superiority of MESI and MOSI actually depends largely on the experiment data. There is only one experiment, the 5th, which manifests the

superiority of MOSI over MESI. Because it is the only one that there is no silent upgrades and less $ to $ transfer.

2* Cache Miss



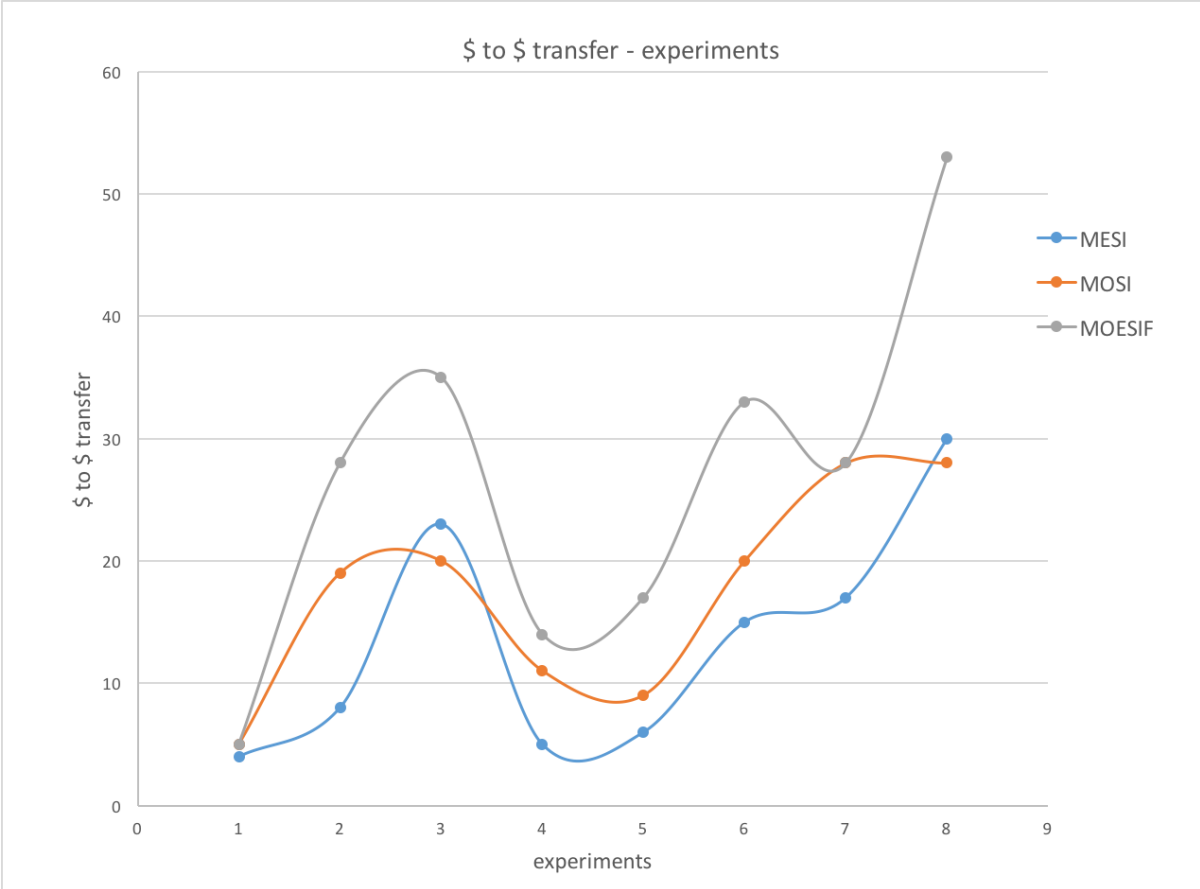
Conclusion:

- In terms of cache miss, superiority:

  MOESIF = MESI > MOSI

- This is because whenS-stage cache writes, without Busupgr, it still has to access memory and be treated as cache miss. Since MESI has E stage, less often the caches would be in S stage.

3* $ to $ Transfer



Conclusion:

- In terms of cache-to-cache transfer , superiority:

  MOESIF > MOSI > MESI
- This is because O stage can always forward dirty blocks to others in I-stage who wants to read.