Instruction	Fetch Inst (T0)	T1	T2	T3	T4	T5	T6	
mv Rx, Ry	ld_ir = 1 pc_inc = 1	Rout = Yreg Rin = Xreg ld_addr = 1	o_mem_rd = 1 done = 1					
add	ld_ir = 1 pc_inc = 1	(put Rx in A) Rout = Xreg Ain = 1	(put Ry on bus and add) Rout = Yreg addsub = 0 Gin = 1	(put g in rx) gout = 1 rin = xreg ldnz = 1 wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1			
sub	ld_ir = 1 pc_inc = 1	(put Rx in A) Rout = Xreg Ain = 1	(put Ry on bus and add) Rout = Yreg addsub = 1 Gin = 1	(put g in rx) gout = 1 ldnz = 1 rin = xreg wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1			
cmp	ld_ir = 1 pc_inc = 1	(put Rx in A) Rout = Xreg Ain = 1	(put Ry on bus and add) Rout = Yreg addsub = 1 Gin = 1	(put g on bus) gout = 1 ldnz = 1 wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1			
ld	ld_ir = 1 pc_inc = 1	(put ry in addr) Rout = Yreg wr = 1 ld_addr = 1	wait 1 cycle to synch o_mem_rd = 1	sel = 0 (rout = 0) rin = xreg done = 1 wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1			
st	ld_ir = 1 pc_inc = 1	(put ry in addr) Rout = Yreg wr = 1 ld_addr = 1	(put rx in data) Rout = Xreg wr = 1 ld_data = 1	o_mem_wr = 1	wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1		
mvi	ld_ir = 1 pc_inc = 1	s8out = 1 rin = xreg wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1					

Instruction	Fetch Inst (T0)	T1	T2	T3	T4	T5	T6	
addi	ld_ir = 1 pc_inc = 1	rout = xreg ain = 1	s8out = 1 gin= 1	(put g in rx) gout = 1 rin = xreg ldnz = 1 wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1			
subi	ld_ir = 1 pc_inc = 1	rout = xreg ain = 1	s8out = 1 addsub = 1 gin = 1	(put g in rx) gout = 1 rin = xreg ldnz = 1 wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1			
cmpi	ld_ir = 1 pc_inc = 1	rout = xreg addsub = 1 ain = 1	s8out = 1 addsub = 1 gin = 1	gout = 1 ldnz = 1 done = 1 ld_addr = 1	o_mem_rd = 1 done = 1			
mvhi	ld_ir = 1 pc_inc = 1	8out = 1 rin = xreg wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1					
jr	ld_ir = 1 pc_inc = 1	(put rx on buswire) rout = xreg ld_pc = 1	(put pc on buswire and read) wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1				
jzr	ld_ir = 1 pc_inc = 1	if (z) rout = xreg ld_pc = 1 else, ld_addr	if (z) ld else rd pc and done					
jnr	ld_ir = 1 pc_inc = 1	if (n) rout = xreg ld_pc = 1 else, rd pc and done						
callr	ld_ir = 1 pc_inc = 1	pc_out = 1 rin = 00000001 ldpc7 = 1	rout = rx ld_pc = 1	(put pc on buswire and read) wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1			
j	ld_ir = 1 pc_inc = 1	put sext11 in A s11out = 1 ain = 1	put PC and add pcout = 1 addsub = 0 gin = 1	put g in pc gout = 1 ld_pc = 1	(put pc on buswi wr = 0 ld_addr = 1	o_mem_rd = 1 done = 1		
jz	ld_ir = 1 pc_inc = 1	if (z) do above else ld_addr	if (z) do above else done and o_mem_addr					

Instruction	Fetch Inst (T0)	T1	T2	T3	T4	T5	T6	
jn	ld_ir = 1 pc_inc = 1	if (n) do above						
call	ld_ir = 1 pc_inc = 1	pc_out = 1 rin = 00000001 ldpc7 = 1	put sext11 in A s11out = 1 ain = 1	put PC and add pcout = 1 addsub = 0 gin = 1	put g in pc gout = 1 ld_pc = 1	(put pc on buswi wr = 0 ld_addr = 1	(put pc on buswire and read) done = 1 o_mem_rd =1	