EECS 16A Designing Information Devices and Systems I
Summer 2017 D. Aranki, F. Maksimovic, V. Swamy Homework 5

This homework is due on Sunday, July 23, 2017, at 23:59.
Self-grades are due on Monday, July 24, 2017, at 23:59.

Submission Format
Your homework submission should consist of **one** file.

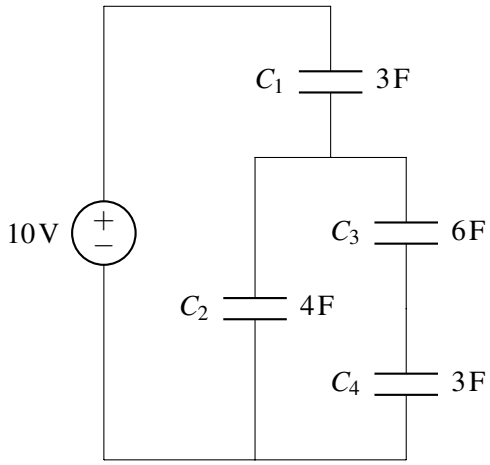
- `hw5.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

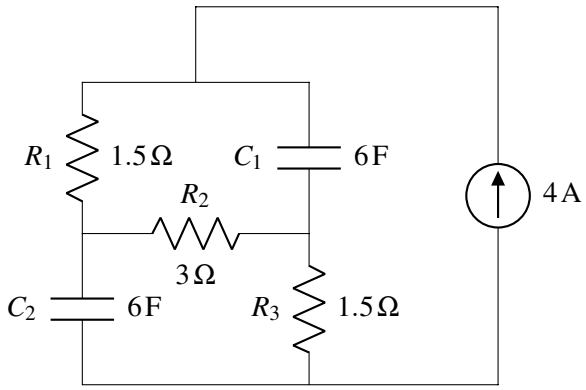
1. Mechanical Circuits with Capacitors and Resistors

(a) Find the voltages across and currents flowing through all of the capacitors in steady state.

current = 0?

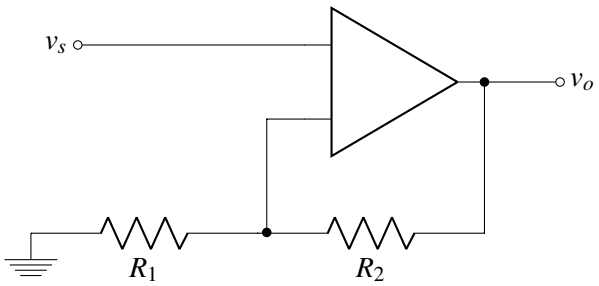


(b) Find the voltages across and currents flowing through all the resistors and capacitors in steady state.

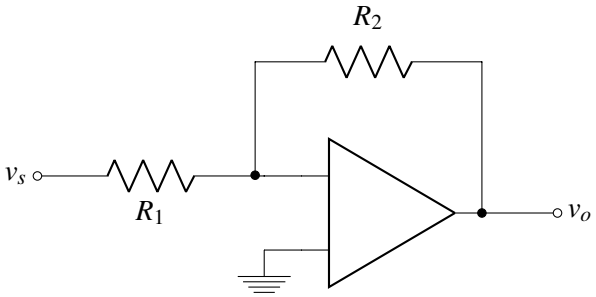


2. Basic Amplifier Building Blocks

The following amplifier stages are used often in many circuits and are well known as (a) the non-inverting amplifier and (b) the inverting amplifier.



(a)



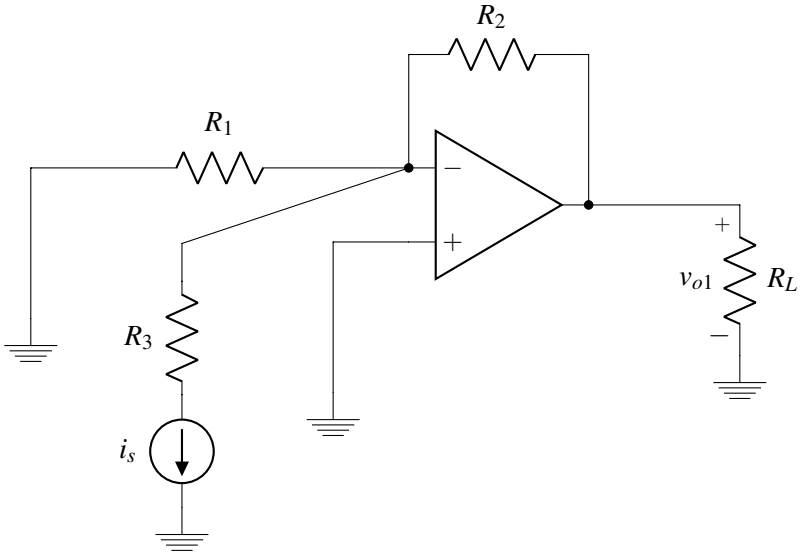
(b)

(a) Label the input terminals of the op-amp labeled (a), so that it is in negative feedback. Then derive the voltage gain of the non-inverting amplifier using the Golden Rules. Explain the origin of the name of the amplifier.

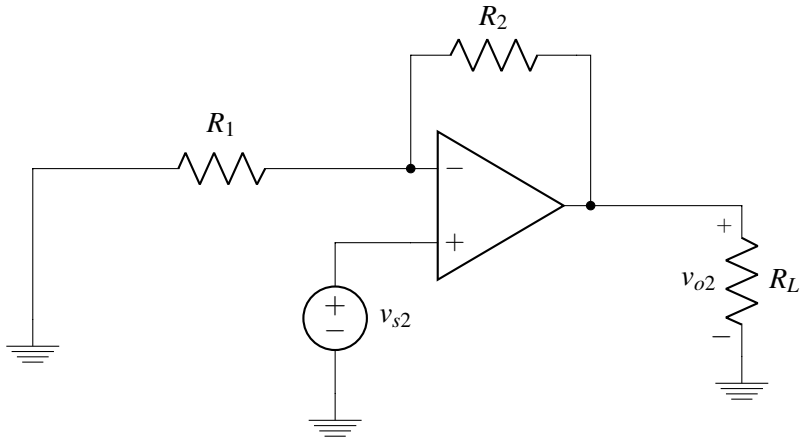
(b) Label the input terminals of the op-amp labeled (b), so that it is negative feedback. Then derive the voltage gain of the inverting amplifier using the Golden Rules. Explain the origin of the name of the amplifier.

3. Amplifier with Multiple Inputs

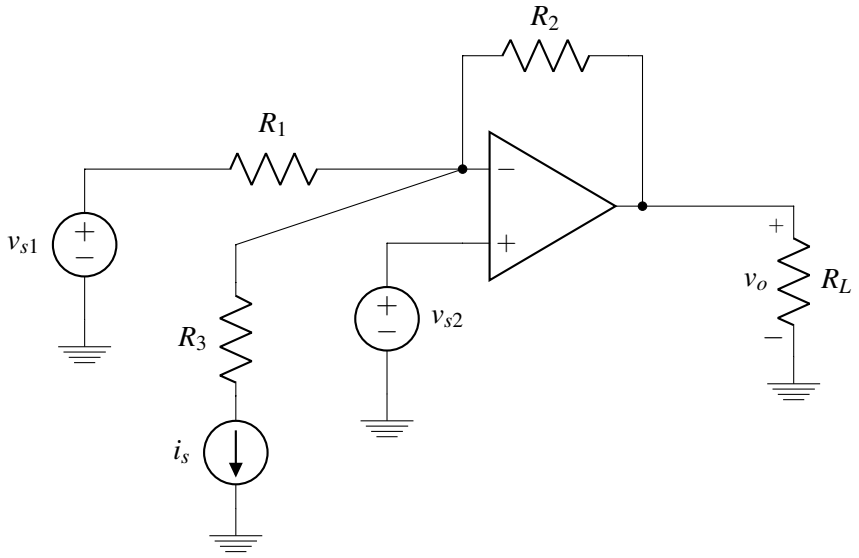
(a) Use the Golden Rules to find v_{o1} for the circuit below.



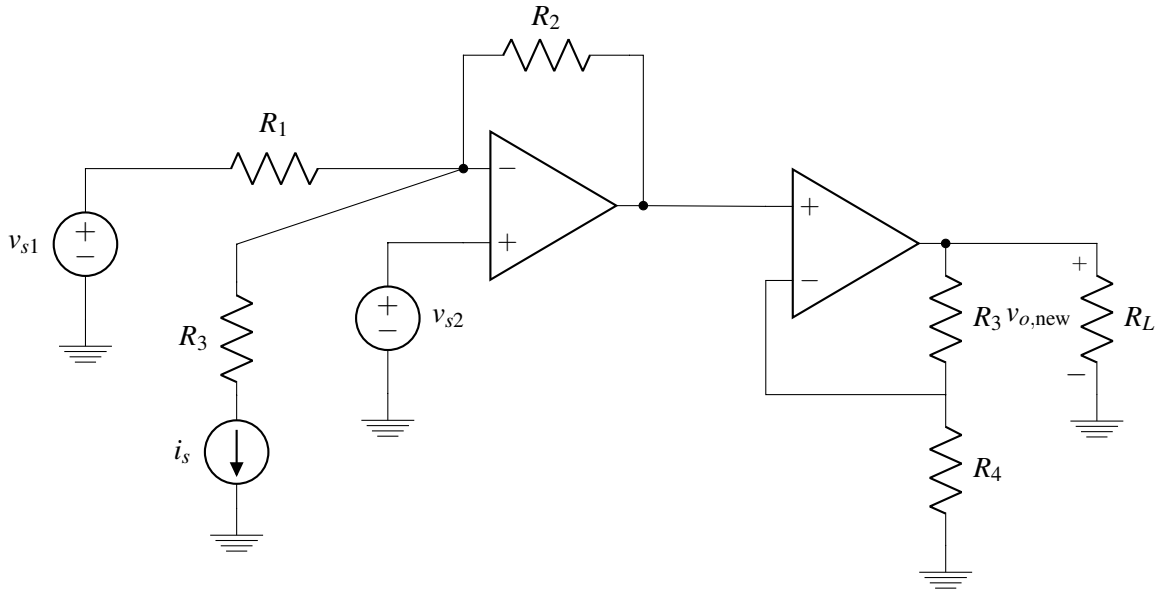
(b) Use the Golden Rules to find v_{o2} for the circuit below.



(c) Use the Golden Rules to find the output voltage v_o for the circuit shown below.

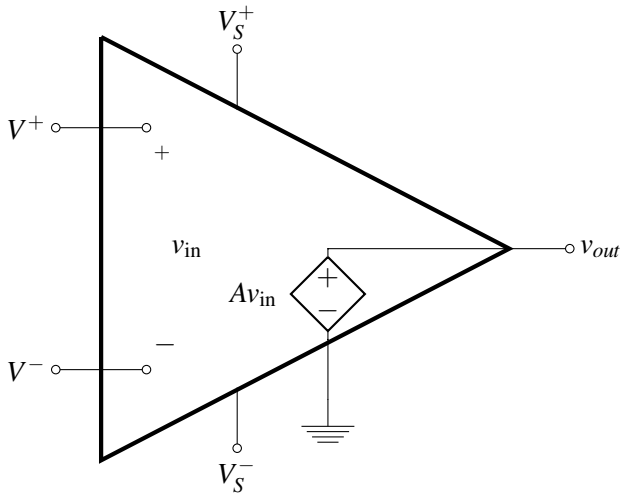


(d) Now add a second stage as shown below. What is $v_{o,\text{new}}$? Does v_o change between part (c) and this part? Does the voltage $v_{o,\text{new}}$ depend on R_L?



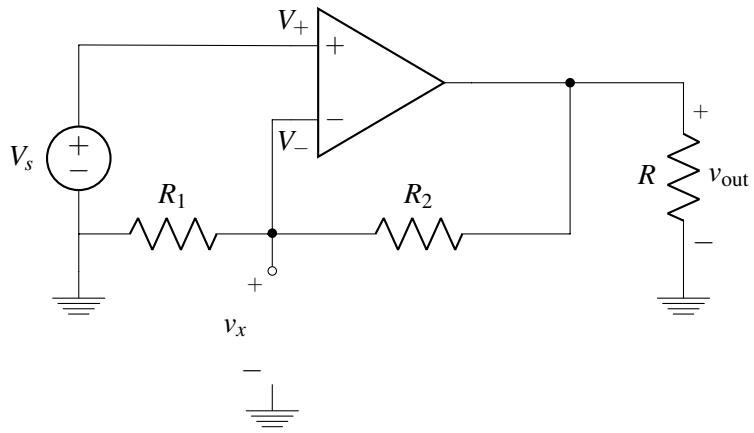
4. Op-Amp Golden Rules

In this question, we are going to show that the Golden Rules for op-amps hold by analyzing equivalent circuits and then taking the limit as the open-loop gain approaches infinity. Below is a picture of the equivalent model of an op-amp we are using for this question.



(a) Now consider the circuit below.

Draw an equivalent circuit by replacing the op-amp with the op-amp model shown above and calculate v_{out} and v_x in terms of A, V_s, R_1, R_2 and R. Is the magnitude of v_x larger or smaller than the magnitude of V_s? Do these values depend on R?

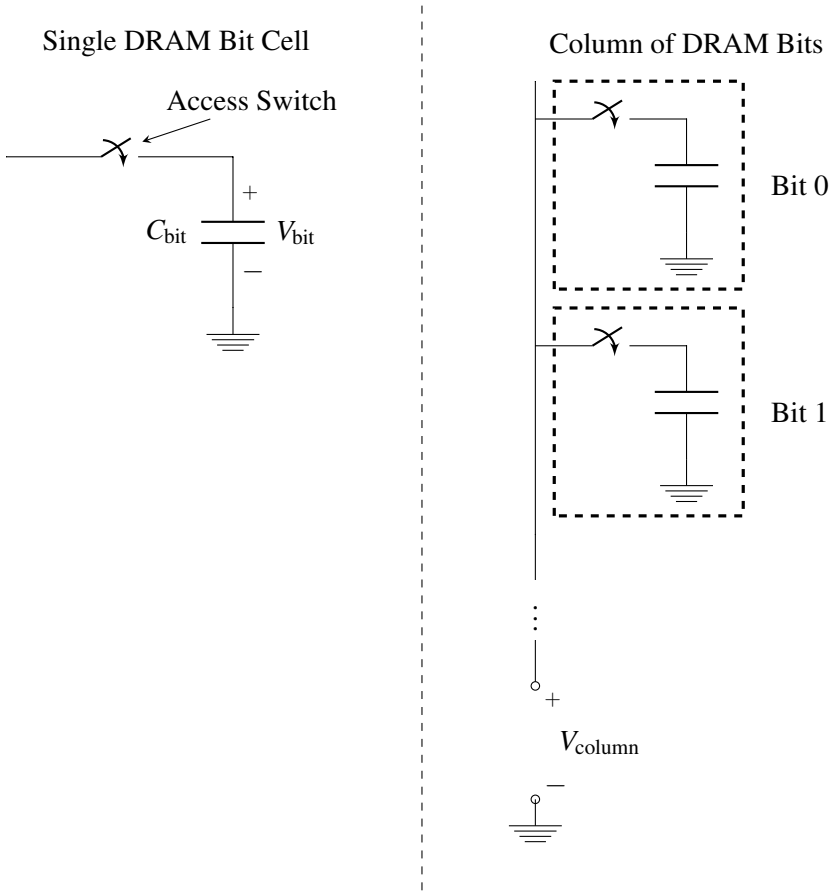


(b) Using your solution to part (a), calculate the limits of v_{out} and v_x as $A \to \infty$. Do you get the same answers if you apply the Golden Rules ($V_+ = V_-$ when there is negative feedback)?

5. Dynamic Random Access Memory (DRAM)

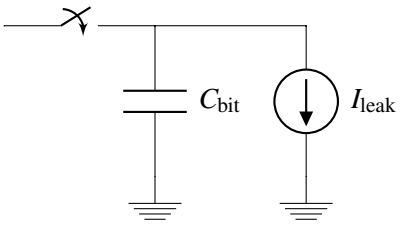
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store > 8 billion bits and is sold for $\approx \$3 - 5$.

At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location. As shown below, in order to pack as many bits together as possible on to a single chip, rather than running a massive number of wires to access every single bit of the DRAM individually, the bits are arranged into a set of columns, where each column uses a single wire to access information from one of the bits. By turning on the access switch within the particular bit cell via the single column wire, the corresponding bit is accessed (while leaving all of the switches in the rest of the cells off).



Building even on only what we've learned about capacitors so far, because of the underlying simplicity of this structure, we can understand a lot about how DRAMs work and are designed. Thus, in this problem we will examine some of the issues and tradeoffs that actual DRAM designers deal with when engineering their products.

(a) In any real capacitor, there is always a path for charge to "leak" off the capacitor and cause it to eventually discharge. In DRAMs, the dominant path for this leakage to happen is through the access switch, but let's ignore this for now and assume that this leakage can be modeled as shown below:



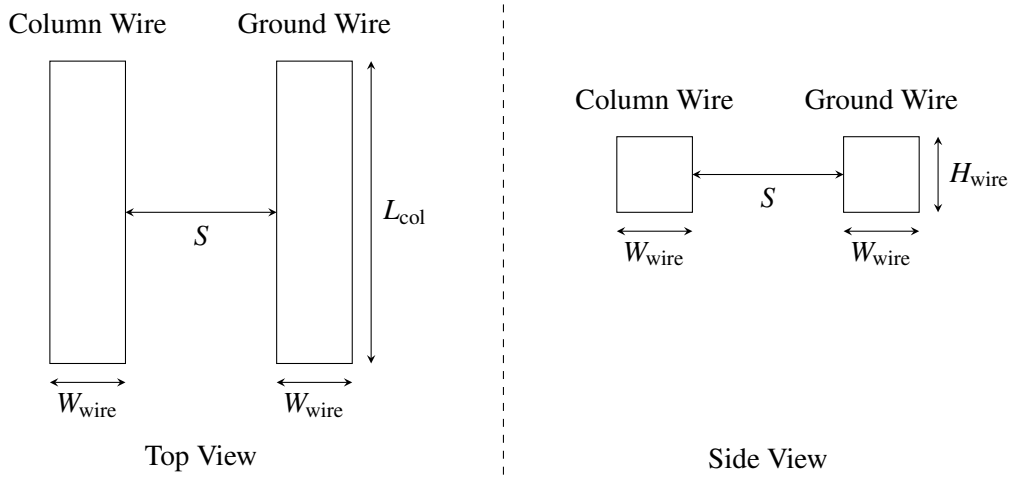
This leakage is actually responsible for the "D" in "DRAM" – the memory is "dynamic" because after a cell is written by storing some charge onto its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 18\,\text{fF}$ (note that $1\,\text{fF} = 1 \times 10^{-15}\,\text{F}$) and the capacitor be initially charged to $1.2\,\text{V}$ to store a "1." V_{bit} must be $> 0.8\,\text{V}$ in order for the circuits outside of the

column to properly read the bit stored in the cell as a "1." What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $> 1\,\text{ms}$?

(b) One of the key decisions a DRAM designer has to make is how many cells to include on a single column. Packing more cells on a single column reduces the total number of wires in the chip, saving some chip space and hence cost (chip cost is strongly related to the physical size of the chip), but as we will see next, making the column too long may stop the DRAM from working properly.

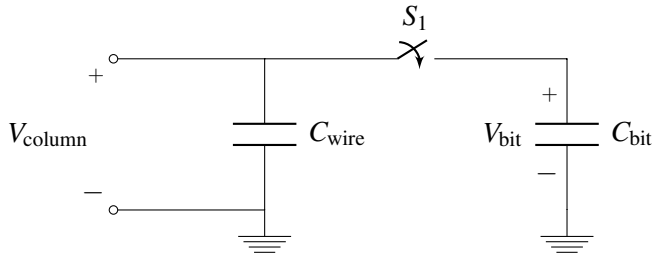
Every time we add another DRAM cell on to the column, the wire that connects all of these cells together must get longer. As shown below, the column wire runs next to another wire that is connected to ground (the same ground that is connected to one side of the capacitors in the DRAM cells). This means that the column wire will have some capacitance to ground.



Let's assume that each DRAM cell that gets added also adds an additional length $0.5\,\mu\text{m}$ (i.e., $0.5 \times 10^{-6}\,\text{m}$) to the column and ground wires. The spacing between the column and ground wires is $S = 0.1\,\mu\text{m}$, and the height of the wire is $H_{\text{wire}} = 0.5\,\mu\text{m}$. If we put 1024 DRAM cells on each column, what is the capacitance between the column wire and the ground wire? Note that you can assume that the two wires are separated by air, but in a real chip, they would be separated by silicon dioxide, but we'll ignore that for this exercise. You should also assume that all of the capacitance is purely parallel plate. Recall that the capacitance of two parallel plates separated by air is $C = \frac{\varepsilon A}{d}$, where A is the area of the plate, d is the perpendicular distance between the two plates, and $\varepsilon = 8.854 \times 10^{-12}\,\frac{\text{F}}{\text{m}}$ is the permittivity of air.

(c) In order to read out the value of an individual cell, we turn on the access switch within that cell to connect the capacitor to the column wire and then read out the resulting voltage on the column wire relative to ground. Note that before this readout operation occurs, the column wire is connected to ground to make sure that it is discharged, i.e. there is no charge on the wire before it is connected to the capacitor.

The situation described above can be modeled using the circuit shown below; note that for simplicity we will ignore the leakage current and its effects from here on out. If $C_{\text{bit}} = 18\,\text{fF}$, $C_{\text{wire}} = 20\,\text{fF}$ (note that this may or may not be your answer to part (b)), and the DRAM cell has a 0 stored in it (i.e., V_{bit} is set to $0\,\text{V}$ before S_1 is turned on), what is V_{column} after switch S_1 is turned on (i.e., makes a connection between the capacitor and column wire)? What will V_{column} be in the case that the DRAM cell has a 1 stored in it, meaning the V_{bit} is set to $1.2\,\text{V}$ before S_1 is turned on?

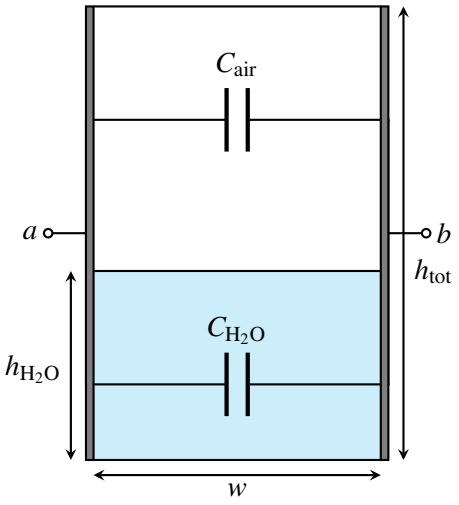


(d) The minimum voltage the readout circuit needs to reliably detect a "1" in a DRAM cell is 0.4 V. Considering that $C_{\text{bit}} = 18\,\text{fF}$ and using the same dimensions provided in part (b) for the wires, what is the maximum number of cells that can be stacked together onto a single DRAM column while still meeting this minimum voltage requirement for the readout?

Note: Real DRAMs do things slightly differently in terms of the voltage they initially set the column wire to, but they use the same basic concept as described above.

6. It's finally raining!

A lettuce farmer in Salinas Valley has grown tired of weather.com's imprecise rain measurements. Therefore, they decided to take matters into their own hands by building a rain sensor. They placed a rectangular tank outside and attached two metal plates to two opposite sides in an effort to make a capacitor whose capacitance varies with the amount of water inside.

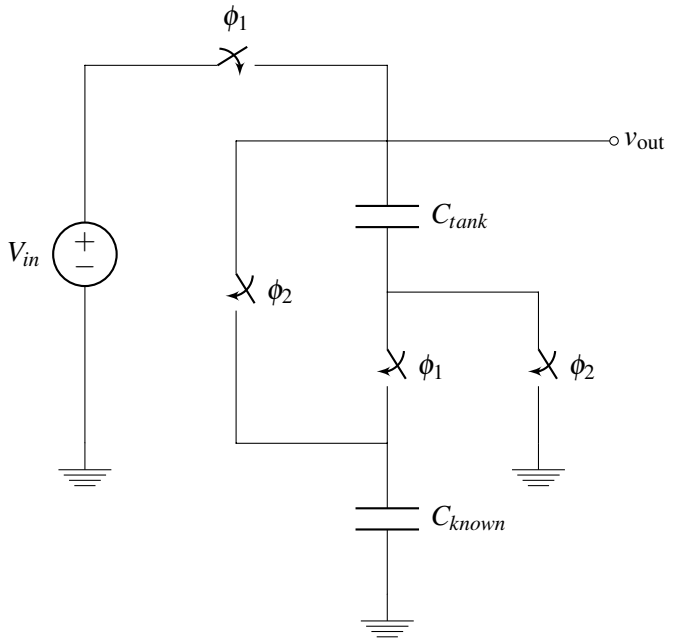


The width and length of the tank are both w (i.e., the base is square) and the height of the tank is h_{tot}.

(a) What is the capacitance between terminals a and b when the tank is full? What about when it is empty?s Note: the permittivity of air is ε, and the permittivity of rainwater is 81ε.

(b) Suppose the height of the water in the tank is h_{H_2O}. Modeling the tank as a pair of capacitors in parallel, find the total capacitance between the two plates. Call this capacitance C_{tank}.

(c) After building this capacitor, the farmer consults the internet to assist them with a capacitance-measuring circuit. A fellow internet user recommends the following:



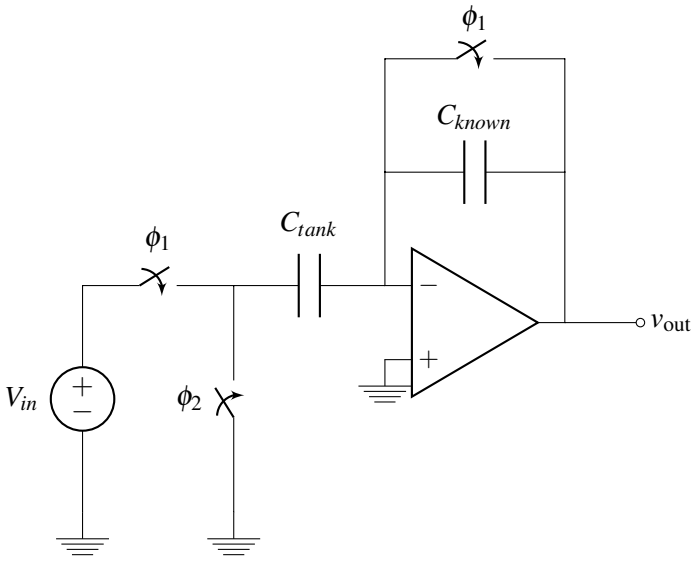
In this circuit, C_{tank} is the total tank capacitance that you calculated earlier. C_{known} is some fixed and known capacitor. Find the voltage v_{out} in phase ϕ_2 as a function of the height of the water. Note that in phase ϕ_1 all switches labeled ϕ_1 are closed and all switches labeled ϕ_2 are open. In phase ϕ_2, all switches labeled ϕ_1 are open and all switches labeled ϕ_2 are closed. You should also assume that before any measurements are taken, the voltages across both C_{known} and C_{tank} are initialized to 0 V.

(d) Use IPython (or any other tool or just do it by hand) to plot this voltage v_{out} as a function of the height of the water. Vary the tank from empty to full. Use values of $V_{\text{in}} = 12\,\text{V}$, $w = 0.5\,\text{m}$, $h_{\text{tot}} = 1\,\text{m}$, and $\varepsilon = 8.854 \times 10^{-12}\,\frac{\text{F}}{\text{m}}$. This ε is called the *permittivity of free space*. For C_{known}, use a similar tank that is known to always be empty.

(e) With the previous part, we were able to derive an expression for v_{out}. What does v_{out} represent? It's something we can measure! Our original goal was to determine what the height of the water in the tank without having to look inside it. Rewrite the last part to solve for h_{water}.

(f) Let's perform a sanity check on our answer. What are the units of your result for v_{out} and for h_{water}?

(g) **PRACTICE:** The farmer has become tired of solving the equation and wishes to generate a voltage proportional to the tank capacitance. A brief consultation with their daughter yields the following circuit:



Calculate v_{out} as a function of $h_{\text{H}_2\text{O}}$ in phase ϕ_2. Use the Golden Rules.

Hint: Think about what must happen to the charge on the capacitor C_{tank} in phase ϕ_2. Where does that charge have to go?

7. Cool For The Summer

You and a friend want to make a box that helps control an air conditioning unit. You both have dials that display a voltage: 0 means you want to leave the temperature as it is. Negative voltages mean that you want to reduce the temperature. (It's hot so we will assume that you never want to increase the temperature – so, we're not talking about a Berkeley summer...)

Your air conditioning unit, however, responds to positive voltages. The higher the magnitude of the voltage, the stronger it runs. At zero, it is off. (If it helps, think of this air-conditioning unit as a heat pump. If you run it with negative voltage, it pumps heat in the opposite direction – from outside to inside. If it reads a positive voltage, it pumps heat from inside to outside.)

Therefore, you need a box that is an inverting summer – it outputs a weighted sum of two voltages where the weights are both negative. The sum is weighted because each of you has your own subjective sense of how much to turn the dial down, so you need to compensate for this.

This problem walks you through this using an op-amp.

(a) As a first step, create a general inverting amplifier and find the voltage gain.

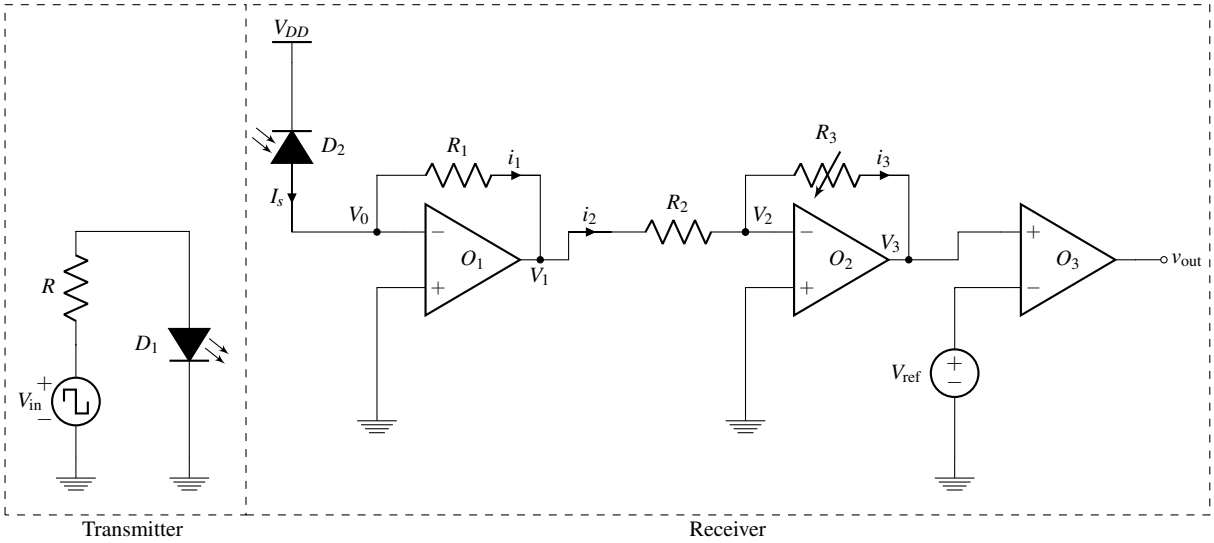
(b) Now add a second input to the amplifier from above. Find the overall voltage gain as a function of the two input voltages.

(c) Let's suppose you want to have the overall voltage gain be $v_{\text{out}} = -\left(\frac{1}{4}V_{S1} + 2V_{S2}\right)$ where V_{S1} and V_{S2} represent the input voltages from you and your friend. Select resistor values such that this is the overall voltage gain.

(d) Now suppose you have another AC unit that you want to add to the same room. This unit however, functions opposite to the already existing unit; it responds to negative voltages. You want to run both units at the same time. Add another simple op-amp circuit to your existing circuit to create an output for the second AC unit.

8. Wireless Communication With An LED

In this question, we are going to analyze the system shown in the figure below. It shows a circuit that can be used as a wireless communication system using visible light (or infrared, very similar to remote controls).



The element D_1 in the transmitter is a light-emitting diode (LED). An LED is an element that emits light and whose brightness is controlled by the current flowing through it. You can recall controlling the light emitted by an LED using your MSP430 in Touchscreen Lab 1. In our circuit, the current across the LED, hence its brightness, can be controlled by choosing the applied voltage V_{in} and the value of the resistor R. In the receiver, the element labeled as D_2 is a reverse biased solar cell. You can recall using an ambient light sensor in Imaging Labs 1 to 3 as a light-controlled current source. We will denote the current supplied by the solar cell by I_{S}. In this circuit, the LED D_1 is used as a means for transmitting information with light, and the reverse-biased solar cell D_2 is used as a light receiver to see if anything was transmitted.

Remark: In Imaging Lab 3, we talked about how non-idealities, such as background light, affect the performance of a system that does light measurements. In this question, we will assume ideal conditions, that is, there is no source of light around except for the LED.

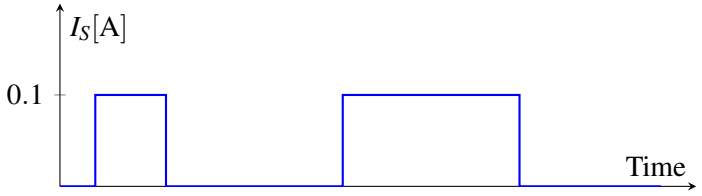
In our system, we define two states for the transmitter: the *transmitter is sending something* when they turn on the LED and the *transmitter is not sending anything* when they turn off the LED. On the receiver side, the goal is to convert the current I_{S} generated by the solar cell into a voltage and amplify it, so that we can read the output voltage V_{out} to see if the transmitter was sending something or not. The circuit implements this operation through a series of op-amps. It might look look complicated at first glance, but we can analyze it one section at a time.

(a) Currents i_1, i_2 and i_3 are labeled on the diagram. Assuming the Golden Rules hold, is $I_{\text{S}} = i_1$? $i_1 = i_2$? $i_2 = i_3$? Treat the solar cell as an ideal current source.

(b) Use the Golden Rules to find V_0, V_1, V_2 and V_3 in terms of I_{S}, R_1, R_2 and R_3.
Hint: Solve for them from left to right, and remember to use the Golden Rules.

(c) In the previous part, how could you check your work to gain confidence that you got the right answer?

(d) Now, assume that the transmitter has chosen the values of V_{in} and R to control the intensity of light emitted by LED, such that when the *transmitter is sending something*, I_S is equal to 0.1 A and when the *transmitter is not sending anything*, I_S is equal to 0 A. The following figure shows a visual example of how this current I_S might look like as time changes (note that this is just to help you visualize the shape of the current supplied by the solar cell).

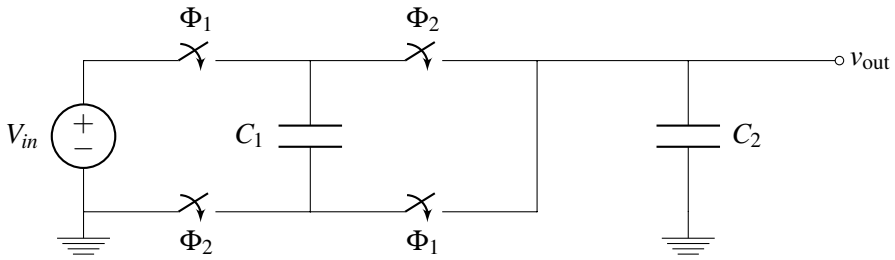


For the receiver, suppose $V_{\text{ref}} = 2\,\text{V}$, $R_1 = 10\,\Omega$, $R_2 = 1000\,\Omega$, and the supply voltages of the op-amps are $V_{\text{DD}} = 5\,\text{V}$ and $V_{\text{SS}} = -5\,\text{V}$. Pick a value of R_3 such that V_{out} is V_{DD} when the *transmitter is sending something* and V_{SS} when the *transmitter is not sending anything*?

(e) In the previous part, how could you check your work to gain confidence that you got the right answer?

9. DC-DC Voltage Divider

One of the reasons for using AC voltages is that we can easily transform the voltage (step up or step down) using transformers. Unfortunately, such circuits do not work at DC and we need to come up with other ways of dividing DC voltages. We have learned about resistive dividers, but we found inefficiencies. An alternative circuit, a capacitive charge pump, is shown below. It relies on two switches that are activated in sequence. First, switch Φ_1 is closed (during this period, Φ_2 switches are open), and then Φ_2 closes and Φ_1 is opened. In practice, this is done periodically, but for this problem, we will analyze each phase separately. Note that V_{in} is a DC voltage.

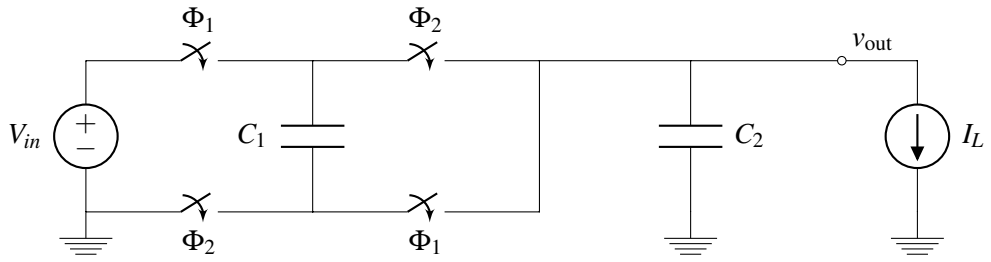


(a) During phase Φ_1, calculate the voltage across and charge stored by each capacitor C_1 and C_2.

(b) During phase Φ_2, calculate the output voltage v_{out} and show that it is a fraction of the input voltage V_{in}.

(c) For the special case of $C_1 = C_2$, calculate the output voltage and the efficiency of the system. To calculate the efficiency, calculate the energy stored in the capacitors at the end of phase Φ_1 and Φ_2.

(d) **PRACTICE:** Assume that this circuit is used with a load represented by the current source $I_L = 10\,\text{mA}$. Suppose that the cycle described above repeats periodically at a rate of 10 kHz, or 10,000 times per second, with each phase Φ_1 and Φ_2 lasting exactly 50% of each cycle. During phase Φ_2, which lasts 50 µs, we want the output voltage to not decrease by more than 5 mV. Specify the capacitances of C_1 and C_2 to satisfy this constraint.



10. Homework Process and Study Group

Who else did you work with on this homework? List names and student ID's. (In case of homework party, you can also just describe the group.) How did you work on this homework?
Working in groups of 3-5 will earn you credit for your participation grade.

11. (PRACTICE) Super-Capacitors

In order to enable small devices for the "Internet of Things" (IoT), many companies and researchers are currently exploring alternative means of storing and delivering electrical power to the electronics within these devices. One example of these are "super-capacitors" - the devices generally behave just like a "normal" capacitor but have been engineered to have extremely high values of capacitance relative to other devices that fit in to the same physical volume.

Your startup named **IoT4eva** is designing a new device that will revolutionize the process of making pizza, and you've been put in charge of selecting an energy source for it. You can't find a battery that quite suits your needs, so you decide to try out some super capacitors in various configurations. The super capacitors will be charged up to a certain voltage in the factory and will then act as the power supply (source of voltage) for the electronics in your device.

(a) Assuming that the electronics in your device can be modeled as drawing a constant current with a value of i_{load}, draw circuit models for your device using the following configurations of super-capacitors as the power supply for the electronics:

- Config 1: a single super-capacitor
- Config 2: two super-capacitors stacked in series
- Config 3: two super-capacitors connected in parallel

(b) If each super-capacitor is charged to an initial voltage v_{init} and has a capacitance of C_{sc}, for each of the three configurations above, write an expression for the voltage supplied to your electronics as a function of time after the device has been activated.

(c) Now let's assume that your electronics require some minimum voltage v_{min} in order to function properly. For each of the three super-capacitor configurations, write an expression you could use to calculate the lifetime of the device.

(d) Assuming that a single super-capacitor doesn't provide you sufficient lifetime and so you have to spend the extra money (and device volume) for another super-capacitor, which configuration would you pick and why would you pick one over the other?

- Config 2: two super-capacitors stacked in series
- Config 3: two super-capacitors connected in parallel