Li Shunyang

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Team-oriented engineer with a proven ability to rapidly learn new tools (e.g., mastered Synopsys Design Compiler in 2 weeks) and deliver high-performance solutions under tight deadlines.

Education

National University of Singapore **Aug 2023 – May 2027**

- *Bachelor of Engineering in Computer Engineering (Hons) specialization in Advanced Electronics*
- Cumulative GPA: 4.93/5.0 (Top 5%)
- Relevant Courses: Computer organization(A+), Digital Design(A), Data structure and algorithm(A), Introduction to Machine learning(A-), VISI digital design

Skills

- **Hardware Development:** Verilog, SystemVerilog (Learning), VHDL, FPGA Optimization (Critical Path Analysis, Pipeline Design, TCL scripting)
- **Low-Latency Systems:** USART Protocol Design, TCP/IP Optimization, Real-Time Signal Processing
- **Programming:** C/C++ (Embedded Systems), Python (Data Analysis, Scripting)
- **Network Protocols:** TCP/IP (port configuration), HTTP/HTTPS, RESTful APIs (Token-based authentication).
- **Languages:** English(Full Professional), Chinese(Native)

Experience

Software Intern *HuaZhong Risk Assessment, China* **Jan 2023 - May 2023**

- Developed a **login and registration portal** using **Token-based authentication (JWT)** to ensure secure access.
- Deployed the system on Alibaba Cloud, configured **TCP/IP ports and firewall rules** to ensure secure communication between distributed engineering teams, reducing latency by **15 percent** through **optimized packet routing**.
- Used **Postman** for API testing, ensuring smooth data exchange between client and server.

Projects

FP8 Floating-Point Adder Design and Optimization| *Verilog, Synopsys* **Dec 2024 – Jan 2025**

- Designed and implemented an **FP8 (8-bit floating-point) adder** in Verilog (RTL) following the IEEE-inspired FP8 (E4M3) format, validated through **256 test cases** using **VCS simulation** and **DVE waveform analysis**.
- Optimized critical paths by replacing a 7-bit shifter with a **priority encoder-based design**, reducing critical path delay to **50ns** and improving throughput by **1.2x** (200MHz → 240MHz) through **5-stage pipeline enhancements**.
- Synthesized the design using **Synopsys Design Compiler**, adhering to **1.5ns clock period** and **0.1ns clock uncertainty constraints**, while analyzing timing violations and area trade-offs.
- Explored pipeline depth variations (3 to 5 stages) to optimize throughput-area balance, achieving **15 percent logic area** reduction with minimal latency penalty.

16-bit RISC CPU Synthesis | *Verilog, Synopsys* **Nov 2024 – D 2025**

- Designed and synthesized the core of **a 16-bit RISC CPU** using Verilog HDL, focusing on the PRGRM_CNT sub-module (program counter) to manage instruction flow with prioritized reset, branch, and return operations.
- Applied **synthesis constraints** (clock period, input/output delays, area limits) via **Synopsys Design Compiler**, optimizing logic mapping to meet a 1.5ns clock period and 200-unit area target using a **GTECH-to-technology library workflow**.
- Automated synthesis flow using **Tcl scripting** (run.tcl), integrating design compilation, constraint application, and report generation to streamline **ASIC design processes**.

FPGA Game Development | *FPGA, Verilog, Vivado* **Mar 2024 – Apr 2024**

- Developed a **Verilog-based Ping Pong game** on **Xilinx Basys3 Boards** under **AMD Artix 7 FPGA architecture**.
- Developed **low-latency USART protocols** (99.9% reliability) for FPGA-based real-time communication, enabling 60 FPS game physics rendering on PMOD OLED.
- **Team Collaboration**: Conducted peer code reviews and iterative testing with 3 developers, resolving signal integrity issues through waveform analysis.

Technical Interests: *Ultra-Low-Latency FPGA Architectures, RISC-V Compute platform*