SSD2825

Advance Information

MIPI Master Bridge

Appendix 1: IC Revision history of SSD2825 Specification

Version	Change Items	Effective Date
0.10	1st Release	23-Feb-11
0.20	1. Modify IO supply from 3.3V to 1.8~3.3V +/-10% 2. Add vsync, hsync and pclk polarity control bit. Command 0xB6 3. Add the lane status bit for clock and data lane. Command 0xC6 4. Add a control bit to flip the TX_LP_CP/TX_LP_CN signal to analog from DSI0 and DSI1. Command 0xDA 5. Add a control bit to invert the BITCLK0/BITCLK1 signal to analog. Command 0xDA 6. Add HED[5:0] bits to control the HS exit period before the next HS transmission. Command 0xDF 7. Change default value of delay parameters, CZD, HZD, CTD, HTD, CPTD 8. Update DC Characteristics	13-May-11
0.30	1. Correct power supply description of feature 2. Modify table 7-4 3. Add remark for command 0xB9, 0xBB 4. Add 10.2.3 ~ 10.2.20 which is related to MIPI detail 5. Modify SHUT pin description 6. Modifiy figure 10-23 and 10-24 7. Modify description of Read, Write and Acknowledgement operation 8. Add decription for 0xFF, 0xB6 [1:0] VPF and 0xD6 [0] CO 9. Add marking and tray information	07-Jul-11
0.40	1. Add information of MCU interface 2. Add Maximum Ratings and Recommended Operating Conditions (12 ~ 13) 3. Add table 10-16 MIPI error report 4. Modify condition of section 15 DC Characteristics	30-Aug-11
1.0	1. Correct typo of “PD” to “PEN” 2. Correct the default value of Register Summary of Command Table	15-Nov-11

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

The SSD2825 IC is an MIPI master bridge chip that connects an application processor with traditional parallel LCD interface and an LCD driver with MIPI slave interface. The SSD2825 supports up to 2 MIPI panels using both parallel RGB, MCU interface and serial SPI interface.

2 FEATURES

- Support 1 or 2 panels 2 independent MIPI links
- Support up to total of 2.4 Gbps over the 2 serial links
- Support up to 4 data lanes for Primary Panel and 2 data lanes for Secondary
- Number of signals is significantly reduced when compare to traditional RGB/MCU transfer
- Support up to 1366 pixels per display row in Video mode
- Reduce power consumption and decrease EMI by using low amplitude signal differential pair for serial data.
- Support parallel VISSI interface (DPI 2.0) up to 24 bits
- Support serial SPI interface (DBI 2.0) up to 16 bits
- Support both command mode and video mode in MIPI DSI standard
- Support 16, 18 and 24 bit per pixel in Raw or Pixel mode for command mode
- Support independent bi-directional data transfer (forward link in High Speed and Power mode and reverse link in Low Power mode) for each DSI
- Support Ultra low power mode in idle state for each DSI
- Support CABC function for Video mode
- On-chip PLL with variable output frequency
- Power supply: (VDDD) 1.2V +/-10%
- IO Power supply: (VDDA and VDDIO) 1.8 ~ 3.3V +/-10%
- Support of MIPI standard DSI(v1.01.00), DCS(v1.02.00), D-PHY (v0.90.00)

2.1 References

- MIPI Alliance Standard for Display Serial Interface, version 1.01
- MIPI Alliance Standard for Display Command Set, version 1.02
- MIPI Alliance Standard for D-PHY, version 0.90
- MIPI Alliance Standard for Display Bus Interface, version 2.0
- MIPI Alliance Standard for Display Pixel Interface, version 2.0

2.2 Definitions

- HS High Speed
- SPI Type C interface option 1 of MIPI Alliance Standard for Display Bus Interface v2.0 (DBI-2)
- LP Low Power
- MCU Type B interface of MIPI Alliance Standard for Display Bus Interface v2.0 (DBI-2)
- ULPS Ultra Low Power State
- RGB MIPI Alliance Standard for Display Pixel Interface v2.0 (DPI-2)
- VC Virtual Channel
- DSI_0 DSI Engine 0 in SSD2825
- DSI_1 DSI Engine 1 in SSD2825

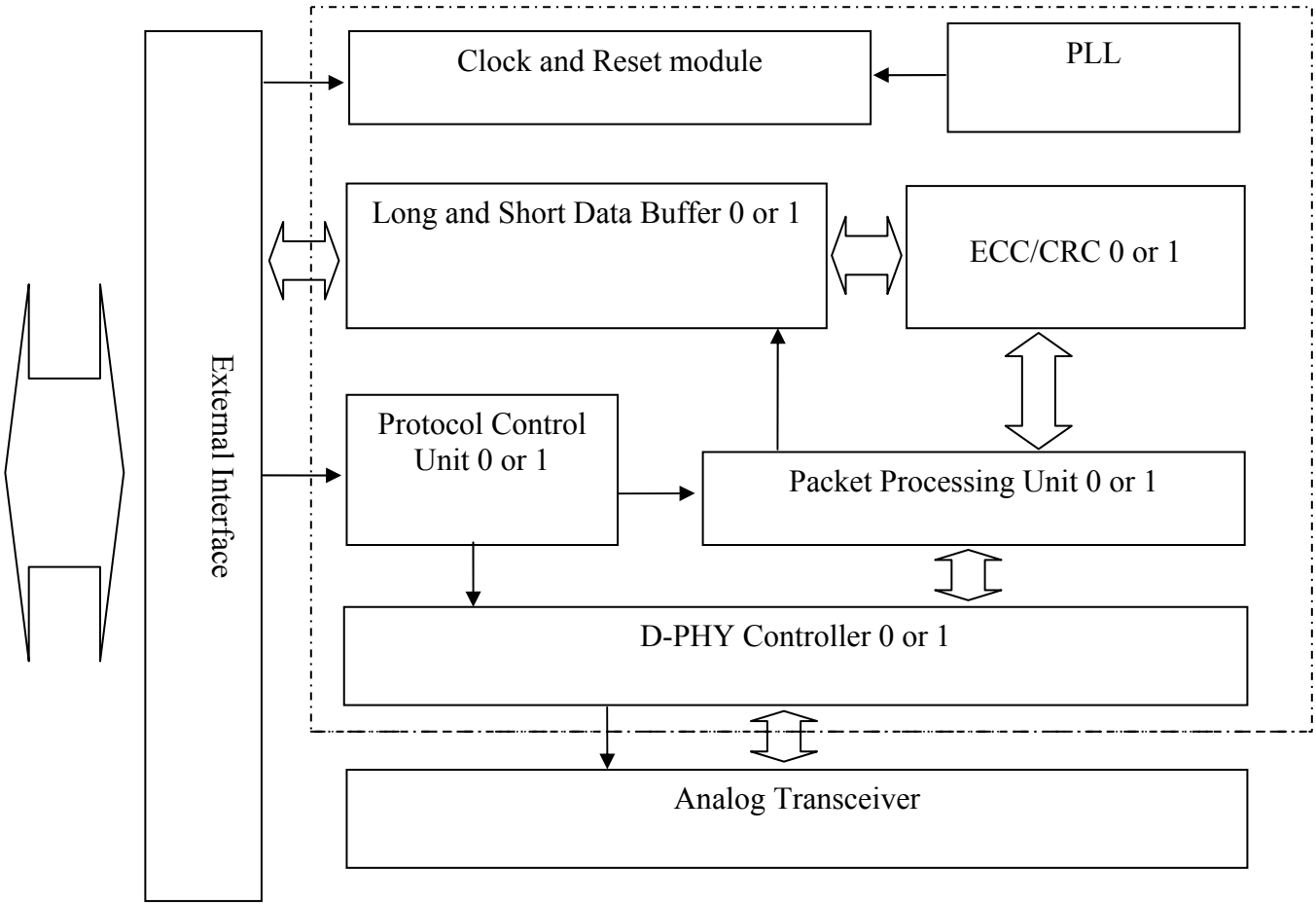
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form
SSD2825QL9	128 LQFP (in Tray form)

4 BLOCK DIAGRAM

Figure 4-1: Block Diagram



5 FUNCTIONAL DESCRIPTION

5.1 Functional Blocks

5.1.1 Clock and Reset Module

The Clock and Reset Module control the generation of the operation clock for the whole system.

5.1.2 External Interface Module

The External Interface Module controls the communication with the host processor. Two types of interface are supported:

- Parallel RGB Interface for dumb display controller. 16 bit, 18 bit and 24 bit data bus width are supported
- Serial SPI interface supports three modes by setting PS1 and PS0:
  - 8 Bit 3 Wire (SCSX, SCK, DIN, DOUT)
  - 8 Bit 4 Wire (SCSX, SCK, SD/C#, DIN, DOUT)
  - 24 Bit 3 Wire (SCSX, SCK, DIN, DOUT)

User can use RGB + SPI interface by setting the IF_SEL and IF_SEL2 pin.

- MUC interface supports six modes by setting PS[4:2]:
  - 8 bit MCU interface (MIPI DBI type B)
  - 16 bit MCU interface (MIPI DBI type B)
  - 8 bit MCU interface (MIPI DBI type A, fixed E or clocked E mode)
  - 16 bit MCU interface (MIPI DBI type A, fixed E or clocked E mode)
  - 24 bit MCU interface (MIPI DBI type B)
  - 24 bit MCU interface (MIPI DBI type A, fixed E or clocked E mode)

5.1.3 Protocol Control Unit (PCU)

The PCU handles outgoing and incoming data stream including:

- Decide the packet type to be sent when an event comes in
- How to react to the received packet.

5.1.4 Packet Processing Unit (PPU)

The PPU is in charge of packet assembly and disassembly. During transmission, the PPU constructs the packet according to the instruction from the PCU. During reception, the PPU extracts information from the incoming packet and pass the information to the PCU.

5.1.5 Error Correction Code / Cyclic Redundancy Check (ECC/CRC)

During transmission, the ECC/CRC module generates ECC or CRC for outgoing bit stream.

During reception, the ECC/CRC module checks the correctness of the ECC and CRC field of the incoming stream.

- If 1 bit error is detected in the data and ECC field, the ECC module will correct the error.
- If more than 1 bit of error is detected in the data and ECC field, the ECC module will report the error.
- If error is detected in the data and CRC field, the CRC module will report the error.

5.1.6 Internal Long and Short Buffer

The internal buffers serve as temporary storage for incoming data from the host processor. After a complete packet is written into the buffer, the SSD2825 will send out the packet.

5.1.7 D-PHY Controller

The D-PHY Controller is in charge of the communication with the Analog Transceiver. During transmission, it receives data from PPU and informs the analog transmitter how to transmit. During reception, it receives data from analog receiver and passes the data to the PPU for further processing. At the same time, it is also performing the handshaking process, such as, bus turn around and switching between different modes.

5.1.8 Analog Transceiver

The Analog Transceiver is front-end for signal communication with MIPI slave. High speed parallel data from D-PHY controller is serialized and transmitted by the high speed transmitter. For control operation, low power transmitter and receiver are used while contention detection is implemented for checking the state conflict.

5.1.9 PLL

The PLL uses either the TX_CLK or the PCLK as reference clock source to generate operating clock for the whole system.

When powering up SSD2825, the PLL is in sleep mode. The system will operate at TX_CLK until PLL is locked.

In HS mode, the PLL output clock is used to generate the clock and data on the MIPI lane. User shall program the PLL such that its output frequency is the same as the data rate required on each data lane.

Refer to SSD2825 Application Note for details in programming the PLL.

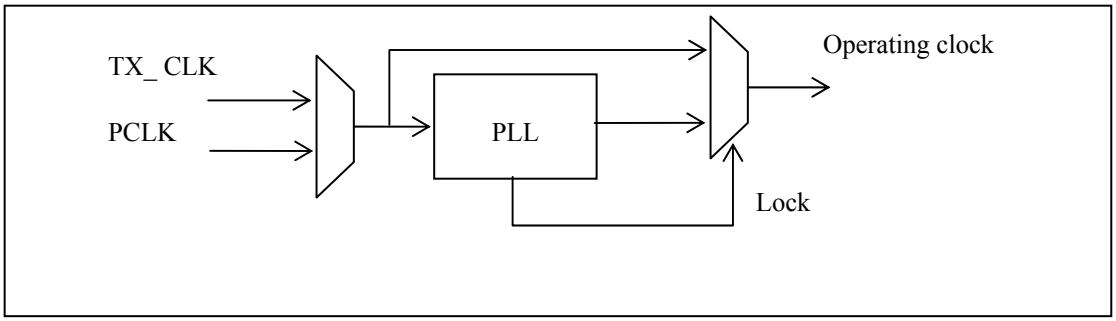


Figure 5-1: SSD2825 Clocking Scheme

5.2 Interface Configuration

The SSD2825 supports two interface configurations:

- RGB + SPI interface.
- MCU interface

Multiple displays can be supported.

5.2.1 RGB + SPI Interface

To select this configuration, the user shall:

- set the IF_SEL pin to low
- select the desired SPI interface by setting PS[1:0]

Below is the interface diagram for the SSD2825 driving 1 MIPI panel. Two types of interface are supported which are RGB and SPI interfaces. The interfaces can be selected through the IF_SEL and PS[1:0] pins.

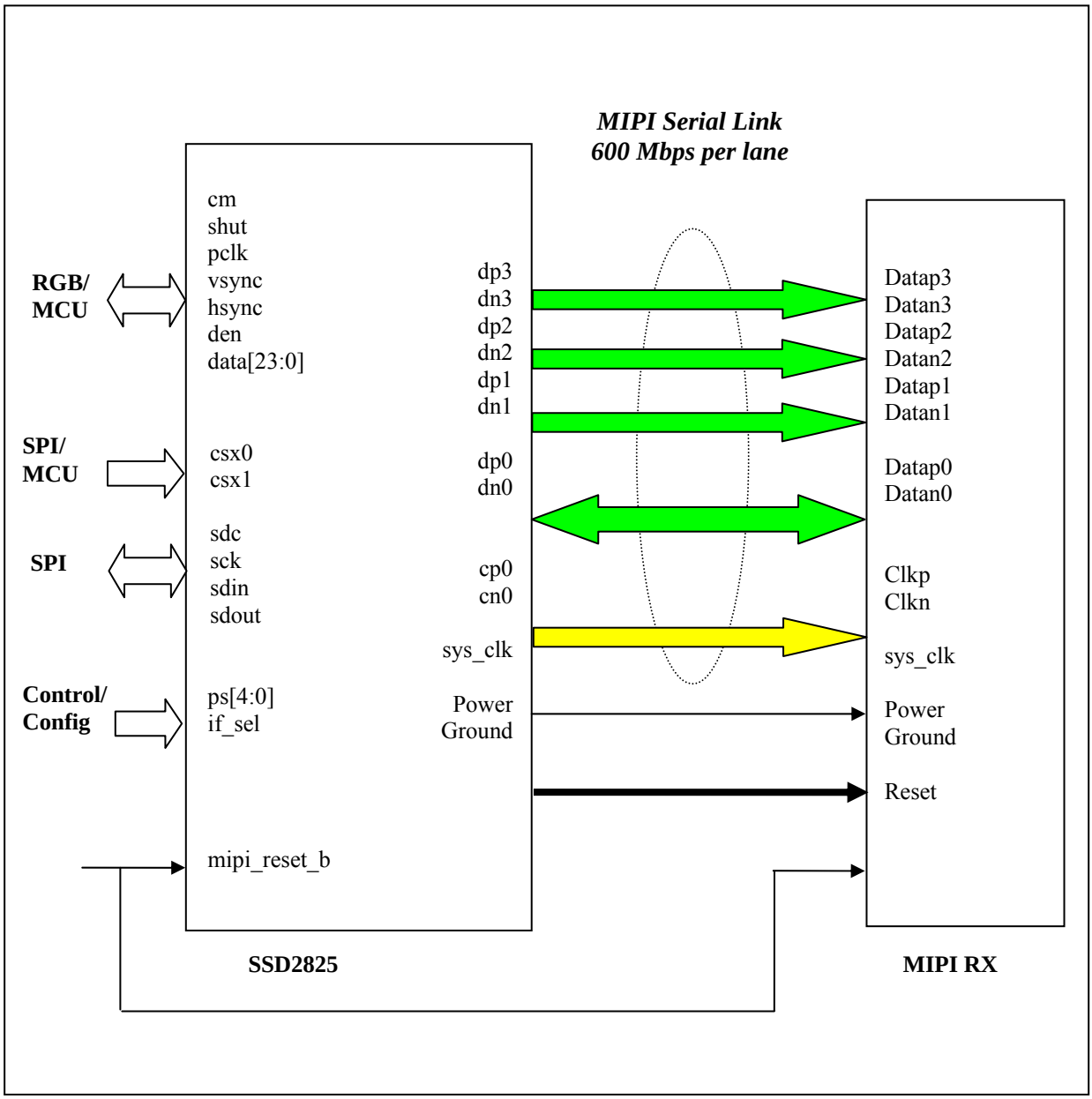


Figure 5-2: SSD2825 with MCU / RGB + SPI Interface

6 SSD2825QL9 Pin Assignment

Table 6-1: SSD2825 Pinout Diagram – 128 LQFP

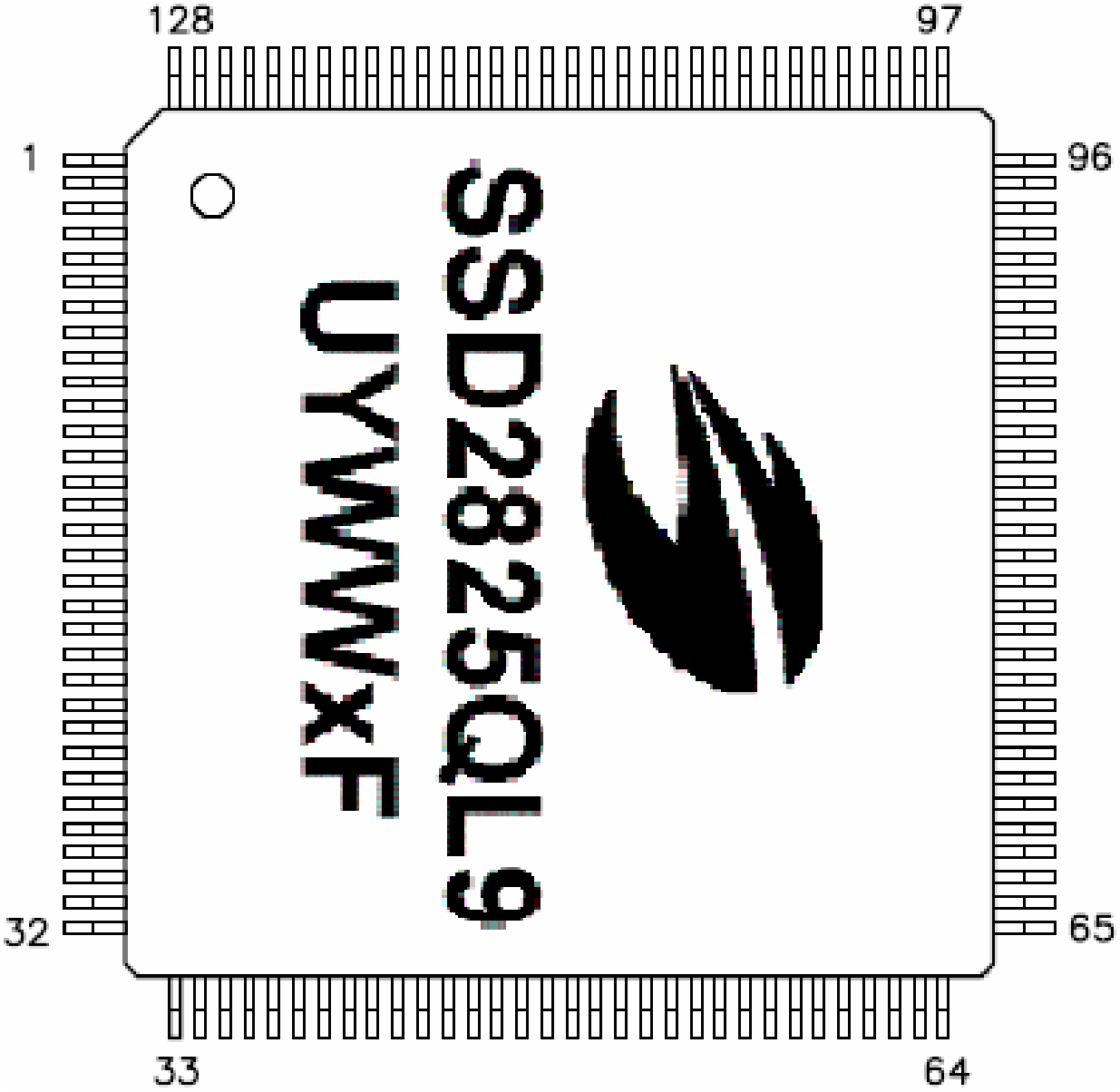


Table 6-2: SSD2825 Pin Assignment

Pad #	Signal	Pad #	Signal
1	NC	65	NC
2	NC	66	VSSIO
3	NC	67	VDD3IO
4	MGNDS	68	VSYNC
5	DATAP0	69	DATA[0]
6	DATAN0	70	DATA[1]
7	MGNDS	71	DATA[2]
8	NC	72	DATA[3]
9	DATAP1	73	DATA[4]
10	DATAN1	74	DATA[5]
11	NC	75	DATA[6]
12	MGNDS	76	DATA[7]
13	CLKP0	77	DATA[8]
14	CLKN0	78	DATA[9]
15	MGNDS	79	DATA[10]
16	NC	80	DATA[11]
17	NC	81	DATA[12]
18	MGNDS	82	DATA[13]
19	DATAP2	83	DATA[14]
20	DATAN2	84	DATA[15]
21	MGNDS	85	DATA[16]
22	NC	86	DATA[17]
23	DATAP3	87	DATA[18]
24	DATAN3	88	DATA[19]
25	NC	89	DATA[20]
26	MGNDS	90	DATA[21]
27	CLKP1	91	DATA[22]
28	CLKN1	92	DATA[23]
29	MGNDS	93	CSX1
30	NC	94	CSX0
31	NC	95	MDVDD
32	NC	96	MDGND
33	NC	97	NC
34	NC	98	NC
35	MAVDD	99	VSSIO
36	MGND	100	VDD3IO
37	MAVDD	101	SYS_CLK_OUT
38	MGND	102	TE_1
39	MAVDD3V	103	TE_0
40	TEST[0]	104	INT_1
41	TEST[1]	105	INT_0
42	TEST[2]	106	VSSIOC
43	PS[0]	107	TX_CLK_XIO
44	PS[1]	108	TX_CLK_XIN
45	PS[2]	109	VDD3IOC
46	PS[3]	110	TX_CLK
47	PS[4]	111	IF_SEL2
48	MIPI_RESET_B	112	IF_SEL
49	MDVDD	113	DBCL
50	VSSIO	114	MDGND
51	VDD3IO	115	MDVDD
52	SDO	116	VCC12A
53	SDI	117	VCC12A
54	SCK	118	GND12A
55	SDC	119	GND12A
56	SHUT	120	MAVDD

57	CM	121	MGND
58	DEN	122	ATC[1]
59	HSYNC	123	ATC[0]
60	PIXEL_CLK	124	TAPAD1
61	MDVDD	125	TAPAD2
62	MDGND	126	MAVDD
63	NC	127	MGND
64	NC	128	NC

7 Pin Description

SSD2825 Pin Function Description

Key:

I = Input
O =Output
I/O = Bi-directional (input/output)
P = Power pin
GND = System VSS

Table 7-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
MGND	P	GND	Ground of Power Supply	Ground for the internal analog circuit and analog interface IO pads	-
MDGND				Ground for the internal digital circuit	-
GND12A				Ground for the PLL	-
VSSIO				Ground for the digital interface IO pads	-
VSIOC					
MGNDS				Ground for the differential signals	-
MAVDD	P	Power supply	Power for Analog Circuits	Power supply for the internal analog circuit. (1.2V +/-10%)	-
MDVDD			Power for Digital Circuits	Power supply for the internal digital circuit. (1.2V +/-10%)	-
VCC12A			Power for PLL Circuits	Power supply for the PLL circuit. (1.2V +/-10%)	-
MAVDD3V			Power for Analog Interface IO	Power supply for the analog interface IO pads. (3.3V +/-10%)	
ATC[1:0]			Power for HS Circuits	Power supply for the high speed circuit. (3.3V +/-10%)	-
VDD3IO			Power for Digital Interface IO	Power supply for the digital interface IO pads (3.3V +/- 10%)	-
VDD3IOC					

Table 7-2: MIPI Pins

Name	Type	Connect to	Function	Description	When not in use
CLKP0	O	MIPI Rx	MIPI Signals	Positive differential clock signal for DSI_0	Open
CLKN0				Negative differential clock signal for DSI_0	
CLKP1				Positive differential clock signal for DSI_1	
CLKN1				Negative differential clock signal for DSI_1	
DATAP0	I/O			Positive differential data signal 0 for DSI_0	
DATAN0				Negative differential data signal 0 for DSI_0	
DATAP1	O			Positive differential data signal 1 for DSI_0	
DATAN1				Negative differential data signal 1 for DSI_0	
DATAP2	I/O			Positive differential data signal 2 for DSI_0 or Positive differential data signal 0 for DSI_1	
DATAN2				Negative differential data signal 2 for DSI_0 or Negative differential data signal 0 for DSI_1	
DATAP3	O			Positive differential data signal 3 for DSI_0 or Positive differential data signal 2 for DSI_0 or Positive differential data signal 1 for DSI_1	
DATAN3				Negative differential data signal 3 for DSI_0 or Negative differential data signal 2 for DSI_0 or Negative differential data signal 1 for DSI_1	

Table 7-3: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
DATA[23:0]	I/O	AP	RGB, MCU Interface	RGB data for RGB interface MCU data for MCU interface	Open
VSYNC / E / WRX	I			- Vsync for RGB interface - E clock signal for MCU interface (This is for MIPI DBI type A interface) - Write enable signal for MCU interface. Enabled when low. (This is for MIPI DBI type B interface)	VDD3IO or GND
PCLK / RWX / RDX				- PCLK for RGB interface - Read/Write selection signal for MCU interface. Read cycle when high, write cycle when low. (This is for MIPI DBI type A interface) - Read enable signal for MCU interface. Enabled when low. (This is for MIPI DBI type B interface.)	VDD3IO or GND
DEN / DCX				- DEN for RGB interface - Data or command signal for MCU interface	VDD3IO or GND
HSYNC				Hsync for RGB interface	VDD3IO or GND
SDC			SPI Interface	Data or command for SPI interface (for 8 bit 4 wire)	VDD3IO or GND
CSX0				Chip select of DSI_0 for SPI interface	VDD3IO
CSX1				Chip select of DSI_1 for SPI interface	VDD3IO
SCK				Serial clock for SPI interface (for 8 bit 3 wire, 8 bit 4 wire, 24 bit 3 wire)	VDD3IO or GND
SDI				Serial data input for SPI interface (for 8 bit 3 wire, 8 bit 4 wire, 24 bit 3 wire)	VDD3IO or GND
SDO	O	-		Serial data output for SPI interface (for 8 bit 3 wire, 8 bit 4 wire, 24 bit 3 wire)	Open

Table 7-4: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
CM	I	VDD3IO or GND	Control Signal	Color mode control signal for RGB interface - 1: 8-color display mode - 0: 16M/262k/64k color display mode	-
SHUT				Shutdown signal of RGB interface (to put the driver into sleep mode) when if_sel is 0. - 1: The panel is shut down - 0: The panel is operating	VDD3IO
IF_SEL				Interface selection signal - 0: A combination of RGB and SPI interface is selected - 1: MCU interface is selected	VDD3IO or GND
IF_SEL2				Interface selection signal for DSI_1 - 0: SPI interface is selected - 1: MCU interface is selected	VDD3IO or GND
PS[4:0]				Interface selection signal PS[1:0] is for SPI interface - 00: 3 wire 24 bit SPI interface - 01: 3 wire 8 bit SPI interface - 10: 4 wire 8 bit SPI interface - 11: No SPI interface PS[4:2] is for the MCU interface When IF_SEL is 1 - 000: 8 bit MCU interface (MIPI DBI type B) - 001: 16 bit MCU interface (MIPI DBI type B) - 010: 8 bit MCU interface (MIPI DBI type A, fixed E or clocked E mode) - 011: 16 bit MCU interface (MIPI DBI type A, fixed E or clocked E mode) - 10x: 24 bit MCU interface (MIPI DBI type B) - 11x: 24 bit MCU interface (MIPI DBI type A, fixed E or clocked E mode)	VDD3IO or GND
TX_CLK		External CLK		TEST[2:0] = 000b. Input system clock. 8 ~ 30MHz TEST[2:0] = 001b. Select input crystal range for the crystal oscillator input. - 0 : 8Mhz to 12Mhz - 1 : 12Mhz to 30Mhz	VDD3IO or GND
TX_CLK_XIN		External CLK		Crystal input. It is only valid during TEST[2:0] = 001b 8 ~ 30MHz	VDD3IO or GND
TX_CLK_XIO	I/O	-		Crystal inout. It is only valid during TEST[2:0] = 001b. In other mode, tie this pin to 1 in other mode.	VDD3IO
SYS_CLK_OUT	O	-		Output system clock for MIPI slave	Open
INT_0	O	-		Output active low interrupt signal from DSI_0	Open
INT_1	O	-		Output active low interrupt signal from DSI_1	Open
TE_0	O	-		Output tearing effect signal from DSI_0	Open
TE_1	O	-		Output tearing effect signal from DSI_1	Open
MIPI_RESET_B	I	VDD3IO or GND		Active low reset signal to the chip	VDD3IO
TEST[2:0]	I	VDD3IO or GND	Test Signals	Test mode selection. Connect to ground for normal mode operation.	GND

TAPAD[2:1]	I/O	VDD3IO or GND		Analog test pad	Open

MCU interface signals are multiplexed differently with the RGB interface signals to save pin count. Moreover, the MCU interface type is controlled by ps[4:2]. The table above shows the multiplexing scheme.

Table 0-1: Multiplexing Scheme for RGB and MCU Interface

Pad Name	**RGB Signals**	**MCU Signals**	
		DBI Type A	**DBI Type B**
PCLK	PCLK	RWX	RDX
VSYNC	VSYNC	E	WRX
DEN	DEN	DCX	DCX
DATA[23:0]	DATA[23:0]	DATA[23:0]	DATA[23:0]

8 COMMAND TABLE

Table 8-1: SSD2825 Register Summary for csx0

Offset	Name	Mnemonic	Reset Value
0xB0	Device Identification Register	DIR	0x2825
0xB1	RGB Interface Control Register 1	VICR1	0x020A
0xB2	RGB Interface Control Register 2	VICR2	0x0214
0xB3	RGB Interface Control Register 3	VICR3	0x0428
0xB4	RGB Interface Control Register 4	VICR4	0x0280
0xB5	RGB Interface Control Register 5	VICR5	0x01E0
0xB6	RGB Interface Control Register 6	VICR6	0x0004
0xB7	Configuration Register 0	CFGR_0	0x0301
0xB8	VC Control Register 0	VCR_0	0x0045
0xB9	PLL Control Register	PCR	0x0000
0xBA	PLL Configuration Register	PLCR	0x8120
0xBB	Clock Control Register 0	CCR_0	0x0003
0xBC	Packet Size Control Register 1 0	PSCR1_0	0x0000
0xBD	Packet Size Control Register 2 0	PSCR2_0	0x0000
0xBE	Packet Size Control Register 3 0	PSCR3_0	0x0100
0xBF	Packet Drop Register 0	PDR_0	0x0000
0xC0	Operation Control Register 0	OCR_0	0x0000
0xC1	Maximum Return Size Register 0	MRSR_0	0x0001
0xC2	Return Data Count Register 0	RDCR_0	0x0000
0xC3	ACK Response Register 0	ARSR_0	0x0000
0xC4	Line Control Register 0	LCR_0	0x0000
0xC5	Interrupt Control Register 0	ICR_0	0x0080
0xC6	Interrupt Status Register 0	ISR_0	0xFF06
0xC7	Error Status Register 0	ESR_0	0x0000
0xC8	Data Format Register 0	DFR_0	0x0000
0xC9	Delay Adjustment Register 1 0	DAR1_0	0x1402
0xCA	Delay Adjustment Register 2 0	DAR2_0	0x2803
0xCB	Delay Adjustment Register 3 0	DAR3_0	0x0416
0xCC	Delay Adjustment Register 4 0	DAR4_0	0x0A0A
0xCD	Delay Adjustment Register 5 0	DAR5_0	0x1000
0xCE	Delay Adjustment Register 6 0	DAR6_0	0x0405
0xCF	HS TX Timer Register 1 0	HTTR1_0	0x0000
0xD0	HS TX Timer Register 2 0	HTTR2_0	0x0010
0xD1	LP RX Timer Register 1 0	LRTR1_0	0x0000
0xD2	LP RX Timer Register 2 0	LRTR2_0	0x0010
0xD3	TE Status Register 0	TSR_0	0x0000
0xD4	SPI Read Register 0	LRR_0	0x00FA
0xD5	PLL Lock Register	PLLR	0x1450
0xD6	Test Register 0	TR_0	0x0005
0xD7	TE Count Register 0	TECR_0	0x0001
0xD8	Analog Control Register 1	ACR1	0x121C
0xD9	Analog Control Register 2	ACR2	0x0000
0xDA	Analog Control Register 3	ACR3	0x0000
0xDB	Analog Control Register 4	ACR4	0x0324
0xDC	Interrupt Output Control Register 0	IOCR_0	0x0000
0xDD	RGB Interface Control Register 7	VICR7	0x0000
0xDE	Lane Configuration Register	LCFR	0x0301
0xDF	Delay Adjustment Register 7	DAR7	0x0010
0xE0	Input Pin Control Register 1	IPCR1	0x5556
0xE1	Input Pin Control Register 2	IPCR2	0x0055

Offset	Name	Mnemonic	Reset Value
0xE2	Bidir Pin Control Register 1	BICR1	0x2AD6
0xE3	Bidir Pin Control Register 2	BICR2	0x414A
0xE4	Bidir Pin Control Register 3	BICR3	0x2110
0xE5	Bidir Pin Control Register 4	BICR4	0x2188
0xE6	Bidir Pin Control Register 5	BICR5	0x210C
0xE7	Bidir Pin Control Register 6	BICR6	0x2114
0xE8	Bidir Pin Control Register 7	BICR7	0x2948
0xE9	CABC Brightness Control Register 1	CBCR1	0x0000
0xEA	CABC Brightness Control Register 2	CBCR2	0x6900
0xEB	CABC Brightness Status Register	CBSR	0x0000
0xFF	Read Register 0	RR_0	0x0000

Note : (*) – Only 1 physical register is available by 2 chip selects(csx0 and csx1)

Table 8-2: SSD2825 Register Summary for csx1

Offset	Name	Mnemonic	Reset Value
0xB0	Device Identification Register	DIR	0x2825
0xB1	RGB Interface Control Register 1	VICR1	0x020A
0xB2	RGB Interface Control Register 2	VICR2	0x0214
0xB3	RGB Interface Control Register 3	VICR3	0x0428
0xB4	RGB Interface Control Register 4	VICR4	0x0280
0xB5	RGB Interface Control Register 5	VICR5	0x01E0
0xB6	RGB Interface Control Register 6	VICR6	0x0004
0xB7	Configuration Register 0	CFGR_0	0x0301
0xB8	VC Control Register 0	VCR_0	0x0045
0xB9	PLL Control Register	PCR	0x0000
0xBA	PLL Configuration Register	PLCR	0x8120
0xBB	Clock Control Register 0	CCR_0	0x0003
0xBC	Packet Size Control Register 1 0	PSCR1_0	0x0000
0xBD	Packet Size Control Register 2 0	PSCR2_0	0x0000
0xBE	Packet Size Control Register 3 0	PSCR3_0	0x0100
0xBF	Packet Drop Register 0	PDR_0	0x0000
0xC0	Operation Control Register 0	OCR_0	0x0000
0xC1	Maximum Return Size Register 0	MRSR_0	0x0001
0xC2	Return Data Count Register 0	RDCR_0	0x0000
0xC3	ACK Response Register 0	ARSR_0	0x0000
0xC4	Line Control Register 0	LCR_0	0x0000
0xC5	Interrupt Control Register 0	ICR_0	0x0080
0xC6	Interrupt Status Register 0	ISR_0	0xFF06
0xC7	Error Status Register 0	ESR_0	0x0000
0xC8	Data Format Register 0	DFR_0	0x0000
0xC9	Delay Adjustment Register 1 0	DAR1_0	0x1402
0xCA	Delay Adjustment Register 2 0	DAR2_0	0x2803
0xCB	Delay Adjustment Register 3 0	DAR3_0	0x0416
0xCC	Delay Adjustment Register 4 0	DAR4_0	0x0A0A
0xCD	Delay Adjustment Register 5 0	DAR5_0	0x1000
0xCE	Delay Adjustment Register 6 0	DAR6_0	0x0405
0xCF	HS TX Timer Register 1 0	HTTR1_0	0x0000
0xD0	HS TX Timer Register 2 0	HTTR2_0	0x0010
0xD1	LP RX Timer Register 1 0	LRTR1_0	0x0000
0xD2	LP RX Timer Register 2 0	LRTR2_0	0x0010
0xD3	TE Status Register 0	TSR_0	0x0000
0xD4	SPI Read Register 0	LRR_0	0x00FA
0xD5	PLL Lock Register	PLLR	0x1450
0xD6	Test Register 0	TR_0	0x0005
0xD7	TE Count Register 0	TECR_0	0x0001
0xD8	Analog Control Register 1	ACR1	0x121C
0xD9	Analog Control Register 2	ACR2	0x0000
0xDA	Analog Control Register 3	ACR3	0x0000
0xDB	Analog Control Register 4	ACR4	0x0324
0xDC	Interrupt Output Control Register 0	IOCR_0	0x0000
0xDD	RGB Interface Control Register 7	VICR7	0x0000
0xDE	Lane Configuration Register	LCFR	0x0301
0xDF	Delay Adjustment Register 7	DAR7	0x0010
0xE0	Input Pin Control Register 1	IPCR1	0x5556
0xE1	Input Pin Control Register 2	IPCR2	0x0055
0xE2	Bidir Pin Control Register 1	BICR1	0x2AD6
0xE3	Bidir Pin Control Register 2	BICR2	0x414A
0xE4	Bidir Pin Control Register 3	BICR3	0x2110

Offset	Name	Mnemonic	Reset Value
0xE5	Bidir Pin Control Register 4	BICR4	0x2188
0xE6	Bidir Pin Control Register 5	BICR5	0x210C
0xE7	Bidir Pin Control Register 6	BICR6	0x2114
0xE8	Bidir Pin Control Register 7	BICR7	0x2948
0xE9	CABC Brightness Control Register 1	CBCR1	0x0000
0xEA	CABC Brightness Control Register 2	CBCR2	0x6900
0xEB	CABC Brightness Status Register	CBSR	0x0000
0xFF	Read Register 0	RR_0	0x0000

Note : (*) – Only 1 physical register is available by 2 chip selects(csx0 and csx1)

9 COMMAND DESCRIPTION

9.1 Device Identification Register

Offset Address

DIR **Device Identification Register** **0xB0**

BIT	15	14	13	12	11	10	9	8
NAME	**DIR[15:8]**							
TYPE	RO							
RESET	**0x28**							
BIT	7	6	5	4	3	2	1	0
NAME	**DIR[7:0]**							
TYPE	RO							
RESET	**0x25**							

Table 9-1: Device Identification Register Description

Name	Description	Setting
DIR Bit 15-0	**Device Identification Number**	0x2825

9.2 RGB Interface Control Register 1

Offset Address

VICR1 **RGB Interface Control Register 1** **0xB1(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**VSA**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HSA**							
TYPE	RW							
RESET	0x0A							

Table 9-2: RGB Interface Control Register 1 Description

Name	Description	Setting
VSA Bit 15-8	**Vertical Sync Active Period** – These bits specify the Vsync active period. The Vsync active period is from the Vsync falling edge to rising edge, in terms of Hsync pulses. It is only used in non-burst mode with Sync pulses.	The minimum value is 1.
HSA Bit 7-0	**Horizontal Sync Active Period** – These bits specify the Hsync active period. The Hsync active period is from the Hsync falling edge to rising edge, in terms of pclk. It is only used in non-burst mode with Sync pulses.	The minimum value is 1.

9.3 RGB Interface Control Register 2

Offset Address

VICR2 **RGB Interface Control Register 2** **0xB2(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**VBP**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HBP**							
TYPE	RW							
RESET	0x14							

Table 9-3: RGB Interface Control Register 2 Description

Name	Description	Setting
VBP Bit 15-8	**Vertical Back Porch Period** – These bits specify the vertical back porch period in terms of Hsync pulses. The vertical back porch period depends on the video mode setting. If the mode is non-burst mode with Sync pulses, it is from the Vsync rising edge to the Hsync of the first line of active display. If the mode is non-burst mode with Sync events, it is from the Vsync falling edge to the Hsync of the first line of active display. If the mode is burst mode, it is the same as the non-burst mode with Sync events.	
HBP Bit 7-0	**Horizontal Back Porch Period** – These bits specify the horizontal back porch period in terms of pclk. The horizontal back porch period depends on the non-burst mode setting. If the mode is non-burst mode with Sync pulses, it is from the Hsync rising edge to the start of the valid display pixel. If the mode is non-burst mode with Sync events, it is from the Hsync falling edge to the start of the valid display pixel. If the mode is burst mode, it is the same as the non-burst mode with Sync events.	

9.4 RGB Interface Control Register 3

Offset Address

VICR3 **RGB Interface Control Register3** **0xB3(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**VFP**							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	**HFP**							
TYPE	RW							
RESET	0x28							

Table 9-4: RGB Interface Control Register 3 Description

Name	Description	Setting
VFP Bit 15-8	**Vertical Front Porch Period** – These bits specify the vertical front porch period in terms of Hsync pulses. The vertical front porch period is from the first Hsync after the last line of active display to the next Vsync falling edge.	
HFP Bit 7-0	**Horizontal Front Porch Period** – These bits specify the horizontal front porch period in terms of pclk. The horizontal front porch period is from the end of the valid display pixel to the next Hsync falling edge.	

9.5 RGB Interface Control Register 4

Offset Address

VICR4 **RGB Interface Control Register 4** **0xB4(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**HACT[15:8]**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HACT[7:0]**							
TYPE	RW							
RESET	0x80							

Table 9-5: RGB Interface Control Register 4 Description

Name	Description	Setting
HACT Bit 15-0	**Horizontal Active Period** – These bits specify the horizontal active period in terms of pclk. During the horizontal active period, the den signal should always be high.	The minimum value is 1.

9.6 RGB Interface Control Register 5

Offset Address

VICR5 **RGB Interface Control Register 5** **0xB5(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**VACT[15:8]**							
TYPE	RW							
RESET	0x01							
BIT	7	6	5	4	3	2	1	0
NAME	**VACT[7:0]**							
TYPE	RW							
RESET	0xE0							

Table 9-6: RGB Interface Control Register 5 Description

Name	Description	Setting
VACT Bit 15-0	**Vertical Active Period** – These bits specify the vertical active period in terms of Hsync pulses.	The minimum value is 1.

9.7 RGB Interface Control Register 6

Offset Address

VICR6 **RGB Interface Control Register6** **0xB6(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**VS_P**	**HS_P**	**PCLK_P**					**CBM**
TYPE	RW	RW	RW	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**NVB**	**NVD**	**BLLP**	**VCS**	**VM**		**VPF**	
TYPE	RW	RW	RW	RW	RW		RW	
RESET	0x0	0x0	0x0	0x0	0x1		0x0	

Table 9-7: RGB Interface Control Register 6 Description

Name	Description	Setting
VS_P Bit 15	**VS_P** – This bit control the polarity of the Vsync pulse input.	0 – Vsync Pulse is active low 1 – Vsync Pulse is active high
HS_P Bit 14	**HS_P** – This bit control the polarity of the Hsync pulse output.	0 – Hsync Pulse is active low 1 – Hsync Pulse is active high
PCLK_P Bit 13	**PCLK_P** – This bit control the polarity of the CM output.	0 – Data is launch at falling edge, SSD2825 latch data at rising edge 1 – Data is launch at rising edge, SSD2825 latch data at falling edge
Reserved Bit 12-9		
CBM **Bit 8**	**Compress Burst Mode Control –** If the mode is burst and this bit is 1, MIPITX will send video packet in compressed burst mode (i.e. no blanking packet after horizontal sync packet)	0 – Video with blanking packet. 1 – Video with no blanking packet.
NVB **Bit 7**	**Non Video Data Burst Mode Control –** This bit specifies how non video data will be interleaved with video data transmission in burst mode.	0 – Non video data will be transmitted during any BLLP period. 1 – Non video data will only be transmitted during vertical blanking period.
NVD Bit 6	**Non Video Data Transmission Control –**This bit specifies how non video data will be interleaved with video data transmission. The SSD2825 will send non video data (written from the SPI interface) during the vertical blanking period (non burst mode) or any **BLLP** period in burst mode (depends on **NVB** setting). The data can be sent either in high speed mode or low power mode. This bit selects which mode to use. If LP mode is selected, the data lane will enter LP mode for **BLLP** period, even	0 – Non video data will be transmitted using HS mode. 1 – Non video data will be transmitted using LP mode.

Name	Description	Setting
	if there is no non-video data to send. Please note that sending data in LP mode is much slower than HS mode. It is the responsibility of the host processor to make sure that the duration is long enough to finish the data transfer and the timing of Hsync and Vsync is not affected.	
BLLP Bit 5	**BLLP Control –** This bit specifies the SSD2825 operation during BLLP period. This bit takes effect only for non burst mode and **NVD** being 0. When the video mode is burst mode, the SSD2825 will not send any blanking packet during BLLP. It will enter LP mode. When **NVD** is 1 in non burst mode, the SSD2825 will stay in LP mode after sending the non video data (if there is any), until the BLLP period ends. When **NVD** is 0 in non burst mode, the SSD2825 will use this bit to decide whether to send blanking packet or enter LP mode after sending non video data (if there is any), until the **BLLP** period ends. Please note that entering and exiting from LP mode needs more time, as the speed of LP mode is slow. It is the responsibility of the host processor to make sure that the period is long enough to finish the data transfer and the timing of Hsync and Vsync is not affected.	0 – Blanking packet will be sent during BLLP period. 1 – LP mode will be used during BLLP period.
VCS Bit 4	**Video Clock Suspend –** This bit specifies the clock lane behavior. This bit is only applicable for burst mode. When the video mode is non burst mode, the clock lane will remain in HS mode all the time.	0 – The clock lane remains in HS mode, when there is no data to transmit. 1 – The clock lane enters LP mode when there is no data to transmit.
VM Bit 3-2	**Video Mode –** These bits specify the video mode the SSD2825 will use, when RGB interface is selected. Please refer to MIPI DSI for the definition of different modes.	00 – Non burst mode with sync pulses 01 – Non burst mode with sync events 10 – Burst mode 11 – Reserved
VPF Bit 1-0	**Video Pixel Format** – These bits specify the pixel format for video mode.	00 – 16bpp 01 – 18bpp, packed 10 – 18bpp, loosely packed 11 – 24bpp

24bpp	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18bpp	**X**	**X**	**X**	**X**	**X**	**X**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16bpp	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

9.8 RGB Interface Control Register 7

Offset Address

VICR7 **RGB Interface Control Register7** **0xDD(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**VBN**				**VFN**			
TYPE	RW				RW			
RESET	0x00				0x00			

Table 9-8: RGB Interface Control Register 7 Description

Name	Description	Setting
Reserved Bit 15-8		
VBN Bit 7-4	**Vertical Front Porch Non Video Data Window** These fields specify the number of vertical back porch counting backward from the first vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when **VEN** is 1 and the interface setting is RGB + SPI(if_sel = 0). This field should not larger than VBP. If it is larger, the internal logic will cap this field to VBP.	
VFN Bit 3-0	**Vertical Back Porch Non Video Data Window** These fields specify the number of vertical front porch from the last vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when **VEN** is 1 and the interface setting is RGB + SPI(if_sel = 0). This field should not larger than VFP. If it is larger, the internal logic will cap this field to VFP.	

Note: Setting VBN ≥ VBP and VFN ≥ VFP at the same time will cause non-video data not being sent out through MIPI link when the video mode is non-burst mode or burst mode with **NVB** = 1.

9.9 Configuration Register 0/1

Offset Address

CFGR_0 **Configuration Register 0** **0xB7(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME						**LPE**	**EOT**	**ECD**
TYPE	RO	RO	RO	RO	RO	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**REN**	**DCS**	**CSS**	**HCLK**	**VEN**	**SLP**	**CKE**	**HS**
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x1

CFGR_1 **Configuration Register 1** **0xB7(csx1)**

BIT	15	14	13	12	11	10	9	8
NAME						**LPE**	**EOT**	**ECD**
TYPE	RO	RO	RO	RO	RO	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**REN**	**DCS**		**HCLK**		**SLP**	**CKE**	**HS**
TYPE	RW	RW	RO	RW	RO	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x1

Table 9-9: Configuration Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-11		
LPE Bit 10	**Long Packet Enable –** This bit specifies whether the SSD2825 will send out a Generic Long Write Packet or Generic Short Write Packet when the payload is no more than 2 bytes. It also specifies whether the SSD2825 will send out a DCS Long Write Packet or DCS Short Write Packet when the payload is no more than 1 byte.	0 – Short Packet 1 – Long Packet
EOT Bit 9	**EOT Packet Enable –** This bit specifies whether the SSD2825 will send out the EOT packet at the end of HS transmission or not.	0 – Do not send 1 – Send
ECD Bit 8	**ECC CRC Check Disable –** This bit specifies whether SSD2825 will perform ECC and CRC checking for the packets received from the MIPI slave.	0 – Enable 1 – Disable
REN Bit 7	**Read Enable –**This bit specifies whether the next operation is a write or read operation.	0 – Write operation 1 – Read operation
DCS Bit 6	**DCS Enable –** This bit specifies whether the packet to be sent is DCS packet or generic	0 – Generic packet (The packet can be any one of Generic Long

Name	Description	Setting
	packet. This bit applies for both write and read operation.	Write, Generic Short Write, Generic Read packet, depending on the configuration.) 1 – DCS packet (The packet can be any one of DCS Long Write, DCS Short Write, DCS Read packet, depending on the configuration.)
CSS Bit 5	**Clock Source Select –** This bit selects the clock source for the PLL. This bit is only valid for csx0. The **CSS** setting should be programmed only when **PEN** is 1. It has no effect when **PEN** is 0.	0 – The clock source is tx_clk 1 – The clock source is pclk
HCLK Bit 4	**HS Clock Disable –** This bit controls the clock lane behavior during the reverse direction communication. This bit takes effect only when **CKE** is 0 and **VEN** is 0.	0 – HS clock is enabled 1 – HS clock is disabled
VEN Bit 3	**Video Mode Enable** – This bit controls the video mode operation. Only after this bit is set to 1, video mode is enabled. This bit takes effect only when the interface setting is RGB + SPI. This bit is only valid for csx0	0 – Video mode is disabled 1 – Video mode is enabled
SLP Bit 2	**Sleep Mode Enable –** This bit controls the sleep mode operation. When this bit is set to 1, the **HS** bit will be cleared to 0 automatically.	0 – Sleep mode is disabled 1 – Sleep mode is enabled. Only the register interface is active.
CKE Bit 1	**Clock Lane Enable –** This bit controls the clock lane mode when data lane enters LP mode.	0 – Clock lane will enter LP mode, if it is not in reverse direction communication. Clock lane will follow the setting of **HCLK**, if it is in reverse direction communication. 1 – Clock lane will enter HS mode for all the cases.
HS Bit 0	**HS Mode –** This bit controls whether the SSD2825 is using HS or LP mode to send data. This bit can be affected by the **SLP** bit value.	0 – LP mode 1 – HS mode

9.10 VC Control Register 0/1

Offset Address

VCR_0/VCR_1 **VC Control Register 0/1** **0xB8(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**VCM**		**VCE**		**VC2**		**VC1**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x0		0x1		0x1	

Table 9-10: VC Control Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-8		
VCM Bit 7-6	**Virtual Channel ID for Maximum Return Size Packet –** These bits specify the VC ID for the Maximum Return Size Packet sent by SSD2825. This register field is included as the VC ID for this packet might be different from the VC ID for the packets carrying the actual data.	
VCE Bit 5-4	**Virtual Channel ID for EOT Packet –** These bits specify the VC ID for the EOT Packet sent by SSD2825. This register field is included as the VC ID for this packet might be different from the VC ID for the packets carrying the actual data.	
VC2 Bit 3-2	**Virtual Channel ID for SPI Interface –** These bits specify the VC ID for the packets written in through the SPI interface, when the interface setting is RGB + SPI(if_sel = 0). This register field is included as the RGB + SPI interface can address two different LCD panels at the same time. The VC ID for the two panels are different.	
VC1 Bit 1-0	**Virtual Channel ID for RGB Interface –** These bits specify the VC ID for the packets written in through the RGB interface, when the interface is RGB + SPI(if_sel = 0). This register field is included as the RGB + SPI interfaces can address two different LCD panels at the same time. The VC ID for the two panels is different.	

9.11 PLL Control Register

Offset Address

PCR **PLL Control Register** **0xB9**

BIT	15	14	13	12	11	10	9	8
NAME	**SYSD**							
TYPE	RW		RO	RO	RO	RO	RO	RO
RESET	0x0		0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**PEN**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 9-11: PLL Control Register Description

Name	Description	Setting
SYSD Bit 15-14	**SYS_clk Divider** – These bits give the divider value for generating the sys_clk from the tx_clk or crystal input.	00 – Divide by 1 01 – Divide by 2 10 – Divide by 4 11 – Divide by 8
Reserved Bit 13-1		
PEN Bit 0	**PLL Enable** – This bit controls the PLL operation.	0 – PLL power down 1 – PLL enable

Remark: Frequency of PLL can only be changed during PEN = 0

9.12 PLL Configuration Register

Offset Address

PLCR **PLL Configuration Register** **0xBA**

BIT	15	14	13	12	11	10	9	8
NAME	**FR**			**MS**				
TYPE	RW		RO	RW				
RESET	0x2		0x0	0x01				
BIT	7	6	5	4	3	2	1	0
NAME	**NS**							
TYPE	RW							
RESET	0x20							

Table 9-12: PLL Configuration Register Description

Name	Description	Setting
FR Bit 15-14	**Frequency Range –** These bits select the range of the output clock. The **FR** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1.	00 – 62.5 < f_{OUT} < 125 01 – 126 < f_{OUT} < 250 10 – 251 < f_{OUT} < 500 11 – 501 < f_{OUT} < 1000
Reserved Bit 13		
MS Bit 12-8	**PLL Divider –** These bits specify the PLL pre-divider value, **MS**. The frequency of the phase detector, f_{REF} is determined by $f_{PRE} = f_{IN} / MS$ The input frequency, f_{IN} and phase detector frequency, f_{REF} should be between 5Mhz to 100Mhz. The **MS** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1.	- 0x00 : MS=1 - 0x01 : MS=1 - 0x02 : MS=2 … - 0x1F : MS=31
NS Bit 7-0	**PLL Multiplier** – These bits specify the PLL output frequency multiplier value, **NS**. The output frequency, f_{OUT} is determined by $f_{OUT} = f_{PRE} * NF$ The **NS** setting should be programmed only when **PEN** is 0. It has no effect when **PEN** is 1	- 0x00 : NS=1 - 0x01 : NS=1 - 0x02 : NS=2 … - 0xFF : NS=255

9.13 PLL Lock Register

Offset Address

PLLR **PLL Lock Register** **0xD5**

BIT	15	14	13	12	11	10	9	8
NAME	**LOCK**							
TYPE	RW							
RESET	0x14							
BIT	7	6	5	4	3	2	1	0
NAME	**LOCK**							
TYPE	RW							
RESET	0x50							

Table 9-13: PLL Lock Register Description

Name	Description	Setting
LOCK Bit 15-0	**LOCK –** These bits specify the PLL lock range in term of PLL reference frequency, f_{FIN} . The maximum PLL lock period is 500us and the default setting assumed the reference clock, f_{FIN} is 10Mhz from tx_clk. The **LOCK** setting should be programmed only when **PEN** is 1. It has no effect when **PEN** is 0.	0x1450 * f_{FIN} = 520us

9.14 Clock Control Register 0/1

Offset Address

CCR_0/CCR_1 **Clock Control Register 0/1** **0xBB(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME			**LPD**					
TYPE	RO	RO	RW					
RESET	0x0	0x0	0x03					

Table 9-14: Clock Control Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-6		
LPD Bit 5-0	**LP Clock Divider** – These bits give the divider value for generating the LP mode clock from the byte clock.	0x0 – NA 0x1 – Divide by 2 … 0x3F – Divide by 64

Remark: e.g. LPD = 0x4

PLL = 400Mbps

= 200MHz

LP clock = 200MHz / LPD / 8 = 200 / 5 / 8 = 5MHz

9.15 Packet Size Control Register 1 0/1

Offset Address

PSCR1_0/PSCR1_1 **Packet Size Control Register1 0/1** **0xBC(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**TDC[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**TDC[7:0]**							
TYPE	RW							
RESET	0x00							

Table 9-15: Packet Size Control Register 1 0/1 Description

Name	Description	Setting
TDC Bit 31-0	**Transmit Data Count** – These bits set the total number of data bytes to be transmitted by the SSD2825 in the next operation. The SSD2825 will use the value in this field to decide what type of packet to send out. It is used together with the **PST** field to decide the outgoing packet length, when the packet is Generic Long Write packet or DCS Long Write packet with DCS command being 0x2C or 0x3C.	

9.16 Packet Size Control Register 2 0/1

Offset Address

PSCR2_0/PSCR2_1 **Packet Size Control Register 2 0/1** **0xBD(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**TDC[31:24]**							
TYPE	RW							
RESET	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**TDC[23:16]**							
TYPE	RW							
RESET	0x0							

Table 9-16: Packet Size Control Register 2 0/1 Description

Name	Description	Setting
TDC Bit 31-0	**Transmit Data Count** – Please see the description of Packet Size Control Register 1.	

9.17 Packet Size Control Register 3 0/1

Offset Address

PSCR3_0 **Packet Size Control Register 3 0** **0xBE(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME				**PST[12]**	**PST[11:8]**			
TYPE	RO	RO	RO	RW	RW			
RESET	0x0	0x0	0x0	0x0	0x1			
BIT	7	6	5	4	3	2	1	0
NAME	**PST[7:0]**							
TYPE	RW							
RESET	0x00							

PSCR3_1 **Packet Size Control Register 3 1** **0xBE(csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								**PST[8]**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**PST[7:0]**							
TYPE	RW							
RESET	0x00							

Table 9-17: Packet Size Control Register 3 0/1 Description

Name	Description	Setting
Reserved Bit 15-13		
PST Bit 12-0	**Packet Size Threshold** – These bits give the threshold value for partitioning the incoming long packet data into smaller packets. The partitioning only applies to the DCS Long Write packet with DCS command being 0x2C or 0x3C. The payload will be partitioned into a few packets where the payload of each packet is (**PST**+1). During smart pixel mode(**IFS** is 1), the **PST** represent the threshold in term of pixel. For example, when **DDF**=10(24 bpp), a **PST** of 50 means the partitioned payload of each packet is (50*3 + 1). For 18 bpp(**DDF**=01), the **PST** should be multiple of 4. During raw mode(**IFS** is 0), the **PST** represent the threshold in term of bytes.	The minimum value is 2 for 16 bit interface and 3 for 24 bit interface. The maximum value allowed is 4159(0x103F) for MCU interface and 511(0x1FF) for SPI interface. If the user tries to program a larger value than the maximum allowed value into this field, SSD2825 will cap the value to the maximum value. In raw mode operation, when the interface setting is 16 bit, the value in this field must be multiple of 2 bytes, or even number. If an odd number is written in, it will be automatically truncated to an even number. For example, 0x5 will be truncated to 0x4.

Name	Description	Setting
		When the interface setting is 24 bit, the value in this field must be in multiple of 3 bytes.

9.18 Generic Packet Drop Register 0/1

Offset Address

GPDR_0/GPDR_1 **Generic Packet Drop Register 0/1** **0xBF(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**GPD[15:8]**							
TYPE	WO							
RESET	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**GPD[7:0]**							
TYPE	WO							
RESET	0x0							

Table 9-18: Generic Packet Drop Register 0/1 Description

Name	Description	Setting
GPD Bit 15-0	**Generic Packet Drop** – This register is not a true register. It is the entry point for the internal buffer. The payload of the generic packets (Generic Short Write, Generic Long Write, and Generic Read) or the command and payload if DCS packet should be written into this register. The SSD2825 will send them out using the corresponding generic or DCS packet. DCS field of CFGR register will be used to determine the data drop into this register is for generic or DCS packet generation. The application processor can treat this register as an FIFO and continuously write data into it. When the interface is 16 bit, the width of this field is 16 bit. When the interface is 8 bit, the width of this field is 8 bit. Since the register is only the entry point of the internal buffer, the application processor is not able to read the data written into the buffer.	

9.19 Operation Control Register 0/1

Offset Address

OCR_0/OCR_1 **Operation Control Register 0/1** **0xC0(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								**RST**
TYPE	RO	RO	RO	RO	RO	RO	RO	RWAC
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**COP**
TYPE	RO	RO	RO	RO	RO	RO	RO	RWAC
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 9-19: Operation Control Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-9		
RST Bit 8	**Software Reset** - Writing a '1' to this bit will reset the entire module except SSD2825 local register setting. This bit will be cleared after the reset is completed. Wrting a '1' to this bit will cause the MIPI link enters TX stop state immediately and any outgoing MIPI packet will be terminated immediately.	0 – NOP 1 – Software Reset
Reserved Bit 7-1		
COP Bit 0	**Cancel Operation** – This bit is to cancel the current operation. When this bit is set to 1, the SSD2825 will still finish transmitting the current packet. (Otherwise, the serial link operation will lose sync.) Afterwards, the SSD2825 will stop any further transmission. It will clear its internal buffer such that all the data being written in and not sent out yet will be cleared. It will also bring the state machine to its initial state. Once this process is finished, the **COP** bit will be automatically set to 0. At the same time, the **PO** bit of the status register will be set to 1 too. At this stage, there is no data in the internal buffer. The application processor can start a new operation. This operation is not valid in video mode(**VEN=1)**.	0 – NOP 1 – Cancel the current operation

9.20 Maximum Return Size Register 0/1

Offset Address

MRSR_0/MRSR_1 **Maximum Return Size Register 0/1** **0xC1(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**MRS**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**MRS**							
TYPE	RW							
RESET	0x01							

Table 9-20: Maximum Return Size Register 0/1 Description

Name	Description	Setting
MRS Bit 15-0	**Maximum Return Size** – These bits set the maximum return size of the read response packet returned by the MIPI slave. The SSD2825 will automatically send out the Set Maximum Return Size packet using the value in this field, before every read operation. It informs the MIPI slave about the limit of the SSD2825. The application processor does not need to program the register before every read operation, if the maximum return size does not change. However, the Set Maximum Return Size packet will always be sent.	

9.21 Return Data Count Register 0/1

Offset Address

RDCR_0/RDCR_1 **Return Data Count Register 0/1** **0xC2(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**RDC**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**RDC**							
TYPE	RO							
RESET	0x00							

Table 9-21: Return Data Count Register 0/1 Description

Name	Description	Setting
RDC Bit 15-0	**Return Data Count** – These bits reflect the number of data bytes received from the MIPI slave read response packet. This register can only be updated by the SSD2825 hardware.	

9.22 ACK Response Status Register 0/1

Offset Address

ARSR_0/ARSR_1 **ACK Response Status Register 0/1** **0xC3(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**AR**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**AR**							
TYPE	RO							
RESET	0x00							

Table 9-22: ACK Response Status Register 0/1 Description

Name	Description	Setting
AR Bit 15-0	**ACK Response** – These bits contain the ACK response from the MIPI slave. The register will be updated when ACK with Error Report packet is received. Otherwise, the value will be set to 0. The bits in this register follow the definition in MIPI DSI. This register can only be updated by the SSD2825 hardware.	

9.23 Line Control Register 0/1

Offset Address

LCR_0/LCR_1 **Line Control Register 0/1** **0xC4(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME			**IBC**	**RT**	**RTB**	**FBC**	**FBT**	**FBW**
TYPE	RO	RO	RW	RWAC	RWAC	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 9-23: Line Control Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-5		
IBC Bit 5	**Ignore Bus Contention** – This bit is to detect bus contention reported by the Analog Phy. If this bit is disabled, whenever bus contention is detected, the state machine will ignore it and continue sending new packet if available. If this bit is enabled, the state machine will halt further transmission.	0 – Detect Bus Contention from Analog Phy 1 – Ignore Bus Contention detected by Analog Phy
RT Bit 4	**Reset Trigger** – This bit is to send a Reset Trigger Message. When this bit is set to 1, the SSD2825 will send a Reset Trigger Message. It is recommended to enter LP mode and send this trigger message. If this bit is programmed during vertical active data is being sent on MIPI link, the reset trigger will be delayed to next vertical blanking period so that the reset trigger message will not disturb the video timing on the MIPI link. Once the Reset Trigger Message is sent out, **RT** bit will be automatically set to 0.	0 – NOP 1 – Send a Reset Trigger Message
RTB **Bit 3**	**Register Triggered BTA** – This bit automatically perform Bus Turnaround(BTA) when link is not used. When bus is returned back from the slave, the link will remains in Low Power state until a new request come in where HS bit determination the transfer mode.	0 – NOP 1 – Automatically perform BTA when link is available. In video mode, it will be sent at the next vertical blanking period.
FBC Bit 2	**Force Bus Contention –** This bit controls whether to force a bus contention on the data lane. This bit will be changed to 0, after the bus contention is not detected.	0 – NOP 1 – Drive the data lane to LP11 to force a bus contention.
FBT	**Force BTA TE –** This bit controls whether to	0 – No BTA after previous BTA

Name	Description	Setting
Bit 1	perform automatic BTA after previous BTA so as to get the TE response from MIPI slave.	1 – Perform automatic BTA after previous BTA
FBW Bit 0	**Force BTA After Write –** This bit controls whether to automatically generate a BTA after a write operation. It is only valid for write operation. After performing BTA, the bus authority has been passed to the MIPI slave. The SSD2825 is not able to send any data to the MIPI slave before the bus authority is passed back. It is the responsibility of the application processor to check the status of the bus before sending any data.	0 – Not BTA after the next write packet. 1 – Automatically perform BTA after the next write packet.

9.24 Interrupt Control Register 0/1

Offset Address

ICR_0/ICR_1 **Interrupt Control Register 0** **0xC5(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**SEE**	**SAE**	**SLEE**	**SLAE**			**MLEE**	**MLAE**
TYPE	RW	RW	RW	RW	RO	RO	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**PLSE**	**LPTOE**	**HSTOE**		**ARRE**	**BTARE**	**POE**	**RDRE**
TYPE	RW	RW	RW	RO	RW	RW	RW	RW
RESET	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 9-24: Interrupt Control Register 0/1 Description

Name	Description	Setting
SEE Bit 15	**Short Buffer Empty Enable –** This bit enables the mapping of **SE** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
SAE Bit 14	**Short Buffer Available Enable –** This bit enables the mapping of **SA** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
SLEE Bit 13	**SPI Long Buffer Empty Enable –** This bit enables the mapping of **SLE** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
SLAE Bit 12	**SPI Long Buffer Available Enable –** This bit enables the mapping of **SLA** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
Reserved Bit 11-10		
MLEE Bit 9	**MCU Long Buffer Empty Enable –** This bit enables the mapping of **MLE** interrupt to the int_0 pin.	0 – Not enabled 1 – Enabled
MLAE Bit 8	**MCU Long Buffer Available Enable –** This bit enables the mapping of M**LA** interrupt to the int_0 pin.	0 – Not enabled 1 – Enabled
PLSE Bit 7	**PLL Lock Status Enable –** This bit enables the mapping of the **PLS** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
LPTOE Bit 6	**LP RX Time Out Enable –** This bit enables the mapping of the **LPTO** interrupt to the int_0/int_1pin.	0 – Not enabled 1 – Enabled
HSTOE Bit 5	**HS TX Time Out Enable –** This bit enables the mapping of the **HSTO** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
Reserved Bit 4		
ARRE Bit 3	**ACK Response Ready Enable –** This bit enables the mapping of **ARR** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled

Name	Description	Setting
BTARE Bit 2	**BTA Response Enable –** This bit enables the mapping of the **BTAR** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
POE Bit 1	**Packet Operation Enable –** This bit enables the mapping of the **PO** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled
RDRE Bit 0	**Read Data Ready Enable –** This bit enables the mapping of the **RDR** interrupt to the int_0/int_1 pin.	0 – Not enabled 1 – Enabled

9.25 Interrupt Status Register 0/1

Offset Address

ISR_0/ISR_1 **Interrupt Status Register 0** **0xC6(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**SE**	**SA**	**SLE**	**SLA**	**CST**	**DST**	**MLE**	**MLA**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**PLS**	**LPTO**	**HSTO**	**ATR**	**ARR**	**BTAR**	**PO**	**RDR**
TYPE	RO	RW1C	RW1C	RW1C	RW1C	RW1C	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x1	0x1	0x0

Table 9-25: Interrupt Status Register 0/1 Description

Name	Description	Setting
SE Bit 15	**Short Buffer Empty –** This bit reflects the status of the internal short buffer of the SPI. If the short buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the short buffer.	0 – The short buffer is not empty. 1 – The short buffer is empty.
SA Bit 14	**Short Buffer Available –** This bit reflects the status of the internal short buffer of the SPI. If the short buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the short buffer.	0 – The short buffer is full. 1 – The short buffer is not full.
SLE Bit 13	**SPI Long Buffer Empty –** This bit reflects the status of the internal long buffer of the SPI interface. If the long buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the long buffer.	0 – The long buffer is not empty. 1 – The long buffer is empty.
SLA Bit 12	**SPI Long Buffer Available –** This bit reflects the status of the internal long buffer of the SPI interface. If the long buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the long buffer.	0 – The long buffer is full. 1 – The long buffer is not full.
CST Bit 11	**Clock Lane Status –** This bit reflects the status at the MIPI Clock lane.	0 – Clock lane is not in LP-11. 1 – Clock lane is in LP-11.
DST Bit 10	**Data Lane Status –** This bit reflects the status at the MIPI Data lane.	0 – Data lane is not in LP-11. 1 – Data lane is in LP-11.
MLE Bit 9	**MCU Long Buffer Empty –** This bit reflects the status of the internal long buffer of the MCU interface. If the long buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the long buffer.	0 – The long buffer is not empty. 1 – The long buffer is empty.
MLA Bit 8	**MCU Long Buffer Available –** This bit reflects the status of the internal long buffer of the MCU interface. If the long buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the long buffer.	0 – The long buffer is full. 1 – The long buffer is not full.

Name	Description	Setting
PLS Bit 7	**PLL Lock Status –** This bit reflects the status of the PLL. Before the PLL is locked, the whole system is running at the reference clock input of the PLL, as the PLL has no output before getting lock. Hence, the application processor must access the registers using slow speed.	0 – PLL has not been locked 1 – PLL has been locked
LPTO Bit 6	**LP RX Time Out –** This bit reflects the status of the LP RX timer.	0 – The LP RX timer has expired. 1 – The LP RX timer has not expired.
HSTO Bit 5	**HS TX Time Out –** This bit reflects the status of the HS TX timer.	0 – The HS TX timer has expired. 1 – The HS TX timer has not expired.
ATR Bit 4	**ACK Trigger Response –** This bit reflects whether the ACK trigger message has been received or not.	0 – ACK trigger message has not been received. 1 – ACK trigger message has been received.
ARR Bit 3	**ACK Response Ready –** This bit reflects whether the ACK response has been received or not. The ACK response can be an ACK trigger message or ACK with Error Report packet.	0 – Response has not been received. 1 – Response has been received.
BTAR Bit 2	**BTA Response –** This bit reflects the data lane status after SSD2825 has made a BTA.	0 – The MIPI slave has not passed the lane authority back. 1 – The MIPI slave has passed the lane authority back.
PO Bit 1	**Packet Operation –** This bit reflects whether the SSD2825 is ready to take in more data from the application processor.	0 – Not ready 1 – Ready
RDR Bit 0	**Read Data Ready –** This bit reflects whether the data from the MIPI slave is ready for read by the application processor. This bit is valid only during the read operation. This bit will be automatically cleared when all the received data are read out.	0 – Not ready 1 – Ready

9.26 Error Status Register 0/1

Offset Address

ESR_0/ESR_1 **Error Status Register 0** **0xC7(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME						**CRCE**	**ECCE2**	**ECCE1**
TYPE	RO	RO	RO	RO	RO	RW1C	RW1C	RW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**SO**	**SLO**		**MLO**		**CONT**		**VMM**
TYPE	RW1C	RW1C	RO	RW1C	RO	RO	RO	RW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 9-26: Error Status Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-11		
CRCE Bit 10	**CRC Error –** This bit reflects the status of CRC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once a CRC error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No CRC error since this bit is cleared 1 – At least 1 CRC error since this bit is cleared
ECCE2 Bit 9	**ECC Multi Bit Error –** This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once an ECC multi-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No ECC multi-bit error since this bit is cleared 1 – At least 1 ECC multi-bit error since this bit is cleared
ECCE1 Bit 8	**ECC Single Bit Error –** This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once an ECC single-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No ECC single-bit error since this bit is cleared 1 – At least 1 ECC single-bit error since this bit is cleared
SO Bit 7	**Short Buffer Overflow –** This bit reflects the status of internal short buffer of the SPI. If the short buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
SLO Bit 6	**SPI Long Buffer Overflow –** This bit reflects the status of internal long buffer of the SPI interface. If the long buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
Reserved Bit 5		

Name	Description	Setting
MLO Bit 4	**MCU Long Buffer Overflow –** This bit reflects the status of internal long buffer of the MCU interface. If the long buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
Reserved Bit 3	Reserved	Reserved
CONT Bit 2	**Contention –** This bit reflects the status of the data lane contention detector.	0 – No contention 1 – Contention has occurred
Reserved Bit 1		
VMM Bit 0	**VC Mis Match –** This bit reflects whether there is a mismatch between the VC ID transmitted by the SSD2825 and the VC ID received from the MIPI slave	0 – No mismatch 1 – Mismatch has occurred

9.27 Data Format Register 0/1

Offset Address

DFR_0/DFR_1 **Data Format Register 0/1** **0xC8(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME				**IFS**	**FT**		**DDF**	
TYPE	RO	RO	RO	RW	RW		RW	
RESET	0x0	0x0	0x0	0x0	0x0		0x0	

Table 9-27: Data Format Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-5		
IFS Bit 4	**Interface Format Select –** This bit specifies the MCU or SPI interface input data format for DCS Long Write packet whose DCS command is 0x2C or 0x3C.	0 – The input is in raw data format. 1 – The input is in pixel format.
FT Bit 3-2	**Interface Format Type –** These bits specify how the data is written in through the MCU or SPI interface. It is valid when **IFS** is 1, the interface type 16 bit and the display data format is 18bpp or 24bpp.	00 – Type 1 01 – Type 2 10 – Type 3 11 – Reserved
DDF Bit 1-0	**Display Data Format –** These bits specify the data format of the incoming data on the MCU or SPI interface. It is valid when **IFS** is 1.	00 – 16bpp 01 – 18bpp 10 – 24bpp 11 – Reserved

NOTE: All these fields are valid only for DCS Long Write packet whose DCS command is 0x2C or 0x3C. In other words, they are valid for DCS Long Write packet that writes data into the display memory. For other DCS commands, the input data is always treated as raw data. These fields are only used in rare cases.

9.28 Delay Adjustment Register 1 0/1

Offset Address

DAR1_0/DAR1_1 **Delay Adjustment Register 1 0/1** **0xC9(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**HZD**							
TYPE	RW							
RESET	0x14							
BIT	7	6	5	4	3	2	1	0
NAME	**HPD**							
TYPE	RW							
RESET	0x02							

Table 9-28: Delay Adjustment Register 1 0/1 Description

Name	Description	Setting
HZD Bit 15-8	**HS Zero Delay** – These bits specifies the number of nibble clock for HS zero delay period $T_{HS-ZERO}$.	
HPD Bit 7-0	**HS Prepare Delay** – These bits specifies the number of nibble clock for HS prepare delay period $T_{HS-PREPARE}$.	

9.29 Delay Adjustment Register 2 0/1

Offset Address

DAR2_0/DAR2_1 **Delay Adjustment Register 2 0/1** **0xCA(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**CZD**							
TYPE	RW							
RESET	0x28							
BIT	7	6	5	4	3	2	1	0
NAME	**CPD**							
TYPE	RW							
RESET	0x03							

Table 9-29: Delay Adjustment Register 2 0/1 Description

Name	Description	Setting
CZD Bit 15-8	**CLK Zero Delay** – These bits specifies the number of nibble clock for CLK zero delay period $T_{CLK\text{-}ZERO}$.	
CPD Bit 7-0	**CLK Prepare Delay** – These bits specifies the number of nibble clock for CLK prepare delay period $T_{CLK\text{-}PREPARE}$.	

9.30 Delay Adjustment Register 3 0/1

Offset Address

DAR3_0/DAR3_1 **Delay Adjustment Register 3 0/1** **0xCB(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**CPED**							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	**CPTD**							
TYPE	RW							
RESET	0x16							

Table 9-30: Delay Adjustment Register 3 0/1 Description

Name	Description	Setting
CPED Bit 15-8	**CLK Pre Delay** – These bits specifies the number of nibble clock for CLK pre delay period $T_{CLK\text{-}PER}$.	
CPTD Bit 7-0	**CLK Post Delay** – These bits specifies the number of nibble clock for CLK post delay period $T_{CLK\text{-}POST}$.	

9.31 Delay Adjustment Register 4 0/1

Offset Address

DAR4_0/DAR4_1 **Delay Adjustment Register 4 0/1** **0xCC(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**CTD**							
TYPE	RW							
RESET	0x0A							
BIT	7	6	5	4	3	2	1	0
NAME	**HTD**							
TYPE	RW							
RESET	0x0A							

Table 9-31: Delay Adjustment Register 4 0/1 Description

Name	Description	Setting
CTD Bit 15-8	**CLK Trail Delay** – These bits specifies the number of nibble clock for CLK trail delay period $T_{CLK\text{-}TRAIL}$.	
HTD Bit 7-0	**HS Trail Delay** – These bits specifies the number of nibble clock for HS trail delay period $T_{HS\text{-}TRAIL}$. Please note that the minimum value for the $T_{HS\text{-}TRAIL}$ is 3.	

9.32 Delay Adjustment Register 5 0/1

Offset Address

DAR5_0/DAR5_1 **Delay Adjustment Register 5 0/1** **0xCD(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**WUD[15:8]**							
TYPE	RW							
RESET	0x10							
BIT	7	6	5	4	3	2	1	0
NAME	**WUD[7:0]**							
TYPE	RW							
RESET	0x00							

Table 9-32: Delay Adjustment Register 5 0/1 Description

Name	Description	Setting
WUD Bit 15-0	**Wake Up Delay** – These bits specifies the number of clock cycles for wake up delay period T_{WAKEUP}. The delay is used to wake up the MIPI slave from ULPS state. The clock is the low power clock.	

9.33 Delay Adjustment Register 6 0/1

Offset Address

DAR6_0/DAR6_1 **Delay Adjustment Register 6 0/1** **0xCE(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME					**TGO**			
TYPE	RO	RO	RO	RO	RW			
RESET	0x0	0x0	0x0	0x0	0x4			
BIT	7	6	5	4	3	2	1	0
NAME					**TGET**			
TYPE	RO	RO	RO	RO	RW			
RESET	0x0	0x0	0x0	0x0	0x5			

Table 9-33: Delay Adjustment Register 6 0/1 Description

Name	Description	Setting
Reserved Bit 15-12		
TGO Bit 11-8	**TA Go Delay** – These bits specifies the number of T_{LPX} for TA go delay period $T_{TA\text{-}GO}$.	
Reserved Bit 7-4		
TGET Bit 3-0	**TA Get Delay** – These bits specifies the number of T_{LPX} for TA get delay period $T_{TA\text{-}GET}$.	

9.34 HS TX Timer Register 1 0/1

Offset Address

HTTR1_0/HTTR1_1 **HS TX Timer Register 1 0/1** **0xCF(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**HTT[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**HTT[7:0]**							
TYPE	RW							
RESET	0x00							

Table 9-34: HS TX Timer Register 1 0/1 Description

Name	Description	Setting
HTT Bit 31-0	**HS TX Timer** – These bits specify the HS TX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2825 enters HS transmit mode. When the SSD2825 exits from HS transmit mode, the timer will be reset. If the timer expires before the end of HS transmission, the SSD2825 will signal an error and switch to LP mode to continue the transmission. At the same time, the **HS** bit will be cleared to 0. Software intervention is required so that the SSD2825 can go back to proper HS transmission mode.	

9.35 HS TX Timer Register 2 0/1

Offset Address

HTTR2_0/HTTR2_1 **HS TX Timer Register 2 0/1** **0xD0(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**HTT[31:24]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**HTT [23:16]**							
TYPE	RW							
RESET	0x10							

Table 9-35: HS RX Timer Register 2 0/1 Description

Name	Description	Setting
HTT Bit 31-0	Please see the description of HS TX Timer Register 1	

9.36 LP RX Timer Register 1 0/1

Offset Address

LRTR1_0/LRTR1_1 **LP RX Timer Register 1 0/1** **0xD1(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**LRT[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**LRT[7:0]**							
TYPE	RW							
RESET	0x00							

Table 9-36: LP TX Timer Register 1 0/1 Description

Name	Description	Setting
LRT Bit 31-0	**LP RX Timer** – These bits specify the LP RX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2825 enters LP receive mode. When the SSD2825 exits from LP receive mode, the timer will be reset. If the timer expires before exiting from LP receive mode, the SSD2825 will signal an error and switch to LP transmit mode. The DPHY will drive the data lane to LP11 state. Software intervention is required so that any possible error could be cleared.	

9.37 LP RX Timer Register 2 0/1

Offset Address

LRTR2_0/LRTR2_1 **LP RX Timer Register 2 0/1** **0xD2(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**LRT[31:24]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**LRT[23:16]**							
TYPE	RW							
RESET	0x10							

Table 9-37: LP TX Timer Register 2 0/1 Description

Name	Description	Setting
LRT Bit 31-0	Please see the description of LP RX Timer Register 1	

9.38 TE Status Register 0/1

Offset Address

TSR_0/TSR_1 **TE Status Register 0/1** **0xD3(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**TER**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 9-38: TE Status Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-1		
TER Bit 0	**TE Response –** This bit reflects whether a TE response has been received or not. Once a TE response is received, this bit will be set to 1. At the same time, the output te_0/te_1 signals will go high. The host processor can write 1 to clear this bit. Once the bit is cleared, the te_0/te_1 signals will go low.	0 –TE response has not been received. 1 – TE response has been received.

9.39 SPI Read Register 0/1

Offset Address

LRR_0/LRR_1 **SPI Read Register 0/1** **0xD4(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**RRA**							
TYPE	RW							
RESET	0xFA							

Table 9-39: SPI Read Register 0/1 Description

Name	Description	Setting
Reserved Bit 15-8		
RRA Bit 7-0	**Register Read Address** – These bits specify the address of the register to be read through the SPI interface, when the interface is SPI 8 bit (either 3 wire or 4 wire).	

9.40 Test Register 0/1

Offset Address

TR_0/TR_1 **Test Register 0/1** **0xD6(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**TM/FL0**		**EIC**					**FLM**
TYPE	RW		RW					RW
RESET	0x0		0x00					0x0
BIT	7	6	5	4	3	2	1	0
NAME	**PNB**						**END**	**CO**
TYPE	RW						RW	RW
RESET	0x01						0x0	0x1

Table 9-40: Test Register 0/1 Description

Name	Description	Setting
TM/FL0 Bit 15-14	**Test Mode –** These bits selects whether to inject CRC/ECC error for the outgoing streams. They are used for debugging purpose only. They should be set to 00 in normal mode! **Force Lane 0** – These bits are valid when **FLM** is 1. During this mode, user can write Low Power value to the MIPI lane 0 data using these bits. SSD2825 will not respond to the normal request through RGB, MCU or SPI interface. **FL0**[1] controls MIPI_DP0 and **FL0**[0] controls MIPI_DN0.	00 – Normal mode 01 – Inject CRC error 10 – Inject 1 bit ECC error 11 – Inject 2 bit ECC error
EIC Bit 13-9	**Error Injection Control –** These bits controls the position of the error being injected for testing. It is only applicable when **TM** is 01.	
FLM Bit 8	**Force Lane Mode –** This bit enable user to write to **FL0** bits to directly control the analog lane DP0 and DP1. The lane should be in Low Power Mode(**HS**=0) when write using **FL0**.	0 – Normal Mode 1 – Force Lane Mode
PNB Bit 7-2	**Packet Number in Blanking Period –** These bits controls the number of packet to send during video mode blanking period.	
END Bit 1	**Endianess** – This bit specifies the endianess of the data transmitted over the serial link. During command mode transmission, this bit takes effect only when the **IFS** bit is 1 and the transmitted packet is DCS write memory packet, 0x2C or 0x3C. During video mode transmission, this bit must be set to 0 so as to follow the MIPI DSI specification.	0 – Least significant byte sent first 1 – Most significant byte sent first
CO Bit 0	**Color Order** – This bit specifies the order of the color component in the pixel. During command mode transmission, this bit takes effect only when the **IFS** bit is 1 and the	0 – RGB. R is in the higher portion of the pixel. 1 – BGR. B is in the higher portion of the pixel.

Name	Description	Setting
	transmitted packet is DCS write memory packet, 0x2C or 0x3C. During video mode transmission, this bit must be set to 1 so as to follow the MIPI DSI specification.	

Remark: 24 bits color format

CO	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0

9.41 TE Count Register 0/1

Offset Address

TECR_0/TECR_1 **TE Count Register 0/1** **0xD7(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**TEC[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**TEC[7:0]**							
TYPE	RW							
RESET	0x01							

Table 9-41: TE Count Register 0/1 Description

Name	Description	Setting
TEC Bit 15-0	**TE Count** – These bits determines the pulse width of the output te_0/te_1 signal. A counter will be started after the TE signal goes to 1. When the counter reaches the value in **TEC** field, the te_0/te_1 signal will be set to 0. The counter uses the PLL reference clock to do counting.	The minimum value is 1.

9.42 Analog Control Register

Offset Address

ACR1 **Analog Control 1 Register** **0xD8**

BIT	15	14	13	12	11	10	9	8
NAME	**MIPI_CONT[15:8]**							
TYPE	RW							
RESET	0x12							
BIT	7	6	5	4	3	2	1	0
NAME	**MIPI_CONT[7:0]**							
TYPE	RW							
RESET	0x1C							

Table 9-42: Analog Control 1 Register Description

Name	Description	Setting
MIPI_CONT Bit 15-0	**MIPI Control** – These bits control the analog Phy input.	

9.43 Analog Control Register 2

Offset Address

ACR2 **Analog Control Register 2** **0xD9**

BIT	15	14	13	12	11	10	9	8
NAME	**MIPI_CONT[31:24]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**MIPI_CONT[23:16]**							
TYPE	RW							
RESET	0x00							

Table 9-43: Analog Control Register 2 Description

Name	Description	Setting
MIPI_CONT Bit 15-0	Please see the description of Analog Phy Control Register 1.	

9.44 Analog Control Register 3

Offset Address

ACR3 **Analog Control Register 3** **0xDA**

BIT	15	14	13	12	11	10	9	8
NAME			**CKI**	**BCI**	**CKF1**	**CKF0**	**GF_E**	**ST_E**
TYPE	RO	RO	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**MIPI_CONT[39:24]**							
TYPE	RW							
RESET	0x00							

Table 9-44: Analog Control Register 3 Description

Name	Description	Setting
CKI Bit 13	**Clock Inversion –** Select to Invert clock lane output polarity inside analog block , when 0, no inversion.	0 – No inversion 1 – Inversion
BCI Bit 12	**Bit Clock Inversion –** This bit controls whether to invert the BITCLK to the analog phy. It should be set to 0 for normal operation.	0 – Do not invert 1 – Invert the BITCLK
CKF1 Bit 11	**ClocK Flip 1 –** This bit controls whether to flip the TX_LP_CP1 and TX_LP_CN1 to the analog block. It should be set to 0 for normal operation.	0 – No Flip 1 – Flip
CKF0 Bit 10	**ClocK Flip 0 –** This bit controls whether to flip the TX_LP_CP0 and TX_LP_CN0 to the analog block. It should be set to 0 for normal operation.	0 – No Flip 1 – Flip
GF_E Bit 9	**Glitch Filter Enable –** This bit controls whether to enable the glitch filter for LP receiver or not.	0 – Disable 1 – Enable
ST_E Bit 8	**Schmitt Trigger Enable –** This bit controls whether to enable or disable the Schmitt Trigger	0 – Disable 1 – Enable
MIPI_CONT Bit 7-0	Please see the description of Analog Phy Control Register 1.	

9.45 Analog Control Register 4

Offset Address

ACR4 **Analog Control Register 4** **0xDB**

BIT	15	14	13	12	11	10	9	8
NAME							**ENLV**	**ISEL[2]**
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**ISEL[1:0]**		**TC**			**TCI**		
TYPE	RW		RW			RW		
RESET	0x0		0x4			0x4		

Table 9-45: Analog Control Register 4 Description

Name	Description	Setting
Reserved Bit 15-10		
ENLV Bit 9	**BandGap Reference Enable**	0 – Disable 1 – Enable
ISEL Bit 8-6	**Current Output Trim**	
TC Bit 5-3	**Temperature Coefficient Select**	
TCI Bit 2-0	**Current Temperature Coefficient Select**	

9.46 Interrupt Output Control Register

Offset Address

IOCR_0/IOCR_1 **Interrupt Output Control Register** **0xDC(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME						**IOT**		**IAS**
TYPE	RO	RO	RO	RO	RO	RW		RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0		0x0

Table 9-46: Interrupt Output Control Register Description

Name	Description	Setting
Reserved Bit 15-3		
IOT Bit 2-1	**Interrupt Output Type –** These bits specify the type of output for the int_0/int_1.	00 – CMOS output 01 – Open Drain active low output(Wired-AND). The IAS should be 0 when selected. 1x – Open Drain active high output(Wired-OR). The IAS should be 1 when selected. 11 – NA
IAS Bit 0	**Interrupt Active State –** This bit indicate the active state of the int_0/int_1 signals.	0 – Active low, normally high 1 – Active high, normally low

9.47 Lane Configuration Register

Offset Address

LCFR **Lane Configuration Register** **0xDE**

BIT	15	14	13	12	11	10	9	8
NAME							**LS1**	**D1E**
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME							**LS0**	
TYPE	RO	RO	RO	RO	RO	RO	RW	
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	

Table 9-47: Lane Configuration Register Description

Name	Description	Setting
Reserved Bit 15-10		
LS1 Bit 9	**Lane Select 1** – This bit, together with **D1E** and **LS0** bits, define the number of lane to be used for DSI_1. When **D1E** is low, **LS1** is invalid.	When **D1E**=0, **LS1** is invalid. When **D1E**=1, **LS0**=00 or 01, 0 – 1 lane mode(DSI_1) 1 – 2 lane mode(DSI_1) When **D1E**=1, **LS0**=10 or 11, 0 – 1 lane mode(DSI_1) 1 – 1 lane mode(DSI_1) When **D1E**=1, if_sel=0, if_sel2=1, DSI_1 follows DSI_0.
D1E Bit 8	**DSI 1 Enable** – This bit controls the enable and disable of the DSI_1 engine. When **D1E** is low, **LS1** is invalid.	0 – DSI_1 is disabled 1 – DSI_1 is enabled
Reserved Bit 7-2		
LS0 Bit 1-0	**Lane Select 0** – These bits, together with **D1E** bits, define the number of lane to be used for DSI_0.	When **D1E**=0, 00 – 1 lane mode(DSI_0) 01 – 2 lane mode(DSI_0) 10 – 3 lane mode(DSI_0) 11 – 4 lane mode(DSI_0) When **D1E**=1 and if_sel=1 00 – 1 lane mode(DSI_0) 01 – 2 lane mode(DSI_0) 10/11 – 3 lane mode(DSI_0) When **D1E**=1 and if_sel=0, if_sel2=1 00 – 1 lane mode(DSI_0) 01/10/11 – 2 lane mode(DSI_0)

9.48 Delay Adjustment Register 7 0/1

Offset Address

DAR7_0/DAR7_1 **Delay Adjustment Register 7 0/1** **0xDF(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME			**HED**					
TYPE	RO	RO	RW					
RESET	0x0	0x0	0x10					

Table 9-48: Delay Adjustment Register 7 0/1 Description

Name	Description	Setting
Reserved Bit 15-6		
HED Bit 5-0	**HS Exit Delay** – These bits specifies the number of nibble clock for HS exit delay period for data and clock lane.	

9.49 Input Pin Control Register 1

Offset Address

IPCR1 **Input Pin Control Register 1** **0xE0**

BIT	15	14	13	12	11	10	9	8
NAME	**PS3_PULL**		**PS2_PULL**		**PS1_PULL**		**PS0_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x1		0x1		0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**TC_PULL**		**IS2_PULL**		**IS_PULL**		**MR_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x1		0x1		0x2	

Table 9-49: Input Pin Control Register 1 Description

Name	Description	Setting
PS3_PULL Bit 15-14	**Pin Select 3 Pull** – These bits select the pull state of the pin PS[3].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS2_PULL Bit 13-12	**Pin Select 2 Pull** – These bits select the pull state of the pin PS[2].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS1_PULL Bit 11-10	**Pin Select 1 Pull** – These bits select the pull state of the pin PS[1].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS0_PULL Bit 9-8	**Pin Select 0 Pull** – These bits select the pull state of the pin PS[0].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
TC_PULL Bit 7-6	**Tx_Clk Pull** – These bits select the pull state of the pin tx_clk.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
IS2_PULL Bit 5-4	**If_Sel2 Pull** – These bits select the pull state of the pin if_sel2.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
IS_PULL Bit 3-2	**If_Sel Pull** – These bits select the pull state of the pin if_sel.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
MR_PULL Bit 1-0	**Mipi_Reset Pull** – These bits select the pull state of the pin mipi_reset_b.	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper

9.50 Input Pin Control Register 2

Offset Address

IPCR2 **Input Pin Control Register 2** **0xE1**

BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**TM2_PULL**		**TM1_PULL**		**TM0_PULL**		**PS4_PULL**	
TYPE	RW		RW		RW		RW	
RESET	0x1		0x1		0x1		0x1	

Table 9-50: Input Pin Control Register 2 Description

Name	Description	Setting
Reserved Bit 15-8		
TM2_PULL Bit 7-6	**Test Mode 2 Pull** – These bits select the pull state of the pin test[2].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
TM1_PULL Bit 5-4	**Test Mode 1 Pull** – These bits select the pull state of the pin test[1].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
TM0_PULL Bit 3-2	**Test Mode 0 Pull** – These bits select the pull state of the pin test[0].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper
PS4_PULL Bit 1-0	**Pin Select 4 Pull** – These bits select the pull state of the pin PS[4].	00 – No pull 10 – 75k pull-up 01 – 75k pull-down 11 – 75k Keeper

9.51 Bidir Pin Control Register 1

Offset Address

BICR1 **Bidir Pin Control Register 1** **0xE2**

BIT	15	14	13	12	11	10	9	8
NAME		**TE0_CTR**					**INT1_CTR[4:3]**	
TYPE	RO	RW					RW	
RESET	0x0	0x0A					0x2	
BIT	7	6	5	4	3	2	1	0
NAME	**INT1_CTR[2:0]**			**INT0_CTR**				
TYPE	RW			RW				
RESET	0x6			0x16				

Table 9-51: Bidir Pin Control Register 1 Description

Name	Description	Setting
Reserved Bit 15		
TE0_CTR Bit 14-10	**Tearing Effect 0 ConTRol** – These bits control the output behavior of the pin te_0. Please refer to Bit 4-0 for definition.	
INT1_CTR Bit 9-5	**Interrupt 1 ConTRol** – These bits control the output behavior of the pin int_1. Please refer to Bit 4-0 for definition.	
INT0_CTR Bit 4-0	**Interrupt 0 ConTRol** – These bits control the output behavior of the pin int_0.	bit 0 : Control the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled bit 1 : Control the direction of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Input 1 – Output bit 2 : Control the output state of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Output is 0 1 – Output is 1 bit 4-3 : Control the pull state of the pin when it is in input state.

9.52 Bidir Pin Control Register 2

Offset Address

BICR2 **Bidir Pin Control Register 2** **0xE3**

BIT	15	14	13	12	11	10	9	8
NAME		**CX0_CTR**					**SO_CTR[4:3]**	
TYPE	RO	RW					RW	
RESET	0x0	0x10					0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**SO_CTR[2:0]**			**TE1_CTR**				
TYPE	RW			RW				
RESET	0x2			0x0A				

Table 9-52: Bidir Pin Control Register 2 Description

Name	Description	Setting
Reserved Bit 15		
CX0_CTR Bit 14-10	**Chip Select 0 ConTRol** – These bits control the output behavior of the pin csx0. Please refer to Bit 4-0 for definition.	
SO_CTR Bit 9-5	**Sys Clock Out ConTRol** – These bits control the output behavior of the pin sys_clk_out. Please refer to Bit 4-0 for definition.	
TE1_CTR Bit 4-0	**Tearing Effect 1 ConTRol** – These bits control the output behavior of the pin te_1.	bit 0 : Control the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled bit 1 : Control the direction of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Input 1 – Output bit 2 : Control the output state of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Output is 0 1 – Output is 1 bit 4-3 : Control the pull state of the pin when it is in input state.

9.53 Bidir Pin Control Register 3

Offset Address

BICR3 **Bidir Pin Control Register 3** **0xE4**

BIT	15	14	13	12	11	10	9	8
NAME		**DM_CTR**					**DH_CTR[4:3]**	
TYPE	RO	RW					RW	
RESET	0x0	0x08					0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**DH_CTR[2:0]**			**CX1_CTR**				
TYPE	RW			RW				
RESET	0x0			0x10				

Table 9-53: Bidir Pin Control Register 3 Description

Name	Description	Setting
Reserved Bit 15		
DM_CTR Bit 14-10	**Data Middle ConTRol** – These bits control the output behavior of the pins DATA[15:8].	
DH_CTR Bit 9-5	**Data High ConTRol** – These bits control the output behavior of the pins DATA[23:16].	
CX1_CTR Bit 14-10	**Chip Select 1 ConTRol** – These bits control the output behavior of the pin csx1.	bit 0 : Control the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled bit 1 : Control the direction of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Input 1 – Output bit 2 : Control the output state of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Output is 0 1 – Output is 1 bit 4-3 : Control the pull state of the pin when it is in input state.

9.54 Bidir Pin Control Register 4

Offset Address

BICR4 **Bidir Pin Control Register 4** **0xE5**

BIT	15	14	13	12	11	10	9	8
NAME		**PCK_CTR**					**VS_CTR[4:3]**	
TYPE	RO	RW					RW	
RESET	0x0	0x08					0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**VS_CTR[2:0]**			**DL_CTR**				
TYPE	RW			RW				
RESET	0x4			0x08				

Table 9-54: Bidir Pin Control Register 4 Description

Name	Description	Setting
Reserved Bit 15		
PCK_CTR Bit 14-10	**Pixel Clock ConTRol** – These bits control the output behavior of the pin pclk. Please refer to Bit 4-0 for definition.	
VS_CTR Bit 9-5	**Vsync ConTRol** – These bits control the output behavior of the pin vsync. Please refer to Bit 4-0 for definition.	
DL_CTR Bit 4-0	**Data Low ConTRol** – These bits control the output behavior of the pins DATA[7:0].	bit 0 : Control the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled bit 1 : Control the direction of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Input 1 – Output bit 2 : Control the output state of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Output is 0 1 – Output is 1 bit 4-3 : Control the pull state of the pin when it is in input state.

9.55 Bidir Pin Control Register 5

Offset Address

BICR5 **Bidir Pin Control Register 5** **0xE6**

BIT	15	14	13	12	11	10	9	8
NAME		**CM_CTR**					**DEN_CTR[4:3]**	
TYPE	RO	RW					RW	
RESET	0x0	0x08					0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**DEN_CTR[2:0]**			**HS_CTR**				
TYPE	RW			RW				
RESET	0x0			0x0C				

Table 9-55: Bidir Pin Control Register 5 Description

Name	Description	Setting
Reserved Bit 15		
CM_CTR Bit 14-10	**Color Mode ConTRol** – These bits control the output behavior of the pin cm. Please refer to Bit 4-0 for definition.	
DEN_CTR Bit 9-5	**Data Enable ConTRol** – These bits control the output behavior of the pin den. Please refer to Bit 4-0 for definition.	
HS_CTR Bit 4-0	**Hsync ConTRol** – These bits control the output behavior of the pin hsync.	bit 0 : Control the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled bit 1 : Control the direction of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Input 1 – Output bit 2 : Control the output state of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Output is 0 1 – Output is 1 bit 4-3 : Control the pull state of the pin when it is in input state.

9.56 Bidir Pin Control Register 6

Offset Address

BICR6 **Bidir Pin Control Register 6** **0xE7**

BIT	15	14	13	12	11	10	9	8
NAME		**SCK_CTR**					**SDC_CTR[4:3]**	
TYPE	RO	RW					RW	
RESET	0x0	0x08					0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**SDC_CTR[2:0]**			**SHUT_CTR**				
TYPE	RW			RW				
RESET	0x0			0x14				

Table 9-56: Bidir Pin Control Register 6 Description

Name	Description	Setting
Reserved Bit 15		
SCK_CTR Bit 14-10	**SPI Clock ConTRol** – These bits control the output behavior of the pin sck. Please refer to Bit 4-0 for definition.	
SDC_CTR Bit 9-5	**SPI DC ConTRol** – These bits control the output behavior of the pin sdc. Please refer to Bit 4-0 for definition.	
SHUT_CTR Bit 4-0	**Shut ConTRol** – These bits control the output behavior of the pin shut.	bit 0 : Control the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled bit 1 : Control the direction of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Input 1 – Output bit 2 : Control the output state of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Output is 0 1 – Output is 1 bit 4-3 : Control the pull state of the pin when it is in input state.

9.57 Bidir Pin Control Register 7

Offset Address

BICR7 **Bidir Pin Control Register 7** **0xE8**

BIT	15	14	13	12	11	10	9	8
NAME		**DBC_CTR**					**SDO_CTR[4:3]**	
TYPE	RO	RW					RW	
RESET	0x0	0x0A					0x1	
BIT	7	6	5	4	3	2	1	0
NAME	**SDO_CTR[2:0]**			**SDI_CTR**				
TYPE	RW			RW				
RESET	0x2			0x08				

Table 9-57: Bidir Pin Control Register 7 Description

Name	Description	Setting
Reserved Bit 15-10		
DBC_CTR Bit 14-10	**Display Brightness Control ConTRol** – These bits control the output behavior of the pin dbcl. Please refer to Bit 4-0 for definition.	
SDO_CTR Bit 9-5	**SPI Data Out ConTRol** – These bits control the output behavior of the pin sdo. Please refer to Bit 4-0 for definition.	
SDI_CTR Bit 4-0	**SPI Data In ConTRol** – These bits control the output behavior of the pin sdi.	bit 0 : Control the pin to be module controlled or register controlled. 0 – Module controlled 1 – Register controlled bit 1 : Control the direction of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Input 1 – Output bit 2 : Control the output state of the pin when bit[0] is 1. When bit[0] is 0, it has no effect. 0 – Output is 0 1 – Output is 1 bit 4-3 : Control the pull state of the pin when it is in input state.

9.58 CABC Brightness Control Register 1

Offset Address

CBCR1 **CABC Brightness Control Register 1** **0xE9(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**WDBV**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**GAM18**	**LBP**	**BL**	**DD**	**BCTR**	**BP_MODE**		**CABC_ EN**
TYPE	RW	RW	RW	RW	RW	RW		RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0		0x0

Table 9-58: CABC Brightness Control Register 1 Description

Name	Description	Setting
WDBV Bit 15-8	**Write Display Brightness Value** – These bits control the brightness setting.	
GAM18 Bit 7	**Gamma 18** – This bit controls gamma 18 select.	
LBP Bit 6	**LCE ByPass** – This bit controls bypass of LCE module.	
BL Bit 5	**BackLight Control** – This bit controls the backlight on/off at BC line.	0 – Off (Completely turn off backlight circuit) 1 – On
DD Bit 4	**Display Dimming** – This bit controls the display dimming feature.	0 – Display Dimming Off 1 – Display Dimming On
BCTR Bit 3	**Brightness Control** – This bit controls the On/Off state of the Brightness Control block.	0 – Off 1 – On
BP_MODE Bit 2-1	**BP MODE** – These bits control the Brightness Preservation of the CABC.	00 – Disable DABC 01 – Conservation Mode (Or User Interface Mode) 10 – Normal Mode (Or Still Picture Mode) 11 – Aggressive Mode (Or Moving Image Mode)
CABC_EN Bit 0	**CABC ENable** – This bit enable the CABC feature. This bit is valid only when if_sel is 0.	0 – CABC is disable 1 – CABC is enable

9.59 CABC Brightness Control Register 2

Offset Address

CBCR2 **CABC Brightness Control Register 2** **0xEA(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**PWM_PS**				**BCB_PS**			
TYPE	RW				RW			
RESET	0x6				0x9			
BIT	7	6	5	4	3	2	1	0
NAME	**CABC_MB**							
TYPE	RW							
RESET	0x00							

Table 9-59: CABC Brightness Control Register 2 Description

Name	Description	Setting
PWM_PS Bit 15-12	**PWM PreScale** – These bits control the PWM signal frequency.	This will depend on pixel clock speed (pclk). For example, 10MHz = “0111” or “1000” 20MHz = “0110” or “0101”
BCD_PS Bit 11-8	**BCB PreScale** – These bits control the number of iternation per second carried out by the BCB unit.	This will depend on pixel clock speed (pclk). For example, 5MHz = “0101” 10MHz = “0110” 25MHz = “1001” 50MHz = “1011” 75MHz = “1100”
CABC_MB Bit 7-0	**CABC Minimum Brightness** – These bits control the CABC Minimum Brightness level.	

9.60 CABC Brightness Status Register

Offset Address

CBSR **CABC Brightness Status Register** **0xEB(csx0)**

BIT	15	14	13	12	11	10	9	8
NAME	**VGA_SEL**							**BCL**
TYPE	RW				RO	RO	RO	RO
RESET	0x0				0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**RDBV**							
TYPE	RO							
RESET	0x00							

Table 9-60: CABC Brightness Status Register Description

Name	Description	Setting
VGA_SEL Bit 15-12	**VGA SELect –** These bits select the type of resolution of the RGB frame. Panel resolutions need not be matched exactly. For example, "0111" will work for any panel with 384000 pixels (+/- 15%). In other words, the range is 326400 to 441600 pixels. Hence, 800x480, 480x800, 512x750 and 750x512 will be supported by **VGA_SEL**= "0111".	0001 - 400x240 (WQVGA) 0010 - 400x300 (SQVGA) 0011 - 480x320 (FVGA) 0100 - 540x360 (FVGA+) 0101 - 600x400 (FVGA++) 0110 - 640x480 (VGA) 0111 - 800x480 (WVGA) 1000 - 800x600 (SVGA) 1001 - 1024x600 (WSVGA) 1010 - 1024x768 (XGA) 1011 - 1280x768 (WXGA) 1100 - 1280x960 (SXGA) 1101 - Reserved 1110 - Reserved 1111 - Reserved
Reserved Bit 11-9		
BCL Bit 8	**Brightness Control Line** – This bit is the pulse width modulation signal output to control external backlight power source. This output is used for Architecture I.	
RDBV Bit 7-0	**Read Display Brightness Value** – These bits show the brightness value of the CABC. This output is used for Architecture II.	

9.61 Read Register 0/1

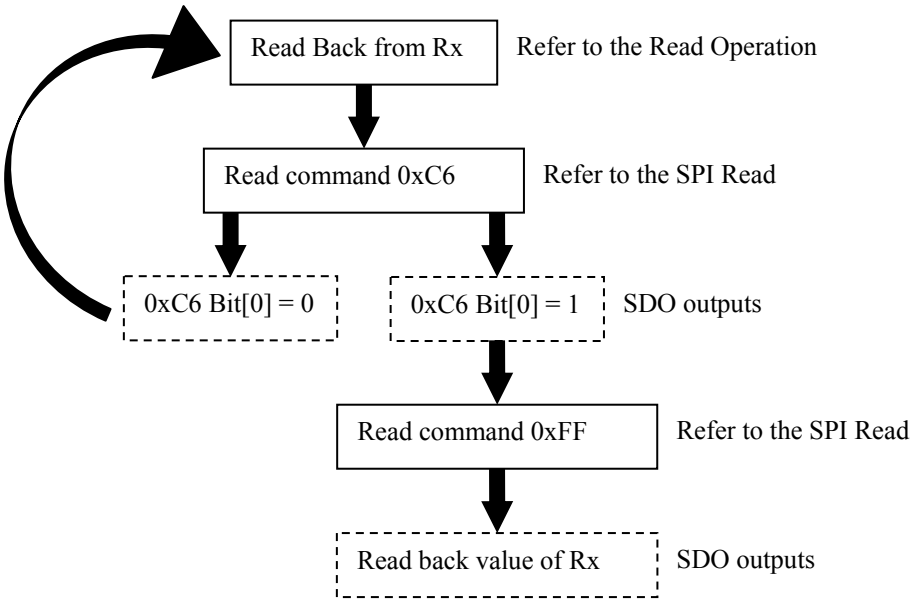
Offset Address

RR_0/RR_1 **Read Register 0/1** **0xFF(csx0/csx1)**

BIT	15	14	13	12	11	10	9	8
NAME	**RD[15:8]**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**RD[7:0]**							
TYPE	RO							
RESET	0x00							

Table 9-61: Read Register 0/1 Description

Name	Description	Setting
RD Bit 15-0	**Read Data** – This register is not a true register. It is the entry point for the internal buffer. It is used to read the data returned by the MIPI slave. The application processor can treat this register as an FIFO and continuously read data from it. When the interface is 16 bit, the width of this field is 16 bit. When the interface is 8 bit, the width of this field is 8 bit. The read of this register is only valid when the **RDY** bit is 1. In other words, only when the data returned by the MIPI slave is received, the application processor can read this register to get return data.	



10 Configuration

The SSD2825 can be configured to support various operations involving 1 or 2 DSI engines. The signals involved are ps[4:0], if_sel, if_sel2 pins, D1E, LS0 and LS1 register bits. These signals define the interface type supported at the front-end as well as lane distribution at the MIPI link. The features that define the operation of SSD2825 are as below.

- 1 or 2 MIPI links
- Number of lane for each MIPI link
- RGB, MCU and SPI interfaces select at the front-end
- Combination of dump, smart, dump/smart, smart/smart configurations
- Selection of the mode within each interface type for MCU, SPI and RGB

The table below explains the relationship of if_sel, if_sel2, D1E, LS0 and LS1 bits.

Table 10-1: SSD2825 Configuration Settings

Use case	if_sel	if_sel2	D1E	LS0	LS1	DSI_0	DSI_1	Setting
1	0	X	0	Select 1, 2, 3 or 4 lanes	NA	RGB+SPI0	OFF	RGB/SPI Mode
2	1	X	0	Select 1, 2, 3 or 4 lanes	NA	MCU0	OFF	MCU Mode
3	0	0	1	Select 1, 2 or 3 lanes	Select 1 or 2 lanes	RGB+SPI0	SPI1	RGB/SPI + SPI Mode
4	0	1	1	Select 1 or 2 lanes	Select 1 or 2 lanes	RGB+SPI0	RGB+SPI1	Split Dump Mode
5	1	0	1	Select 1, 2 or 3 lanes	Select 1 or 2 lanes	MCU0	SPI1	MCU + SPI Mode
6	1	1	1	Select 1, 2 or 3 lanes	Select 1 or 2 lanes	MCU0	MCU1	MCU + MCU Mode

Note :
- SPI0 = SPI interface using csx0
- SPI1 = SPI interface using csx1
- MCU0 = MCU interface using csx0
- MCU1 = MCU interface using csx1
- SPI = SPI0 or SPI1, MCU = MCU0 or MCU1

-

10.1 Lane Management

The number of lanes used for each DSI engine is determined by the LS0, LS1 and D1E bits. The SSD2825 DPHY lanes consist of 2 clock lanes(CL0, CL1) and 4 data lanes(DL0, DL1, DL2, DL3) and they are shared by the 2 DSI engines.

The table below list down all the combination of lane usage for each DSI engine and the active state of each of the DPHY lanes.

Table 10-2: SSD2825 Lane Management

D1E	LS0	LS1	DSI_0	DSI_1	CL0	CL1	DL0	DL1	DL2	DL3	Max. Speed
0	00	X	1 lane	NA	DSI_0	OFF	DSI_0	OFF	OFF	OFF	DSI_0 up to 0.6Gbps
0	01	X	2 lanes	NA	DSI_0	OFF	DSI_0	DSI_0	OFF	OFF	DSI_0 up to 1.2Gbps
0	10	X	3 lanes	NA	DSI_0	OFF	DSI_0	DSI_0	DSI_0	OFF	DSI_0 up to 1.8Gbps
0	11	X	4 lanes	NA	DSI_0	OFF	DSI_0	DSI_0	DSI_0	DSI_0	DSI_0 up to 2.4Gbps
1	00	0	1 lane	1 lane	DSI_0	DSI_1	DSI_0	OFF	DSI_1	OFF	DSI_0 up to 0.6Gbps, DSI_1 up to 0.6Gbps
1	00	1	1 lane	2 lane	DSI_0	DSI_1	DSI_0	OFF	DSI_1	DSI_1	DSI_0 up to 0.6Gbps, DSI_1 up to 1.2Gbps
1	01	0	2 lanes	1 lane	DSI_0	DSI_1	DSI_0	DSI_0	DSI_1	OFF	DSI_0 up to 1.2Gbps, DSI_1 up to 0.6Gbps
1	01	1	2 lanes	2 lanes	DSI_0	DSI_1	DSI_0	DSI_0	DSI_1	DSI_1	DSI_0 up to 1.2Gbps, DSI_1 up to 1.2Gbps
1	10 or 11	X	3 lanes	1 lane	DSI_0	DSI_1	DSI_0	DSI_0	DSI_1	DSI_0	DSI_0 up to 1.8Gbps, DSI_1 up to 0.6Gbps

10.2 SSD2825 Registers Accessibility

The MIPI registers are divided into 3 classes, cfg class, cs0 and cs1 classes. For cfg class, it can be accesses by csx0 or csx1 in MCU or SPI modes. For cs0 class, it can only be accesses by chip select signal, csx0 and for cs1 class; it can only be accesses by chip select signal, csx1.

The table below list out the accessibility of the registers for each of the configuration settings.

Table 10-3: SSD28265 Registers

Use case	D1E	if_sel	if_sel2	cfg registers	cs0 registers for DSI_0	cs1 registers for DSI_1
1	0	0	X	SPI0	SPI0	NA
2	0	1	X	MCU0	MCU0	NA
3	1	0	0	SPI0 or SPI1	SPI0	SPI1
4	1	0	1	SPI0 or SPI1	SPI0	SPI1
5	1	1	0	MCU0 or SPI1	MCU0	SPI1
6	1	1	1	MCU0 or MCU1	MCU0	MCU1

Note :
- SPI0 = SPI interface using csx0
- SPI1 = SPI interface using csx1
- MCU0 = MCU interface using csx0
- MCU1 = MCU interface using csx1
- SPI = SPI0 or SPI1, MCU = MCU0 or MCU1

10.3 Memory Usage

There are short buffers and long buffers within SSD2825. They are shared between DSI_0 and DSI_1 engines, depends on the configurations or the use cases. Long buffer is used when the byte count for Generic packet or DCS packet(including DCS header) is greater or equal than 8. Short buffer is used when the byte count is less than 8.

The table below list out the accessibility of the buffer memories for each of the configuration settings.

Table 10-4: Buffer Memory Management for SSD2825

Use case	D1E	if_ sel	if_ sel2	Long Buffer (4096 bytes)	Long Buffer (128 bytes)	Long Buffer (512 bytes)	Short Buffer DSI_0 (8 slots)	Short Buffer DSI_1 (8 slots)	Mode
1	0	0	X	RGB (DSI_0)	SPI0 (DSI_0)	NA	SPI0 (DSI_0)	NA	RGB/SPI0
2	0	1	X	MCU0 (DSI_0)	NA	NA	MCU0 (DSI_0)	NA	MCU0
3	1	0	0	RGB (DSI_0)	SPI0 (DSI_0)	SPI1 (DSI_1)	SPI0 (DSI_0)	SPI1 (DSI_1)	RGB/SPI0+ SPI1
4	1	0	1	RGB0, RGB1 (DSI_0, DSI_1)	SPI0 (DSI_0)	SPI1 (DSI_1)	SPI0 (DSI_0)	SPI1 (DSI_1)	RGB/SPI0+RGB/SPI1
5	1	1	0	MCU0 (DSI_0)	NA	SPI1 (DSI_1)	MCU0 (DSI_0)	SPI1 (DSI_1)	MCU0+SPI1
6	1	1	1	MCU0 (DSI_0)	NA	MCU1 (DSI_1)	MCU0 (DSI_0)	MCU1 (DSI_1)	MCU0+MCU1

Note :
- SPI0 = SPI interface using csx0
- SPI1 = SPI interface using csx1
- MCU0 = MCU interface using csx0
- MCU1 = MCU interface using csx1
- SPI = SPI0 or SPI1, MCU = MCU0 or MCU1
- In use case 4, the long buffer is shared by both engines. Each engine accesses half of the 1 video line.

10.4 Use cases

The SSD2825 can support 2 kinds of interface configuration. One is MCU interface. The other is a combination of RGB and SPI interface. Both can be used to drive multiple display panels. The details of supported configuration are listed below.

10.4.1 One MIPI link

The SSD2825 operates in single MIPI link mode when **D1E** bit is 0.

10.4.1.1 RGB + SPI Interface (use case 1 in Table 10-1)

The application processor can use this configuration to drive a dumb display panel or a smart display panel or both panels. The user needs to set the if_sel pin to low and set PS[1:0] to select the desired SPI interface. When the SPI interface is not used, the csx0 or csx1 pins needs to be kept high.

Since the RGB and SPI interface are completely separated, the two interfaces can operate independently. The RGB interface is used to provide display data for the video mode. The SPI interface is used to program the local registers of SSD2825. If a dumb display panel is driven and the registers of the display need to be programmed, the SPI interface can also be used for register programming in command mode. If a smart display panel is driven, the SPI interface can also be used to configure the smart display and send display data, in command mode. Below are some illustrations for the use case.

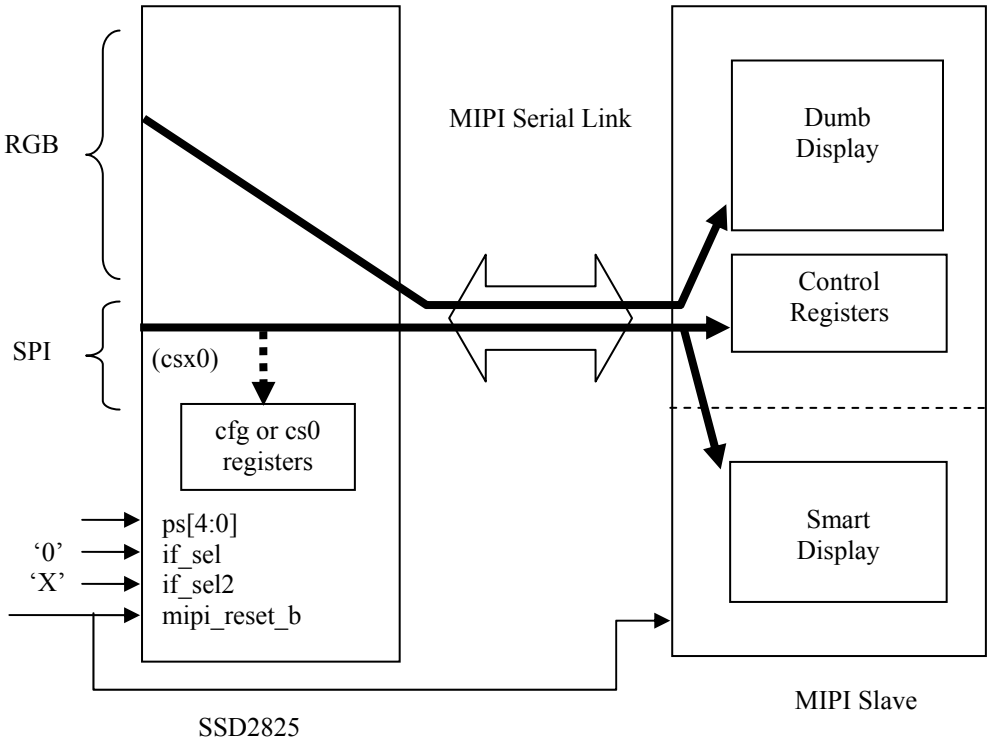


Figure 10-1: SSD2825 with RGB and SPI Interface using 1 MIPI link

The data for different destinations are separated by the VC field of the packets. The user can program the register **VCR** to set the VC field. When this configuration is used, the primary usage of the serial link is for sending display video data to the dumb panel. If there is a need to send non-video data through SPI interface concurrently, the SSD2825 can put them into generic write or DCS write packet and interleave them with the video packets.

If the non-burst video mode is selected, the non-video data packet will only be sent during vertical blanking period. If burst video mode is selected, the non-video data packet can be sent during both horizontal and vertical blanking period (e.g. BLLP period).

During both horizontal and vertical blanking period, the serial link can either remain in HS mode (sending blanking packet) or enter LP mode. The non-video data can also be sent in HS or LP mode. Options have been provided for whether to use HS or LP mode for the blanking period and whether to send the non-video data in HS or LP mode. The **NVD** and **BLLP** bits in register **VICR6** are provided for this purpose. Please refer to the table below for details.

Table 10-5: Operation during Video Mode BLLP Period

NVD	BLLP	Non-burst mode	Burst mode
0	0	If there is no non-video data to send, the serial link will send blanking packet in HS mode during BLLP period. If there is non-video data to send, the non-video data will be sent in HS mode. Afterwards, the serial link will send blanking packet in HS mode for the remaining period of BLLP period.	If there is no non-video data to send, the serial link will enter LP mode during BLLP period. If there is non-video data to send, non-video data will be sent in HS mode. Afterwards, the serial link will enter LP mode for the remaining period of BLLP period.
0	1	If there is no non-video data to send, the serial link will enter LP mode during BLLP period. If there is non-video data to send, non-video data will be sent in HS mode. Afterwards, the serial link will enter LP mode for the remaining period of BLLP period.	Same as non-burst mode.
1	x	The serial link will enter LP mode for BLLP mode. If there is non-video data to send, the data will be sent in LP mode at the beginning of BLLP period.	Same as non-burst mode.

10.4.1.2 MCU Interface(use case 2 in Table 10-1)

The application processor can use this configuration to drive a smart display panel through. The MCU interface control signals are multiplexed with the RGB interface control signals to reduce the pin count, as the two interfaces do not operate at the same time. The user needs to set the if_sel pin to high and ps[4:2] to select the desired MCU interface. When the MCU interface is not used, the csx0 or csx1 pins need to be kept high.

The MCU interface is also used to program the local registers of SSD2825, configure and send display data to the smart panels in command mode. Below are some illustrations for the use case.

The data for different destinations are separated by the VC field of the packets. The user can program the **VCR** register to set the VC field. The multiple smart displays can be updated in a time multiplexing manner.

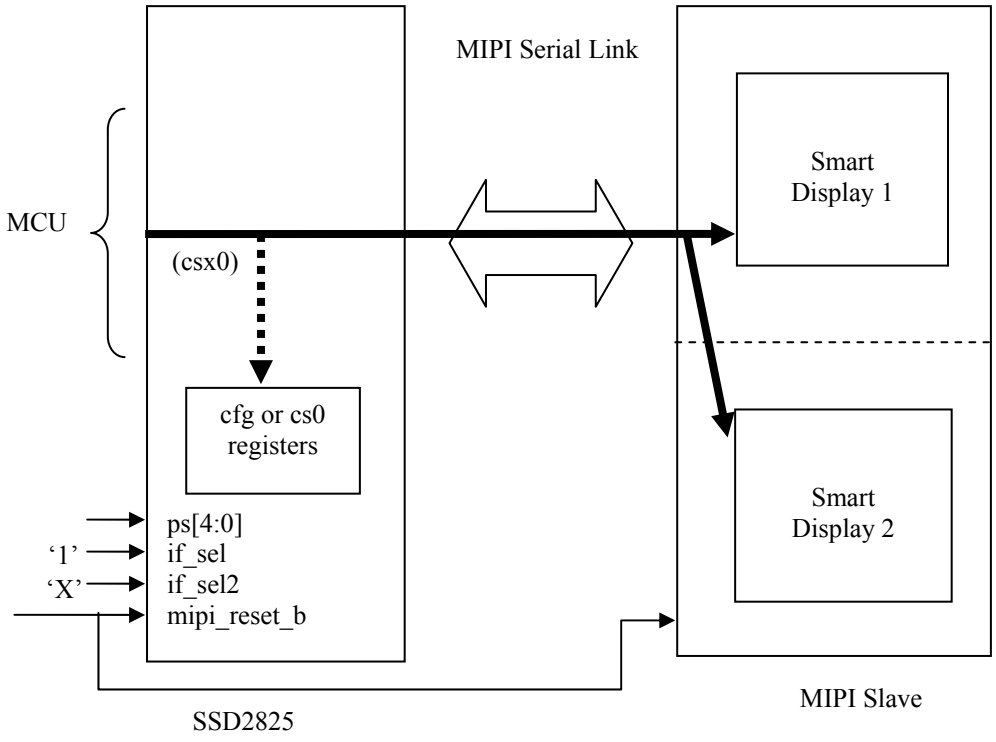


Figure 10-2: SSD2825 with MCU Interface using 1 MIPI link

10.4.2 Two MIPI links

The SSD2825 operates in dual MIPI links mode when **D1E** bit is 1.

10.4.2.1 RGB + 2 SPI Interface (use case 3 in Table 10-1)

The application processor can use this configuration to drive a dumb display panel and another smart display panel using 2 MIPI links. The user needs to set the if_sel pin to low and set PS[1:0] to select the desired SPI interface. When the SPI interface is not used, the csx0 or csx1 pins needs to be kept high.

Since the RGB and SPI interface are completely separated, the two interfaces can operate independently. The RGB interface is used to provide display data for the video mode. The SPI interface using csx0 is used to program the local registers of SSD2825. If a dumb display panel is driven and the registers of the display need to be programmed, the SPI interface using csx0 can also be used for register. If the smart display panel is driven on the secondary MIPI slave, the SPI interface using csx1 can be used to configure the smart display. Below are some illustrations for the use case.

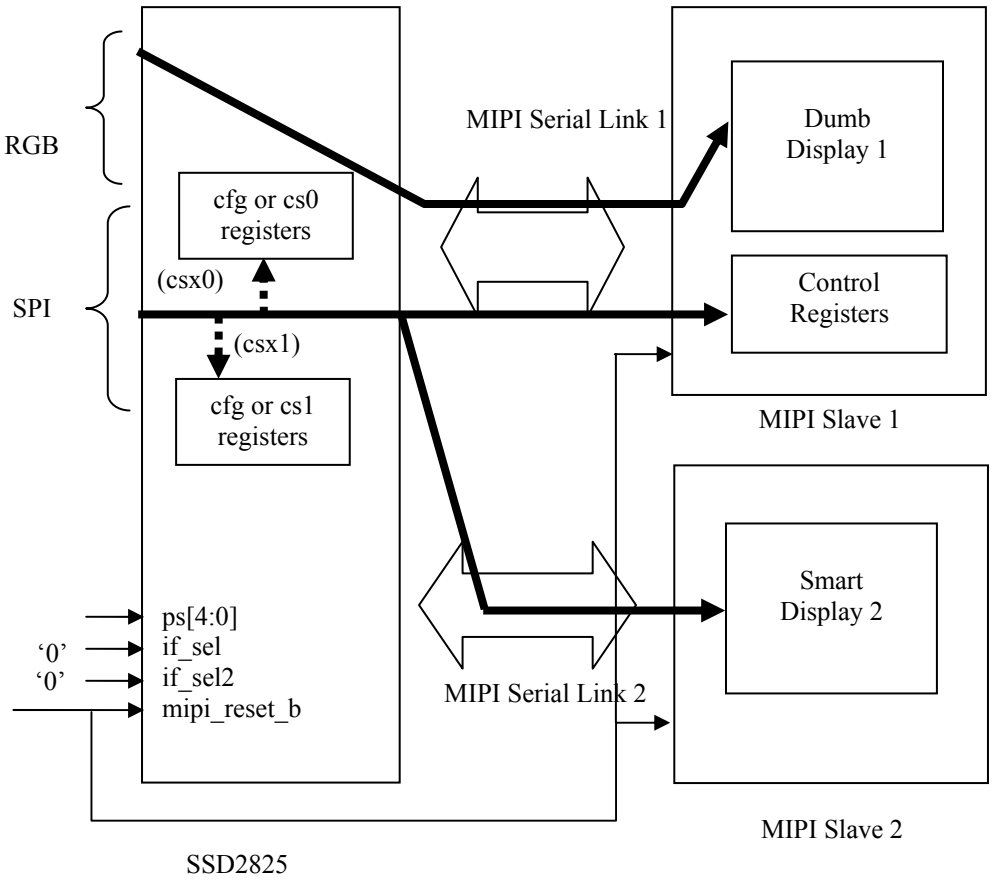


Figure 10-3: SSD2825 with RGB and 2 SPI Interfaces using 2 MIPI links

10.4.2.2 Two MCU Interface(use case 5 in Table 10-1)

The application processor can use this configuration to drive multiple smart display panels. The MCU interface control signals are multiplexed with the RGB interface control signals to reduce the pin count, as the two interfaces do not operate at the same time. The user needs to set the if_sel pin to high and ps[4:2] to select the desired MCU interface. When the MCU interface is not used, the csx0 or csx1 pins needs to be kept high.

The MCU interface is used to program the local registers of SSD2825, configure and send display data to the smart panels in command mode. SSD2825 can drive multiple smart panels. Below are some illustrations for the use case.

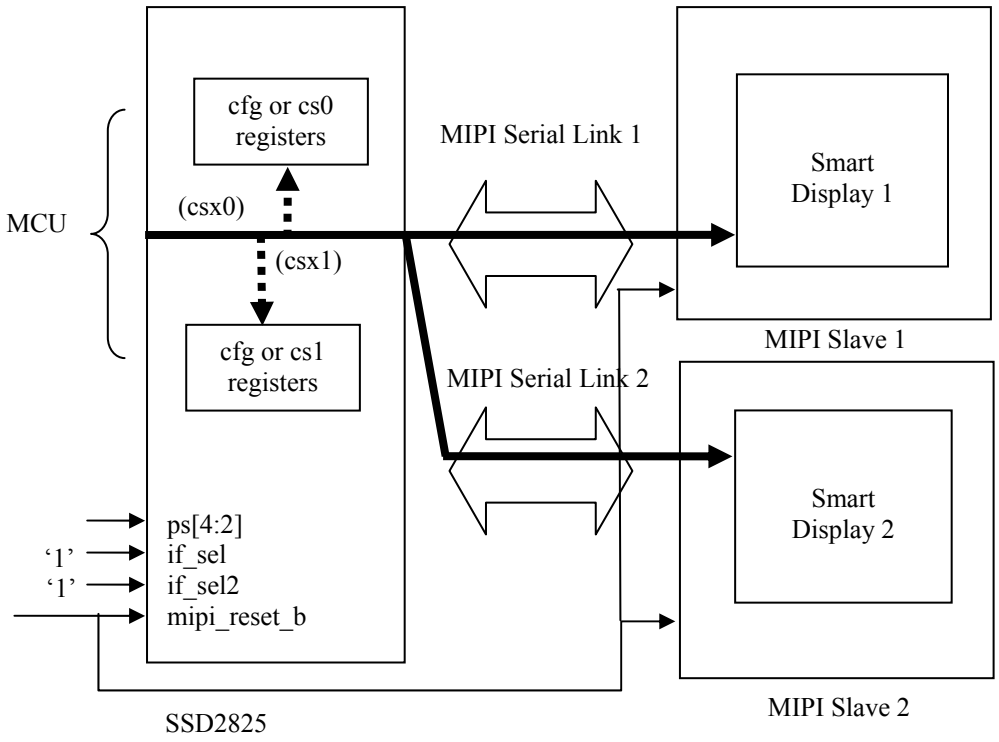


Figure 10-4: SSD2825 with 2 MCU Interfaces using 2 MIPI links

10.4.2.3 2 RGB + 2 SPI Interfaces (use case 4 in Table 10-1)

The application processor can use this configuration to drive 2 dumb display panels as though as it is driving 1 panel using 2 MIPI links. The user needs to set the if_sel pin to low, if_sel2 to high and set PS[1:0] to select the desired SPI interface. When the SPI interface is not used, the csx0 or csx1 pins needs to be kept high.

Since the RGB and SPI interface are completely separated, the two interfaces can operate independently. The RGB interface is used to provide display data for the video mode. The SPI interface is used to program the local registers of SSD2825. If a dumb display panel is driven and the registers of the display need to be programmed, the SPI interface can also be used for register programming in command mode using csx0.

The SSD2825 will split the incoming video line into 2 and store it in the RGB buffers for DSI_0 and DSI_1. Once full line is received, it will activate DSI_0 and DSI_1 and send out each half of the full line to the dump displays. The data for the first half of the line will be sending to DSI_0, while the second half of the line will be send to DSI_1.

In this mode, the number of lane selected for DSI_1 will depends on DSI_0. If DSI_0 is selected for 1 lane mode, DSI_1 will be in 1 lane mode. If DSI_0 is selected for 2 lanes mode, DSI_1 will be in 2 lanes mode.

Below are some illustrations for the use case.

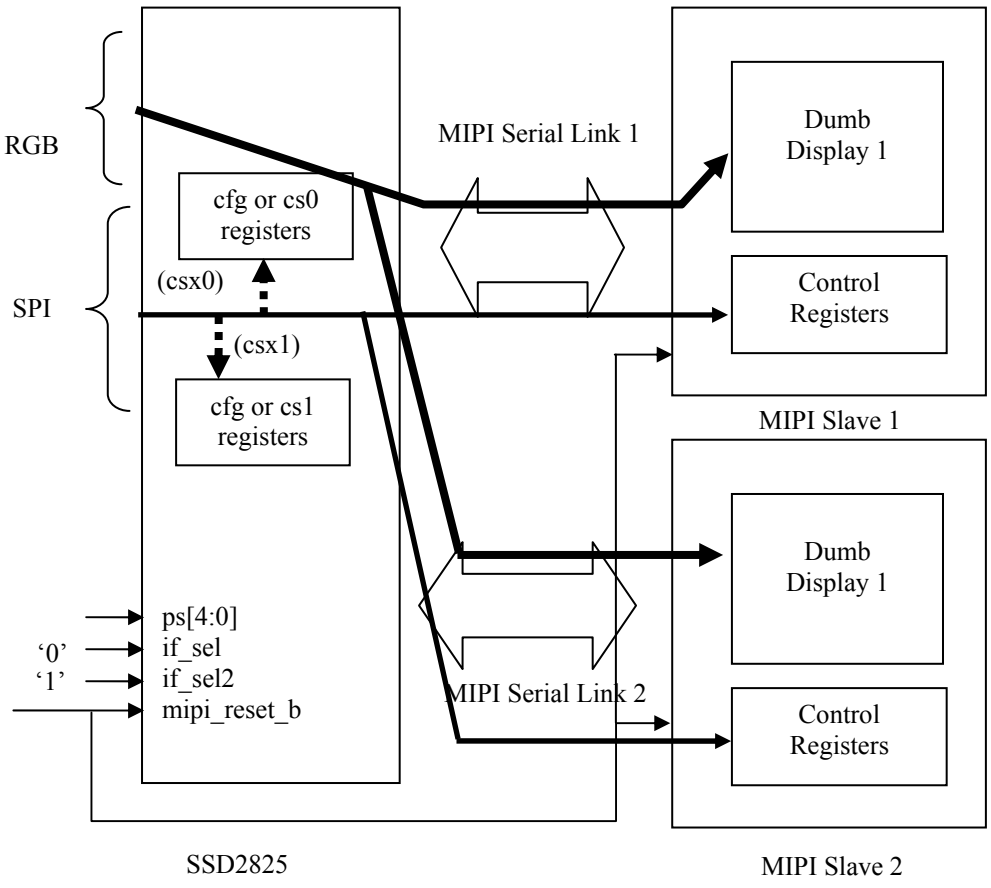


Figure 10-5: SSD2825 with 2 RGB and 2 SPI Interfaces (split dump) using 2 MIPI links

10.4.3 MIPI DC Characteristics

Different State Code of the DSI represents different DC voltage levels in the Data and Clock Lanes as stated in below table.

Table 10-6: DSI State Code and DC Characteristics

State Code	Line Voltage Levels	
	Dp-Line	**Dn-Line**
HS-0	HS Low	HS High
HS-1	HS High	HS Low
LP-00	LP Low	LP Low
LP-01	LP Low	LP High
LP-10	LP High	LP Low
LP-11	LP High	LP High

As shown in Figure 10-6, the logic level is different in different state.

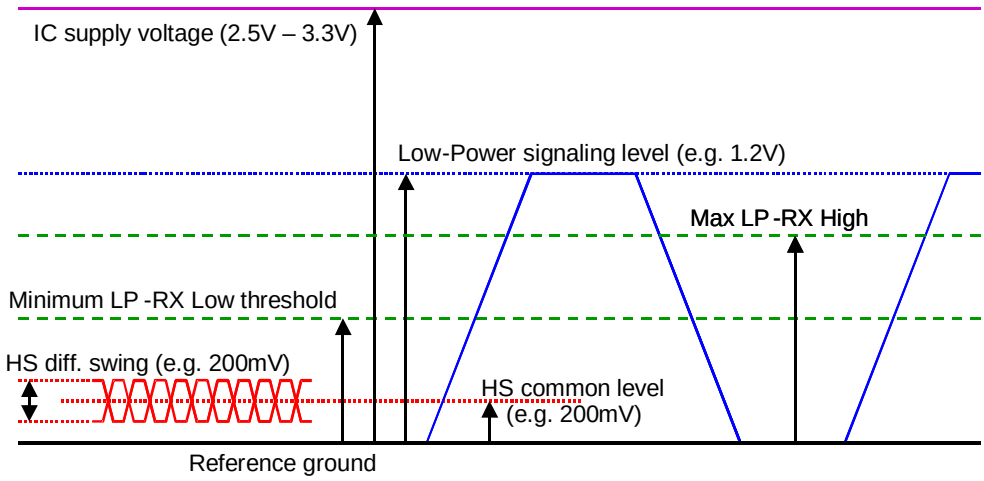


Figure 10-6: MIPI Line Levels

10.4.4 High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock Start and Stop procedures are shown in the following figure.

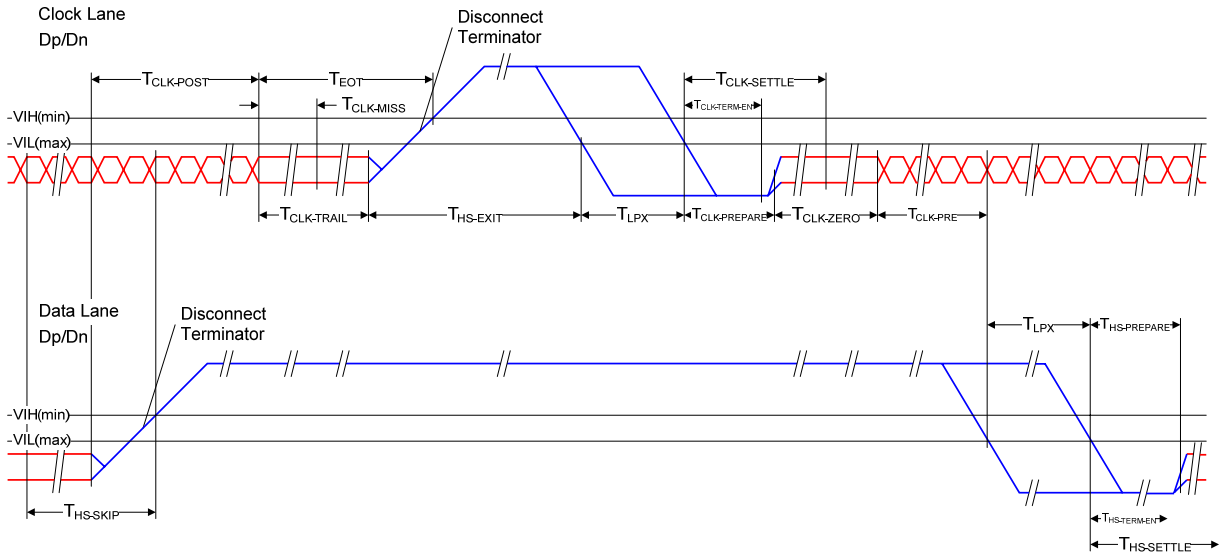


Figure 10-7: Switching the Clock Lane between High Speed Mode and Low-Power Mode

10.4.5 Data Lane State Flow

There are three modes that the Data Lane can be driven into:

1. High Speed Data Transmission
2. Bi-Directional Data Lane Turnaround
3. Escape Mode

Table 10-7: Data Lane Mode Entering/Exiting Sequences

Mode	Entering Mode Sequences	Exiting Mode Sequences
High Speed Data Transmission	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11
Bi-Directional Data Lane Turnaround	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Escape	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z

10.4.6 High Speed Data Transmission

High-Speed Data Transmission occurs in bursts. Transmission starts from, and ends with, a Stop state. During the intermediate time between bursts a Data Lane shall remain in the Stop state, unless a Turnaround or Escape request is presented on the Lane. During a HS Data Burst the Clock Lane shall be in High-Speed mode, providing a DDR Clock to the Slave side.

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure.
Table 10-8 describes the sequence of events on TX and RX side.

Table 10-8: Start-of-Transmission Sequence

Observes Stop state
Observes transition from LP-11 to LP-01 on the Lines
Observes transition form LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D\text{-}TERM\text{-}EN}$
Enables HS-RX and waits for Time-out $T_{HS\text{-}SETTLE}$ in order to neglect transition effects
Starts looking for Leader-Sequence
Synchronizes upon recognition of Leader Sequence '011101'
Receives payload data

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 10-9 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

Table 10-9: End-of-Transmission Sequence

Receives payload data
Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
Neglect bits of last period $T_{HS\text{-}SKIP}$ to hide transition effects
Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

The following shows the sequence of the high speed data transmission including SoT data.

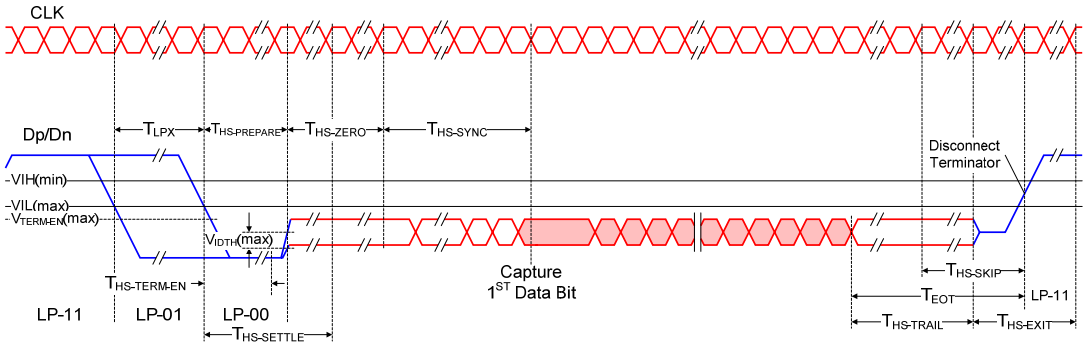


Figure 10-8: High-Speed Data transmission in Bursts

10.4.7 Bi-Directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction.

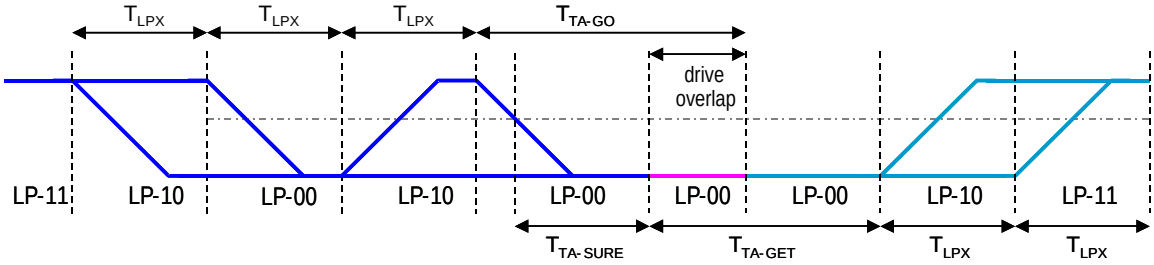


Figure 10-9: Turnaround Procedure

10.4.8 Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and is optional in the Reverse direction. If supported, Escape mode does not have to include all available features.

A Data Lane enters Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Table 10-10 lists all currently available Escape mode commands and actions. All unassigned commands are reserved for future expansion.

The Stop state is be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

Table 10-10: MIPI Escape Mode Entry Code

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Tearing Effect	Trigger	01011101
Acknowledge	Trigger	00100001
Unknown-5	Trigger	10100000

10.4.9 Low Power Data Transmission

The Low Power Data Transmission can be started as the following sequences:

- Start: LP-11
- Escape Mode Entry: LP-11, LP-10, LP-00, LP-01,LP-00
- Low Power Data Transmission command: 11100001
  - One or more bytes (8 bit)
  - Pause mode when data lane are stopped
- Exit Escape Mode: LP-00, LP-10, LP-11
- Stop State : LP-11

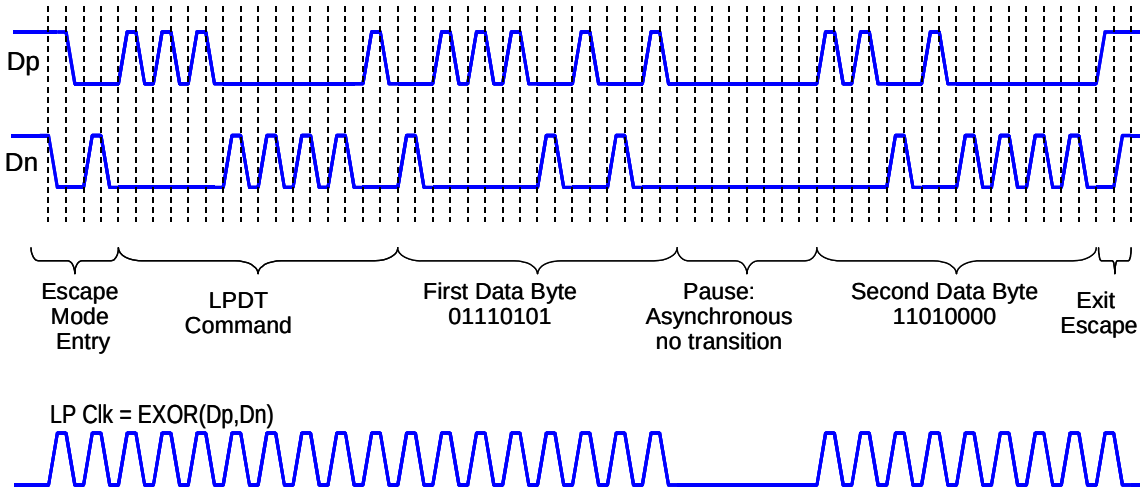


Figure 10-10: Low Power Data Transmission

10.4.10 Reset Trigger

The MCU can inform to the display module that it should be reseted in Reset trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11, LP-10, LP-00, LP-01, LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00, LP-10, LP-11
- Stop State: LP-11

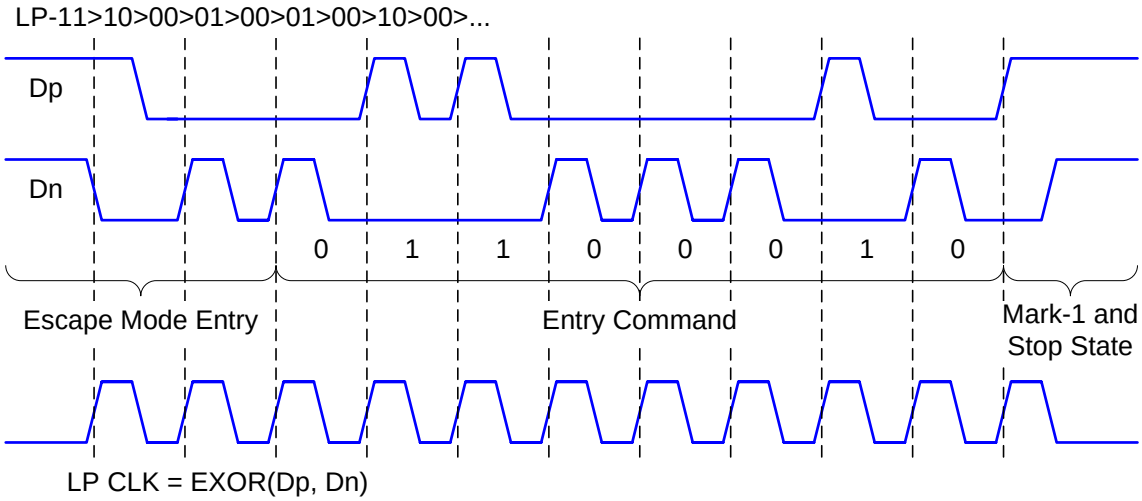


Figure 10-11: Trigger – Reset Command in Escape Mode

10.4.11 Tearing Effect

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11, LP-10, LP-00, LP-01, LP-00
- Tearing Effect: 0101 1101 (First to Last bit)
- Mark-1: LP-00, LP-10, LP-11
- Stop State: LP-11

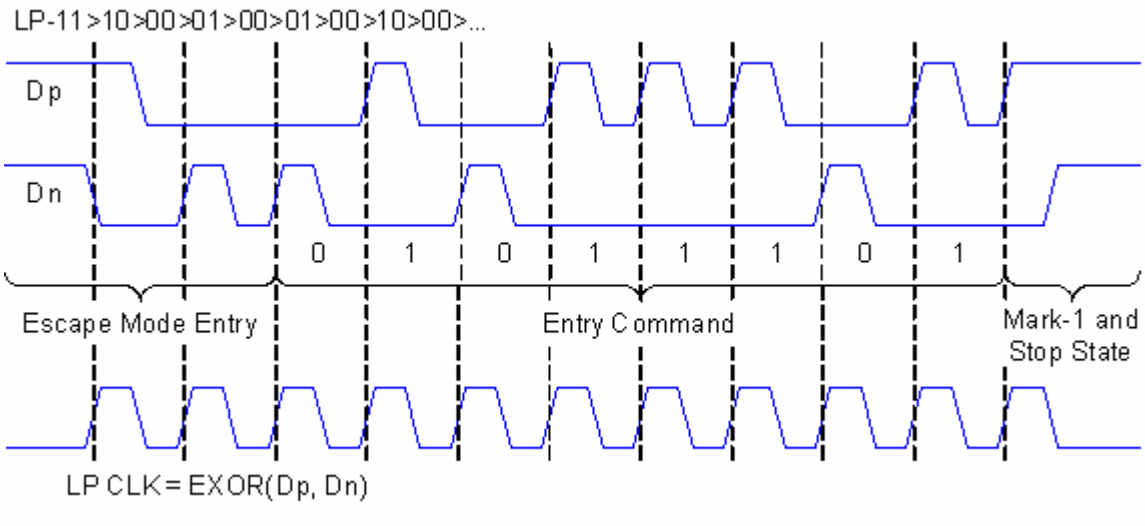


Figure 10-12: Tearing Effect Command in Escape Mode

10.4.12Acknowledge

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK). The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11, LP-10, LP-00, LP-01, LP-00
- Acknowledge (ACK) command: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- Stop State: LP-11

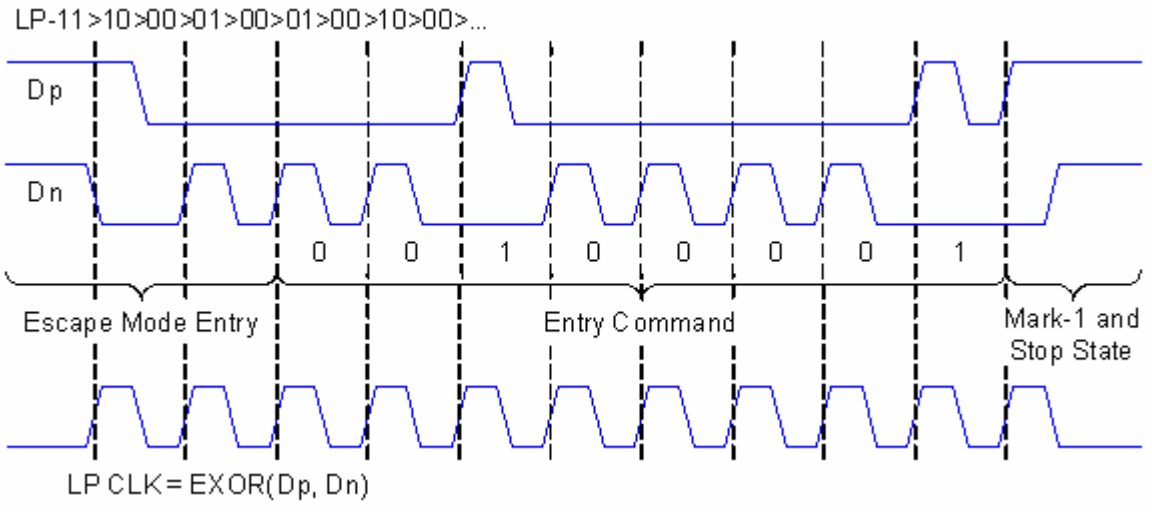
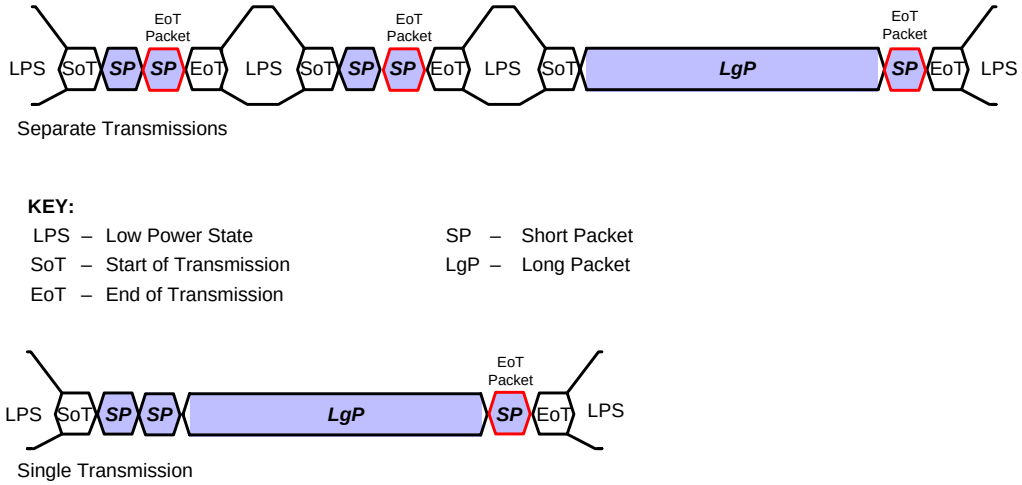


Figure 10-13: Acknowledge Command in Escape Mode

10.4.13 Packet Transmission

SSL MIPI CORE supports two data transmission defined in MIPI DSI specification.

Figure 10-14: Two Data Transmission Mode (Separate, single)



10.4.14 HS Transmission Example

Figure 10-15: One Lane Data Transmission Example

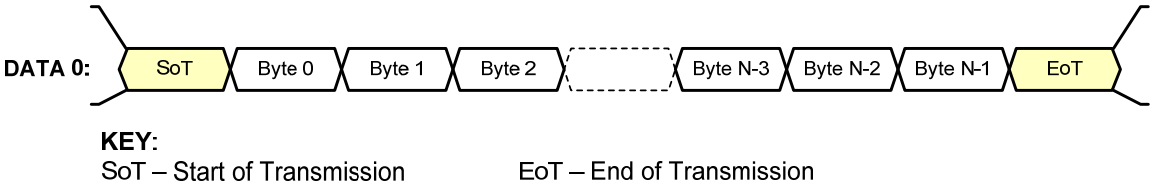
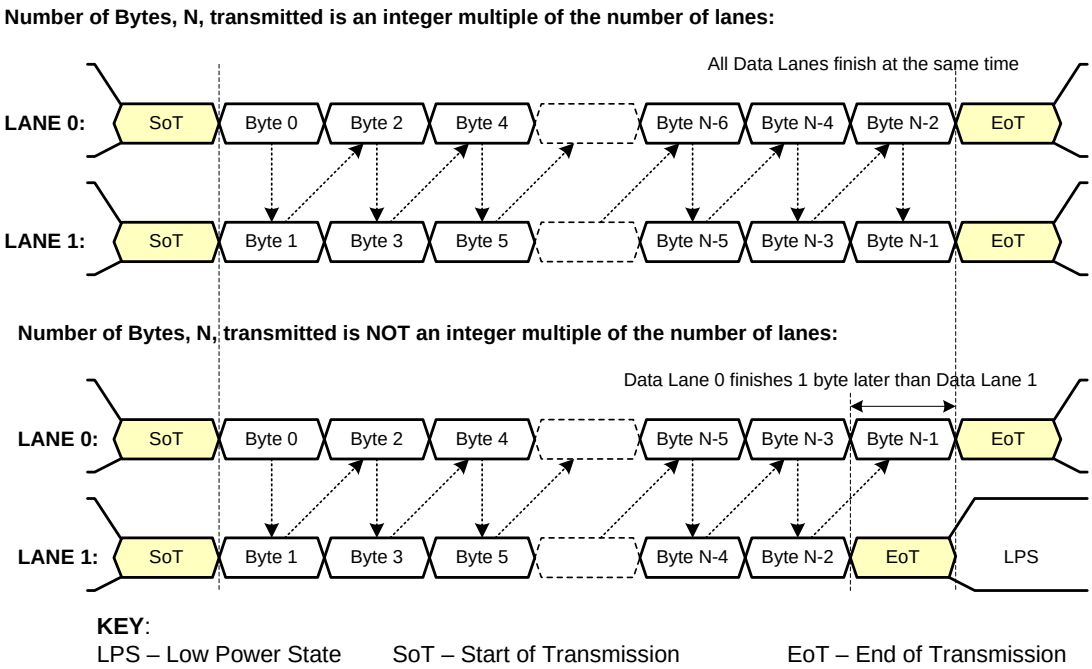


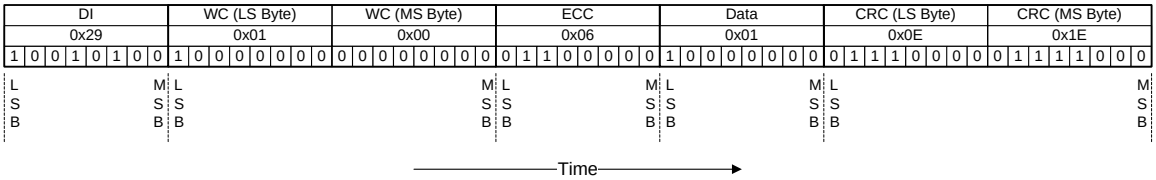
Figure 10-16: Two Lane HS Transmission Example



10.4.15 General Packet Structure

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet. All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

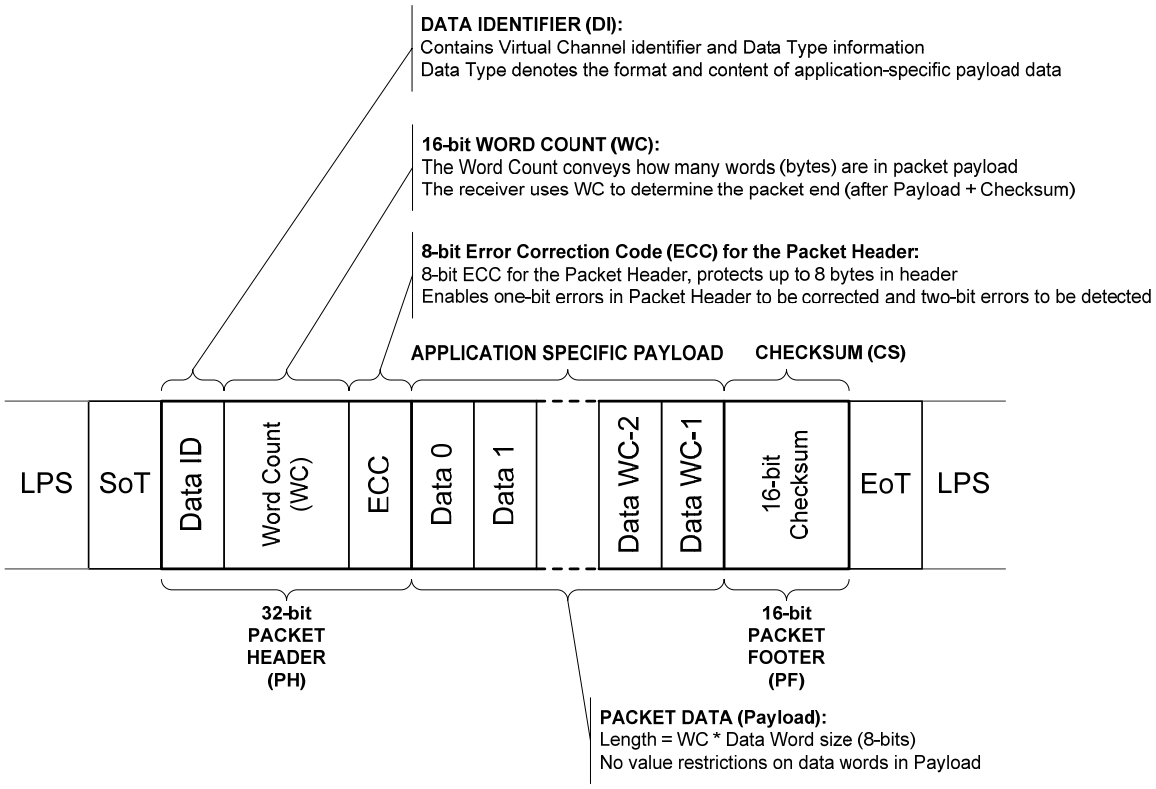
Figure 10-17: Endian Example (Long Packet)



10.4.16 Long Packet Format

Figure 10-18 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

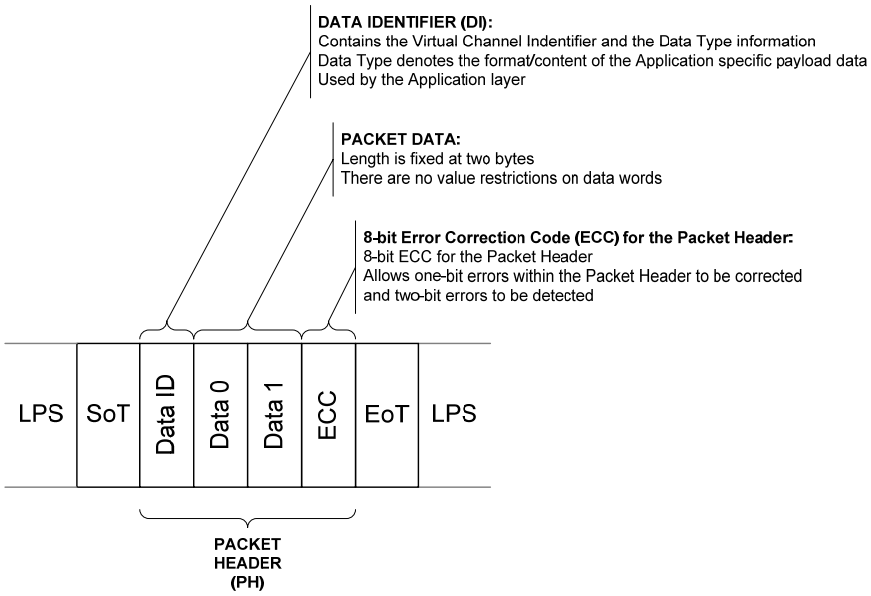
Figure 10-18: Long Packet Structure



10.4.17 Short Packet Structure

Figure 10-19 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

Figure 10-19: Short Packet Structure



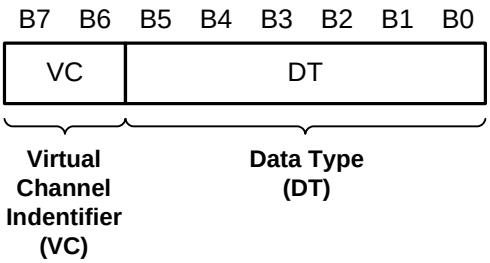
All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Figure 10-17 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

10.4.18 Data Identifier (DI)

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data.

Figure 10-20: Data Indentifier Structure



10.4.19 Victual Channel Identifier (VC)

The VC is the address of the channel between the MCU and the display modules. During the data transactions, both MCU and display module will use the same VC for communication. In SSD2085, the VC for the command mode is 0x02H and the VC for the video mode is 0x01H.

10.4.20 Data Type (DT)

There are two groups of Data Type:

- Processor to Display Module,
- Display Module to Processor

Table 10-11: Data Types for Processor-sourced Packets

Data Type, hex	Data Type, binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission (EoT) packet	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS WRITE, no parameters	Short
15h	01 0101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long

Data Type, hex	Data Type, binary	Description	Packet Size
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x0h and xFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Table 10-12: Data Types for Peripheral-sourced Packets

Data Type, hex	Data Type, binary	Description	Packet Size
00h – 01h	00 000x	Reserved	Short
02h	00 0010	Acknowledge and Error Report	Short
03h – 07h	00 0011 – 00 0111	Reserved	
08h	00 1000	End of Transmission (EoT) packet	Short
09h – 10h	00 1001 – 01 0000	Reserved	
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
13h – 19h	01 0011 – 01 1001	Reserved	
1Ah	01 1010	Generic Long READ Response	Long
1Bh	01 1011	Reserved	
1Ch	01 1100	DCS Long READ Response	Long
1Dh – 20h	01 1101 – 10 0000	Reserved	
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short
23h – 3Fh	10 0011 – 11 1111	Reserved	

Figure 10-21: 16-bit per pixel RGB Color Format, Long packet for MIPI Interface

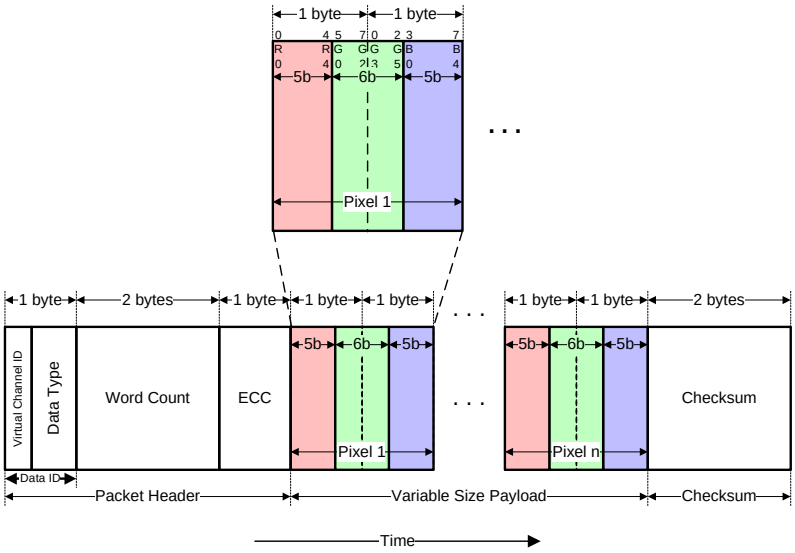


Figure 10-22: 18-bit per Pixel– RGB Color Format, Long packet for MIPI Interface

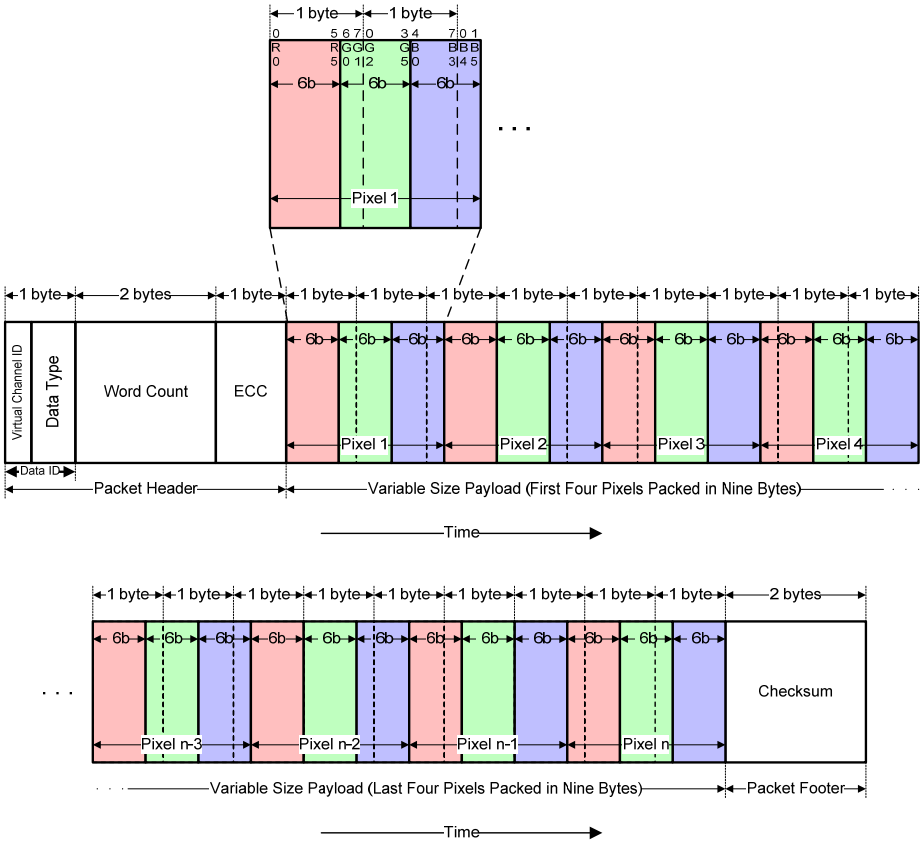


Figure 10-23: 18-bit per Pixel in Three Bytes – RGB Color Format, Long packet for MIPI Interface

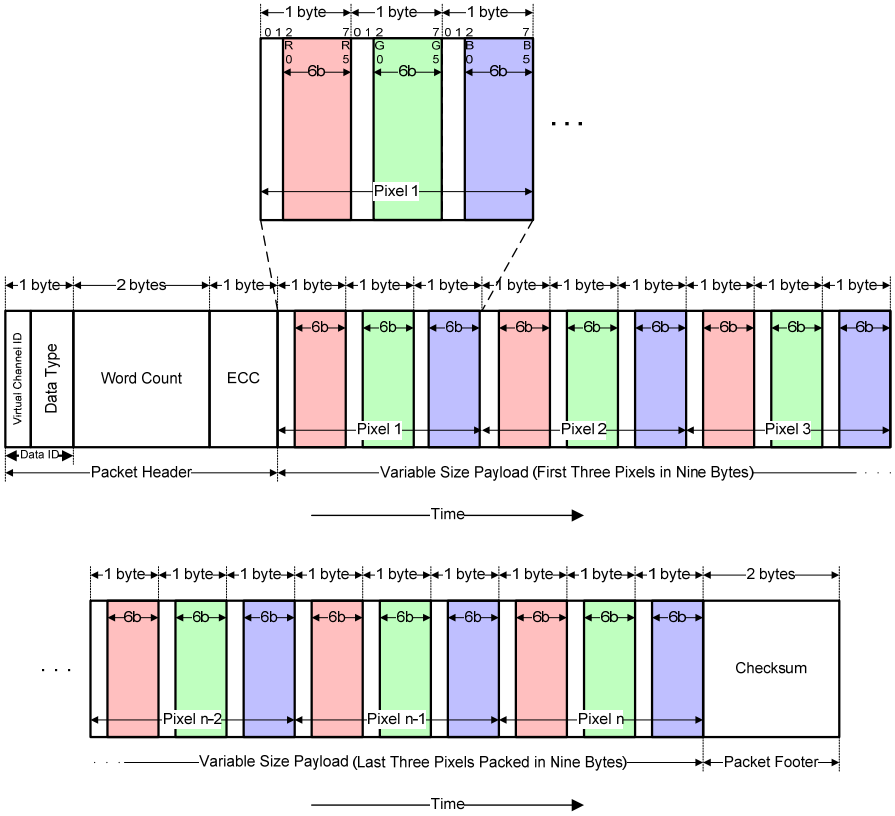
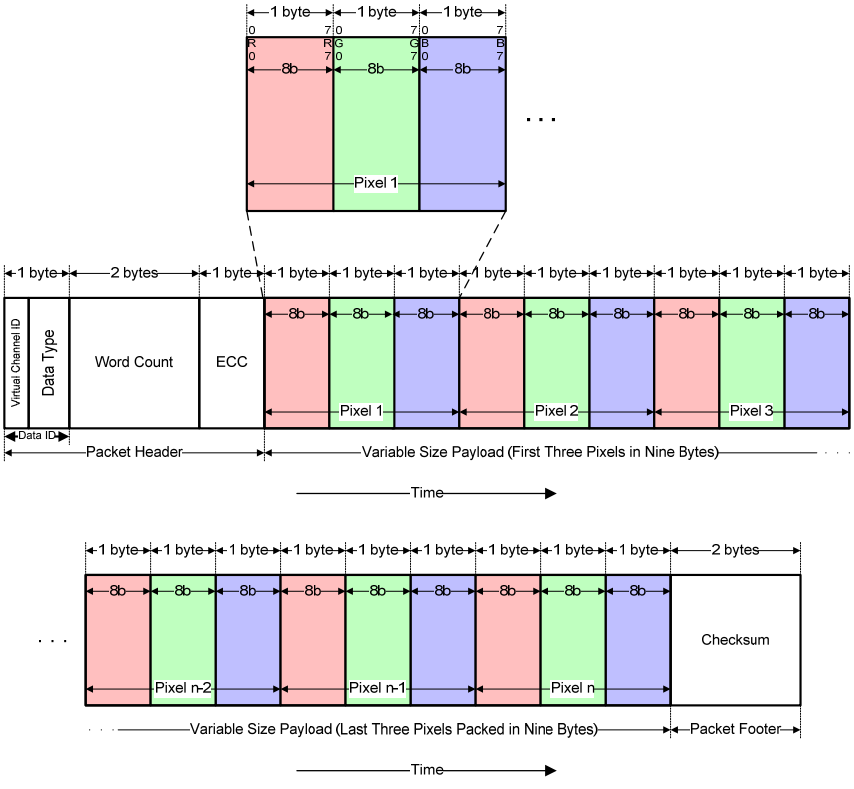


Figure 10-24: 24-bit per Pixel – RGB Color Format, Long packet for MIPI Interface



10.5 Operating Modes

10.5.1 Video Mode

In order to enable the video mode transmission, the user must set if_sel to 0 to select the interface as a combination of RGB and SPI interface. The video data come from the RGB interface and the configuration is done through the SPI interface. To support different bpp settings, the following data pins are used. For all cases, R should be at the upper bits and B should be at the lower bits.

- DATA[15:0] for 16 bpp.
- DATA[17:0] for 18 bpp, packed.
- DATA[17:0] for 18 bpp, loosely packed.
- DATA[23:0] for 24 bpp.

The user, first, needs to program the registers **VICR1** to **VICR6** with correct values. The user also needs to program the **END** and **CO** bits to 0 and 1 respectively. After programming those register fields, the user can turn on the RGB interface and enable the **VEN** bit to start transmission. All three video mode sequence defined in the MIPI DSI specification are supported.

In Non-Burst Mode, the **CSS** (register 0xB7 bit 5) can be set to 0 or 1. When it is set to 1 to select the pclk as PLL reference clock, the PLL multiplication factor should be equal to the bpp value. When it is set to 0 to select the tx_clk as PLL reference clock, the PLL multiplication factor should be set such that the serial link data rte is faster than the incoming data rate. Please refer to the table below for the PLL settings. Registers **VICR1** to **VICR6** (0xB1 to 0xB6) needs to be programmed. (**VICR1** is not used for non-burst mode with Sync Events). (**VICR1** is not used for non-burst mode with Sync Events.) Below is the diagram to illustrate the definition of all the fields.

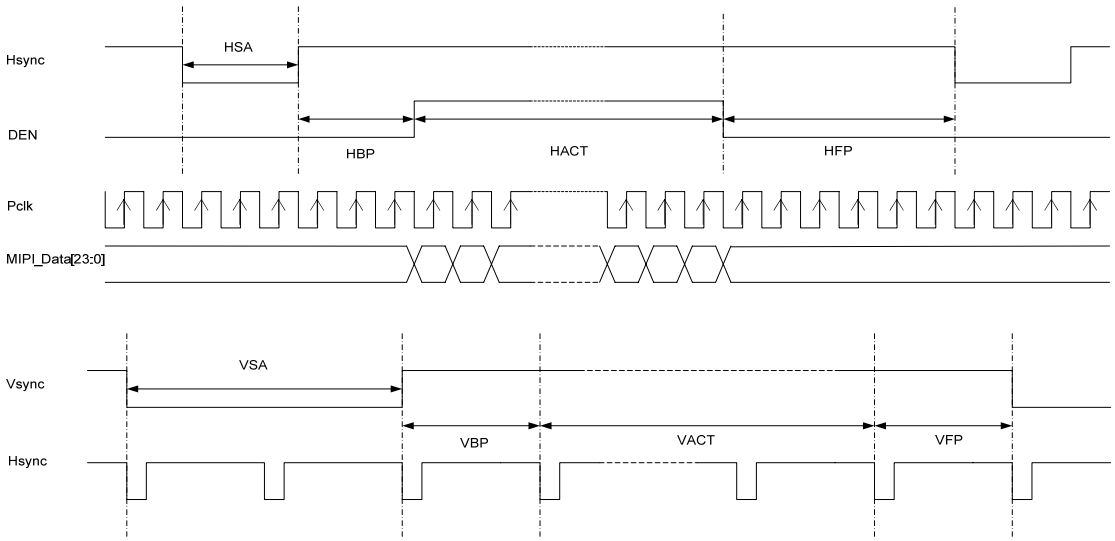


Figure 10-25: Illustration of RGB Interface Parameters for Non-burst Mode with Sync Pulses

Table 10-13: PLL Setting for Non-burst Mode (PLL reference using pclk)

BPP (bit per pixel)	PLL Multiplication Factor		PLL Output Clock Frequency	
	1 data lane	**2 data lane**	**1 data lane**	**2 data lane**
16	16	8	16 x pclk	8 x pclk
18, packed	18	9	18 x pclk	9 x pclk
18, loosely packed	24	12	24 x pclk	12 x pclk
24	24	12	24 x pclk	12 x pclk
	3 data lane	**4 data lane**	**3 data lane**	**4 data lane**
16	5.33	4	5.33 x pclk	4 x pclk
18, packed	6	4.5	6 x pclk	4.5 x pclk
18, loosely packed	8	6	8 x pclk	6 x pclk
24	8	6	8 x pclk	6 x pclk

Table 10-14: PLL Setting for Non-burst Mode (PLL reference using tx_clk)

BPP (bit per pixel)	PLL Multiplication Factor		PLL Output Clock Frequency	
	1 data lane	**2 data lane**	**1 data lane**	**2 data lane**
16	NA	NA	>= 16 x pclk	>= 8 x pclk
18, packed	NA	NA	>= 18 x pclk	>= 9 x pclk
18, loosely packed	NA	NA	>= 24 x pclk	>= 12 x pclk
24	NA	NA	>= 24 x pclk	>= 12 x pclk
	3 data lane	**4 data lane**	**3 data lane**	**4 data lane**
16	NA	NA	>= 5.33 x pclk	>= 4 x pclk
18, packed	NA	NA	>= 6 x pclk	>= 4.5 x pclk
18, loosely packed	NA	NA	>= 8 x pclk	>= 6 x pclk
24	NA	NA	>= 8 x pclk	>= 6 x pclk

In Burst Mode, the **CSS** (register 0xB7 bit 5) needs to be set to 0 to select the tx_clk as PLL reference clock. The PLL multiplication factor should be set such that the serial link data rate is faster than the incoming data rate. Please refer to the table below for the PLL settings. Registers **VICR2** to **VICR6** (0xB1 to 0xB6) needs to be programmed. **VICR1** is not used for this mode. The definition of all the fields is the same as non-burst mode with Sync Events.

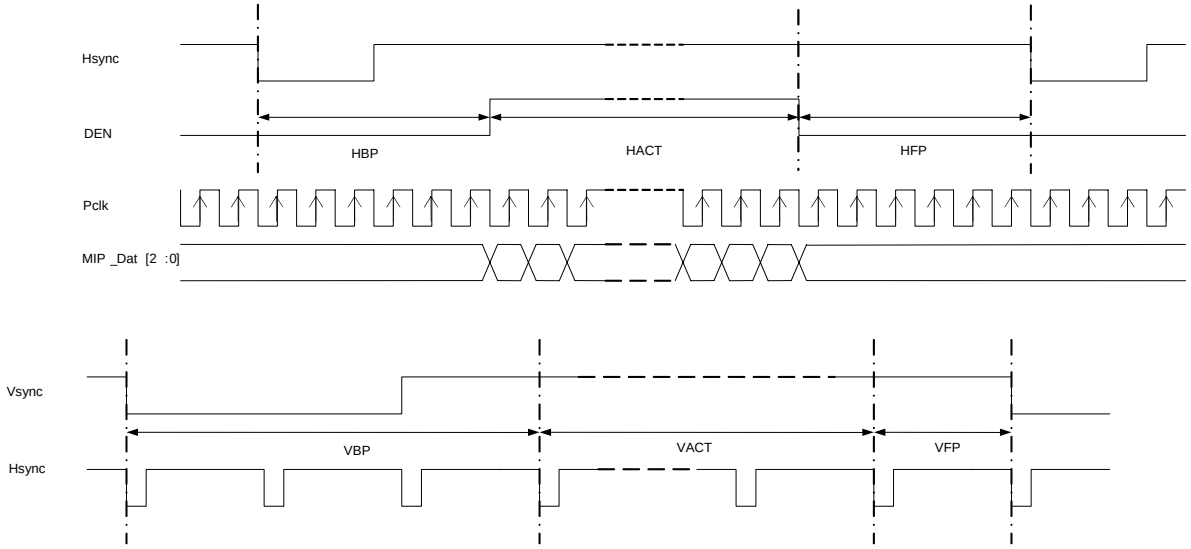


Figure 10-26: Illustration of RGB Interface Parameters for Non-burst Mode with Sync Events and Burst Mode

Table 10-15: PLL Setting for Burst Mode

BPP (bit per pixel)	PLL Multiplication Factor		PLL Output Clock Frequency	
	1 data lane	**2 data lane**	**1 data lane**	**2 data lane**
16	NA	NA	>= 16 x pclk	>= 8 x pclk
18, packed	NA	NA	>= 18 x pclk	>= 9 x pclk
18, loosely packed	NA	NA	>= 24 x pclk	>= 12 x pclk
24	NA	NA	>= 24 x pclk	>= 12 x pclk
	3 data lane	**4 data lane**	**3 data lane**	**4 data lane**
16	NA	NA	>= 5.33 x pclk	>= 4 x pclk
18, packed	NA	NA	>= 6 x pclk	>= 4.5 x pclk
18, loosely packed	NA	NA	>= 8 x pclk	>= 6 x pclk
24	NA	NA	>= 8 x pclk	>= 6 x pclk

*: This value should be set such that the serial link data rate is faster than incoming data rate

The SSD2825 will also monitor the status of CM and SHUT signal. When there is a change of these signals, it will send out appropriate packets. On the rising edge of CM, the CM on packet will be sent. On the falling edge of CM, the CM off packet will be sent. On the rising edge of SHUT, the Shut Down Peripheral packet will be sent. On the falling edge of SHUT, the Turn On Peripheral packet will be sent. With these packets, the MIPI slave will be able to reconstruct the RGB interface signals.

As mentioned, the user can also send command mode data through SPI interface, during the video mode transmission. The data will be sent during the horizontal or vertical blanking period.

10.5.1.1 Write Operation

To perform write operation, the user needs to set the **REN** bit to 0. The SSD2825 can issue four kinds of packets for write operation, which are Generic Short Write Packet, Generic Long Write Packet, DCS Short Write Packet and DCS Long Write Packet. The bit **DCS** controls whether Generic Write Packet or DCS Write Packet will be sent out. The **VC1** or **VC2** field determines the VC ID of the outgoing packets. (Please see the 9.10 for the difference between **VC1** and **VC2**.)

The SSD2825 needs to know the payload size of the outgoing packets. Hence, the user needs to program the corresponding control registers. **PSCR1** and **PSCR2** form the **TDC** field that indicates the total number of payload bytes.

To send a DCS Write Packet, the user needs to write the DCS command/header and the payload to the register **PDR** and **DCS** bit set to 1**.** If the **TDC** field is no more than 2, the SSD2825 will send out DCS Short Write Packet with the correct type. Otherwise, DCS Long Write Packet will be sent out.

To send a Generic Write Packet, the user needs to write the payload to the register **PDR** and **DCS** bit set to 0. If the **TDC** field is no more than 2, the SSD2825 will send out Generic Short Write Packet with the correct type. Otherwise, Generic Long Write Packet will be sent out.

Sometimes, the payload size is too large for SSD2825 to send them out in a single packet. The SSD2825 will automatically partition the payload into a few smaller packets to send out. The **TDC** is used together with the **PST** field to determine the size of outgoing packets. The automatic partition is done differently for DCS Write Packet and Generic Write Packet.

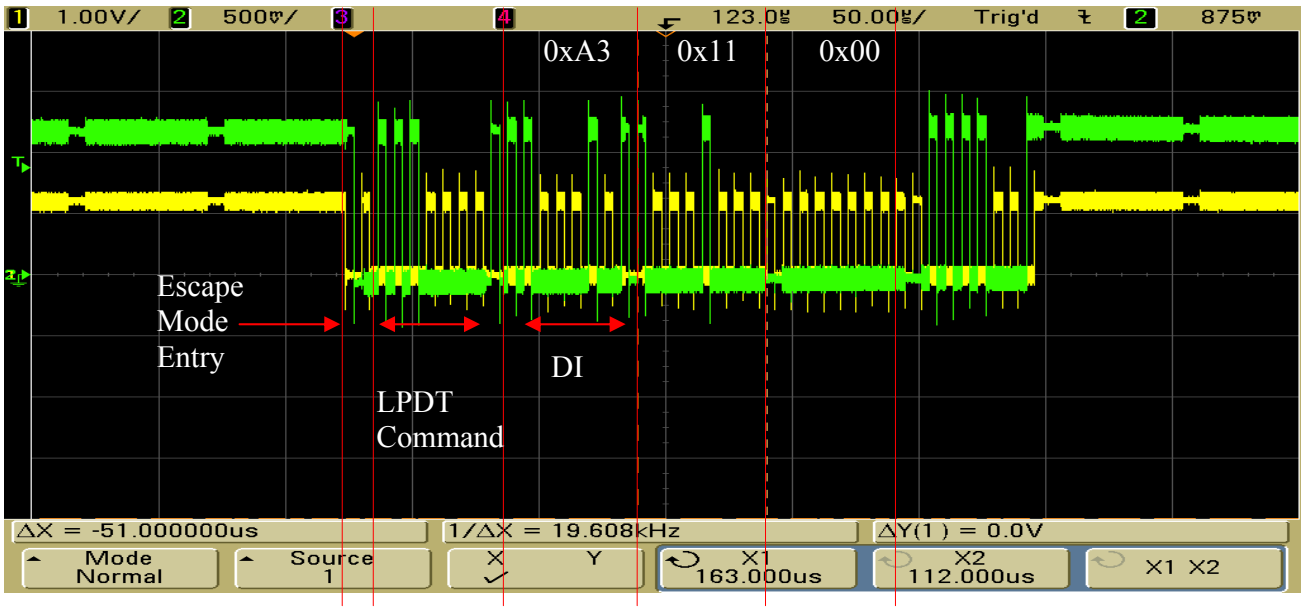
For DCS Write Packet, the partition is only enabled if the DCS command is 0x2C or 0x3C. Otherwise, SSD2825 will not perform automatic partition. (This is because the DCS command 0x2C and 0x3C are to write display data into the LCD panel display memory.) The payload will be partitioned into a few packets where the payload of each packet is (**PST**+1) bytes. The first byte is the DCS command and the following **PST** bytes are the payload. Only the last packet

might contain less payload, as the total payload might not be integer multiple of **PST**. If the incoming DCS command is 0x2C, the DCS command for the first packet is 0x2C and the DCS command for all other packets is 0x3C. If the incoming DCS command is 0x3C, the DCS command of all the packets is 0x3C.

For Generic Write Packet, the payload will be partitioned into a few packets where the payload of each packet is **PST** bytes. Only the last packet might contain less payload, as the total payload might not be integer multiple of **PST**.

For example, if the **TDC** field is 200 and **PST** field is 80, 3 packets will be sent. The first two have 80 bytes of payload. The last packet has 40 bytes of payload.

After performing a write operation, the user can optionally make a BTA to let the MIPI slave report its status. This is done by setting **FBW** bit to 1. The SSD2825 will automatically make a BTA after each write operation.

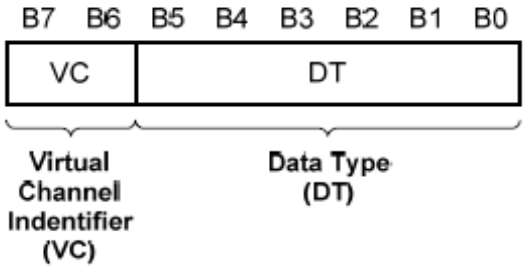


DI = 1010 0011

VC = 10

DT = 10 0011

Generic Short WRITE, 2 parameters



10.5.1.2 Read Operation

To perform read operation, the user needs to set the **REN** bit to 1. The SSD2825 can issue two kinds of packets for read operation, which are Generic Read Packet, and DCS Read Packet. The bit **DCS** controls whether Generic Read Packet or DCS Read Packet will be sent out. The **VC1** or **VC2** field determines the VC ID of the outgoing packets. (Please see the 9.10 for the difference between **VC1** and **VC2**.)

Before the read packet is sent out, the SSD2825 will always send out the Set Maximum Return Size Packet. This is to limit the Read Response Packet sent by the MIPI slave such that there is no over flow. Two factors determine the maximum size. One is the limit of the SSD2825 and the other is the limit of the application processor. The limit of SSD2825 is 4104 bytes of data. The user should choose the smaller one among these two limits to use as the maximum return size.

The parameter in the Set Maximum Return Size Packet is taken from register **MRSR**. The user could program the **MRSR** before every read so that the correct value is sent through Set Maximum Return Size Packet. If the value in the **MRSR** is already the desired value, the user can choose not to program it. The SSD2825 will always automatically send out Set Maximum Return Size Packet using the value in **MRSR**.

To send a DCS Read Packet, the user just needs to write the DCS command (as there is no parameter for DCS read) to PDR register and **DCS** bit set to 1.

To send a Generic Read Packet, the user needs to write the payload to the register **PDR** and **DCS** bit set to 0.

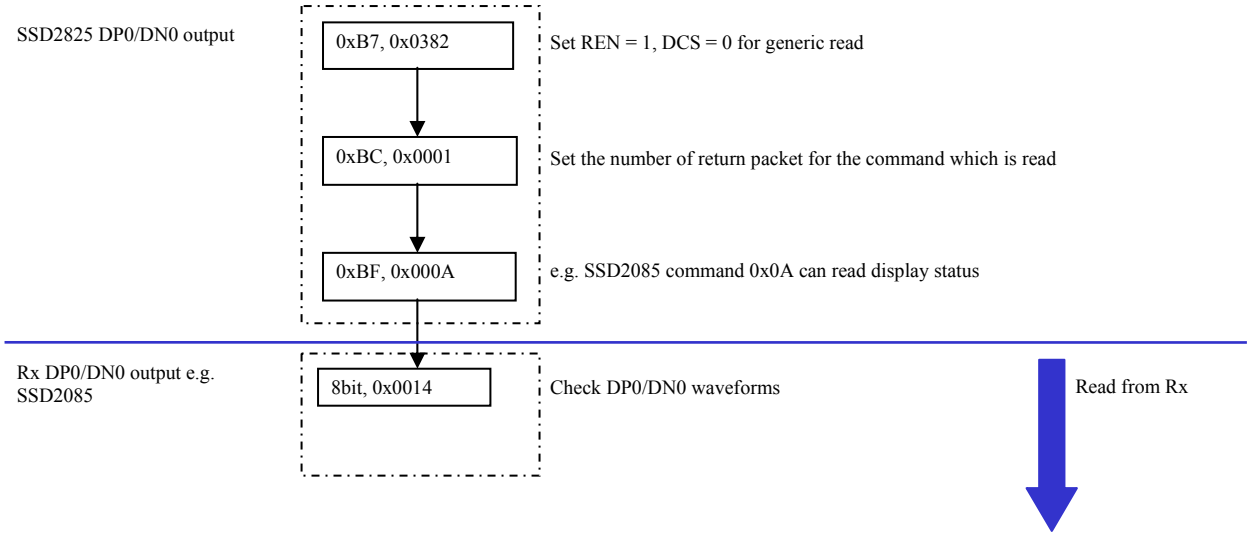
Similar to the write operation, the **TDC** field is used to determine the payload size of the outgoing packet. For DCS Read Packet, the payload is just the DCS command. There is no parameter associated. For Generic Read Packet, the SSD2825 will send out the correct packet type according to the **TDC** value.

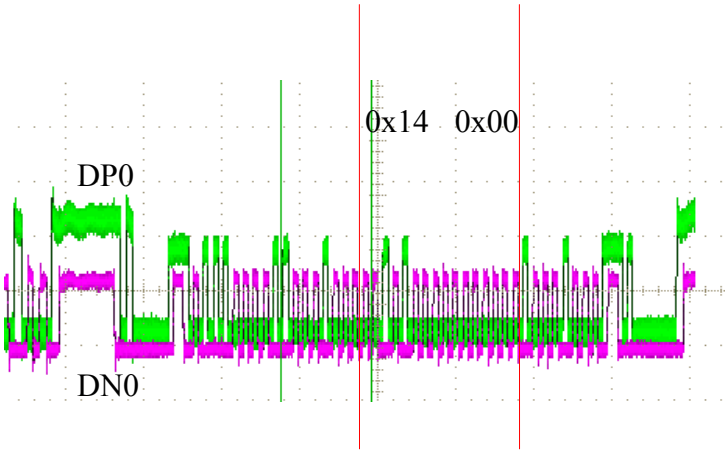
After sending out the read packet, the SSD2825 will automatically perform a BTA to wait for the Read Response Packet from the MIPI slave. The return data will be stored in register **RR**. No matter what read packet is sent out, there is only one packet returning data. Therefore, no matter whether the read is DCS read or Generic read, no matter what command is used in DCS read, the return data is always stored in register **RR**. The user can read the data out when the **RDR** bit is set to 1. After seeing **RDR** bit been set to 1, the user should first read register **RDCR** which contains the number of bytes returned by the MIPI slave. By using this information, the user will know how many data should be read out from register **RR**. After all the return data are read out, the **RDR** bit will be set to 0 by the SSD2825.

After the **RDR** bit been set to 1, the user can choose not to read the data out from register **RR**. The user can continue performing another operation. Once the user does so, the **RDR** bit will be set to 0 by the SSD2825.

There might be Acknowledge and Error Report Packet sent by the MIPI slave at the same time. The operation of acknowledgement handling is described in 0.

Under certain circumstance, the MIPI slave might only send back Acknowledge and Error Report Packet without any data. Thus, the **RDR** bit will not be set. Therefore, it is recommended that the user check the bit **BTAR** first. The **BTAR** is to indicate whether the MIPI slave has passed the bus authority back to the SSD2825 or not. Only when the **BTAR** is 1, there might be return data. If there is no return data, the user should follow 0 to handle the acknowledgement.


SSD2825 DP0/DN0 output
0xB7, 0x0382
Set REN = 1, DCS = 0 for generic read
0xBC, 0x0001
Set the number of return packet for the command which is read
0xBF, 0x000A
e.g. SSD2085 command 0x0A can read display status
Rx DP0/DN0 output e.g. SSD2085
8bit, 0x0014
Check DP0/DN0 waveforms
Read from Rx


0x14
0x00
DP0
DN0

10.5.1.3 Acknowledgement Operation

The SSD2825 can perform a BTA to give the bus authority to the MIPI slave and let it report its status. The BTA can be enabled by setting **FBW** bit to 1 and performing a write operation, or just performing a read operation. After the MIPI slave passes the bus authority back, the SDD2805 will set bit **BTAR** to 1.

If there is no error on the slave side, the MIPI slave will return ACK trigger message, if the packet before BTA is a write packet. The MIPI slave will return Read Response Packet, if the packet before BTA is a read packet. In this case, after receiving the response from the MIPI slave, SSD2825 will set bit **ARR** and **ATR** bits to 1. **ARR** indicates that response has been received from MIPI slave. **ATR** indicates that the MIPI slave has reported no error with ACK trigger message. Consequently, the register **ARSR** will be cleared to 0.

If there is error on the slave side, the MIPI slave will return Acknowledge and Error Report packet, if the packet before BTA is a write packet. The MIPI slave will return Read Response Packet (depending on the error type) and Acknowledge and Error Report Packet, if the packet before BTA is a read packet. In this case, after receiving the response from the MIPI slave, SSD2825 will set bit **ARR** bit to 1 and **ATR** bits to 0. **ARR** indicates that response has been received from MIPI slave. **ATR** indicates that the MIPI slave has sent Acknowledge and Error Report Packet instead of ACK trigger message. Therefore, the MIPI slave has reported error. The error reported by the MIPI slave will be stored in register **ARSR**. The user can read this register to see what error the MIPI slave has encountered.

For the detailed description of each error bit, please refer to MIPI DSI specification. Below are the flow charts of handling the MIPI slave acknowledgement. They are just for reference.

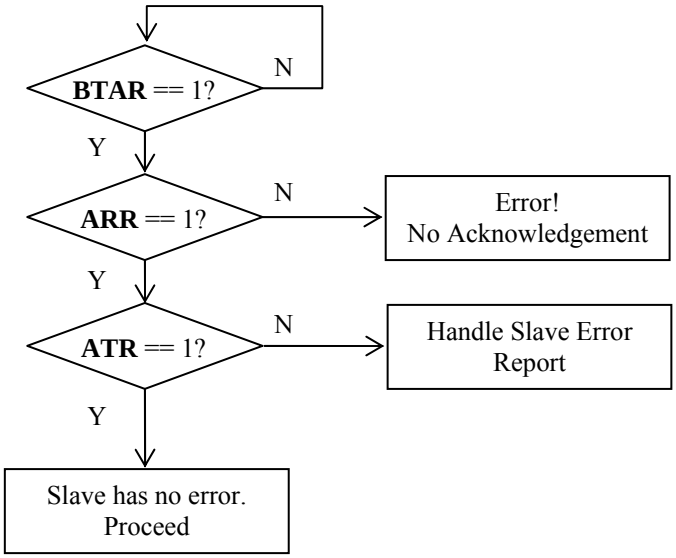


Figure 10-27: Acknowledgement Handling after Non-Read Command

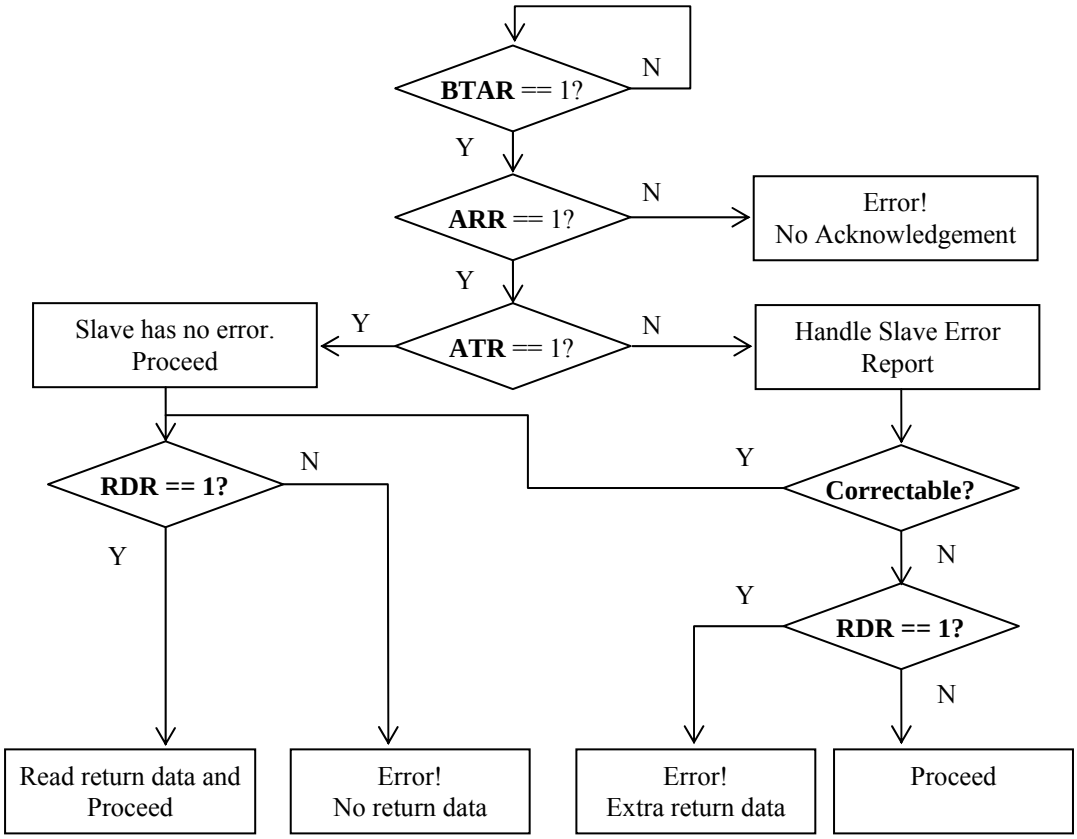
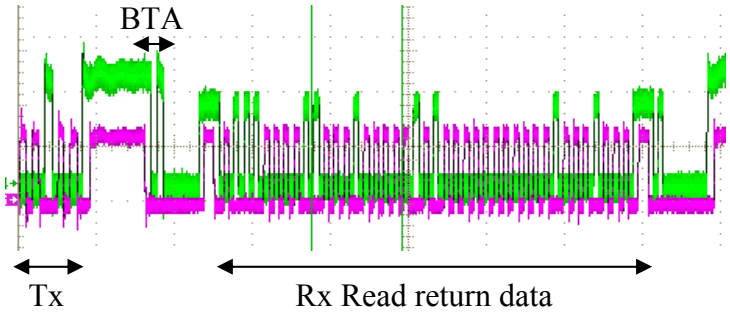


Figure 10-28: Acknowledgement Handling after Read Command



Remark: LP clock of Rx must be within 10% of Tx LP clock

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 10-16: MIPI error report

10.5.1.4 Tearing Effect (TE) Operation

The TE operation is to perform a BTA following the previous BTA without transmitting anything in between. The bus is handed to the MIPI slave for providing TE information. After getting the TE event from display driver, the MIPI slave will pass the bus authority back to the SSD2825 by using BTA trigger message.

The TE operation can be enabled by setting bit **FBT** and **FBW** to 1 before writing the last command to the MIPI slave. Afterwards, the application processor can instruct the SSD2825 to send out the last command in a write packet. Since **FBW** is 1, the SSD2825 will automatically perform a BTA after the write operation. The MIPI slave will response and pass the bus authority back. Since **FBT** is 1, the SSD2825 will perform another BTA without sending any data. This makes the MIPI slave enter TE mode.

The MIPI slave will send a TE trigger message back when it gets the TE event. After getting the trigger message, the SSD2825 will set the TE pin to 1 to indicate that TE event has been received. DATA[16] is used as the TE pin. At the same time, bit **TER** will be set to 1. The application processor can write 1 to this bit to clear it. As the TE trigger message only determines when the TE pin will be set to 1, a counter is used to determine when to set the TE pin to 0. The TE pin will be set to 0, once the counter reaches the value in **TEC**. The counter uses the reference clock to do counting.

If the MIPI slave does not send back the TE trigger message but just perform a BTA to pass the bus back, the SSD2825 will automatically perform another BTA to pass the bus to the MIPI slave again. It will continue do so until the MIPI slave respond with the TE trigger message, or the **FBT** bit is set to 0, or the LP RX timer expires.

If the MIPI slave does not send back the TE trigger message and still holds the bus, the user can set the bit **FBC** to 1 to force a bus contention. After bus contention is resolved, the slave will pass the bus back to SSD2825.

10.5.1.5 Contention Detection and Timer Operation

Two timers have been defined in SSD2825 to resolve the potential contention issue on the bus. The two timers are the HS TX timer and LP RX timer. Please see the register description for the detailed usage.

Whenever the SSD2825 sees a contention being detected, it will reset the state machine and enter the default mode, which is LP TX idle mode. The data line will be kept at LP11.

10.5.1.6 Interrupt Operation

An interrupt signal int_0/int_1 has been provided to interrupt the application processor so that it does not need to poll the status all the time. This will save the processing time of the application processor. int_0/int_1 is an active low signal, in other words, when the event has happened, it will go low.

There are many sources that can be mapped to the interrupt signal. The user can select different source to perform different task. If more than 1 source is selected, the int_0/int_1 signal will go low when the event for 1 of the sources has happened. In this case, the user needs to read the register **ISR** to determine what event has happened. The different sources can be enabled/disabled through register **ICR**. Below is the list of available interrupt sources and their usage.

RDR

To indicate that return data from MIPI slave is available for read.

BTAR

To indicate whether the SSD2825 has the bus authority or not. It can be used after SSD2825 makes a BTA. If the MIPI slave has returned the bus authority back to SSD2825, the interrupt will be set to indicate so. Please note that, on power up, the bus authority is already on the SSD2825. Hence, the SSD2825 will show that it has the bus authority.

ARR

To indicate whether the SSD2825 has received the acknowledge response from the MIPI slave. The acknowledge response can either report error or not error. This is to be determined by the **ATR** bit.

The above three interrupts are provided to the user to handle reading data from the MIPI slave or getting acknowledgement response from the MIPI slave.

PLS

To indicate whether the PLL has been locked or not. If the PLL is not locked, the programming speed at the external interface must be slow. After changing the PLL setting or changing the reference clock source, the user also needs to use this interrupt to determine the PLL status.

On power up, only **PLS** interrupt is enabled. This is to let the user determine the programming speed before configuring the SSD2825.

LPTO

To indicate that there is LP RX time out.

HSTO

To indicate that there is HS TX time out.

The above two interrupts are provided to the user for error handling.

PO

To indicate whether the SSD2825 is ready to accept any data from the user. The SSD2825 has several internal buffers to hold the data written by the user. When the user writes after than the serial link speed, those buffers will be full. If the user still writes data to SSD2825, those data will be lost. The length of the payload of the next packet that the user is going to write is determined by **TDC**, **PST**, and **DCS** fields. The SSD2825 will use these fields to decide whether the user can write the next packet or not. Hence, after programming the above mentioned fields, the user needs to check the interrupt status before writing.

SE, SA, SLE, SLA, MLE, MLA

All these interrupts are provided to indicate the status of the internal data buffers. They are used if the user is familiar with the buffer management of the SSD2825. Otherwise, it is recommended to use the **PO** interrupt.

One important thing to note is the interrupt latency. The output interrupt signal does not change immediately after an operation. This is due to the internal processing of the SSD2825. For example, after changing the interrupt source from one to another, the output int_0/int_1 level will remain at the old level for a short period after the programming is done. Another example is that after programming the **TDC** field, the interrupt will take a short period to reflect the correct **PO** status on int_0/int_1. There is always a delay between the actual event and the interrupt.

In order to guarantee that the user can get the correct interrupt, it is recommended that the user performs a read of any SSD2825 local register before taking in the interrupt signal or polling the interrupt status bits. The read operation will cover the interrupt latency period. Alternatively, the user can wait for certain amount of time to make sure the interrupt reflects the true status. Below is a diagram for illustration.

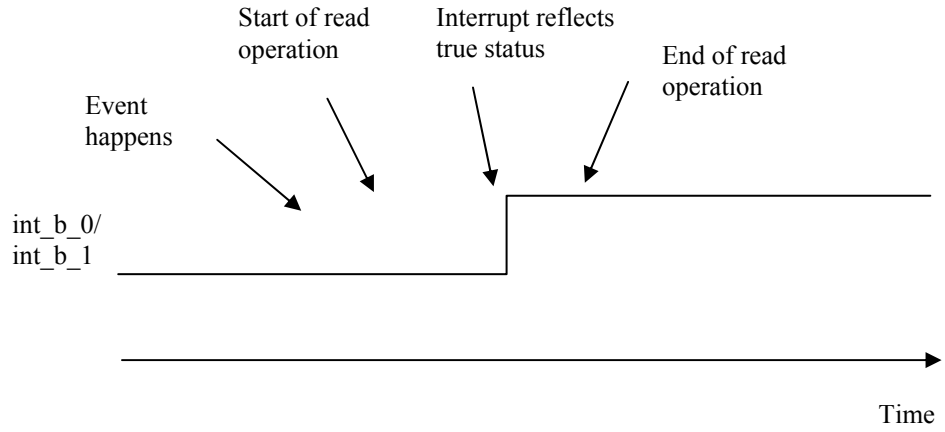


Figure 10-29: Illustration of Interrupt Latency

10.5.1.7 Internal Buffer Status

There are totally 5 data buffers inside the SSD2825, which are MCU interface long buffer (ML0) for DSI_0, SPI interface long buffer (LL0) for DSI_0, SPI interface long buffer (LL1) for DSI_1, MCU/SPI interface short buffer(SB0) for DSI_0, MCU/SPI interface short buffer(SB1) for DSI_1.

The ML0, SB0 and SB1 buffers are used to store the data written through MCU and RGB interface. However, since there is no flow control for the RGB interface, the status is only valid for MCU interface.

The LL0, LL1, SB0 and SB1 buffers are used to store the data written through SPI interface.

For SB buffers, any packet with payload of no more than 8 bytes will be stored into them. They can store 8 such packets respectively. Below is a list of possible packets

- Generic Short Write Packet
- Generic Read Packet
- DCS Short Write Packet
- DCS Read Packet
- Generic Long Write Packet (TDC<=8 bytes)
- DCS Long Write Packet (TDC<=8 bytes. There is one byte for DCS command.)

These buffers are used to hold the packets which are usually used to configure the MIPI slave or the display driver.

For ML and LL buffers, any packet with payload of more than 8 bytes will be stored into them. They can store 2 such packets. The maximum size of ML and LL buffer is 4159 bytes and 511 bytes respectively. They are used to hold

- Generic Long Write Packet
- DCS Long Write Packet

In case of automatic partitioning, the packet length is determined by the **PST** field. It is not recommended to make the **PST** field so small that the packet will be put in MS or LS buffers, as it is a waste.

The user can write the data through SPI interface. With the information above, the user knows whether the next packet will be written into LL or SB buffers. Hence, the user needs to check the corresponding interrupts. The usage of the interrupts is listed below.

SE

To indicate that the short buffer is empty. Since the short buffer can hold 8 packets, the user can write up to 8 such packets into short buffer without needing to look at the interrupt status.

SA

To indicate that the short buffer can hold at least 1 more packet. The user can write 1 such packet into short buffer.

SLE

To indicate that SPI long buffer is empty. Since the SPI long buffer can hold 2 packets, the user can write up to 2 such packets into SPI long buffer without needing to look at the interrupt status.

SLA

To indicate that the SPI long buffer can hold at least 1 more packet. The user can write 1 such packet into LL buffer.

The user can also write the data through MCU interface. With the information above, the user knows whether the next packet will be written into ML or SB buffers. Hence, the user needs to check the corresponding interrupts. The usage of the interrupts is listed below.

MLE

To indicate that ML buffer is empty. Since the ML buffer can hold 2 packets, the user can write up to 2 such packets into ML buffer without needing to look at the interrupt status.

MLA

To indicate that the ML buffer can hold at least 1 more packet. The user can write 1 such packet into ML buffer.

The 6 interrupts mentioned here can be used as flow control between the application processor and the SSD2825. However, it requires the user to know the buffer operation well. The **PO** interrupt is a combination of the six. It makes decision according to the parameters provided by the user for the next packet to be written. Hence, the user does not need to know which buffer is going to be used and how the buffer status is.

10.5.2 State machine operation

The state machine controls the sending and receiving of the data packet over the serial link. It is triggered by an event from the application processor or the received data. Once a complete packet is written into the SSD2825 buffer, it will send it out through the serial link. The user can write 1 to bit **COP** at any time to cancel all the current operations. Please see 9.19 for the description.

When the SSD2825 is in high speed mode, the serial link is mainly used to send display data. If there is no data to send, it will send null packet to maintain the serial link timing. If the application processor does not have display data to send in a long period, it can turn the serial link into low power mode by setting the register bit **HS** to 0.

When the SSD2825 is in low power mode, the serial link is mainly used to send command and configuration data. If there is no data to sent, the SSD2825 will be idle in LP TX stop mode.

The user can also enter sleep mode by writing 1 to **SLP** bit. Once the **SLP** bit is set to 1, the SSD2825 will automatically enter LP mode. If the **HS** bit is 1, the SSD2825 will clear the **HS** bit to 0 and switch from HS to LP mode. Afterwards, the SSD2825 will issue ULPS trigger message to the MIPI slave to enter Ultra Low Power State. During this state, the clock to SSD2825 can be switched off such that the SSD2825 only consumes leakage current. This will save the overall system power consumption. When exiting from the ULPS, the user can write 0 to **SLP** bit. However, the user should be aware that the time to exit from ULPS is relatively long (pleaser refer to MIPI DPHY specification). Hence, the user cannot perform any data transmission before the system exits from ULPS.

During reception, the state machine will disassemble the incoming data packet and put the received register content into the internal buffer for reading out. Once all the data are put into the buffers, it will set the register bit **RDY** to 1 to indicate that the SSD2825 is ready for read. The total number of received bytes will also be stored in **RDCR**.

After the reception is completed, the SSD2825 will perform a bus turn around to enter the transmission mode. It will always come back to the LP TX stop mode before it enters any other mode.

10.5.3 D-PHY operation

D-PHY controls the operation of the analog transceiver. It controls whether the serial link is in high speed or low power mode and whether it's in transmit or receive mode.

In transmit mode, the D-PHY will perform the handshaking procedure when switching between LP mode and HS mode according to the control from PCU. During HS mode, D-PHY will provide parallel data and clock to the analog transmitter for transmitting in differential signals serially. During LP mode, D-PHY will directly drive the Datap and Datan line output. It will provide serial data to the analog transmitter.

In receive mode, D-PHY will detect the handshaking sequence in LP mode and inform the PCU. Once entering escape mode, it will collect the serial data from analog receiver and put them in byte form for the PCU to process.

Various timing parameter has been defined in MIPI DPHY specification. The timing parameters are a mixture of absolute time and cycle counts. Hence, for different operation speed, there is different timing requirement. Registers **DAR1** to **DAR6** are provided for this purpose. The user can adjust the value in these registers to have different DPHY timing parameters. This gives maximum flexibility for different operation speed.

10.5.4 Analog Transceiver

10.5.5 PLL

The PLL output frequency is calculated by the equations below,

$$f_{PRE} = \frac{f_{IN}}{MS}$$
$$f_{OUT} = f_{PRE} * NS$$

where the f_{IN} is the input reference clock frequency and f_{OUT} is the output clock frequency of the PLL.

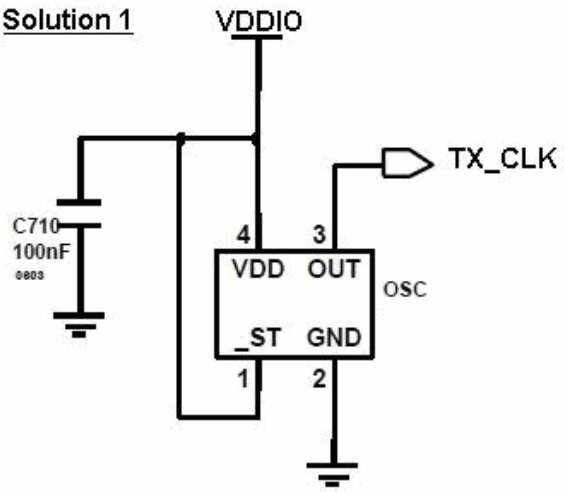
The clock frequencies need to satisfy the constraint below.

$$5MHz > f_{IN} \geq 100MHz$$
$$5MHz > f_{REF} \geq 100MHz$$
$$62.5MHz > f_{OUT} \geq 1000MHz$$

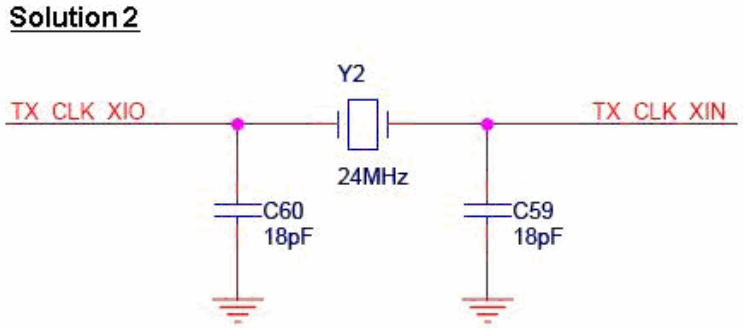
The value of FR, MS, and NS are controlled in the register **PLCR**.

All the values of FR, MS and NS can only be modified when the PLL is turned off. Hence, the sequence for modification is to turn off PLL, modify register value, and turn on PLL.

10.5.6 Clock Source Example



Pin	Connection
TX_CLK_XIN	VDDIO/GND
TX_CLK_XIO	VDDIO
TEST2	GND
TEST1	GND
TEST0	GND



Pin	Connection
TX_CLK	VDDIO
TEST2	GND
TEST1	GND
TEST0	VDDIO

11 External Interface

The SSD2825 supports three types of MCU interface,

- Type A, fixed E mode, DBI 2.0
- Type A, clocked E mode, DBI 2.0
- Type B, DBI 2.0

three types of SPI interface,

- 8 bit 3 wire (type C option 1, DBI 2.0)
- 8 bit 4 wire (type C option 3, DBI 2.0)
- 24 bit 3 wire

and RGB interfaces.

The selection is controlled by ps[4:0], if_sel and if_sel2 pins.

MCU interface supports both 8 bit, 16 bit and 24 bit data bus. Below are the data pins used for each interface. For 8 bit interface, the least significant byte should be written first. For 16 or 24 bit interface, the lease significant word should be written first.

- data[7:0] for 8 bit interface.
- data[15:0] for 16 bit interface.
- data[23:0] for 24 bit interface.

RGB interface supports 4 bpp settings. Below are the data pins used for each interface. For all cases, R should be at the upper bits and B should be at the lower bits.

- data[15:0] for 16 bpp.
- data[17:0] for 18 bpp, packed.
- data[17:0] for 18 bpp, loosely packed.
- data[24:0] for 24 bpp.

SPI interface supports 8 bit data bus. The least significant byte should be written first.

Below is the operation and timing diagram for each of the interfaces.

11.1 MCU Interface Type A, fixed E mode

This interface consists of data[23:0], rwx, dcx, e and csx0 or csx1. It supports 24 bit, 16 bit and 8 bit data bus. The first cycle should be a command write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

e should be driven to 1 in this mode.

rwx indicates whether the operation is a read or a write operation. When rwx is 1, the operation is a read operation. When rwx is 0, the operation is a write operation.

During write operation, dcx indicates whether the operation is for data or command. When dcx is 1, the operation is for data. When dcx is 0, the operation is for command. During the read operation, the dcx should be 1.

During the write operation, data[23:0] are sampled at the rising edge of csx0 or csx1. During read operation, data[23:0] are provided at the falling edge of csx0 or csx1 and the application processor should use the rising edge of csx0 or csx1 to sample.

Below is a diagram for illustration. Please see section **Error! Reference source not found.** for the detailed waveform and timing parameters.

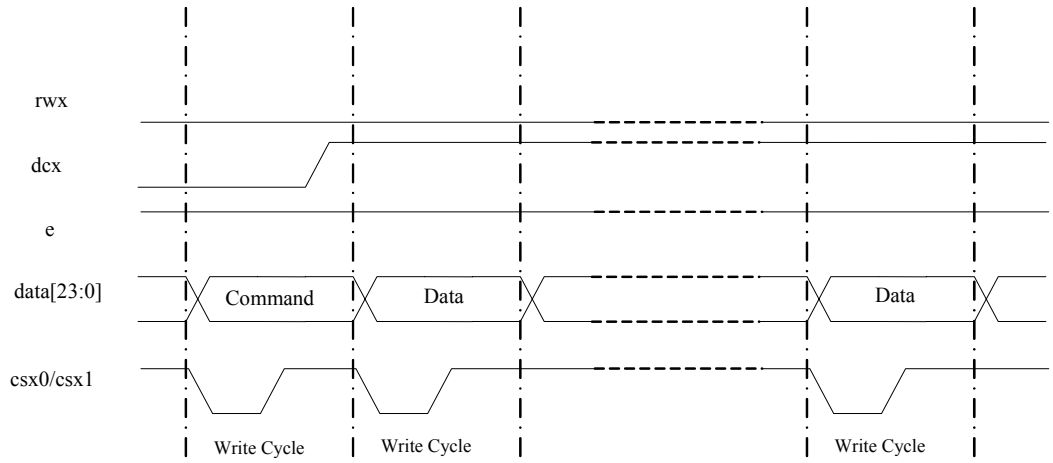


Figure 11-1: Illustration of Write Operation for Type A, Fixed E Mode Interface

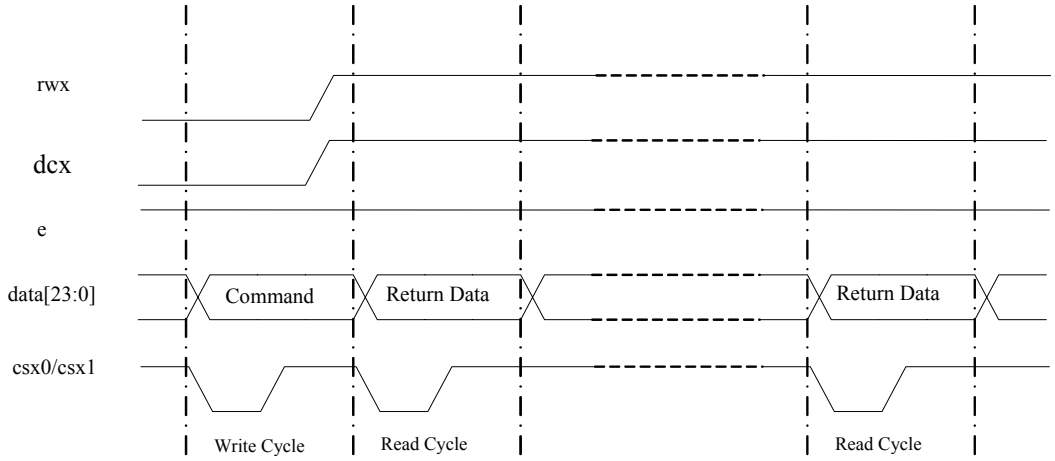


Figure 11-2: Illustration of Read Operation for Type A, Fixed E Mode Interface

11.2 MCU Interface Type A, Clocked E Mode

This interface consists of data[23:0], rwx, dcx, e and csx0 or csx1. It supports 24 bit, 16 bit and 8 bit data bus. The first cycle should be a command write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

csx0 or csx1 should be driven to 0 in this mode.

rwx indicates whether the operation is a read or a write operation. When rwx is 0, the operation is a write operation. When rwx is 1, the operation is a read operation.

During write operation, dcx indicates whether the operation is for data or command. When dcx is 1, the operation is for data. When dcx is 0, the operation is for command. During the read operation, the dcx should be 1.

During the write operation, data[23:0] are sampled at the falling edge of E. During read operation, data[23:0] are provided at the rising edge of e and the application processor should use the falling edge of e to sample.

Below is a diagram for illustration. Please see section **Error! Reference source not found.** for the detailed waveform and timing parameters.

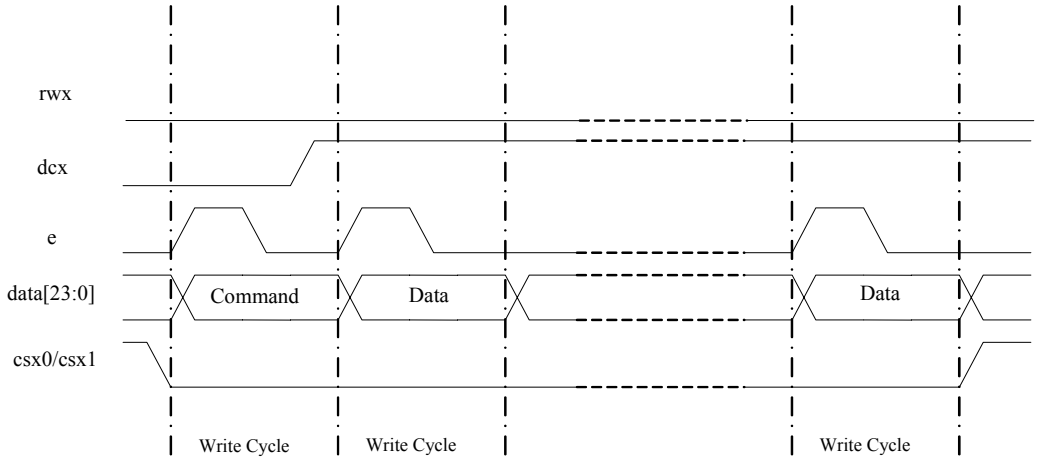


Figure 11-3: Illustration of Write Operation for Type A, Clocked E Mode Interface

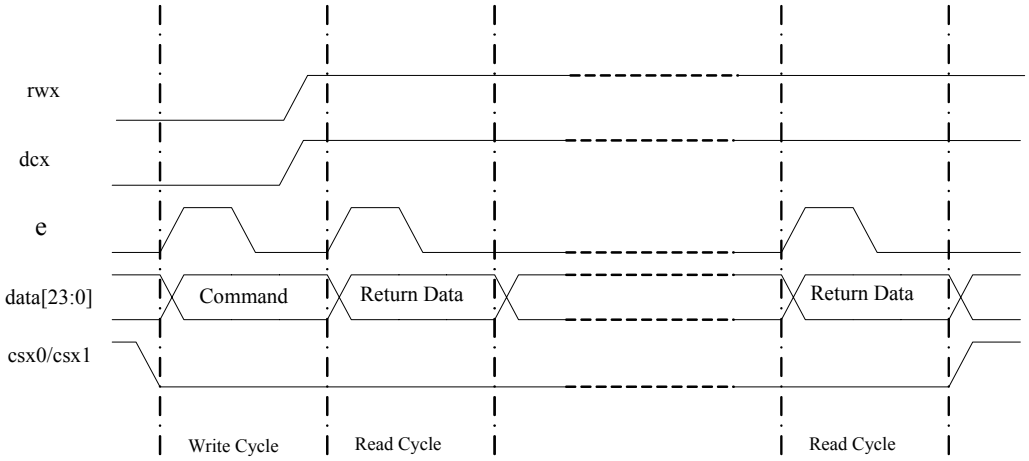


Figure 11-4: Illustration of Read Operation for Type A, Clocked E Mode Interface

MCU Interface Data Pin Mapping for Command Cycle

In the first write cycle, only 8 bit data are written into the SSD2825, as the command can only be 8 bit. No matter whether the interface is 8, 16 bit or 24 bit, lower 8 bits are used. Please refer to the table below.

Interface	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24 bit	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	C7	C6	C5	C4	C3	C2	C1	C0
16 bit									x	x	x	x	x	x	x	x	C7	C6	C5	C4	C3	C2	C1	C0
8 bit																	C7	C6	C5	C4	C3	C2	C1	C0

In the sub sequent read or write cycles, command parameters can be written into the SSD2825. Depending on the interface width, different data pin mapping is adopted. Please refer to the table below.

When the parameter is odd number of bytes and interface width is 16 bit, the last byte should be put on data[7:0].

Table 11-1: MCU Interface Data Pin Mapping for Parameter Cycle

Interface	Cycle	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24 bit	1st	Parameter [23:0]																							
	2nd	Parameter [47:24]																							
16 bit	1st									Parameter [15:0]															
	2nd									Parameter [21:16]															
8 bit	1st																	Parameter [7:0]							
	2nd																	Parameter [15:8]							
	3rd																	…							

For certain DCS commands, the data is for LCD display. The data can be optionally written in pixel format instead of raw format. Please refer to **DFR_0/DFR_1** description for more details. In this case, the data pin mapping is given in the table below.

Table 11-2: MCU Interface Data Pin Mapping for Display Data Pixel Format

Interface	Color mode	Cycle	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24 bit	16M		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
	262k		R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x
	64k		R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B4	B3	B2	B1	B0	x	x	x
16 bit	16M type1	1st									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		2nd									x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0
	16M type2	1st									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		2nd									R7	R6	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x
	16M type3	1st									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
		3rd									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	262k, type1	1st									G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x
		2nd									x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x
	262k, type2	1st									G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x
		2nd									R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x
	262k, type3	1st									G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x
		2nd									B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x
		3rd									R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x
	64k										R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
8 bit	16M	1st																	B7	B6	B5	B4	B3	B2	B1	B0
		2nd																	G7	G6	G5	G4	G3	G2	G1	G0
		3rd																	R7	R6	R5	R4	R3	R2	R1	R0
	262k	1st																	B5	B4	B3	B2	B1	B0	x	x
		2nd																	G5	G4	G3	G2	G1	G0	x	x
		3rd																	R5	R4	R3	R2	R1	R0	x	x
	64k	1st																	G2	G1	G0	B4	B3	B2	B1	B0
		2nd																	R4	R3	R2	R1	R0	G5	G4	G3

11.3 MCU Interface Type B

This interface consists of data[23:0], rdx, wrx, dcx, and csx0 or csx1. It supports 24 bit, 16 bit and 8 bit data bus. The first cycle should be a command write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

csx0 or csx1 should be driven to 0 in this mode.

When wrx is driven from 1 to 0 and 0 to 1, the operation is a write operation. When rdx is driven from 1 to 0 and 0 to 1, the operation is a read operation.

During write operation, dcx indicates whether the operation is for data or command. When dcx is 1, the operation is for data. When dcx is 0, the operation is for command. During the read operation, the dcx should be 1.

During the write operation, data[23:0] are sampled at the rising edge of wrx. During read operation, data[23:0] are provided at the falling edge of rdx and the application processor should use the rising edge of rdx to sample.

Below is a diagram for illustration. Please see section **Error! Reference source not found.** for the detailed waveform and timing parameters.

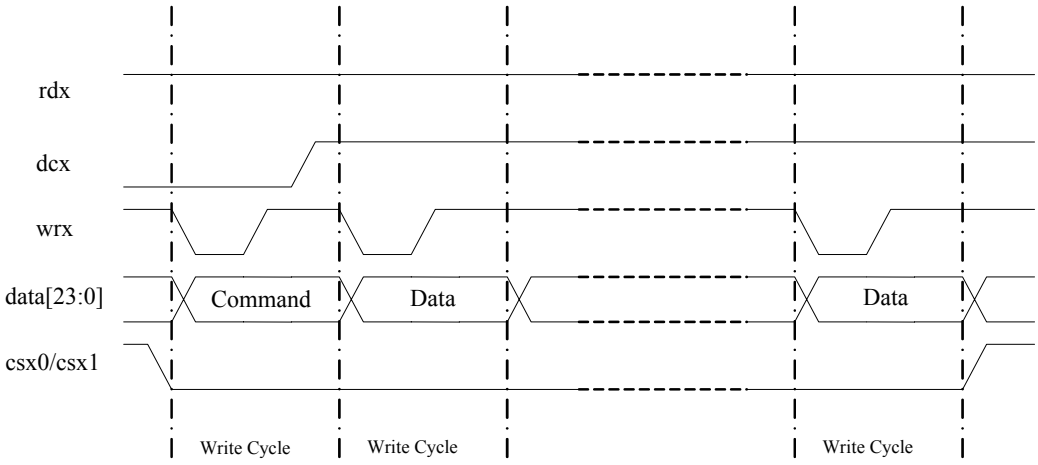


Figure 11-5: Illustration of Write Operation for Type B Interface

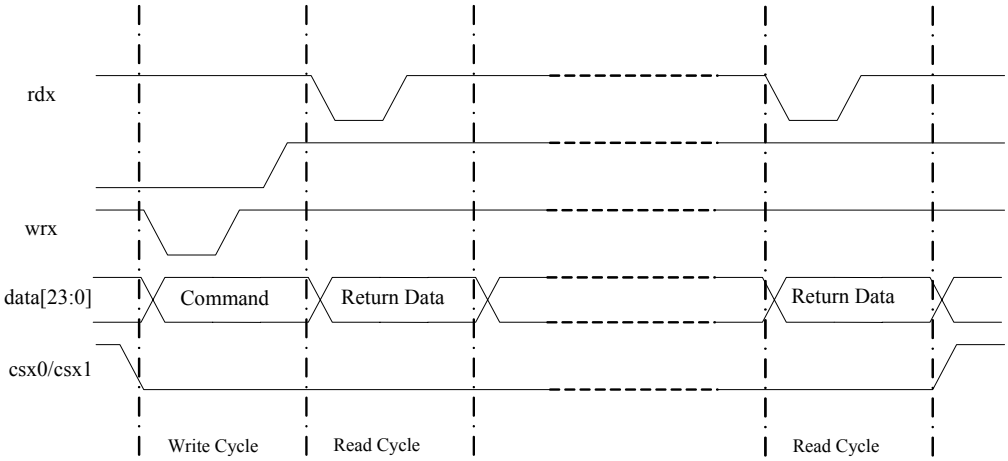


Figure 11-6: Illustration of Read Operation for Type B Interface

11.4 SPI Interface 8 bit 4 Wire

This interface consists of sdcx, sck, sdin, sdout and csx0 or csx1. It only supports 8 bit data. Each cycle contains 8 bit data. The first cycle should be a command write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx0 or csx1 should be driven from 1 to 0 to start an operation and from 0 to 1 to end an operation. During 1 operation, the application processor can write or read multiple bytes.

sdcx indicates whether the operation is for data or command. When sdcx is 1, the operation is for data. When sdcx is 0, the operation is for command. sdcx is sampled at every 8th rising edge of sck during 1 operation.

During write operation, sdin will be sampled by SSD2825 at the rising edge of sck. The first rising edge of sck after the falling edge of csx0 or csx1 samples the bit 7 of the 8 bit data. The second rising edge of sck samples the bit 6 of the 8 bit data, and so on. The value of sdcx is sampled at the 8th rising edge of sck, together with bit 0 of the 8 bit data. Please see the diagram below for illustration. Optionally, the csx0 or csx1 can be driven to 1 in between cycles.

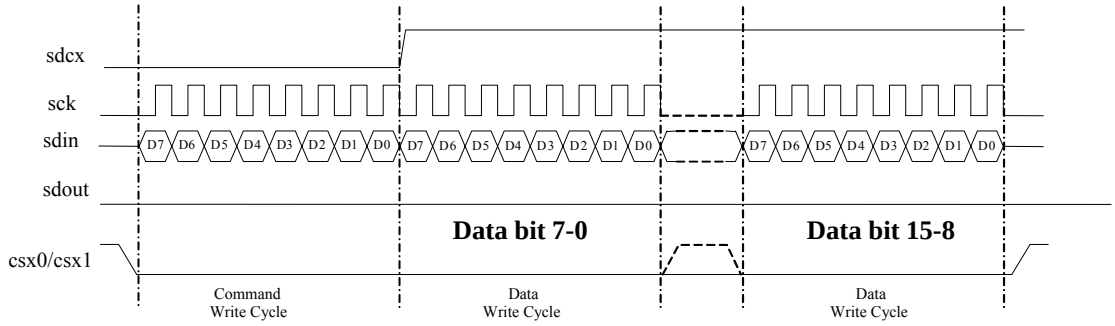


Figure 11-7: Illustration of Write Operation for 8 bit 4 Wire Interface

Remark: Send LSB 8bit of data before MSB 8bit

During read operation, since there is no rwx signal to indicate whether the operation is read or write, the read operation for SPI interface needs to be handled differently from the MCU interface. After csx0 or csx1 is driven low, the first cycle is always a command write cycle, which specifies the register to access. The second cycle is still a command write cycle. If the command in this cycle matches the command in register **LRR**, the SPI interface will enter read mode. The subsequent cycles will be read cycles. If the command does not match, the SPI interface will remain in write mode.

After entering the read mode, the return data is provided on sdout, on the falling edge of sck. The application processor should use the rising edge of sck to sample the data. sdcx should be driven to 1 during the read cycles. Please see the diagram below for illustration. Optionally, the csx0 or csx1 can be driven to 1 in between cycles.

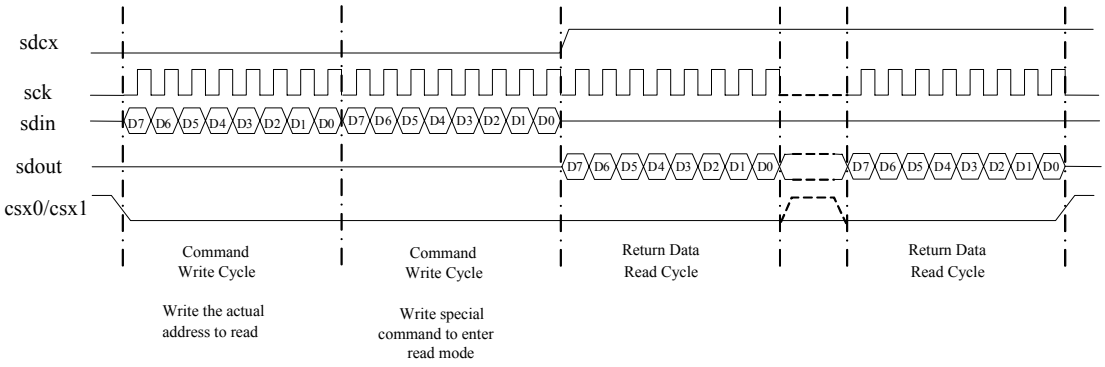


Figure 11-8: Illustration of Read Operation for 8 bit 4 Wire Interface

11.5 SPI Interface 8 bit 3 Wire

This interface consists of sck, sdin, sdout and csx0 or csx1. It only supports 8 bit data. Each cycle contains 8 bit data. The first cycle should be a write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx0 or csx1 should be driven from 1 to 0 to start an operation and from 0 to 1 to end an operation. During 1 operation, the application processor can write or read multiple bytes.

Instead of sdcx, an sdcx bit is used to indicate whether the operation is for data or command. Each byte is associated with an sdcx bit. When sdcx is 1, the operation is for display data. When sdcx is 0, the operation is for command. The sdcx bit is sent priori to each byte. In other words, the sdcx bit is the first bit of every 9 bits during 1 operation.

During write operation, sdin will be sampled by SSD2825 at the rising edge of sck. The first rising edge of sck after the falling edge of csx0 or csx1 samples the sdcx bit. The second rising edge samples bit 7 of the 8 bit data. The third rising edge of sck samples the bit 6 of the 8 bit data, and so on. Please see the diagram below for illustration. Optionally, the csx0 or csx1 can be driven to 1 in between cycles.

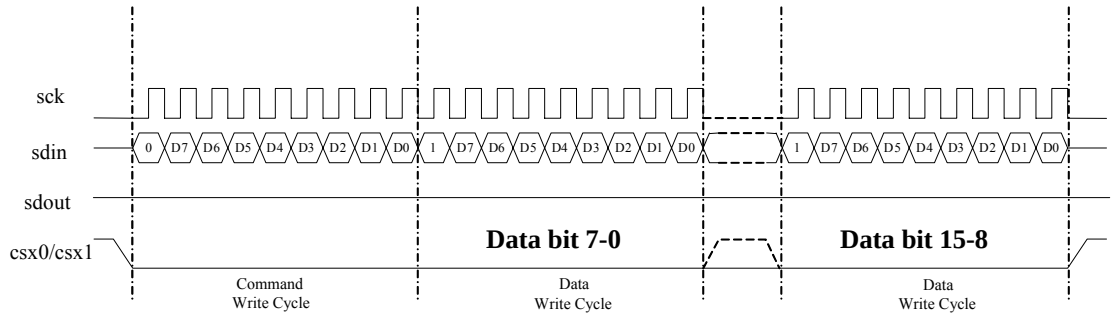


Figure 11-9: Illustration of Write Operation for 8 bit 3 Wire Interface

Remark: Send LSB 8bit of data before MSB 8bit

During read operation, since there is no rwx signal to indicate whether the operation is read or write, the read operation for SPI interface needs to be handled differently from the MCU interface. After csx0 or csx1 is driven low, the first cycle is always a command write cycle, which specifies the register to access. The second cycle is still a command write cycle. If the command in this cycle matches the command in register **LRR**, the SPI interface will enter read mode. The subsequent cycles will be read cycles. If the command does not match, the SPI interface will remain in write mode.

After entering the read mode, the return data is provided on sdout, on the falling edge of sck. The application processor should use the rising edge of sck to sample the data. Please note that there is no sdcx bit to read out from SSD2825. Hence, each read cycle consists of 8 bits instead of 9 bits. This is the difference between read and write cycles. Please see the diagram below for illustration. Optionally, the csx0 or csx1 can be driven to 1 in between cycles.

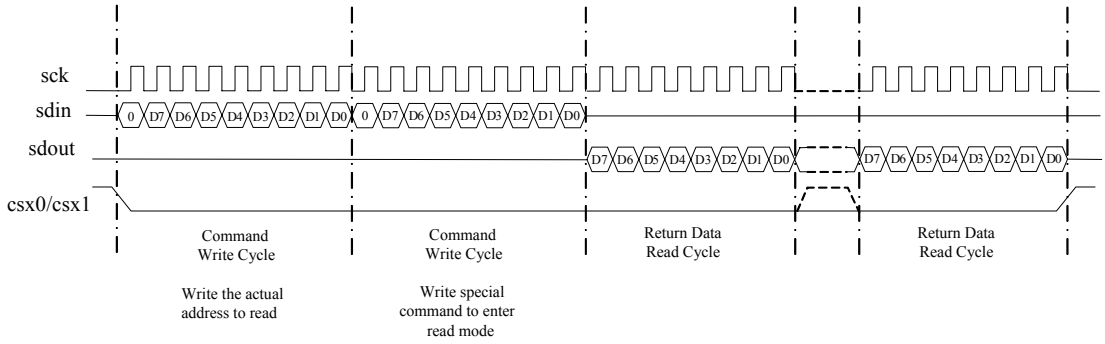
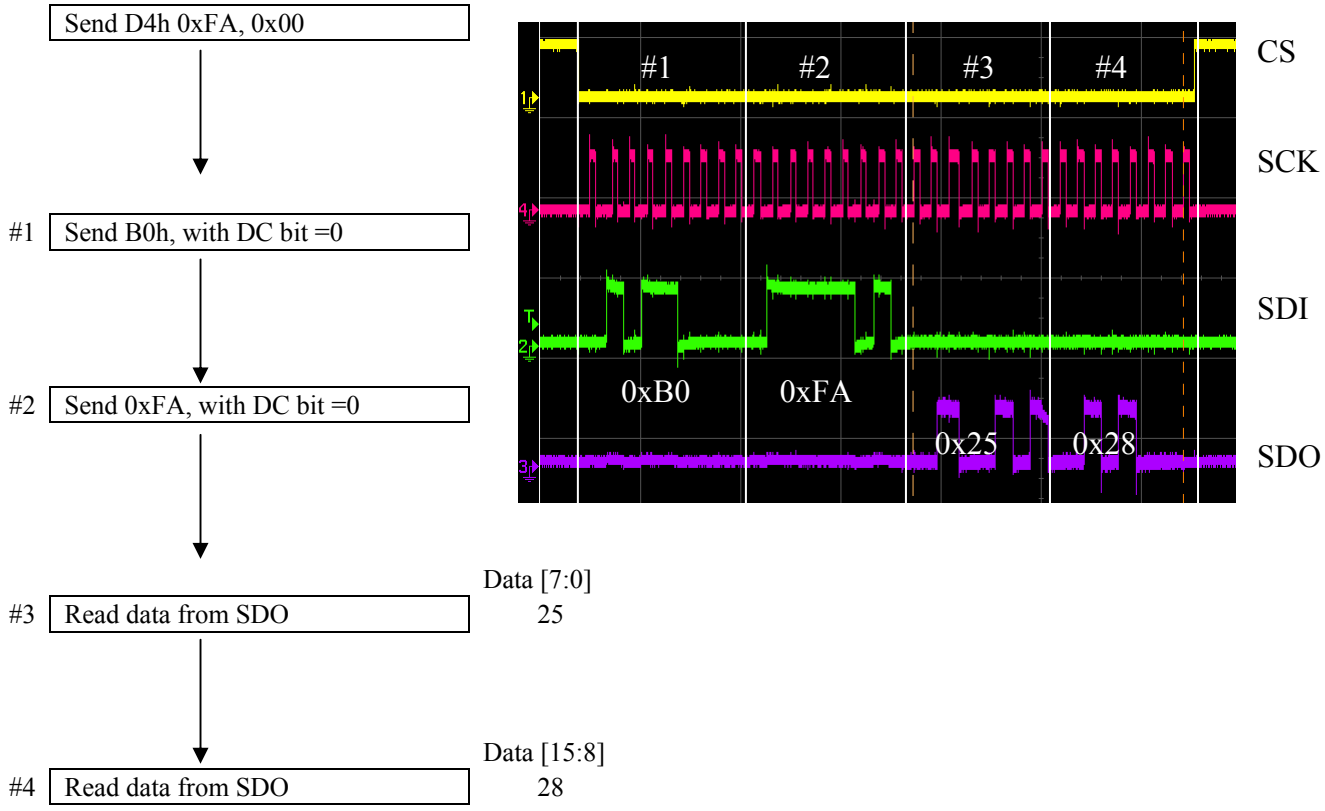


Figure 11-10: Illustration of Read Operation for 8 bit 3 Wire Interface

Read sequence of register e.g.0xB0h



11.6 SPI Interface 24 bit 3 Wire

This interface consists of sck, sdin, sdout and csx0 or csx1. It only supports 16 bit data. Each cycle contains 16 bit data. The first cycle should be a write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx0 or csx1 should be driven from 1 to 0 to start cycle and from 0 to 1 to end a cycle. During 1 operation, the application processor can have multiple write or read cycles. However, the csx0 or csx1 must go from 0 to 1 at the end of each cycle.

Each cycle contains 24 bit data. Among the 24 bit data, the first 8 bit are for control purpose and the next 16 bit are the actual data. The first 6 bit are the ID bit for SSD2825, which must be 011100. If this field does not match, the cycle will not be taken in. The 7th bit is the sdcx bit which is the same as the 8 bit 3 wire interface. The 8th bit is the RW bit which indicates whether the current cycle is a read or write cycle. When RW is 1, the cycle is a read cycle. When RW is 0, the cycle is a write cycle.

During write operation, sdin will be sampled by SSD2825 at the rising edge of sck. Please see the diagram below for illustration. It is an example for writing data 0x1264 to register address 0x28.

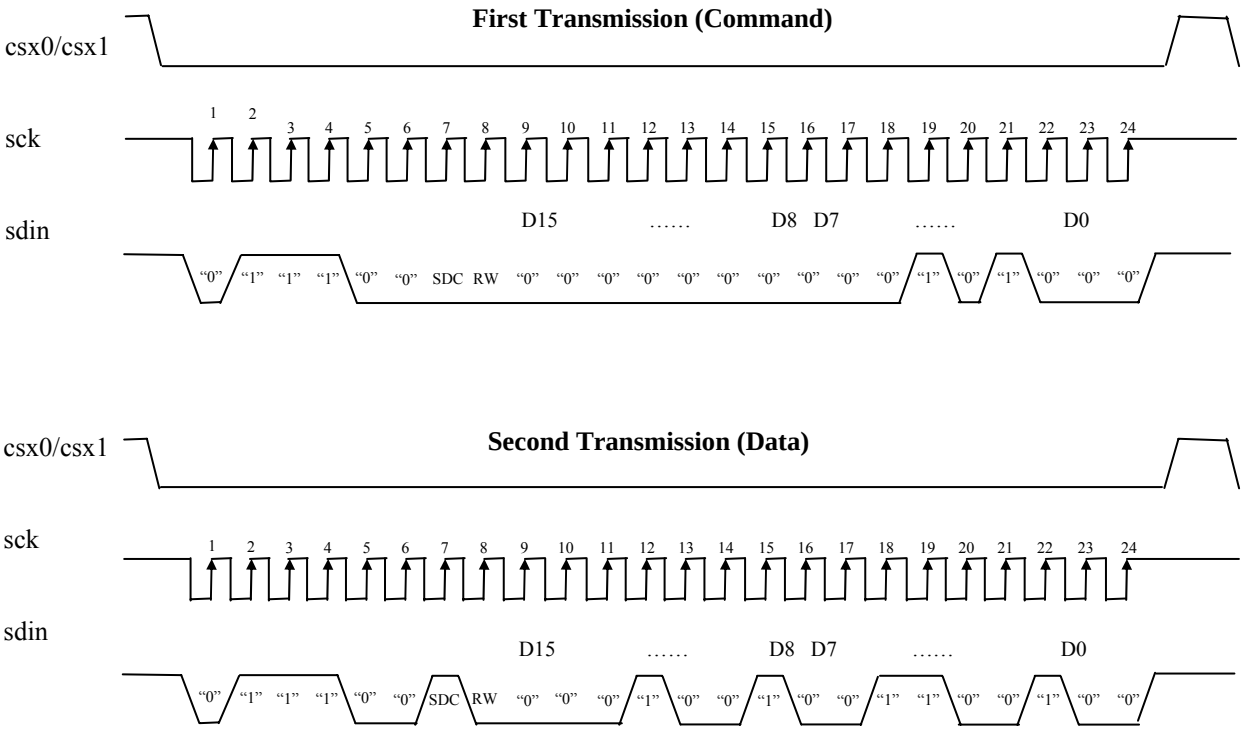


Figure 11-11: Illustration of Write Operation for 24 bit 3 wire Interface

Remark: Send MSB 8bit of data before LSB 8bit

During read operation, the first 8 bit are still written by the application processor to specify whether the following 16 bit are for command or data. Afterwards, the SSD2825 will provide the return data on sdout, on the falling edge of sck. The application processor should use the rising edge of sck to sample. Please see the diagram below for illustration.

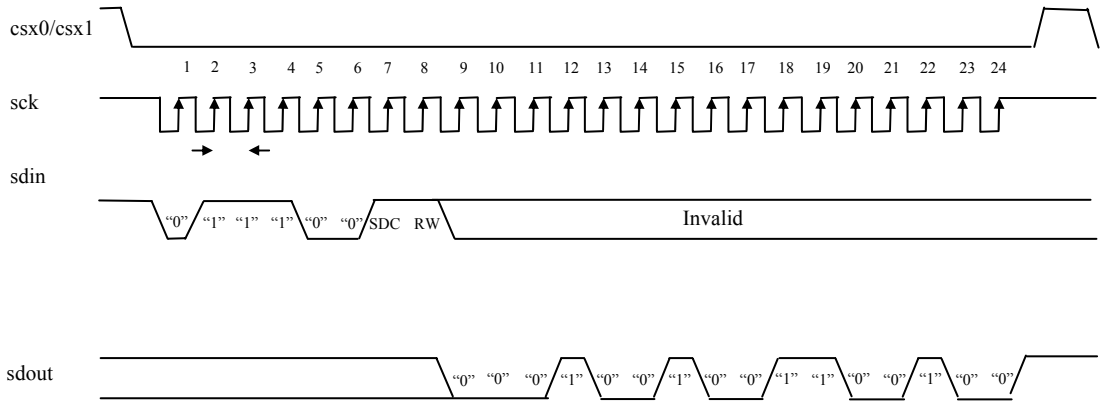
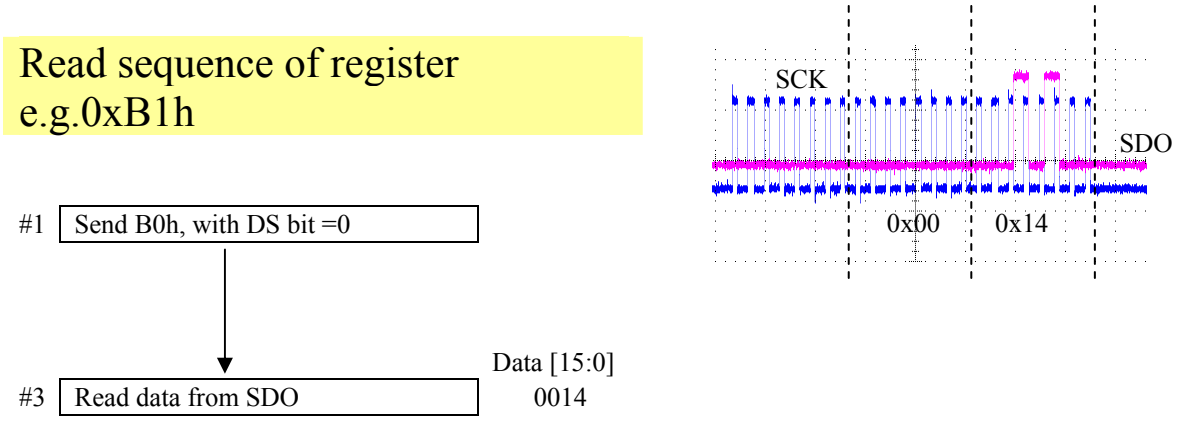


Figure 11-12: Illustration of Read Operation for 24 bit 3 Wire Interface



12 MAXIMUM RATINGS

Table 12-1: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{MDVDD}	Digital Core Power Supply	-0.3 to 1.44	V
V_{MAVDD}	Analog Core Power Supply	-0.3 to 1.44	V
V_{VDDIO}	I/O Power Supply	-0.3 to 4.0	V
T_{SOL}	Solder Temperature / Time	225 for 40 sec max at solder ball	^{o}C
T_{STG}	Storage Temperature	-40 to 100	^{o}C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits specified in the electrical characteristics tables and Pin Description section

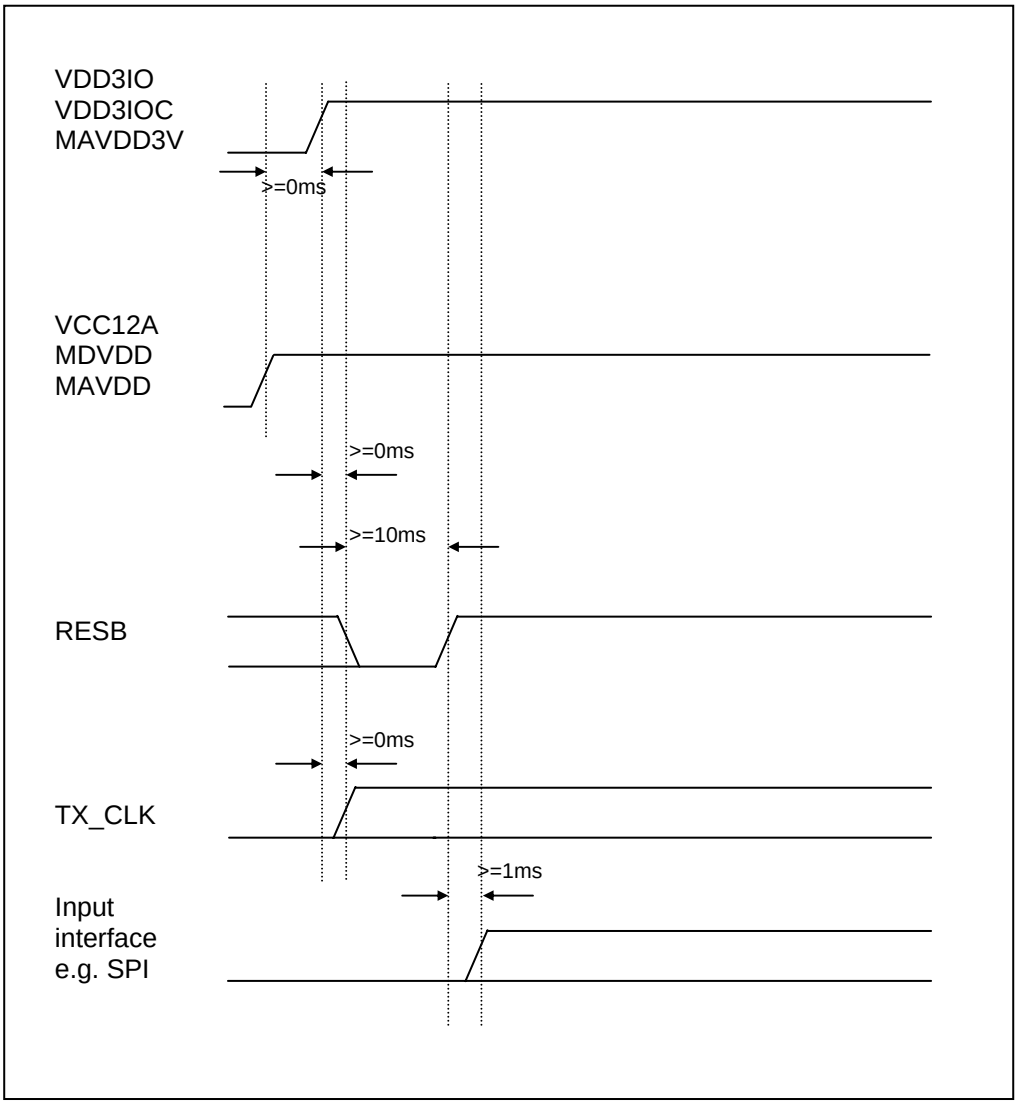
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

13 RECOMMENDED OPERATING CONDITIONS

Table 13-1: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{MDVDD}	Digital Core Power Supply	1.08	1.2	1.32	V
V_{MAVDD}	Analog Core Power Supply	1.08	1.2	1.32	V
V_{VDDIO}	I/O AND Digital Power Supply	2.97	3.3	3.63	V
		1.62	1.8	1.98	V
T_A	Operating Temperature	-30	25	85	^oC

14 Power up sequence



15 DC Characteristics

Conditions: Voltage referenced to V_{SS}
VDDD (Digital voltage) → MAVDD, MDVDD, VCC12A = 1.2V
VDDA (Analog voltage) → MAVDD3V, ATC[1:0] = 3.3V
VDDIO (IO voltage) → VDD3IO, VDD3IOC = 3.3V
Frame frequency = 60Hz
Number of lane = 4
Display pattern = 720x1280, 8 colors vertical bar
T_A = 25°C

Table 15-1: DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{DDD_HS}	High Speed Mode Current	500Mbps	-	31.10	50.65	mA
I_{DDA_HS}			-	0.07	0.15	mA
I_{DDIO_HS}			-	0.24	0.50	mA
I_{DDD_LP}	Low Power Mode Current	250Mbps	-	15.94	39.85	mA
I_{DDA_LP}			-	0.07	0.15	mA
I_{DDIO_LP}			-	0.17	0.43	mA
I_{DDD_ULPS}	Ultra Low Power State Current	PLL off, no change in all input signals	-	70	165	µA
I_{DDA_ULPS}			-	46	115	µA
I_{DDIO_ULPS}			-	200	450	µA
$V_{OH\ (CMOS)}$	Output High Voltage (CMOS)	I_{OH} = -2 ~ -16 mA	V_{DDIO} x 0.8	-	-	V
$V_{OL\ (CMOS)}$	Output Low Voltage (CMOS)	I_{OL}= 2 ~ 16 mA	-	-	V_{DDIO} x 0.15	V
$V_{IH\ (CMOS)}$	Input High Voltage (CMOS)		V_{DDIO} x 0.7	-	-	V
$V_{IL\ (CMOS)}$	Input Low Voltage (CMOS)		-	-	V_{DDIO} x 0.2	V
I_{OZ}	Tri-state Output Leakage Current		-	TBD	-	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DDIO} or V_{SS}	-	TBD	-	µA
C_{IN}	Input Capacitance		-	TBD	-	pF

Table 15-2: HS Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}	HS Transmit Static Common-mode Voltage	150	-	250	mV
$\|V_{OD}\|$	HS Transmit Differential Voltage	140	-	270	mV
$\|\Delta V_{OD}\|$	HS Differential Mismatch	-	-	10	mV
V_{OHHS}	HS Output High Voltage	-	-	360	mV

Table 15-3: LP Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	LP Thevenin Output High Level	1.1	1.2	1.3	V
V_{OL}	LP Thevenin Output Low Level	-50	-	50	mV
Z_{OLP}	LP Transmitter Output Impedance	110	-	-	Ohm

Table 15-4: LP Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	LP Logic 1 Input Voltage	880	-	-	mV
V_{IL}	LP Logic 0 Input Voltage	-	-	550	mV

16 AC Characteristics

NOTE:

1. After PLL gets locked, T is the period of the PLL output clock. Before PLL gets locked, T is the period of PLL input reference clock. The reference clock can be either the tx_clk or the pclk, depending on the **CSS** bit.

   1 / T = PLL / 2,

   e.g. When PLL is Off <0xB9 0x0000>,

   PLL = TX_CLK = 10MHz,

   1 / T = 5MHz

2. W is the width of the display, e.g. the number of pixels for the horizontal line.

3. The AC characteristics specifie the maximum speed of the incoming signals at the input interface. However, the data throughput on the serial link is another factor affecting the speed. If the user takes in the int_0/int_1 signal, there will be automatic flow control. If the user does not take the int_0/int_1 signal, the user needs to ensure that the output throughput is larger than the incoming data rate.

Table 16-1: MCU Interface (Type A) Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	6T		-	ns
PW_{CSH}	Control Pulse Low Width	3T		-	ns
PW_{CSL}	Control Pulse High Width	3T		-	ns
t_{AS}	Address Setup Time	1		-	ns
t_{AH}	Address Hold Time	0		-	ns
t_{DSW}	Data Setup Time	5		-	ns
t_{DHW}	Data Hold Time	1		-	ns
t_{ACC}	Data Access Time	-		5.3+4T	ns
t_{DHW}	Read Data Hold Time	1+2T		5.3+4T	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

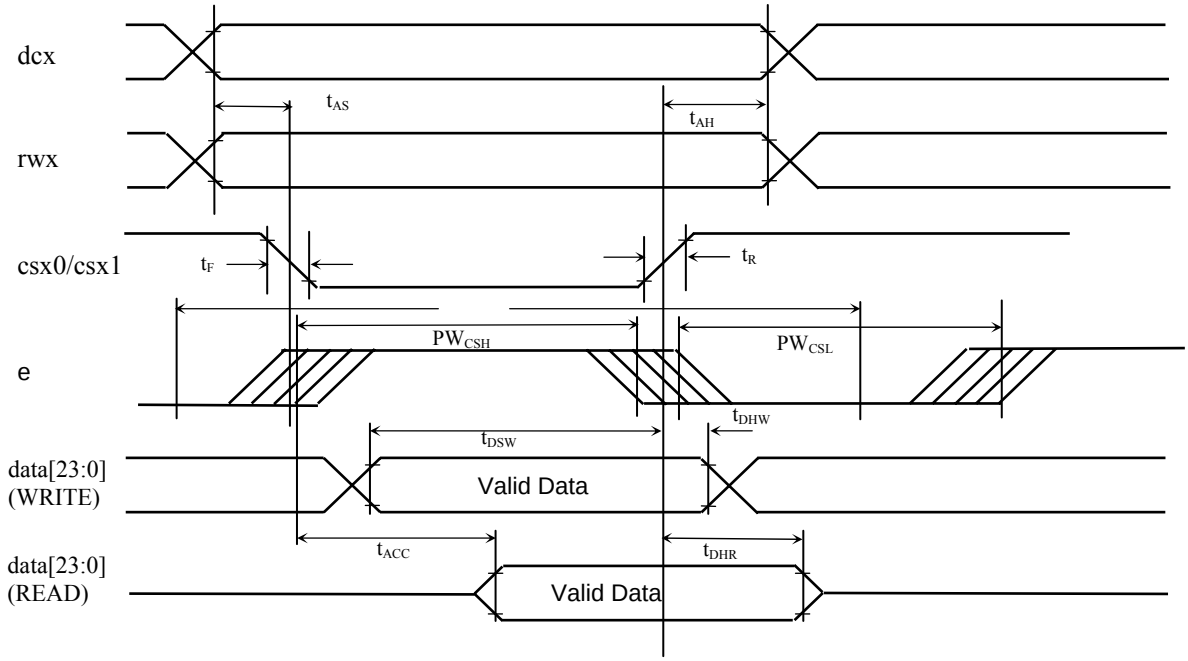
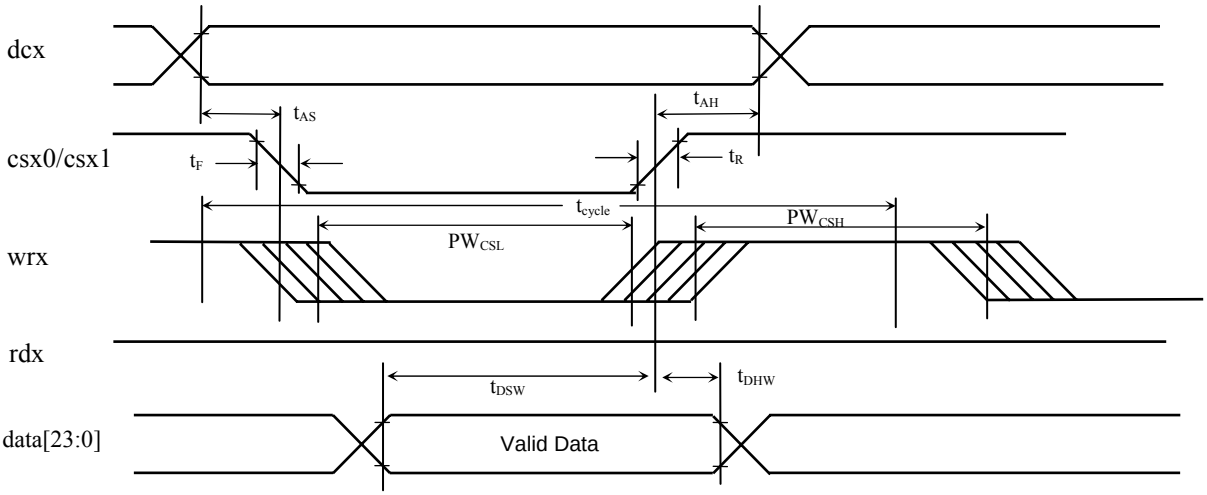


Figure 16-1: MCU Interface (Type A) Timing Diagram

Table 16-2: MCU Interface (Type B) Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	6T		-	ns
PW_{CSH}	Control Pulse Low Width	3T		-	ns
PW_{CSL}	Control Pulse High Width	3T		-	ns
t_{AS}	Address Setup Time	1		-	ns
t_{AH}	Address Hold Time	0		-	ns
t_{DSW}	Data Setup Time	5		-	ns
t_{DHW}	Data Hold Time	1		-	ns
t_{ACC}	Data Access Time	-		5.3+4T	ns
t_{DHR}	Read Data Hold time	1+2T		5.3+4T	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

Write



Read

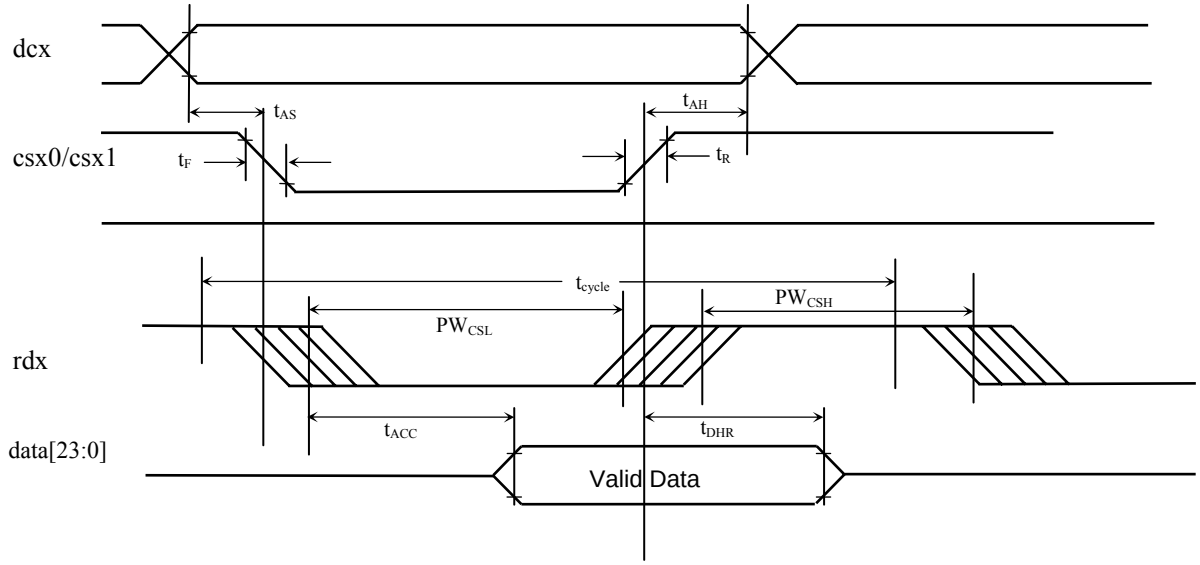


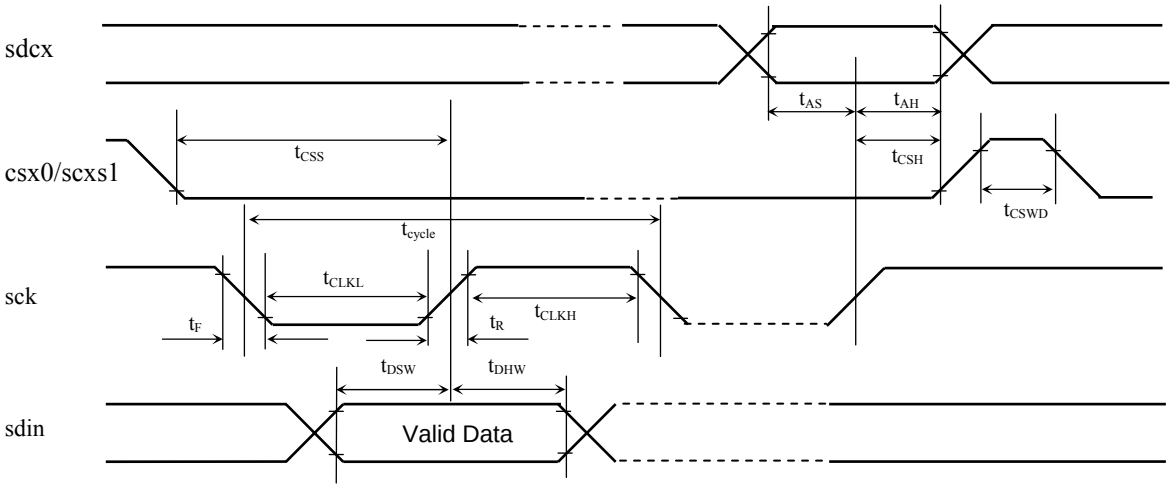
Figure 16-2: MCU Interface (Type B) Timing Diagram

Table 16-3: 8 Bit 4 Wire SPI Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	8T		-	ns
f_{CLK}	Serial Clock Cycle Time	-		1/8T	MHz
t_{AS}	Register select Setup Time	4		-	ns
t_{AH}	Register select Hold Time	0		-	ns
t_{CSS}	Chip Select Setup Time	4		-	ns
t_{CSH}	Chip Select Hold Time	0		-	ns
t_{DSW}	Write Data Setup Time	4		-	ns
t_{DHW}	Write Data Hold Time	0		-	ns
t_{ACC}	Read Data Access Time	-		4.4+6T	ns
t_{DHR}	Read Data Hold Time	1.2+4T		4.4+6T	ns
t_{CLKL}	Clock Low Time	4T		-	ns
t_{CLKH}	Clock High Time	4T		-	ns
t_{CSWD}	Chip Select Write Delay Time	8T		-	ns
t_{CSRD}	Chip Select Read Delay Time	16T		-	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

Note: All timings are based on 20% to 80% of supply voltage

Write



Read

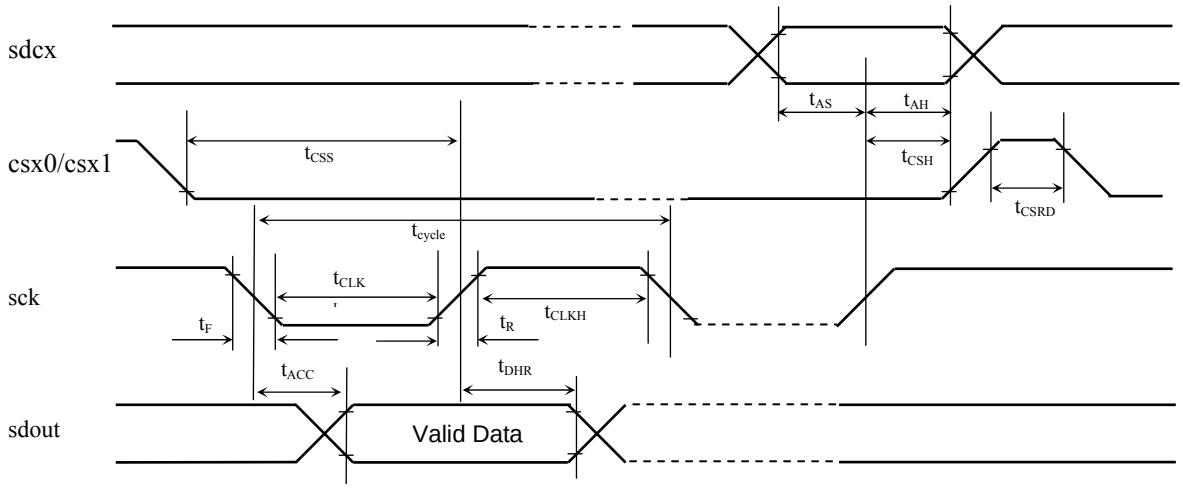


Figure 16-3: 8 Bit 4 Wire SPI Interface Timing Diagram

Table 16-4: 8 Bit 3 Wire SPI Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	8T		-	ns
f_{CLK}	Serial Clock Cycle Time	-		1/8T	MHz
t_{CSS}	Chip Select Setup Time	4		-	ns
t_{CSH}	Chip Select Hold Time	0		-	ns
t_{DSW}	Write Data Setup Time	4		-	ns
t_{OHW}	Write Data Hold Time	0		-	ns
t_{ACC}	Read Data Access Time	-		4.4+6T	ns
t_{DHR}	Read Data Hold Time	1.2+4T		4.4+6T	ns
t_{CLKL}	Clock Low Time	4T		-	ns
t_{CLKH}	Clock High Time	4T		-	ns
t_{CSWD}	Chip Select Write Delay Time	8T		-	ns
t_{CSRD}	Chip Select Read Delay Time	16T		-	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

Note: All timings are based on 20% to 80% of supply voltage

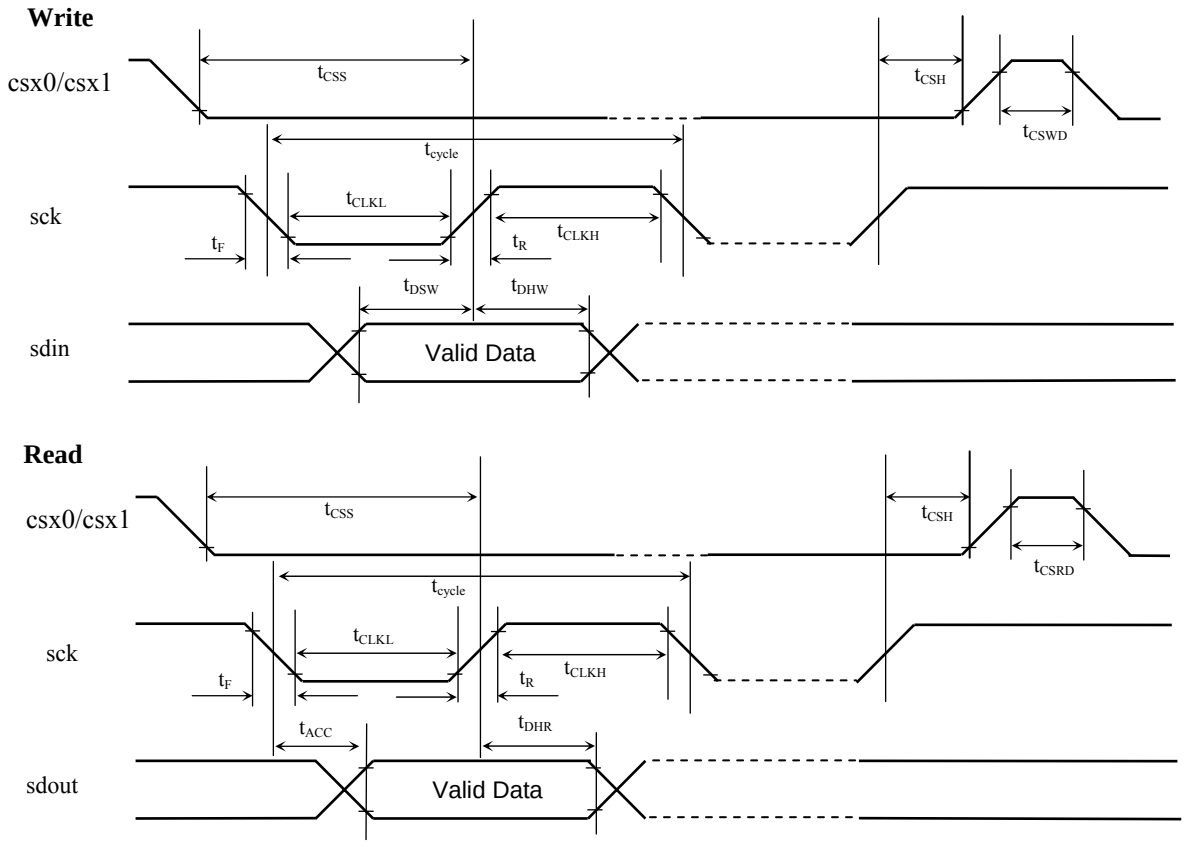


Figure 16-4: 8 Bit 3 Wire SPI Interface Timing Diagram

Table 16-5: 24 Bit 3 Wire SPI Interface Timing Characteristics

Symbol	Parameters	Min	Typ	Max	Units
t_{cycle}	Clock Cycle Time	8T		-	ns
f_{CLK}	Serial Clock Cycle Time	-		1/8T	MHz
t_{CSS}	Chip Select Setup Time	4		-	ns
t_{CSH}	Chip Select Hold Time	0		-	ns
t_{DSW}	Write Data Setup Time	4		-	ns
t_{OHW}	Write Data Hold Time	0		-	ns
t_{ACC}	Read Data Access Time	-		4.4+6T	ns
t_{DHR}	Read Data Hold Time	1.2+4T		4.4+6T	ns
t_{CLKL}	Clock Low Time	4T		-	ns
t_{CLKH}	Clock High Time	4T		-	ns
t_{CSWD}	Chip Select Write Delay Time	8T		-	ns
t_{CSRD}	Chip Select Read Delay Time	16T		-	ns
t_R	Rise time	-		2	ns
t_F	Fall time	-		2	ns

Note: All timings are based on 20% to 80% of supply voltage

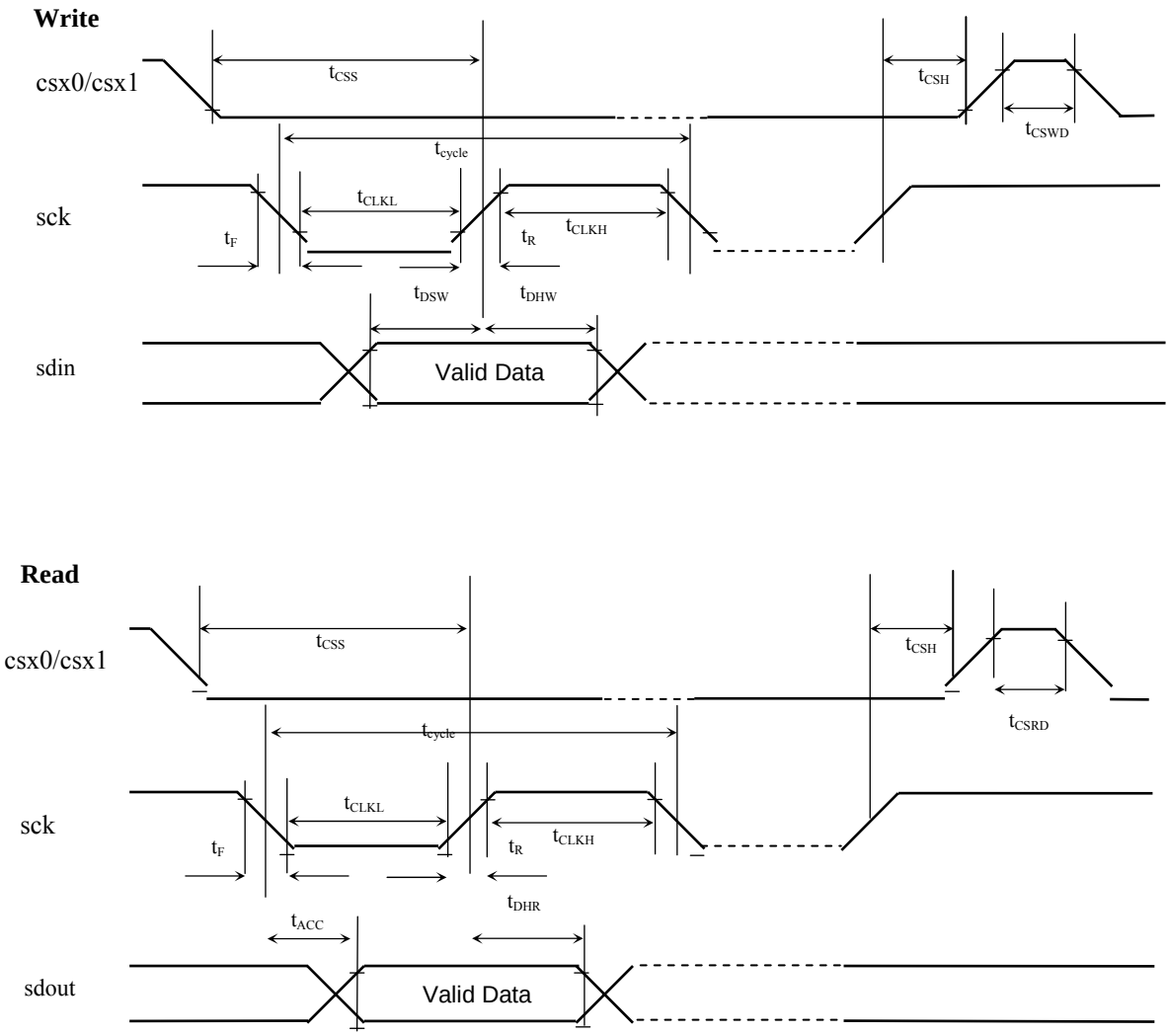


Figure 16-5: 24 Bit 3 Wire SPI Interface Timing Diagram

Table 16-6: RGB Interface Timing Characteristics

Symbol	Parameters	Min	Typ	Max	Units
t_{pclk}	pclk Period	16/18/24T	16/18/24T		ns
t_{vsys}	Vertical Sync Setup Time	5			ns
t_{vsyh}	Vertical Sync Hold Time	5			ns
t_{hsys}	Horizontal Sync Setup Time	5			ns
t_{hsyh}	Horizontal Sync Hold Time	5			ns
t_{hv}	Phase difference of Sync Signal Falling Edge	0		W	t_{pclk}
t_{CKL}	pclk Low Period	8/9/12T	8/9/12T		ns
t_{CKH}	pclk High Period	8/9/12T	8/9/12T		ns
t_{ds}	Data Setup Time	5			ns
t_{dh}	Data hold Time	5			ns

Note:
1. All timings are based on 20% to 80% of supply voltage
2. The pclk period depends on the bit per pixel (bpp) setting and whether the video mode is burst or non-burst mode. In burst mode, the values in the Min column should be followed. In non-burst mode, the values in the Typ column should be followed. Please refer to 10.5.1 for more details.

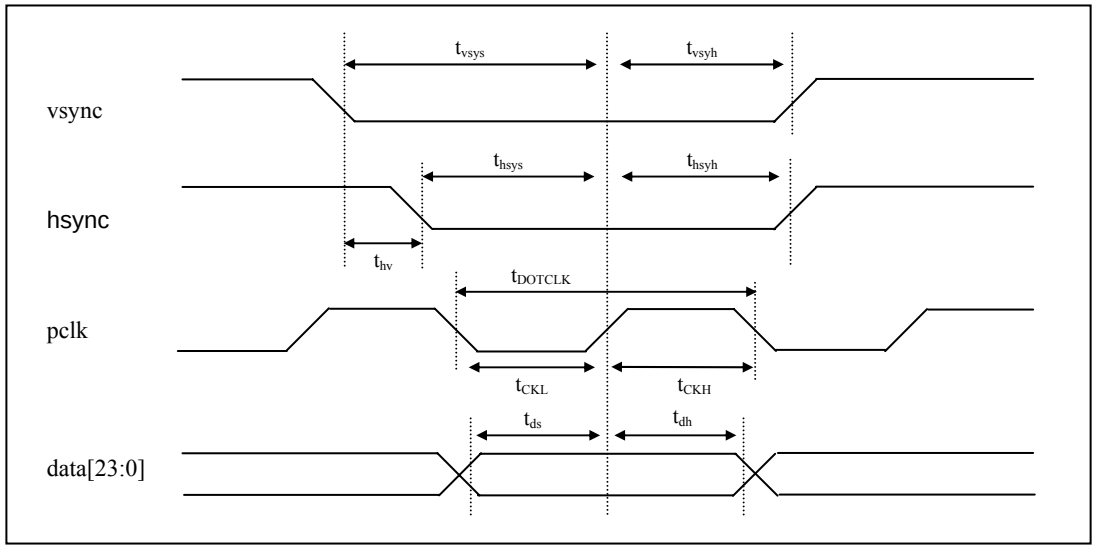


Figure 16-6: RGB Interface Timing Diagram

16.1 Serial Link Data Order

There are many possible ways of doing parallel to serial conversion. SSD2825 provides flexibility by programming two register bits **END** and **CO**. During video mode, they must be programmed to 0 and 1 respectively.

Below is the order to receive the display data over the serial link, when the **END** bit is 1 and **CO** bit is 0.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0

Time

Below is the order to send the display data over the serial link, when the **END** bit is 0 and **CO** bit is 0.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
G2	G1	G0	B4	B3	B2	B1	B0	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	R4	R3	R2	R1	R0	G5	G4	G3

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
G1	G0	B5	B4	B3	B2	B1	B0	R3	R2	R1	R0	G5	G4	G3	G2	B5	B4	B3	B2	B1	B0	R5	R4	R1	R0	G5	G4	G3	G2	G1	G0

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	R5	R4	R3	R2	R1	R0

Time

Below is the order to send the display data over the serial link, when the **END** bit is 1 and **CO** bit is 1.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	R5	R4	R3	R2	R1	R0

Time

Below is the order to send the display data over the serial link, when the **END** bit is 0 and **CO** bit is 1.

For 16 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0	B4	B3	B2	B1	B0	G5	G4	G3

Time

For 18 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							

G1	G0	R5	R4	R3	R2	R1	R0	B3	B2	B1	B0	G5	G4	G3	G2	R5	R4	R3	R2	R1	R0	B5	B4	B1	B0	G5	G4	G3	G2	G1	G0

Time

For 24 bit per pixel data, below is the byte order. Each byte of data is sent in the order of LSB first and MSB last.

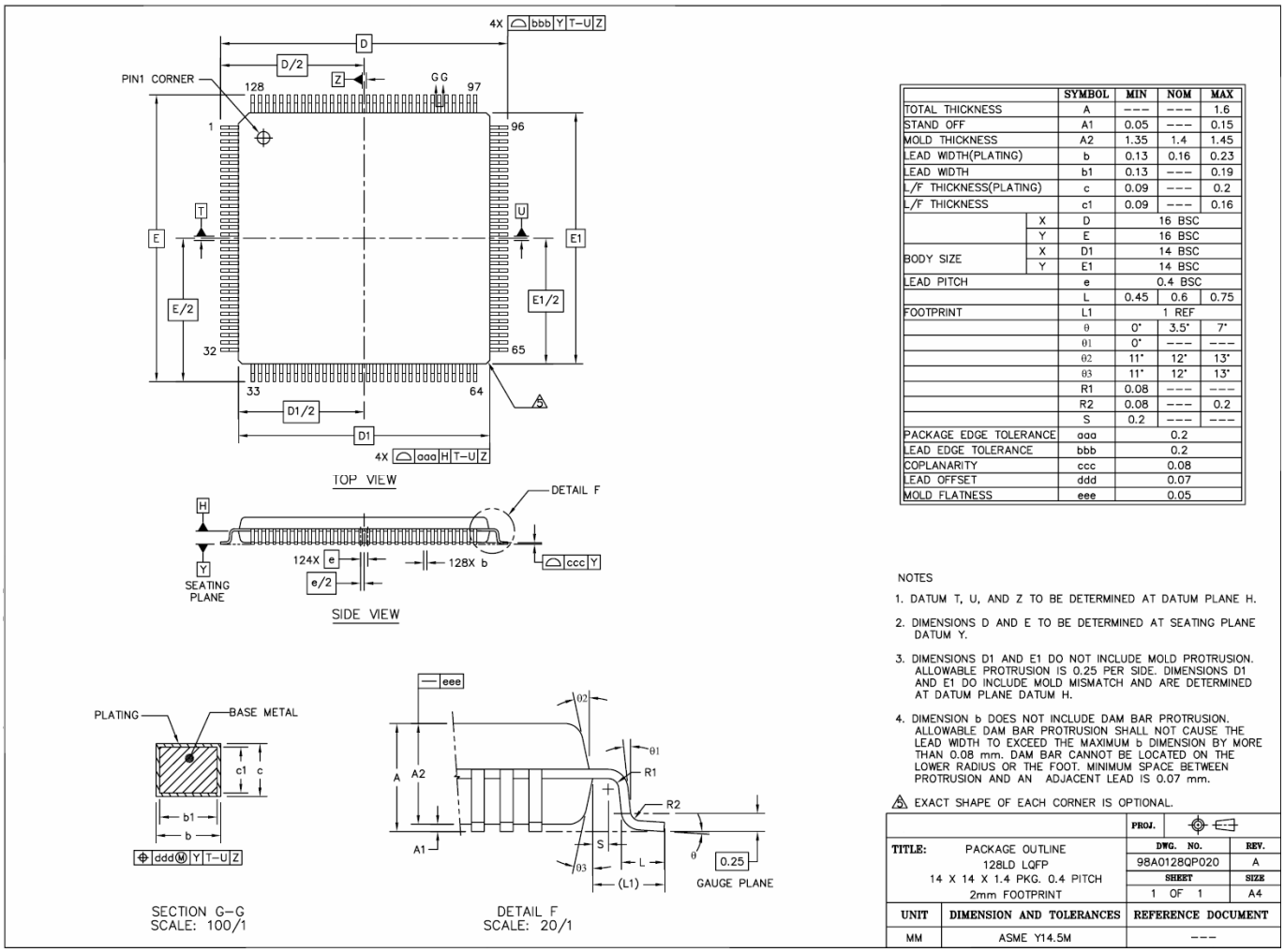
MSB Byte 1 LSB								MSB Byte2 LSB								MSB Byte3 LSB								MSB Byte4 LSB							
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0

Time

17 PACKAGE INFORMATION

17.1 Dimension for SSD2825

Figure 17-1- Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
FOOTPRINT		L	0.45	0.6	0.75
		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

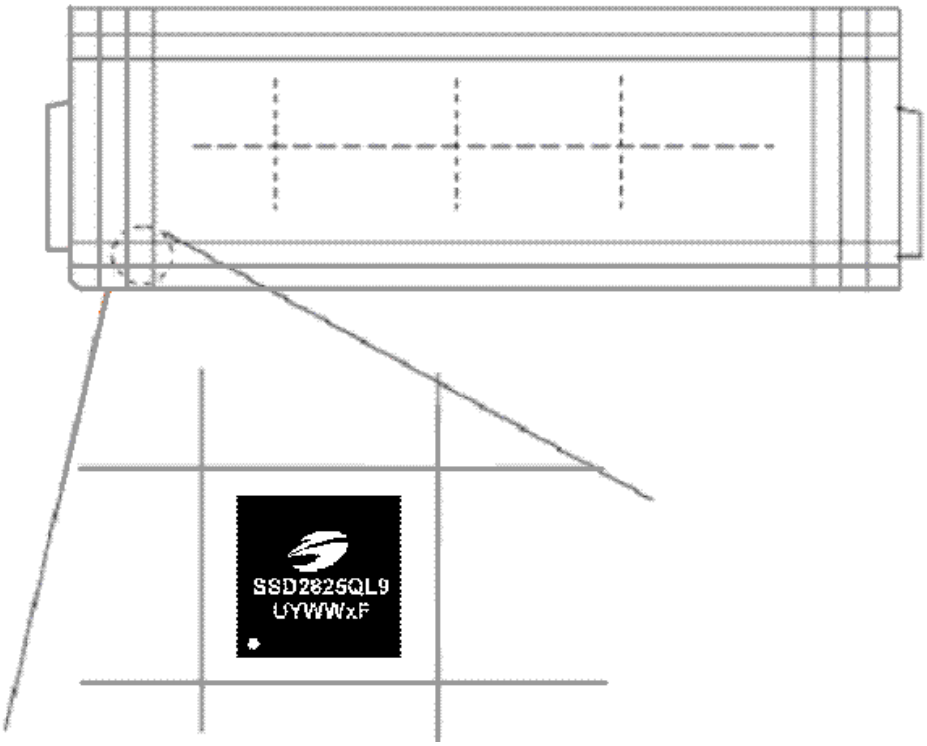
TITLE: PACKAGE OUTLINE 128LD LQFP 14 X 14 X 1.4 PKG. 0.4 PITCH 2mm FOOTPRINT	PROJ.	
	DWG. NO.	REV.
	98A0128QP020	A
	SHEET	SIZE
	1 OF 1	A4
UNIT: MM	DIMENSION AND TOLERANCES: ASME Y14.5M	REFERENCE DOCUMENT: ---

17.2 Marking for SSD2825

Figure 17-2- Marking Information

17.3 Chip Tray for SSD2825

Figure 17-3- Tray Information



The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

http://www.solomon-systech.com