DATA SHEET

旭曜科技
ORISE TECH

SPLC792A

18COM/80SEG LCD Controller/Driver

Preliminary

OCT. 15, 2010

Version 0.3

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18COM / 80SEG LCD Controller / Driver

1. GENERAL DESCRIPTION

The SPLC792A, a dot-matrix LCD controller and driver from ORISE, is a unique design for displaying alpha-numeric, Japanese-Kana characters and symbols. The SPLC792A provides 4-bit, 8-bit and serial interfaces mode can be easy control by microprocessor. The SPLC792A is able to display 2-line of 16-character and 80-Icon on the display panel. The CMOS technology ensures the power saves in the most efficient way and the performance keeps in the highest rank.

2. FEATURES

■ Operation Voltage Range
- — Power supply voltage (VDD) : 2.4 to 5.5V
- — LCD driving voltage : 3.0 to 6.0V

■ Display data RAM: 640 bits
- — 80 Character of display data

■ Character generator ROM: 10240 bits
- — Character font 5 x 8 dots : 256 characters

■ Character generator RAM: 320 bits
- — Character font 5 x 8 dots : 8 characters

■ Icon RAM: 80 bits

■ Interface Mode
- — 4-bit or 8-bit 6800 / 8080 MPU interfaces
- — 3-Wire / 4-Wire Serial interfaces
- — I^2C interfaces

■ LCD Display
- — 1/8 duty: 1 lines of 5 x 8 dots / line without Icon display
- — 1/9 duty: 1 lines of 5 x 8 dots / line with Icon display
- — 1/16 duty: 2 lines of 5 x 8 dots / line without Icon display
- — 1/17 duty: 2 lines of 5 x 8 dots / line with Icon display

■ Built-in power on automatic reset circuit and external reset pin

■ Built-in oscillator circuit and external clock mode (without external resistor)

■ Built-in voltage booster and voltage follower circuit (low power consumption)

■ Com/Seg bi-direction selectable by pin control

■ Instruction compatible to SPLC780, SPLC782A , KS0066U and HD44780

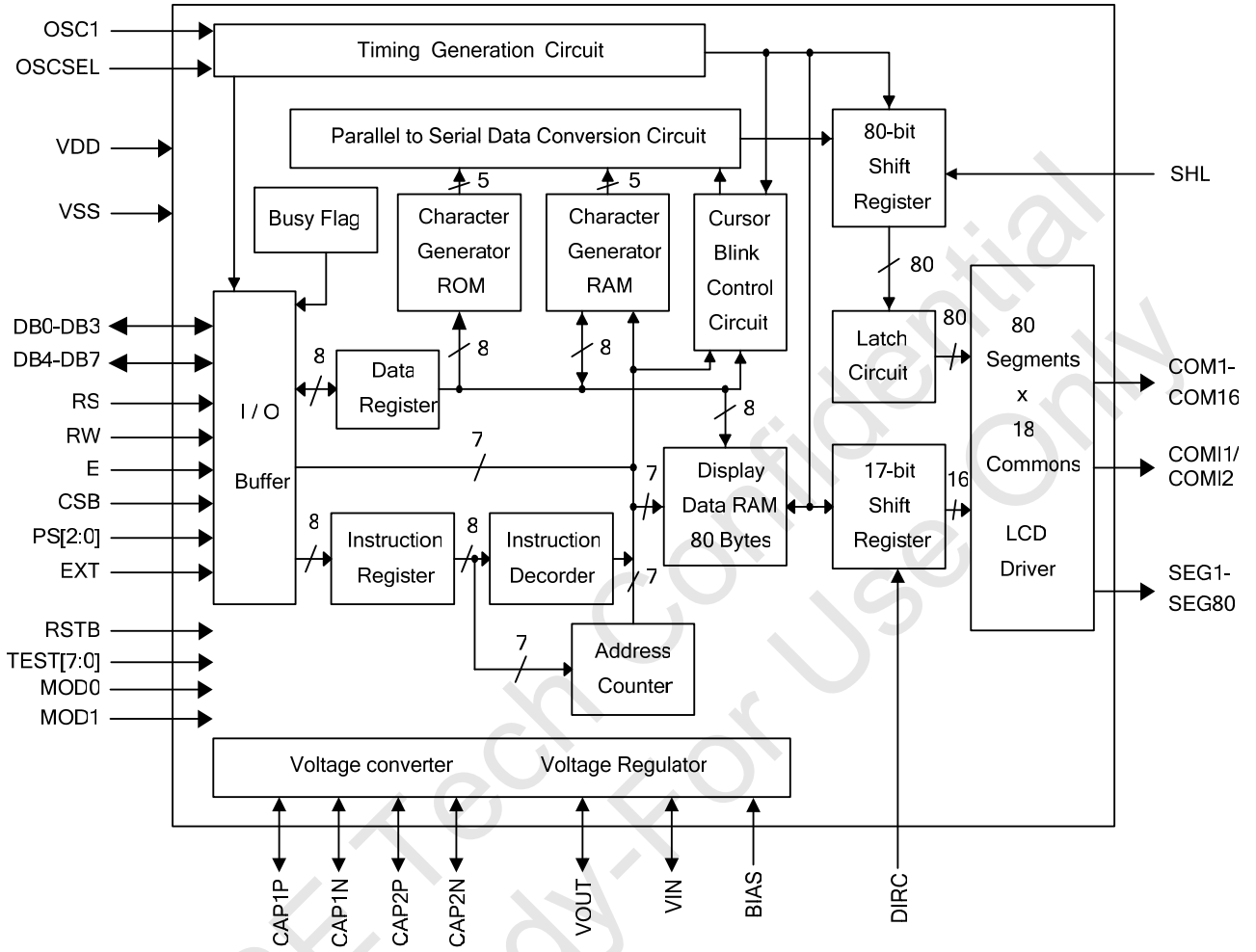
■ Application Panel Resolution

Product Name	COM	SED	Bias	VREF Temperature Gradient	VOUT voltage source
SPLC792A	8	80	1/4, 1/5	-0.05%/℃	External Power supply
	16	80			External Power supply
	10	80			Internal Booster circuit
	18	80			Internal Booster circuit

■ Application MPU interface mode

SPLC792A	**6800-4bit / 8bit , 8080-4bit / 8bit , 4-line , 3-line , I^2C**

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

4.1. Power Supply Pins

Mnemonic	Type	Connected with	Description
VDD	P	Power supply	Power input
VSS	P		Ground

P: Power Supply

4.2. LCD Power Supply Circuit Terminals

Mnemonic	Type	Connected with	Description
VOUT	P	Power supply	DC/DC voltage converter. Connect a capacitor between this terminal with VSS when the built-in booster is used. When the DC/DC voltage converter is not used, the VOUT terminal must be connect to VIN
VIN	P	Power supply	Power input for booster EXT = 0 : VIN must be connecting to VOUT. EXT = 1 : VIN muse be connecting to VDD.
CAP1P	P	Step-up capacitor	Booster capacitor connect pin
CAP1N	P		Booster capacitor connect pin
CAP2P	P		Booster capacitor connect pin
CAP2N	P		Booster capacitor connect pin

4.3. System Bus Connection Terminals

Mnemonic	Type	Connected with	Description
RSTB	I	MPU	When RSTB is set to 'L', the settings are initialized. The RSTB signal low level performs the reset operation.
CSB	I		This is the chip select signal. When CSB = 'L', the chip select becomes active, and data/command I/O is enabled.
RS	I		This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. RS = 'H': Indicates DB7 - 0 is display data. RS = 'L': Indicates DB7 - 0 is control data.
E (RD)	I		6800-series interface (E) A start signal for reading or writing data in parallel mode 8080-series interface (RD) Read enable signal input pin (low active)
RW (WR)	I		6800-series interface (R/W) A signal for selecting read or write actions in parallel mode 1: Read, 0: Write. 8080-series interface (WR) Write enable signal input pin (low active) This pin can't floating and must be connected to VDD or VSS when use for serial or I^2C interface mode.

<table>
<tr><th>Mnemonic</th><th>Type</th><th>Connected with</th><th>Description</th></tr>
<tr><td>DB7(SI)
DB6(SCL)
DB5
DB4
DB3
DB2
DB1
DB0</td><td>I/O</td><td>MPU</td><td>For 8-bit parallel interface mode :
DB[7:0] : Bi-direction data bus
For 4-bit parallel interface mode :
DB[7:4] : Bi-direction data bus
DB[3:0] : must be connect to VDD or VSS
For 3-Wire / 4-Wire SPI Interface Mode
DB7(SI) : Serial input data
DB6 (SCL) : Serial input clock
DB[5:0] are high impedance.
For I^{2}C Interface Mode
DB7 (SI_IN) : Serial input data
DB6(SCLK) : Serial input clock
DB5 (SI_OUT) : Serial data acknowledge output pin
DB4(SA1), DB3(SA0) : Slave address for I^{2}C Interface Mode
DB7, DB5 must be connected together (SI) for normally I^{2}C Interface Mode .
DB[2:0] are high impedance.</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td rowspan="6">VDD/VSS</td><td>Interface modes can be selected by PS[2:0] when EXT is VDD or VSS
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>X</td><td>6800 series parallel Interface Mode</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>8080 series parallel Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4-Wire SPI Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-Wire SPI Interface Mode</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>I^{2}C Interface Mode</td></tr>
</table></td></tr>
<tr><td>EXT</td><td>I</td><td>Extra Instruction Set Select
0 : Instruction Set can be fully compatible with SPLC782A
It is only external VOUT power supply and without ICON function.
1 : Add extra command for Icon display and others LCD control
register setting. It is only internal pump and with ICON function.</td></tr>
<tr><td>DIRC</td><td>I</td><td>COM direction selection input
0 : COM1 → COM2 → . . . → COM16 → COMI1(COMI2)
1 : COM16 → COM15 → . . . → COM1 → COMI1(COMI2)</td></tr>
<tr><td>SHL</td><td>I</td><td>SEG direction selection input
0 : SEG1 → SEG2 → . . . → SEG80
1 : SEG80 → SEG79 → . . . → SEG1</td></tr>
<tr><td>BIAS</td><td>I</td><td>Bias Select
0 : 1/4 Bias
1 : 1/5 Bias</td></tr>
<tr><td>MOD1
MOD0</td><td>I</td><td>CGROM / CGRAM Mode Select
<table>
<tr><th>MOD1</th><th>MOD0</th><th>Function</th></tr>
<tr><td>1</td><td>1</td><td>$00 ~ $0F as CGRAM</td></tr>
<tr><td>1</td><td>0</td><td>$00 ~ $07 as CGRAM, $08 ~ $0F as CGROM</td></tr>
<tr><td>0</td><td>1</td><td>$00 ~ $03 as CGRAM, $04 ~ $0F as CGROM</td></tr>
<tr><td>0</td><td>0</td><td>$00 ~ $0F as CGROM</td></tr>
</table></td></tr>
</table>

4.4. Liquid Crystal Drive terminals

Mnemonic	Type	Connected with	Description
SEG1 - SEG80	O	LCD	Segment signals for LCD.
COM1 - COM16	O	LCD	Common signals for LCD.
COMI1 COMI2	O	LCD	Icon Common signals for LCD.
OSC1	I	Open	For external clock operation, the clock is input to OSC1. For internal clock operation mode, kept floating of this pin
OSCSEL	I	VDD/VSS	Oscillator source select 0 : Internal oscillator clock mode 1 : External clock mode
TEST[0:7]	I	Open	Test Pin, not accessible to user, must be left open

5. FUNCTIONAL DESCRIPTIONS

5.1. The MPU Interface

5.1.1. SELECTING THE INTERFACE TYPE

There are several types of data operations: 4-bit, 8-bit, 3-Wire SPI, 4-Wire SPI and I^2C Interface operations.

SPLC792A provides (1) 8bit / 4bit 6800 MCU interface.

(2) 8bit / 4bit 8080 MCU interface

(3) 3-wire / 4-wire Serial interface.

(4) I^2C interface.

The selection of a given interfaces are done by setting PS2, PS1 and PS0 pins as shown in Table 5-1 and Table 5-2

Table 5-1

PS2	PS1	PS0	Interface
0	0	X	6800 series 8-bit / 4-bit parallel interface mode
0	1	X	8080 series 8-bit / 4-bit parallel interface mode
1	0	0	4-Wire SPI Interface Mode
1	0	1	3-Wire SPI Interface Mode
1	1	X	I^2C -bus interface mode

'X' indicates fixed to either 'H' or to 'L'

Table 5-2

PS2	PS1	PS0	DL*	Interface	CSB	RS	E	RW	DB[7:0]
0	0	X	1	6800 series 8-bit parallel interface mode	CSB	RS	E	R/W	DB[7:0]
0	0	X	0	6800 series 4-bit parallel interface mode	CSB	RS	E	R/W	DB[7:4] DB[3:0] : must be connect to VDD or VSS
0	1	X	1	8080 series 8-bit parallel interface mode	CSB	RS	/RD	/WR	DB[7:0]
0	1	X	0	8080 series 4-bit parallel interface mode	CSB	RS	/RD	/WR	DB[7:4] DB[3:0] : must be connect to VDD or VSS

PS2	PS1	PS0	DL*	Interface	CSB	RS	E	RW	DB[7:0]
1	0	0	X	4-Wire SPI Interface Mode	CSB	RS	(Hi-Z)	(Hi-Z)	DB7(SI) DB6(SCL) DB[5:0] (Hi-Z)
1	0	1	X	3-Wire SPI Interface Mode	CSB	(Hi-Z)	(Hi-Z)	(Hi-Z)	DB7(SI) DB6(SCL) DB[5:0] (Hi-Z)
1	1	X	X	I^2C -bus interface mode	(Hi-Z)	(Hi-Z)	(Hi-Z)	(Hi-Z)	DB7 (SI_IN) DB6 (SCL) DB5 (SI_OUT) DB4(SA1), DB3(SA0) DB7, DB5 must be connected together. DB[2:0] (Hi-Z)

'X' indicates fixed to either 'H' or 'L'

'DL* ': Software Function set (see the 6.8 Instruction Table (EXT=0) & 6.9 Instruction Table(EXT=1))

DL : Set the interface data length (8-bit/4-bit)

5.1.2. The parallel interface

The type of data transfer is determined by signals at RS, E and RW as shown in **Table 5-3** and **Table 5-4**.

Table 5-3 6800-series

RS	E	RW	Description
1	**1**	1	Read 8-bits / 4-bits display data (DB7 to DB0)
1	↓	0	Write 8-bits / 4-bits display data (DB7 to DB0)
0	**1**	1	Read 8-bits / 4-bits command (DB7 to DB0)
0	↓	0	Write 8-bits / 4-bits command (DB7 to DB0)

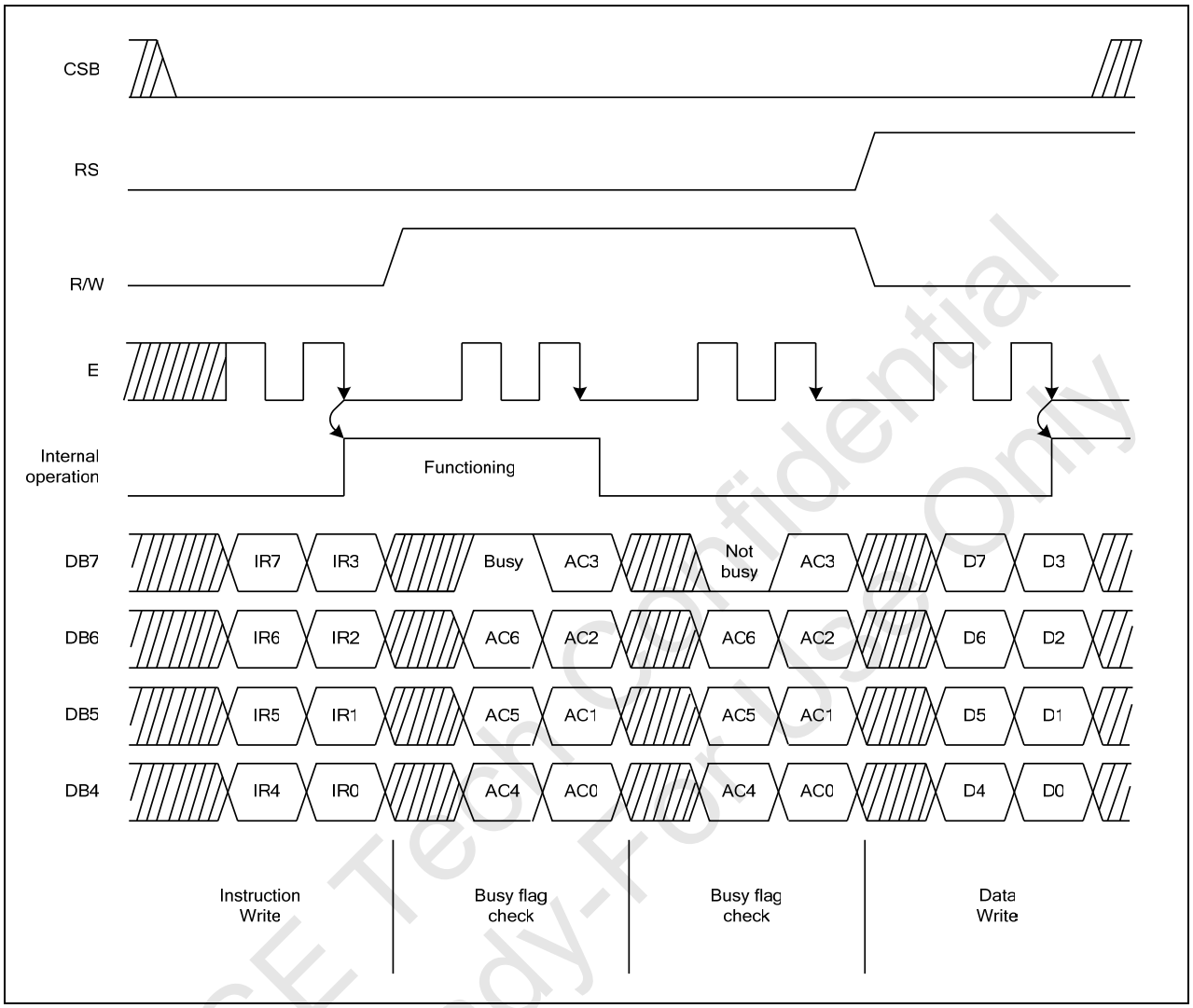
Table 5-4 8080-series

RS	E	RW	Description
1	1	↑	Write 8-bits / 4-bits display data (DB7 to DB0)
1	**0**	1	Read 8-bits / 4-bits display data (DB7 to DB0)
0	1	↑	Write 8-bits / 4-bits command (DB7 to DB0)
0	**0**	1	Read 8-bits / 4-bits command (DB7 to DB0)

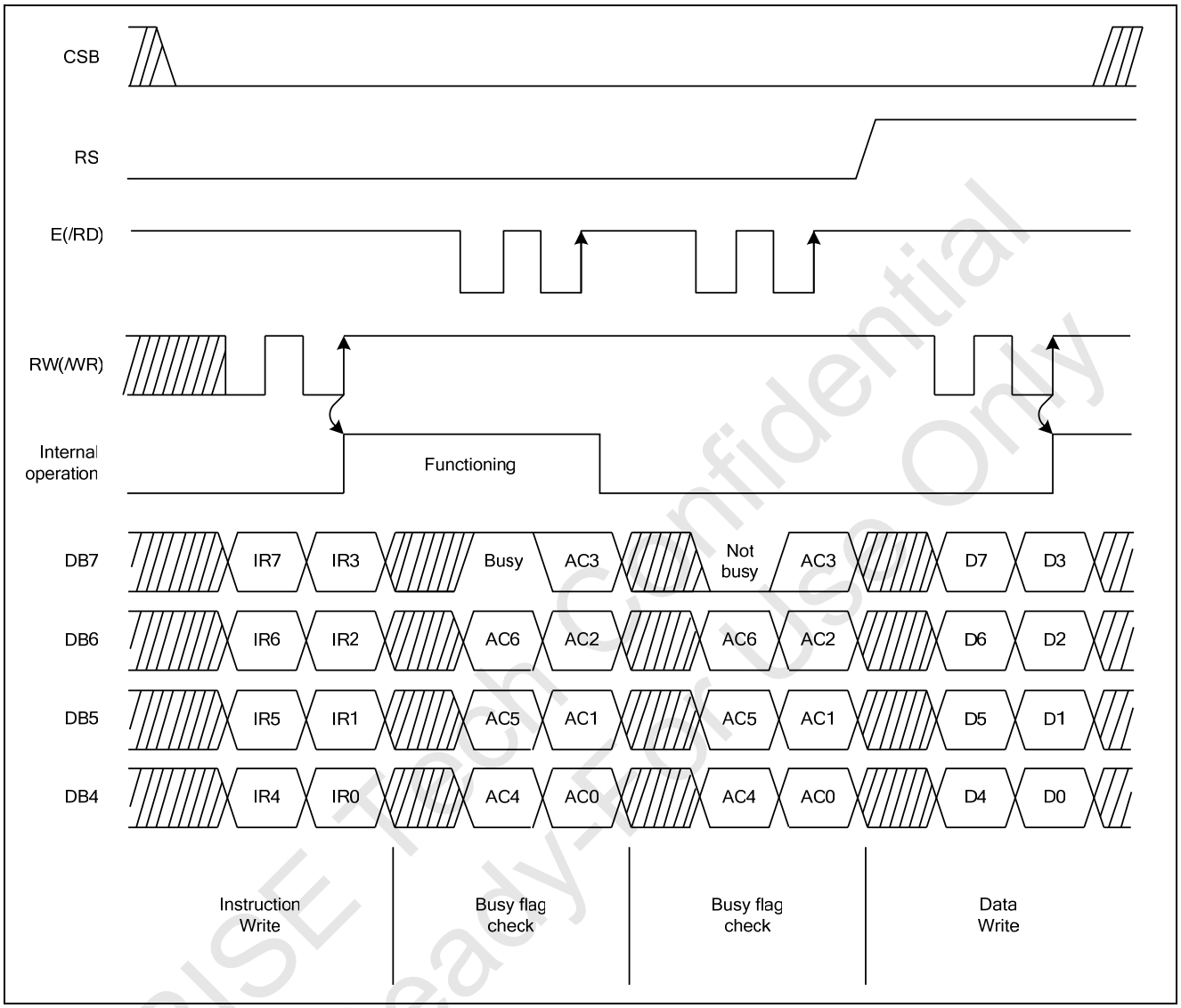
5.2. 4-bit interface mode

Using 4-bit MPU, the interfacing 4-bit data is transferred by 4-bus line (DB4 to DB7). Thus, DB0 to DB3 bus lines are not used. Using 4-bit MPU to interface 8-bit data requires two times transferring. First, the higher 4-bit data is transferred by 4-bus line (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4-bus line (for 8-bit operation, DB3 to DB0). The 4-bit data transfer order will be set as higher 4-bit data first by two method : To set the CSB pin as VDD or RESET pin as VSS

The CSB can't not go VDD before the whole 8-bit data be transferred by two times transferring.



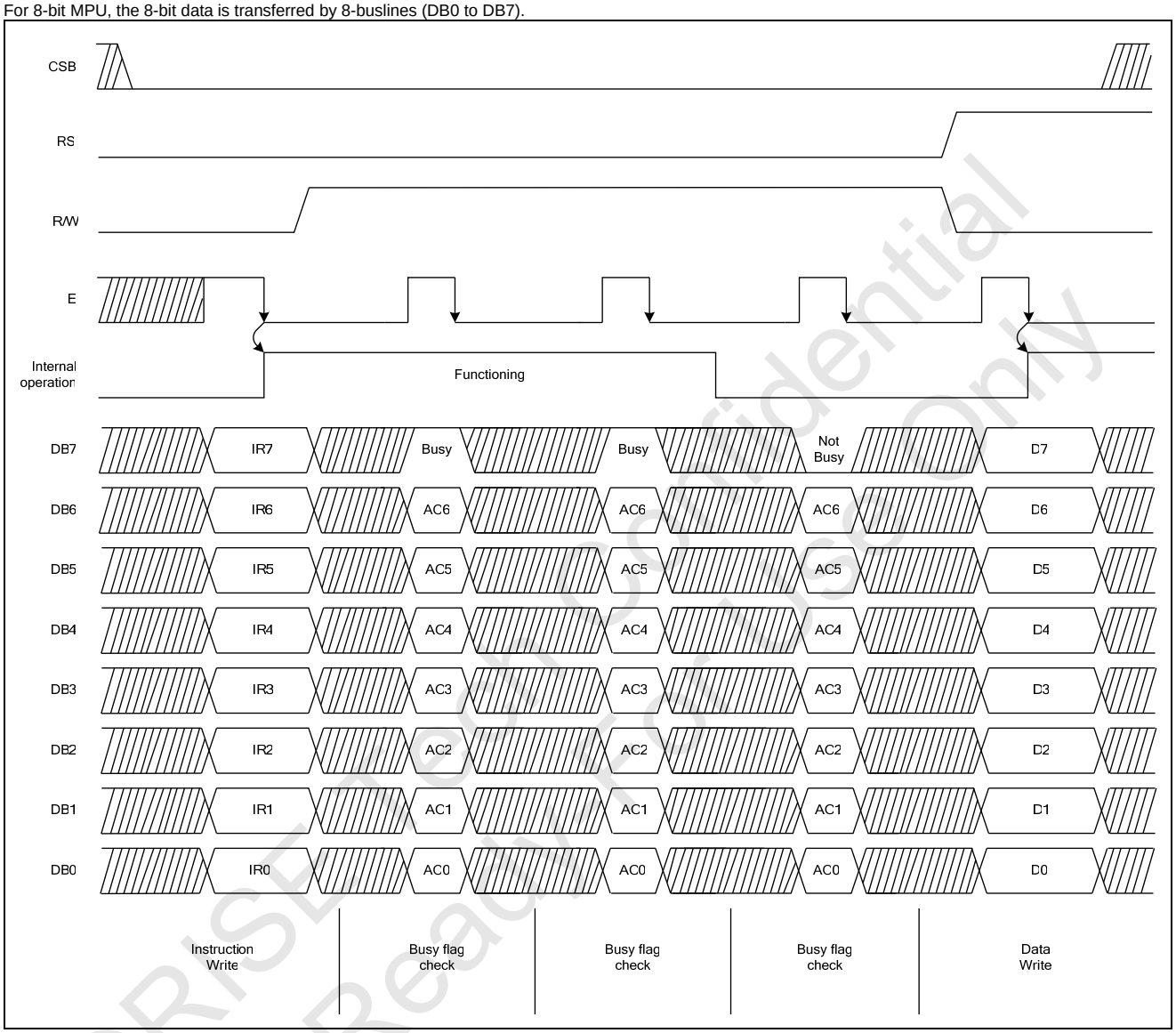
Example of 4-bit Data Transfer Timing Sequence (68 series MPU Mode)



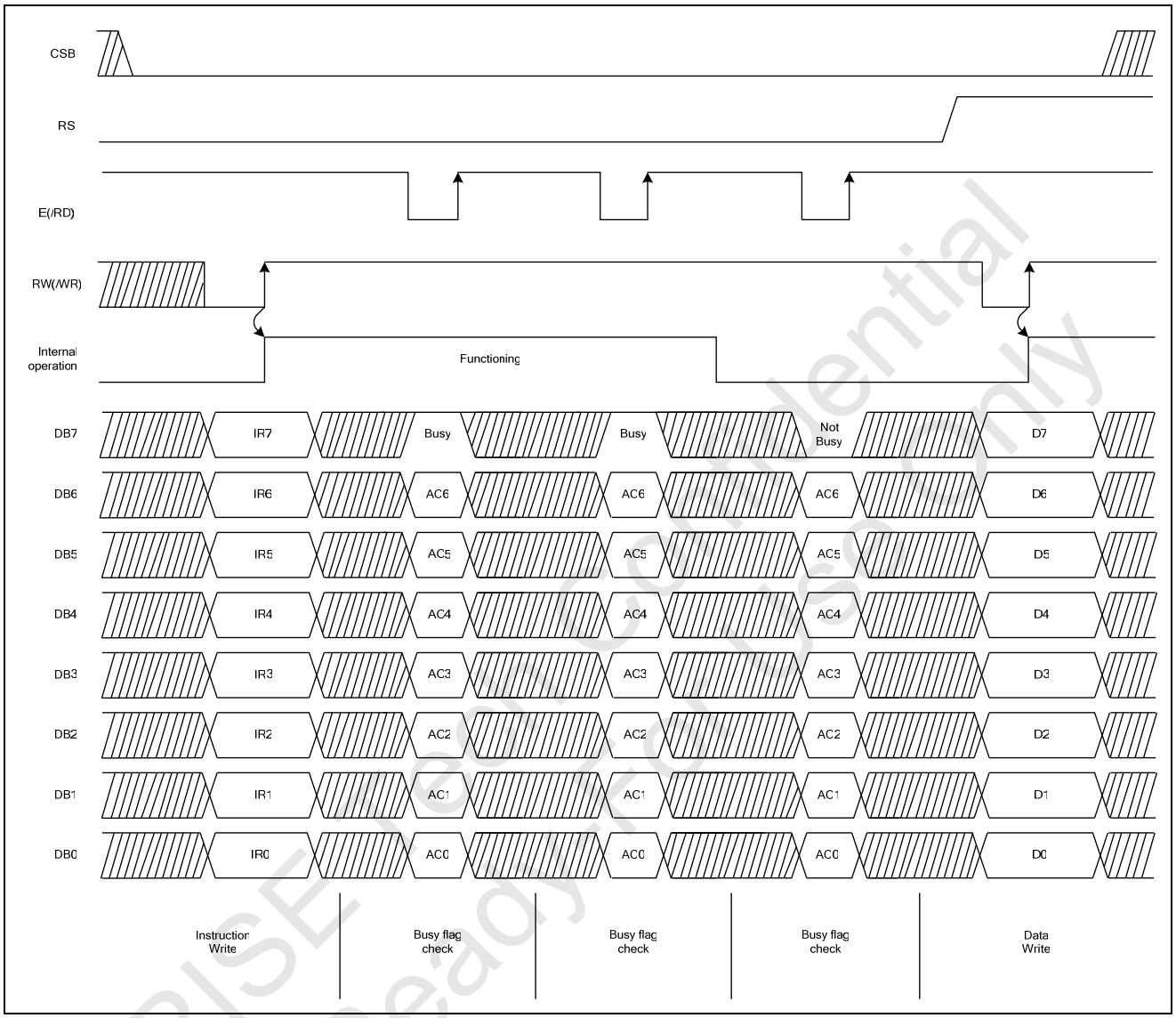
Example of 4-bit Data Transfer Timing Sequence (80 series MPU Mode)

5.3. 8-bit interface mode

For 8-bit MPU, the 8-bit data is transferred by 8-buslines (DB0 to DB7).



Example of 8-bit Data Transfer Timing Sequence (68 series MPU Mode)



Example of 8-bit Data Transfer Timing Sequence (80 series MPU Mode)

5.3.1. The serial interface

The serial interface is a 3-wires/ 9-bits or 4-wires/ 8-bts bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-wires serial use: CSB, SI (DB7) and SCL (DB6) and the 4-wires serial use: CSB, RS, SI (DB7) and SCL (DB6) is used for interface with MCU only, so it can be stopped when no communication is necessary. The serial interface are 3-wire / 4-wire SPI interface face mode and I^2C-bus interface mode, it is only support write function mode, it is not support read function mode.

5.3.2. 4-wires SPI interface

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 4-wires serial data packet contains just transmission byte and control bit RS is transferred by the RS pin.. If RS is “low”, the transmission byte is interpreted as a command byte. If RS is “high”, the transmission byte is stored in the display data RAM (Memory write command).The read feature is not supported in 4-wires SPI mode.

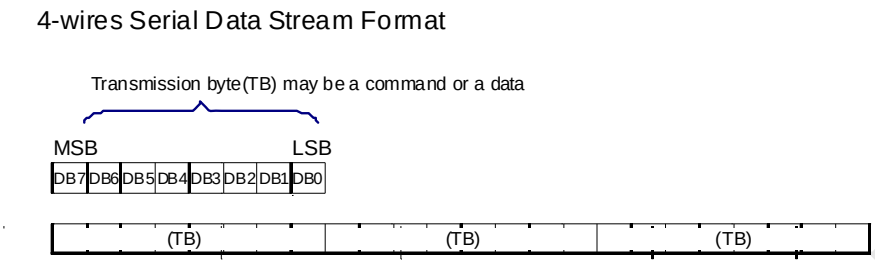


Figure 5-1 4-wires serial data stream format

Serial data on SI is latched at the rising edge of serial clock on SCL. After the eighth serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

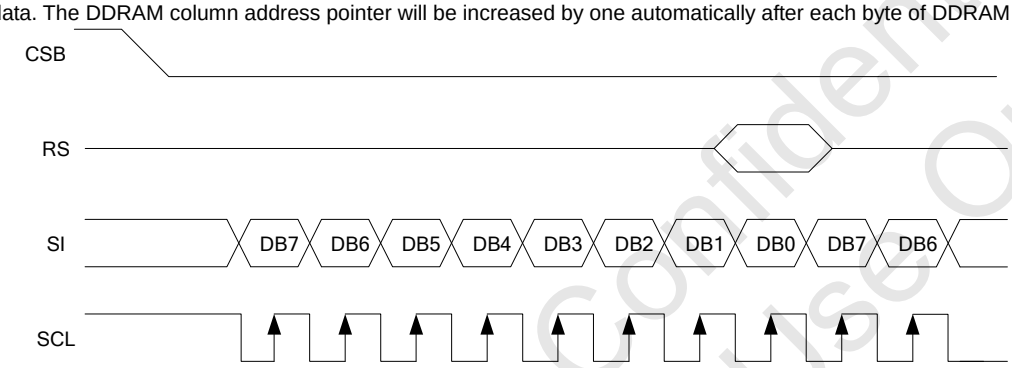


Figure 5-2 4-wires SPI timing

The serial interface is initialized when CSB is high status. In this state, the internal 8-bit shift register and the 3-bit counter are reset. A falling edge on CSB enables the serial interface and indicates the start of data transmission.

5.3.3. 3-wires SPI interface

The 3-wires serial data packet contains a control bit A0 and a transmission byte. The control bit A0 indicates, whether the byte is command code (A0="0") or RAM data (A0="1").The read feature is not supported in 3-wires SPI mode.

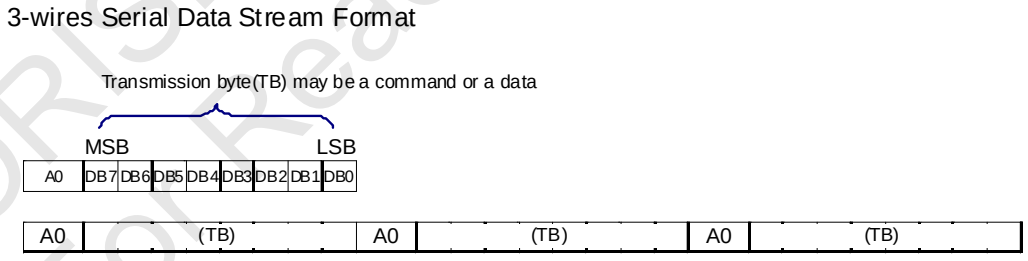


Figure 5-3 3-wires serial interface data stream format

The serial interface is initialized when CSB is high status. In this state, the internal 8-bit shift register and the 3-bit counter are reset. A falling edge on CSB enables the serial interface and indicates the start of data transmission.

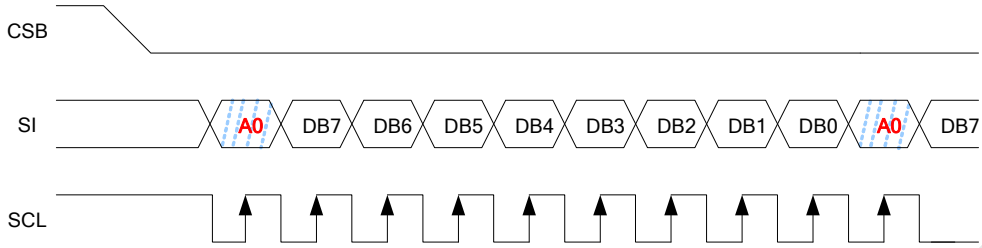


Figure 5-4 3-wires serial interface data stream format

5.3.4. I²C interface

The SPLC792A receives commands or RAM data and sent RAM data via the I²C interface. The communication between different devices is via two bi-directional wires, SI and SCL. Both wires are connected to positive supply voltage via pull-up resistor respectively.

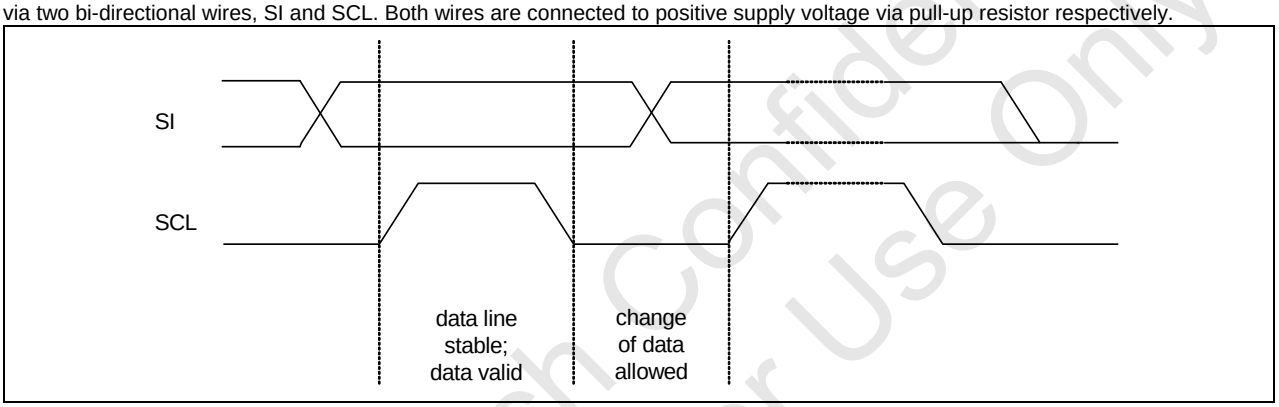


Figure 5-5 Bit transfer on I²C I/F

Figure 5-5 During the HIGH period of the SCL, the change in the SI wire at this time will be interpreted as a control signal. The valid data on the SI wire must remain stable during this time. The change of data only allowed at LOW period of the SCL.

The START condition (S) is a HIGH to LOW transition on SI wire when SCL at HIGH period. A LOW to HIGH transition on SI wire at the SCL is HIGH that is defined as the STOP condition (P) (see Figure 5-6). When the I²C bus is not busy, both SI and SCL are to keep HIGH.

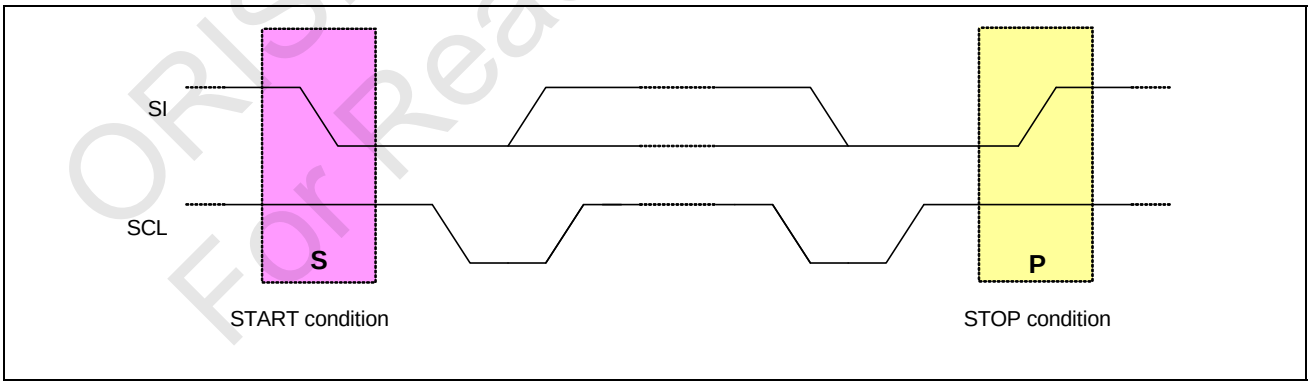


Figure 5-6 START and STOP conditions on I²C I/F

Every byte put on the SI wire must be 8-bits long. Each byte must be followed by an acknowledge bit. The master generates an extra acknowledge-related clock pulse. At this time, the transmitter releases the SI wire (HIGH). At the same time, a slave receiver which has been addressed must pull down the SI wire so that it remains stable LOW (see Figure 5-7). Also, set-up time and hold time must be taken into account. A master receiver has to signal the end of data to the slave transmitter by not generating acknowledge on the last byte that was clocked out of the slave. The slave transmitter has to release the SI wire so that the master to generate a STOP condition or repeated START condition.

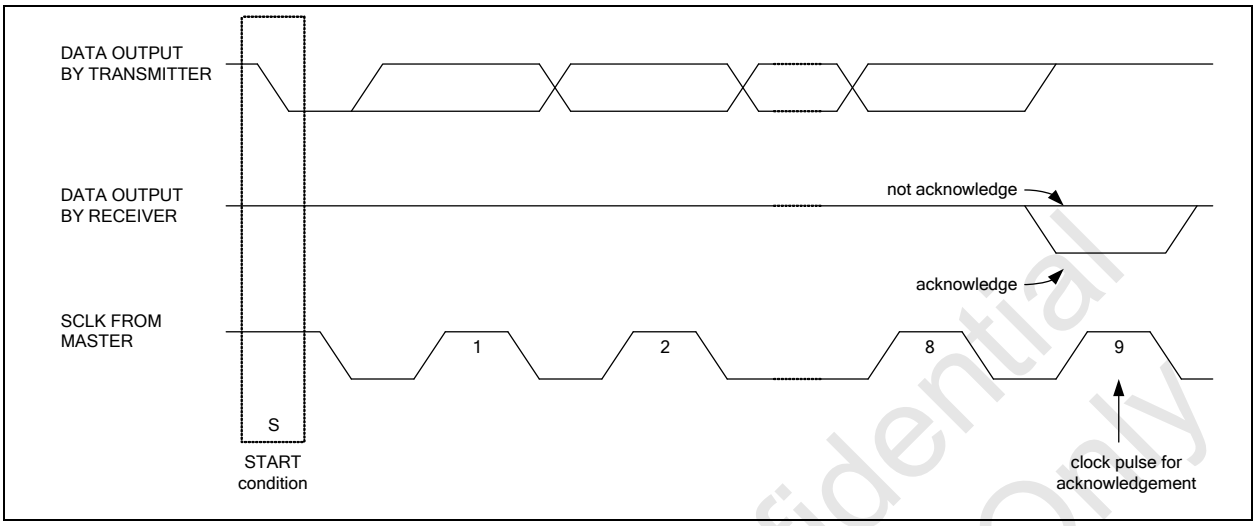


Figure 5-7 Acknowledgement on the I²C-bus I/F

The I²C Bus system configuration is show in Figure 5-8. The Table 5-5 is the definition of I²C bus terminology.

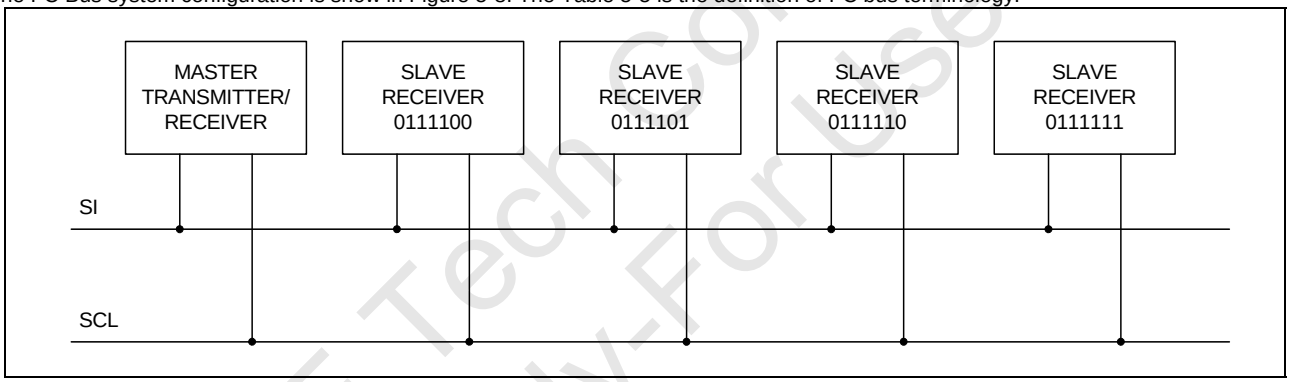


Figure 5-8 System configuration

Table 5-5

NO.	TREM	Description
1	Transmitter	The device which sends the data to the bus
2	Receiver	The device which receives the data from the bus
3	Master	The device which initiates a transfer, generates clock signals and terminates a transfer
4	Slave	The device addressed by a master
5	Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
6	Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
7	Synchronization	Procedure to synchronize the clock signals of two or more devices

The SPLC792A supports command and data write. Before any data is transmitted on the I²C -bus, the device to respond is addressed first. The slave address is made up by the first seven bits of the first byte. The eighth bit of the first byte determines the direction of the message (only write). Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the SPLC792A. The least two bit of the slave address is set by connecting the input SA1 and SA0 to either logic “0” (VSS) or “1”(VDD).

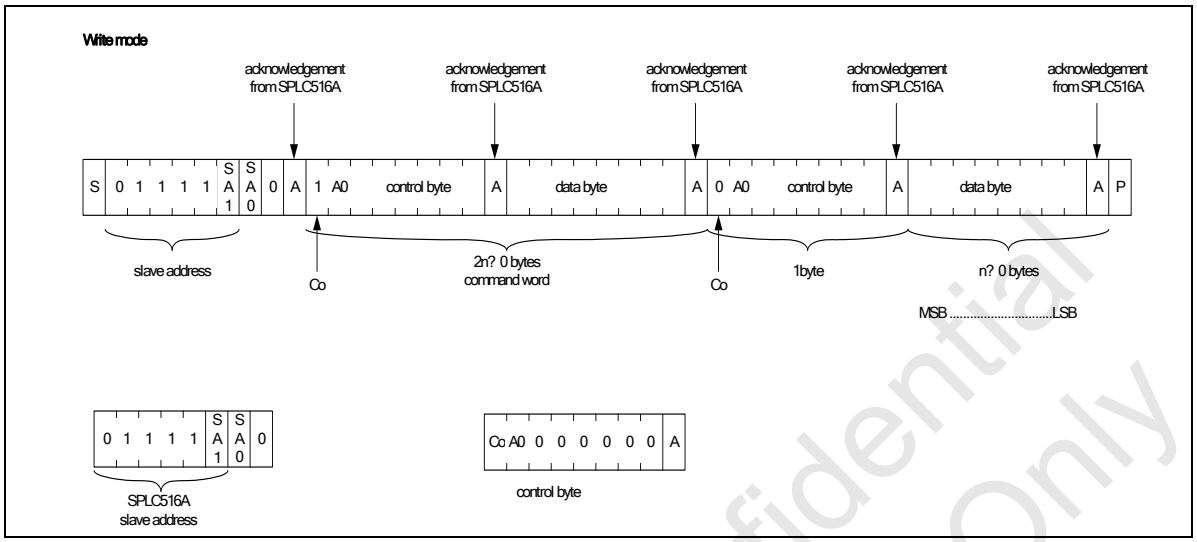


Figure 5-9 I²C interface protocol

The sequence is initiated by a START condition (S) from the I²C -bus master. After the START condition procedure is done. The slave address will be transmitted. All slaves with the corresponding address acknowledge in parallel, and all others will ignore the I²C -bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte and a data byte. In control byte, the first two bits described Co and A0 respectively (see Figure 5-9).
The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only the data bytes will follow. The state of the A0-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the A0 bit setting, either a series of display data bytes or command data bytes may follow. If the A0 bit is set to “1”, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SPLC792A device. If the A0 bit of the last control byte is set to “0”, these command bytes will be decoded and the setting of the device will be changed based on the received commands. The acknowledgement after each byte is made only by the addressed slave. The I²C -bus master issues a stop condition (P) at the end of the transmission.

5.4. Oscillator

The SPLC792A supports external and internal oscillator operation mode. It doesn’t need any external resistor for internal oscillator mode.

5.5. Control and Display Instructions

Control and display instructions are described in details as follows:

5.5.1. Clear display

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

It clears the entire display and sets Display Data RAM Address 0 in Address Counter.
Maximum execution time 1.0us

5.5.2. Return home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

X: Do not care (0 or 1)

It sets Display Data RAM Address 0 in Address Counter and the display returns to its original position. The cursor or blink goes to the most-left side of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

Maximum execution time 1.0us

5.5.3. Entry mode set

During writing and reading data, it defines cursor moving direction and shifts the display.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

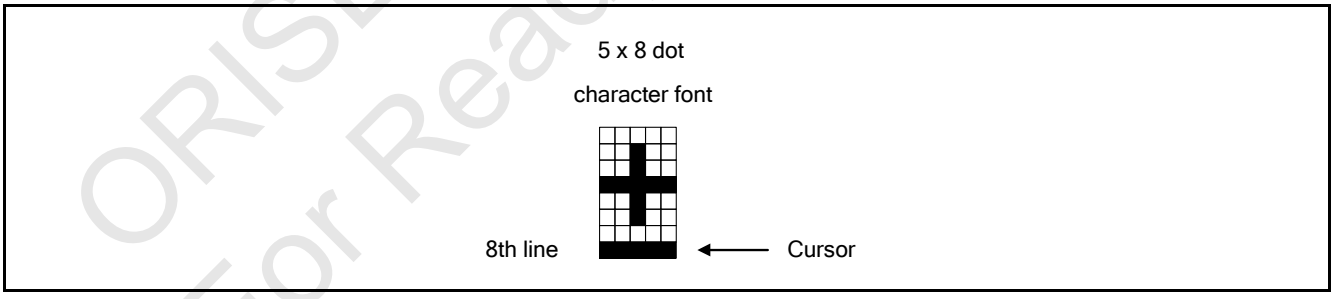
5.5.4. Display ON/OFF control

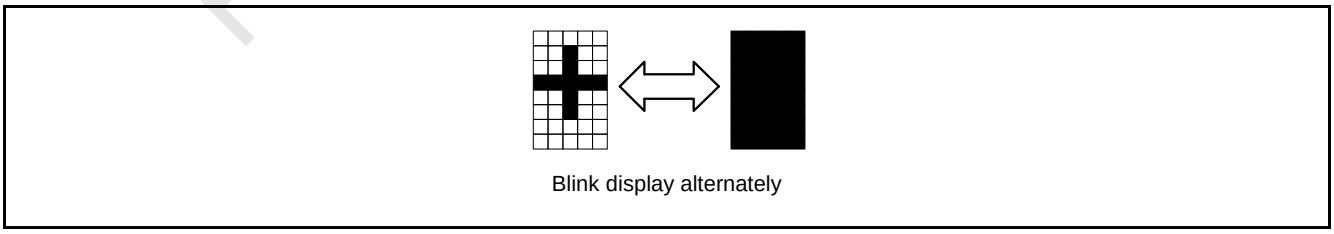
RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

B = 1: Blinks on, B= 0: Blinks off





5.5.5. Cursor or display shift

Without changing DD RAM data, it moves cursor and shifts display.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

X: Do not care (0 or 1)

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

5.5.6. Function set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	X	X	X

X: Do not care (0 or 1)

DL: It sets the interface data length

DL = 1: Data transferred with 8-bit length (DB7 - 0).

DL = 0: Data transferred with 4-bit length (DB7 - 4).

It requires two times to accomplish data transferring at 4-bit interface mode.

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	DH	0	IS

DH: It sets the double height font display mode.

DH = 0: Normal mode display.

DH = 1: Double height mode display.

IS: It sets the Instruction Register for extension command use.

EXT	N	DH	No. of Display Lines	Character Font	Duty Factor
0	0	X	1	5 x 8 dots	1 / 8
0	1	X	2	5 x 8 dots	1 / 16
1	0	0	1	5 x 8 dots	1 / 9
1	1	0	2	5 x 8 dots	1 / 17
1	0	1	1	5 x 16 dots	1 / 9
1	1	1	1	5 x 16 dots	1 / 17

Note : It must set N=1 for double height mode operation, because the LCD display area will be disable at COM9 ~ COM16 while one line (N=0) and double height mode (DH=1) is selected.

5.5.7. Set character generator RAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	a	a	a	a	a	a

It sets Character Generator RAM Address $(aaaaaa)_2$ to the Address Counter.

Character Generator RAM data can be written after this setting. It's also can be read when using the 4-bit or .8-bit parallel interface mode .

5.5.8. Set display data RAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	a	a	a	a	a	a	a

It sets Display Data RAM Address $(aaaaaaa)_2$ to the Address Counter.

Display data RAM data can be written after this setting. It's also can be read when using the 4-bit or .8-bit parallel interface mode.

In one-line display (N = 0),

$(aaaaaaa)_2$: $(00)_{16}$ - $(4F)_{16}$.

In two-line display (N = 1),

$(aaaaaaa)_2$: $(00)_{16}$ - $(27)_{16}$ for the first line,

$(aaaaaaa)_2$: $(40)_{16}$ - $(67)_{16}$ for the second line.

5.5.9. Set Icon RAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	a	a	a	a

It sets Icon RAM Address $(aaaa)_2$ to the Address Counter.

Icon RAM data can be written after this setting. It's also can be read when using the 4-bit or 8-bit parallel interface mode .

5.5.10. Read busy flag and address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	a	a	a	a	a	a	a

When BF = 1, it indicates the system is busy now and it will not accept any instruction until not busy (BF = 0). At the same time, the content of Address Counter $(aaaaaaa)_2$ is read.

5.5.11. Write data to character generator RAM, display data RAM or Icon RAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	d	d	d	d	d	d	d	d

It writes data $(dddddddd)_2$ to display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	X	X	X	d	d	d	d	d

It writes data $(ddddd)_2$ to character generator RAM or Icon RAM.

5.5.12. Read data from character generator RAM or display data RAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	d	d	d	d	d	d	d	d

It reads data $(dddddddd)_2$ from display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	X	X	X	d	d	d	d	d

It reads data $(ddddd)_2$ from character generator RAM or Icon RAM

To read data correctly, do the following:

1). Set the address of the Character Generator RAM, Display Data RAM, Icon RAM or shift the cursor instruction.

2). The " Read " instruction.

5.5.13. ICON and LCD control

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	Ion	X	C5	C4

X: Do not care (0 or 1)

Ion: Icon display control.

Ion = 0: Icon display off (Default)

Ion = 1: Icon display on

C[5:0]: Contrast adjust for internal voltage regulator mode

5.5.14. Voltage control

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	-	Rab2	Rab1	Rab0

Rab[2:0]: Voltage Regulator amplified ratio

Rab2	Rab1	Rab0	Amplified ratio (1 + Rb / Ra)
0	0	0	1.818
0	0	1	2.222
0	1	0	2.667
0	1	1	3.333
1	0	0	3.636
1	0	1	4.000
1	1	0	4.444
1	1	1	5.000

(Default of Rab[2:0] = 011, Amplified ratio = 3.333)

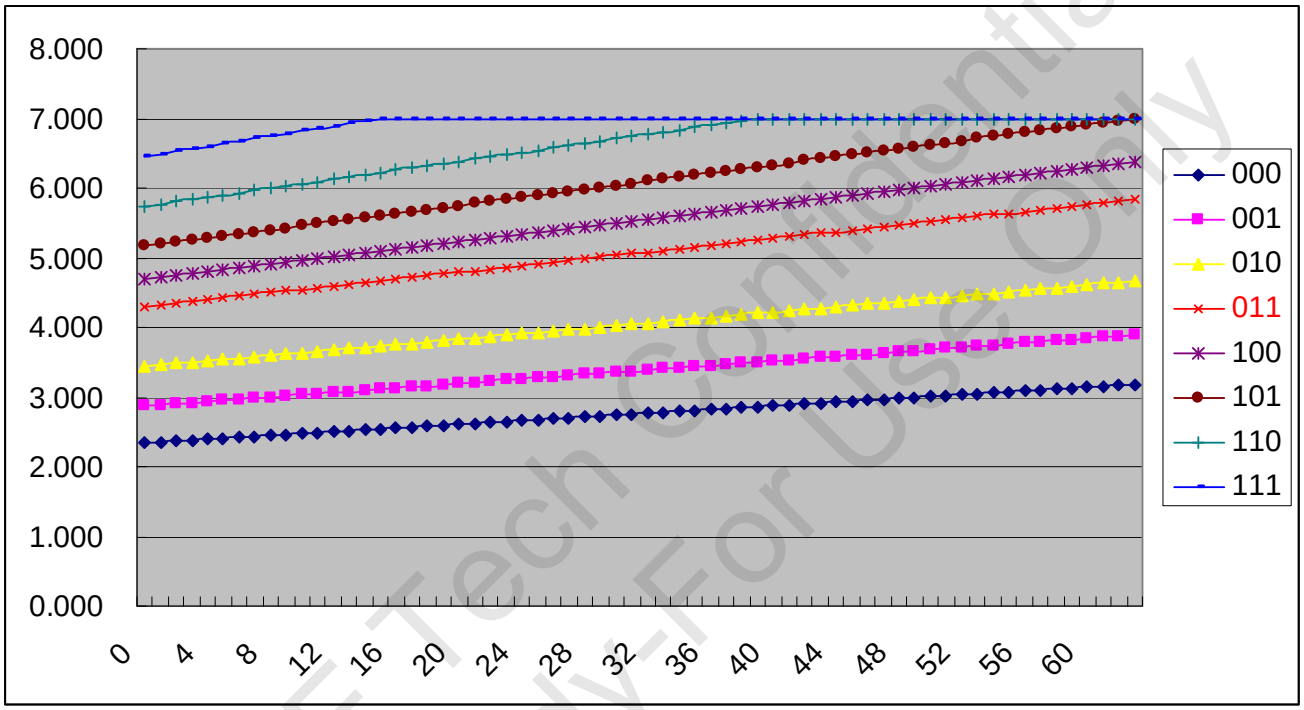
5.5.15. Contrast control

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	C3	C2	C1	C0

C[5:0]: Contrast adjust for internal voltage regulator mode

VLCD = Vref x (1 + Rb/Ra), Vref =1.75V x (177 + a) / 240,

(Default of C[5:0] = [100000])



5.6. Display Data RAM (DD RAM)

The 80-bit DD RAM is normally used for storing display data. Its address is configured in the Address Counter. The relationships between Display Data RAM Address and LCD's position are depicted as follows.

1-line display mode, 80 display characters data store in DDRAM

1	2	3	4	5	6	...	79	80	← Display position
00	01	02	03	04	05	- - - - - - - - - - - - - - - - - - - -	4E	4F	← Display data RAM address

(Example) 1-line display, 16 display characters

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display position
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← Display data RAM address

When the display shift operation is performed, the display data RAM's address moves as :

(i) Left shift

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

(ii) Right shift

4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

2-line display mode, 80 display characters data store in DDRAM

1	2	3	4	5	6		38	39	40	← Display position
00	01	02	03	04	05	- - - - - - - - - - - - - - - - - - - -	25	26	27	← Display data RAM
40	41	42	43	44	45	- - - - - - - - - - - - - - - - - - - -	65	66	67	← Display data RAM

(Example) 2-line display, 16 display characters by 2-line

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display position
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← Display data RAM
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	← Display data RAM

When the display shift operation is performed, the display data RAM's address moves as :

(i) Left shift

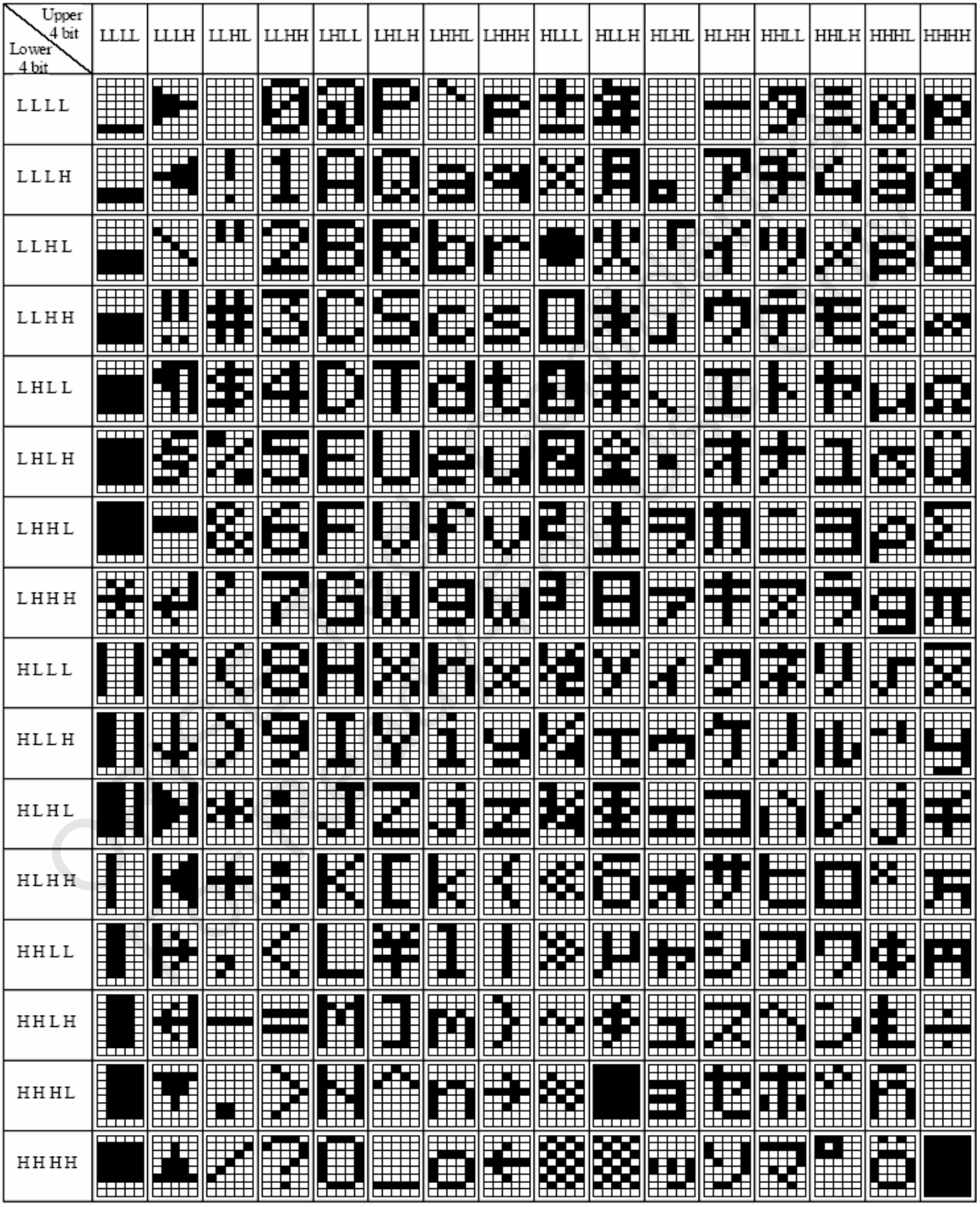
01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(ii) Right shift

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

5.7. Character Generator ROM (CG ROM)

The character generator ROM generates 5 x 8 dots 256 characters. The address (00h – 0Fh) can be use for CGRAM display.



5.8. Character Generator RAM (CG RAM)

Users can easily change the character patterns in the character generator RAM through program. It can be written to 5 x 8 dots, 8-character patterns. By writing font data to CGRAM, user-defined character can be applied.

5.8.1. Relationship between character code (DDRAM) and character pattern (CGRAM)

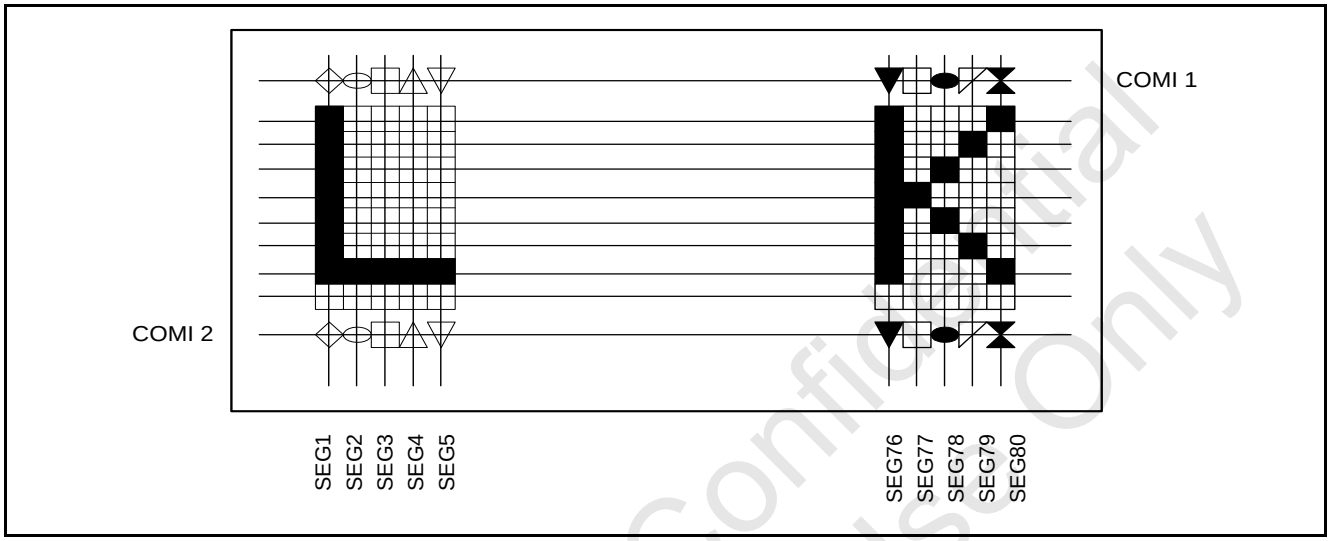
Character code (DDRAM data)								DD/CGRAM address							CGRAM data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0 (00h)	1	0	0	0	0	0	0	-	-	-	0	1	0	1	0	Pattern 1
								1	0	0	0	0	0	1	-	-	-	1	0	1	0	1	
								1	0	0	0	0	1	0	-	-	-	0	1	0	1	0	
								1	0	0	0	0	1	1	-	-	-	1	0	1	0	1	
								1	0	0	0	1	0	0	-	-	-	0	1	0	1	0	
								1	0	0	0	1	0	1	-	-	-	1	0	1	0	1	
								1	0	0	0	1	1	0	-	-	-	0	1	0	1	0	
								1	0	0	0	1	1	1	-	-	-	1	0	1	0	1	
0	0	0	0	0	0	0	1 (01h)	1	0	0	1	0	0	0	-	-	-	0	0	0	0	0	Pattern 2
								1	0	0	1	0	0	1	-	-	-	1	1	1	1	1	
								1	0	0	1	0	1	0	-	-	-	0	0	0	0	0	
								1	0	0	1	0	1	1	-	-	-	1	1	1	1	1	
								1	0	0	1	1	0	0	-	-	-	0	0	0	0	0	
								1	0	0	1	1	0	1	-	-	-	1	1	1	1	1	
								1	0	0	1	1	1	0	-	-	-	0	0	0	0	0	
								1	0	0	1	1	1	1	-	-	-	1	1	1	1	1	
0	0	0	0	0	0	1	0 (02h)	1	0	1	0	0	0	0	-	-	-	0	1	0	1	0	Pattern 3
								1	0	1	0	0	0	1	-	-	-	0	1	0	1	0	
								1	0	1	0	0	1	0	-	-	-	0	1	0	1	0	
								1	0	1	0	0	1	1	-	-	-	0	1	0	1	0	
								1	0	1	0	1	0	0	-	-	-	0	1	0	1	0	
								1	0	1	0	1	0	1	-	-	-	0	1	0	1	0	
								1	0	1	0	1	1	0	-	-	-	0	1	0	1	0	
								1	0	1	0	1	1	1	-	-	-	0	1	0	1	0	
0	0	0	0	0	0	1	1 (03h)	1	0	1	1	0	0	0	-	-	-	0	1	1	1	0	Pattern 4
								1	0	1	1	0	0	1	-	-	-	1	0	1	0	1	
								1	0	1	1	0	1	0	-	-	-	1	1	0	1	1	
								1	0	1	1	0	1	1	-	-	-	1	0	1	0	1	
								1	0	1	1	1	0	0	-	-	-	0	1	1	1	0	
								1	0	1	1	1	0	1	-	-	-	1	1	1	1	1	
								1	0	1	1	1	1	0	-	-	-	1	1	1	1	1	
								1	0	1	1	1	1	1	-	-	-	1	1	1	1	1	

Character code (DDRAM data)								DD/CGRAM address							CGRAM data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
								1	1	0	0	0	0	0	-	-	-	1	1	0	1	0	
								1	1	0	0	0	0	1	-	-	-	1	0	0	0	1	
								1	1	0	0	0	1	0	-	-	-	0	0	0	0	0	
0	0	0	0	0	1	0	0	1	1	0	0	0	1	1	-	-	-	1	0	0	0	1	Pattern 5
			(04h)					1	1	0	0	1	0	0	-	-	-	1	1	0	1	1	
								1	1	0	0	1	0	1	-	-	-	1	1	1	1	1	
								1	1	0	0	1	1	0	-	-	-	1	1	1	1	1	
								1	1	0	0	1	1	1	-	-	-	1	1	1	1	1	
								1	1	0	1	0	0	0	-	-	-	1	1	1	1	1	
								1	1	0	1	0	0	1	-	-	-	1	1	1	1	1	
								1	1	0	1	0	1	0	-	-	-	0	0	0	0	0	
0	0	0	0	0	1	0	1	1	1	0	1	0	1	1	-	-	-	0	0	0	0	0	Pattern 6
			(05h)					1	1	0	1	1	0	0	-	-	-	1	1	1	1	1	
								1	1	0	1	1	0	1	-	-	-	1	1	1	1	1	
								1	1	0	1	1	1	0	-	-	-	0	0	0	0	0	
								1	1	0	1	1	1	1	-	-	-	0	0	0	0	0	
								1	1	1	0	0	0	0	-	-	-	0	0	1	1	0	
								1	1	1	0	0	0	1	-	-	-	0	0	1	1	0	
								1	1	1	0	0	1	0	-	-	-	0	0	1	1	0	
0	0	0	0	0	1	1	0	1	1	1	0	0	1	1	-	-	-	0	0	1	1	0	Pattern 7
			(06h)					1	1	1	0	1	0	0	-	-	-	0	0	1	1	0	
								1	1	1	0	1	0	1	-	-	-	0	0	1	1	0	
								1	1	1	0	1	1	0	-	-	-	0	0	1	1	0	
								1	1	1	0	1	1	1	-	-	-	0	0	1	1	0	
								1	1	1	1	0	0	0	-	-	-	0	0	0	0	0	
								1	1	1	1	0	0	1	-	-	-	1	0	0	0	1	
								1	1	1	1	0	1	0	-	-	-	1	1	0	1	1	
								1	1	1	1	0	1	1	-	-	-	1	0	0	0	1	
0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	-	-	-	0	0	0	0	0	Pattern 8
			(07h)					1	1	1	1	1	0	1	-	-	-	1	0	0	0	1	
								1	1	1	1	1	1	0	-	-	-	1	1	0	1	1	
								1	1	1	1	1	1	1	-	-	-	1	1	1	1	1	

Note: "-" - Don't care

5.9. Segment Icon RAM (ICONRAM)

ICONRAM contains segment control data and segment pattern data. COMI1 and COMI2 are the same signal but the name is different. As a result, the icons on the same SEG are displayed at the same time. The number of icons is 80.



Relationship between ICONRAM and Icon Display

5.9.1. Relationship between ICONRAM address and display pattern

When SHL=0, ICON RAM map refer below table

ICONRAM address	ICONRAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	-	-	-	S1	S2	S3	S4	S5
01h	-	-	-	S6	S7	S8	S9	S10
02h	-	-	-	S11	S12	S13	S14	S15
03h	-	-	-	S16	S17	S18	S19	S20
04h	-	-	-	S21	S22	S23	S24	S25
05h	-	-	-	S26	S27	S28	S29	S30
06h	-	-	-	S31	S32	S33	S34	S35
07h	-	-	-	S36	S37	S38	S39	S40
08h	-	-	-	S41	S42	S43	S44	S45
09h	-	-	-	S46	S47	S48	S49	S50
0Ah	-	-	-	S51	S52	S53	S54	S55
0Bh	-	-	-	S56	S57	S58	S59	S60
0Ch	-	-	-	S61	S62	S63	S64	S65
0Dh	-	-	-	S66	S67	S68	S69	S70
0Eh	-	-	-	S71	S72	S73	S74	S75
0Fh	-	-	-	S76	S77	S78	S79	S80

Note: "-" - Don't care

When SHL=1, ICON RAM map refer below table

ICONRAM address	ICONRAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	-	-	-	S80	S79	S78	S77	S76
01h	-	-	-	S75	S74	S73	S72	S71
02h	-	-	-	S70	S69	S68	S67	S66
03h	-	-	-	S65	S64	S63	S62	S61
04h	-	-	-	S60	S59	S58	S57	S56
05h	-	-	-	S55	S54	S53	S52	S51
06h	-	-	-	S50	S49	S48	S47	S46
07h	-	-	-	S45	S44	S43	S42	S41
08h	-	-	-	S40	S39	S38	S37	S36
09h	-	-	-	S35	S34	S33	S32	S31
0Ah	-	-	-	S30	S29	S28	S27	S26
0Bh	-	-	-	S25	S24	S23	S22	S21
0Ch	-	-	-	S20	S19	S18	S17	S16
0Dh	-	-	-	S15	S14	S13	S12	S11
0Eh	-	-	-	S10	S9	S8	S7	S6
0Fh	-	-	-	S5	S4	S3	S2	S1

Note: "-" - Don't care

5.10. Instruction Table (EXT=0)

While control pin EXT =0, the Instruction Set is description as following table. It's can be fully replace the SPLC782A

Instruction	Instruction Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.
Function Set	0	0	0	0	1	DL	N	-	-	-	DL : Set the interface data length (8-bit/4-bit) N : Set numbers of display line (N: 2-line/1-line)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read Busy Flag (BF=1 in busy state). The contents of address counter can also be read.
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM / ICONRAM).
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM / ICONRAM).
Power save mode											Display OFF(D=0) into sleep mode.

Note1: "—": don't care

Note2: The LCD duty is automatic setting as 1/8 duty for one-line display mode(N=0) while EXT=0

Note3: The LCD duty is automatic setting as 1/16 duty for two-line display mode(N=1) while the EXT=0

5.11. Instruction Table (EXT=1)

While EXT =1, the Instruction Set is description as following table. It's add Double height and some extra command

Instruction	Instruction Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor, and blinking of cursor(B) on/off control bit.
Function Set	0	0	0	0	1	DL	N	DH	0*	**IS**	DL : Set the interface data length (8-bit/4-bit) N : Set numbers of display line (N: 2-line/1-line) DH : Double Height font display IS : Extra Command setting for two difference Instruction Set switching
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read Busy Flag (BF=1 in busy state). The contents of address counter can also be read.
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM / ICONRAM).
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM / ICONRAM).
Power save mode											Display OFF(D=0) into sleep mode.
IS=0											
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.
IS=1											
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.
Icon and Booster control	0	0	0	1	0	1	Ion	-	C5	C4	Ion: ICON display on/off C5, C4: Contrast adjust high byte
Voltage control	0	0	0	1	1	0	-	Rab 2	Rab 1	Rab 0	Rab[2:0] : select voltage regulator amplified ratio. :
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast adjust for internal voltage regulator mode
Reserve command	0	0	0	0	0	0	0	-	-	-	Don't use this Instruction

Note1: "—": don't care

Note2: Function Set DB1 normal use must set 0, DB1=0 into test mode.

Note3: The LCD duty is setting as 1/9 duty for one-line display mode(N=0) while EXT=1

Note4: The LCD duty is setting as 1/17 duty for two-line display mode(N=1) while the EXT=1

5.12. Initial State after Hardware Reset

After Reset trigger, the following register will be set as the default value

Register	Default Value	Description
I/D	1	I/D = 1 : Cursor moving direction is increment
S	0	S = 0 : The display does not shift
D	0	D = 0 : Display off
C	0	C = 0 : Cursor off
B	0	B = 0 : Blinks off
DL	1	DL = 1 : 8-bit data length
N	0	N = 0 : One-line display
DH	0	DH = 0 : Normal mode display (Double height mode disable)
IS	0	IS = 0 :Instruction set mode select when EXT=1
Ion	0	Ion = 0 : Icon display off
Rab[2:0]	[1, 1, 1]	Rab[2:0] = [0, 1, 1] : Voltage regulator amplified ratio is set as 3.333
C[5:0]	[1, 0, 0, 0, 0, 0]	C[5:0] = [1, 0, 0, 0, 0, 0] : Contrast register set as 32

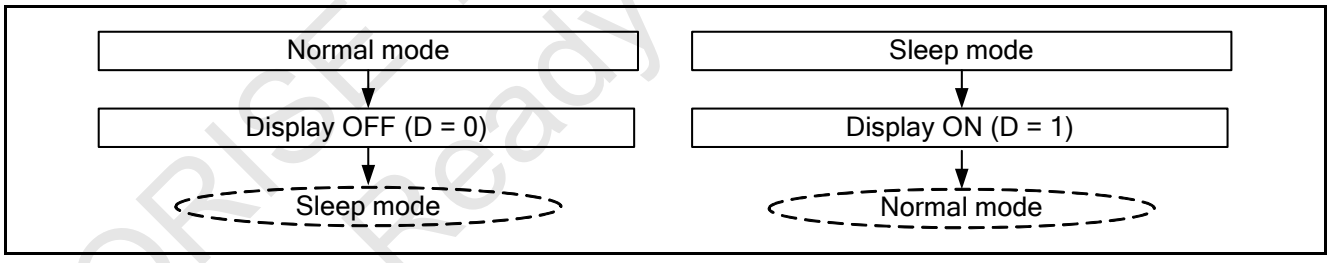
5.13. Power Save

This is compound instruction. The 1st instruction is Display OFF (D=0).

The Power Save mode starts the following procedure:

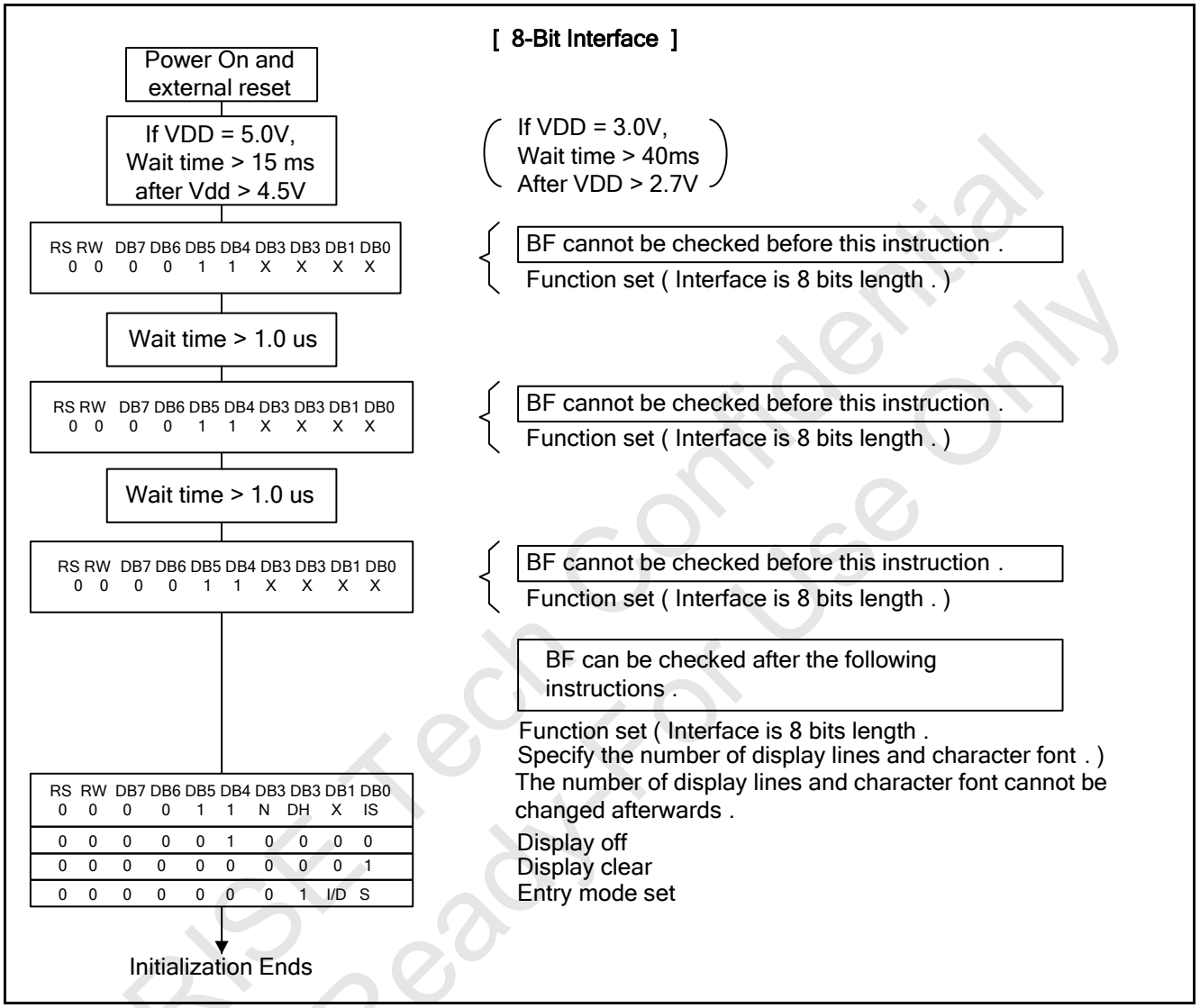
1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.

After exiting Power Save mode, the settings will return to be as they were before.

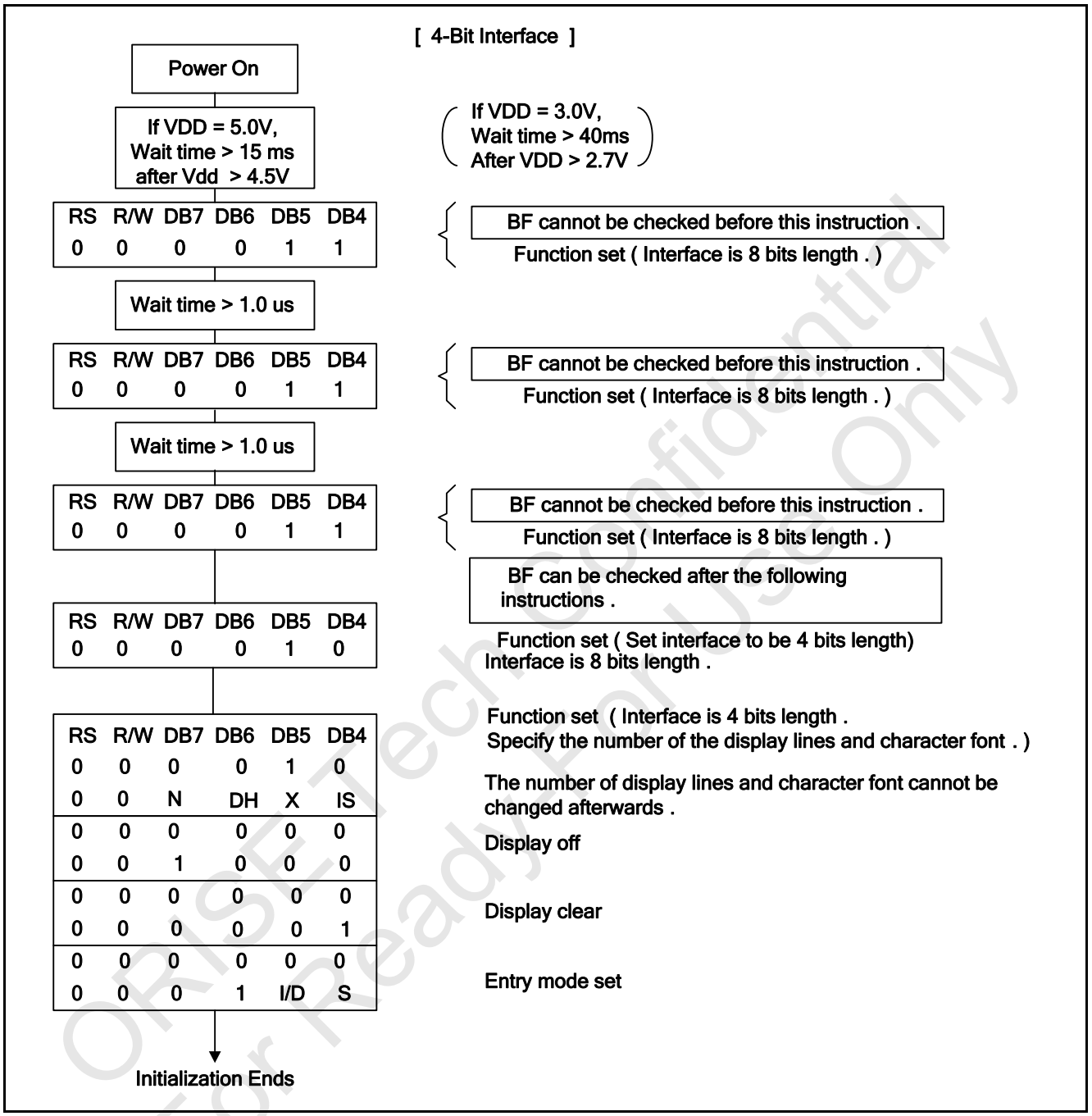


5.14. Reset Function

At power on, it starts the internal auto-reset circuit and executes the initial instructions. There are the initial procedures shown as below:



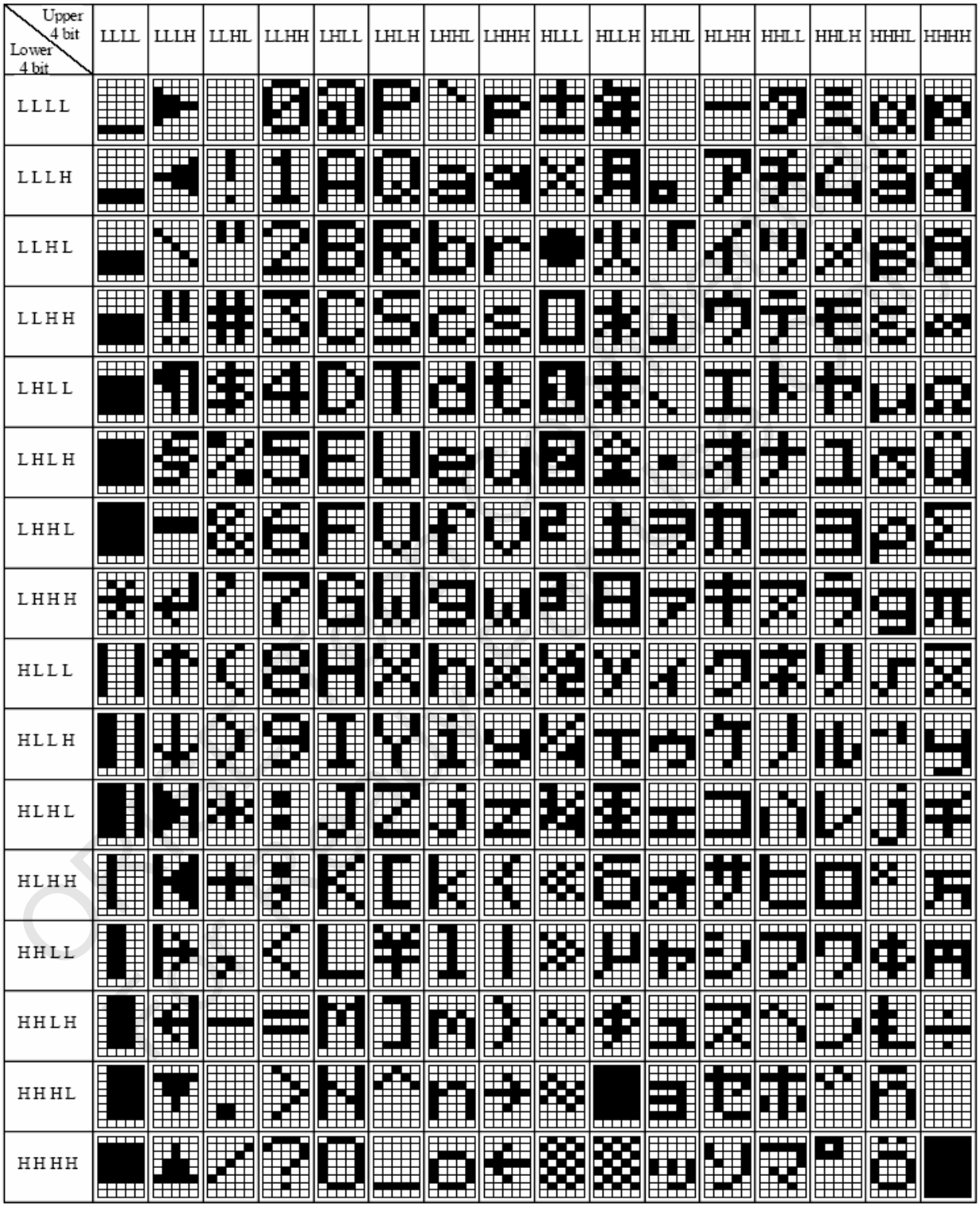
Reset Function (8-bit Interface)



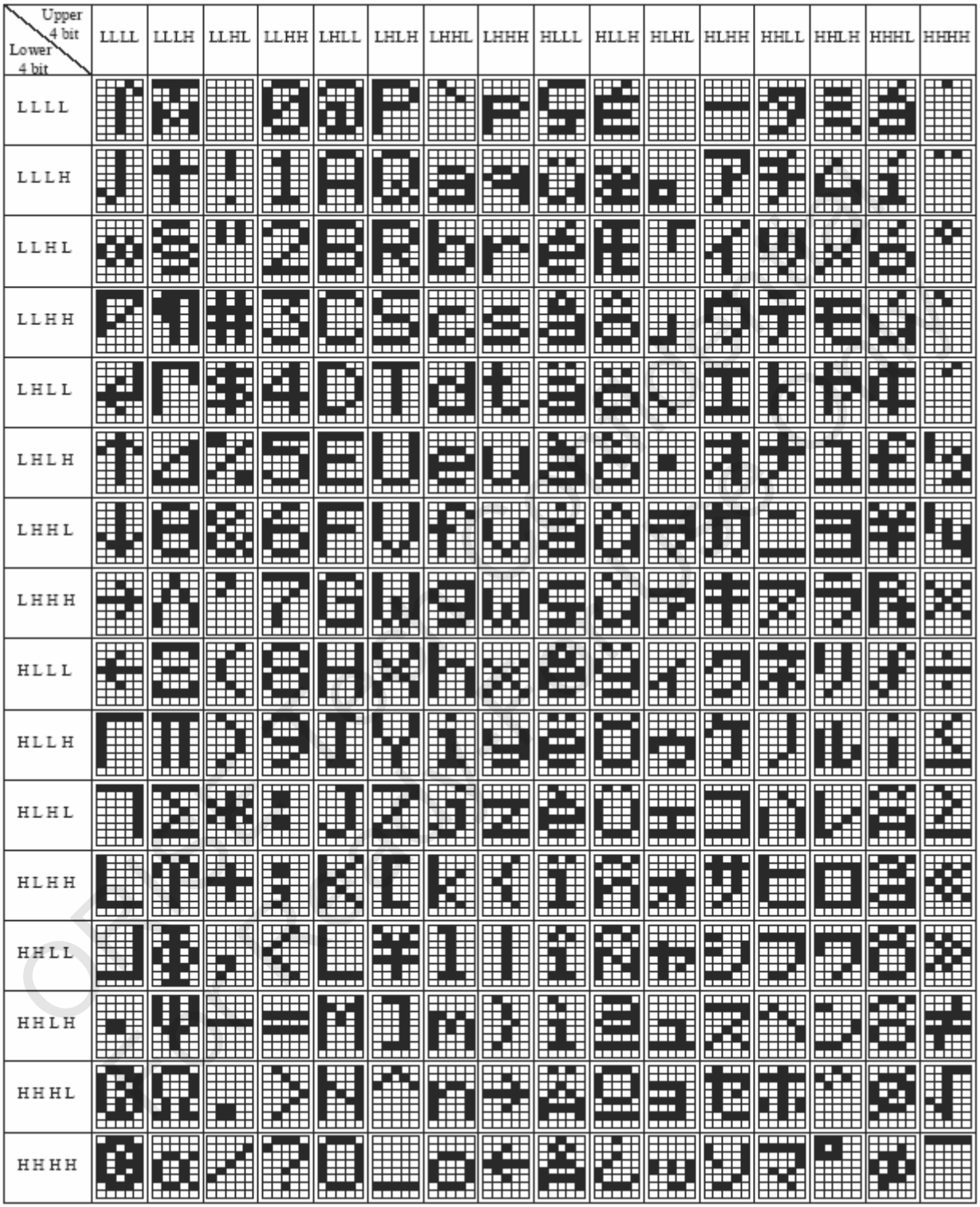
Reset Function (4-bit Interface)

6. CHARACTER GENERATOR ROM

6.1. SPLC792A-001A



6.2. SPLC792A-002A



7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{out}	-0.3V to +7V
Input Voltage Range	V_{IN}	-0.3V to VDD + 0.3V
Operating Temperature	T_A	-30℃ to +80℃
Storage Temperature	T_{STO}	-55℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

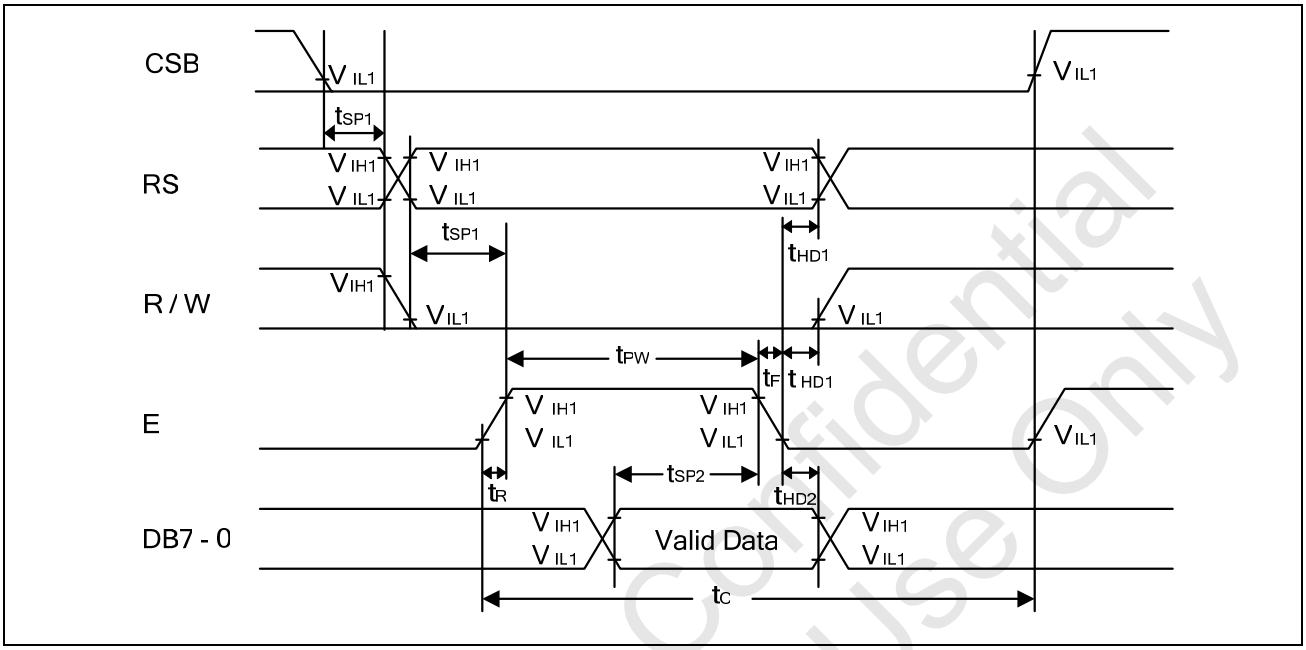
7.2. DC Characteristics (VDD = 2.4V to 5.5V, T_A = -30℃ to +80℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	IDD	-	0.2	0.4	mA	VDD=3V
Sleeping Current	$I_{DD(SLEEP)}$	-	-	5.0	μA	
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	
Input Low Voltage	V_{IL1}	-0.3	-	0.3VDD	V	
Input High Current	I_{IH}	-1.0	-	1.0	μA	
Input Low Current	I_{IL}	-1.0	-	1.0	μA	
Output High Voltage (TTL)	V_{OH1}	VDD – 0.4V	-	-	V	I_{OH} = - 1mA Pins: DB7 - DB0
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4V	V	I_{OL} = 1mA Pins: DB7 - 0
Driver ON Resistance (COM)	R_{COM}	-	-	5.0	KΩ	I_O = ±50.0μA, V_{LCD} = 4.0V Pins: COM[16 : 1] , COM[I2 : I1]
Driver ON Resistance (SEG)	R_{SEG}	-	-	10.0	KΩ	I_O = ±50.0μA, V_{LCD} = 4.0V Pins: SEG80 - 1
Frame frequency (Internal OSC)	f_{FR}	70	75	80	HZ	VDD = 3.0V, T_A = 25℃,
LCD Voltage	V_{LCD}	3.0	-	6.0	V	

Note: Internal oscillator, VDD = 3.0V, all outputs are no loads.

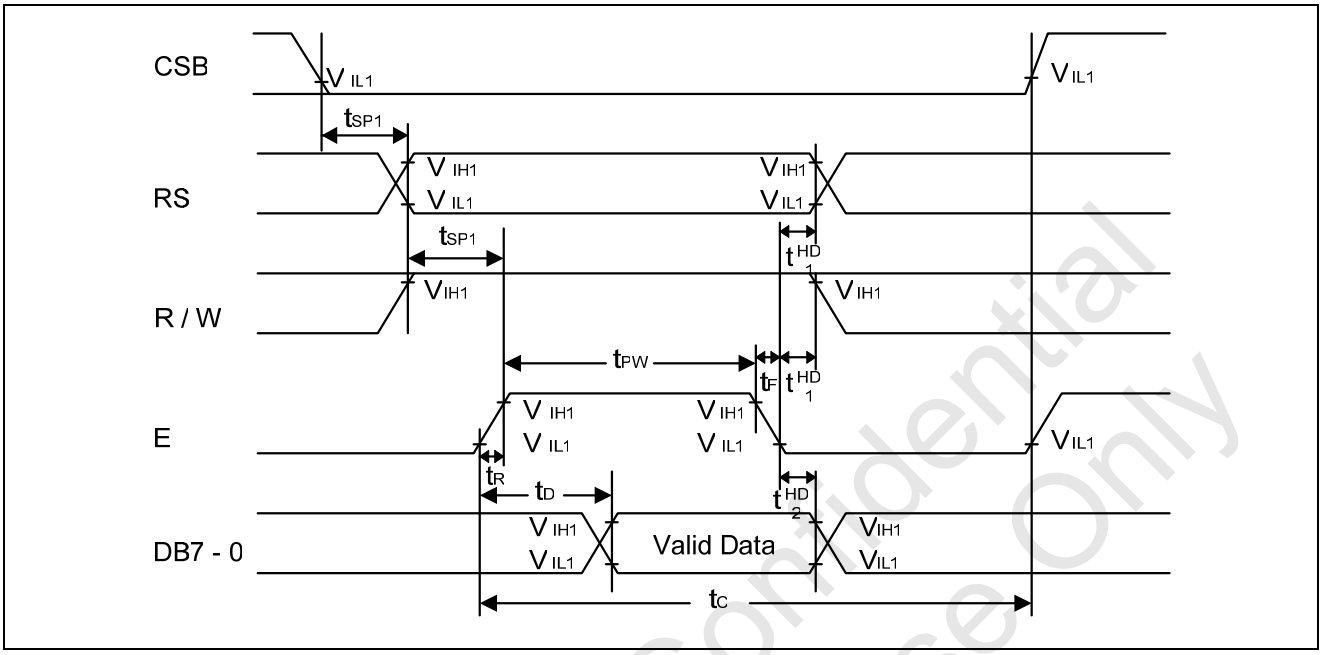
7.3. AC Characteristics (VDD = 2.4V to 5.5V, TA = -30℃ to +80℃)

7.3.1. Write mode (Writing data from MPU to SPLC792A)



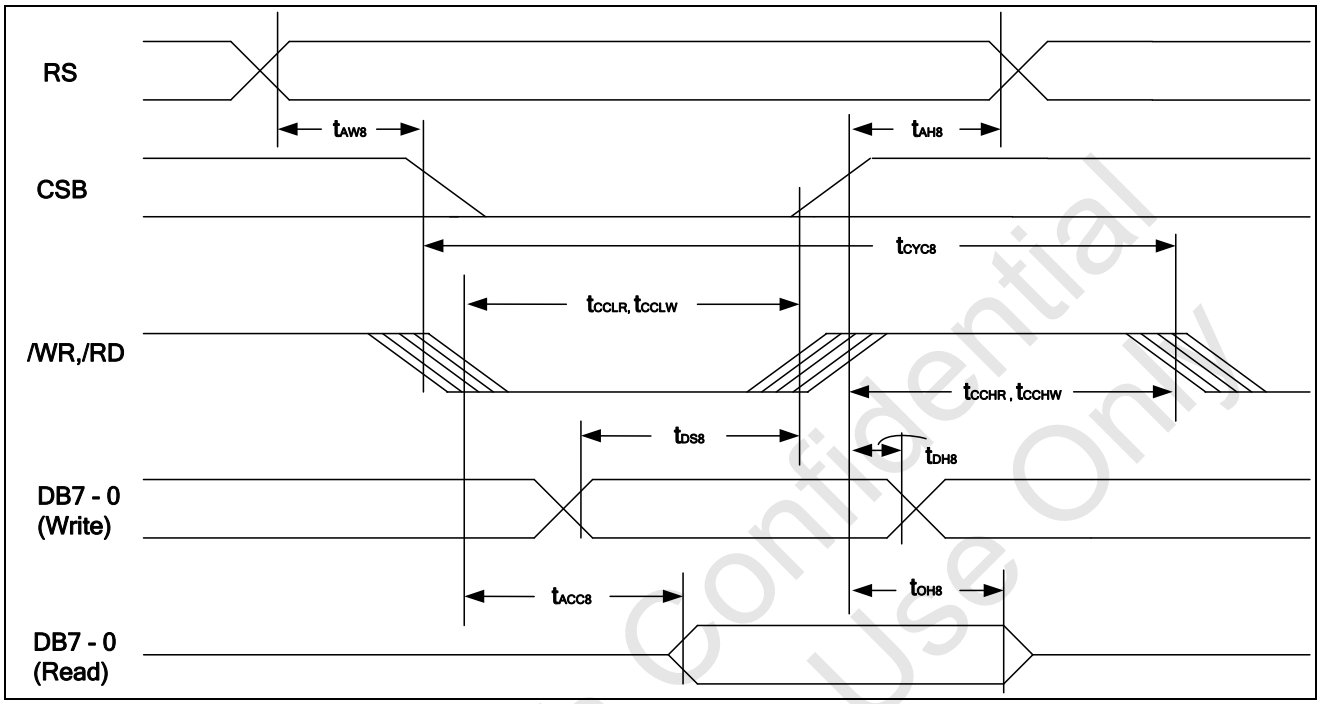
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	200	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	40	-	-	ns	Pins: DB7 - 0
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB7 - 0

7.3.2. Read mode (Reading data from SPLC792A to MPU)



Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_W	200	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	200	ns	Pins: DB7 – 0, CL = 50pF
Data hold time	t_{HD2}	10	-	-	ns	Pin DB7 - 0

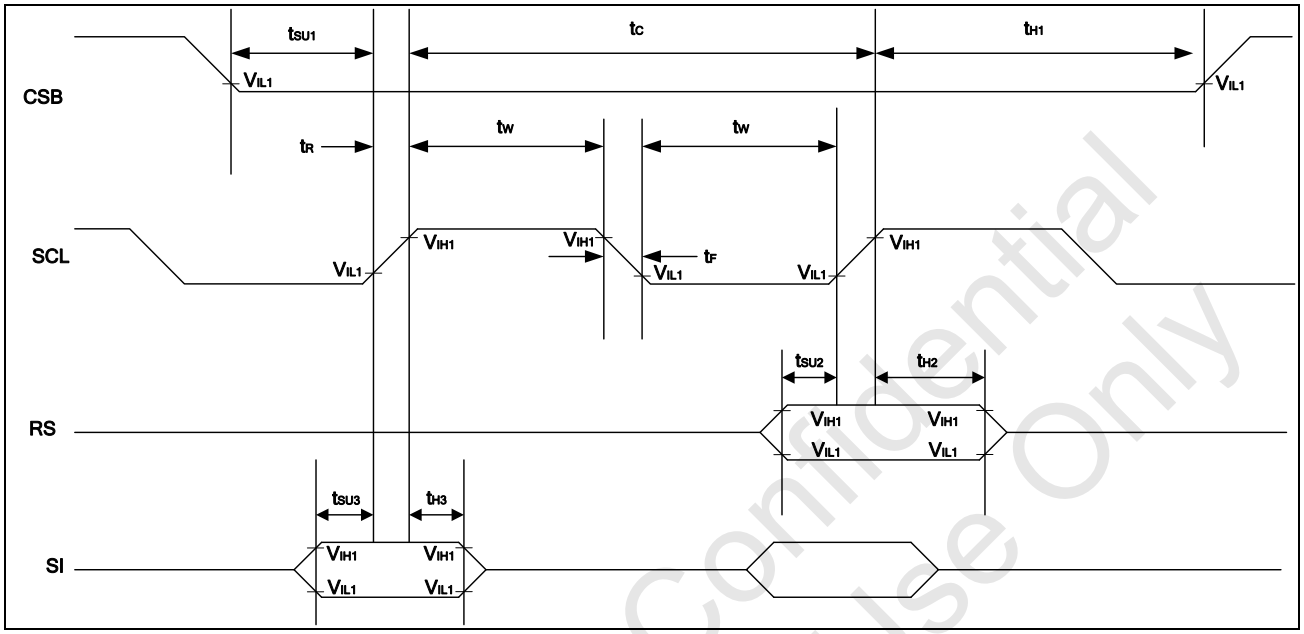
7.3.3. System bus read/write characteristics (For the 8080 Series MPU)



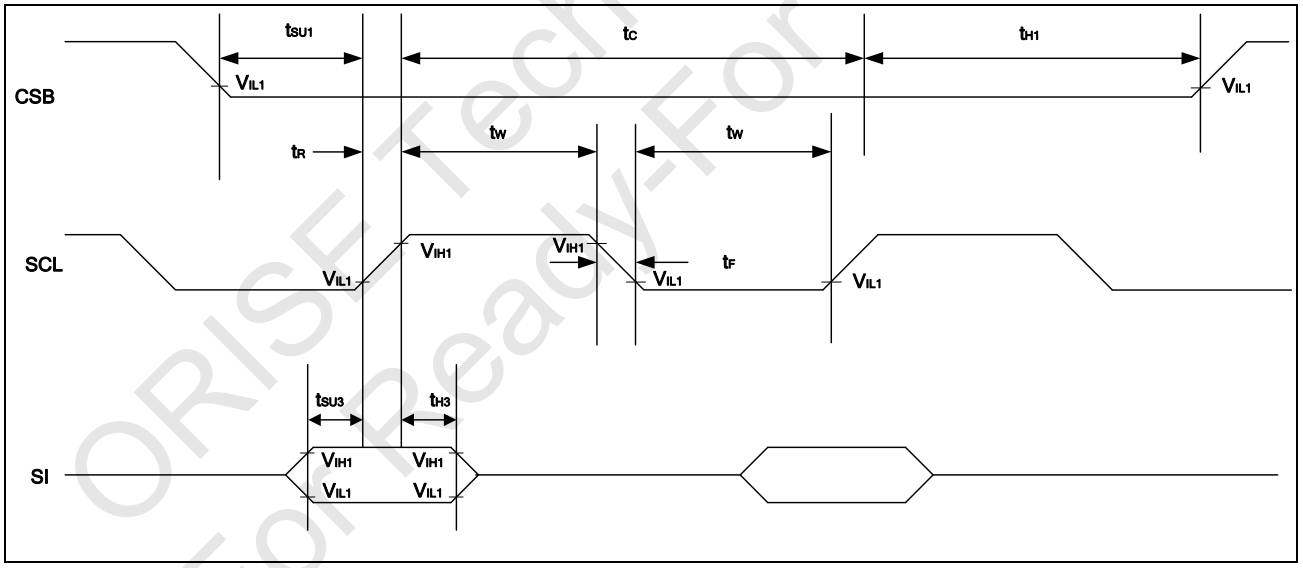
Signal	Parameter	Symbol	Conditions	Min.	Max.	Unit
RS	Address hold time	t_{AH8}		10	-	ns
	Address setup time	t_{AW8}		100	-	ns
	System cycle time	t_{CYC8}		400	-	ns
/WR	Control L pulse width (/WR)	t_{CCLW}		100	-	ns
/RD	Control L pulse width (/RD)	t_{CCLR}		100	-	ns
/WR	Control H pulse width (/WR)	t_{CCHW}		100	-	ns
/RD	Control H pulse width (/RD)	t_{CCHR}		100	-	ns
DB7 - 0	Data setup time	t_{DS8}		40	-	ns
	Address hold time	t_{DH8}		15	-	ns
	E access time	t_{ACC8}	C_L = 100pF	-	140	ns
	Output disable time	t_{OH8}		10	100	ns

7.3.4. Clock synchronized serial mode (VDD = 2.4V to 5.5V, TA = -30℃ to +80℃)

4-Wire SPI Interface Mode timing diagram

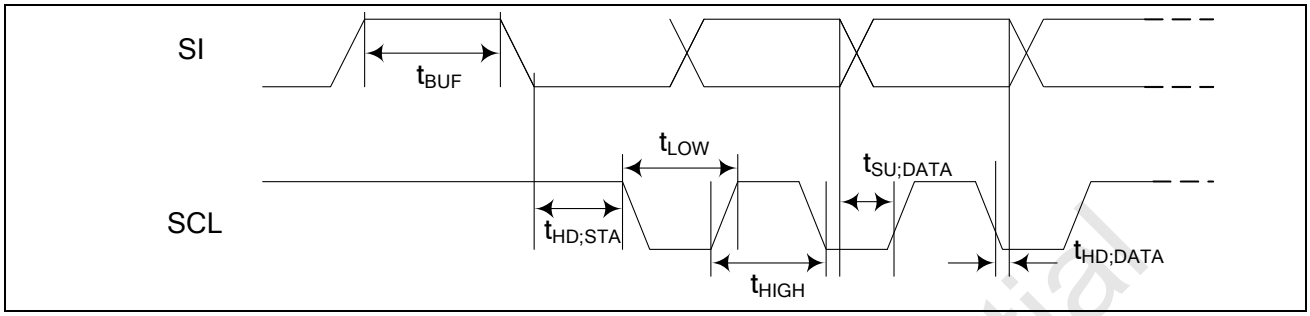


3-Wire SPI Interface Mode timing diagram



Characteristic	Symbol	Min.	Typ.	Max.	Unit
SCL Clock Cycle Time	t_C	500	-	-	ns
Pulse Rise / Fall Time	t_R, t_F	-	-	20	
SCL Clock Width (High, Low)	t_W	200	-	-	
CSB Setup Time	t_{SU1}	100	-	-	
CSB Hold Time	t_{H1}	300	-	-	
RS Data Setup Time	t_{SU2}	40	-	-	
RS Data Hold Time	t_{H2}	40	-	-	
SI Data Setup Time	t_{SU3}	40	-	-	
SI Data Hold Time	t_{H3}	40	-	-	

7.3.5. Serial interface (I²C-bus)



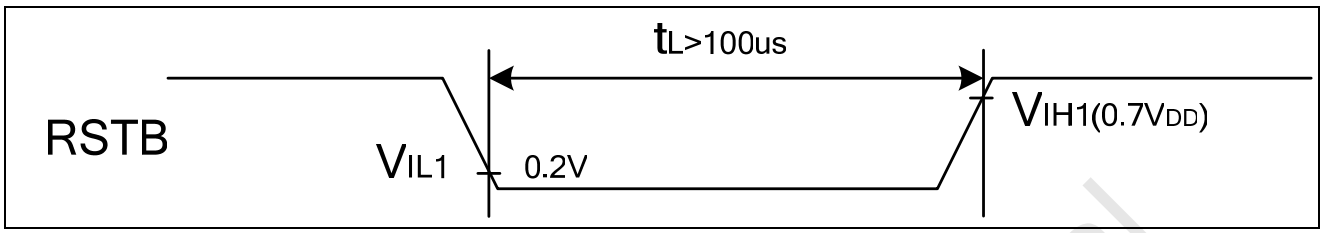
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCLK}		DC	-	400	KHz
SCL clock LOW period	t_{LOW}		1.3	-	-	µs
SCL clock HIGH period	t_{HIGH}		0.6	-	-	µs
data set-up time	$t_{SU;DATA}$		100	-	-	ns
data hold time	$t_{HD;DATA}$		0	-	0.9	µs
SCL and SI rise time	t_R	(2)	$20+0.1C_b$	-	300	ns
SCL and SI fall time	t_F	(2)	$20+0.1C_b$	-	300	ns
SI fall time for read out	t_F	VDD1 = < 3.3V	$20+0.1C_b$	-	1000	ns
Capacitive load represented by each bus line	C_b		-	-	400	pF
Setup time for a repeated START condition	$t_{SU;STA}$		0.6	-	-	µs
START condition hold time	$t_{HD;STA}$		0.6	-	-	µs
Setup time for STOP condition	$t_{SU;STO}$		0.6	-	-	µs
Tolerable spike width on bus	t_{SW}	(1)	-	-	50	ns
BUS free time between a STOP and START condition	t_{BUF}		1.3	-	-	µs

Note1: The device inputs SI and SCL are filtered and will reject spikes on the bus lines of width $<t_{SW(max)}$.

Note2: The rise and fall times specified here refer to the driver device (i.e. not SPLC792A) and are part of the general fast I²C-bus specification. C_b = capacitive load per bus line.

Note3: All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of VSS to VDD.

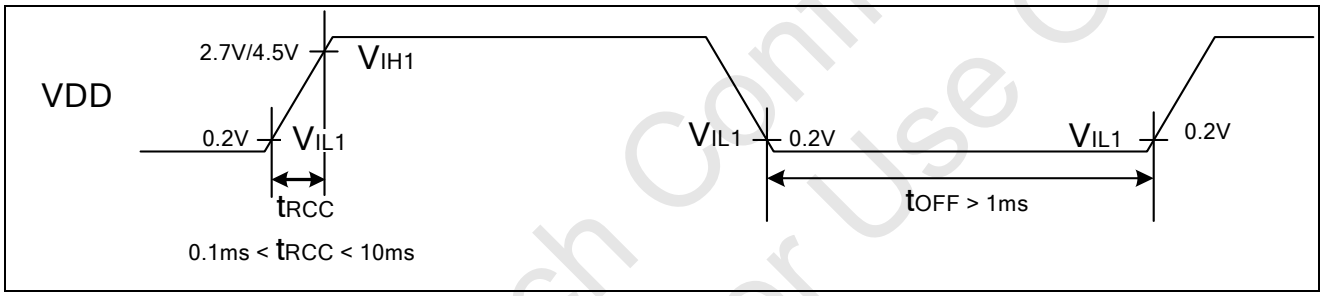
7.4. Hardware Reset Timing (VDD = 2.4V to 5.5V, TA = -30℃ to +80℃)



Characteristic	Symbol	Min.	Typ.	Max.	Unit
Reset Low Period	t_L	100			us

Note : For hardware reset can be operate normally, the reset pulse width must be large than 100us.

7.5. Internal Power On Reset Timing (VDD = 2.4V to 5.5V, TA = -30℃ to +80℃)

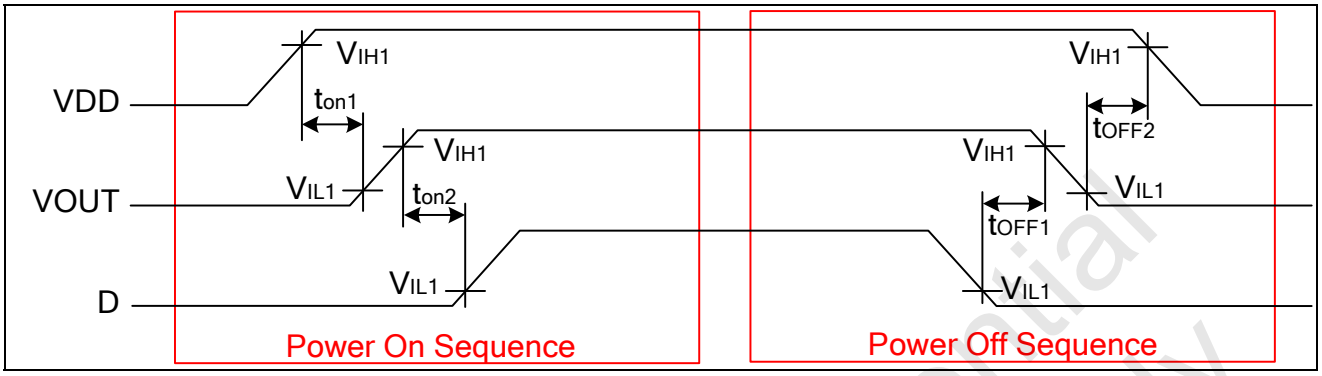


Characteristic	Symbol	Min.	Typ.	Max.	Unit
Power ON Rising Time	t_{RCC}	0.1	-	10	ms
Power OFF Period	t_{OFF}	1.0			ms

Note :

1. The Internal Power ON Reset Function only for EXT = 0.
2. Specified at 4.5V for 5V operation, and 2.7V for 3V operation.
3. If the t_{RCC} and t_{OFF} can not meet in specification, the internal power on reset circuit will not operate normally.
4. If the internal power on reset circuit are not operate normally, all the initial state in Register will be not correct. The Register contents can also be set by software initial and hardware reset.

7.5.1. Used the External Power for LCD Power Supply Mode



Characteristic	Symbol	Min.	Typ.	Max.	Unit
VDD Power stable time	t_{on1}	0	-		ms
VLCD stable time	t_{On2}	0			ms
LCD discharge time	t_{OFF1}	5			ms
VDD Power Off time	t_{OFF2}	0			ms

Note :

1. The Voltage Follower V1 ~ V4 will be automatic turn on for LCD Driver when used as EXT=0
2. The external power VOUT supply must be waiting for VDD power ready (t_{on1} > 0ms)
3. The LCD display turn on must be waiting for VOUT power ready (t_{on2} > 0ms)

8. APPLICATION CIRCUITS

8.1. Interface to MPU

8.1.1. Interface to 8-bit MPU (6805)

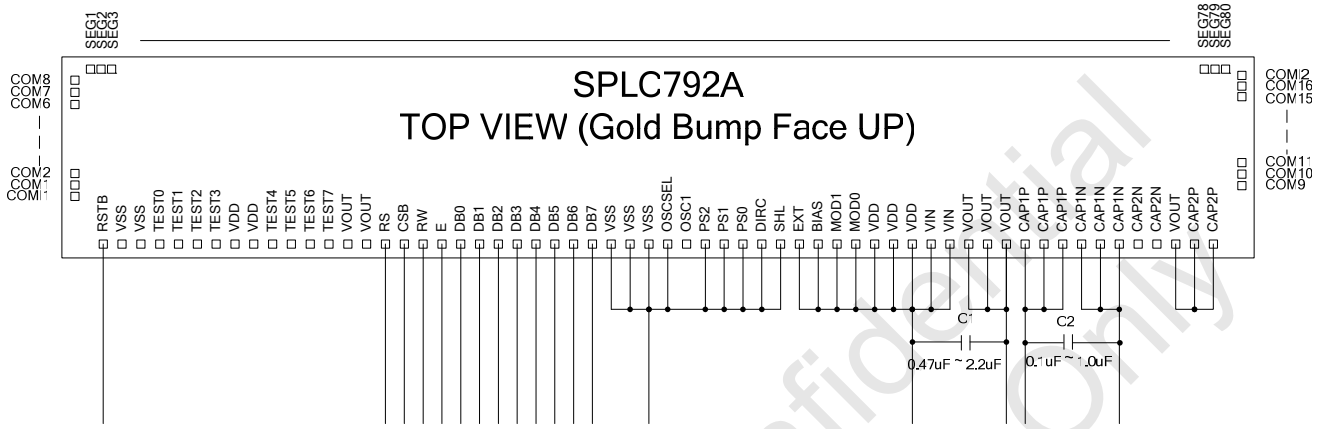


Figure 8-1 Interface to 8-bit MPU (6805)

8.1.2. Interface to 4-bit MPU (6805)

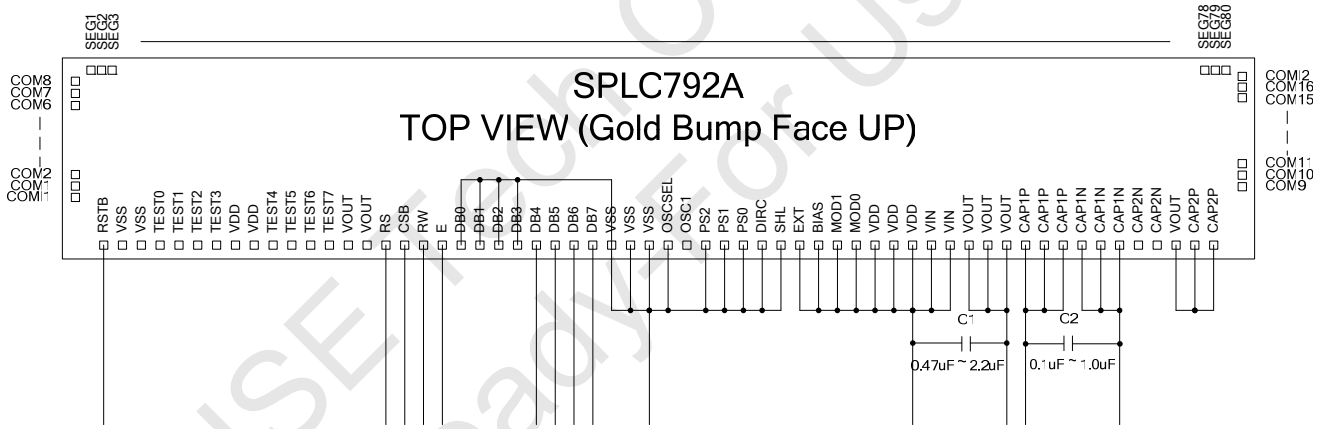


Figure 8-2: Interface to 4-bit MPU (6805)

8.1.3. Interface to 8-bit MPU (8080)

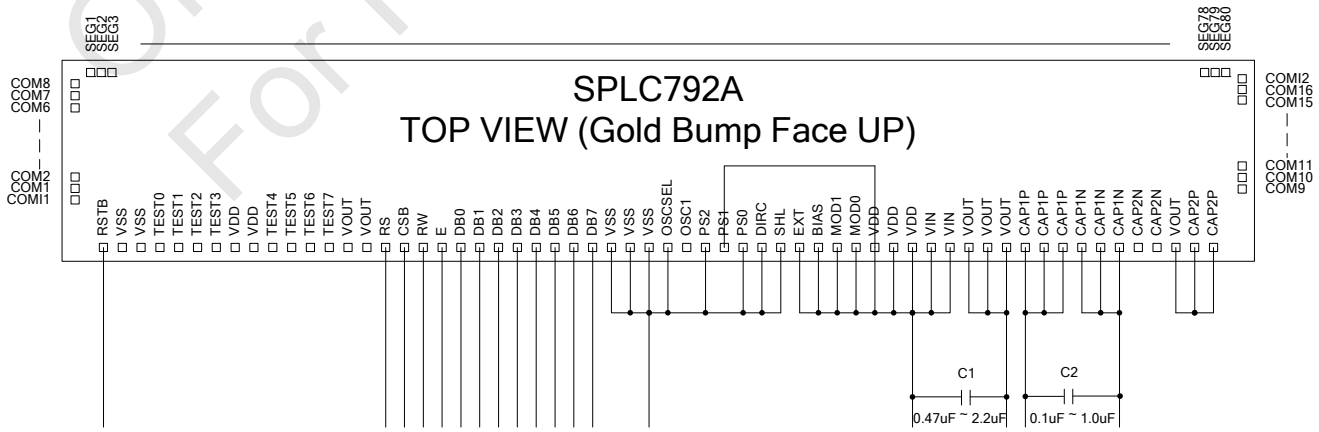


Figure 8-3: Interface to 8-bit MPU (8080)

8.1.4. Interface to 4-bit MPU (8080)

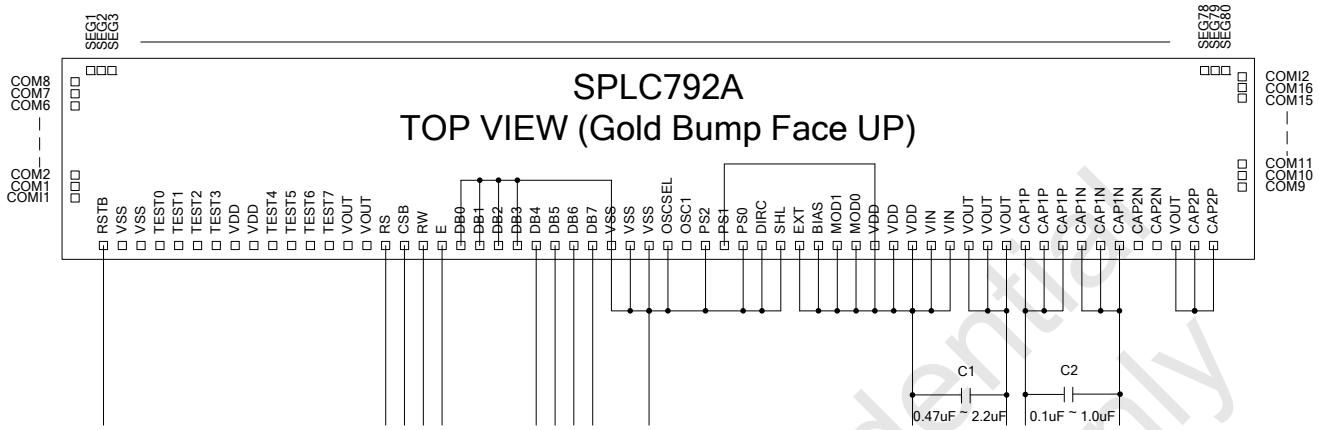


Figure 8-4: Interface to 4-bit MPU (8080)

8.1.5. Interface to 4-wire SPI

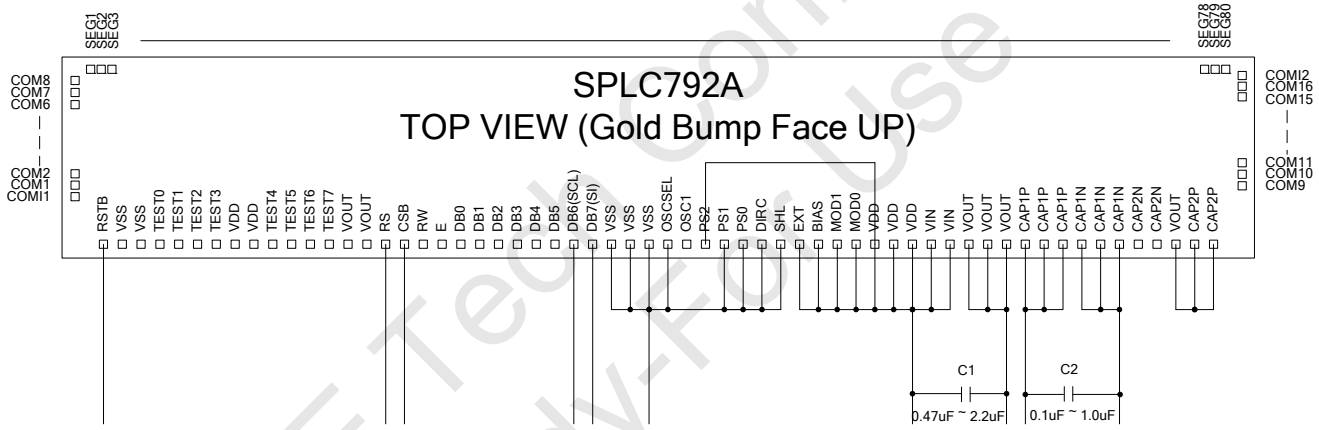


Figure 8-5: Interface to 4-wire SPI

8.1.6. Interface to 3-wire SPI

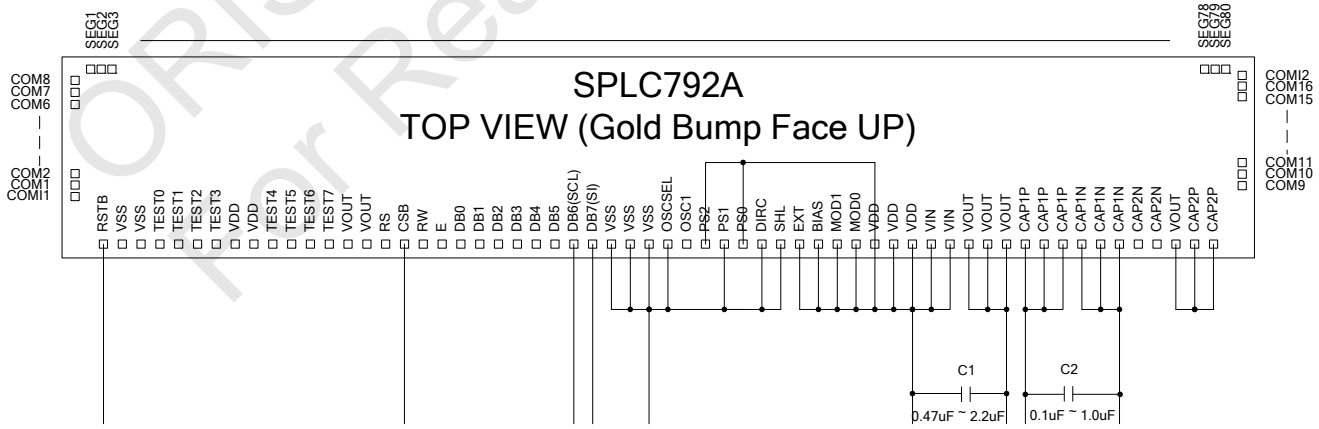


Figure 8-6: Interface to 3-wire SPI

8.1.7. Interface to I²C Interface

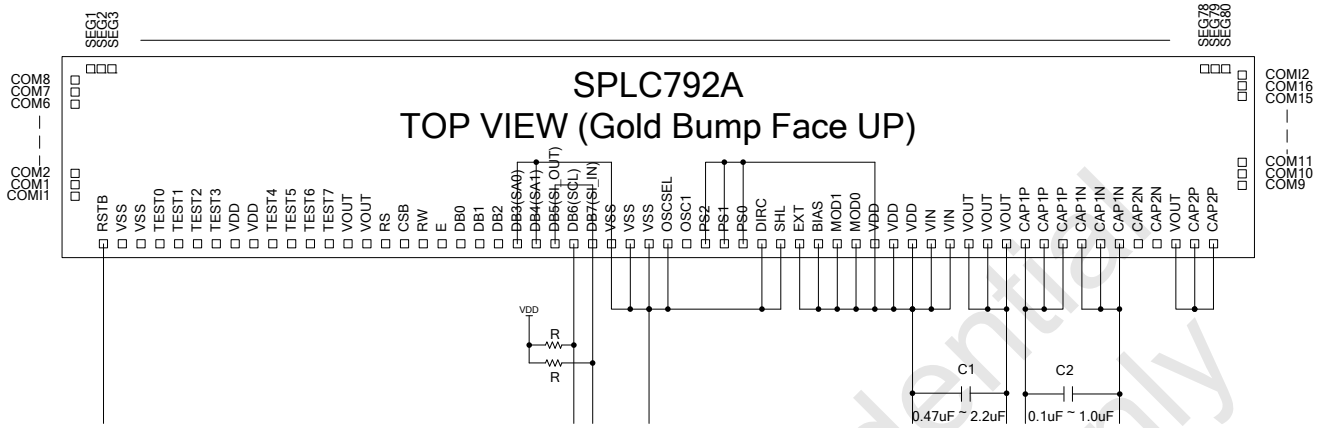


Figure 8-7: Interface to I²C Interface

8.2. Application for LCD

8.2.1. Chip Top & IC at panel lower side (DIRC = "0", SHL = "0")

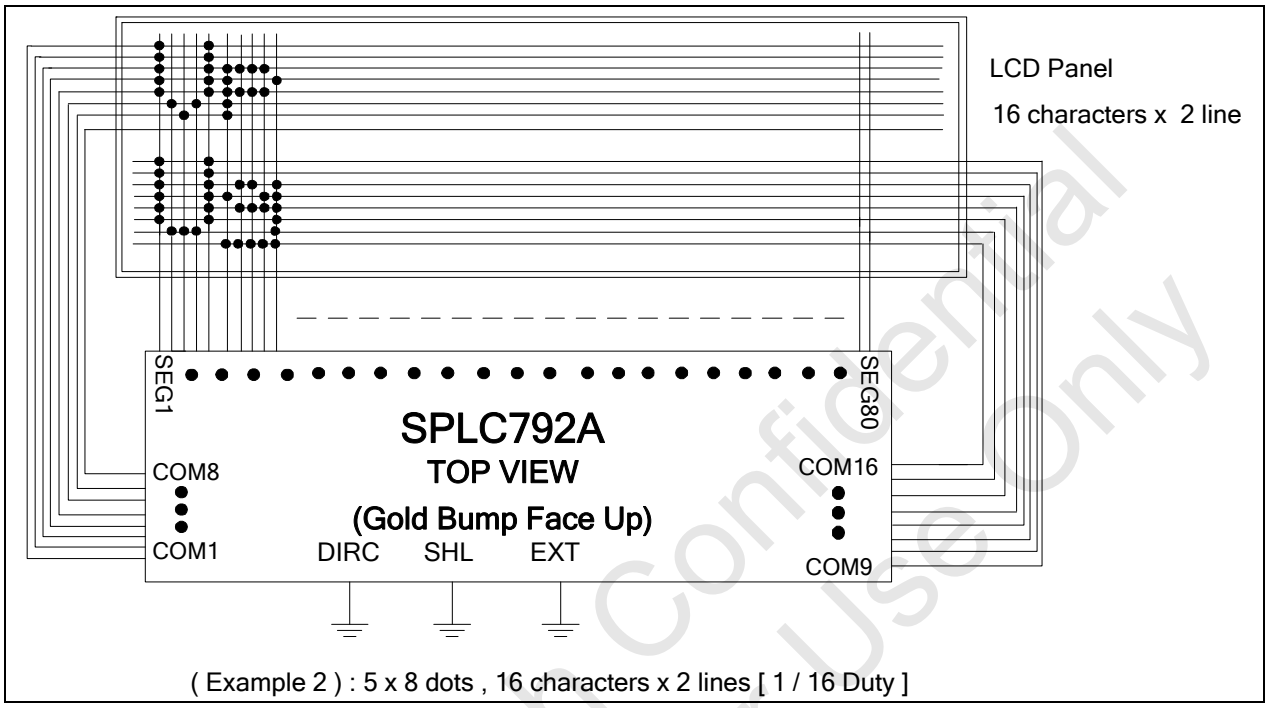


Figure 8-8: Chip Top & IC at panel lower side (Example 1)

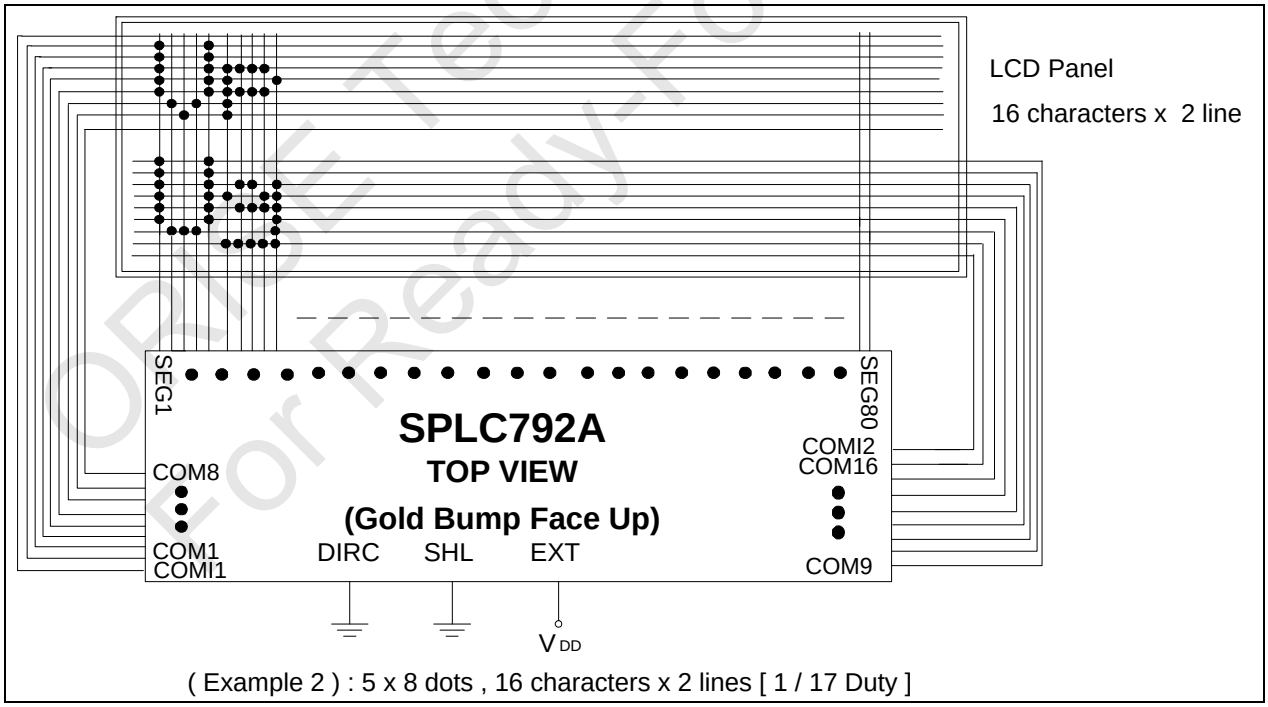


Figure8-9: Chip Top & IC at panel lower side (Example 2)

8.2.2. Chip Top & IC at panel upper side (DIRC = "1", SHL = "1")

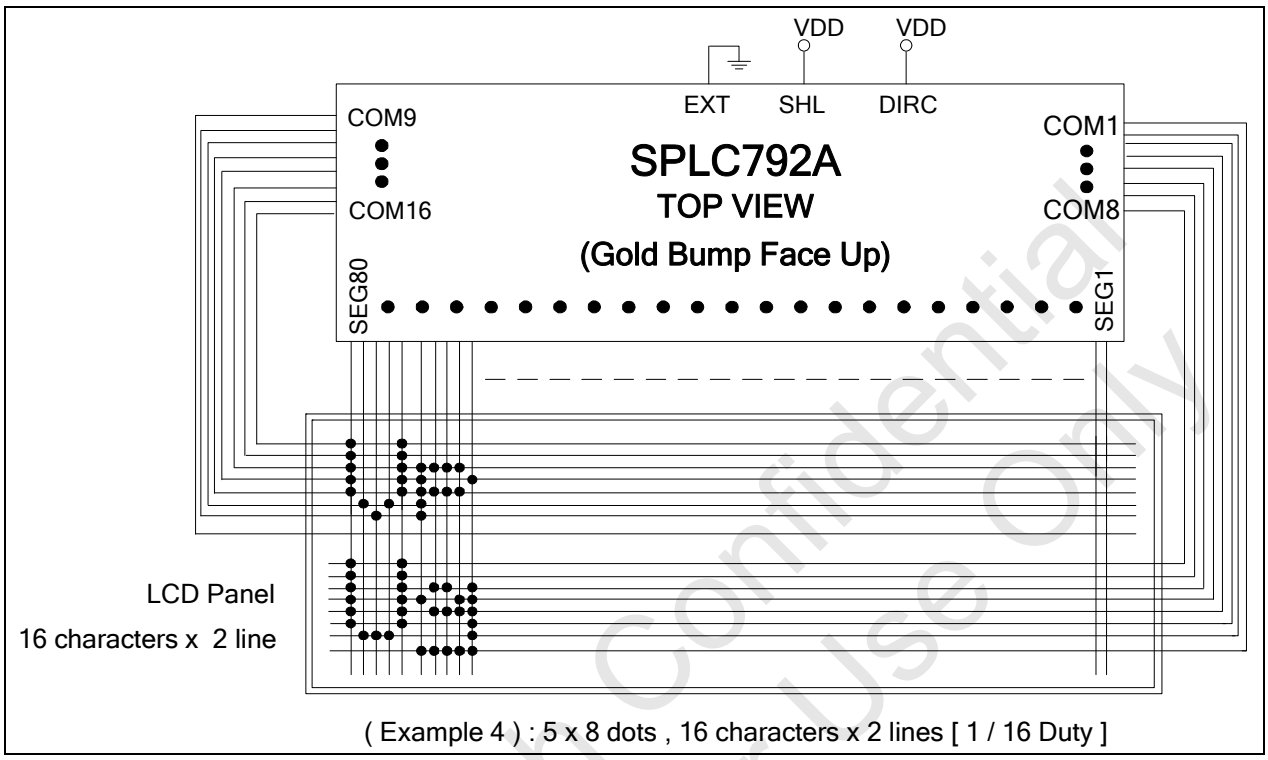


Figure 8-10: Chip Top & IC at panel upper side (Example 3)

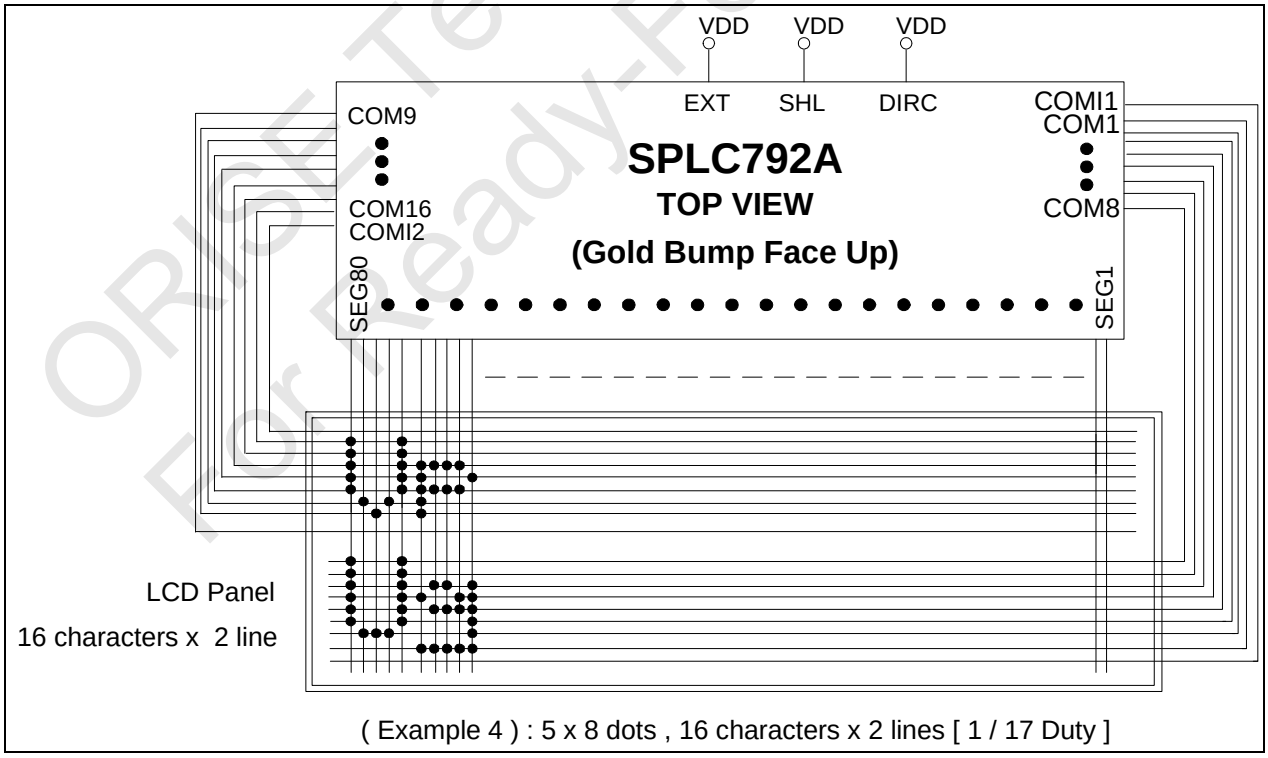


Figure 8-11: Chip Top & IC at panel upper side (Example 4)

8.2.3. Chip Bottom & IC at panel lower side (DIRC = "0", SHL = "1")

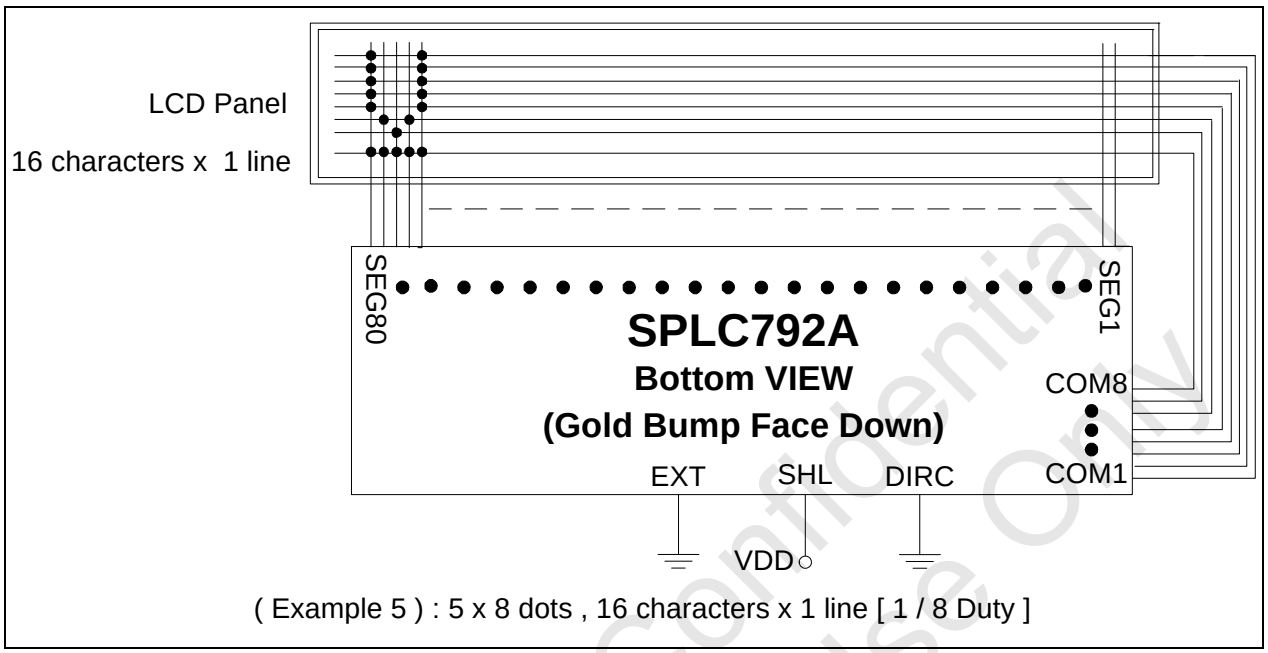


Figure 8-12: Chip Bottom & IC at panel lower side (Example 5)

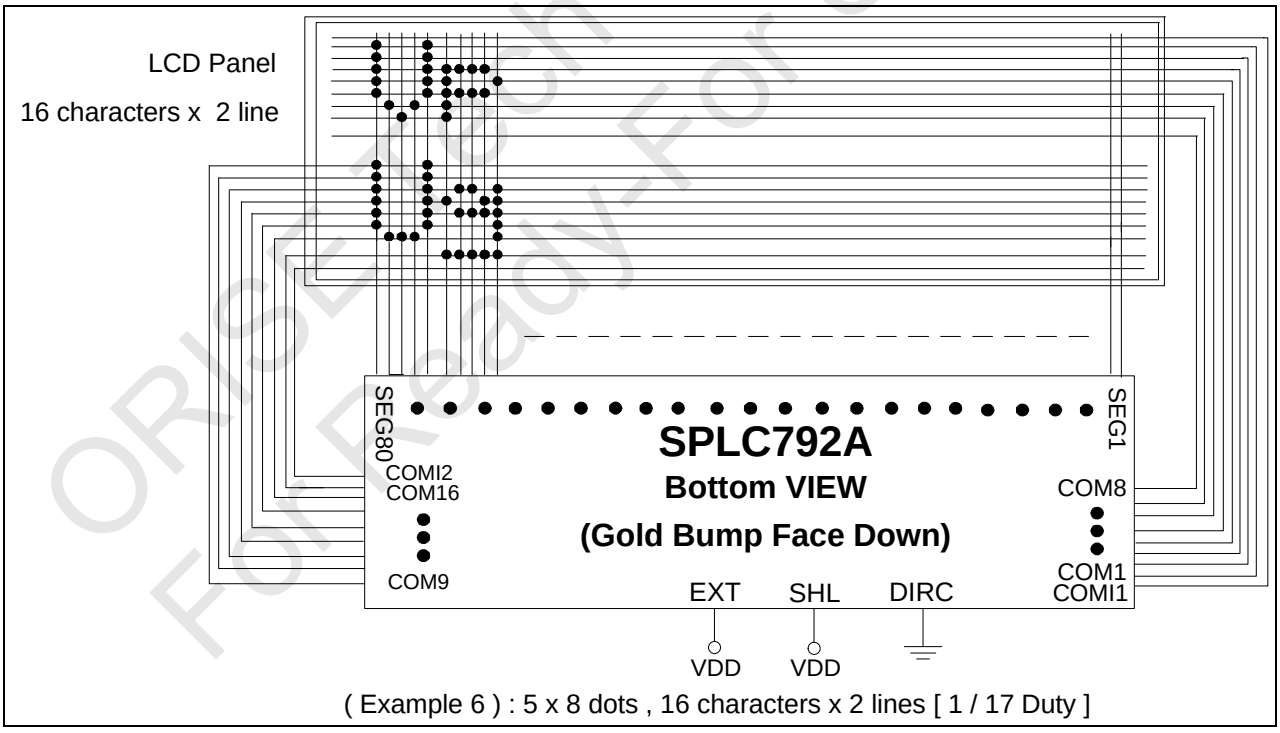


Figure 8-13: Chip Bottom & IC at panel lower side (Example 6)

8.2.4. Chip Bottom & IC at panel upper side (DIRC = "1", SHL = "0")

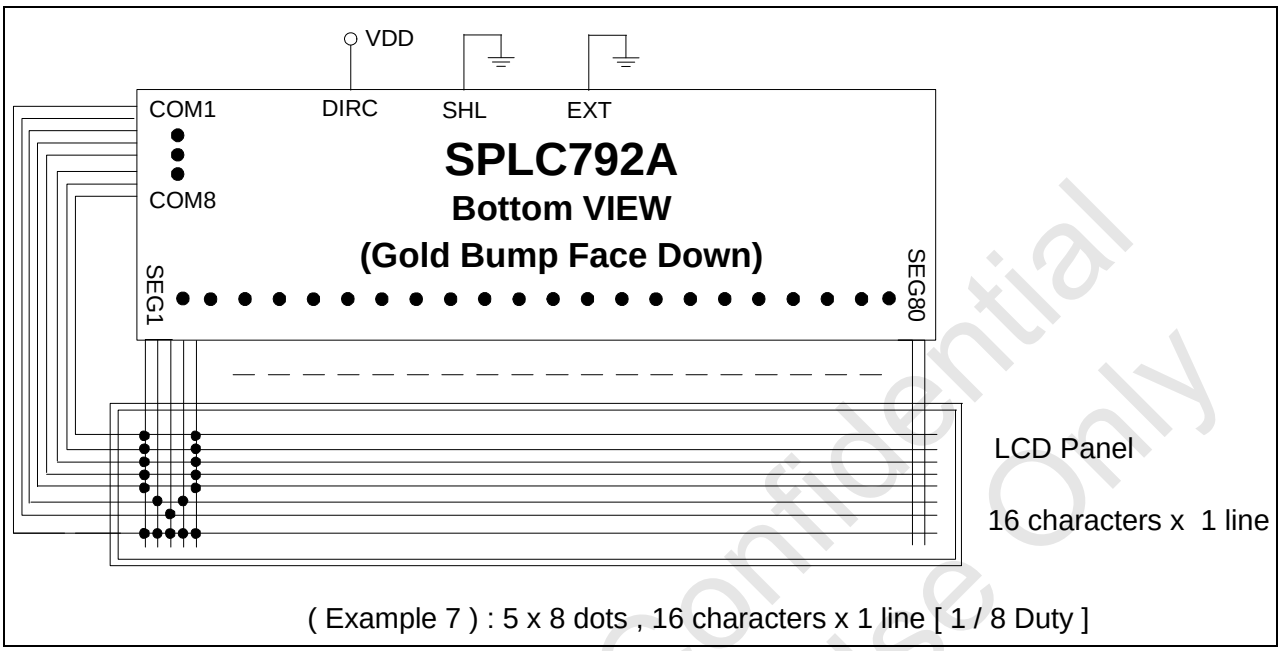


Figure 8-14: Chip Bottom & IC at panel upper side (Example 7)

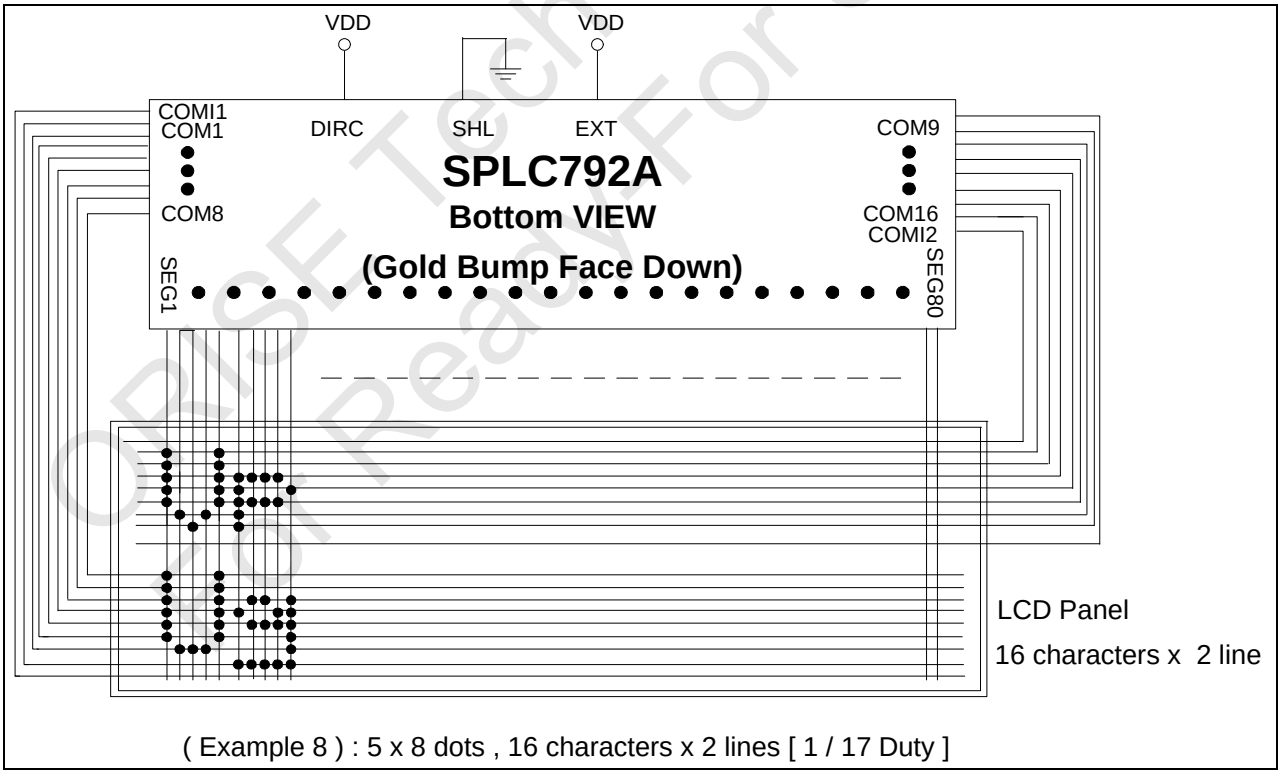
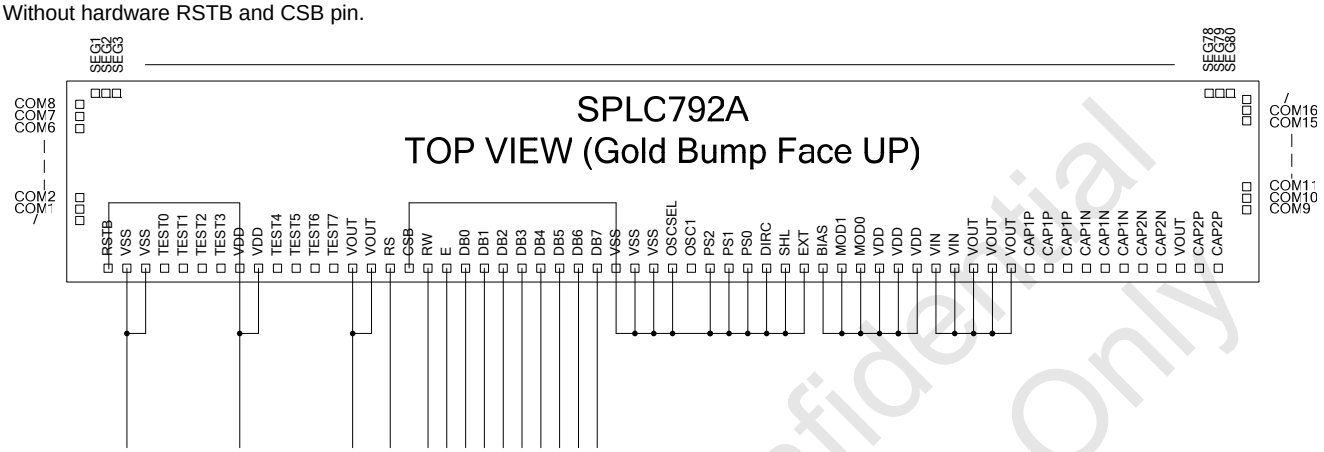


Figure 8-15: Chip Bottom & IC at panel upper side (Example 8)

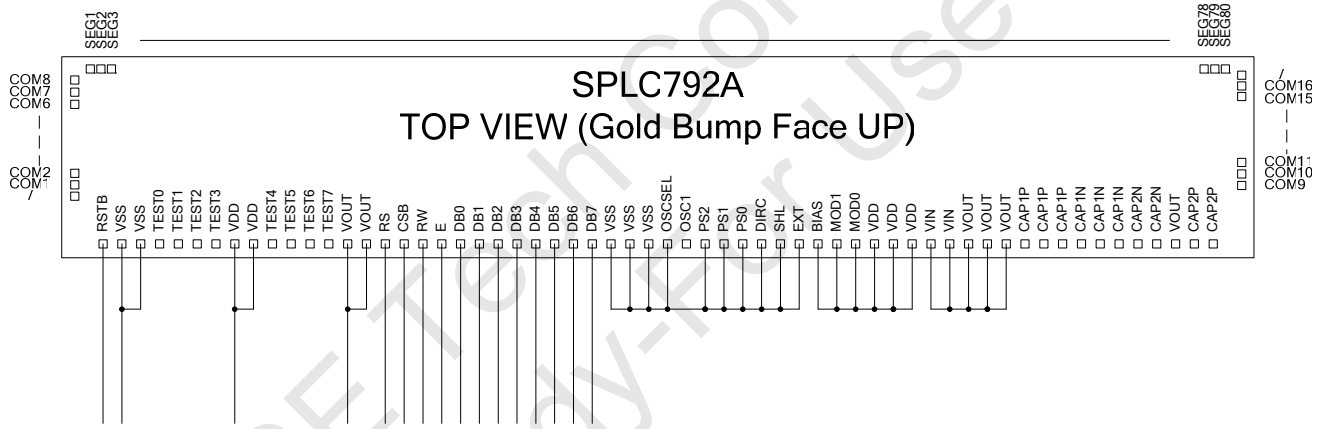
8.3. The application circuit

8.3.1. The application circuit of SPLC792A to replace SPLC782A 8-bit / 4-bit mode

Without hardware RSTB and CSB pin.



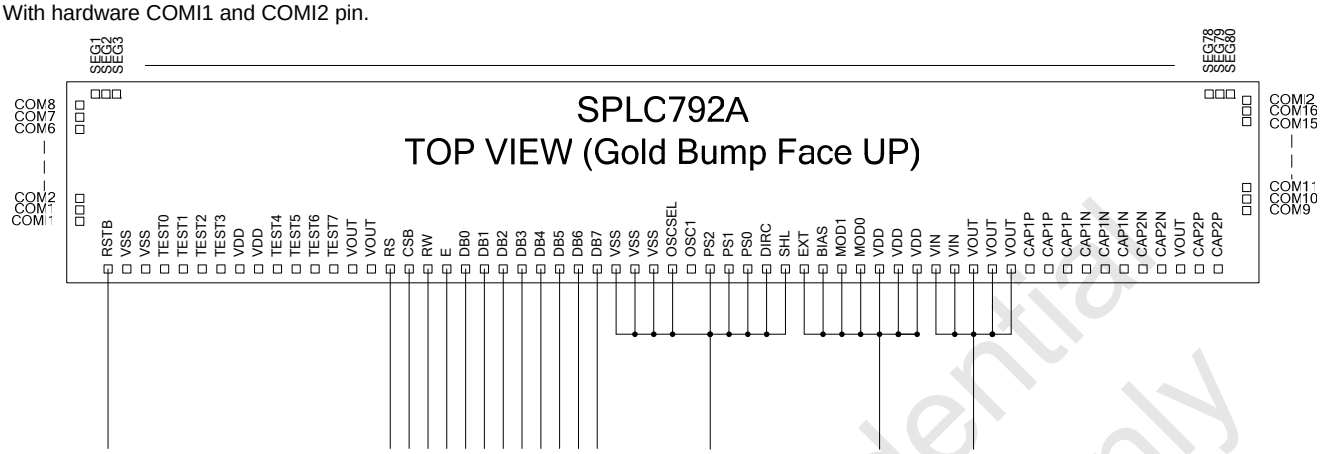
With hardware RSTB and CSB pin.



Interface			6800 series 8-bit / 4bit parallel interface mode (**Reference 5.1.1 SELECTING THE INTERFACE TYPE**) 4-bit interface mode DB[3:0] must be connect to VDD or VSS		
Resolution			**16-Character x 2-Line (16-COM x 80-SEG)**		
Booster default value			External VOUT (VIN must be connecting to VOUT.)		
Bias ratio default value			1/5		
6800 interface			**Reference 5.1.2. The parallel interface**		
Interface Setting			Configuration Setting		
PS2	VSS	6800 series parallel Interface Mode	DIRC	VSS	COM1 → COM2 → . . . → COM16 → COMI1(COMI2)
PS1	VSS		SHL	VSS	SEG1 → SEG2 → . . . → SEG80
PS0	VSS		EXT	VSS	Disable ICON function and Disable Booster circuit
OSCSEL	VSS	Internal oscillator clock mode	BIAS	VDD	1/5 bias
MOD0	VDD	$00 ~ $0F as CGRAM	OSC1	OPEN	
MOD1	VDD		TEST[0:7]	OPEN	

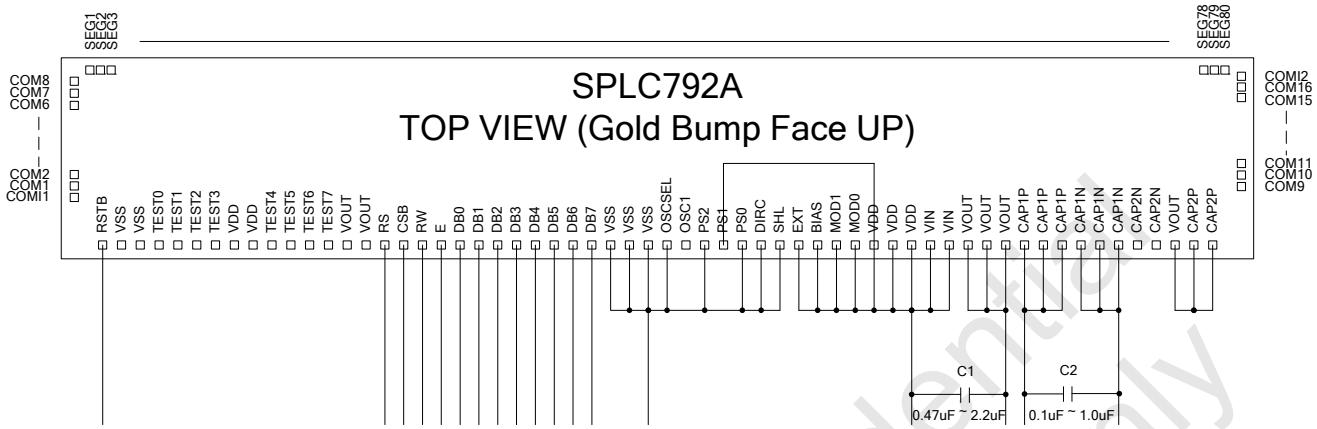
8.3.2. The application circuit of 6800 serial 8-bit / 4-bit interface mode

With hardware COMI1 and COMI2 pin.



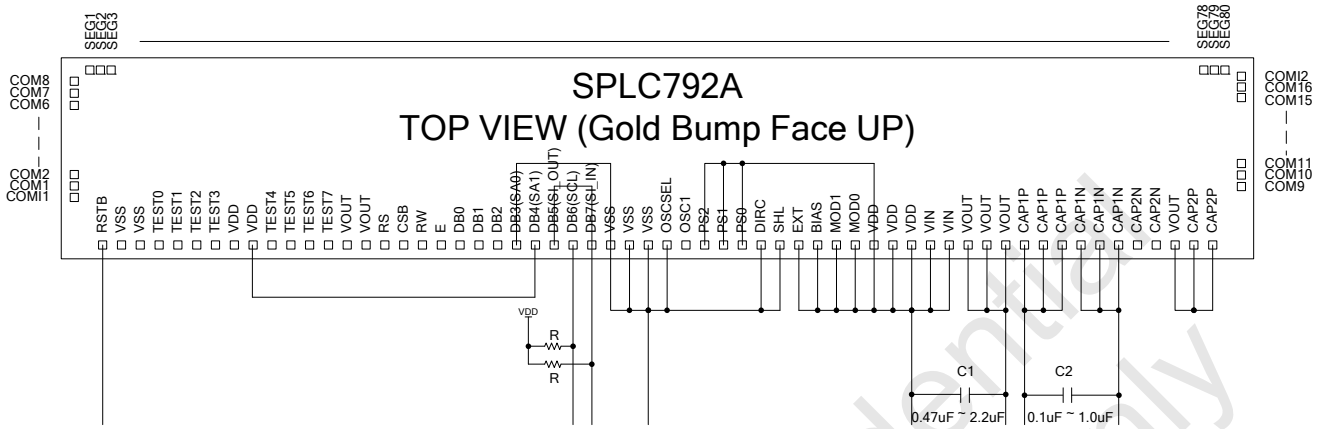
Interface			6800 series 8-bit / 4bit parallel interface mode (**Reference 5.1.1 SELECTING THE INTERFACE TYPE**) 4-bit interface mode DB[3:0] must be connect to VDD or VSS		
Resolution			**16-Character x 2-Line with 80-Icon (18-COM x 80-SEG)**		
Booster default value			External VOUT (VIN must be connecting to VOUT.)		
Bias ratio default value			1/5		
6800 interface			**Reference 5.1.2. The parallel interface**		
Interface Setting			Configuration Setting		
PS2	VSS	6800 series parallel Interface Mode	DIRC	VSS	COM1 → COM2 → . . . → COM16 → COMI1(COMI2)
PS1	VSS		SHL	VSS	SEG1 → SEG2 → . . . → SEG80
PS0	VSS		EXT	VDD	Enable ICON function and Enable Booster circuit
OSCSEL	VSS	Internal oscillator clock mode	BIAS	VDD	1/5 bias
MOD0	VDD	$00 ~ $0F as CGRAM	OSC1	OPEN	
MOD1	VDD		TEST[0:7]	OPEN	

8.3.3. The application circuit of 8080 serial 8-bit / 4-bit interface mode



Interface			8080 series 8-bit / 4bit parallel interface mode (**Reference 5.1.1 SELECTING THE INTERFACE TYPE**) 4-bit interface mode DB[3:0] must be connect to VDD or VSS		
Resolution			**16-Character x 2-Line with 80-Icon (18-COM x 80-SEG)**		
Booster default value			VDD X 2 (VIN must be connecting to VDD.) (VOUT must be connecting to CAP2P.)		
Bias ratio default value			1/5		
8080 interface			**Reference 5.1.2. The parallel interface**		
Interface Setting			Configuration Setting		
PS2	VSS	8080 series parallel Interface Mode	DIRC	VSS	COM1 → COM2 → . . . → COM16 → COMI1(COMI2)
PS1	VDD		SHL	VSS	SEG1 → SEG2 → . . . → SEG80
PS0	VDD/VSS		EXT	VDD	Enable ICON function and Enable Booster circuit
OSCSEL	VSS	Internal oscillator clock mode	BIAS	VDD	1/5 bias
MOD0	VDD	$00 ~ $0F as CGRAM	OSC1	OPEN	
MOD1	VDD		TEST[0:7]	OPEN	

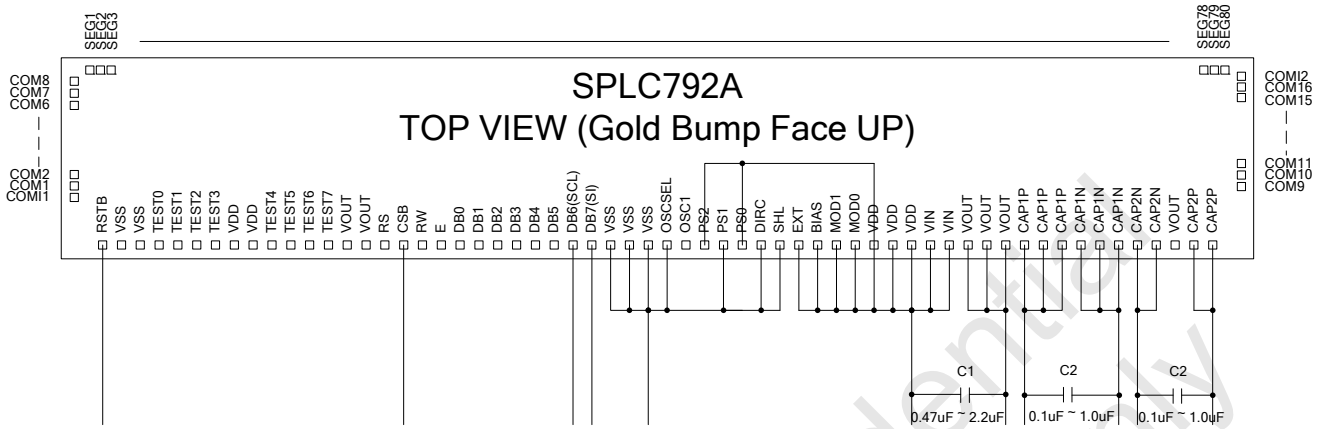
8.3.4. The application circuit of IIC mode



Interface			IIC bus interface mode (**Reference 5.1.1 SELECTING THE INTERFACE TYPE**)		
Resolution			**16-Character x 2-Line with 80-Icon (18-COM x 80-SEG)**		
Booster default value			VDD X 2 (VIN must be connecting to VDD.) (VOUT must be connecting to CAP2P.)		
Bias ratio default value			1/5		
IIC bus interface mode			**Reference 5.3.4. I²C interface**		
Interface Setting			Configuration Setting		
PS2	VDD	IIC bus interface mode	DIRC	VSS	COM1 → COM2 → . . . → COM16 → COMI1(COMI2)
PS1	VDD		SHL	VSS	SEG1 → SEG2 → . . . → SEG80
PS0	VDD/VSS		EXT	VDD	Enable ICON function and Enable Booster circuit
OSCSEL	VSS	Internal oscillator clock mode	BIAS	VDD	1/5 bias
MOD0	VDD	$00 ~ $0F as CGRAM	OSC1	OPEN	
MOD1	VDD		TEST[0:7]	OPEN	

The IIC-bus interface mode is not support read data and read busy flag function.

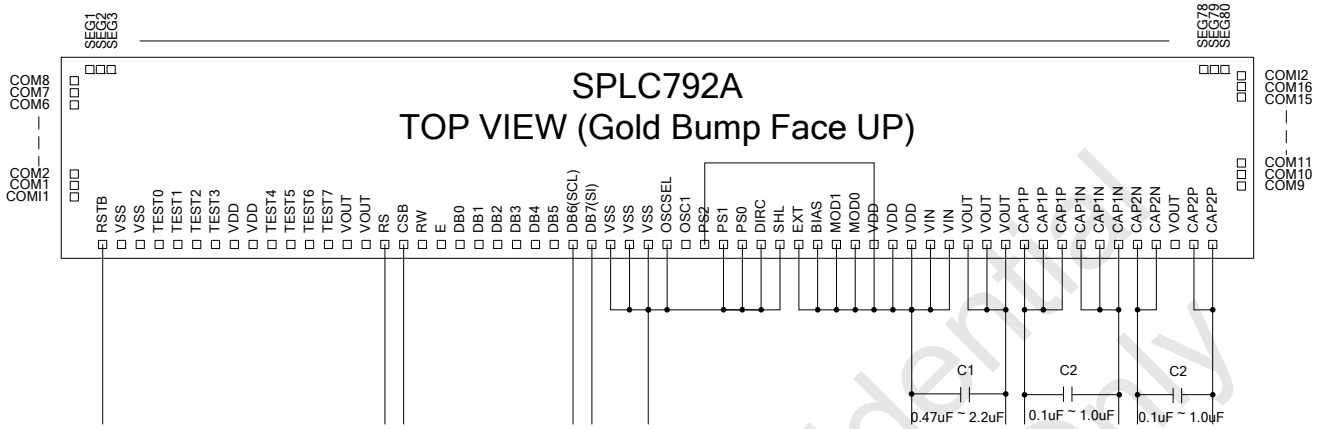
8.3.5. The application circuit of 3-SPI mode



Interface			3-wire SPI interface mode (**Reference 5.1.1 SELECTING THE INTERFACE TYPE**)		
Resolution			**16-Character x 2-Line with 80-Icon (18-COM x 80-SEG)**		
Booster default value			VDD X 3 (VIN must be connecting to VDD.)		
Bias ratio default value			1/5		
3-wire SPI interface mode			**Reference 5.3.3. 3-wires SPI interface**		
Interface Setting			Configuration Setting		
PS2	VDD	3-wire SPI interface mode	DIRC	VSS	COM1 → COM2 → . . . → COM16 → COMI1(COMI2)
PS1	VSS		SHL	VSS	SEG1 → SEG2 → . . . → SEG80
PS0	VDD		EXT	VDD	Enable ICON function and Enable Booster circuit
OSCSEL	VSS	Internal oscillator clock mode	BIAS	VDD	1/5 bias
MOD0	VDD	$00 ~ $0F as CGRAM	OSC1	OPEN	
MOD1	VDD		TEST[0:7]	OPEN	

The 3-wire SPI interface mode is not support read data and read busy flag function.

8.3.6. The application circuit of 4-SPI mode

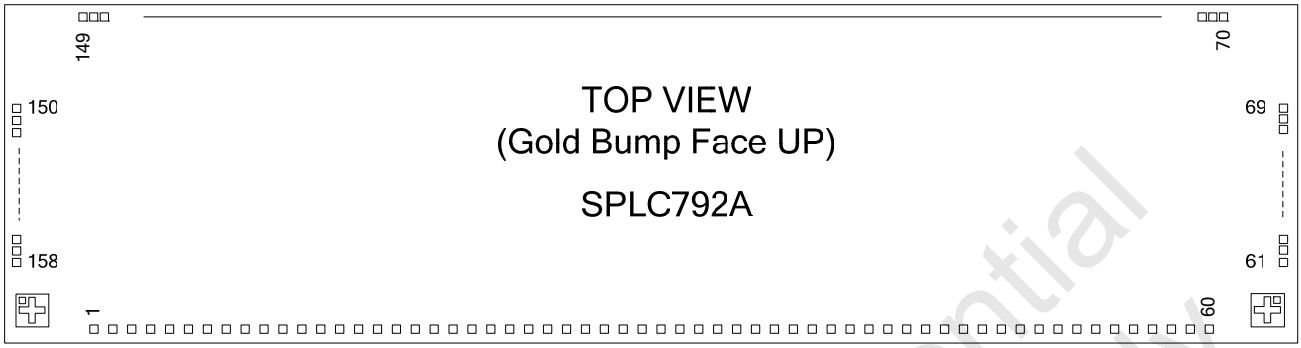


Interface			4-wire SPI interface mode (**Reference 5.1.1 SELECTING THE INTERFACE TYPE**)		
Resolution			**16-Character x 2-Line with 80-Icon (18-COM x 80-SEG)**		
Booster default value			VDD X 3 (VIN must be connecting to VDD.)		
Bias ratio default value			1/5		
4-wire SPI interface mode			**Reference 5.3.2. 4-wires SPI interface**		
Interface Setting			Configuration Setting		
PS2	VDD	4-wire SPI interface mode	DIRC	VSS	COM1 → COM2 → . . . → COM16 → COMI1(COMI2)
PS1	VSS		SHL	VSS	SEG1 → SEG2 → . . . → SEG80
PS0	VSS		EXT	VDD	Enable ICON function and Enable Booster circuit
OSCSEL	VSS	Internal oscillator clock mode	BIAS	VDD	1/5 bias
MOD0	VDD	$00 ~ $0F as CGRAM	OSC1	OPEN	
MOD1	VDD		TEST[0:7]	OPEN	

The 4-wire SPI interface mode is not support read data and read busy flag function.

9. CHIP INFORMATION

9.1. PAD Assignment



9.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size		4040	700	μm
Chip thickness		400 ± 20		
Pad pitch	1~60	59		
	61~69, 150~158		42	
	70~149	42		
Pad size	1~60	44	80	
	61~158	29	95	

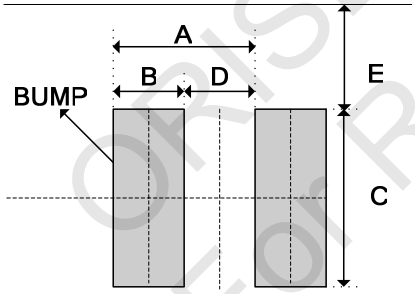
Note1: Chip size included scribe line.

Note2: The Chip thickness is an average value. Please refer to ISO document to get the specific Chip thickness information.

9.2.1. Output Pads

◎Pad no. 61 ~ 158(Output)

Boundary (Include Scribe Land)

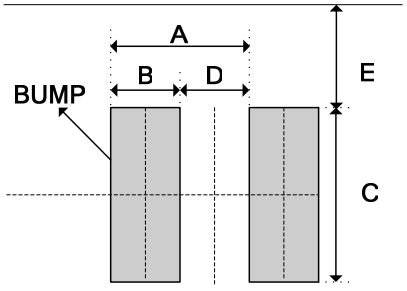


Item	Symbol	Size
Bump Pitch	A	42 um
Bump Width	B	27 um
Bump height	C	95 um
Bump space	D	15 um
Bump area	BxC	2565 um^2
Chip boundary	E	65 um

9.2.2. Input Pads

◎Pad no. 1 ~ 60 (Input)

Boundary (Include Scribe Land)



Item	Symbol	Size
Bump Pitch	A	59 um
Bump Width	B	44 um
Bump height	C	80 um
Bump space	D	15 um
Bump area	BxC	3520 um^2
Chip boundary	E	65 um

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	RSTB	-1740.5	-245
2	VSS	-1681.5	-245
3	VSS	-1622.5	-245
4	TEST0	-1563.5	-245
5	TEST1	-1504.5	-245
6	TEST2	-1445.5	-245
7	TEST3	-1386.5	-245
8	VDD	-1327.5	-245
9	VDD	-1268.5	-245
10	TEST4	-1209.5	-245
11	TEST5	-1150.5	-245
12	TEST6	-1091.5	-245
13	TEST7	-1032.5	-245
14	VOUT	-973.5	-245
15	VOUT	-914.5	-245
16	RS	-855.5	-245
17	CSB	-796.5	-245
18	RW	-737.5	-245
19	E	-678.5	-245
20	DB0	-619.5	-245
21	DB1	-560.5	-245
22	DB2	-501.5	-245
23	DB3	-442.5	-245
24	DB4	-383.5	-245
25	DB5	-324.5	-245
26	DB6	-265.5	-245
27	DB7	-206.5	-245
28	VSS	-147.5	-245
29	VSS	-88.5	-245
30	VSS	-29.5	-245
31	OSCSEL	29.5	-245
32	OSC1	88.5	-245
33	PS2	147.5	-245
34	PS1	206.5	-245
35	PS0	265.5	-245
36	DIRC	324.5	-245
37	SHL	383.5	-245
38	EXT	442.5	-245
39	BIAS	501.5	-245
40	MOD1	560.5	-245
41	MOD0	619.5	-245
42	VDD	678.5	-245
43	VDD	737.5	-245
44	VDD	796.5	-245
45	VIN	855.5	-245
46	VIN	914.5	-245
47	VOUT	973.5	-245
48	VOUT	1032.5	-245
49	VOUT	1091.5	-245
50	CAP1P	1150.5	-245
51	CAP1P	1209.5	-245
52	CAP1P	1268.5	-245
53	CAP1N	1327.5	-245
54	CAP1N	1386.5	-245
55	CAP1N	1445.5	-245
56	CAP2N	1504.5	-245
57	CAP2N	1563.5	-245
58	VOUT	1622.5	-245
59	CAP2P	1681.5	-245
60	CAP2P	1740.5	-245
61	COM9	1907.5	-157
62	COM10	1907.5	-115
63	COM11	1907.5	-73
64	COM12	1907.5	-31
65	COM13	1907.5	11
66	COM14	1907.5	53
67	COM15	1907.5	95
68	COM16	1907.5	137
69	COMI2	1907.5	179
70	SEG80	1659	237.5
71	SEG79	1617	237.5
72	SEG78	1575	237.5
73	SEG77	1533	237.5
74	SEG76	1491	237.5
75	SEG75	1449	237.5
76	SEG74	1407	237.5
77	SEG73	1365	237.5
78	SEG72	1323	237.5
79	SEG71	1281	237.5
80	SEG70	1239	237.5
81	SEG69	1197	237.5
82	SEG68	1155	237.5
83	SEG67	1113	237.5
84	SEG66	1071	237.5
85	SEG65	1029	237.5
86	SEG64	987	237.5
87	SEG63	945	237.5
88	SEG62	903	237.5
89	SEG61	861	237.5
90	SEG60	819	237.5
91	SEG59	777	237.5
92	SEG58	735	237.5
93	SEG57	693	237.5
94	SEG56	651	237.5
95	SEG55	609	237.5
96	SEG54	567	237.5
97	SEG53	525	237.5
98	SEG52	483	237.5
99	SEG51	441	237.5
100	SEG50	399	237.5
101	SEG49	357	237.5
102	SEG48	315	237.5
103	SEG47	273	237.5
104	SEG46	231	237.5
105	SEG45	189	237.5
106	SEG44	147	237.5
107	SEG43	105	237.5
108	SEG42	63	237.5
109	SEG41	21	237.5
110	SEG40	-21	237.5
111	SEG39	-63	237.5
112	SEG38	-105	237.5
113	SEG37	-147	237.5
114	SEG36	-189	237.5
115	SEG35	-231	237.5
116	SEG34	-273	237.5
117	SEG33	-315	237.5
118	SEG32	-357	237.5
119	SEG31	-399	237.5
120	SEG30	-441	237.5
121	SEG29	-483	237.5
122	SEG28	-525	237.5
123	SEG27	-567	237.5
124	SEG26	-609	237.5
125	SEG25	-651	237.5
126	SEG24	-693	237.5
127	SEG23	-735	237.5
128	SEG22	-777	237.5
129	SEG21	-819	237.5
130	SEG20	-861	237.5
131	SEG19	-903	237.5
132	SEG18	-945	237.5
133	SEG17	-987	237.5
134	SEG16	-1029	237.5
135	SEG15	-1071	237.5
136	SEG14	-1113	237.5
137	SEG13	-1155	237.5
138	SEG12	-1197	237.5
139	SEG11	-1239	237.5
140	SEG10	-1281	237.5
141	SEG9	-1323	237.5
142	SEG8	-1365	237.5
143	SEG7	-1407	237.5
144	SEG6	-1449	237.5
145	SEG5	-1491	237.5
146	SEG4	-1533	237.5
147	SEG3	-1575	237.5
148	SEG2	-1617	237.5
149	SEG1	-1659	237.5
150	COM8	-1907.5	179
151	COM7	-1907.5	137
152	COM6	-1907.5	95
153	COM5	-1907.5	53
154	COM4	-1907.5	11
155	COM3	-1907.5	-31
156	COM2	-1907.5	-73
157	COM1	-1907.5	-115
158	COMI1	-1907.5	-157

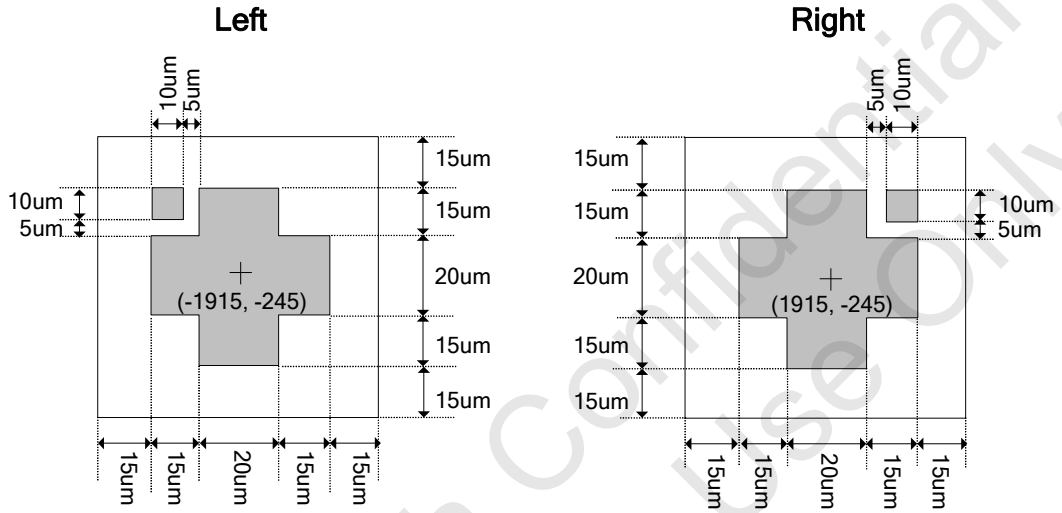
9.4. Alignment Mark

--Alignment Mark coordinate

Left (-1915, -245)

Right (1915, -245)

--Alignment Mark size



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11. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 15, 2010	0.3	Modify Pin Description : For 3-Wire / 4-Wire SPI Interface Mode DB7(SI) : Serial input data DB6 (SCL) : Serial input clock	7
NOV. 05, 2009	0.2	1. Add SPLC792A-002A Font Information. 2. Modify VIN must be connecting to VDD ➔ VIN must be connecting to VOUT.	36 52
MAY. 27, 2009	0.1	Original	61