TX: 4 lane RX: 4 lane jesd204b subclass1,所以使用SYSREF和SYNC信号,保证deterministic latency

ADRV9009 JESD debug

1、4个DAC: IO/Q0, I1/Q1, DAC为14bit, 实际 JESD204B传输按照16bit传输

2、4个ADC: I0/Q0, I1/Q1,ADC为16bit,实 JESD204B传输按照16bit传输

即4个DAC对应两路TX,每路TX对应I/Q两路, 所以需要两个DAC

xilinx的jesd204b的IP中,Lanes per Link参数配置,指的是每个IP中最多有几个lane,比如zynq 7100中最多有8个lane

## 1.每个lane最多有8个link

The JESD204B specification calls out three device subclasses: Subclass 0—no support for deterministic latency, Subclass 1—deterministic latency using SYNEC-, Subclass 2—deterministic latency using SYNCC-, Subclass 0 can simply be compared to a JESD204A link. Subclass 1 is primarily intended for converters operating at or above 500 MSPS white Subclass 2 is primarily for converters operating below \$00 MSPS

2. JESD204B三个subclass的区别 © 500 MSF

JESD204的版本对比和LVDS对比 ⊙

3. 可支持的最大lane data rate 🌼 12.5Gbp

## Table 1. Comparison Between Serial LVDS and JESD204 Specifications

JESD204E

Function	Serial LVDS	JESD204	JESD204A	JESD204B
Specification Release	2001	2006	2008	2011
Maximum lane Rate	1.0 Gbps	3.125 Gbps	3.125 Gbps	12.5 Gbps
Multiple Lanes	No	No	Yes	Yes
Lane Synchronization	No	No	Yes	Yes
Multidevice Synchronization	No	Yes	Yes	Yes
Deterministic Latency	No	No	No	Yes
Harmonic Clocking	No	No	No	Yes



Calculate the lane rate using Equation 1.

Lane Rate = I/Q Sample Rate  $\times M \times N' \times (10 \div 8) \div L$  (1)