Application Report
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JESD204B Multi-Device Synchronization Using LMK0461x

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ABSTRACT

JESD204B is getting increasingly popular in communication space adopting the beamforming technology. Multiple Antennas per system are used to have better sensitivity. Each Antenna requires synchronization between them to have precise control of phases during transmission and reception. JESD40B is also getting popular in Medical Imaging, phase array radar applications.

The LMK0461x device family is the industry's highest performance with lowest power jitter cleaner family with JESD204B support. High-frequency device clock and low frequency SYSREF clocks can be generated with programmable analog and digital delays and SYNC functionality. The device provides possibility to control the SYNC and SYSREF functions by SYNC pin (pin mode) or SPI programming. Each clock output can be used either as a device clock or SYSREF clock.

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1 LMK0461X JESD204B Support

The LMK04616 can be used to generate 16 DEVICE/SYSREF clocks and LMK04610 can generate 10 DEVICE/SYSREF clocks. As mentioned previously, each clock output can be configured as a DEVICE clock or a SYSREF clock. This gives extra flexibility to have different SYSREF frequencies on the outputs if needed. LMK0461x supports continuous SYSREF mode and a pulsed SYSREF mode. The SYNC and RISREF requests can be issued either by SPI interface or using the SYNC pin. The SYNC pin have dual functionality. It can be configured to issue the Dividers SYNC or it can also be configured send SYSREF request. The SYSREF clock can be a continuous clock or can be predefined number of pulses which can be programmed for 1 to 32. The SYSREF clock can also be disabled glitch free when it is not required. To have more flexibility in adjusting the relative timings and compensating for the routing mismatches, digital delays or analog delays can be added in the each clock output.

2 Multichip Synchronization Support Using LMK0461x Devices

The LMK0461x device generates the 5 or 8 Device clock and SYSREF pairs. Each of the 10/16 outputs can be a device clock or a SYSREF clock. Up to 8 devices requiring JESD204B clock pairs can be attached to the single devices. For more complex systems requiring more than 8 Device clock and SYSREF pairs, multiple LMK0461x can be used in chained configurations. LMK04616 can also be used in Master stave configuration to have many clocks pairs. The following sections describe some of the possible configurations.

3 Multichip Synchronization Configuration Using Single LMK0461x

Configuration shown in Figure 1 can be used for the system requiring up to 8 SYSREF and Device clock pairs using the LMK04616. Alternatively, LMK04610 can be used if up to 5 SYSREF and Device clocks pairs are required. After the device configuration, once the SYNC is issued, all the clocks are edge aligned. LMK04616 in this case is working in dual PLL jitter cleaner mode. Alternatively, if the input clock is clean and does not require jitter cleaning, LMK0461x can be configured in the Single PLL2 only mode and the input clock can be applied at OSCin.

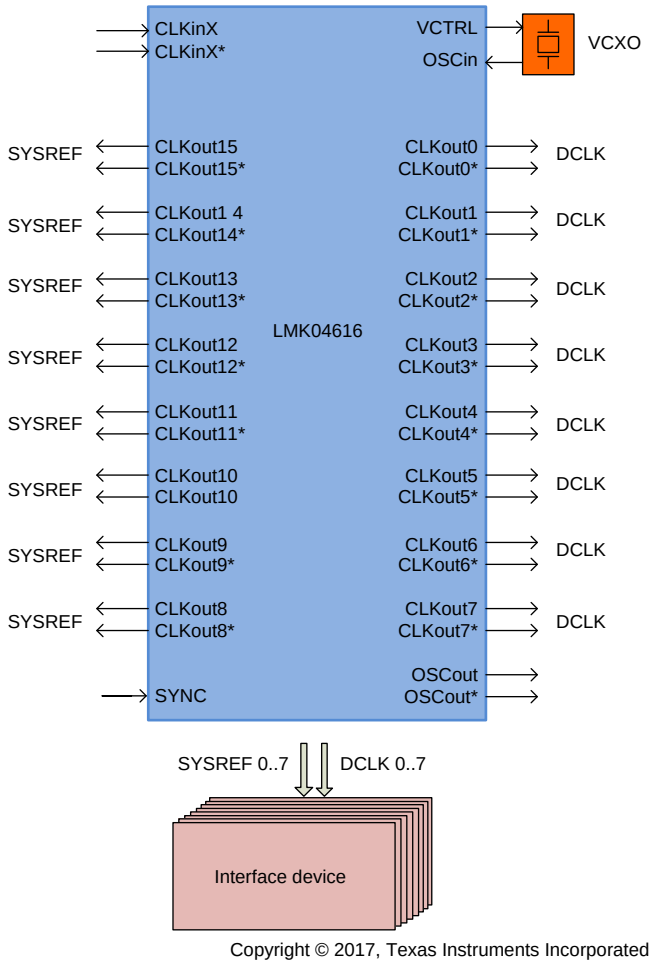

Figure 1. Multichip Synchronization Using LMK0461x

Figure 2 explains the SYNC and SYSREF execution flow.

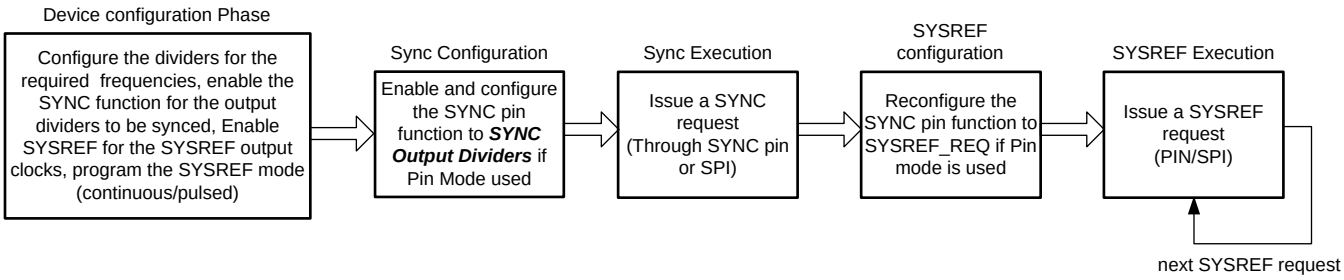

Figure 2. LMK0461x Configuration Flow for SYSREF Generation

Once the correct output dividers are programmed, the SYNC to the output dividers is required. This ensures that all the channel dividers start with the same edge of the clock. Doing that, all the output clocks are edge aligned. As mentioned earlier, the dividers SYNC can be done with the SPI or through the SYNC pin by configuring this pin to the Dividers SYNC mode. Once SYNC is issued, SYSREF functions can be used on the output clocks. The Sync can also be SPI controlled or Pin controlled. If SYSREF request through SYNC pin is used, the SYNC pin needs to be reconfigured to SYSREF_REQ function.

3.1 SYSREF Modes

There are three SYSREF modes supported by LMK0461x, which are explained below:

3.1.1 Continuous SYSREF Mode

If SYSREF needs to be always on, then there is no difference between the device clock setup and SYSREF setup. Output dividers should to be programed to the desired value and after that SYNC is executed, all the clocks are aligned. Digital and Analog delay functions can be anyway used on individual outputs.

3.1.2 SYSREF Request Mode

The SYSREF clocks in this case can be enabled or disabled glitch free when in this mode. This mode can be entered using SPI or SYNC pin. SYSREF Pulse counter should be set to Continuous. While using the SPI, when GLOBAL_CONT_SYSREF is set to 1, the SYSREF continuous clock is enabled for the clocks which are enabled for SYSREF functions. When GLOBAL_CONT_SYSREF is set to 0, the clock is disabled. This mode can also be enabled by using the SYNC pin. For that, the SYNC pin function should be enabled and set to SYSREF_REQ. A high level on the SYNC pin will enable the SYSREF clocks and low level will disable the clocks. The waveform in Figure 3 clarifies the function.

Figure 3. SYSREF Request Mode

The SYSREF pulses can be controlled by the pulse width at the SYNC pin. When the SYNC pin is asserted, the channel is synchronously set to continuous mode providing continuous pulses at the SYSREF frequency until the SYNC pin is unasserted. SYSREF stops after completing the final pulse synchronization.

3.1.3 Pulsed SYSREF Mode

When OUTCH_SYSREF_PLSCNT is set from between 1 to 32, the SYSREF pulser is enabled. While using the SPI interface for SYSREF, setting GLOBAL_SYSREF to 1 enables the number of pulses from the SYSREF enabled outputs. The GLOBAL_SYSREF is a self-clearing bit.

The pulser can also be enabled using the SYNC pin. When SYNC pin is enabled for SYSREF functions, based on the polarity configuration of the pin, an edge on the SYNC pin triggers the pulses at the outputs. Figure 4 shows the function using Pin mode.

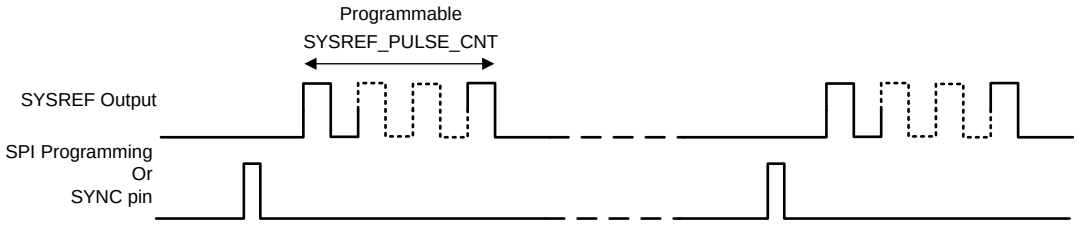

Figure 4. Pulsed SYSREF Mode

4 Multiple SYSREF Frequencies

LMK0461x supports multiple SYSREF frequencies. In case of multiple SYSREF frequencies the latencies until SYSREF pulses start are different. As shown in Figure 5, the different SYSREF signals are rising edge aligned with the device clock. The different SYSREF signals might not be rising edge aligned if different SYSREF frequencies are used.

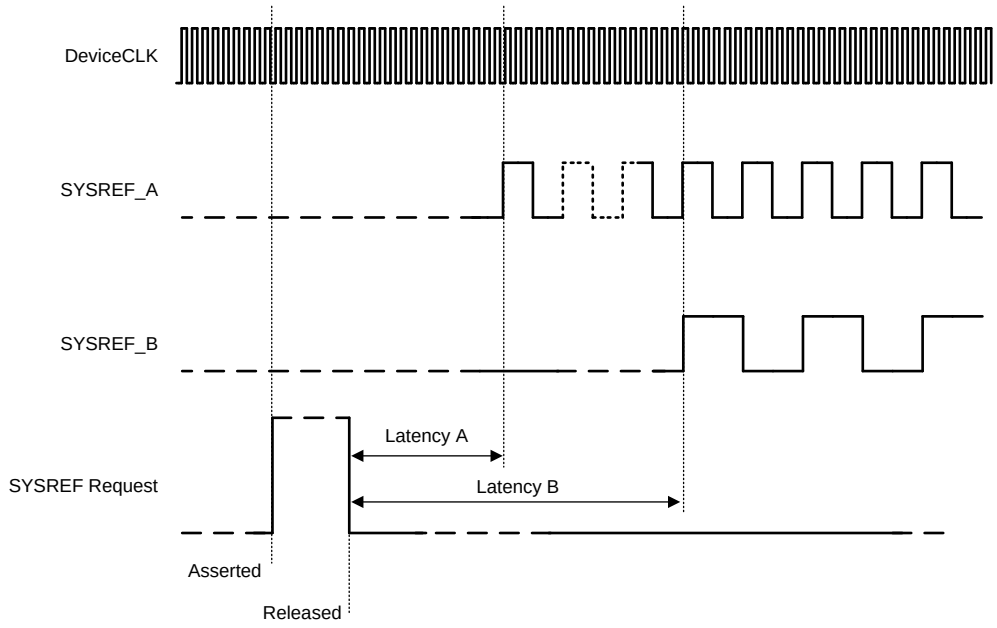

Figure 5. Multiple SYSREF Frequencies

5 LMK0461x Device JESD204B Setup Examples

The step-by-step setup procedure for different modes is shown below.

5.1 SYNC Functions

5.1.1 SYNC Function Using Pin Mode

Following steps can be followed to trigger the output divider SYNC:

STEP 1: SYNC_EN_CHx should be set 1 for the channels which needs to synced.

STEP 2: Program EN_SYNC_PIN_FUNC to 1. This enables the different functions supported by the SYNC pin.

STEP 3: Program SYNC_PIN_FUNC[1:0] to 00b (default). This sets the SYNC pin for SYNC function.

STEP 4: SYNC_INV, when set to 0 (default), SYNC is rising edge triggered. When set to 1, the SYNC pin is internally inverted and is falling edge triggered.

STEP 5: Depending on the SYNC_INV value, an edge on the SYNC pin triggers the synchronization of the output channels.

5.1.2 SYNC Using SPI

1. Program the EN_SYNC_PIN_FUNC to 0. This disables the pin mode for SYNC function.
2. SYNC_EN_CHx should be set 1 for the channels which must synced.
3. Writing 1 to the GLOBAL_SYNC puts the device into SYNC. Writing 0 exits the SYNC.

5.2 SYNC Using TICSpro Interface

1. Go to OUTPUTS tab, enable the SYNC function for the output dividers to be synced as Figure 6 shows.

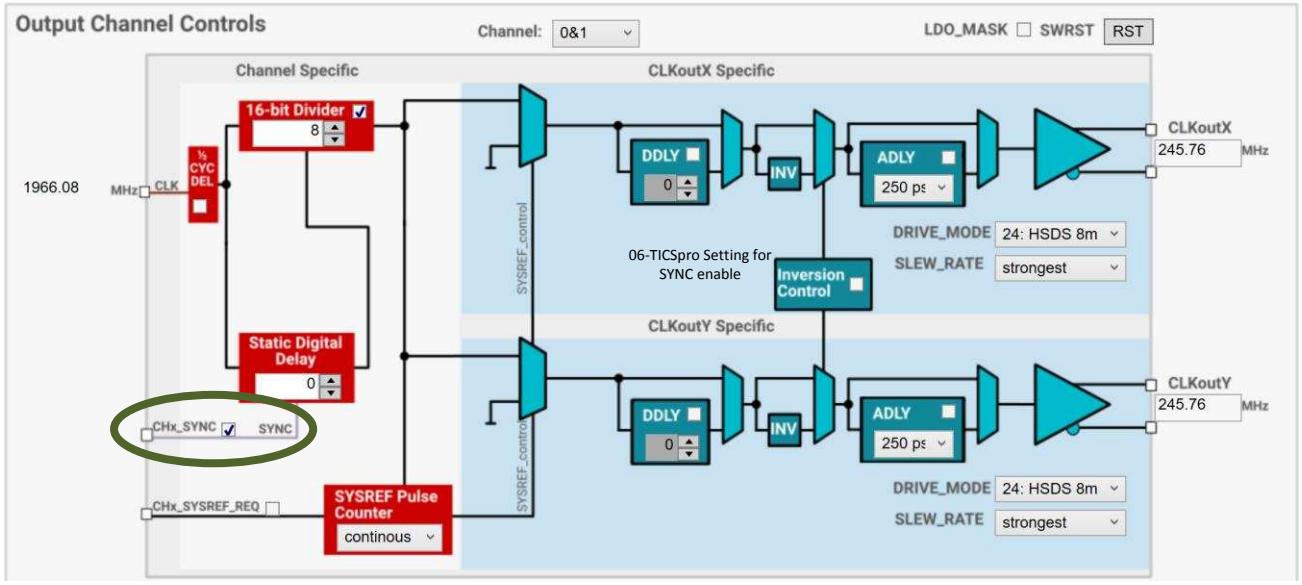

Figure 6. TICSpro Setting for SYNC Enable

2. Go to Generic Tab and set the EN_SYNC_PIN_FUNC as Figure 7 shows.

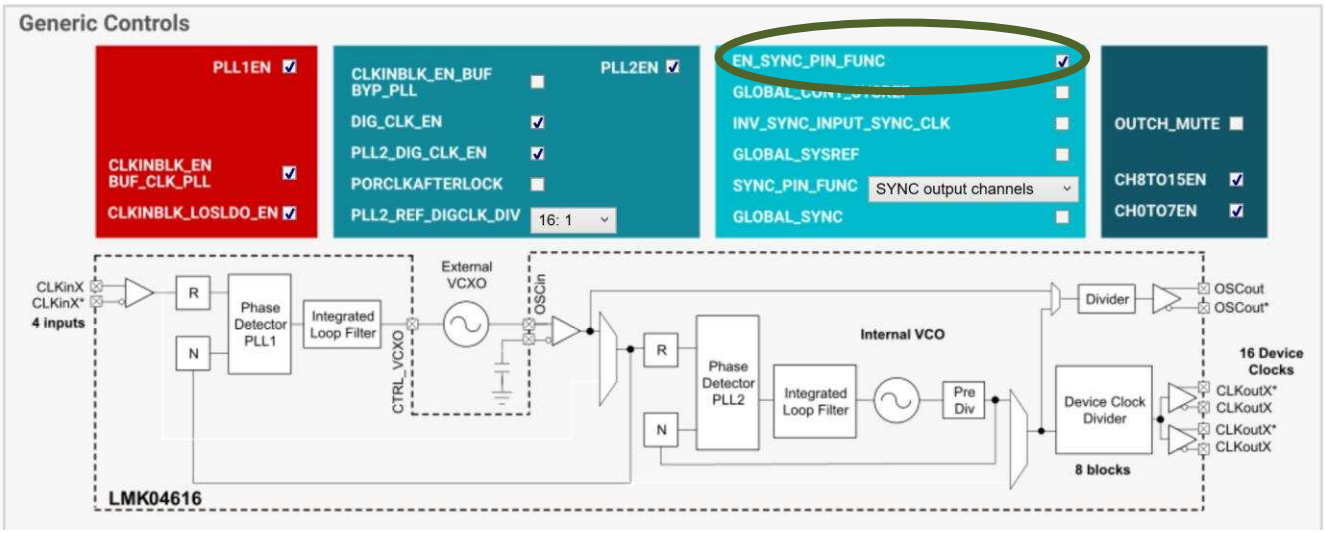

Figure 7. TICSpro Setting for SYNC Pin Function Enable

3. Select SYNC output Channels from the SYNC_PIN_FUNC drop-down options, as Figure 8 shows.

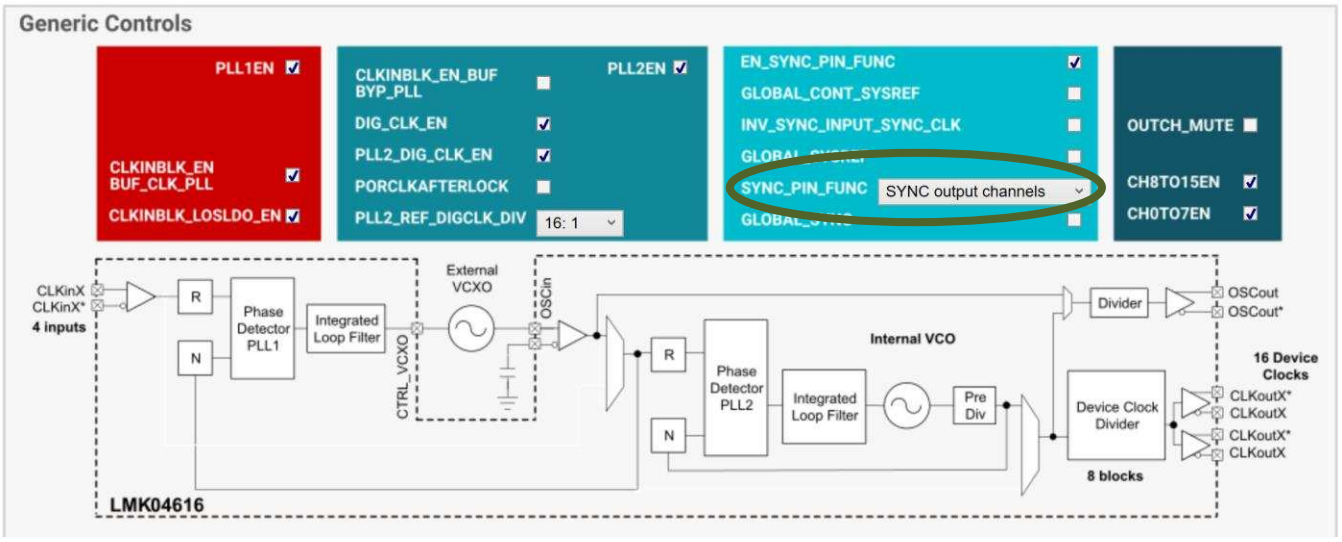

Figure 8. TICSpro Setting SYNC Pin Function

4. SYNC can be initiated by either of following ways

   (a) By checking and unchecking the SYNC from User Controls tab:

Figure 9. TICSpro SYNC Pin Control

   (b) By clicking on the Toggle Sync from the menu options

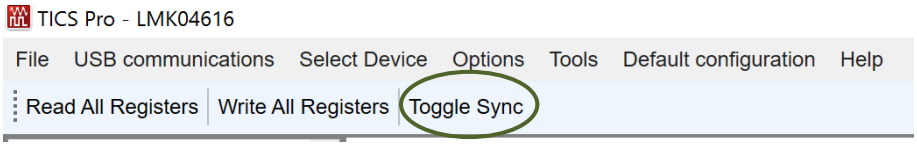

Figure 10. TICSpro Toggle Sync

   (c) By checking and unchecking Global SYNC from Generic tab.

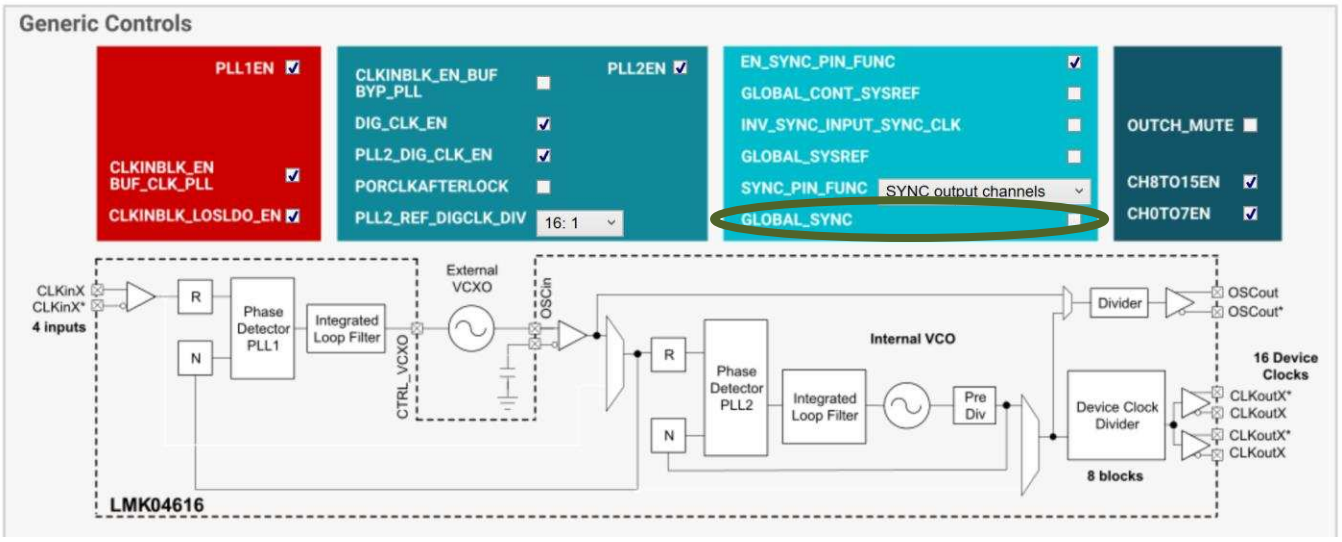

Figure 11. TICSpro Initiating SYNC Using GLOBAL_SYNC Bit

5.3 Configuring LMK0461x for SYSREF

This section provides the step-by-step instructions to configure the device for SYSREF generation.

5.3.1 Pulser Mode, Pin Controlled

1. Program SYSREF_EN_CHxx=1, enables corresponding output channels to generate SYSREF clock pulses.
2. Program EN_SYNC_PIN_FUNC=1, SYNC pin is enabled for SYSREF requests.
3. Program SYNC_PIN_FUNC=01, SYNC pin is programmed to accept the SYSREF requests.
4. Program OUTCH_SYSREF_PLSCNT= xx (1 to 32), programs the number of SYSREF pulses to be generated.
5. Applying rising Edge at SYNC pin generates **xx** number of pulses at the outputs enabled for SYSREF clocks.

5.3.2 Pulser Mode, SPI Controlled

1. Program SYSREF_EN_CHxx=1, enables corresponding output channels to generate SYSREF clock pulses.
2. Program EN_SYNC_PIN_FUNC=0, the SYSREF function on the SYNC pin is not enabled.
3. Program OUTCH_SYSREF_PLSCNT= xx (1 to 32), programs the number of SYSREF pulses to be generated.
4. Programming GLOBAL_SYSREF=1 generates the defined number of pulses on the SYSREF enabled channels.

5.4 SYSREF Configuration Example Using TICSpro Interface

5.4.1 SYSREF Pulsar Mode

1. Switch to OUTPUTS tab, enable the SYSREF function for the desired outputs. Set the SYSREF pulse counter to the desired number. It is set to 8 in this example. CHx_SYNC should also be enabled for the channel.

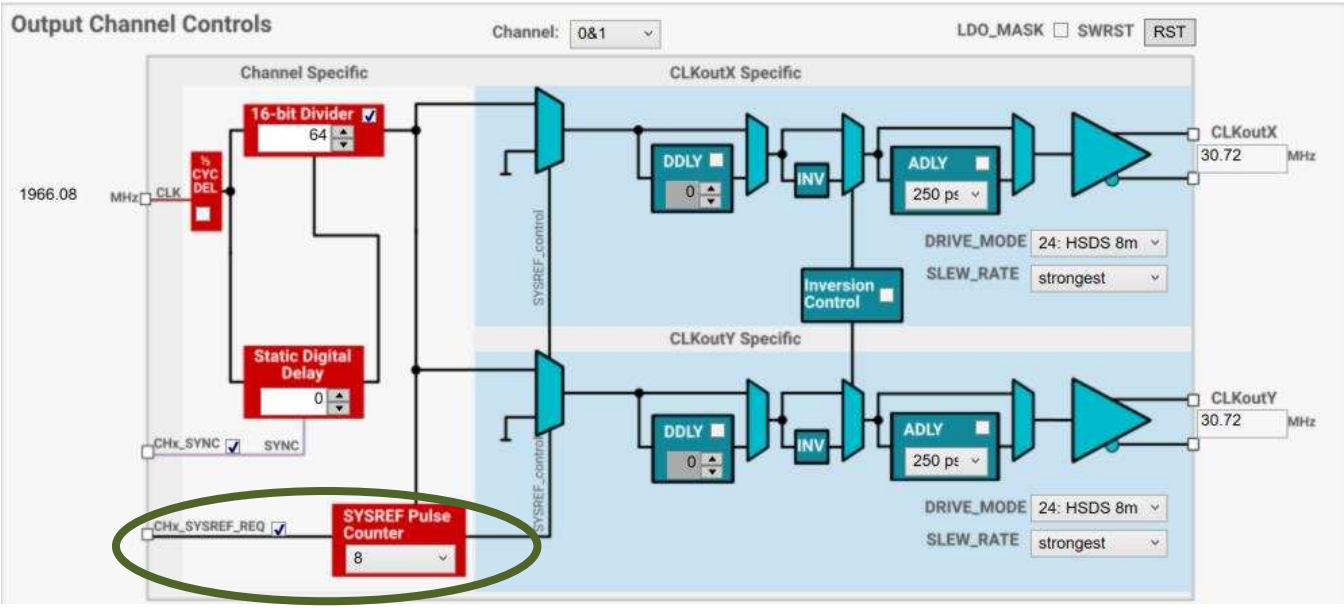

Figure 12. TICSpro Enabling Channel for SYSREF Pulsar Mode

2. Go to Generic Tab and set the EN_SYNC_PIN_FUNC lie shown in Figure 13.

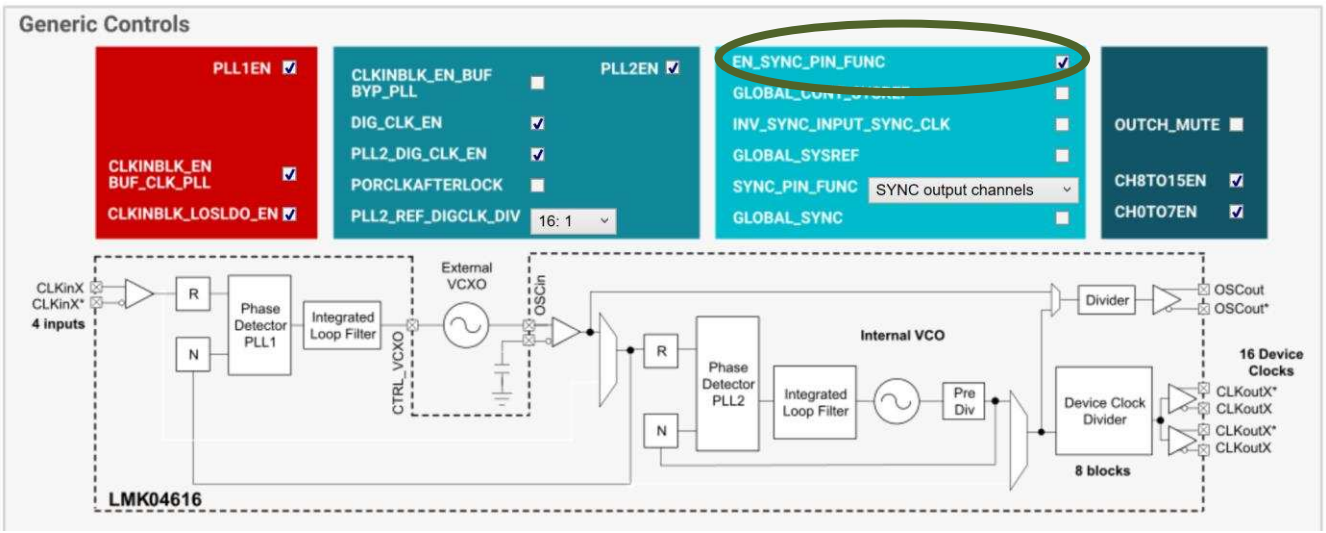

Figure 13. TICSpro Enabling SYNC Pin Function

3. Select SYSREF Request from the SYNC_PIN_FUNC drop-down options as shown in Figure 14.

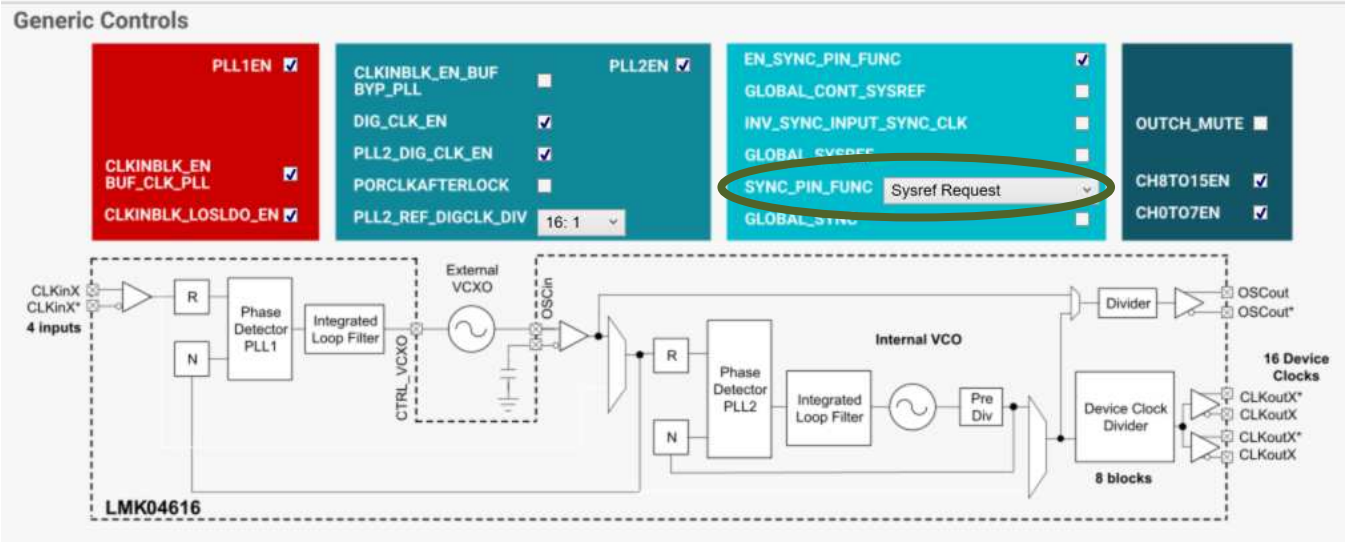

Figure 14. TICSpro Setting SYNC Pin Function to SYSREF Request

4. Issue a SYNC by clicking on the Toggle Sync from the menu options

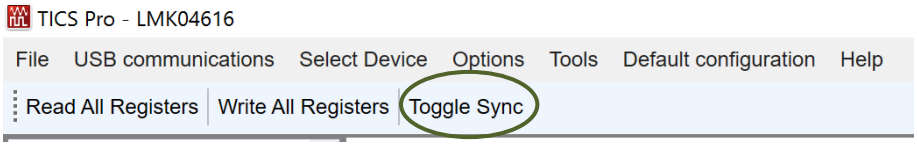

Figure 15. Issuing a SYNC Using Toggle SYNC

SYNC can also be issued by SYNC pin or CLOBAL_SYNC like explained in the SYNC section.

5. Switch to User Controls tab. Checking and unchecking the SYNC triggers the SYSREF pulses at the selected outputs.

Figure 16. TICSpro SYNC Pin Control

5.4.2 SYSREF Continuous Mode With Enable/Disable

1. Switch to OUTPUTS tab, enable the SYSREF function for the desired outputs. Set the SYSREF Pulse Counter to Continuous as shown in Figure 17.

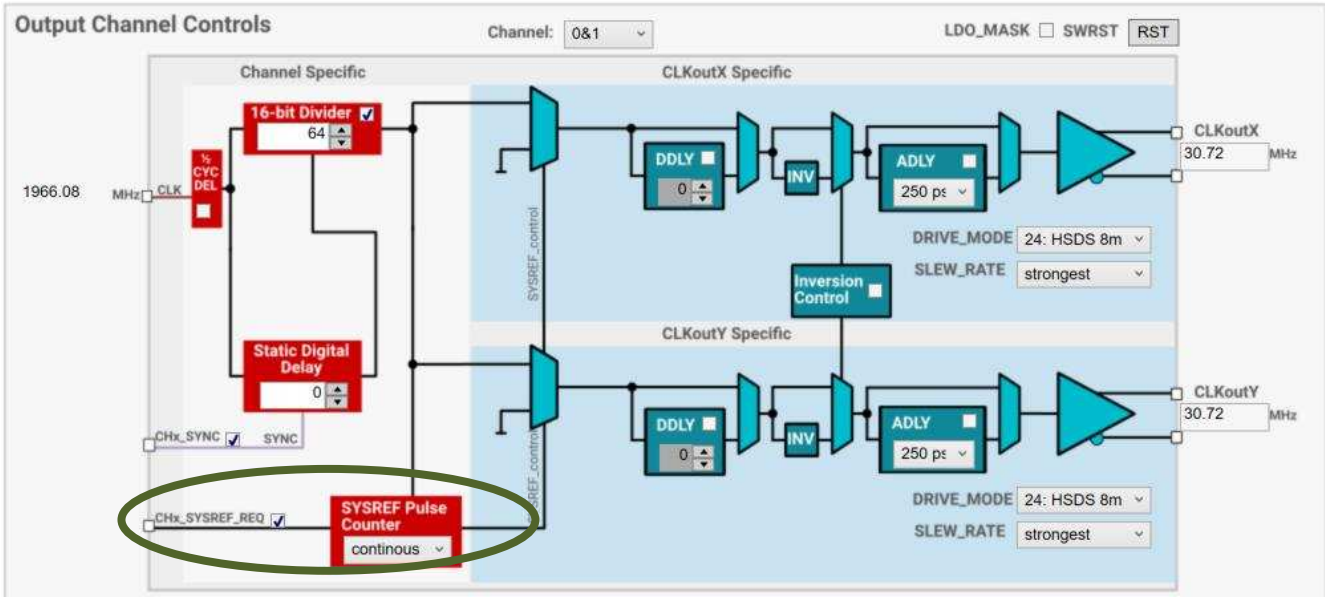

Figure 17. TICSpro Setting an Output in Continuous SYSREF Mode

2. Repeat step 2, 3, and 4 from the previous example.
3. As long as the signal level at the SYNC pin stays HIGH(SYNC ticked), the continuous pulses of SYSREF clock are generated at the corresponding outputs. Low level at the SYNC pin stops the SYSREF pulses.

6 Multi-Chip Synchronization Using Multiple LMK0461x Devices

Following sections shows some possible configurations of multiple LNMK0461X devices used for JESD204B link. Lab measurements are also performed on those configurations and shown in the next sections. The shown configurations are just few examples of how LMKo461x can be used in Multi-device Master slave environment. LMK0461x devices are not limited to these configurations only and more configurations are possible based on the system requirements.

6.1 LMK0461x Multi-Chip Sync Configuration 1A

The configuration is shown in Figure 18. Any of the two devices can be replaced by LMK04610 if fewer outputs are required. Using the LMK04616 devices, up to 16 SYSREF and 16 Device clocks can be generated using this configuration. Device-1 here operates in the dual-loop jitter cleaner mode and generates all the high performance Device clocks. The second device (Device-2) operates in the single-loop PLL2 only mode with zero delay enabled and generates all the SYSREF clocks. As the PLL2 in the first LMK04616 and the PLL2 in the second LMK04616 gets the same reference from the VCXO, after issuing a SYNC to the Device-1 and 2, all device clocks are aligned to each other and all SYSREF clocks are aligned to generate a deterministic timings. The SYNC signal inside the two devices is sampled with the Clock tree clock (output of the VCO Prescaler).

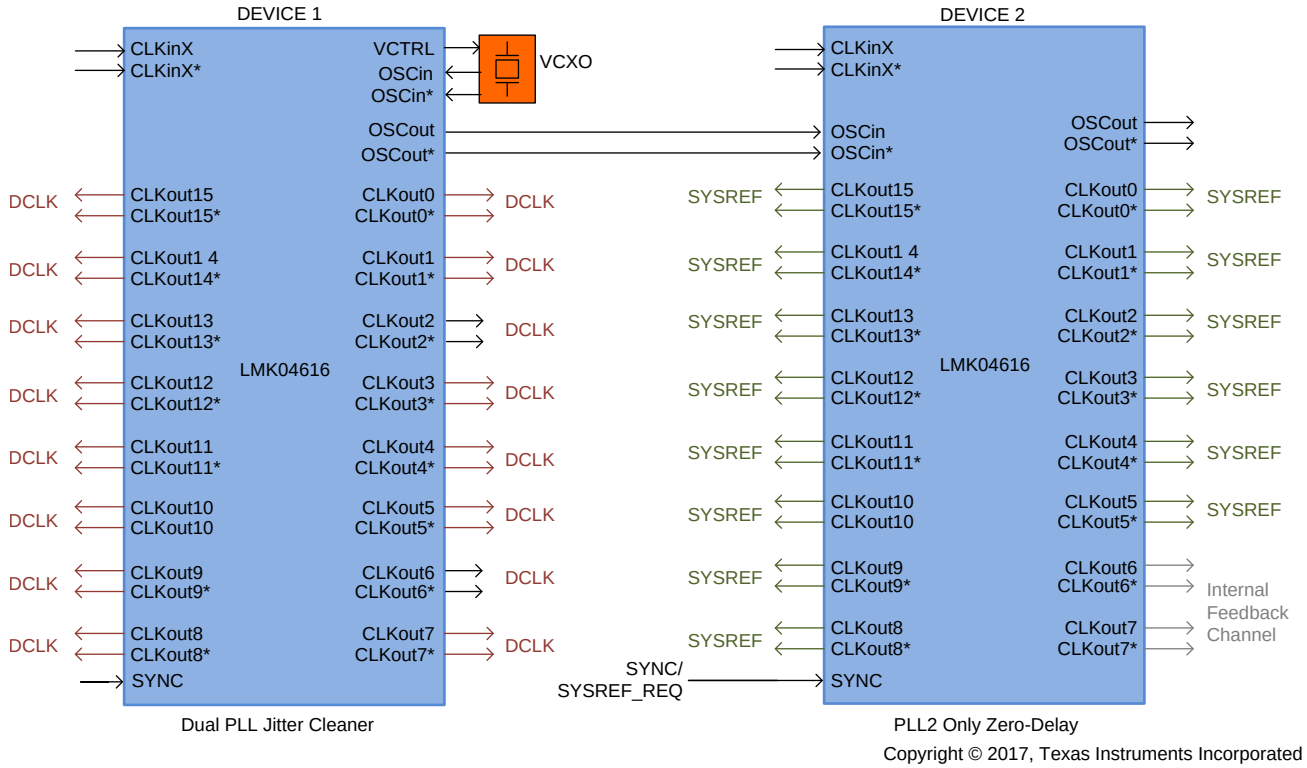

Figure 18. LMK0461x Device Configuration 1A

6.2 LMK0461x Multi Chip Sync Configuration 1B

Another configuration which can be derived from configuration 1A is the one shown in Figure 19.

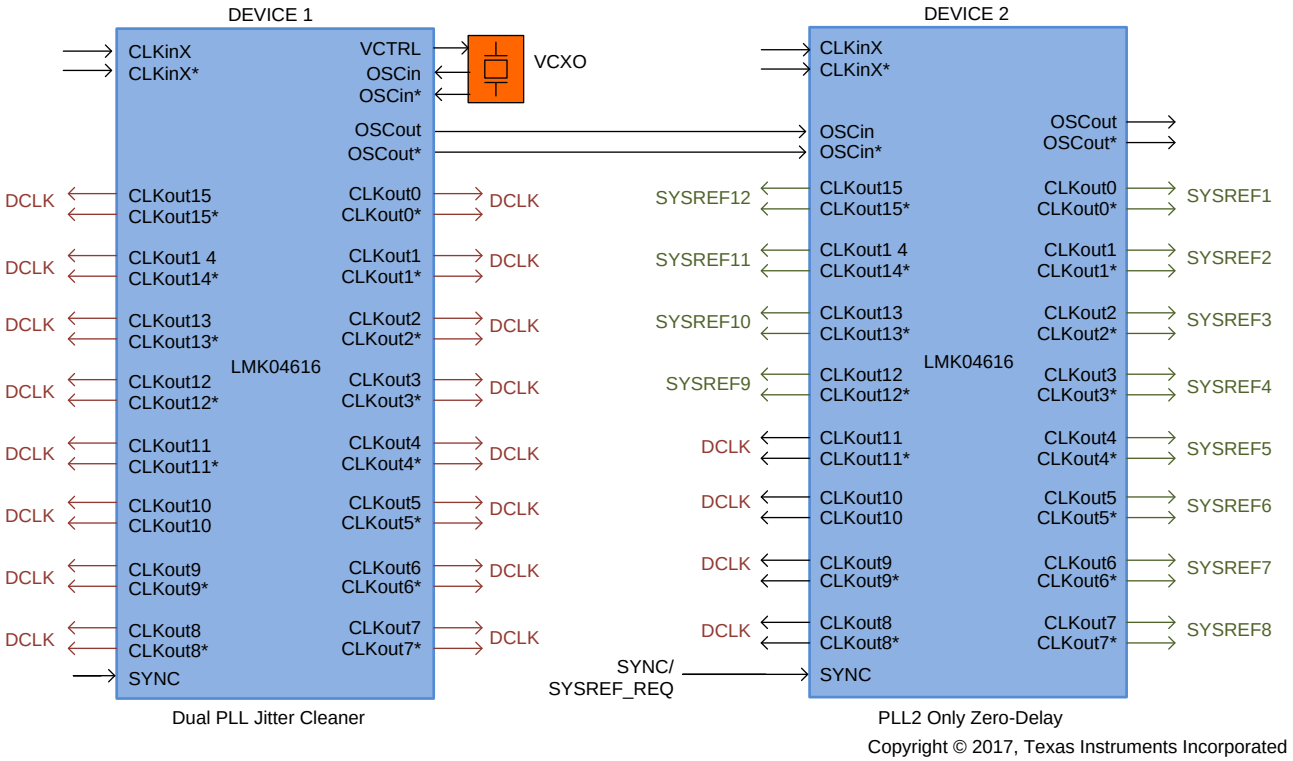

Figure 19. LMK0461x Device Configuration 1B

Here Device-1 is generating all the Device Clocks/high frequency clocks and Device-2 is used to generate some device clocks and all SYSREF clocks needed in the system. Device-1 can be in dual-loop jitter cleaner mode and the Device-2 is configured in PLL2-only zero delay mode and locks to the high frequency clock coming out of Device-1. This configuration can be used when there are fewer high frequency device clocks than SYSREF clocks.

6.3 Configuration 1C

Another improved configuration compared to the one shown above is to add a buffer after the VCXO. In this case, the clock input paths to the PLL2 in the two devices are very symmetrical.

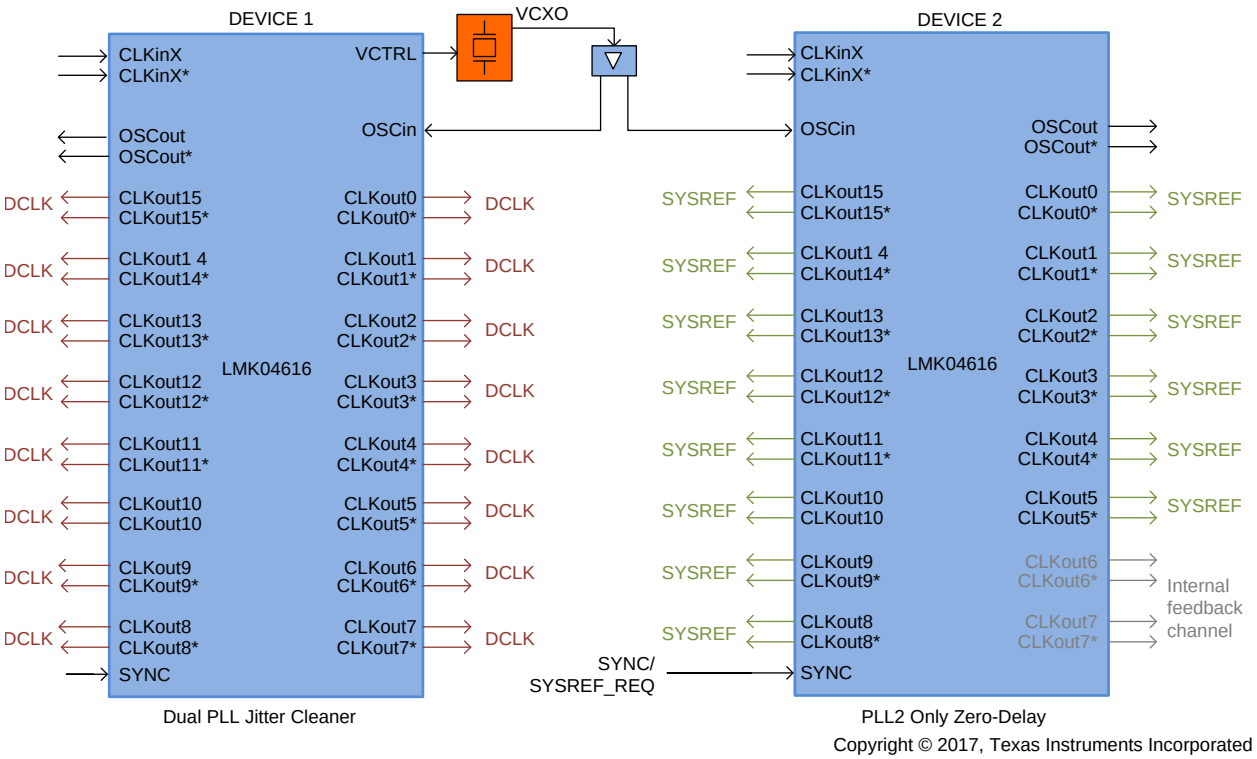

Figure 20. LMK0461x Device Configuration 1C

6.4 Configuration 2

Another configuration is shown in Figure 21 with three LMK0461x devices.

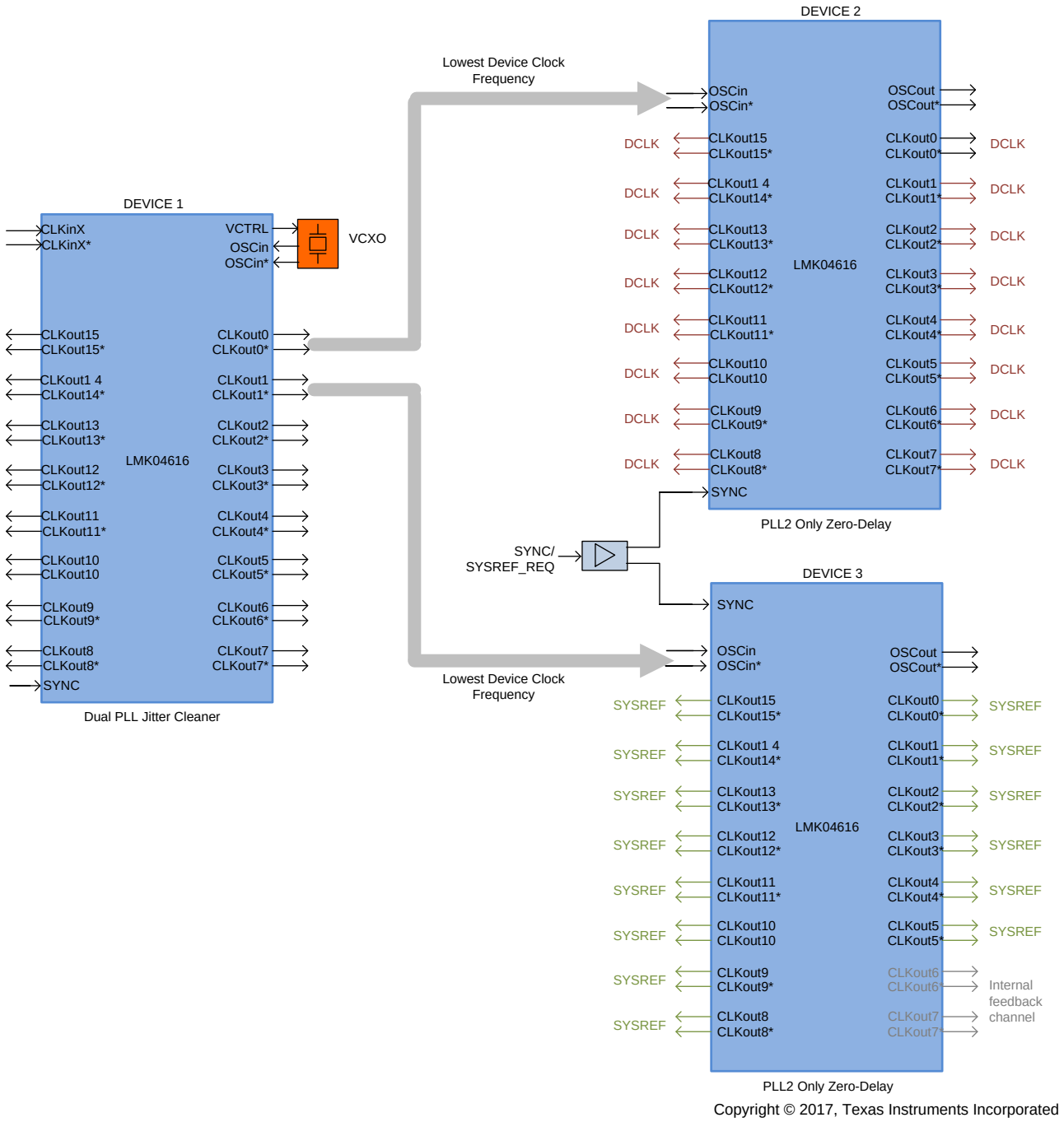

Figure 21. LMK0461x Device Configuration 2

In this configuration, Device-1 generates the synced high frequency clock and is supplied to two LMK0461x devices downstream. Device-1 can be in Jitter cleaner mode generating high the output clocks from dirty reference., while Device-2 and Device-3 downstream are in PLL2-only Zero delay mode and locking to the input clock. One of the downstream Devices generates the SYSREF clocks and the second generates the Device clocks. The timing uncertainty between the Device-2 and Device-3 is one Prescaler clock cycle because of the SYNC is sampled with the Prescaler clock and can start the dividers with one Prescaler cycle difference.

6.5 Configuration 3

Another configuration for generating multiple SYSREF clocks is shown in Figure 22.

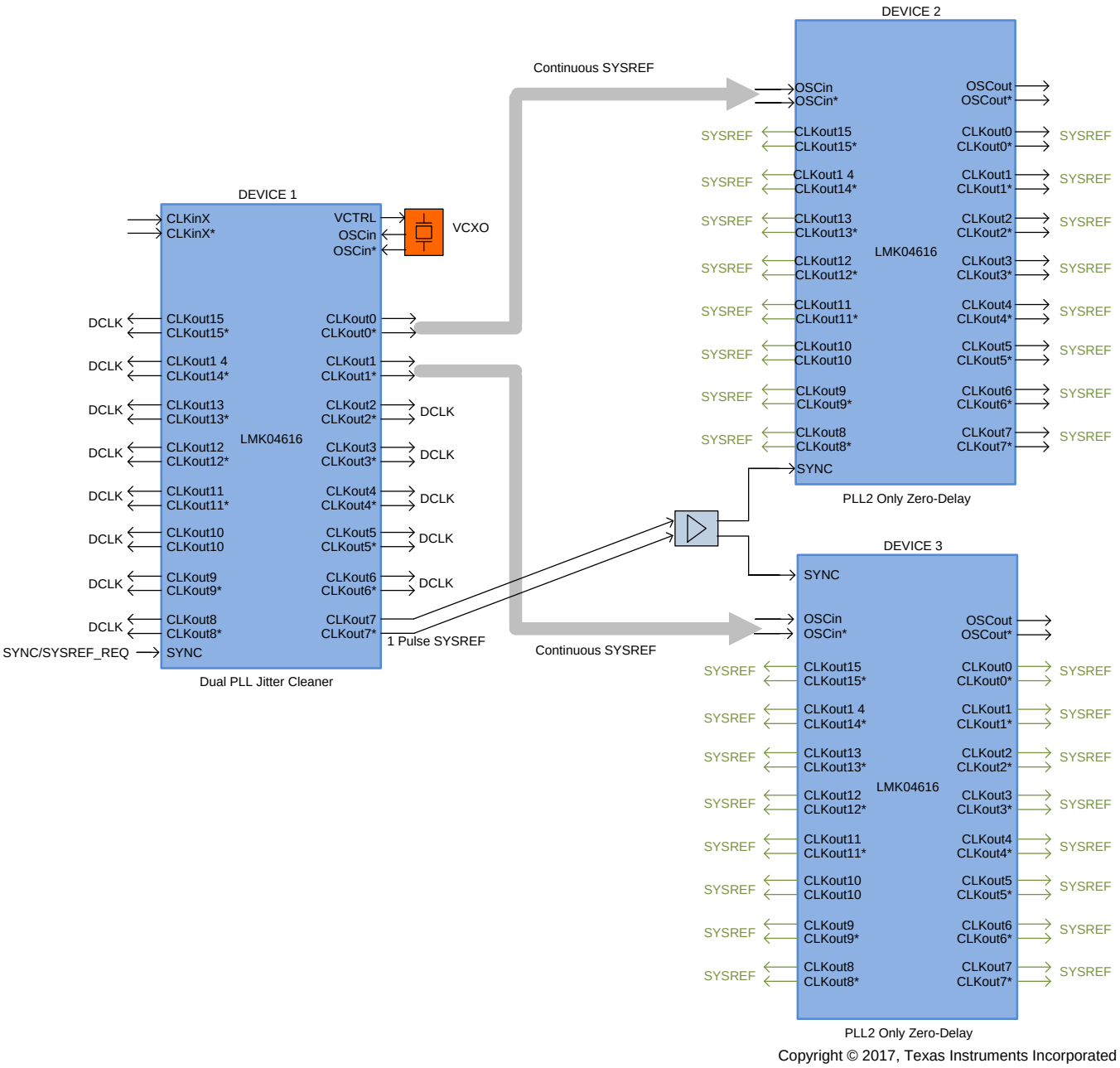

Figure 22. LMK0461x Device Configuration 3

Here the Device-1 acts as a master device and can generate all Device clocks. Device-2 and Device-3 are the slave devices and generates the SYSREF clocks. The slave devices are triggered by the master device synchronously. Master device generates two continuous SYSREF clocks and feeds it to the two slave devices. The slave devices operate in PLL2-only zero delay mode and lock to the input clock. The master device also generates a single pulse SYSREF and through the buffer connects to the SYNC pin. The slave devices are triggered synchronously by the master. The slave devices can be configured in pulsed or continuous SYSREF mode.

6.6 Configuration 4

The following master slave configuration can be used to generate SYSREF pairs from the slave devices.

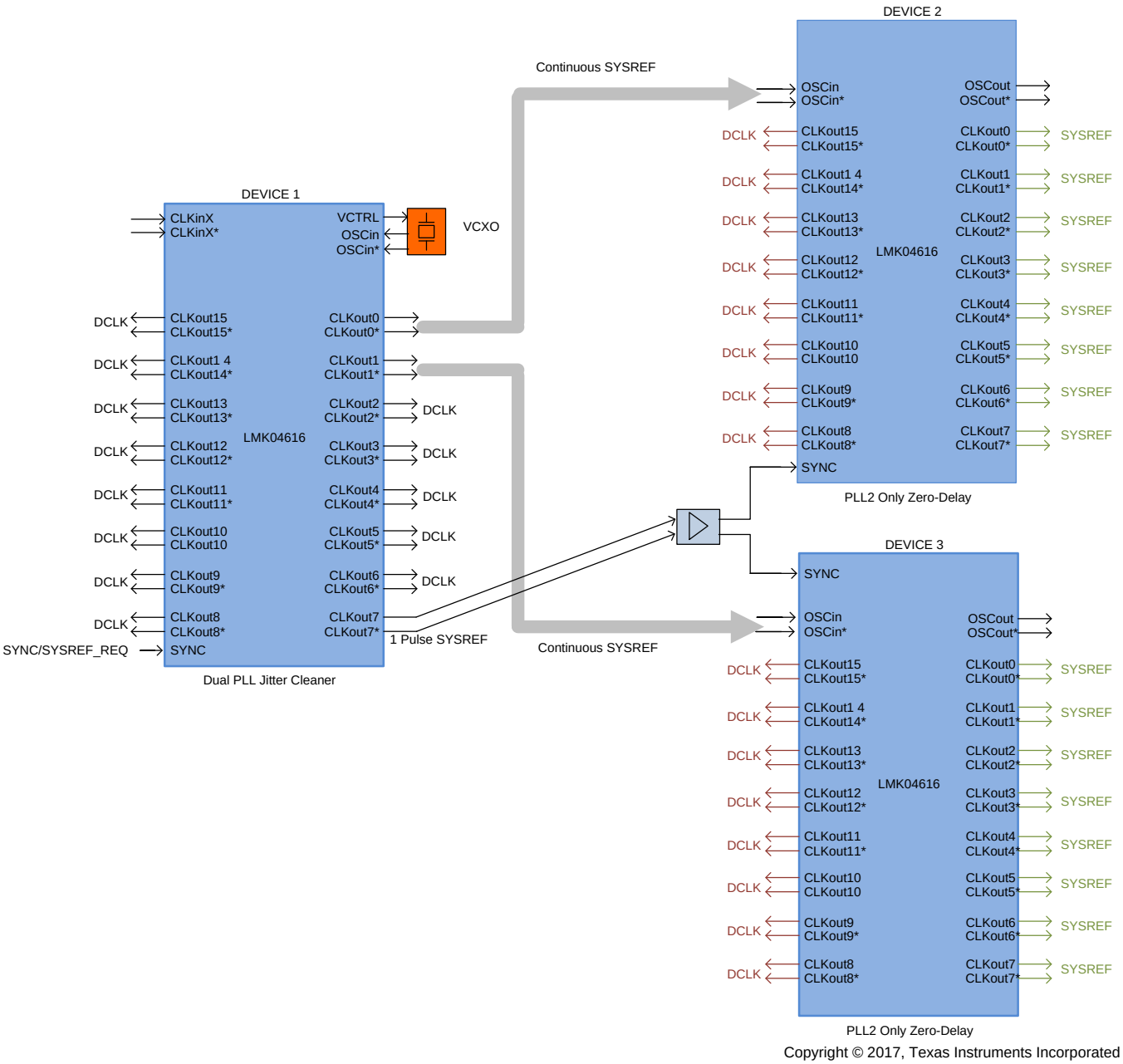

Figure 23. LMK0461x Device Configuration 4

Like in Configuration 3, the Device-1 is the master device and configured in Jitter cleaner mode to clean the dirty reference clock input. The Slave devices Device-2 and Device-3 are in the PLL2 only low skew mode. The difference from the Configuration 3 is that the slave devices generates the SYSREF and Device clock pairs instead of generating SYSREF clocks only. The topology can be further extended by using additional LMK0461x devices as shown in Figure 24.

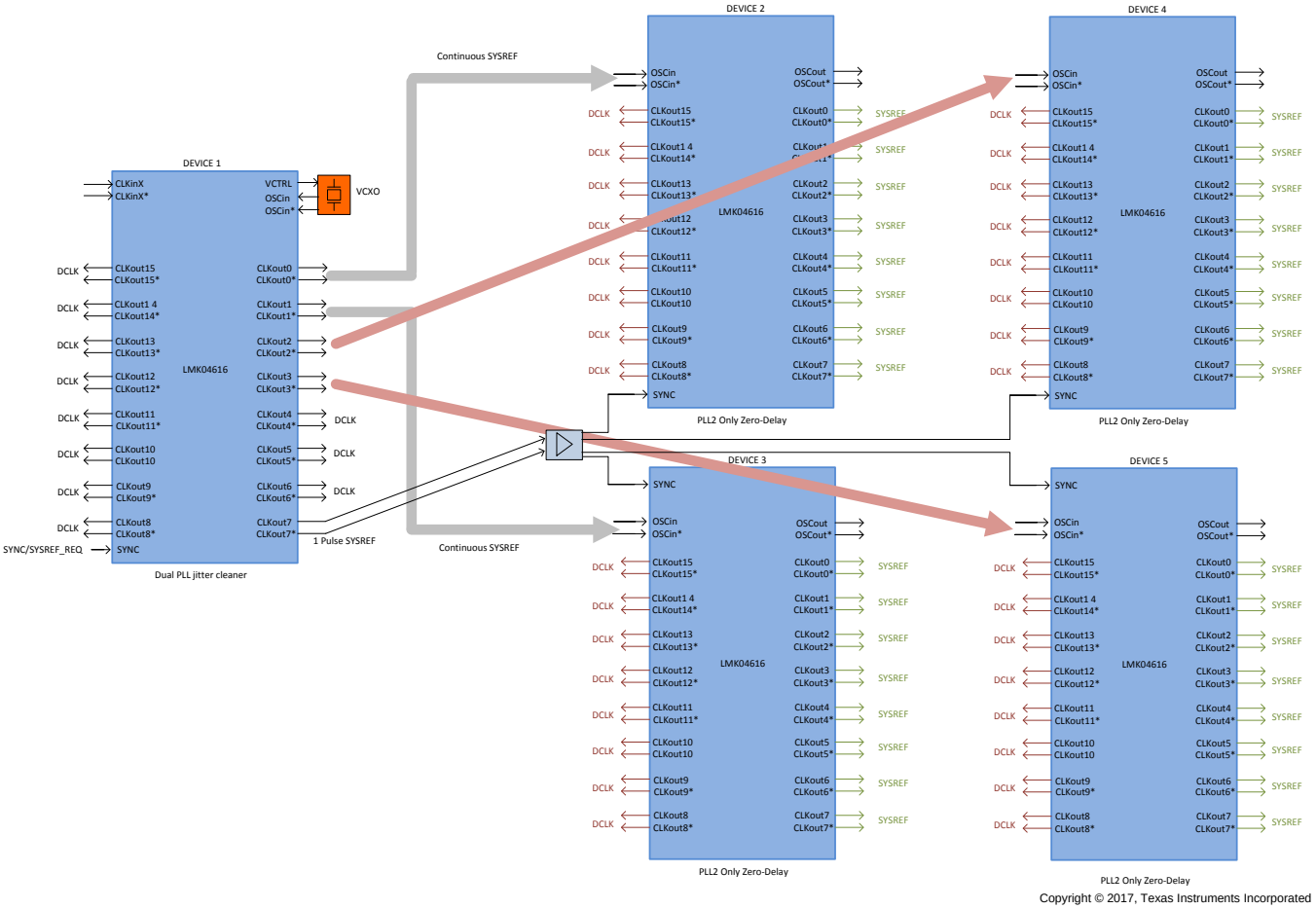

Figure 24. LMK0461x Device Configuration 4A

6.7 Configuration 5

Another possible configuration not requiring a synchronous SYNC/SYSREF_REQ is shown in Figure 25.

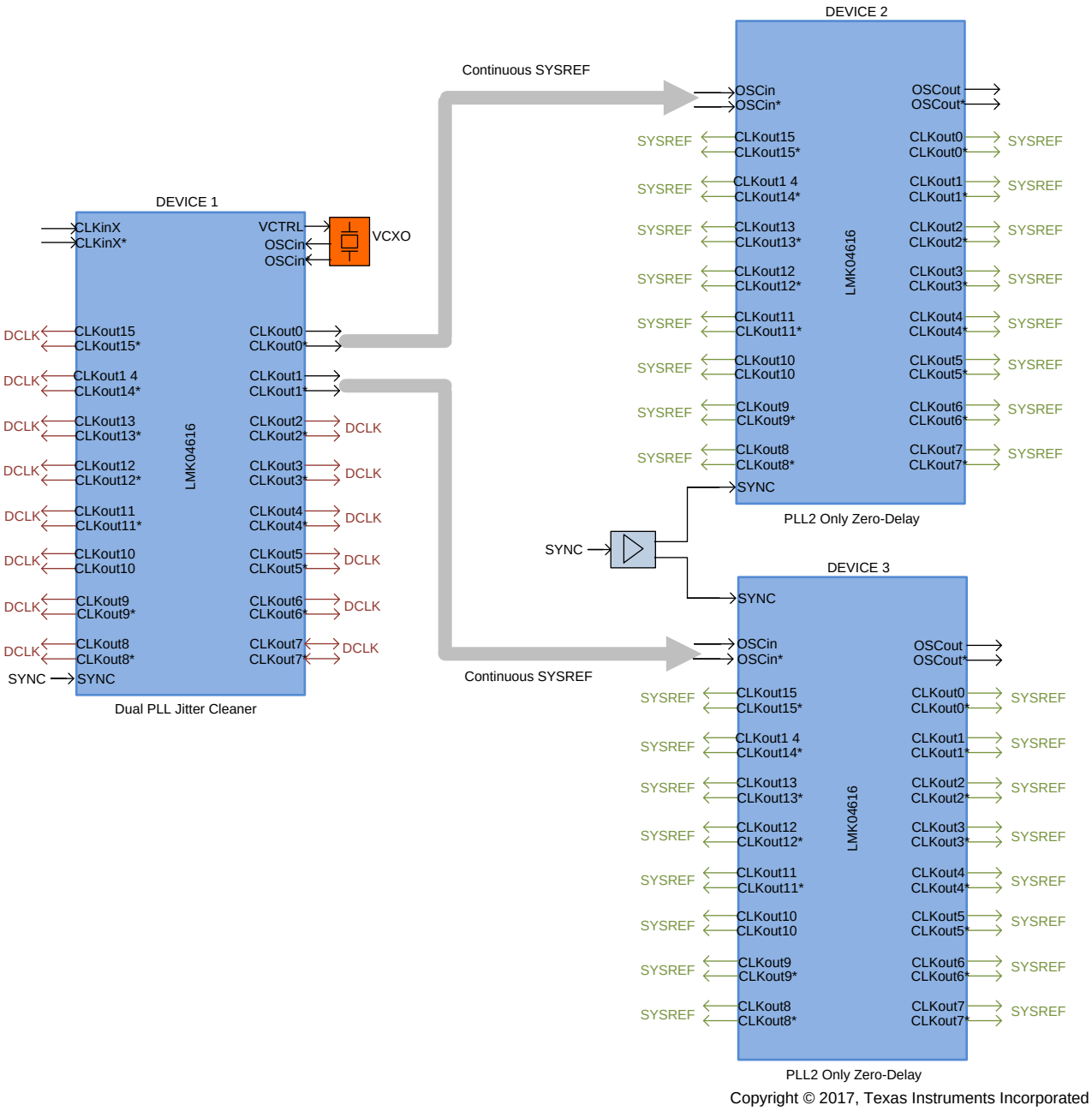

Figure 25. LMK0461x Device Configuration 5

This configuration is similar to Configuration 3 with the difference being that the SYNC/SYSREF_REQ is not coming from the Device-1 synchronous to the clock, but is asynchronously applied to the two slave devices. If the SYSREF clock from the slave devices is continuous SYSREF, then there is no difference in Configuration 3 and Configuration 5 in terms of SYSREFs timing from the two slave devices. But the difference comes while using the pulsed SYSREF. If SYSREF is used in Pulsed mode from the slave devices, then from the SYSREF_REQ edge to the rising edge of the SYSREF at the output of the two salve deices might differ by one SYSREF cycle. All SYSREF clocks coming out of the single devices are aligned to each other. The difference comes only while looking at the SYSREF coming out of Device-2 to Device-3. This is shown in Figure 26.

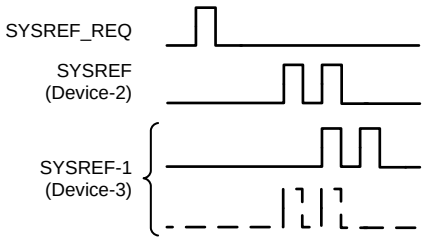

Figure 26. Waveforms for Configuration 5

SYSREF from one of the device can look like SYSREF-1 (Device-3) solid line or the dotted line although the edges relative to each other remains aligned.

7 Summary of Configurations

Table 1. Summary of Configurations

CONFIGURATION	NUMBER OF CLOCKS	WHEN TO USE	CAREABOUTS
Single LMK0461x configuration	8-SYSREF & DCLK clock pairs	-When all Device clocks and SYSREF clocks can be generated from Single device. -LMK04616 can provide 16 outputs and LMK04610 provides 10 outputs	Outputs/Output skew Only
Configuration 1A	16 DCLK & 14 SYSREF	-When all the device clocks and SYSREF clock needs can be fulfilled by two LMK0461x devices. -Asynchronous SYSREF request can be used	PLL2 in both device is in similar configuration getting the clock input from the VCXO, but from VCXO to Device 2, there is additional OSCin to OSCout path.
Configuration 1B	DCLK ≥ 16, SYSREF ≤ 14	-Required number of Device clocks are more than the SYSREF clocks, Some of the device clocks can be generated by second device. -Asynchronous SYSREF request can be used	Device clocks from Device-2 are aligned to SYSREFs because both come from same device, but from DCLK from Device 1 to SYSREF from device-2 has additional path as explained in Configuration 1A
Configuration 1C	16 DCLK & 14 SYSREF	- When all the device clocks and SYSREF clock needs can be fulfilled by two LMK0461x devices. -Path from VCXO to outputs from two devices is matched. -Asynchronous SYSREF request can be used	Additional buffer needed
Configuration 2	14 DCLK-SYSREF pairs+16 DCLK	-All required DCLKs and SYSREF can be generated by using 3	There is a symmetrical path from clock inputs to the outputs of Device-2 & 3. DCLK from Device-2 compared to DCLK from Device 1 have additional TPD variation from Device-2.
Configuration 3	14 DCLK & 32 SYSREF (SYSREF Fanout)	-Suitable when two or more LMK461x are needed for SYSREF generation. -Configuration expandable by adding more devices	-SYSREF_REQ should be synchronous to the Clock input for Device-2 & Device 3 which can be generated from Device-1 SYSREF output operated in 1 pulse mode

Table 1. Summary of Configurations (continued)

CONFIGURATION	NUMBER OF CLOCKS	WHEN TO USE	CAREABOUTS
Configuration 4	16 SYSREF-DCLK pairs+14 DCLK	-Multiple devices to generate SYSREF pairs triggered by one master -Configuration expandable by adding more devices	-SYSREF_REQ should be synchronous to the Clock input for the downstream devices -DCLK in-band phase noise performance little worse from the downstream devices compared to DCLK from Device-1
Configuration 5	14 DCLK & 32 SYSREF (SYSREF Fanout)	-Multiple devices to generate SYSREFs -Asynchronous SYSREF_REQ for the downstream Devices -Expandable by adding more devices	-When Pulsed mode SYSREF is used, there is one SYSREF cycle uncertainty for the start of first pulse and the last pulse

8 Measurement Results

8.1 Measurement Procedure

Two or three EVMs of the LMK0461x devices are used in the configurations explained earlier. The Device-1 is LMK04616EVM and Device-2 and Device-3 are LMK04610. The following measurement procedure is applied in a loop to one of the LMK04610 EVM for at least one overnight. Fixed delay offset between the outputs from different devices is one time calibrated out using analog/digital delays. The waveform plots are taken in persistence mode.

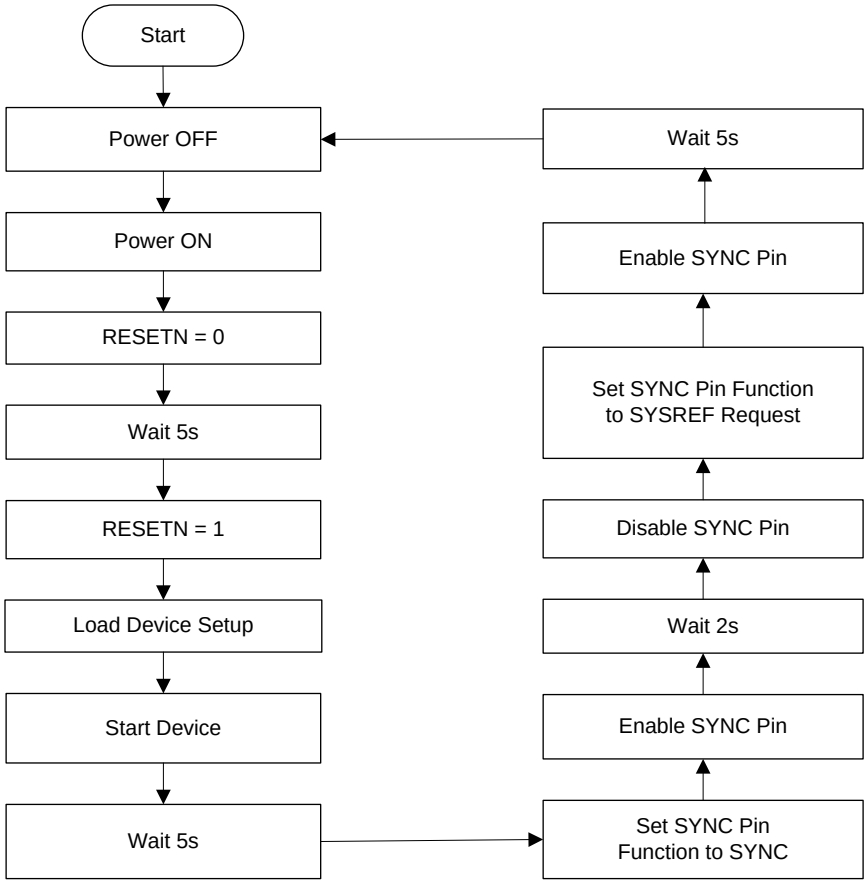

Figure 27. Measurement Procedure

8.2 Measurement Results - Configuration 1B

Two LMK0461x EVMs are used for this test. Referring to Figure 19, the devices configured are:

Device 1 - LMK04616EVM

Device 2- LMK04610EVM

The PLL2 in both devices are configured in Zero delay mode. The power cycle shown in Figure 27 is applied to the Device-2. An asynchronous SYSREF_REQ is applied to the Device-2 SYNC pin. The scope is triggered with the SYSREF rising edge coming out from Device-2. The waveform snapshot is shown in Figure 28.

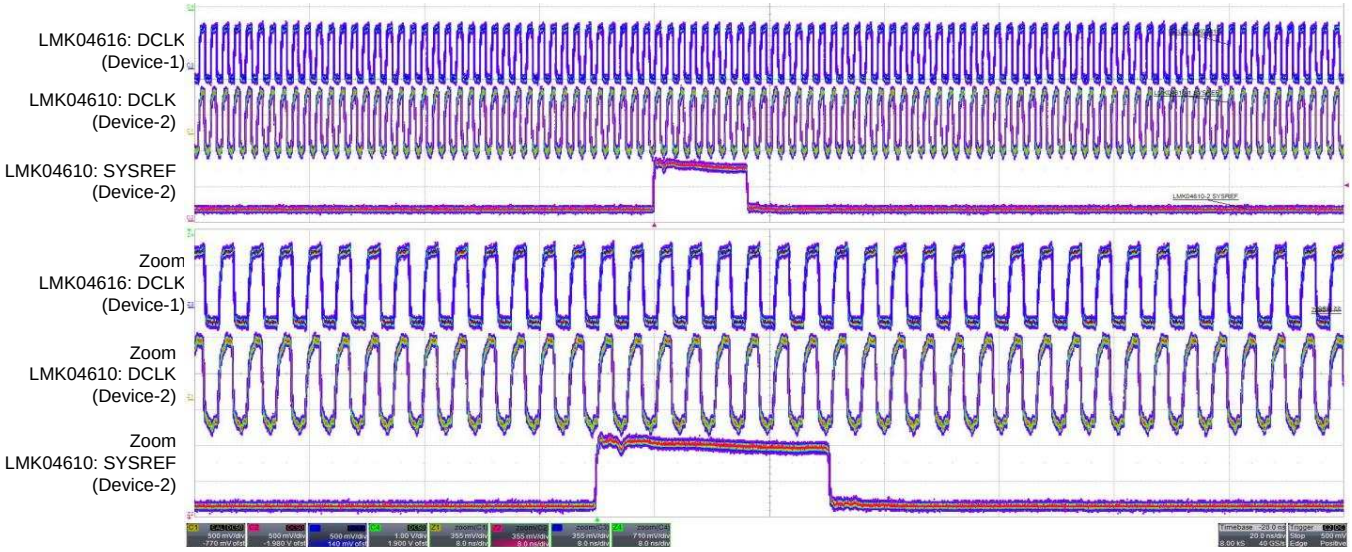

Figure 28. Configuration 1B Measurement

8.3 Measurement Results - Configuration 2

As shown in Figure 21, three LMK0461x EVMs are used for this configuration test.

Device-1 - LMK04616EVM

Device-2 - LMK04610EVM

Device-3 - LMK04610EVM

The Device-1 is in dual-loop jitter cleaner mode and Device-2 and 3 are in PLL2-only zero delay mode. Both Device-2 and Device-3 locks to the clock coming out of Device-1 and an asynchronous SYSREF request is applied though a buffer. Device-3 outputs are configured for 1 pulse SYSREF mode with SYNC pin as SYSREF request. The power cycle as shown in Figure 27 is applied to Device-3. The Scope is triggered with the rising edge of the SYSREF output in persistence mode. The scope shot is shown in Figure 29.

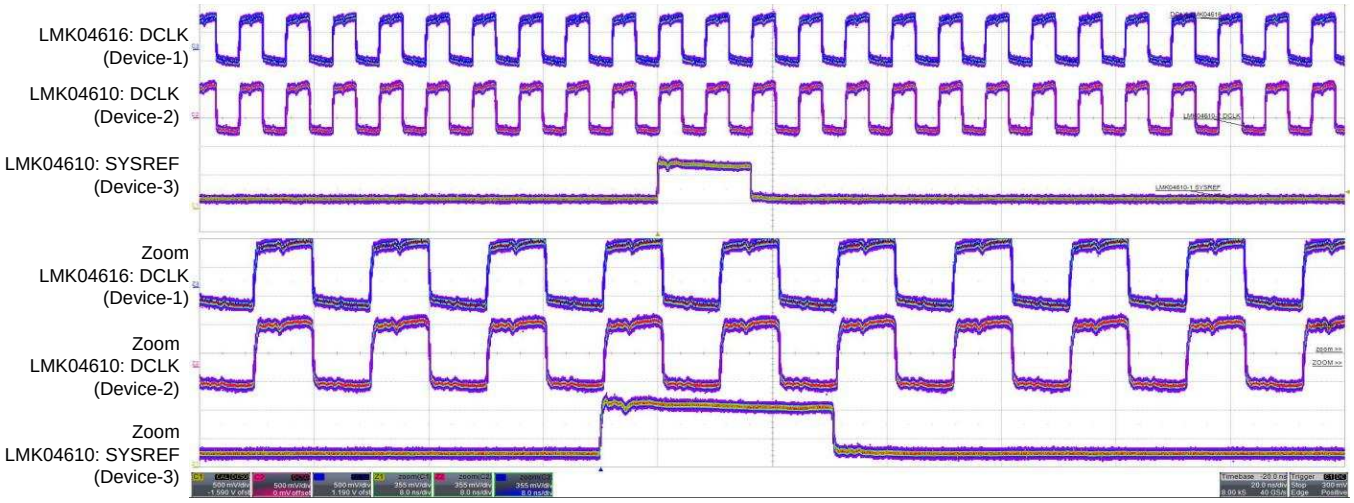

Figure 29. Configuration 2 Measurement

8.4 Measurement Results - Configuration 3

Referring to Figure 22, the three devices shown are configured like shown below:

Device-1 - LMK4616EVM

Device-2 - LMK04610EVM

Device-3 LMK04610EVM

Asynchronous SYSREF request is applied to the LMK04616 through SYNC pin. Power cycles as shown in Figure 27 are applied to Device-3. The persistence mode scope shot is shown in Figure 30. As can be seen, the SYSREF from the two LMK04610 devices are in SYNC with multiple power cycles and have deterministic phase relationship to the Device clock from the LMK04616 Master.

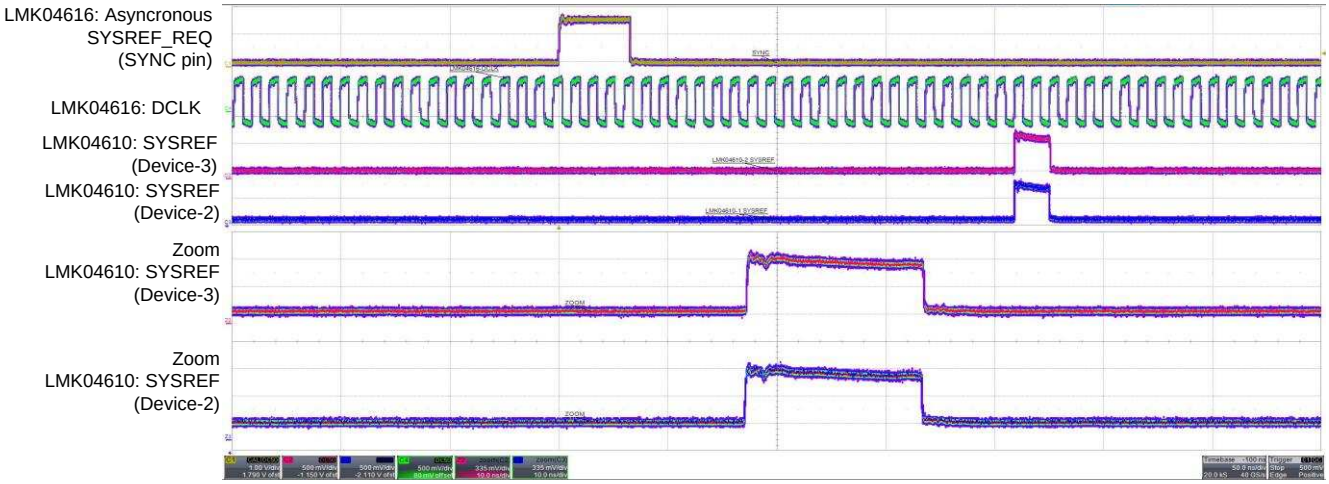

Figure 30. Configuration 3 Measurement

8.5 Measurement Results - Configuration 4

As shown in Figure 23, three LMK0461x EVMs are used in the following device configuration:

Device-1 - LMK4616EVM

Device-2 - LMK04610EVM

Device-3 LMK04610EVM

Device-2 and 3 locks to the continuous SYSREF clock coming from Device-1. Synchronous SYSREF request is applied to the Device-2 and Device-3 though a differential to single ended buffer. The two downstream devices generates SYSREF clock and Device clocks in pairs. The measurement waveform is shown in Figure 31.

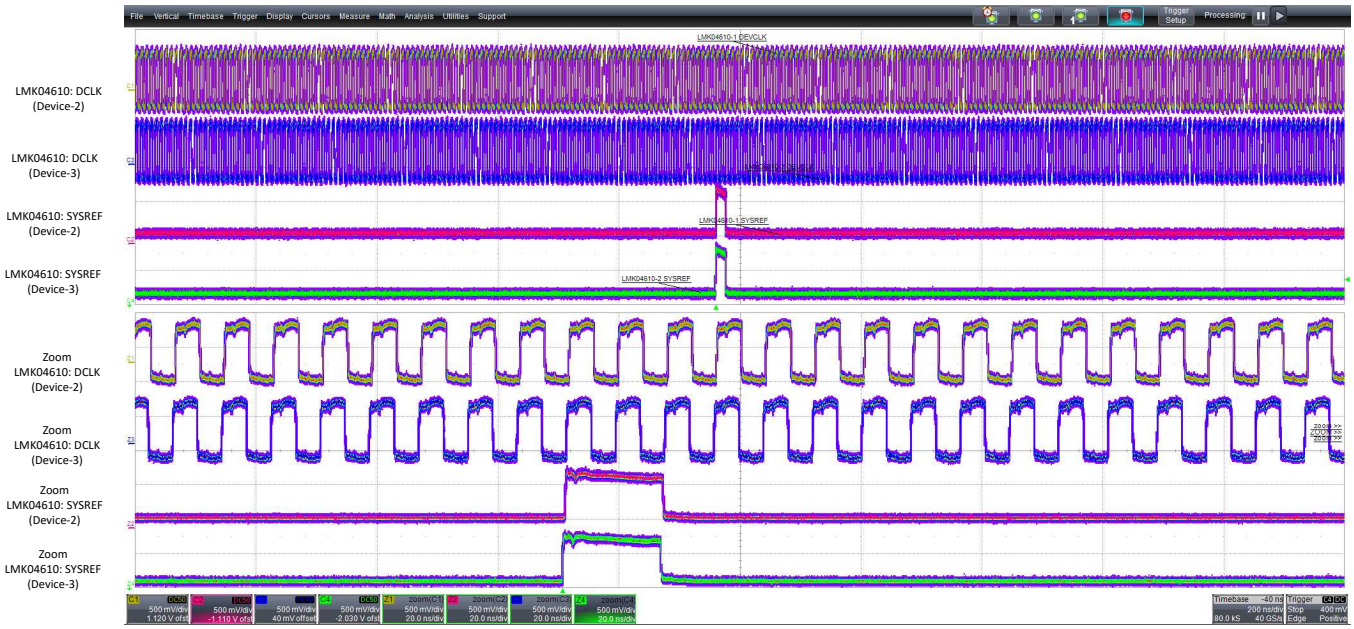

Figure 31. Configuration 4 Measurement

8.6 Measurement Results - Configuration 5

In this configuration, the two slave devices lock to the SYSREF from Master. The SYSREF request to the slave LMK04610s is applied with a matched path. To ensure that the SYSREF_REQ comes to the two slave device at the same point in time, a buffer is inserted in the SYSREF_REQ path. For this test configuration, the SYSREF request is sent to the input of the buffer asynchronously interval.

As explained in Section 6.7, The SYSREF generated from the slave devices are phase aligned, but when used in pulsed mode, the start of the first pulse might happen with 1-SYSREF cycle difference. The measurement snapshot in persistence mode is shown in Figure 32.

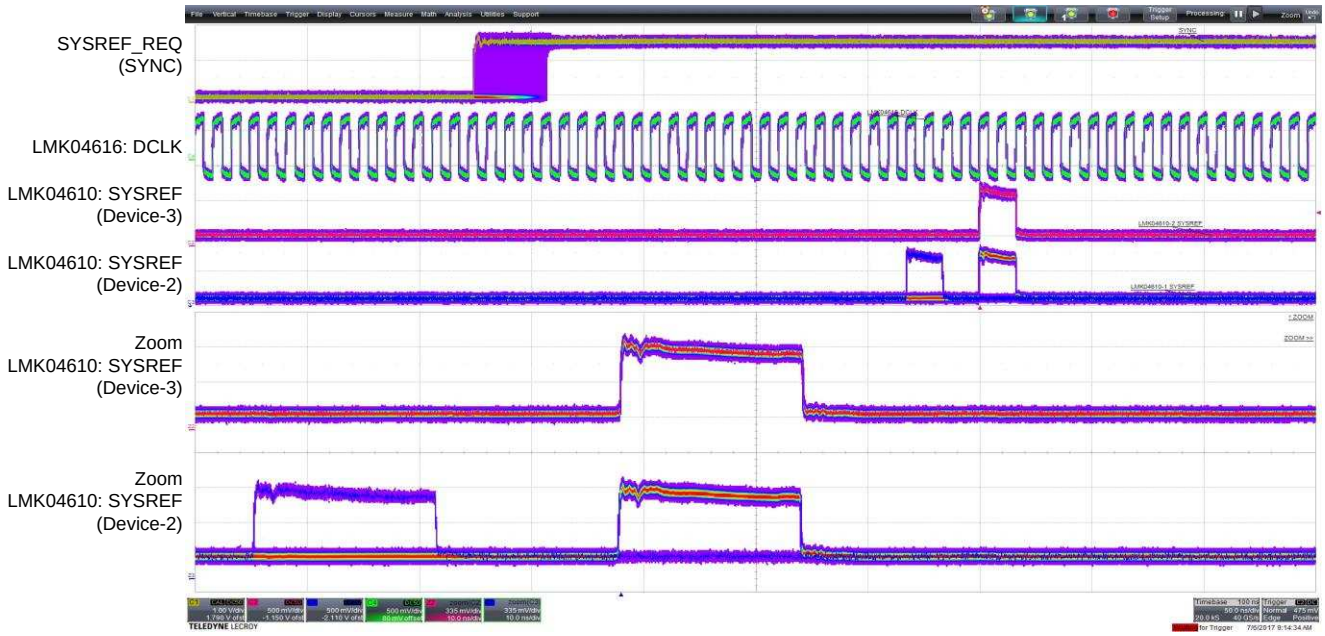

Figure 32. Configuration 5 Measurement

9 References

1. *JESD204B Overview* (SLAP161)
2. *When is the JESD204B interface the right choice?* (SLYT559)
3. *JESD204B multi-device synchronization: Breaking down the requirements* (SLYT628)
4. *Understanding JESD204B Subclasses and Deterministic Latency* (SNAU140)
5. *Ready to make the jump to JESD204B?* (SLYY057)

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