# **Engineering Manual**

for the

# Sun-2/120 Backplane

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# **Revision History**

| Revision | Date              | Comments  |
|----------|-------------------|---|
| 50       | 28 September 1984 | First release of this Theory of Operation Manual. |
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## **Contents**

| Chapter 1 Backplane             | 1-1 |
|---------------------------------|-----|
| Appendix A Backplane Schematics | A-1 |

## **Contents**

| Chapter 1 Backplane                    | 1_1 |
|--|-----|
| 1.1. Overview                          |     |
| 1.2. P1 Section — Levels of Compliance |     |
| 1.3. The P2 Section                    |     |
| 1.3.1. 120 Backplane Configuration     | 1-3 |
| 1.3.2. 170 Backplane Configuration     | 1-4 |
| 1.4. P1 and P2 Signal List             | 1-5 |
| 1.4. P1 and P2 Signal List             | 1-5 |
| Appendix A Backplane Schematics        | A-  |

## **Tables**

| Table 1-1 | Multibus Compliance                 | 1-1 |
|-----------|-------------------------------------|-----|
|           | Pin Assignments on the P1 Connector |     |
| Table 1-3 | Pin Assignments on the P2 Connector | 1-7 |

# **Figures**

| Figure 1-1 9-Slot Backplane  | 1-3 |
|------------------------------|-----|
| Figure 1-2 15-Slot Backplane | 1-4 |

### **Preface**

### Purpose and Audience

The purpose of this manual is to enable Sun customers and licensors of the Sun Workstation design to understand how the backplane is used. Licensors of the Sun Workstation design should use this manual to aid them in modifying the backplane.

#### **Summary of Contents**

This manual describes the Sun-2/120' and Sun-2/170' backplanes. It details the level of compliance with the IEEE-796 Multibus specification for the P1 bus. This manual also describes the P2 configurations for both the 120 (nine-slot) and 170 (15-slot) models. Also included is a description of the pin assignments on the P1 and P2 connectors.

At the end of this manual, we have supplied a reader comment form. Please use the comment form to list errors and omissions. Your responses will help a great deal in our efforts to keep our documentation up to date.

#### **Notations Used In This Manual**

When possible, the schematics were drawn to standard drafting conventions. Signal flow is shown from left to right, and top to bottom. Connected sections of the design are logically grouped together, as much as the available space allows.

Conventions used for hardware signal names in this manual are:

- Both active-high and active-low signals are used. A signal name that is followed by a minus sign (-) indicates that the signal is active LOW (<0.4V). For example, the Column Address Strobe, M.CASO-, is such a low-active signal.
- A signal that is *not* followed by a minus sign is understood to be a HIGH active signal (>2.0V). An example of such a signal would be the parity error signal, PARERR.
- For signals with multiple meanings or synonyms, the signal names are listed as separated by a slash (/). An example of this would be the on-board, memory expansion select signal, PM.OB-/P2. A high signal is understood to be an assertion of the P2 bus, while a low signal is an assertion of on-board status.
- Bus signals are indicated by a common prefix followed by a number. For example, a 16-bit data bus might be labelled D0, D1, D2, and so on until D15.
- A group of signals that is part of a signal vector is denoted by a common prefix separated from its suffix by a period. For example, all P1 signals start with the prefix "P1.", and P1 bus address signals are P1.A00, P1.A01, etc.

• Connector signals are distinguished by a suffix of "[]" with an optional string enclosed inside the square brackets identifying the connector name.

#### **Components**

Components in the schematics are identified by *component name* (this is also referred to as the "body name" in the wirelist). Components are named according to their generic or industry standard names. The way the components are drawn reflects their circuit function rather than the manufacturer's definition.

Each component carries a *location label* identifying its component type and approximate location in the schematics. Location labels consist of a letter followed by three digits. For instance, U300 is a DIP positioned on page three of the schematics.

The letter stands for the type of component, and is one of the following:

| Letter | Component Type           |  |  |  |
|--------|--------------------------|--|--|--|
| С      | Standard Capacitor       |  |  |  |
| D      | Diode                    |  |  |  |
| K      | Electrolytic Capacitor   |  |  |  |
| L      | Inductor                 |  |  |  |
| X      | Decoupling Capacitor     |  |  |  |
| J      | Jumper or Connector      |  |  |  |
| R      | Resistor                 |  |  |  |
| S      | Single-in-Line Component |  |  |  |
| U      | Dual-in-Line Component   |  |  |  |
| PL     | Programmable Logic Array |  |  |  |

Programmable logic components, such as PALs and PROMs, are described in a high-level functional language from which they are translated automatically into the bit patterns for programming. Programmable logic elements are identified by name.

### Chapter 1

### Backplane

#### 1.1. Overview

This manual describes the Sun 120' and 170' backplanes. The main features of the backplanes are:

- IEEE-796 bus standard compatible
- Arbitration using the parallel priority technique
- 20-bit address
- 8- or 16-bit data bus
- 9 slots on the 120 backplane
- 15 slots on the 170 backplane

The reader should have copies of the IEEE-796 bus specification, 120 backplane schematics, and the 170 backplane schematics.

### 1.2. P1 Section — Levels of Compliance

The P1 section of the Multibus complies to the IEEE-796 specification as follows:

Table 1-1: Multibus Compliance

| Data Path            | D16 | 8 or 16-bit data path               |
|----------------------|-----|-------------------------------------|
| Memory Address Path  | M20 | 20-bit memory address path          |
| I/O Address Path     | I16 | 8 or 16-bit I/O address path        |
| Interrupt Attributes | V0  | Non-bus-vectored interrupt requests |

A parallel priority bus arbitration technique is used on both backplanes. Priorities on the 9-slot backplane are slot C9 highest, and slot C1 lowest. Priorities on the 15-slot backplane are slot C1 highest, and slot C15 lowest.

The following are deviations from the IEEE-796 specification. The first three deviations are due to the CPU in the Sun-2/120 and Sun-2/170.

- 1) INIT- pulse length during a reset instruction (non-power-up reset) will not meet the five-millisecond minimum. It will be 12.4 microseconds (usec).
- 2) INT0- through INT7- are reversed in priority as per the 68010. INT0- is not used and INT7- is the highest priority.

- 3) The LOCK function is not implemented.
- 4) The pullups on CBRQ— and BUSY— have been reduced to 320 ohms (1K in parallel with 470 ohms) so that these signals will be pulled up within 100 nsec (max bus clock of 10 MHz).

### 1.3. The P2 Section

The P2 section of the backplane is configured differently for the nine-slot (120) and 15-slot (170) backplanes.

### 1.3.1. 120 Backplane Configuration

All nine P1 slots are connected together and the P2 slots are connected as shown in Figure 1-1:

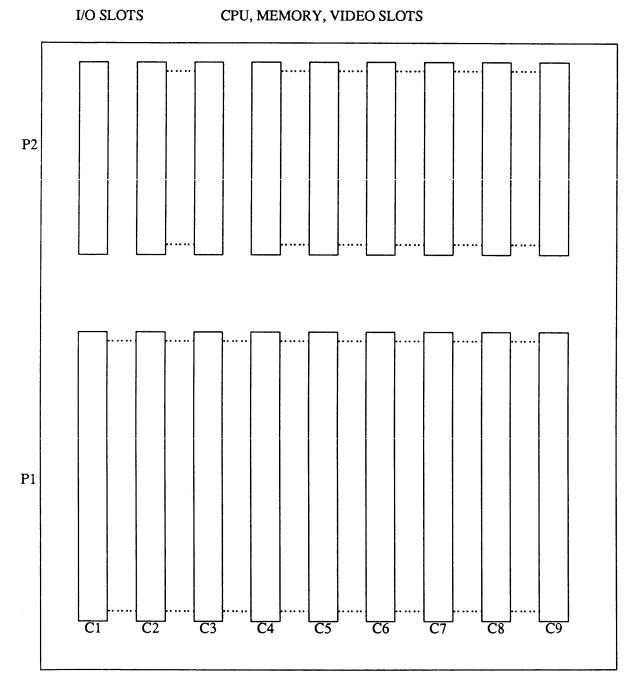


Figure 1-1: 9-Slot Backplane

### 1.3.2. 170 Backplane Configuration

All fifteen P1 slots are connected together and the P2 slots are connected as shown in Figure 1-2:

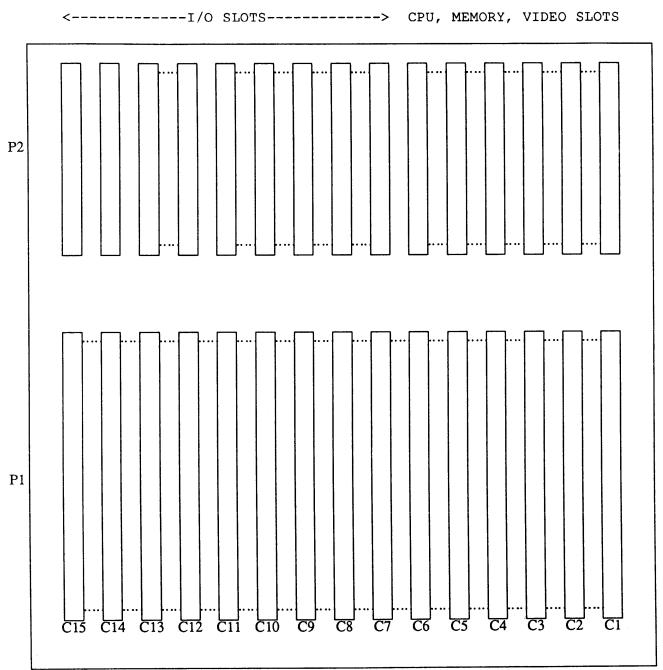


Figure 1-2: 15-Slot Backplane

### 1.4. P1 and P2 Signal List

The P1 slots (120 and 170) have the following pin assignments:

Table 1-2: Pin Assignments on the P1 Connector

|            | ρ.  | n   Component Side<br>  Mnemonic   Description |                    | Pin |          | Circuit Side            |  |
|------------|-----|--|--------------------|-----|----------|-------------------------|--|
|            | Pin |  |                    | Pin | Mnemonic | Description             |  |
| Power      | 1   | GND  | Signal GND         | 2   | GND      | Signal GND              |  |
| Supplies   | 3   | +5V  | +5Vdc              | 4   | +5v      | +5Vdc                   |  |
|            | 5   | +5V  | +5Vdc              | 6   | +5V      | +5Vdc                   |  |
|            | 7   | +12V   | +12Vdc             | 8   | +12V     | +12Vdc                  |  |
|            | 9   | -5V  | -5Vdc              | 10  | -5V      | -5V dc                  |  |
|            | 11  | GND  | Signal GND         | 12  | GND      | Signal GND              |  |
| Bus        | 13  | BCLK-  | Bus Clock          | 14  | INIT-    | Initialize              |  |
| Controls   | 15  | BPRN-  | Bus Pri. In        | 16  | BPRO-    | Bus Pri. Out            |  |
|            | 17  | BUSY-  | Bus Busy           | 18  | BREQ-    | Bus Request             |  |
|            | 19  | MRDC-  | Mem Read Cmd       | 20  | MWTC-    | Mem Write Cmd           |  |
|            | 21  | IORC-  | I/O Read Cmd       | 22  | IOWC-    | I/O Write Cmd           |  |
|            | 23  | XACK-  | XFER Acknowledge   | 24  | INH1-    | Inhibit 1 (disable RAM) |  |
| Bus        | 25  | LOCK-  | Lock               | 26  | INH2-    | Inhibit 2 (disable PROM |  |
| Controls   | 27  | BHEN-  | Byte High Enable   | 28  | AD10-    | or ROM)                 |  |
| and        | 29  | CBRQ-  | Common Bus Request | 30  | AD11-    | Address                 |  |
| Address    | 31  | CCLK-  | Constant Clk       | 32  | AD12-    | Bus                     |  |
|            | 33  | INTA-  | Intr Acknowledge   | 34  | AD13-    |                         |  |
| Interrupts | 35  | INT6   | Parallel           | 36  | INT7-    | Parallel                |  |
|            | 37  | INT4-  | Interrupt          | 38  | INT5-    | Interrupt               |  |
|            | 39  | INT2-  | Requests           | 40  | INT3-    | Requests                |  |
|            | 41  | INTO-  |                    | 42  | INT1     |                         |  |
| Address    | 43  | ADRE-  |                    | 44  | ADRF-    |                         |  |
|            | 45  | ADRC-  |                    | 46  | ADRD-    |                         |  |
|            | 47  | ADRA-  | Address            | 48  | ADRB-    | Address                 |  |
|            | 49  | ADR8-  | Bus                | 50  | ADR9-    | Bus                     |  |
|            | 51  | ADR6-  |                    | 52  | ADR7-    |                         |  |
|            | 53  | ADR4-  |                    | 54  | ADR5-    |                         |  |
|            | 55  | ADR2-  |                    | 56  | ADR3-    |                         |  |
|            | 57  | ADR0-  |                    | 58  | ADR1-    |                         |  |
| Data       | 59  | DATE-  |                    | 60  | DATF-    |                         |  |
|            | 61  | DATC-  |                    | 62  | DATD-    | _                       |  |
| ]          | 63  | DATA-  | Data               | 64  | DATB-    | Data                    |  |
|            | 65  | DAT8-  | Bus                | 66  | DAT9     | Bus                     |  |
| 1          | 67  | DAT6   |                    | 68  | DAT7-    |                         |  |
|            | 69  | DAT4-  |                    | 70  | DAT5-    |                         |  |
|            | 71  | DAT2-  |                    | 72  | DAT3-    |                         |  |
|            | 73  | DAT0-  |                    | 74  | DAT1-    |                         |  |
| Power      | 75  | GND  | Signal GND         | 76  | GND      | Signal GND              |  |
| Supplies   | 77  |  | Reserved, bussed   | 78  |          | Reserved, bussed        |  |
|            | 79  | -12V   | -12Vdc             | 80  | -12V     | -12Vdc                  |  |
|            | 81  | +5V  | +5Vdc              | 82  | +5V      | +5Vdc                   |  |
|            | 83  | +5V  | +5Vdc              | 84  | +5V      | +5Vdc                   |  |
|            | 85  | GND  | Signal GND         | 86  | GND      | Signal GND              |  |

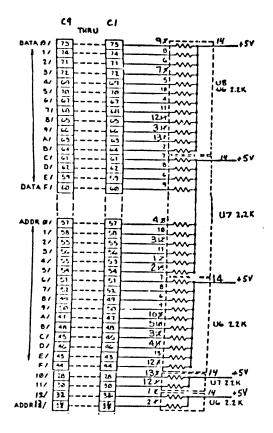
The CPU, Memory, and Video board P2 slots (C4:9 for the 120, C1:6 for the 170) have the following pin assignments:

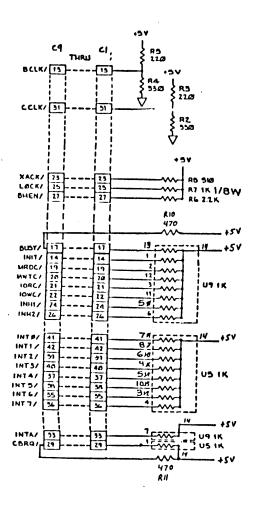
Table 1-3: Pin Assignments on the P2 Connector

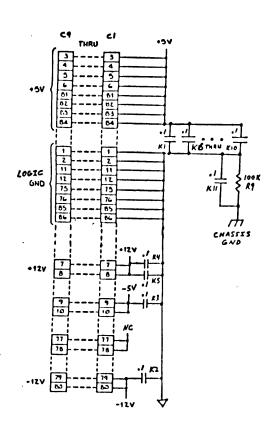
| Pin Component Side |          | omponent Side          | D:  | Circuit Side |                           |  |
|--------------------|----------|------------------------|-----|--------------|---------------------------|--|
| Pin                | Mnemonic | Description            | Pin | Mnemonic     | Description               |  |
| 1                  | A09      | Address bit 9          | 2   | A18          | Address bit 18            |  |
| 3                  | A19      | Address bit 19         | 4   | A20          | Address bit 20            |  |
| 5                  | CAS-     | Column Address Strobe  | 6   | RAS-         | Row Address Strobe        |  |
| 7                  | WAIT-    | DTACK WAIT signal      | 8   | WEL-         | Write Enable — lower byte |  |
| 9                  | DI00     | Data In 0              | 10  | DO00         | Data Out 0                |  |
| 11                 | DI01     | Data In bit 1          | 12  | DO01         | Data Out bit 1            |  |
| 13                 | A01      | Address bit 1          | 14  | A21          | Address bit 21            |  |
| 15                 | DI02     | Data In bit 2          | 16  | DO02         | Data Out bit 2            |  |
| 17                 | D103     | Data In bit 3          | 18  | DO03         | Data Out bit 3            |  |
| 19                 | A02      | Address bit 2          | 20  | A22          | Address bit 22            |  |
| 21                 | DI04     | Data In bit 4          | 22  | DO04         | Data Out bit 4            |  |
| 23                 | DI05     | Data In bit 5          | 24  | DO05         | Data Out bit 5            |  |
| 25                 | A03      | Address bit 3          | 26  | REFR-        | Refresh                   |  |
| 27                 | DI06     | Data In bit 6          | 28  | DO06         | Data Out bit 6            |  |
| 29                 | DI07     | Data In bit 7          | 30  | DO07         | Data Out bit 7            |  |
| 31                 | A04      | Address bit 4          | 32  | GND          | Signal GND                |  |
| 33                 | DIL      | Parity In — lower byte | 34  | DOL          | Parity Out — lower byte   |  |
| 35                 | DIU      | Parity In — upper byte | 36  | DOU          | Parity Out — upper byte   |  |
| 37                 | A05      | Address bit 5          | 38  | GND          | Signal GND                |  |
| 39                 | DI08     | Data In bit 8          | 40  | DO08         | Data Out bit 8            |  |
| 41                 | DI09     | Data In bit 9          | 42  | DO09         | Data Out bit 9            |  |
| 43                 | A06      | Address bit 6          | 44  | GND          | Signal GND                |  |
| 45                 | DI10     | Data In bit 10         | 46  | DO10         | Data Out bit 10           |  |
| 47                 | DI11     | Data In bit 11         | 48  | DO11         | Data Out bit 11           |  |
| 49                 | A07      | Address bit 7          | 50  | R/W-         | Read — high, Write — low  |  |
| 51                 | DI12     | Data In bit 12         | 52  | DO12         | Data Out bit 12           |  |
| 53                 | Di13     | Data In bit 13         | 54  | DO13         | Data Out bit 13           |  |
| 55                 | 80A      | Address bit 8          | 56  | WEU-         | Write Enable — upper byte |  |
| 57                 | DI14     | Data In bit 14         | 58  | DO14         | Data Out bit 14           |  |
| 59                 | DI15     | Data In bit 15         | 60  | DO15         | Data Out bit 15           |  |

## Appendix A

## **Backplane Schematics**







| P1 MULTIBUS CONNECTIONS - 9 SLOT |              |           |  |  |
|----------------------------------|--------------|-----------|--|--|
| K. 81234K                        | Suly 11,1984 | 141 1 6 3 |  |  |
| <del></del>                      |              |           |  |  |

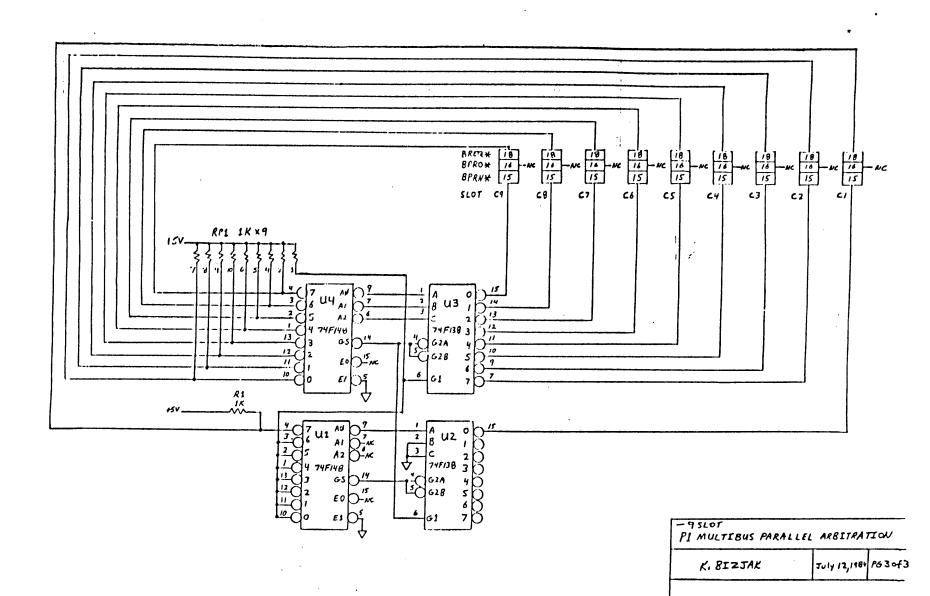
| 1  | (2.  | C3          |   |
|--|------|-------------|---|
| 3  |      | <u> </u>    |   |
| 4  |      | <b>ゴ</b> き  |   |
| 0  | 1    | 그礻          |   |
| 0  | 3    | - 3         |   |
| 0  | 15   | -  •        |   |
| 30   | 6    | 二 ;;        |   |
| 30   | 9    | <b>_</b> ↓• |   |
| 30   | 10   | <u></u>     |   |
| 30   | ::   | ᆉᆢ          | - |
| 30   | 13   | 口片          | • |
| 30   | 14   | 114         |   |
| 30   | 15   | - 15        |   |
| 30   | 15   | 7!5         |   |
| 30   | 10   | ]治          |   |
| 30   | 19   | 119         | I |
| 30   | 10   | 20          |   |
| 30   | 127  | 771         | ı |
| 30   | 13   | 725         |   |
| 30   | 74   | - 24        | ŀ |
| 30   | 25   | 75          | ı |
| 30   | 1/2  | 14          |   |
| 30   | 20   | 7 2/3       |   |
| 34 34 34 35 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36                               | 27)  | 19          |   |
| 34 34 34 35 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36                               | 30   | - [33]      |   |
| 34 34 34 35 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36                               | 31   | 크레          |   |
| 34 34 34 35 35 35 36 36 36 36 36 36 36 36 36 36 36 36 36                               | 33   | ];;;        |   |
| 10   10   10   10   10   10   10   10  | 34   | -1341       |   |
| 10   10   10   10   10   10   10   10  | 35   | 35          |   |
| 30   36   36   37   37   38   37   38   38   38   38                                   | 36   | 그는          |   |
| 40   41   42   43   44   44   44   44   44   44  | 30   | 134         |   |
| 41 41 41 42 44 44 44 45 45 45 55 55 55 55 55 55 55                                     | 39   | 39          |   |
| 44 44 44 44 44 44 44 44 44 44 44 44 44   |      | 40          |   |
| 44 45 45 45 45 45 45 45 45 45 45 45 45 4   | 141  | 14!         |   |
| 44 45 45 45 45 45 45 45 45 45 45 45 45 4   |      | 1::1        |   |
| 40 40 40 40 40 40 40 40 40 40 40 40 40 4   | 44   | 144         |   |
| 41   | 45   | 45          |   |
| 41   | 4    | 14          |   |
| 41   | 120  | 1::-        |   |
| 50 50<br>51 51<br>52 51<br>53 55<br>55 55<br>55 55<br>56 55<br>57 56                   | 41   | 44          |   |
| 51<br>52<br>53<br>53<br>53<br>53<br>53<br>53<br>53<br>53<br>53<br>53<br>53<br>53<br>53 | 50   | (50)        |   |
| Sh S   | 151  |             |   |
| Sh S   | 124  | ]끍          |   |
| 51 51 50   | 12   | 1           |   |
|  | [35] | 55          |   |
|  | 5    | 범           |   |
|  | 145  | [:          |   |
| [iv]   | 5.71 | 57          |   |
|  | [13] | 20          |   |

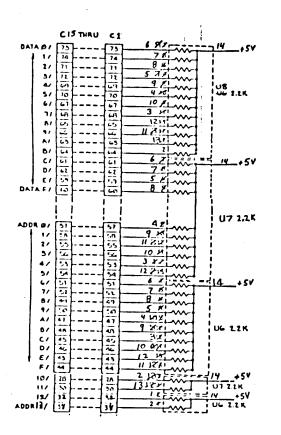
|                             | <b>C4</b>  | Y THR     | U C9     |
|-----------------------------|------------|-----------|----------|
| P2. A \$ 7                  |            | }         | [        |
| PL.A18                      | Ţ          | <b></b> - |          |
| P2.A19                      | 3          | -t:-      |          |
| P2.A20<br>P2.CASK           | 13         | Ţ         | -15      |
| P2.RASH                     | 6          | 1         | [6]      |
| P2.WATTK                    | 7          | }         | [7]      |
| PI.WELH                     | 0          | <b>}</b>  |          |
| P1.D100                     | 7          | t         | - 10     |
| P2.D0##<br>P2.D1#1          | 11         | []        | - 1 1111 |
| P2.00#1                     | 12         | 1         | -111     |
| 12. A Ø I                   | 13         | }         | [15]     |
| P2 . A21                    | 14         | }         | -14      |
| P2.DI <b>#2</b><br>P2.DO #2 | 15         | [·        | - 13     |
| 72.0002<br>71.01¢3          | 117        | [         | 16       |
| P2. D0 #3                   | 18         | <u> </u>  |          |
| P2. A62                     | 19         | 1         | 119      |
| P2. A22                     | 10         | ļ         | 10       |
| P2.D1#4                     | 21         | <b></b>   | - [21]   |
| P2.D0#4<br>P2.D1#5          | 11         | [         | 그품       |
| P2.0005                     | 24         | £         | 그음       |
| P2.AP3                      | 25         |           | 15       |
| p2.REFRX                    | 1          | }         | - 24     |
| P2 . DI #6                  | 27         |           | - 27     |
| P1. D0 \$6<br>P1. D1 \$7    | 20         | [         | 28       |
| P1.0107                     | 30         |           | 33       |
| P2.APY                      | 31         |           | - 35     |
| GNO                         | 51         |           | - 31     |
| PI.DIL                      | [55]       |           | - 35     |
| P1.DOL<br>P1.DIU            | 35         |           | 14       |
| Pr. DOU                     | 꽆          |           | 그        |
| PZ ABS                      | 37         |           | -5       |
| GND                         | 513        |           | 31       |
| P2.DI#8                     | 37         |           | 39       |
| P2.D0#8<br>P2.D1#9          | 40         |           | 12       |
| P2.D1#4                     | 7          |           | 1#       |
| P2. AP6                     | 43         |           | 13       |
| GND                         | 44         |           | -[44]    |
| P2.0E1#                     | 45         |           | 45]      |
| P1.001#                     | 4          |           | 44       |
| P2.DI11<br>P2.DOI1          | 3          |           | 급하       |
| P1.AP7                      | 411        |           | 49       |
| PI.R/WH                     | 5          |           | - 30     |
| P1 D212 [                   | 51         |           | 131      |
| P1.0012                     | 17         |           | 155      |
| F2 DOIS                     | 끍          |           | 그걸       |
| F2.A # B                    | <u></u>    |           | 155      |
| F2.WEUX                     | <u>:</u> - |           | 45       |
| F1.DLIV                     | 한          |           | 델        |
| F2.0014                     | 4          |           | 150      |
| P2.D115                     |            |           | 뜶        |
| 17.0013                     |            |           | ريسا     |

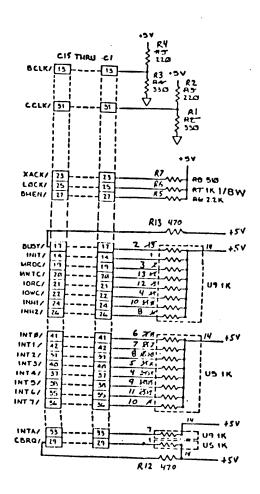
I/O P2 CONNECTOR SLOTS

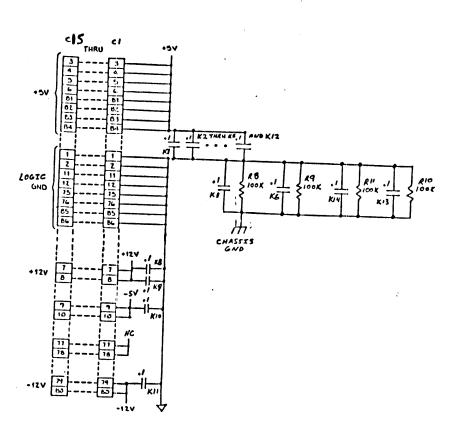
CPU, MEMORY, VIDEO PZ CONNECTOR SLOTS

|   | PZ MULTIBUS | CONNECTIONS . 9 SL. |
|---|-------------|---------------------|
| 1 | V STATAN    | TA 12 000 00 2 00 3 |









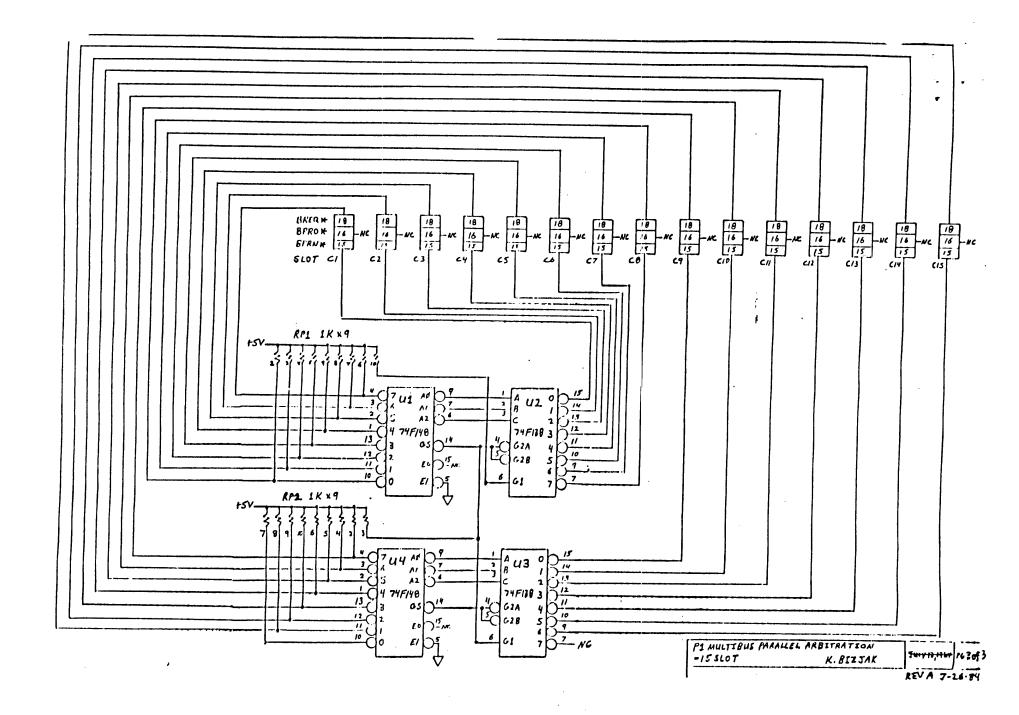
| P1 MULTIBUS CONNECTIONS - 15 SLOT |                            |         |
|-----------------------------------|----------------------------|---------|
| K.BIZSAK                          | E-1-12,457<br>(604 7-24-87 | 161 0 3 |

| C15   | СИ               | C13 C12                                      | C// THRU C7   |                               | C6 THRU    | Cl       |
|---|------------------|--|---|-------------------------------|------------|----------|
|   |                  |  | <u> </u>  | P2. A69                       | T          |          |
| 1 2   | [2]              |  | \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\  | P2.A18                        | <u> </u>   | 团        |
| 121   | 14               |  | 3 3   | P2.A19                        | [3]        | 3        |
| 3   | 151              | 3 3  | ) <del></del>   | P2 . A20                      | 1          | <b>3</b> |
| 5   | 1 2 3 4 5 6      | 6  | <u> </u>  | PZ. CASK<br>PZ. RASK          |            | 레        |
| 1   | 7                | 7  | [   | PT. WATER                     | 7          | 鬥        |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>7        | 17               | 7 7  |   | P1.WEL <del>X</del>           | <u> </u>   | 5        |
| 10  | 10               | 10 10  |   | 72.0100                       | 7          | 10       |
| 111   | 11               |  | h <del></del> 1   | P2.DE#1                       | hi         | 1        |
| 12  | 12               | 12 12  | \ <u>!\!</u> }\!\   | P1.00 #1                      | 12         | 12       |
|   | 13               |  | 122 [ 123 ]   | f2. AØI                       | 13         | 15       |
| 131   | 15               | 13 13 15 15 15 15 15 15 15 15 15 15 15 15 15 | P   | P2.A2 <br>P2.DI#2             | 13         | 14       |
| 10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0      | 16               | 16   | ]   | P2.00#2                       | 16         | 문        |
| 11  | 11               | [17][17]                                     | [1] }{11}   | 12. DI#3                      | 17         | 17       |
| 10  | 10               | 10 10  | 10 10   | P2. DO #3                     | 10         | 10.      |
|   | 123              | 10 10  |   | Γ1·A∱2<br>Γ2·A22              | 10         | 10       |
| <u>                                    </u> | 21               | 21 21  |   | 72.DI#4                       | 11         | 71       |
| 1 11 1                                      | $[\overline{n}]$ | [11] [11]                                    | 11 11   | P2. DO #4                     | 11         | 112      |
| 73<br>74<br>76                              | <u>ii</u>        | 25 25  | 25 25   | PI.DIES                       | 13         | 25       |
| 14  | 11               |  | 75 p.   | P1.DAAS<br>P1.AP3<br>P2.REFRX | 74         | 74       |
| 144   | 15               | 14   14                                      | $\begin{vmatrix} P_1 \\ \overline{P_2} \end{vmatrix} = \begin{vmatrix} P_1 \\ \overline{P_2} \end{vmatrix}$ | PZ.APJ<br>DZ.REBR¥            | 7          | 120      |
| 17<br>18                                    | 111              | $\overline{n}$                               | 1111  | P1.01/4                       | 11         | 17       |
| [in]  | 7.0              | // // // // // // // // // // // // //       | [A][IN]   | 12. DO 66                     | /ñ         | 2A       |
| 111   | in               | <u> </u>                                     | 19 [29]   | P2.D147                       | <u>n</u>   | 29       |
| 50  | · · ·            | 11 11  | 11 11   | ቦኔ ፡ ቦሳቶቸ<br>ቦኔ ፡ ለሶዣ         | 9          | 30       |
| 111   | 52               | 32    32                                     | 1 1 1 21  | GND                           | 51         | 51       |
| 35  | 133              | [35][35]                                     |   | PI.DIL                        | 33         | 23       |
| <u>  m</u>                                  | <u>  4   </u>    |  | <u>M</u> <u>M</u>   | 12.DOL                        | 34         | 54       |
|   | 2                | 35 35 V.                                     |   | rz.DIU<br>rz.paił             | 35         | 35       |
|   | 3.1              | 31 31  |   | PL-A#S                        | 31         | 37       |
| 71<br>28<br>31                              | 30<br>31         | 20 30  | 78 28   | BNP                           | 31         | 3A<br>31 |
| [37]  | [57]             | [32]   |   | P2.01#8                       | 37         |          |
| 1     | 10               | 10 10  | 41 41   | P2.00/8                       | 41         | 13       |
|   | [:]              | 11   |   | F1-D1#7<br>P1-D0#9            | 41         | 42       |
|   | [45]             | 1      | [3][3]  | 12. A16                       | 15         | 45       |
| <u></u>                                     | ₩<br>₩.          | 14 14 14 14 14 14 14 14 14 14 14 14 14 1     |   | GND                           | 44         | 44       |
| \$\frac{45}{44}\$<br>\$\frac{4}{6}\$        | <u>v.</u>        | 42   | 15 165  | PZ. DEIP                      | 45         | 45       |
| 141   | 41               |  | 1:-1 1:-1   | P2.DE11                       | A1         | 41       |
|   | 10               | 120  | 40  | P1. DOIL                      | in         | 111      |
| <u>  m</u>                                  | 9                | 1 <u>1</u>                                   | 111   | P3.AP7                        | 49         | 49       |
| 13  | 20               | 31 31  | [   | 12.8/WW                       |            | 761      |
| 21  | 51               | 51 51  |   | P3 - D 1 12                   | 51         | 51       |
| 4.812 51515 51516 4.5516 4.5516 555         | 黑                | [55][55]                                     |   | P2.0012<br>P2.0113            | \$2<br>\$4 | 53       |
| 54  |                  | ₩<br>55 <u>₩</u>                             | M   | F2. DOI3                      | 54         | 54       |
| [ <u>55</u> ]                               | 55               | 55 55  | 55 15   | P2.APB                        | <u>s</u>   | 25       |
|   | 31               | 51 51  | 16 10   10   10   10   10   10   10   | PI.WEUN                       | 51         | 57       |
| 134   | 121              | 50   |   | P1.P1/4<br>P2.P0/4            | <b>ઝ</b>   | 20       |
| 益   | 58<br>7.9        | [70][50]                                     | [ <u>[1]</u>     <u>[1]</u>   | r2.p215                       | 6          | 07       |
| w   | [w]              | انا—رة                                       | <u>10</u> [13]  | P2.D015                       | <u></u>    | 40       |
|   |                  |  |   |                               |            |          |

I/O P2 CONNECTOR SLOTS

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