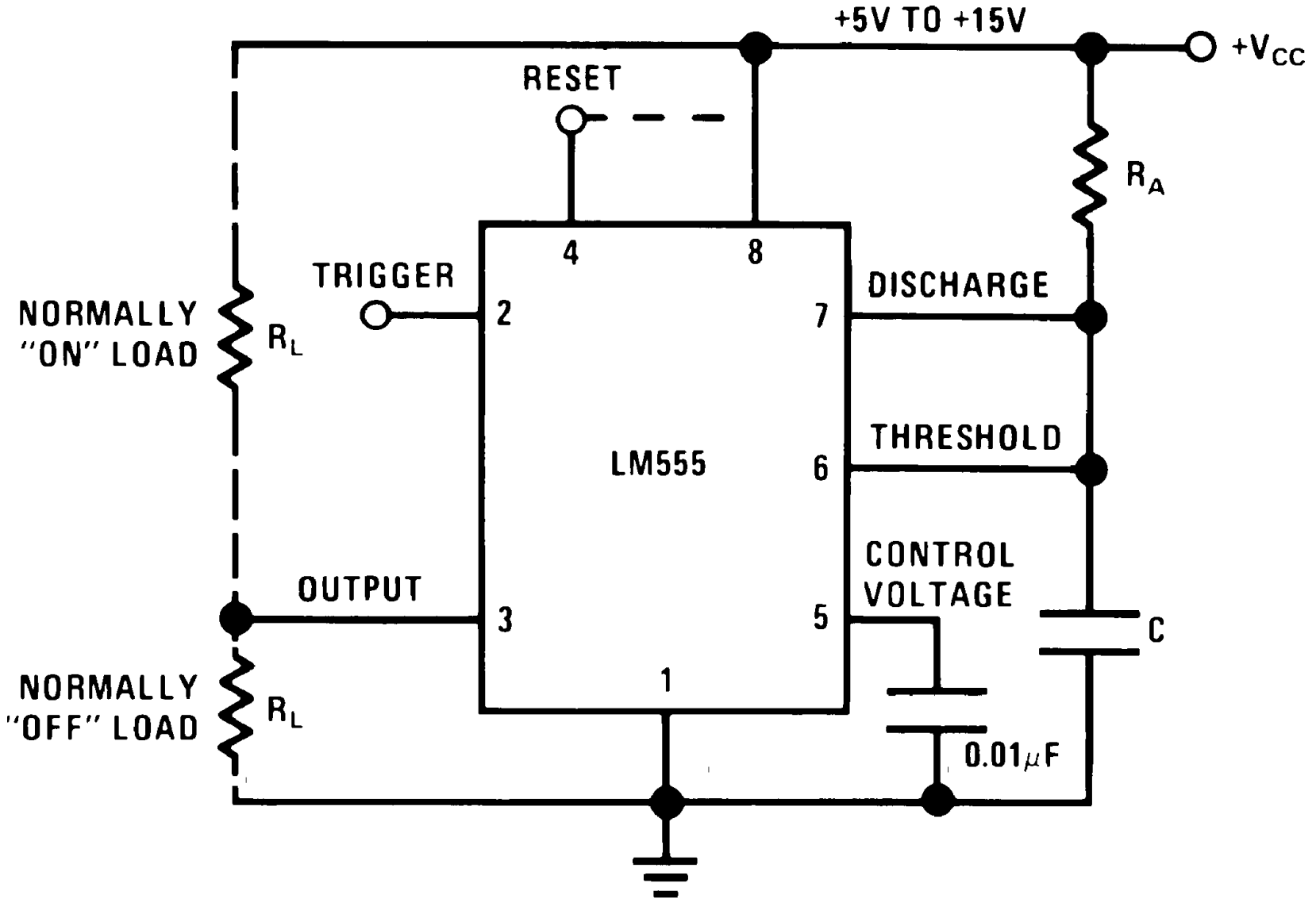

Figure 11. Monostable

Figure 20 is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01-µF bypass capacitor for control voltage pin
- C3 – 0.1-µF bypass ceramic capacitor
- C4 – 1-µF electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

10.2 Layout Example

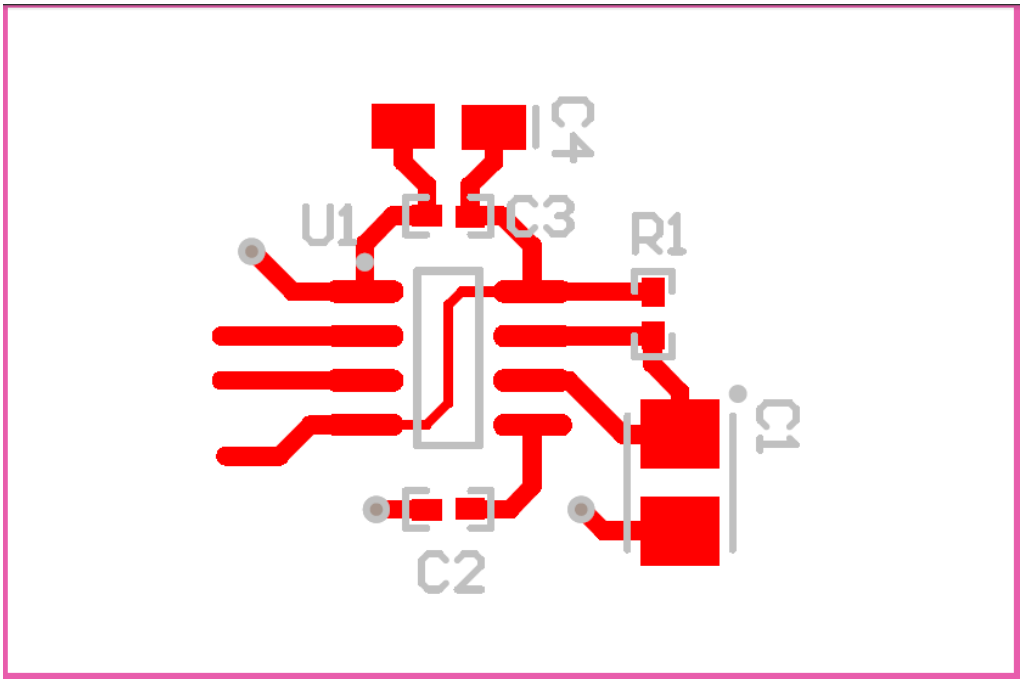

Figure 20. Layout Example