

## SERVICE SHEET 10

## N2 OSCILLATOR ASSEMBLY A13

Normally, causes of malfunctions in the Model 8660B will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A13 assembly, a part of the two-assembly N2 phase lock loop is shown schematically and described on this service sheet. The N2 Phase Detector assembly, A14, is shown schematically and described on Service Sheet 9.

When trouble has been isolated to the A13 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the N2 loop circuits the adjustment procedures specified in Section V paragraph 5-30 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-3)

Digital Voltmeter  
Frequency Counter

## N2 LOOP GENERAL INFORMATION

The purpose of the N2 loop is to generate digitally controlled RF signals in the range of 19.80 to 29.79 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section. The RF output of the N2 loop is applied to Summing Loop 2.

## 1 VOLTAGE CONTROLLED OSCILLATOR

Varactors CR8 and CR9, transistors Q2 and Q9 and associated components comprise a voltage controlled oscillator. Two varactors are used in parallel to provide high Q as well as the wide capacitance range required. C18 provides isolation for the dc levels required to bias the varactors. C17 provides the feedback required to sustain oscillation. The resonant tank circuit is coupled to Q9 by means of capacitive divider C22 and C23. The FET acts as a source follower in the feedback circuit; it provides a high impedance at the gate and a low impedance at the source. The gain of the FET amplifier for the output signal is less than one; this minimizes the Miller effect which might otherwise reflect capacitance back into the oscillator tank circuit.

Q1 amplifies the signal and applies it to U1A which functions as a Schmitt trigger. U1D inverts the output from U1A and applies it to the programmable divider in the A14 assembly. U1C inverts the output from U1A and applies it to the divide-by-one hundred circuit in Summing Loop 2.

## TEST PROCEDURE 1

## NOTE

Do not use long coax leads from the counter to TP3. The capacitive loading may attenuate the signal below a useable level.

## SERVICE SHEET 10 (Cont'd)

**Test 1-a.** Connect the counter to TP3 and set Center Frequencies as shown in Table 8-5. The counter readout should be as shown in the table. (Make allowances for counter accuracy.)

## NOTE

If the frequency readouts listed in Table 8-30 are not approximately as shown check the voltage levels shown for TP2 in Table 8-30. If the voltage levels are incorrect proceed to test procedure 2.

If the signal is present use the oscilloscope to check the outputs at XA13-1 pins 4 and 6 with center frequency set to zero. The signal at XA13-1-4 should be about 0.8 volt p/p and the signal at XA13-1-6 should be about 0.3 volt.

If the signal is present at TP3 but is not present at XA13-1 pins 4 and 6 check U1.

**Test 1-b.** If the signal is not present at TP3 use the oscilloscope to check the signal at the collector of Q1. The signal should be about 1 volt in amplitude.

If the signal is not present at Q1-c use the oscilloscope to check the signal at the Q1 base. If the signal is now present (about 0.3 volt), Q1 is probably defective.

If the signal is not present at Q1 base, check Q2, Q9 and associated components.

## 2 PRETUNING CIRCUIT

The frequency of the voltage controlled oscillator is roughly preset by the digital to analog converter (U2, U3, transistors connected to the outputs of the NAND gates and associated components). The digital to analog converter cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the loop. The inputs to U2 and U3 are BCD bits coded 8, 4, 2 and 1. When any of the BCD inputs are high they cause the output of the NAND gate with which they are associated to go low; the transistor associated with the NAND gate is switched on.

When all of the BCD inputs are low Q4 is biased to provide approximately -25 volts at TP1 (Q3-e). With this dc level at TP1 the oscillator is roughly preset to 29.79 MHz.

When any one or more of the BCD inputs go high the transistor associated with it saturates and draws current through R34 and R35. The change in bias for Q4 causes the voltage at TP1 to go less negative (closer to ground level). Finally when the binary input is 99, the voltage at TP1 is approximately -5.2 volts and the oscillator frequency is roughly preset to 19.80 MHz.

Q12 is a summing amplifier which combines the output of the digital to analog converter and the signal from the N2 phase detector. The summing point (Q12-e) sums the current from three sources, a current source from the +20 volt supply through R28, R30 and R37, a negative source from the digital to analog converter (TP1) and the signal from the N2 phase detector. The voltage at the summing point is always zero volts.

When TP1 is at approximately -25 volts (no BCD input), most of the current from the +20 volt supply flows through Q4 and Q3; very little flows through Q12. Under these conditions the voltage at Q12-c is about -30 volts. As the voltage at TP1 decreases (gets closer to ground level) less current flows through Q4 and Q3, more current flows through Q12, and the Q12 collector voltage decreases.

## SERVICE SHEET 10 (Cont'd)

**Test 1-a.** Connect the counter to TP3 and set Center Frequencies as shown in Table 8-5. The counter readout should be as shown in the table. (Make allowances for counter accuracy.)

## NOTE

If the frequency readouts listed in Table 8-30 are not approximately as shown check the voltage levels shown for TP2 in Table 8-30. If the voltage levels are incorrect proceed to test procedure 2.

If the signal is present use the oscilloscope to check the outputs at XA13-1 pins 4 and 6 with center frequency set to zero. The signal at XA13-1-4 should be about 0.8 volt p/p and the signal at XA13-1-6 should be about 0.3 volt.

If the signal is present at TP3 but is not present at XA13-1 pins 4 and 6 check U1.

**Test 1-b.** If the signal is not present at TP3 use the oscilloscope to check the signal at the collector of Q1. The signal should be about 1 volt in amplitude.

If the signal is not present at Q1-c use the oscilloscope to check the signal at the Q1 base. If the signal is now present (about 0.3 volt), Q1 is probably defective.

If the signal is not present at Q1 base, check Q2, Q9 and associated components.

## 2 PRETUNING CIRCUIT

The frequency of the voltage controlled oscillator is roughly preset by the digital to analog converter (U2, U3, transistors connected to the outputs of the NAND gates and associated components). The digital to analog converter cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the loop. The inputs to U2 and U3 are BCD bits coded 8, 4, 2 and 1. When any of the BCD inputs are high they cause the output of the NAND gate with which they are associated to go low; the transistor associated with the NAND gate is switched on.

When all of the BCD inputs are low Q4 is biased to provide approximately -25 volts at TP1 (Q3-e). With this dc level at TP1 the oscillator is roughly preset to 29.79 MHz.

When any one or more of the BCD inputs go high the transistor associated with it saturates and draws current through R34 and R35. The change in bias for Q4 causes the voltage at TP1 to go less negative (closer to ground level). Finally when the binary input is 99, the voltage at TP1 is approximately -5.2 volts and the oscillator frequency is roughly preset to 19.80 MHz.

Q12 is a summing amplifier which combines the output of the digital to analog converter and the signal from the N2 phase detector. The summing point (Q12-e) sums the current from three sources; a current source from the +20 volt supply through R28, R30 and R37, a negative source from the digital to analog converter (TP1) and the signal from the N2 phase detector. The voltage at the summing point is always zero volts.

When TP1 is at approximately -25 volts (no BCD input), most of the current from the +20 volt supply flows through Q4 and Q3; very little flows through Q12. Under these conditions the voltage at Q12-c is about -30 volts. As the voltage at TP1 decreases (gets closer to ground level) less current flows through Q4 and Q3, more current flows through Q12, and the Q12 collector voltage decreases.

## SERVICE SHEET 10 (Cont'd)

CR4 through CR7, CR11 through CR16 and associated resistors are used to shape the voltage applied to the varactors in the voltage controlled oscillator circuit so that the frequency will be linear with the voltage change. The voltage at the junction of R42 and R47 is about -27.5 volts. When there is no BCD input (Q12-c is about -30 volts) all of the diodes in the shaper are reverse biased. As the voltage at TP1 decreases (gets closer to -5.2 volts) current through Q12 increases and the Q12 collector voltage also decreases. As the Q12-c voltage decreases first CR4, then CR5, etc. are forward biased. As the diodes are forward biased resistors are added in parallel with R31 and R32 to shape the voltage curve to the varactors.

Q11 and Q10 are emitter followers which couple the output of Q12 to the varactors. Q11 provides a high impedance for the output of the summing amplifier, Q12.

## TEST PROCEDURE 2

**Test 2-a.** Use the digital voltmeter to check the voltages at TP1 and TP2. These dc levels should be about as shown in Table 8-30 for the center frequencies shown.

If the voltages at TP1 are about right, but those at TP2 are not, check Q12, Q11, Q10 and associated components.

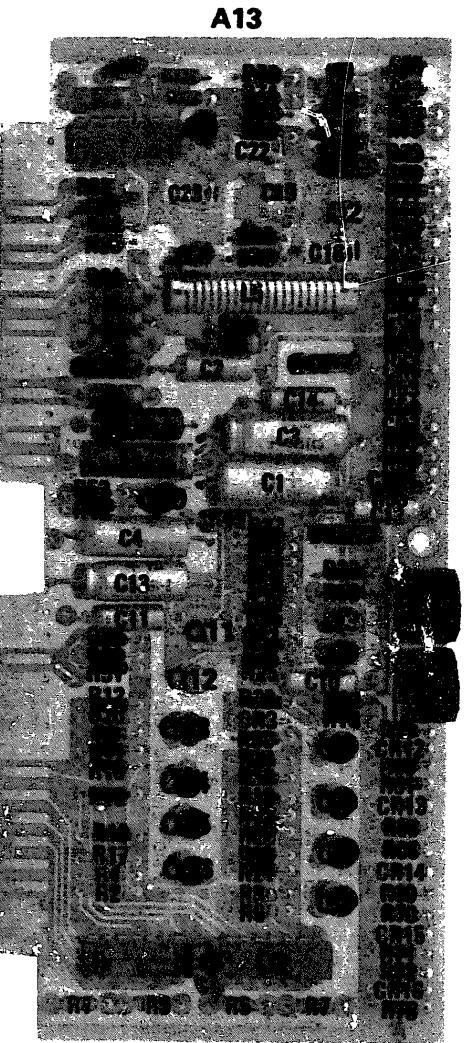
If the voltages at TP1 are not approximately as shown in Table 8-30, check the components in the digital to analog converter.

## NOTE

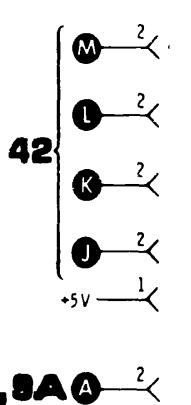
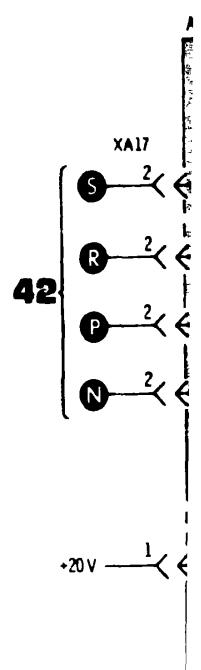
Also check the BCD input lines for the correct levels. With CF digits 4 and 5 set to a zero all eight input lines should be low. With CF digits 4 and 5 set to a 1 inputs at XA13-2 pins 11 and 9 should be high, etc..

Table 8-30. N2 Frequency versus Voltage Chart

Center Frequency	Counter Readout	TP1 Volts	TP2 Volts
00000 Hz	29.790000 MHz	-25	-31
11100 Hz	28.680000 MHz	-23	-26
22200 Hz	27.570000 MHz	-21	-21
33300 Hz	26.460000 MHz	-18.5	-16.8
44400 Hz	25.350000 MHz	-16.4	-13.4
55500 Hz	24.240000 MHz	-14.2	-10.6
66600 Hz	23.130000 MHz	-12	-8.3
77700 Hz	22.020000 MHz	-9.8	-6.4
88800 Hz	20.910000 MHz	-7.7	-4.8
99900 Hz	19.800000 MHz	-5.4	-3.6



**Figure 8-36. A13 N2 VCO Component Location**



## SERVICE SHEET 11

### N3 PHASE DETECTOR ASSEMBLY A10

Normally, causes of malfunctions in the Model 8660B will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A10 assembly, a part of the two-assembly N3 phase lock loop is shown schematically and described on this service sheet. The N3 oscillator assembly, A8, is shown schematically and described on Service Sheet 12.

When trouble has been isolated to the A10 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

#### NOTE

After making repairs to any part of the N3 loop circuits the adjustment procedures specified in Section V paragraph 5-31 should be performed to ensure proper operation of the instrument.

### TEST EQUIPMENT REQUIRED (See Table 1-3)

Oscilloscope (with 10:1 divider probes)

Digital Voltmeter  
Frequency Counter

### N3 LOOP GENERAL INFORMATION

The purpose of the N3 loop is to generate digitally controlled RF signals in the range of 20.01 to 21.00 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section.

The RF output of the N3 voltage controlled oscillator is divided by ten before being applied to the SL2 assembly. The output to SL2 is 2.001 to 2.100 MHz in 1 kHz increments.

### 1 N3 PROGRAMMABLE DIVIDER CIRCUIT

All of the integrated circuits in the A10 assembly are used to count down the input from the N3 voltage controlled oscillator.

When there are no BCD inputs to U5 and U6 (all inputs low), the input from the oscillator will be 21.00 MHz when the oscillator is phase locked; the programmable divider will divide by 2100 to provide a 10 kHz output at TP3. U5 and U6 are preset by CF digits 1 and 2 and programmed to vary between start counts of 00 and 99. Operation of the circuit is as follows:

Assume that initially all BCD inputs are low and U4, U5 and U6 have been preset to zero. Assume also that U2A pin 6 ( $\bar{Q}$ ) and U2B pin 8 ( $\bar{Q}$ ) are both low. U1B pin 8 ( $Q$ ) and U1A pin 6 ( $\bar{Q}$ ) are both high.

NAND gate U7C couples the input from the N3 oscillator to the clock input of U5. U5 provides a divided-by-ten output to clock U6 and also provides A, B and C (BCD 1, 2 and 4) outputs. The A, B and C outputs are not used until the count of 2097 has been reached.

U6 provides a divided-by-ten output to clock U4 and also provides A and D (BCD 1 and 8) outputs to AND gates U3A and U3C. The A and D outputs are not used until the count has reached 2090.

U4 provides a divided-by-ten output to clock U2A. At the count of 1000 U4 clocks U2A and the U2A  $\bar{Q}$  output at pin 6 goes high. At the count of 2000 U4 again clocks U2A and the negative-going  $\bar{Q}$  output at pin 6 clocks U2B. When U2B is clocked  $\bar{Q}$  at pin 8 goes high and is applied to pins 2 and 13 of AND gate U3A.

At the count of 2090 the high A and D outputs of U6 are applied to AND gates U3A and U3C. Since U3A pins 2 and 13 are both high, U3A is enabled and it places a high on pin 11 of AND gate U3C.

## SERVICE SHEET 11 (Cont'd)

At the count of 2097 the high A, B and C outputs of U5 are applied to AND gates U3B and U3C to provide a high at the J input of U1B at pin 11.

At the count of 2098 U1B is clocked, U1B  $\bar{Q}$  (pin 8) goes low and sets U1A. U1A  $\bar{Q}$  (pin 6) goes low and presets U2, U4, U5 and U6; they are held in preset until the count is completed.

When U1A is set Q (pin 5) goes high and initiates the sampling pulse. The first pulse to the sampling phase detector is initiated by the 2098th input cycle. Since two more cycles are required to restart the count cycle, following sampler pulses are 2100 cycles apart when there is no BCD input.

At the count of 2099 U1B is again clocked and  $\bar{Q}$  (pin 8) goes high. The high at pin 8 is applied to the K input of U1A (pin 2).

At the count of 2100 U1A is clocked and pin 6  $\bar{Q}$  goes high to end the preset pulse. The next input to U5 initiates the next count cycle.

When there is a BCD input programmed into U5 and U6 pins 3, 4, 10 and 11 the terminal count is still 2100. However, the count starts at the number programmed into the BCD inputs. As an example, if the BCD input to U5 and U6 is 99, the first input cycle would cause the same digital circuit changes that the 100th input cycle caused in the discussion above (U4 would be clocked). The frequency division would be 2100-99, equal to division by 2001. The phase lock loop operation would result in an input frequency to the programmable divider of 20.01 MHz. When divided by 2001, the divider output at TP3 would again be 10 kHz.

The output from U1A pin 5 is always 10 kHz when the oscillator is phase locked regardless of the oscillator frequency.

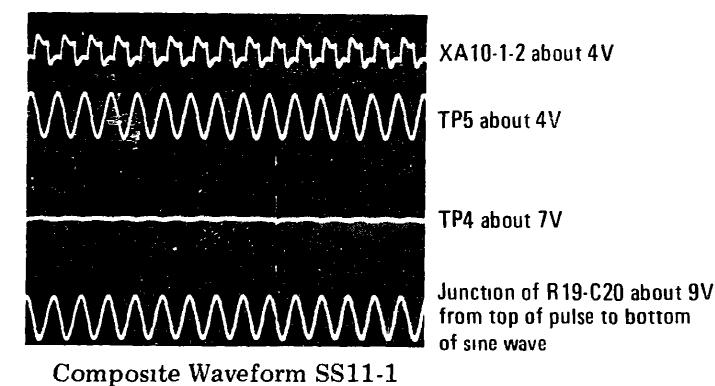
### TEST PROCEDURE 1

Composite Waveform SS11-1 illustrates the proper timing relationship between the 100 kHz reference input, the pulse output from the pulse generator and the sampling point on the 100 kHz reference signal when the loop is locked.

#### NOTE

Center Frequency is initially set to zero.

Test 1-a. Use the counter and the oscilloscope to check for a 100.000 kHz sine wave at approximately 5 volts p/p at TP5. The display should be similar to that shown in the second trace from the top of composite waveform SS11-1.



## SERVICE SHEET 11 (Cont'd)

If the counter readout is 100,000 kHz but the sine wave is distorted, check Q1, Q2 and associated components.

If the signal is not present, connect the counter and the oscilloscope to XA10-1-2. The counter readout should be 100.000 kHz and the oscilloscope display should be similar to that shown in the top trace of composite waveform SS11-1.

If the correct signal is present at XA10-1-2, but was not present at TP5, check Q1, Q2 and associated components.

If the signal is not present at XA10-1-2 check interconnections to the reference loop and, if necessary, the reference loop.

Test 1-b. Connect the oscilloscope and the counter to TP4. The counter readout should be 100.000 kHz and the oscilloscope should display positive-going pulses as shown in composite waveform SS11-1 at about 7 volts amplitude. If the signal is not present, proceed to test 1-c.

If the signal is present, connect the oscilloscope to the junction of R19 and C20. The oscilloscope display should be similar to that shown in the lowest trace of composite waveform SS11-1.

If the programmable divider and the pulse generator are working properly but the loop is not phase locked, the oscilloscope may still display the signals at the junction of R19 and C20, but the relationship between the pulses and the sine wave will not be the same as shown in composite waveform SS11-1. If the voltage controlled oscillator and the summing circuit in the A8 assembly are known to be functioning properly, proceed to test procedure 2.

Test 1-c. If the pulses are not present at TP4, and the counter counts randomly or not at all, connect the oscilloscope to TP3. The oscilloscope display should be a series of pulses at approximately 10 kHz and about 3.5 volts in amplitude.

If the pulses are present at TP3, but were not present at TP4, check Q6, Q7 and associated components.

If the pulses are not present at TP3, proceed to test 1-d.

Test 1-d. If the pulse is not present at TP3 connect the oscilloscope to NAND gate U7C pin 8. The oscilloscope should display a slightly distorted sine wave at about 21 MHz and about 3 volts in amplitude.

If the signal is not present at U7C pin 8, connect the oscilloscope to XA10-2-15. The 21 MHz signal should be about 0.1 volt in amplitude. If the signal is present, U7 is probably defective. If the signal is not present check interconnections to the A8 assembly and, if necessary the A8 assembly.

Test 1-e. It is assumed in this test that the signal input is present at U5 pin 8. Composite waveforms SS11-2 through SS11-6 illustrate the correct waveforms for the integrated circuit points shown.

#### NOTE

These waveforms were taken with the oscilloscope triggered from TP3.

## SERVICE SHEET 11 (Cont'd)

Follow the numerical sequence of the waveforms shown; when an IC output is missing the trouble is found. Replace the defective component and repeat test 1-b.

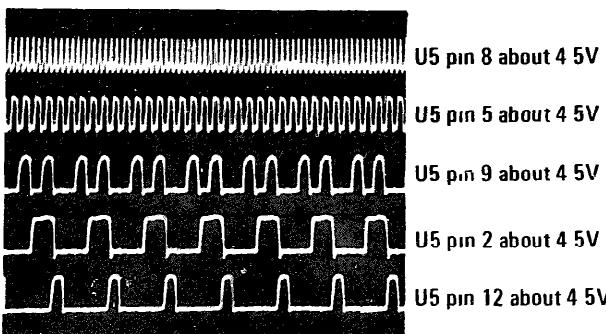
## NOTE

If the output from U5 is not present proceed to test 1-f before replacing U5.

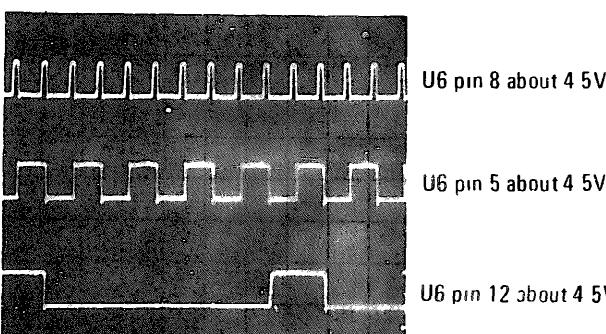
**Test 1-f.** Composite waveform SS11-7 illustrates correct waveforms for a properly operating U1. In this test the oscilloscope was again triggered by TP3 and the sweep delay of the oscilloscope was used to center the pulses shown.

If the waveforms in composite waveform SS11-7 cannot be observed (because an adequate oscilloscope is not available or other reasons) measure the voltage at U1 pin 6, it should be about +3.7 volts; U1 pin 5 should be at about +100 millivolts. If the voltages are not as specified, ground U1 pin 10. The voltages should then be; U1 pin 6 about +130 millivolts and U1 pin 5 about +3.8 volts. If the voltages are as specified in either case and there is no output from U5, U5 is probably defective.

If there is no change in the dc levels at U1 pins 5 and 6 with U1 pin 10 grounded U1 is probably defective.

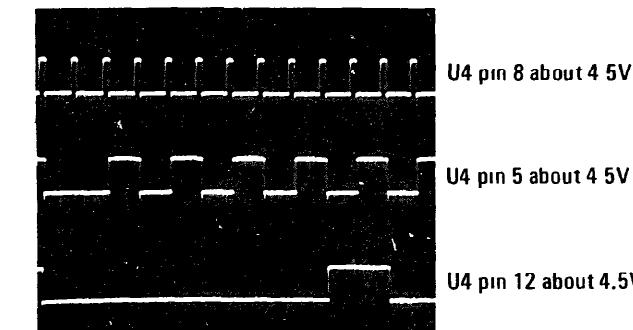


Composite Waveform SS11-2

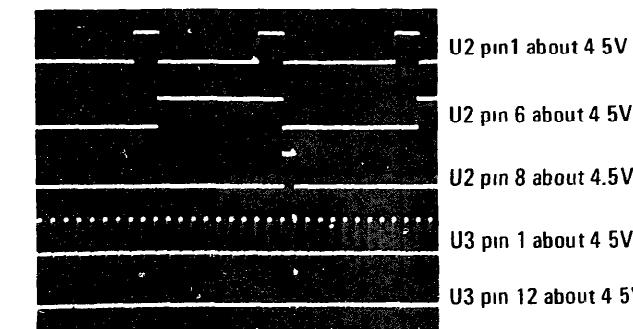


Composite Waveform SS11-3

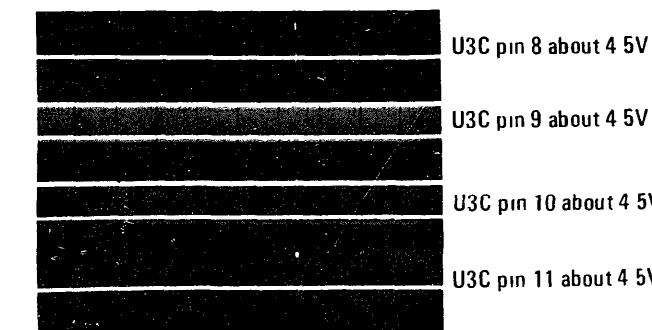
## SERVICE SHEET (Cont'd)



Composite Waveform SS11-4

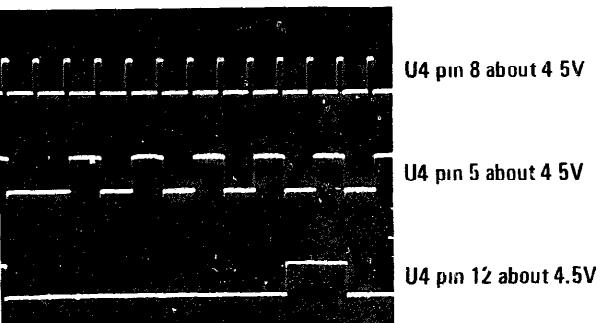


Composite Waveform SS11-5



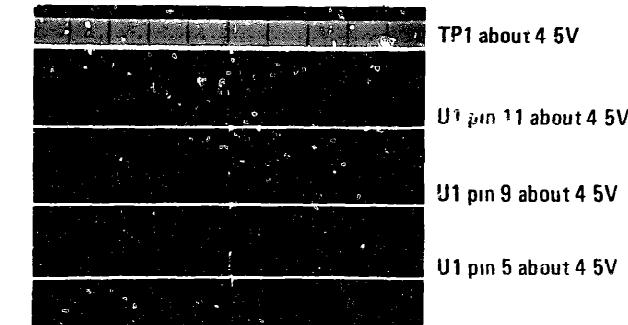
Composite Waveform SS11-6

## SERVICE SHEET 11 (Cont'd)

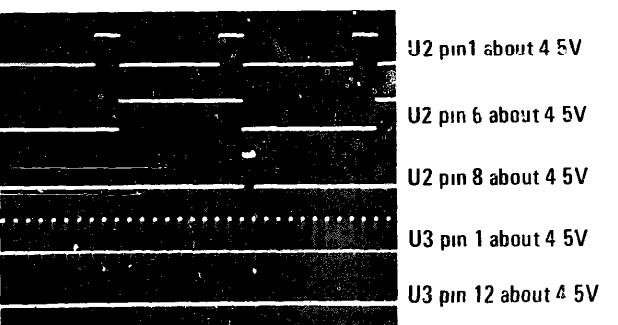


Composite Waveform SS11-4

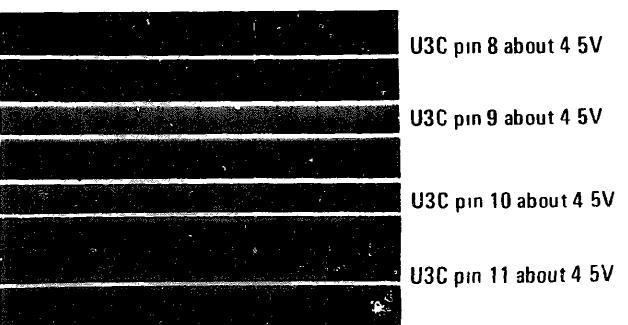
## SERVICE SHEET 11 (Cont'd)



Composite Waveform SS11-7



Composite Waveform SS11-5



Composite Waveform SS11-6

**2 SAMPLING PHASE DETECTOR**

The positive-going output from U1A Q (pin 5) is used to generate the pulse required to open the sampler gate. Common base amplifier Q6 and emitter follower Q7 amplifies and couples the pulse to T1. C<sub>P1</sub> and CR2 are used to minimize transformer flyback action. CR2 also bypasses the negative-going pulse around the transformer primary to ensure that only the positive-going pulse is coupled to the transformer secondary.

A 100 kHz signal from the reference loop is applied through Q2 and Q1 to the secondary center tap of T1. L5 and C8 (along with C4 in the reference loop A4A1 assembly) comprise a low pass filter; it has an impedance of about 450 ohms and a cutoff frequency of about 150 kHz. The TTL input from the reference loop is reshaped into a sine wave by the low pass filter Q2 and Q1 amplify the signal to the level required in the sampling phase detector. L7 and C13 comprise a tuned circuit which bypasses unwanted high frequency signals and further filters the sine wave.

Sampler diodes CR3 and CR4 are normally reverse biased. When the sampling pulse appears across the secondary of T1 it is coupled through C20 and C21 to forward bias CR3 and CR4. Since the gate pulses are equal in amplitude but opposite in polarity, they will cancel at TP6.

While CR3 and CR4 are forward biased the sampling gate is open and the 100 kHz reference input signal is sampled.

This type of sampling phase detector may be phase locked to virtually any point on the sine wave slope. Ideally, the zero crossover point of the sine wave should be used to improve the lock and lock hold capabilities of the loop.

If the divided down output of the voltage controlled oscillator (10 kHz pulses) is not phase locked to the 100 kHz reference signal an ac error signal will be developed at TP6. The polarity of the error signal at any given point in time depends on the polarity of the 100 kHz reference signal at the time the last sample was taken. The amplitude of the error signal at any given time depends on what part of the sine wave the last sample was taken from. Each time CR3 and CR4 are forward biased the 100 kHz reference signal at T1 terminals 4 and 6 are coupled through the sampling gate to control the charge on C22.

When the sampling gate pulse ends CR3 and CR4 are again reverse biased and the sampling gate is closed. Since Q4 is a high impedance input device, the charge will remain on C22 until the next sampling pulse. The current through Q4 is controlled by the difference in Gate-source voltage of the lower FET. Operation of the dual FET sets the output level at the low FET drain to exactly the level at the upper FET gate. The output is coupled through two emitter followers in the A8 assembly.

SERVICE SHEET 11 (Cont'd)

TEST PROCEDURE

**Test 2-a.** Connect the oscilloscope to TP6. If the 100 kHz reference signal is present one of the sampling gate diodes (CR3 or CR4) is probably shorted. If the gate pulses are present one of the sampling gate diodes is probably open (Negative-going pulses CR4 - positive-going pulses CR3). Proceed to test 2-b.

**Test 2-b.** With the oscilloscope connected to TP6, ground TP8. The oscilloscope should display a low frequency sine wave (about 4 volts) that varies in frequency. The frequency of the signal will be the difference frequency detected by the sampling gate.

If the signal is present at TP6, connect the oscilloscope to Q5-e. The sine wave should be the same as seen at TP6.

If the signal is present at Q5-e the error amplifier and the sampler circuit are functioning properly.

If the signal is not present at Q5-e and was present at TP6, check Q3, Q4, Q5 and associated components.

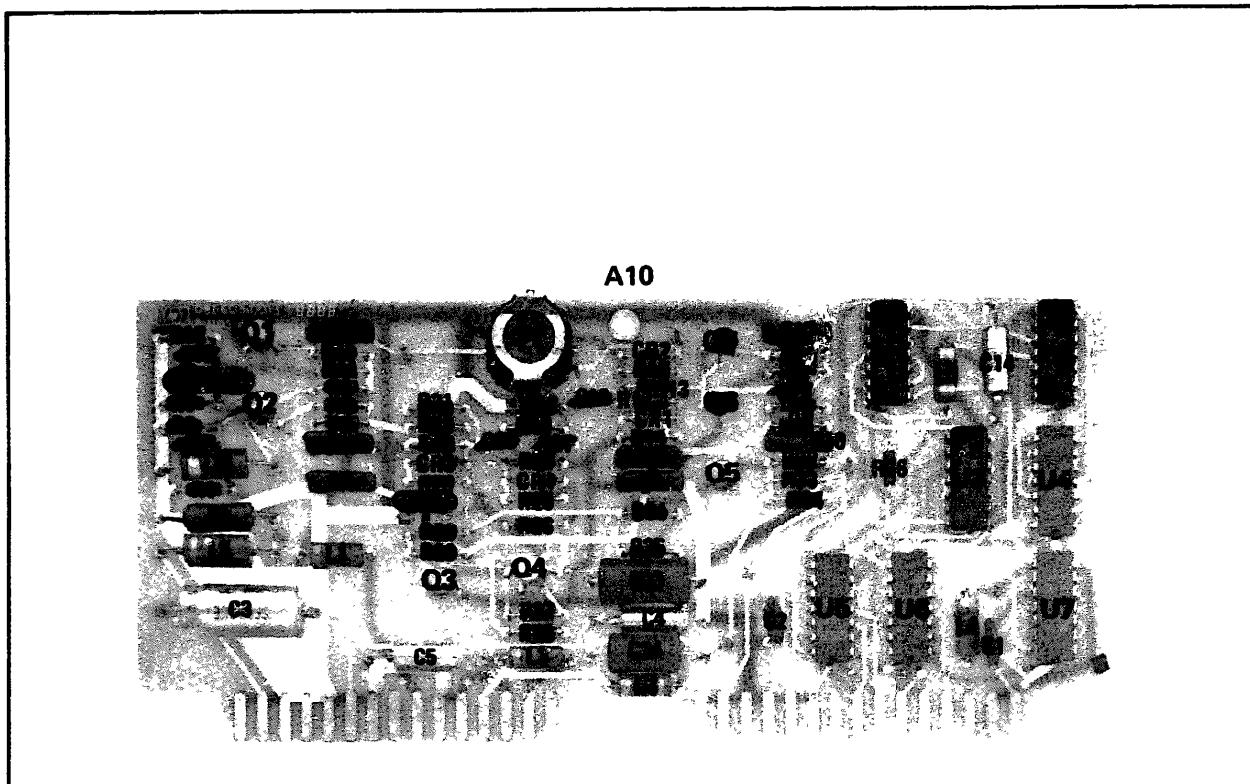
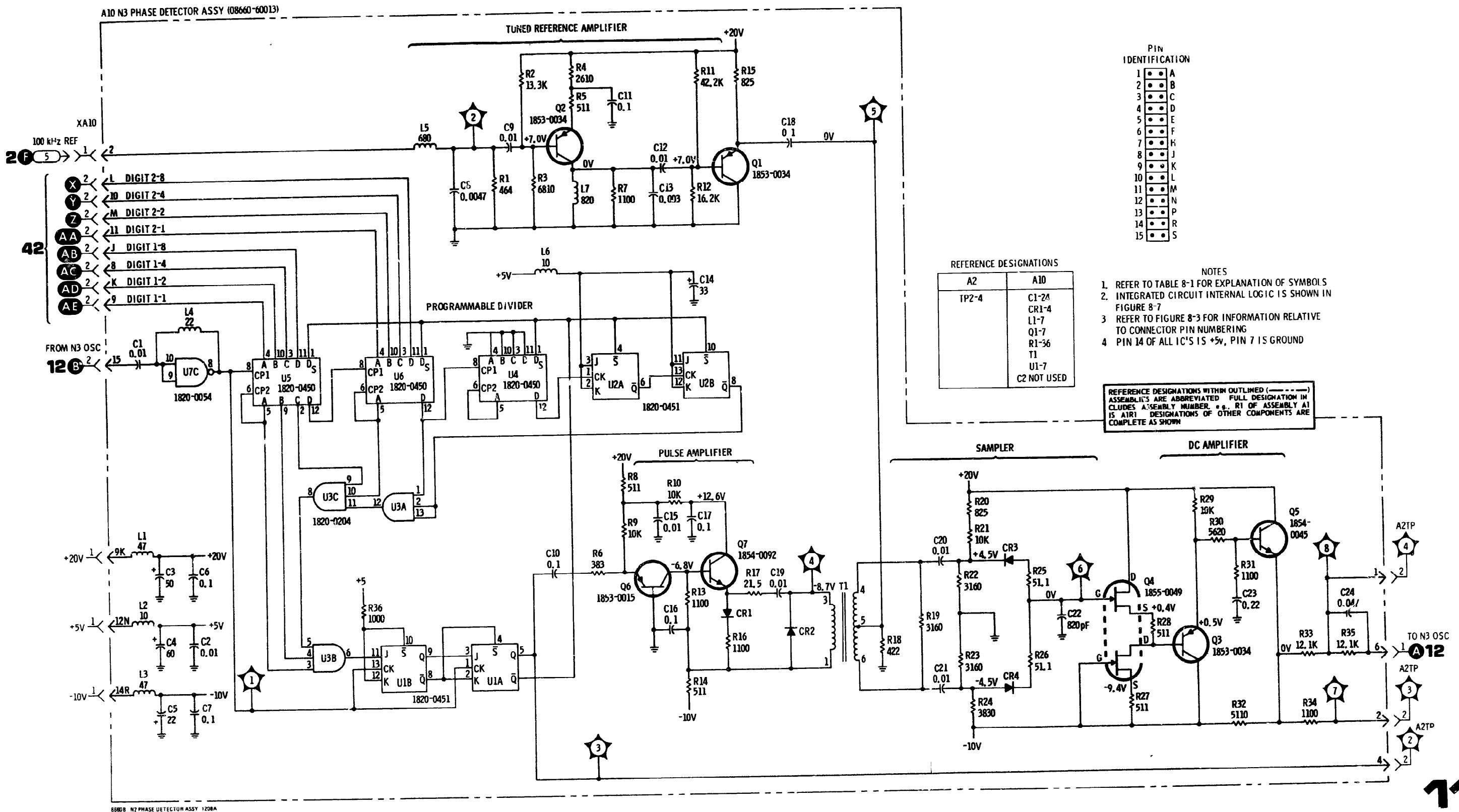


Figure 8-38. A10 N3 Phase Detector Component Locations

11  
A10Figure 8-39 N3 Phase Detector Schematic  
8-91

## SERVICE SHEET 12

### N3 OSCILLATOR ASSEMBLY A8

Normally, causes of malfunctions in the Model 8660B will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A8 assembly, a part of the two-assembly N3 phase lock loop is shown schematically and described on this service sheet. The N3 Phase Detector assembly, A10, is shown schematically and described on Service Sheet 11.

When trouble has been isolated to the A8 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

#### NOTE

After making repairs to any part of the N3 loop circuits the adjustment procedures specified in Section V paragraph 5-31 should be performed to ensure proper operation of the instrument.

#### TEST EQUIPMENT REQUIRED (See Table 1-3)

Digital Voltmeter  
Frequency Counter

#### N3 LOOP GENERAL INFORMATION

The purpose of the N3 loop is to generate digitally controlled RF signals in the range of 20.01 to 21.00 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section. The RF output of the N3 voltage controlled oscillator is divided by ten before it is applied to summing Loop 2. The output from the N3 assembly to SL2 is 2.001 to 2.100 MHz in selectable 1 kHz increments.

#### VOLTAGE CONTROLLED OSCILLATOR

Q2, Q7 and associated components comprise a voltage controlled oscillator. C14 and C17 provide isolation for the dc levels required to bias the varactor. C13 provides the feedback required to sustain oscillation. The resonant tank is coupled to Q7 by capacitive divider C16 and C17. The FET acts as a source follower in the feedback circuit; it provides a high impedance at the gate and a low impedance at the source. The gain of the FET for the output signal at the drain is held at less than unity to minimize the Miller effect which might otherwise reflect capacitance back into the oscillator tank circuit.

Q1 amplifies the voltage controlled oscillator output and applies it to U1A which functions as a Schmitt trigger. U1D provides the output to the N3 programmable divider in the A10 assembly. U1B and U3 provide a divided by ten output to Summing Loop 2.

## SERVICE SHEET 12 (Cont'd)

### TEST PROCEDURE

#### NOTE

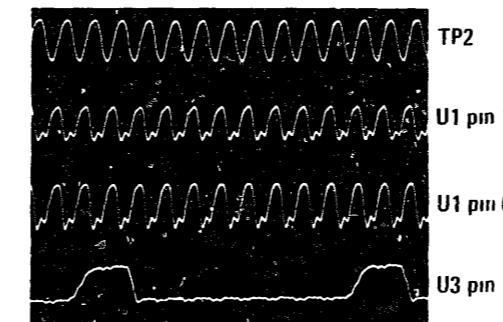
Do not use long coax leads from the counter to N3 test points. The capacitive loading may attenuate the signal below a useable level.

**Test 1-a.** Connect the counter to TP2. With the center frequency set to zero the counter readout should be 21.00 MHz. Set CF digits 1 and 2 to the settings specified in Table 8-31. Frequency readouts on the counter should follow those specified in the table. (Make allowances for counter accuracy).

#### NOTE

If the frequency readouts listed in Table 8-31 are not approximately as shown, check the voltage levels shown for TP3 in the table. If the voltage levels are incorrect proceed to test procedure 2.

If the signal is present use the oscilloscope to check the signal at points shown in composite waveform SS12-1. Signals shown are about 4 volts in amplitude.



Composite Waveform SS12-1

If the signal is present at TP2 but is not present at U1 pin 11, U1 is probably defective; if the signal is not present at U3 pin 12, U1 or U3 may be defective.

If the signal is not present at TP2 use the oscilloscope to check for the signal at Q1-b. If the signal is present at Q1-b check Q1 and NAND gate U1A. If the signal is not present check Q2, Q7 and associated components.

#### 2 PRETUNING CIRCUIT

The frequency of the voltage controlled oscillator is roughly preset by the digital to analog converter (U2 and Q8 through Q11). The digital to analog converter

## SERVICE SHEET 12 (Cont'd)

cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the phase lock loop. The inputs to U2 are BCD bits coded 1, 2, 4 and 8. When any one of the BCD inputs are high they cause the output of the NAND gate to which they are connected to go low; the transistor connected to the NAND gate output is switched on.

When all of the BCD inputs are low Q6 is biased to provide approximately -8.5 volts at TP1 (Q5-e). With this dc level at TP1 the oscillator is roughly preset to 21 MHz (how close depends on adjustment of R24 and R26).

When any one or more BCD inputs go high the transistor associated with it saturates and the current through Q6 is reduced. The reduction of current through Q6 changes the bias on Q5 and causes the voltage at TP1 to go less negative (closer to dc ground level). Finally, when the BCD input is 9, the voltage at TP1 is approximately -6.7 volts and the oscillator is roughly preset to 20.01 MHz (again depending on adjustment of R24 and R26).

Q3 is a summing amplifier which combines the output of the digital to analog converter and the error signal from the N3 Phase Detector. The summing point (Q3-e) sums the current from three sources; a current source from the +20 volt power supply through R19, R25 and R26, a negative source from the digital to analog converter (TP1), and the error signal from the phase detector. The voltage at the summing point is always zero volts when the loop is locked.

The output from Q3 is coupled through Q4 and Q12 to control the bias on varactor CR5 and the frequency of the voltage controlled oscillator.

## TEST PROCEDURE 2

**Test 2-a.** Use the digital voltmeter to check the voltages at TP1 and TP3. These dc levels should be about as shown in Table 8-31 for the center frequencies shown.

## NOTE

These voltages are typical. They will vary from instrument to instrument because of differences in individual varactor characteristics.

If the voltages at TP1 are about right, but those at TP3 are not, check Q3, Q4, Q12 and associated components.

If the voltages at TP1 are not approximately as shown in Table 8-31, check the components in the digital to analog converter.

## NOTE

Also check the dc levels at the BCD input lines.

## SERVICE SHEET 12 (Cont'd)

Table 8-31. N3 Frequency Versus Voltage Chart

Center Frequency	Counter Readout	TP1 Voltage	TP3 Voltage
00 Hz	21.000000 MHz	-8.5 V	-3.7 V
11 Hz	20.890000 MHz	-8.3 V	-3.6 V
22 Hz	20.780000 MHz	-8.1 V	-3.5 V
33 Hz	20.670000 MHz	-7.9 V	-3.4 V
44 Hz	20.560000 MHz	-7.7 V	-3.3 V
55 Hz	20.450000 MHz	-7.5 V	-3.2 V
66 Hz	20.340000 MHz	-7.3 V	-3.1 V
77 Hz	20.230000 MHz	-7.1 V	-3.0 V
88 Hz	20.120000 MHz	-6.9 V	-2.9 V
99 Hz	20.010000 MHz	-6.7 V	-2.8 V

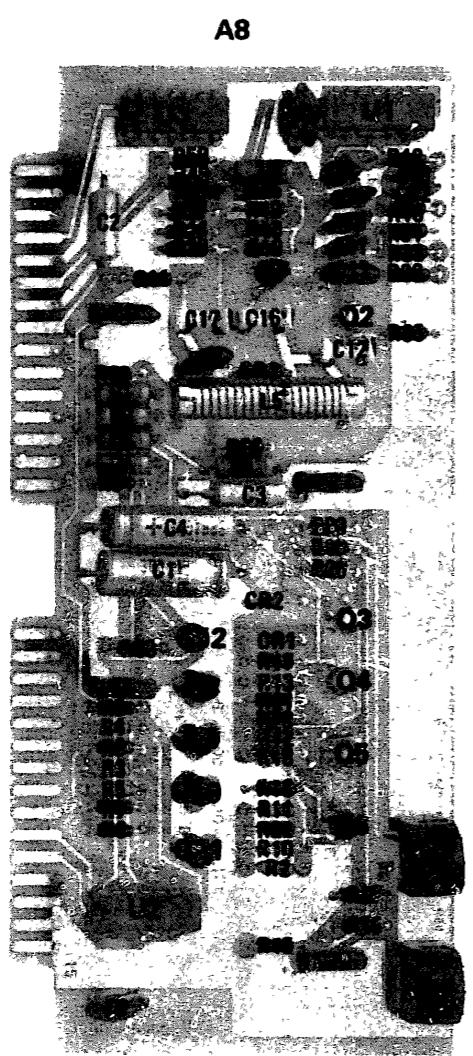


Figure 8-40. A8 N3 VCO Component Locations

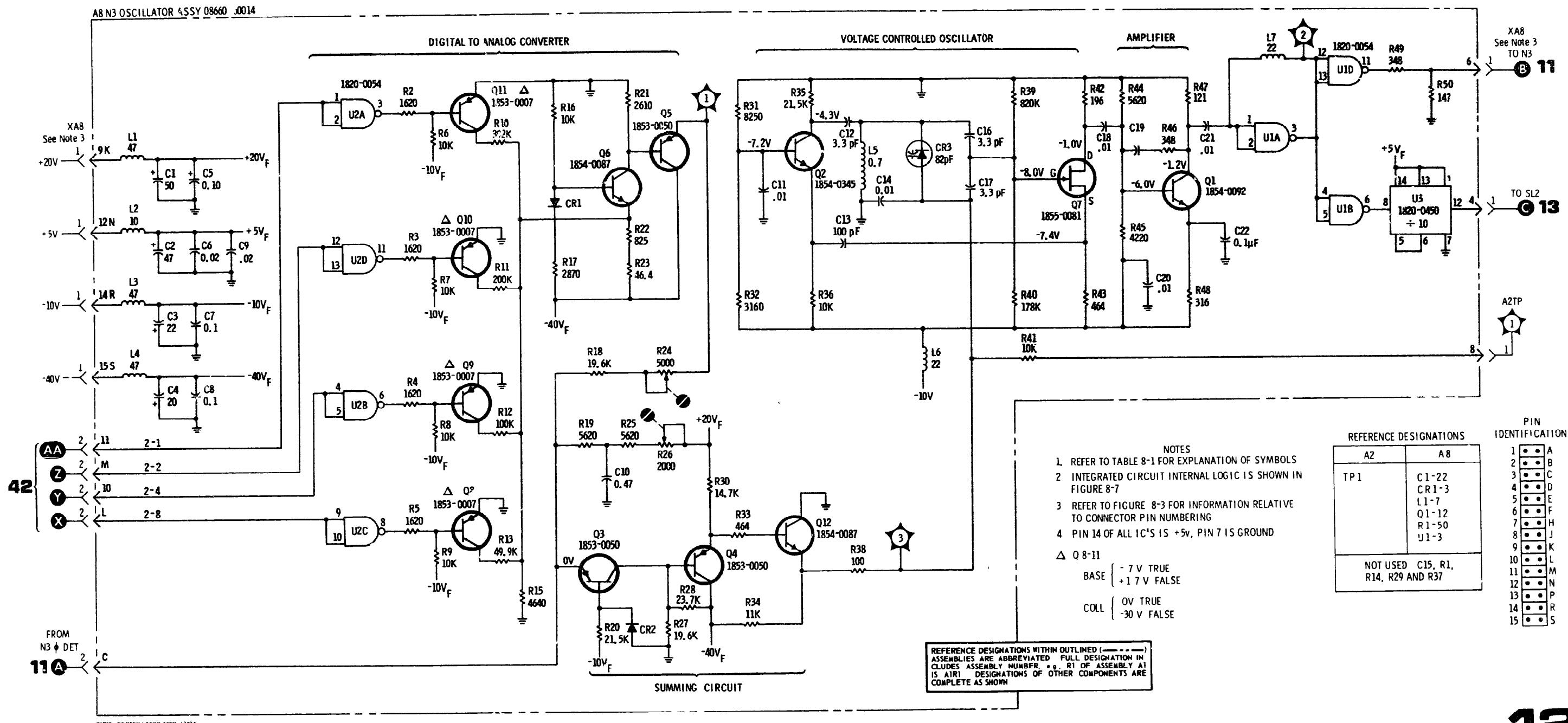


Figure 8-41. N3 VCO Schematic

## SERVICE SHEET 13

### SUMMING LOOP 2 PHASE DETECTOR A12

Normally, causes of malfunctions in the Model 8660B will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A12 assembly, a part of the two-assembly SL2, is shown schematically and described on this Service Sheet. The SL2 Oscillator Assembly (A11) is shown schematically and described on Service Sheet 14.

When trouble has been isolated to the A12 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

#### NOTE

After making repairs to any part of the SL2 circuits the adjustment procedures in Section V paragraph 5-32 should be performed to ensure proper operation of the instrument.

#### TEST EQUIPMENT REQUIRED (See Table 1-3)

Oscilloscope (with 10:1 divider probes)  
Digital Voltmeter  
Frequency Counter

### SUMMING LOOP 2 GENERAL

The purpose of Summing Loop 2 (SL2) is to generate digitally controlled RF signals in the range of 20.0001 to 30.0000 MHz in selectable 100 Hz increments. The difference frequency between the SL2 voltage controlled oscillator and the input from the N2 loop is phase locked to the divided-by-ten output of the N3 assembly. The output of SL2 is applied to SL1.

The portion of the pretuning circuit that appears on service sheet 13 (U8 and Q8 through Q11) is explained in the text for service sheet 14.

### PHASE DETECTOR

There are three signal inputs to the phase detector assembly. They are the output of the N2 voltage controlled oscillator, the divided by ten output of the N3 voltage controlled oscillator and the output of the SL2 voltage controlled oscillator.

The N2 and SL2 signals are mixed and the difference frequency is used as one input to the digital phase detector. The second input to the digital phase detector is the divided by ten input from the N3 assembly.

The output of the N3 voltage controlled oscillator is divided by ten in the N3 assembly and again divided by ten by U9. Q12 and NAND gate U7A shape the resulting pulses which vary in frequency (depending on programming to the N3 loop) from 0.2001 to 0.2100 MHz. The pulses at TP2 are negative-going.

## SERVICE SHEET 13 (Cont'd)

The inputs from the N2 loop and the SL2 voltage controlled oscillator are applied to double balanced mixer E1 R and L ports. The difference signal from the X port is amplified by Q5 and Q4 and shaped by Q3, Q7 and NAND gates U4B and U4C. When the loop is phase locked the negative-going pulses at TP3 are at the same frequency as those at TP2. The pulses do not appear in time coincidence; they are received alternately.

U7B, U7D, U4A and U4D comprise a coincidence gate which inhibits signals that appear simultaneously at TP2 and TP3. Normally, when signals are not present, TP2 and TP3 are both high. When a signal appears at TP2, U7B pin 6 and U4D pin 13 go high. If there is no signal at TP3 U5D pin 12 is also high; U4D pin 11 goes low, and U1B pin 6 goes high. The positive pulse at TP5 drives the clock generator and the sense circuit or phase detector. When a signal appears at TP3, U4A pin 3 and U7D pin 12 go high. If there is no signal at TP2, U7D pin 13 is also high; U7D pin 11 goes low, and U7C pin 8 goes high. The positive pulse at TP9 drives the clock generator and the sense circuit or the phase detector. When signals appear at TP2 and TP3 at the same time U7D pin 13 and U4D pin 12 go low, U7D pin 11 and U4D pin 11 remain high, and the signals cannot reach TP5 or TP9.

U1A, U1C, U1D and U5C comprise a clock generator which clocks U2A and U2B each time a signal appears at TP5 or TP9. With no signals present TP5 and TP9 are low. When a positive pulse appears at TP9 U1A pin 3 goes low, U1D pin 11 goes high and a negative-going pulse appears at TP6. When a positive pulse appears at TP5 operation of the circuit is the same except that U1C pin 8 goes low (rather than U1A pin 3). Since a clock pulse is generated for each input, the pulse frequency at TP6 is the sum of the frequencies at TP5 and TP9.

Since the sense circuit does not function when the loop is locked, operation of the phase detector will be discussed first.

When the loop is phase locked U2A  $\bar{Q}$  is held high to enable U3A and U3D. Assume that initially U2B  $\bar{Q}$  is high, U3B pin 6 is low and U3C pin 8 is high. When a positive-going signal from TP9 appears at U3A pin 1, U3A pin 3 goes low and causes a change in state of flip-flop U3B/U3C; U3B pin 6 goes high and U3C pin 8 goes low. The high at U2B pin 12 sets the flip/flop and the positive-going trailing edge of the clock pulse causes U2B Q to go high. The following positive pulse from TP5 is applied to U3D pin 12, U3D pin 11 goes low and changes the state of flip/flop U3B/U3C. U3B pin 6 goes low and the clock pulse causes U2B  $\bar{Q}$  to again go high. This sequence continues as long as the signals at TP5 and TP9 are received alternately.

The signals at TP5 and TP9 are applied to the sense circuit even when the loop is phase locked. They have no effect on the circuit because of the relationship of the Q and  $\bar{Q}$  outputs of U2B to the incoming signals.

## SERVICE SHEET 13 (Cont'd)

When U2B Q is high NAND gates U6A and U6C are enabled. When the signal from TP5 appears at U6C pin 9, U6C pin 8 goes low; flip/flop U5A/U5B does not change state because U5B pin 3 is low. The signal at U6B has no effect because U2B  $\bar{Q}$  and U6B pin 4 are low.

When U2B  $\bar{Q}$  is high NAND gates U6B and U6D are enabled. When the signal at TP9 appears at U6D pin 13, U6D pin 11 goes low; flip/flop U5A/U5B does not change state because U5B pin 3 is low. The signal at pin 1 of U6A has no effect on the circuit because U2B Q and pin 2 of U6A are low.

When two or more consecutive pulses from either input (TP5 or TP9) occur between pulses from the other input the sense circuit functions to disable the phase detector until the frequency error is corrected.

As an example of circuit operation assume that two pulses from TP9 (SL2 signal) are received between two pulses from TP5 (N3 signal) indicating that the SL2 frequency is high. When the first pulse from TP9 is received U3A pin 3 goes low, U3B pin 6 goes high to set U2B and the clock pulse causes U2B Q to go high. When the second consecutive pulse is received from TP9 U6A has been enabled by the high Q output of U2B. U6A pin 3 goes low and causes flip/flop U5A/U5B to change state. When the D input of U2A goes low the clock pulse causes U2A  $\bar{Q}$  to go low and inhibit U3A and U3D. If a third SL2 signal is received prior to receipt of an N3 signal U6A pin 3 will again go low but will have no effect on flip/flop U5A/U5B because U5A pin 13 is low.

When an N3 pulse is received U2B Q is still high and U6C pin 8 will go low to change the state of flip/flop U5A/U5B. When the D input of U2A goes low the clock pulse causes U2A  $\bar{Q}$  to go high and enable U3A and U3D. The propagation time of the signal through the sense circuit is long enough for the pulse from N3 (TP5) to have ended before U3D is enabled so the state of flip/flop U3B/U3C does not change.

The next pulse from SL2 will again cause U6A pin 3 to go low and change the state of flip/flop U5A/U5B. With the D input to U2A high again, the clock pulse again causes U2A  $\bar{Q}$  to go low and inhibit U3A and U3D. The signal applied to U3A has no effect on flip/flop U3B/U3C because U3B pin 5 is low.

The sense circuit continues operation in the manner described above until two consecutive N3 pulses are received between two SL2 signals. When this occurs the first pulse causes U6C pin 8 to go low and change the state of flip/flop U5A/U5B. With the D input to U2A low the clock pulse will cause U2A  $\bar{Q}$  to go high and enable U3A and U3D. Again, because of propagation time through the sense circuit

## SERVICE SHEET 13 (Cont'd)

U2B Q is high NAND gates U6A and U6C are enabled. When signal from TP5 appears at U6C pin 9, U6C pin 8 goes low, but U5A/U5B does not change state because U5B pin 3 is low. Signal at U6B has no effect because U2B  $\bar{Q}$  and U6B pin 4 are high.

U2B  $\bar{Q}$  is high NAND gates U6B and U6D are enabled. When signal at TP9 appears at U6D pin 13, U6D pin 11 goes low, but U5A/U5B does not change state because U5B pin 3 is low. Signal at pin 1 of U6A has no effect on the circuit because U2B pin 2 of U6A are low.

Two or more consecutive pulses from either input (TP5 or TP9) between pulses from the other input the sense circuit functions enable the phase detector until the frequency error is corrected.

Example of circuit operation assume that two pulses from TP9 (N3 signal) are received between two pulses from TP5 (N3 signal) indicating that the SL2 frequency is high. When the first pulse from TP5 is received U3A pin 3 goes low, U3B pin 6 goes high to set U2B. The clock pulse causes U2B Q to go high. When the second consecutive pulse is received from TP9 U6A has been enabled by the output of U2B. U6A pin 3 goes low and causes flip/flop U5B to change state. When the D input of U2A goes low the pulse causes U2A  $\bar{Q}$  to go low and inhibit U3A and U3D. If a SL2 signal is received prior to receipt of an N3 signal U6A pin 3 will go low but will have no effect on flip/flop U5A/U5B because U5A pin 13 is low.

If an N3 pulse is received U2B Q is still high and U6C pin 8 will not change the state of flip/flop U5A/U5B. When the D input to U2A goes low the clock pulse causes U2A  $\bar{Q}$  to go high and enable U3D. The propagation time of the signal through the sense circuit is long enough for the pulse from N3 (TP5) to have ended before U3D is enabled so the state of flip/flop U3B/U3C does not change.

The next pulse from SL2 will again cause U6A pin 3 to go low and change the state of flip/flop U5A/U5B. With the D input to U2A pin 13, the clock pulse again causes U2A  $\bar{Q}$  to go low and inhibit U3D. The signal applied to U3A has no effect on flip/flop U3C because U3B pin 5 is low.

The sense circuit continues operation in the manner described above until two consecutive N3 pulses are received between two SL2 signals. When this occurs the first pulse causes U6C pin 8 to go low changing the state of flip/flop U5A/U5B. With the D input to U2A pin 13, the clock pulse will cause U2A  $\bar{Q}$  to go high and enable U3A and U3D. Again, because of propagation time through the sense circuit

## SERVICE SHEET 13 (Cont'd)

the pulse will have ended before U3D is enabled. The second consecutive N3 pulse again causes U6C pin 8 to go low but, because U5B pin 3 is low, no change in state occurs in flip/flop U5A/U5B. Since U3D is now enabled, U3D pin 11 goes low and causes flip/flop U3B/U3C to change state. With the D input to U2B low, the clock pulse causes U2B Q output to go high. Phase lock has been achieved and the loop will remain locked as long as pulses at the same frequency appear alternately at TP5 and TP9.

When the SL2 frequency is low U2B Q is low. When the SL2 frequency is high U2B Q is high.

DC amplifier Q2, Q1, Q6 and associated components filter the Q output of U2B and applies it to a summing circuit in the A11 assembly to precisely control the voltage controlled oscillator.

## TEST PROCEDURE

**Test 1-a.** Connect the oscilloscope input to test points shown by composite waveform SS13-1. This composite waveform illustrates correct waveforms and timing relationships for the points tested. All signals are about 4 volts in amplitude.

## NOTE

The oscilloscope was triggered from TP1 for these tests.



Composite Waveform SS13-1

If the pulses are not present at TP2 proceed to test 1-b.

If the pulses are not present at TP3 proceed to test 1-c.

If the pulses are present at TP2 and TP3, but opposite polarity pulses are not present at TP5 and/or TP9, check the NAND gates between TP2 and TP5 or TP3 and TP9 as appropriate.

## SERVICE SHEET 13 (Cont'd)

If the positive-going pulses are present at TP5 and TP9, but negative-going pulses are not present at TP6 for each of the pulses, check NAND gates U1A, U1C, U1D and U5C as appropriate.

If the pulses are approximately as shown in the top five traces of composite waveform SS13-1 but there is no square wave at TP7, use the oscilloscope to check the signal at NAND gate U3B pin 6. The display should be the same as that shown for TP7. If the signal is present, U2B is probably defective.

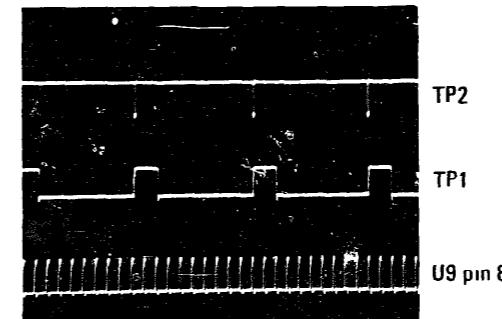
If the signal is not present at U3B pin 6 use the oscilloscope to check the signals at NAND gates U3D pin 11 and U3A pin 3. The signals should appear as they did at TP5 and TP9 except that they are inverted. If the signals are present U3B or U3C may be defective. If the signal is present at one of the NAND gate outputs but not at the other, replace U3.

If the signal is not present at U3D pin 11 or U3A pin 3, use the digital voltmeter to check the dc level at U2A pin 6. The dc level should be about +4 volts. If U2A pin 6 is at about +4 volts, U2 is defective.

If the +4 volts is not present at U2A pin 6, ground U2A pin 1. If the voltage at U2A pin 6 does not go to about +4 volts, U2 is defective.

If trouble still has not been found, connect the counter to TP3 and the digital voltmeter and the oscilloscope to NAND gate U5A pin 12. The counter readout should be about 210 kHz and U5A pin 12 should be low (about +60 millivolts). If the counter readout is lower or higher than 210 kHz and U5A pin 12 is high, slowly rotate A11R19 through its range while observing the counter and the oscilloscope. As the counter readout passes through the 210 kHz point the oscilloscope display should show a change in dc level, if it does not, U5 or U6 is probably defective.

**Test 1-b.** If there is no signal at TP2, or the signal is not approximately as shown in the top trace of composite waveform SS13-2, connect the oscilloscope first to TP1, then to U9 pin 8. TP1 and U9 pin 8 signals should be as shown in composite waveform SS13-2. All signal levels are about 4 volts.



Composite Waveform SS13-2

## SERVICE SHEET 13 (Cont'd)

If the positive-going pulses are present at TP5 and TP9, but negative-going pulses are not present at TP6 for each of the pulses, check NAND gates U1A, U1C, U1D and U5C as appropriate.

If the pulses are approximately as shown in the top five traces of composite waveform SS13-1 but there is no square wave at TP7, use the oscilloscope to check the signal at NAND gate U3B pin 6. The display should be the same as that shown for TP7. If the signal is present, U2B is probably defective.

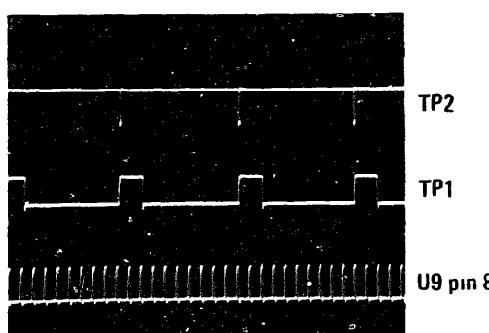
If the signal is not present at U3B pin 6 use the oscilloscope to check the signals at NAND gates U2D pin 11 and U3A pin 3. The signals should appear as they did at TP5 and TP9 except that they are inverted. If the signals are present U3B or U3C may be defective. If the signal is present at one of the NAND gate outputs but not at the other, replace U3.

If the signal is not present at U3D pin 11 or U3A pin 3, use the digital voltmeter to check the dc level at U2A pin 6. The dc level should be about +4 volts. If U2A pin 6 is at about +4 volts, U3 is defective.

If the +4 volts is not present at U2A pin 6, ground U2A pin 1. If the voltage at U2A pin 6 does not go to about +4 volts, U2 is defective.

If trouble still has not been found, connect the counter to TP3 and the digital voltmeter and the oscilloscope to NAND gate U5A pin 12. The counter readout should be about 210 kHz and U5A pin 12 should be low (about +60 millivolts). If the counter readout is lower or higher than 210 kHz and U5A pin 12 is high, slowly rotate A11R19 through its range while observing the counter and the oscilloscope. As the counter readout passes through the 210 kHz point the oscilloscope display should show a change in dc level; if it does not, U5 or U6 is probably defective.

**Test 1-b.** If there is no signal at TP2, or the signal is not approximately as shown in the top trace of composite waveform SS13-2, connect the oscilloscope first to TP1, then to U9 pin 8. TP1 and U9 pin 8 signals should be as shown in composite waveform SS13-2. All signal levels are about 4 volts.



Composite Waveform SS13-2

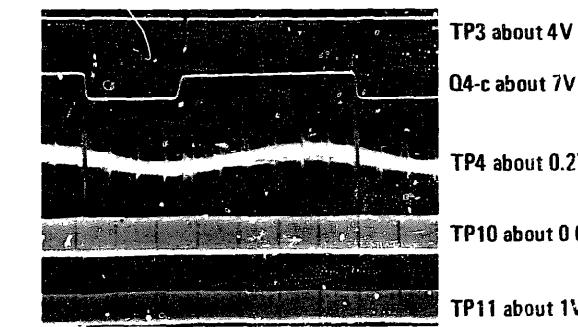
## SERVICE SHEET 13 (Cont'd)

If the signal is as shown at TP1, U7A or Q12 may be defective.

If the signal is as shown at U9 pin 8 but does not appear at TP1, U9 is probably defective.

If the signal does not appear at U9 pin 8 check the interconnections to the N3 loop and, if necessary, the N3 loop.

**Test 1-c.** If there is no signal at TP3, or the signal is not approximately as shown in the top trace of composite waveform SS13-3, connect the oscilloscope, in turn, to the points shown in composite waveform SS13-3.



Composite Waveform SS13-3

If the signal shown in the second trace from the top of composite waveform SS13-3 is not as shown check Q3, Q7, U4B, U4C and associated components.

If the signal does not appear at Q4-c but the signal at TP4 is present check Q5, Q4 and associated components.

If the signal is not present at TP4 check for signals shown at TP10 and TP11. If both signals are present mixer E1 is probably defective. If either TP10 or TP11 signals are not present, trouble is in the N2 Loop or the SL2 voltage controlled oscillator.

**Test 1-d.** To check operation of the dc amplifier connect the digital voltmeter to TP8 and rotate A11R19 through its range. The digital voltmeter readout should vary from about -1.5 volt to about +1.5 volt. If the voltage does not vary as A11R19 is adjusted, check Q2, Q1, Q6 and associated components.

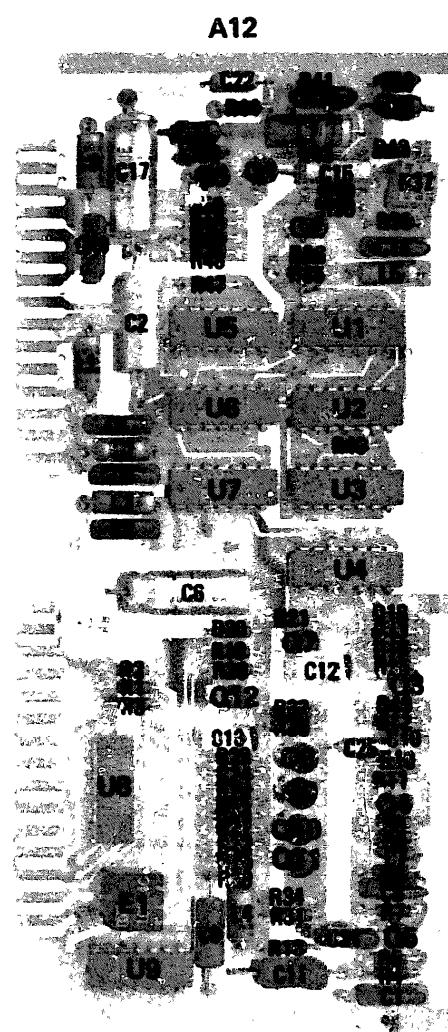


Figure 8-42. A12 SL2 Phase Detector Component Locations

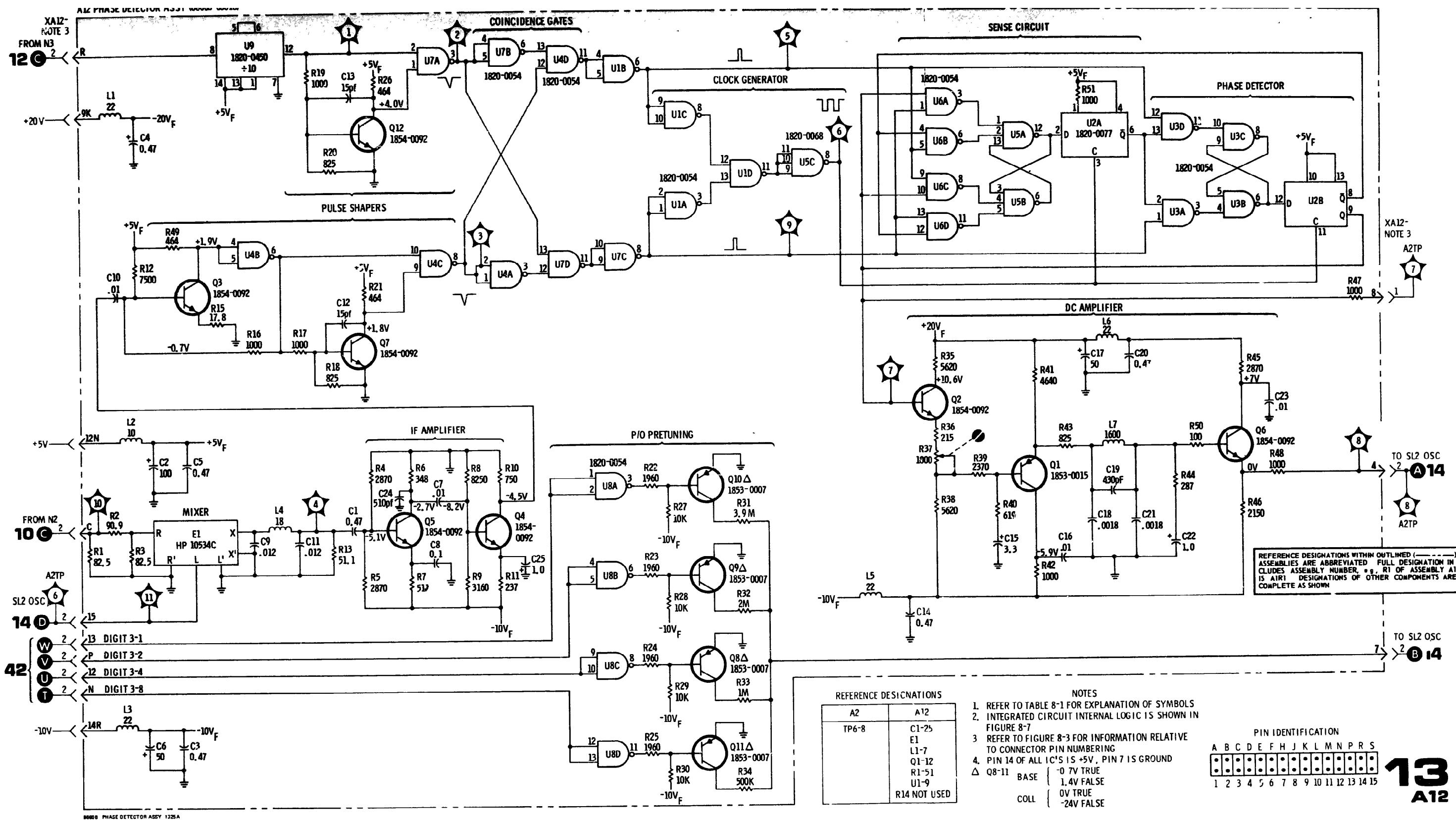


Figure 8-43. SL2 Phase Detector Schematic  
8-95

**13**  
**A12**

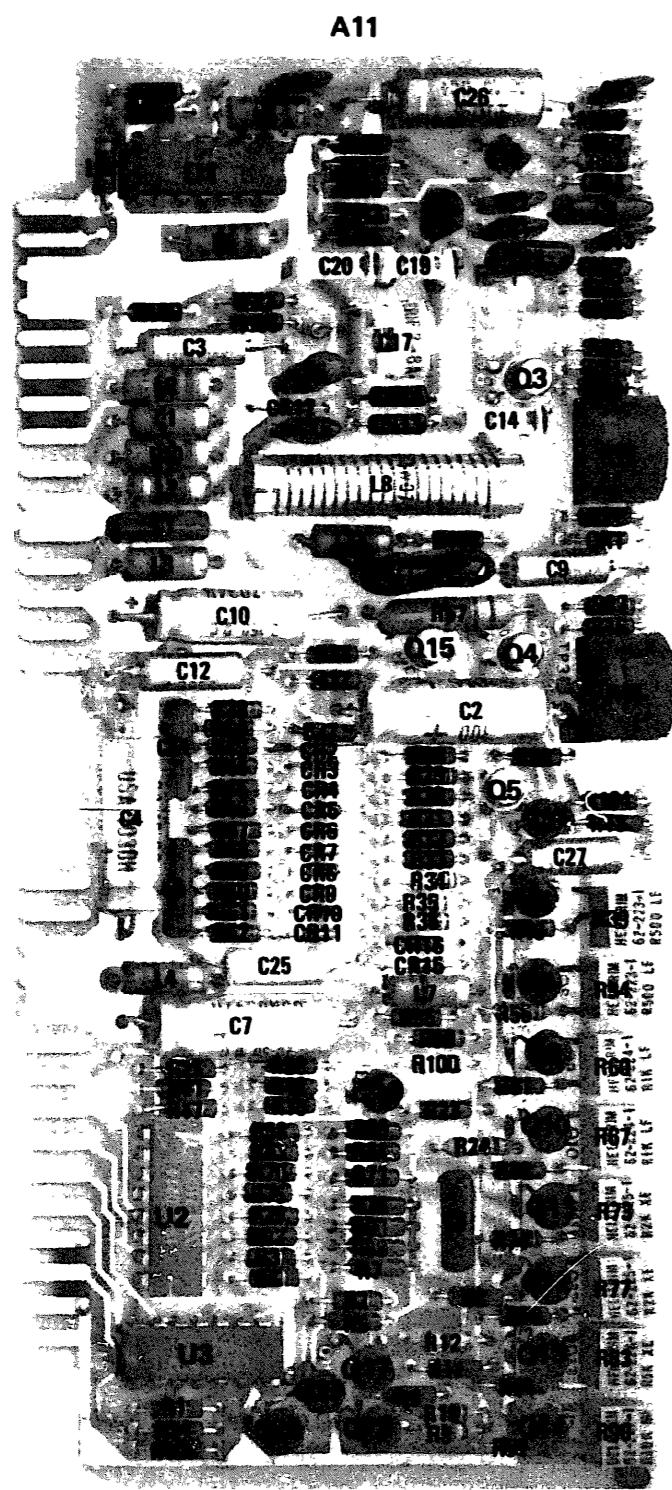
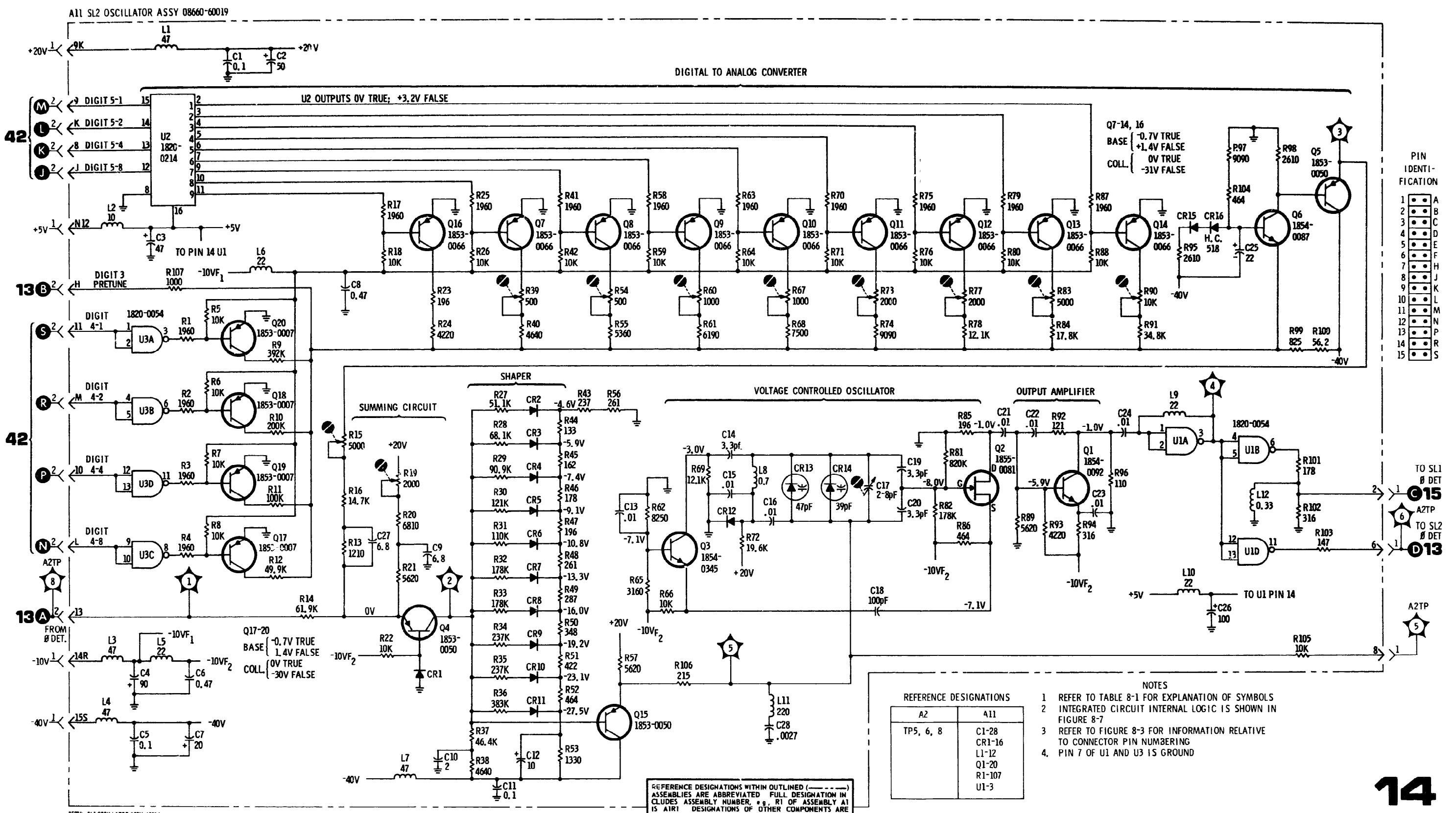


Figure 8-44. A11 SL2 VCO Component Locations



14

Figure 8-45. SL2 VCO Schematic

## SERVICE SHEET 15

### SUMMING LOOP 1 PHASE DETECTOR A15

Normally, causes of malfunctions in the Model 8660B will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A15 assembly, a part of the three-assembly SL1, is shown schematically and described on this Service Sheet. The SL1 Oscillator Assembly (A19) is shown schematically and described on Service Sheet 17. The SL1 Mixer and D/A Converter Assembly (A18) is shown schematically and described on Service Sheet 16.

When trouble has been isolated to the A15 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

#### NOTE

After making repairs to any part of the SL1 circuits the adjustment procedures in Section V paragraph 5-33 should be performed to ensure proper operation of the instrument.

#### TEST EQUIPMENT REQUIRED (See Table 1-3)

Oscilloscope (with 10: 1 divider probes)

Digital Voltmeter

Frequency Counter

#### SUMMING LOOP 1 GENERAL

The purpose of Summing Loop 1 (SL1) is to generate digitally controlled RF signals in the range of 20.000001 to 30.000000 MHz in selectable increments as low as 1 Hz. The SL1 voltage controlled oscillator is phase locked to the divided by one hundred output of the SL2 loop and the difference frequency of the N1 loop and the SL1 oscillator. The output of SL1 is applied to the RF Section plug-in.

#### ■ PHASE DETECTOR ASSEMBLY A15

There are two signal inputs to the phase detector assembly. One is the input from the SL2 loop which is shaped by U10D and divided by 100 by U6 and U5. The output of U5 is again shaped by Q5 and U4A to provide negative-going pulses at TP2. The other input to the phase detector is from the SL1 mixer and is the difference frequency between the N1 oscillator and the SL1 voltage controlled oscillator. Q6, U4B, Q4 and U4C shape the signal and provides negative-going pulses at TP3.

The pulse frequency at TP2 and TP3 varies (depending on programming) from 0.200001 to 0.300000 MHz. When the phase lock loop is locked the pulse frequency is the same at TP2 and TP3. The sampling ratio is 1:1.

U9A, U3B, U4D and U9B comprise coincidence gates which inhibit signals which appear simultaneously at TP2 and TP3. Normally, when signals are not present, TP2 and TP3 are both high.

When a signal appears at TP2, U9A pin 3 and U3B pin 4 go high. If there is no signal at TP3, U3B pin 5 is also high; U3B pin 6 goes low and U3C pin 8 goes high. The positive pulse at TP4 drives the clock generator and the sense circuit or the phase detector.

When a signal appears at TP3, U4D pin 11 and U9B pin 5 go high. If there is no signal at TP2, U9B pin 4 is also high; U9B pin 6 goes low and U9D pin 11 goes high. The positive pulse at TP8 drives the clock generator and the sense circuit or the phase detector.

When signals appear simultaneously at TP2 and TP3, U9B pin 4 and U3B pin 5 go low: U9B pin 6 and U3B pin 6 remain high and the signals cannot reach TP4 or TP8.

U7C, U9C, U3D and U3A comprise a clock generator which clocks U2A and U2B each time a signal appears at TP4 or TP8. With no signals present TP4 and TP8 are low. When a positive pulse appears at TP8, U9C pin 8 goes low, U3D pin 11 goes high and a negative-going pulse appears at TP5. When a positive pulse appears at TP4 operation of the circuit is the same except that U7C pin 8 (rather than U9C pin 8 goes low). Since a clock

#### SERVICE SHEET 15 (Cont'd)

pulse is generated for each input, the clock pulse frequency at TP5 is the sum of the pulse frequencies at TP4 and TP8. U2A and U2B are clocked by the positive-going trailing edge of the negative clock pulses.

Since the sense circuit does not function when the loop is locked, operation of the phase detector will be described first.

When the loop is phase locked U2A  $\bar{Q}$  is held high to enable U1A and U1B. Assume that initially U2B  $\bar{Q}$  is high U1D pin 11 is low and U1C pin 8 is high. When a positive pulse from TP8 appears at U1A pin 1, U1A pin 3 goes low and causes a change in state of flip/flop U1D/U1C: U1D pin 11 goes high and U1C pin 8 goes low. The high at U1D pin 11 sets the D input to U2B and the clock pulse causes U2B Q to go high. The following positive pulse at TP4 is applied to U1B pin 5, U1B pin 6 goes low and changes the state of flip/flop U1D/U1C. U1D pin 11 goes low and the clock pulse causes U2B  $\bar{Q}$  to again go high. This sequence continues as long as the pulses at TP4 and TP8 alternate.

The signals at TP4 and TP8 are applied to the sense circuit even when the loop is phase locked. They have no effect on the circuit because of the relationship between the Q and  $\bar{Q}$  outputs of U2B to the incoming signals.

When U2B is high, NAND gates U8A and U8C are enabled. When the signal from TP4 appears at U8C pin 9, U8C pin 8 goes low; flip/flop U7A/U7B does not change state because U7B pin 3 is low. The signal at U8B pin 4 has no effect because U2B  $\bar{Q}$  and U8B pin 5 are low.

When two or more consecutive pulses from either input (TP4 or TP8) occur between pulses from the other input, the sense circuits function to disable the phase detector until the frequency error has been corrected.

As an example of circuit operation, assume that two pulses from TP8 are received between two pulses from TP4, indicating that the SL1 frequency is too high. When the first pulse from TP8 is received U1A pin 3 goes low, U1D pin 11 goes high to set the D input to U2B and the clock pulse causes U2B Q to go high. When the second consecutive pulse is received from TP8, U8A has been enabled by the high Q output of U2B. U8A pin 3 goes low and causes flip/flop U7A/U7B to change state. When the D input to U2A goes high, the clock pulse causes U2A  $\bar{Q}$  to go low and inhibit NAND gates U1A and U1B. If a third pulse from TP8 is received prior to receipt of a signal from TP4, U8A pin 3 will again go low but will not affect flip/flop U7A/U7B because U7A pin 13 is low.

When a pulse is received from TP4, U2B Q is still high and U8C pin 8 will go low and change the state of flip/flop U7A/U7B. When the D input to U2A goes low the clock pulse will cause U2A  $\bar{Q}$  to go high and enable U1A and U1B. The propagation time of the signal through the sense circuit is long enough for the pulse from TP4 to have ended before U1B is enabled so the state of flip/flop U1D/U1C does not change.

The next pulse from TP8 will again cause U8A pin 3 to go low and change the state of flip/flop U7A/U7B. With the D input of U2A high again, the clock pulse causes U2A  $\bar{Q}$  to go low and inhibit U1A and U1B. The signal applied to U1A has no effect on flip/flop U1D/U1C because U1D pin 12 is low.

The sense circuit continues operation in the manner described above until two consecutive pulses are received at TP4 between two pulses at TP8. When this occurs the first pulse causes U8C pin 8 to go low and change the state of flip/flop U7A/U7B. With the D input to U2A low the clock pulse will cause U2A  $\bar{Q}$  to go high and enable NAND gates U1A and U1B. Because of the propagation time through the sense circuit, the pulse will have ended before U1B is enabled. The second consecutive pulse from TP4 again causes U8C pin 8 to go low, but because U7B pin 3 is now low, no change in state occurs in flip/flop U7A/U7B. Since U1B is enabled, U1B pin 6 goes low and causes flip/flop U1D/U1C to change state. With the D input of U2B low, the clock pulse will cause U2B  $\bar{Q}$  output to go high.

**SERVICE SHEET 15 (Cont'd)**

Phase lock has been achieved and the loop will remain locked as long as pulses at the same frequency are received alternately at TP4 and TP8.

When the SL1 frequency is too low, U2B Q is low. When the SL1 frequency is too high, U2B Q is high.

DC amplifier Q1, Q2, Q3 and associated components filter the Q output of U2B and applies it to a summing circuit in the A19 assembly to precisely control the voltage controlled oscillator.

**TEST PROCEDURE**

**Test 1-a.** Connect the oscilloscope input to test points shown by composite waveform SS15-1. This composite waveform illustrates correct waveforms and timing relationships for the points tested. All signals are about 4 volts in amplitude.

**NOTE**

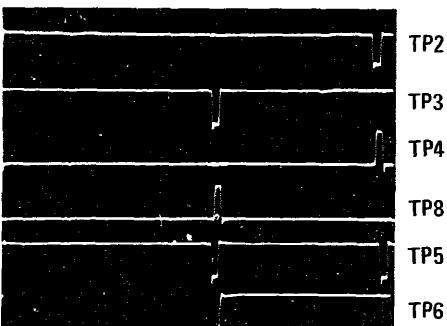
The oscilloscope was triggered from TP1 for all waveforms.

If the pulses are not present at TP2 proceed to test 1-b.

If the pulses are not present at TP3 proceed to test 1-c.

If the pulses are present at TP2 and TP3, but opposite polarity pulses are not present at TP4 and/or TP8, check the NAND gates between TP2 and TP4 or TP3 and TP8 as appropriate.

If the positive-going pulses are present at TP4 and TP8, but negative-going pulses are not present at TP5 for each of the pulses, check NAND gates U3A, U3D, U7C, and U9C as appropriate.



Composite Waveform SS15-1

If the pulses are approximately as shown in the top five traces of composite waveform SS15-1 but there is no square wave at TP6, use the oscilloscope to check the signal at NAND gate U1D pin 11. The display should be the same as that shown for TP6. If the signal is present, U2B is probably defective.

If the signal is not present at U1D pin 11 use the oscilloscope to check the signals at NAND gates U1A pin 3 and U1B pin 6. The signals should appear as they did at TP4 and TP8 except that they are inverted. If the signals are present, U1C or U1D may be defective. If the signal is present at one of the NAND gates but not at the other, replace U1.

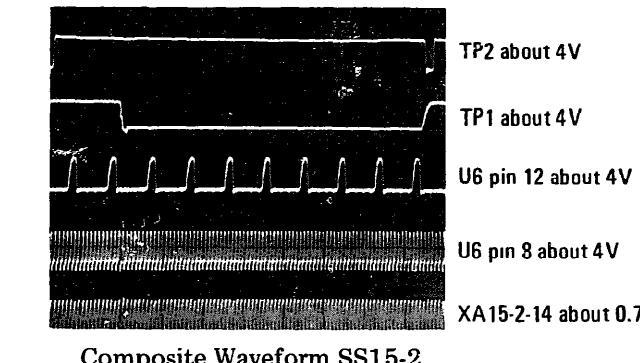
If the signal is not present at U1A pin 3 or U1B pin 6, use the digital voltmeter to check the dc level at U2A pin 6. If U2A pin 6 is about +4 volts, U1 is defective.

If the +4 volts is not present at U2A pin 6, ground U2A pin 1. If the voltage at U2A pin 6 does not go to about +4 volts, U2 is defective.

**SERVICE SHEET 15 (Cont'd)**

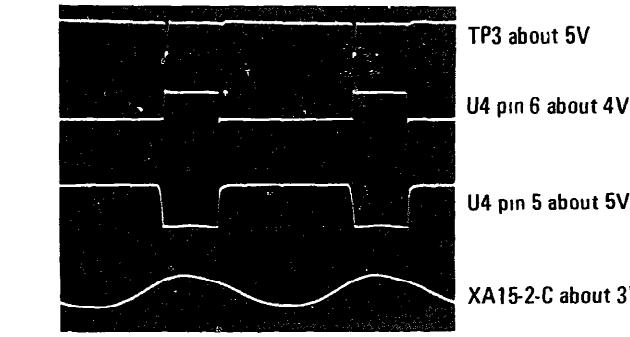
If the cause of trouble still has not been found, connect the counter to TP3 and the digital voltmeter and oscilloscope to NAND gate U7A pin 12. The counter readout should be about 300.000 kHz (center frequency set to zero) and U7A pin 12 should be low (about +70 millivolts). If the counter readout is lower or higher than 300 kHz and U5A pin 12 is high, slowly rotate A15R14 through its range while observing the counter and the oscilloscope. As the counter readout passes through the 300 kHz point the oscilloscope display should show a change in level; if it does not, U7 or U8 is probably defective.

**Test 1-b.** If there is no signal at TP2 or the signal is not approximately as shown in the top trace of composite waveform SS15-2, connect the oscilloscope first to TP2, then U6 pin 12, U6 pin 8 and finally to XA15-2-14. In making the checks in the order shown, the point at which the correct signal is first observed is followed by the defective circuit. If the signal is not present at XA15-2-14, check the interconnections to the SL2 loop and, if necessary, the SL2 loop.



Composite Waveform SS15-2

**Test 1-c.** If there is no signal at TP3 or the signal is not approximately as shown in the top trace of composite waveform SS15-3 connect the oscilloscope first to U4 pin 6, then to U4 pin 4 or 5 and finally to XA15-2-C.



Composite Waveform SS15-3

In making the checks in the order shown, the point at which the signal is first observed is followed by the defective circuit. If the signal is not present at XA15-2-C check the interconnections to the A18 assembly and, if necessary, the A18 assembly.

**Test 1-d.** To check operation of the dc amplifier connect the digital voltmeter to Q3-e, ground TP7, and rotate A15R14 through its range. The digital voltmeter readout should vary from about -1.5 volts to about +1.5 volts. If the voltage does not vary as A15R14 is adjusted, check Q1, Q2, Q3 and associated components.

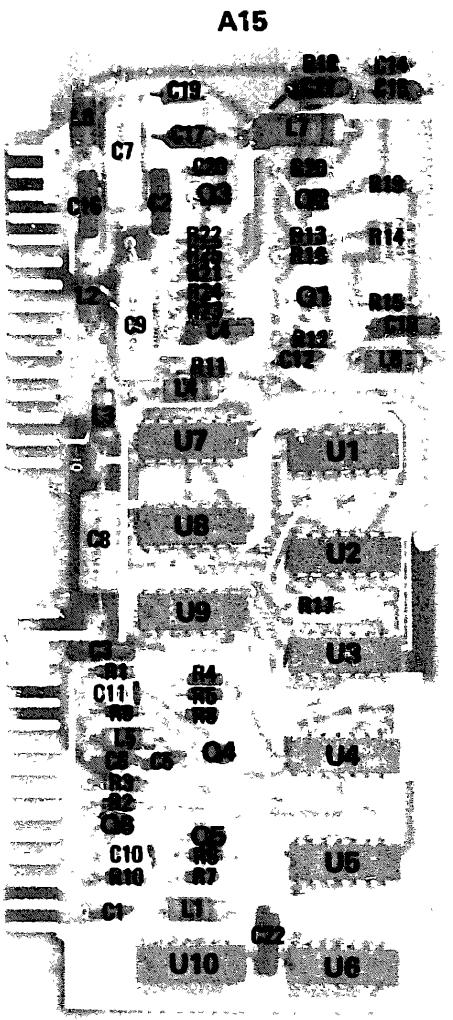


Figure 8-46. A1o SL1 Phase Detector Component Locations

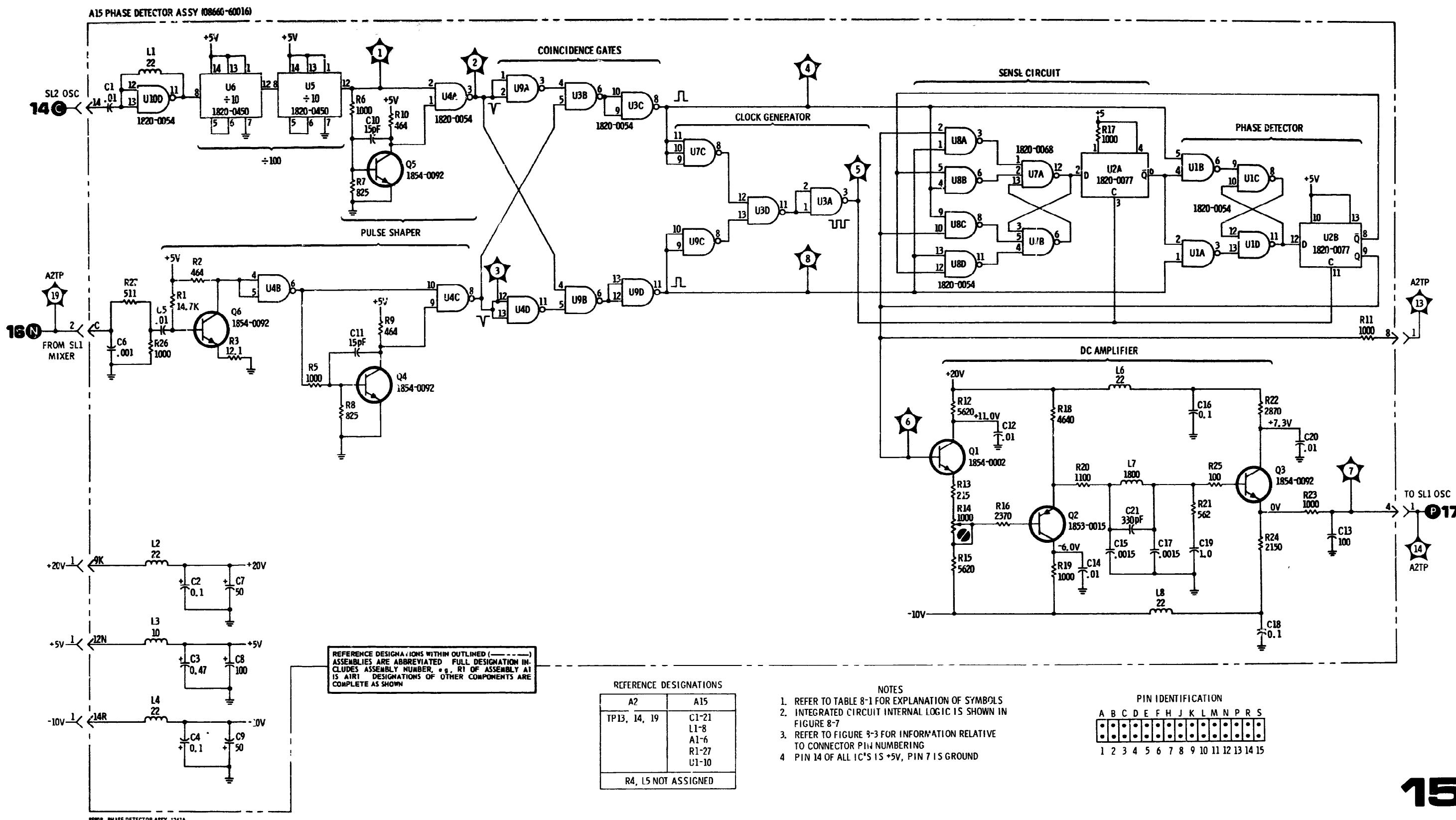


Figure 8-47 SL1 Phase Detector Schematic

## SERVICE SHEET 16

## SUMMING LOOP 1 MIXER AND D TO A CONVERTER A18

Normally, causes of malfunctions in the Model 8660B will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A18 assembly, a part of the three-assembly SL1, is shown schematically and described on this Service Sheet. The SL1 Phase Detector Assembly (A15) is shown schematically and described on Service Sheet 15. The SL1 Oscillator Assembly (A19) is shown schematically and described on Service Sheet 17.

When trouble has been isolated to the A18 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the SL1 circuits the adjustment procedures in Section V paragraph 5-33 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-3)

Oscilloscope (with 10:1 divider probes)  
Digital Voltmeter  
Frequency Counter

## SUMMING LOOP 1 GENERAL

The purpose of Summing Loop 1 (SL1) is to generate digitally controlled RF signals in the range of 20.000001 to 30.000000 MHz in selectable increments as low as 1 Hz. The SL1 voltage controlled oscillator is phase locked to the divided by one hundred output of the SL2 loop and the difference frequency of the N1 loop and the SL1 oscillator. The output of SL1 is applied to the RF Section output plug-in.

## 1 MIXER AND AMPLIFIERS

E1 is a double balanced mixer which mixes the output of the SL1 voltage controlled oscillator with the output of the N1 loop and provides an output which is the difference frequency of the two inputs.

Q14 and Q1 amplify the input from the SL1 voltage controlled oscillator.

Q2, Q15, Q18 and associated components amplify the output from the mixer before applying it to the phase detector circuit in the A15 assembly.

## TEST PROCEDURE 1

**Test 1-a.** With the center frequency set to zero use the counter and the oscilloscope to check for the following (approximately sine wave) signals.

TP5 300.000 kHz at about 4 volts p/p  
TP4 (oscilloscope only) 300 kHz at about 0.1 volt p/p  
TP3 29.700000 MHz at about 0.5 volt p/p  
Q1-e 30.000000 MHz at about 1.1 volt p/p  
TP2 30.000000 MHz at about 0.5 volts p/p

## SERVICE SHEET 16 (Cont'd)

## 2 DIGITAL TO ANALOG CONVERTER

U3 is a decoder which converts the BCD inputs from digit 7 to an output that will turn on one of nine transistors in a resistive network. Quad NAND gates U2 and U1 turn on one or more transistors connected to their outputs in a resistive network. U2 and U1 are controlled by digits 6 and 5 respectively.

The current flow through Q4 and the bias for Q3 is determined by which of the transistors in the resistive network are saturated. The dc level at TP1 is determined by which transistors are on. This dc level is applied to a summing circuit in the A19 assembly and used to roughly pre-tune the voltage controlled oscillator. When the BCD input is 000 the dc level at TP1 is about -25 volts. When the BCD input is 999 the dc level is about -5 volts.

## TEST PROCEDURE 2

**Test 2-a.** Connect the digital voltmeter to TP1 and the counter to TP5. Refer to Table 8-33 for CF settings, counter readouts, and approximate voltage levels.

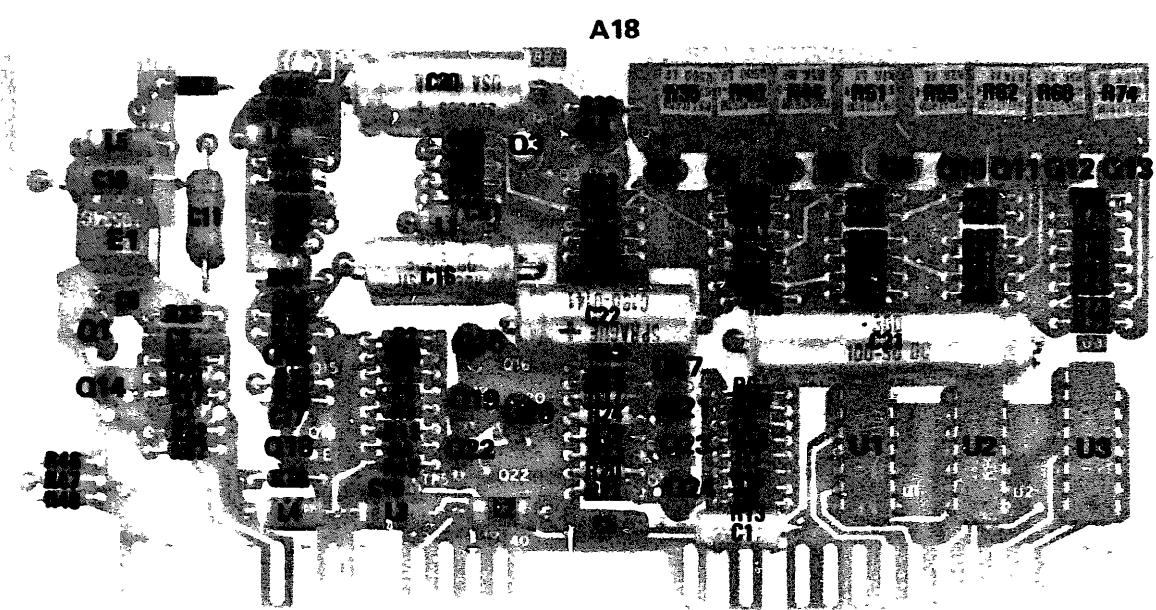
## NOTE

The voltage readings are typical and may vary greatly from that shown due to differences in varactor characteristics. The important point to note is the ratio of change as the center frequency is changed.

If the voltage ratio changes about as shown but the frequency requirements are not met, trouble is probably in the oscillator assembly or the phase detector assembly.

Table 8-33. SL1 Frequency Versus Voltage Chart

Center Frequency	Frequency TP5	Voltage TP1
0000000 Hz	300.000 kHz	-25.5 V
1110000 Hz	290.000 kHz	-23.4 V
2220000 Hz	280.000 kHz	-21.0 V
3330000 Hz	270.000 kHz	-18.8 V
4440000 Hz	260.000 kHz	-16.6 V
5550000 Hz	250.000 kHz	-14.3 V
6660000 Hz	240.000 kHz	-12.1 V
7770000 Hz	230.000 kHz	-9.9 V
8880000 Hz	220.000 kHz	-7.7 V
9990000 Hz	210.000 kHz	-5.4 V
9999999 Hz	200.000 kHz	-5.4 V



*Figure 8-48. A18 SL1 Mixer and D/A Converter Component Locations*

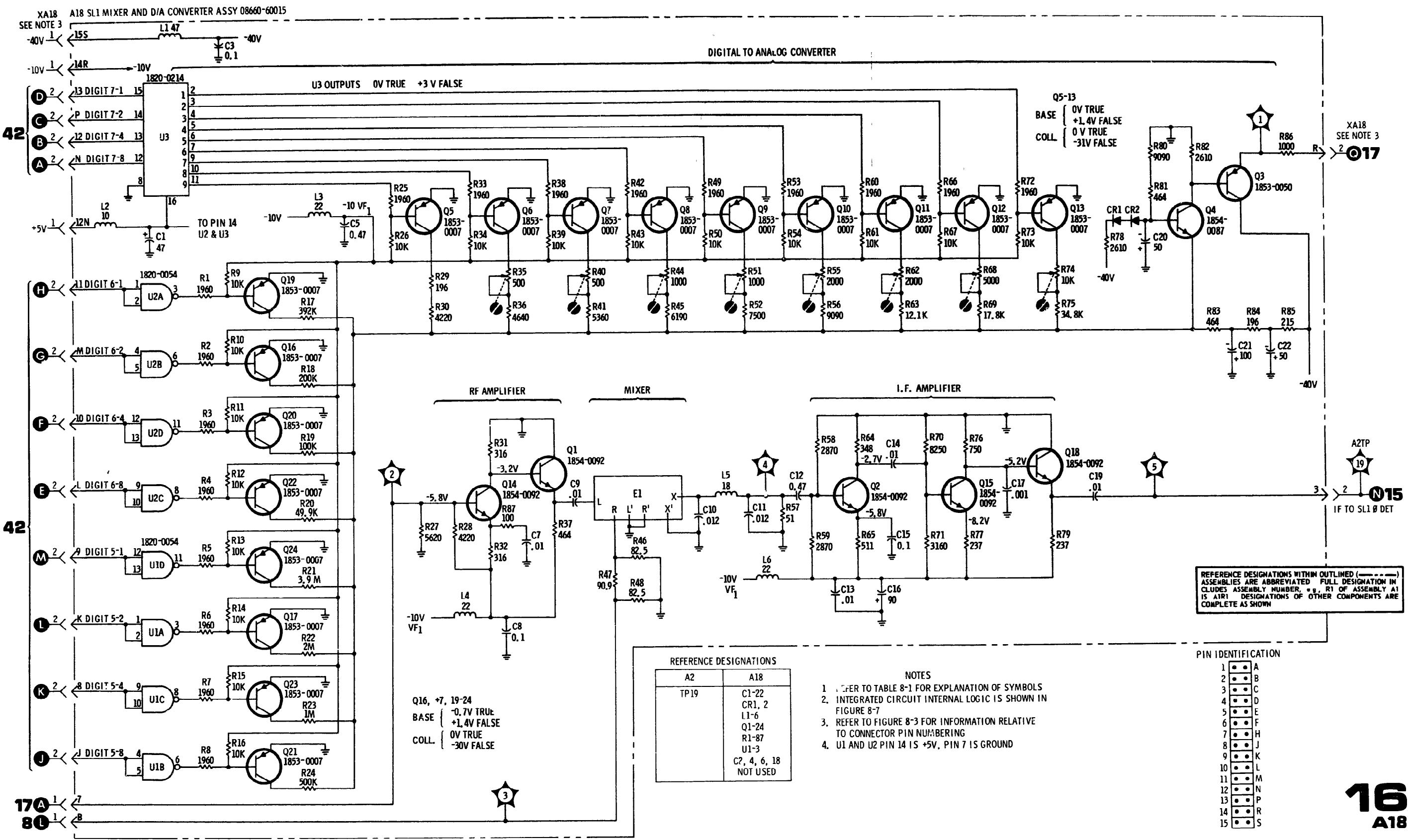


Figure 8-49. SL1 Mixer and D/A Converter Schematic

## SERVICE SHEET 17 (Cont'd)

CR1 through CR10 and associated resistors are used to shape the voltage curve applied to the voltage controlled oscillator tuning varactors to ensure that frequency change is linear with voltage change. The voltage at the junction of R32 and R39 is about -27.5 volts. When all BCD input to the A18 assembly are low, Q6-c is about -30 volts and all of the diodes in the shaper are reverse biased. As the voltage from the digital to analog converter decreases (gets closer to -5 volts) current through Q6 increases and the Q6 collector voltage decreases. As the Q6-c voltage decreases first CR10, then CR9, etc. are forward biased. As the diodes are forward biased resistors are added in parallel with R35 and R38 to shape the voltage curve to the varactors. Q7 provides a low impedance output to drive the varactors.

## TEST PROCEDURE 1

**Test 1-a.** Connect the digital voltmeter to TP1 and set the center frequency as shown in Table 8-34.

## NOTE

The voltage readings are typical and may vary greatly from that shown due to differences in varactor characteristics. The important point to note is the ratio of change as the center frequency is changed.

If the voltage at TP1 does not change as the CF are changed check the input from the digital to analog converter (A18) at XA19-2-J. If the voltage levels at this point do not change as the CF is changed, trouble is probably in the A18 assembly.

If the voltage level from the digital to analog converter does change, but the level at TP1 does not, check Q6, Q7 and associated components.

## 2 VOLTAGE CONTROLLED OSCILLATOR AND AMPLIFIERS

Q5, Q4 and associated components comprise a voltage controlled oscillator. C17, C20 and C21 provide isolation for the dc levels required to bias the varactors. C19 provides the feedback necessary to sustain oscillation. The resonant tank circuit is coupled to Q4 by capacitive divider C20 and C21. The FET acts as a source follower in the feedback circuit; it provides a high impedance at the gate and a low impedance at the source.

Q3 is a power splitter which drives two two-stage amplifiers. One amplifier output is applied to the RF Section plug-in and the other is applied to the mixer in the A18 assembly.

## TEST PROCEDURE 2

**Test 2-a.** Connect the oscilloscope to TP3 then to TP4. The sine wave at both test points should be about 0.3 volts p/p.

## SERVICE SHEET 17 (Cont'd)

If the signal is not present at either TP3 or TP4 connect the oscilloscope to Q3-b. The signal level should be about 0.2 volts p/p. If the signal is present at Q3-b but was not present at TP3 or TP4, Q3 is probably defective. If the signal is not present at Q3-b, check Q5, Q4 and associated components.

**Test 2-b.** Connect the counter to TP3 or TP4 and check for correct frequencies at the CF shown in Table 8-34.

Table 8-34 Varactor Bias Versus Frequency SL1

Center Frequency	Frequency TP3 or TP4	Voltage TP1
0000000 Hz	30.000000 MHz	-30.7 V
1110000 Hz	28.890000 MHz	-25.3 V
2220000 Hz	27.780000 MHz	-21.2 V
3330000 Hz	26.670000 MHz	-17.2 V
4440000 Hz	25.560000 MHz	-13.4 V
5550000 Hz	24.450000 MHz	-10.6 V
6660000 Hz	23.340000 MHz	-8.2 V
7770000 Hz	22.230000 MHz	-6.3 V
8880000 Hz	21.120000 MHz	-4.7 V
9990000 Hz	20.010000 MHz	-3.3 V
9999999 Hz	20.000001 MHz	-3.2 V

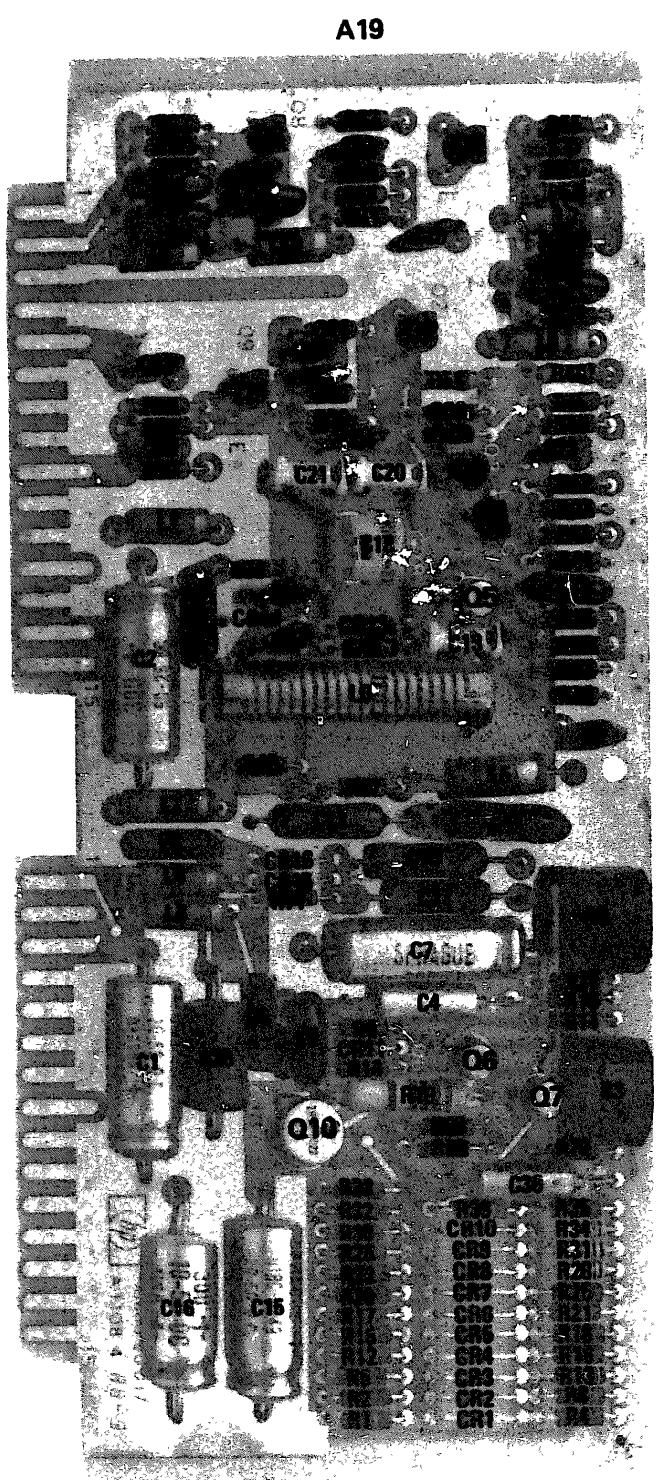


Figure 8-50. A19 SL1 VCO Component Locations

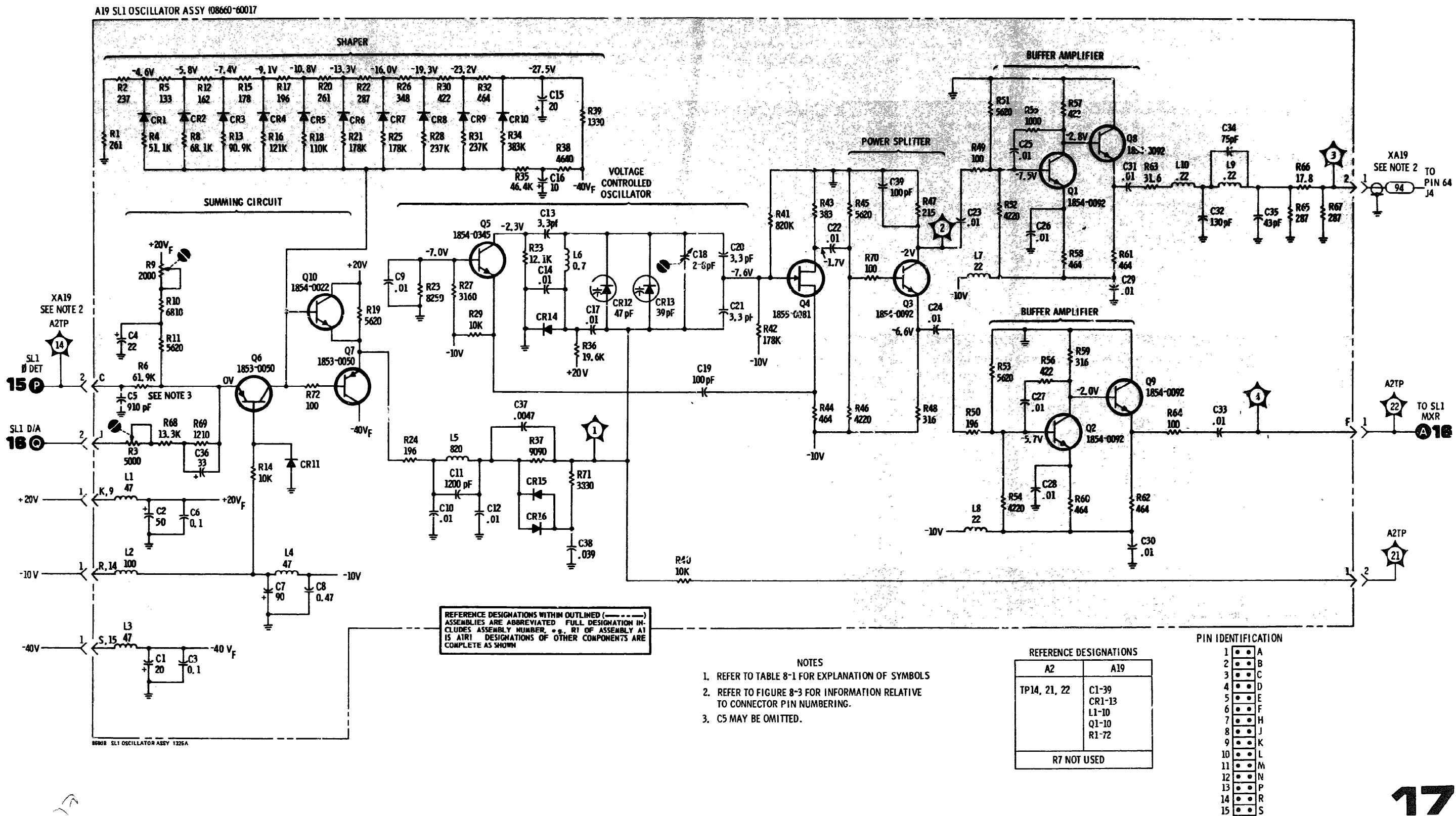


Figure 8-51. SL1 VCO Schematic

## SERVICE SHEET 18

### DCU BLOCK DIAGRAM

#### GENERAL

The DCU (Digital Control Unit) controls all functions of the mainframe in the local mode of operation. In addition, in the remote mode of operation, the DCU displays the selected center frequency (CF) and processes the programming data to control all functions of the mainframe and the plug-in sections.

The DCU is a bus oriented system with three major buses.

All of the data from the keyboard shift register (KYBD SR), the Arithmetic Logic Unit (ALU) and the CF register is routed through the T bus to their destination(s).

The R bus couples the outputs of the CF, A and M registers to the ALU on command.

The S bus couples the outputs of the step and sweep width registers, and the output of a read-only-memory (ROM) to the ALU on command.

The following information describes, in general terms, the overall operation of the various functions of the DCU. More detailed information to the circuit level appears on the foldout page opposing the schematic diagrams of the individual circuits.

#### KEYBOARD

The keyboard (KYBD) assembly consists of 20 non-contacting keys and a circuit board containing 20 printed circuit transformers. The transformer secondaries are series connected and the primaries are connected in series pairs. The transformer windings in each pair are oppositely paired. Each pair of the transformers are controlled by one numeral (0-9) key and one function (D.P., CF, MHz, etc.) key. A 100 kHz clock controls scanning of the transformer pairs.

When a key is pressed, a spring loaded, metal disc closely coupled to the transformer changes the mutual inductance between the primary and secondary of the corresponding transformer. The key detect and encode circuit in the A1A2 keyboard control assembly then determines which key of the pair has been pressed.

The keyboard is shown schematically on Service Sheet 21.

#### KEYBOARD CONTROL ASSEMBLY

**Key Detect and Encode.** The keyboard control assembly provides a train of 100 kHz pulses to the ten key-pair transformers on the keyboard. The keyboard pairs are strobed successively in the scanning process. When a key is pressed the scanning is stopped until the key is released.

During the period of time that scanning is stopped, the key detect and encode circuit determines which key of the pair has

## SERVICE SHEET 18 (Cont'd)

been pressed and furnishes outputs to MPX I (multiplexer I) or to the qualifier select circuits on the A1A4 assembly. Numerical information goes to MPX I and all other information goes to A1A4.

**Keyboard Register and Multiplexers.** In order to simplify the following discussion the multiplexers in the keyboard control assembly are referred to as MPX I, MPX II and MPX III. Each of the multiplexers has four-line inputs to points labeled I<sub>0</sub> and I<sub>1</sub>. The input to be used is determined by the level at the I<sub>S</sub> selector line, i.e., a high level, logic 1, would select the I<sub>1</sub> inputs.

In the local mode, K<sub>0</sub> register and the KYBD SR function as a four-bit, eleven digit, recirculating shift register. The purpose of recirculating the BCD information is to ensure that when all data is stored in the KYBD SR, the least significant digit is stored in a position to be the first digit shifted out of the register.

Operation of the circuit is as follows (example entry is 12.345678 MHz); KYBD key 1 is pressed first and the BCD information (0001) is coupled through MPX I to be stored in K<sub>0</sub>. The KYBD SR is then clocked by a burst of ten clock pulses and the BCD information is shifted to the least significant digit position in the KYBD SR.

The second KYBD entry, a 2 (0010) is clocked into K<sub>0</sub>. A burst of ten clock pulses again transfers the K<sub>0</sub> data to the least significant digit of the KYBD SR. Now, however, there is an input to MPX I, I<sub>1</sub>, which is clocked into K<sub>0</sub>; this entry, BCD 0001, follows the BCD 0010 information through to the KYBD SR. When the burst of ten clock pulses ends, the BCD 0010 data is stored in the KYBD SR least significant storage and the BCD 0001 data is stored in the next least significant digit storage.

The third keyboard entry, for the example used, is a decimal point (DP) which does not directly affect the KYBD SR. The DP information is applied to the qualifier select circuit in the A1A4 assembly.

The fourth keyboard entry, for the example used, a 3 (0011) is processed in the same manner as the first and second entries. At the end of the burst of ten clock pulses the information stored in the KYBD SR is 0000000123.

#### NOTE

If the KYBD pushbutton is now pressed the CF readout will display 12.3.

The remaining keyboard entries are processed in the same manner as entries 1, 2 and 4. When all information has been entered the KYBD SR data will be 0012345678. If the KYBD pushbutton is pressed the CF readout will display 12.345678.

## SERVICE SHEET 18 (Cont'd)

The last keyboard entry (in the example an 8, BCD1000), will be the first digit clocked out when the data is transferred to another shift register.

When information is clocked out of the KYBD SR it is also recirculated through MPX III and clocked back into the KYBD SR. In the local mode the information is retained in the KYBD SR until the keyboard is cleared or a new data entry is made.

In the remote mode, MPX III I<sub>0</sub> inputs are enabled by the RMT CMND-L line which goes low on command. Information from the mainframe interface circuits is applied to MPX III I<sub>0</sub> inputs with the least significant digit first. Data is entered in the KYBD SR until all required data is entered.

It should be noted that when the information in the KYBD SR is clocked out in the remote mode, it is again coupled back to MPX I and MPX III. This feedback is coupled through MPX I to K<sub>0</sub> but cannot affect the KYBD SR because MPX II I<sub>1</sub> is selected. Since MPX III I<sub>S</sub> is low only when remote data is being programmed in from an external source, the feedback flows through MPX III and MPX II to recirculate the information in the KYBD SR. When the data is stored in a final register the KYBD SR is cleared.

The output from the KYBD SR is applied to the A1A6 register assembly.

Refer to Service Sheets 19 and 20 for more detailed information regarding these circuits.

#### REGISTER ASSEMBLY

The A1A6 assembly contains the CF, STEP, SWEEP WIDTH and M registers.

The data inputs to the A1A6 assembly consist of inputs from the KYBD SR and the ALU. Most instructions are received from the A1A5 ROM output assembly.

The BCD inputs from the KYBD SR are applied to two sets of gates. If these BCD inputs are data inputs for the plug-in sections, the gates are enabled by the input ST01-H, and the data is transferred to the appropriate register in the addressed plug-in section.

If the information stored in the KYBD SR is not for the plug-in sections, gates may be enabled by KTT-H to couple the information to the T bus. Simultaneously, the information on the T bus is clocked into one, or more, of the shift registers on the A1A3 or A1A9 assembly as well as the A1A6 assembly.

Most of the registers are preceded by multiplexers. These multiplexers may be an integral part of the register integrated circuit or a separate integrated circuit.

When new information is present on the T bus, one set of multiplex gates is enabled to couple the information to the

## SERVICE SHEET 18 (Cont'd)

register. When information is being clocked out of a register, the other set of multiplexer gates are enabled to recirculate the information to the register. This ensures that register information is retained for future use without re-programming.

*Center Frequency (CF) Register*

The CF register is the only register that feeds its output back to the T bus. This output to the T bus, which is coupled through gates enabled by CTT-H occurs when:

1. Entry of an out-of-range frequency has been attempted (state 3/8).
2. A frequency increment (STEP) has been added to or subtracted from, the center frequency (state 2/7).
3. The instrument has been switched from the sweep mode to the fixed frequency mode (state 2/9).
4. The readout is to display CF again after the readout has been used to display KYBD, STEP, or SWP WIDTH (state 1/8).

Refer to Service Sheet 29 for more detailed information about the CF register.

*Step Register*

Any frequency (within the range of the RF Section in use) may be stored in the step register and added to, or subtracted from, the center frequency by the ALU. Since the step register is a recirculating register, the stored information may be used as many times as desired.

Refer to Service Sheet 30 for more detailed information about the step register.

*Sweep Width Register*

Any sweep width within the range of the RF Section in use may be stored in the sweep width register. In the sweep mode the sweep width is centered on the center frequency. Example; CF 50 MHz, SWP WIDTH 50 MHz, RF output is swept from 25 to 75 MHz.

Refer to Service Sheet 30 for more detailed information about the sweep width register.

*M Register and Limit*

When CF data from the KYBD SR is first clocked to the T bus it is applied only to the M register. The M register and the frequency limits decoder then determine if the programmed frequency is within the limits of the RF Section in use.

The M register is a six digit register. Only the six most significant digits are required for limit detection.

## SERVICE SHEET 18 (Cont'd)

The frequency limits decoder, in addition to the BCD inputs from the M register has MAIN L and 13GL inputs. The MAIN L and 13GL inputs are decoded inputs from the RF Section plug-in which are used to select the frequency limits.

The frequency limits decoder controls operation of the OUT OF RNG lamp and also provides Code 1 and Code 2 dc levels to the RF Section power amplifiers to operate two transistor switches to change the response time for output leveling.

The gate enabled by MTR is not used in the present equipment configuration. It is provided for possible future use.

After the M register and the frequency limits decoder have determined that the CF data is valid, the KYBD SR data is again clocked via the T bus into the CF, readout (RO) and A registers. The data is then clocked from the A register through the ALU via the R bus to the T bus and to A1A10, the output register.

Refer to Service Sheet 31 for a more detailed description of the M register and frequency limits circuit.

**ARITHMETIC LOGIC UNIT (ALU)**

The ALU, as the name implies, arithmetically manipulates the inputs from the other registers. The ALU may add, subtract, or allow the data to flow through without change. It also has a ROM (read-only-memory) which contains incrementing numbers used for the manual tune operation. The ROM may be used to cause the selected center frequency to be offset by any frequency within the range of the RF Section in use.

**NOTE**

Offset is a special option. The frequency offset must be specified, and the ROM programmed at the factory.

Refer to Service Sheet 32 for a more complete description of the ALU circuits.

**OUTPUT REGISTER**

The output register converts the serial BCD data from the T bus to parallel BCD data. This is referred to as parallel dump. The advantage of parallel dump over serial dump is that only those mainframe phase lock loops which are programmed for a different rf output lose phase lock. This improves switching time and avoids generation of unwanted frequencies.

Refer to Service Sheet 35 for a more detailed explanation of the output register circuit.

**SWEEP COUNT ASSEMBLY**

Shown directly under the ALU block is the sweep count assembly. The major function of this assembly is to keep track of the number of steps which have been taken in the sweep

**SERVICE SHEET 18 (Cont'd)**

The frequency limits decoder, in addition to the BCD inputs from the M register has MAIN L and 13GL input's. The MAIN L and 13GL inputs are decoded inputs from the RF Section plug-in which are used to select the frequency limits.

The frequency limits decoder controls operation of the OUT OF RNG lamp and also provides Code 1 and Code 2 dc levels to the RF Section power amplifiers to operate two transistor switches to change the response time for output leveling.

The gate enabled by MTR is not used in the present equipment configuration. It is provided for possible future use.

After the M register and the frequency limits decoder have determined that the CF data is valid, the KYBD SR data is again clocked via the T bus into the CF, readout (RO) and A registers. The data is then clocked from the A register through the ALU via the R bus to the T bus and to A1A10, the output register.

Refer to Service Sheet 31 for a more detailed description of the M register and frequency limits circuit.

**ARITHMETIC LOGIC UNIT (ALU)**

The ALU, as the name implies, arithmetically manipulates the inputs from the other registers. The ALU may add, subtract, or allow the data to flow through without change. It also has a ROM (read-only-memory) which contains incrementing numbers used for the manual tune operation. The ROM may be used to cause the selected center frequency to be offset by any frequency within the range of the RF Section in use.

**NOTE**

Offset is a special option. The frequency offset must be specified, and the ROM programmed at the factory.

Refer to Service Sheet 32 for a more complete description of the ALU circuits.

**OUTPUT REGISTER**

The output register converts the serial BCD data from the T bus to parallel BCD data. This is referred to as parallel dump. The advantage of parallel dump over serial dump is that only those mainframe phase lock loops which are programmed for a different rf output lose phase lock. This improves switching time and avoids generation of unwanted frequencies.

Refer to Service Sheet 35 for a more detailed explanation of the output register circuit.

**SWEEP COUNT ASSEMBLY**

Shown directly under the ALU block is the sweep count assembly. The major function of this assembly is to keep track of the number of steps which have been taken in the sweep

**SERVICE SHEET 18 (Cont'd)**

operation. The three UP/DN counters have the capability of counting to 1000 steps. When the sweep is set to 100 steps the first UP/DN counter is bypassed and the count is 100.

When the sweep mode is selected, the sweep always starts at the center frequency. In the AUTO mode the frequency steps are always to a higher frequency. When the upper limit of the sweep range is reached, the sweep starts at the lower limit of the range and is stepped up in frequency until the upper limit is again reached.

In the manual (MAN) sweep mode the sweep may be stepped either up or down by use of the manual tuning control.

The D/A (digital to analog) output (0 to +8V) may be used as an input to X-Y recorders, oscilloscopes, etc.

For more complete details about the sweep count assembly refer to Service Sheet 33.

**SWITCH CONTROL ASSEMBLY**

The switch control assembly is shown at the far left side of the block diagram. This assembly provides six clocks for use in various parts of the DCU. It also generates and stores qualifiers for all of the front panel controls except the keyboard numbers.

For a more complete description of the switch control assembly refer to Service Sheets 19 and 20.

**ROM INPUT AND ROM OUTPUT ASSEMBLIES**

The outputs of the seven state flip-flops control the qualifier select and seven of the address bits of the ROMs. When the eighth address bit is provided to the ROMs, the seven state flip/flops are set to the next state by the outputs of ROMs 1 and 2. ROM 2 also provides 1 output instruction and ROM 3 provides 4 output instructions.

Circuits are also provided to manually clock (single step) the DCU. When this feature is used, light emitting diodes verify the machine state.

**NOTE**

The term 'machine state' refers to a given set of conditions at a given point in

time. These states are shown in logical succession on the Algorithmic State Machine (ASM) Flow Chart on the last foldout sheet of this manual.

For a more complete description of circuit operation refer to Service Sheet 26.

The box labeled qualifier select in the ROM input assembly is shown schematically on Service Sheet 25. Multiple devices form a large selector circuit providing one output selected from 36 qualifier inputs. Seven inputs from the seven state flip-flops control the selection. The single output provides the eighth address bit to ROMs 1, 2 and 3.

For a more detailed description of circuit operation refer to Service Sheet 25.

The ROM output assembly contains a clock burst control which selects the number of pulses in the clock train, and a state decoder which converts the coded outputs of the seven state flip-flops to instructions.

For a more detailed description of the circuits refer to Service Sheets 27 and 28.

**READOUT CONTROL ASSEMBLY**

The major function of the A1A3 readout control assembly is to justify (position) the decimal point in the readout. The assembly also contains a 10 digit readout register which controls the ROMs in the readout assembly. Blanking of the leading zeros, and scanning of the register for the readout assembly is also provided.

For a more detailed description of the circuits in the readout control assembly refer to Service Sheets 23 and 24.

**READOUT ASSEMBLY**

The readout assembly contains two side by side solid state readouts. One is a 6 digit readout (least significant digits) and the other is a four digit readout. The most significant digit is controlled by a transistor switch. All other digits are scanned at a 10 kHz rate.

For a more complete description of the readout assembly circuits refer to Service Sheet 36

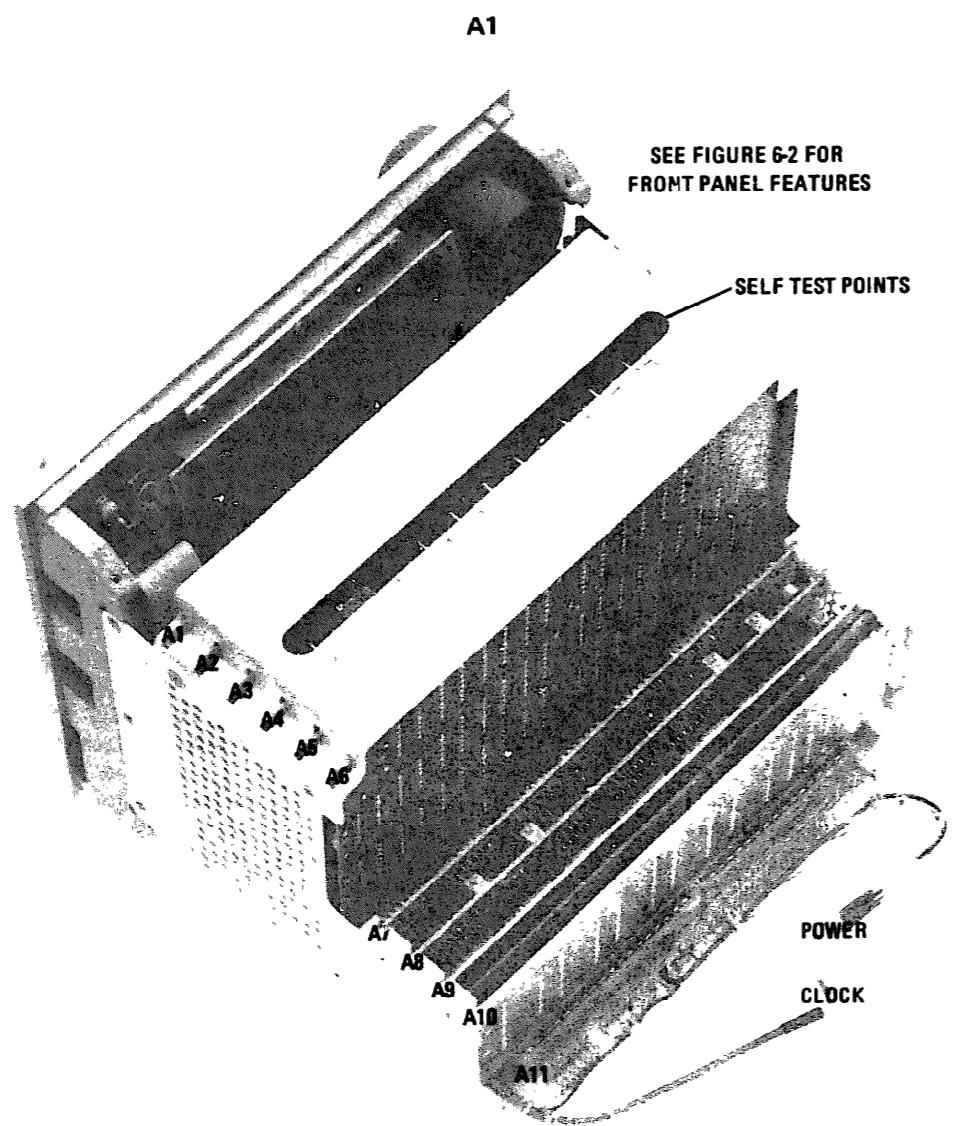
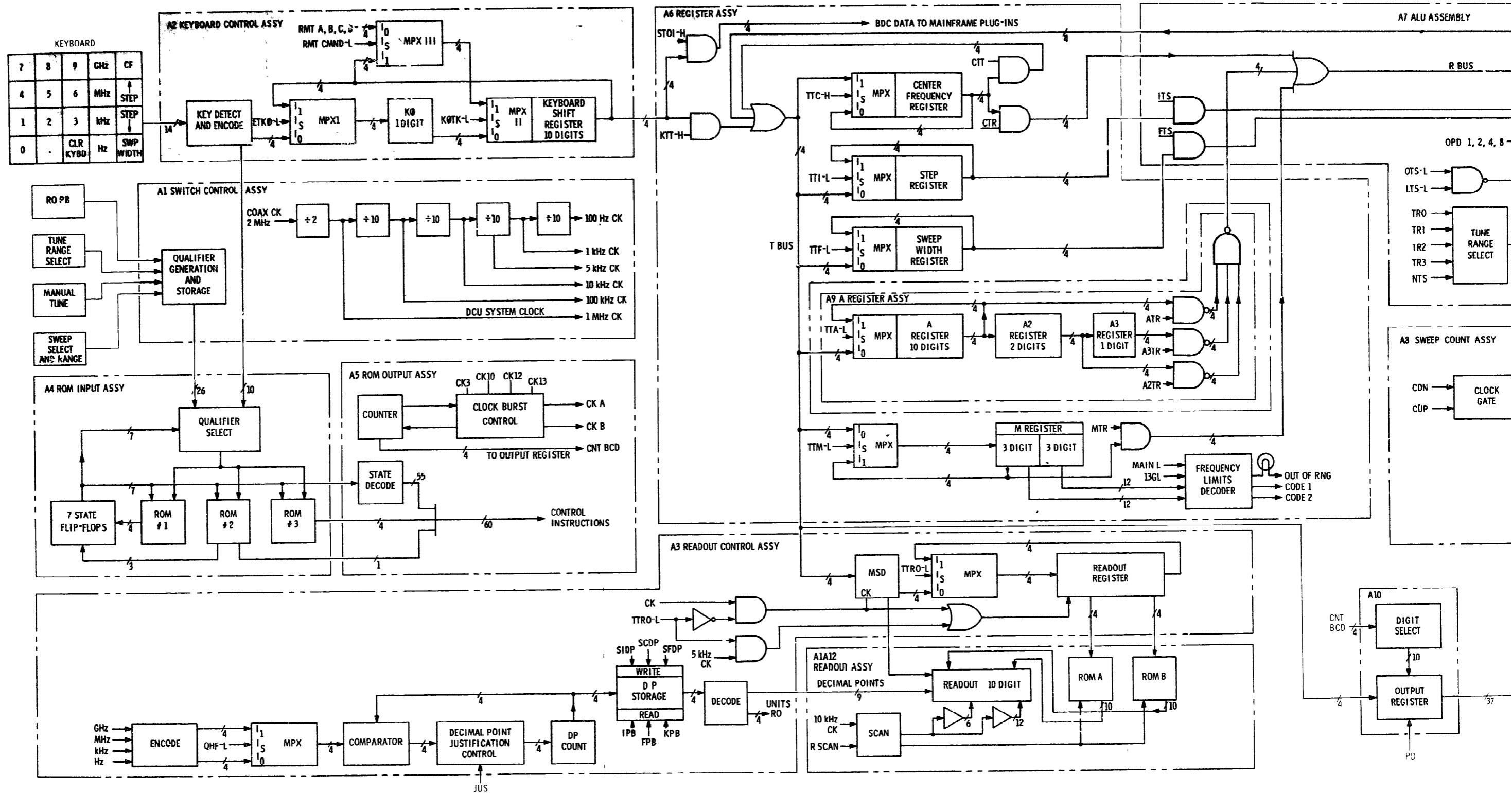


Figure 8-52. 8660B DCU (A1)



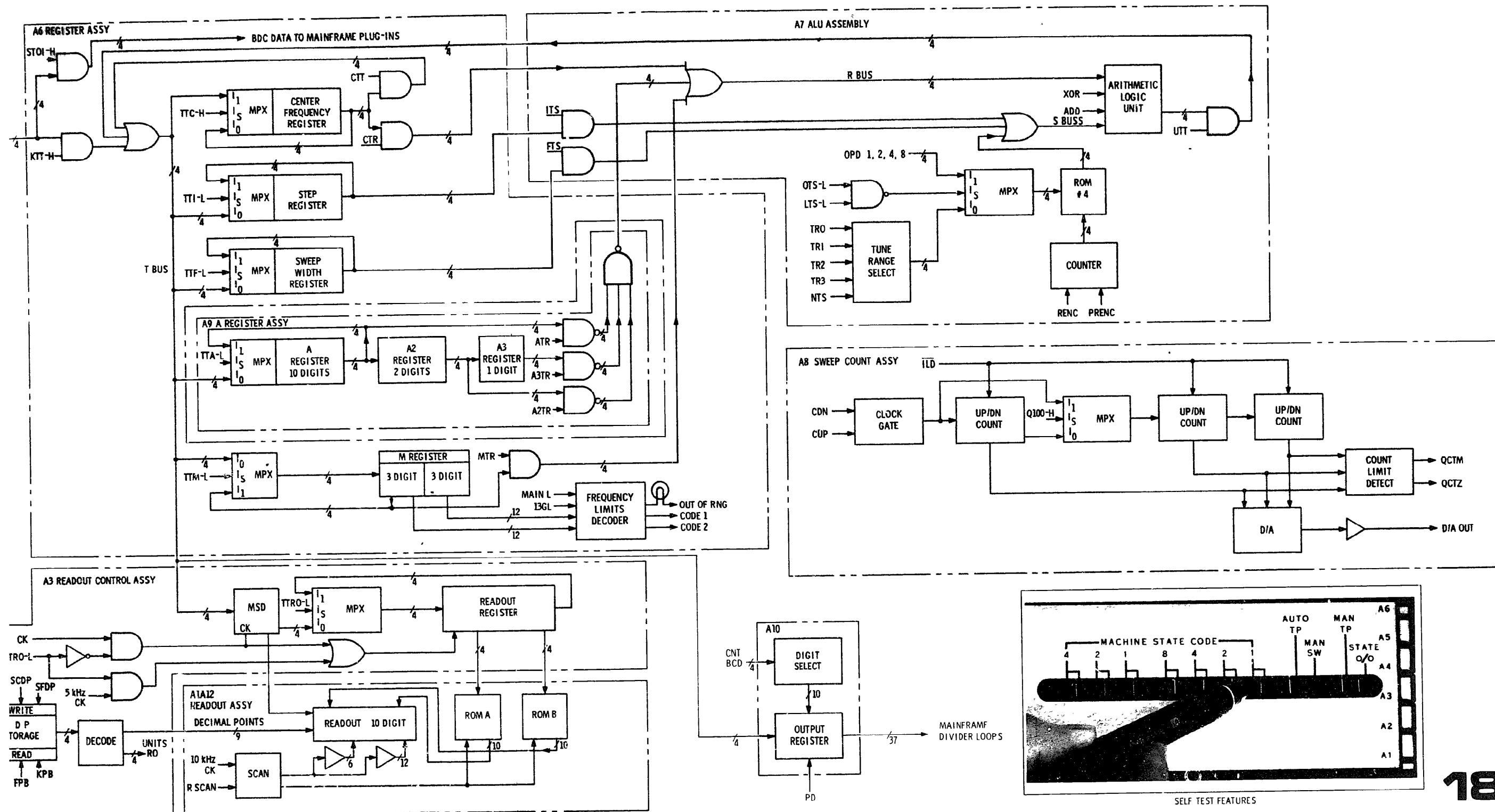
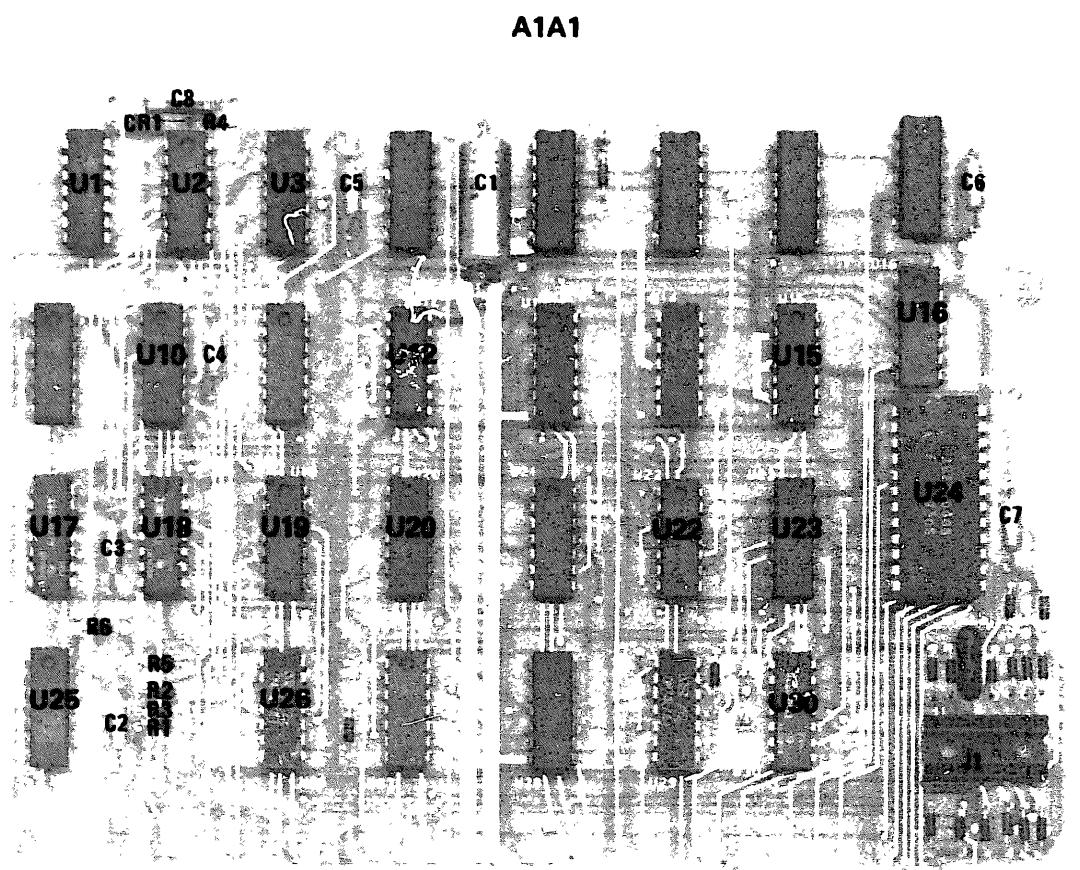


Figure 8-53. DCU Block Diagram, A1  
8-105



*Figure 8-54. P/O A1A1 Switch Control Assy. Component Locations (Part 1)*

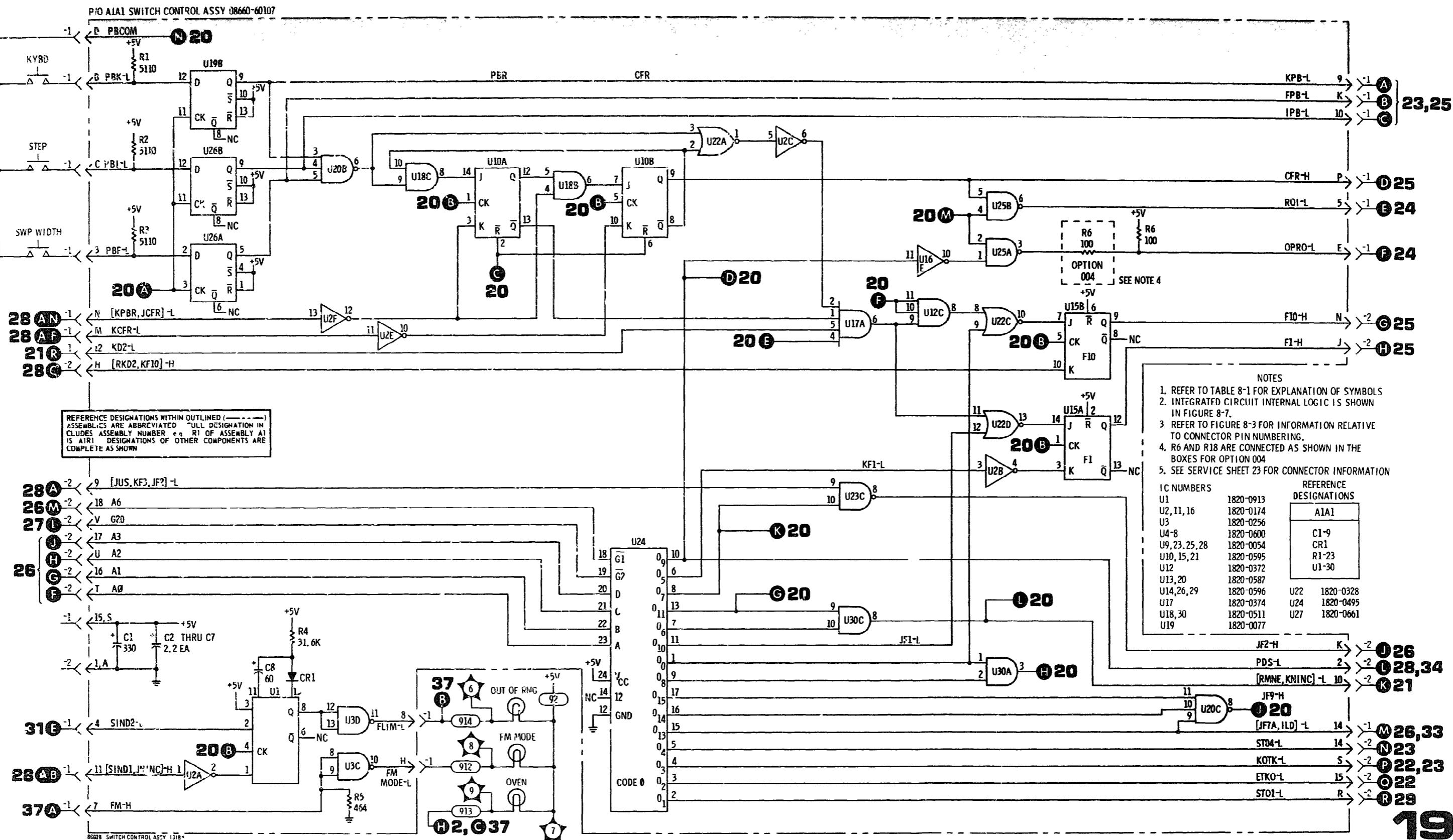


Figure 8-55. A1 A1 Switch Control Assy (Part 1)

## SERVICE SHEET 20

## P/O SWITCH CONTROL ASSEMBLY A1A1

Service Sheets 19 and 20 show the circuits of the A1A1 assembly schematically.

The circuits receive inputs from all front panel switches except the keyboard. These inputs serve to set (or reset) certain flip/flops or may simply flow through the assembly for use in other assemblies.

A principal output is qualifier F10-H from flip/flop U15 shown on SS19. When qualifier F10-H is set the state machine will go through the various states to set up the operation selected by the operator. Principal inputs to the F10 flip/flop are from the keyboard via input KD2-L, the readout pushbutton switches, the sweep control switches or the manual mode tuning dial.

A second principal circuit is the 4-to-16 selector U24 (shown on SS19) which is one of four such selectors in the DCU. Selector U24, which is designated as CODE 0, is a part of this assembly because many of the outputs are directly used in other circuits in the assembly. The other three selectors are located on the A1A5 assembly which appears on Service Sheet 28.

A third principal circuit is the clock dividers which provide six different clock outputs used in various DCU circuits.

The first divider, D type flip/flop U29B divides the 2 MHz coax clock by two. The 1 MHz output of U29B drives divide-by-ten U8 and is also used as the system clock.

The second divider, U8, divides by ten. The 100 kHz output drives divide-by-ten U7 and is also used as the keyboard clock.

The third divider, U7, divides by ten. The 10 kHz output drives U6 and is also used in the readout assembly.

The fourth divider, U6, provides two outputs. The first, a divide-by-two, 5 kHz clock is used in the readout control assembly. The second output is a divided-by-ten 1 kHz clock used in controlling the sweep. The 1 kHz output also drives U5.

The fifth divider, U5, divides by ten. The 100 Hz output is used in the sweep control circuits and to clock the pushbutton flip/flops (see SS19).

In the upper left hand corner of the schematic is a block labeled ROTARY PULSE GENERATOR (abbreviated RPG). The RPG is enabled by the MANUAL MODE RESOLUTION switch in any position except OFF. The RPG is also enabled when the SWEEP MODE switch is placed in the MAN position. The SWEEP MODE switch takes precedence over the MANUAL MODE RESOLUTION switch.

The RPG contains a light source and two photocells which are used to generate two square waves. These two square waves have a quadrature relationship - they are 90° out of phase.

## SERVICE SHEET 20 (Cont'd)

The circuits following the RPG CW and CCW outputs must detect when a manual entry has been made and also whether the input is an increase or a decrease in frequency.

AND gate U12B is driven by the output of NAND gate U25C and the CW and CCW inputs from the RPG. The output of NAND gate U25C is high in the local mode whenever the MANUAL TUNE RESOLUTION switch is set to STEP, FINE, MED, or COARSE or when the SWEEP MODE switch is set to MAN.

Assume that the RPG is to be turned in the CW direction and that initially the CW output is low. The CCW output is low when the CW output goes high. When the CCW output goes high AND gate U12B is enabled and its output is high. When the CW output goes low, PLS-H goes high to cause an add operation and the low output of AND gate U12B clocks U29A through NAND gate U28D to cause the Q output (MNE-H) to go high.

When the RPG is turned CCW, the CCW output will go high at a time when the CW output is low. 90° later CW goes high and AND gate U12B output goes high. When, 90° later, CCW goes low, U12B output goes low and clocks U29A through U28D. The CW output is still high so the output of NAND gate U28A, PLS-H, is low. A subtraction operation is directed rather than an addition operation.

The enabling input to NAND gate U28A is from a cross-connected pair flip/flop, U28B/C. TR0-L is low only during the power detect operation when the instrument is first turned on. TR0-L is also coupled back to NAND gate U23B and U3A to inhibit the front panel manual controls during power detect.

Divide-by-five counter U4 is used when the HF RF output unit is in use and the 1 MHz (COARSE) step increment is selected. This is done to provide a fine control over the 1 MHz COARSE operation. Only every fifth input from the RPG can clock the MNE-H flip/flop, and control is improved.

Option 004 instruments have a 100 Hz resolution rather than 1 Hz resolution. Part of the changes required for this change is to shift R18 from its location shown on the schematic to a point between U30D pin 13 to ground. The step increments in OPT 004 instruments are 100 Hz, 10 kHz and 1 MHz.

## SWEEP ENABLE CIRCUITS

The SW1 flip/flop, U21A, Q output (SW1-H) and SWON-H go high for all sweep operations. Selection of AUTO or MAN sweep controls the J input of U21A through AND gate U12A and U22B when enabled by state 0/0 at 19 (H). Selection of SWEEP OFF controls the K inputs for reset of U21A through NAND gate U20A.

Flip/flop U21B, also referred to as the F9 flip/flop, is the sweep rate control. When the instrument is first turned on the K input to U21B is high due to the state of the TR0 flip/flop (U28B/U28C), so the  $\bar{Q}$  output is set high.

When state 0/13, 0/14 or 0/15 is reached the J input to U21B goes high and the system clock causes the Q output to go high. When U21B Q output is high NAND gate U23D is enabled and the system clock is coupled through

## SERVICE SHEET 20 (Cont'd)

to NAND gate U13C. These three states enable the sweep to step at the maximum clock rate (1 MHz) during certain parts of the sweep operation.

The  $\bar{Q}$  output of the single sweep flip/flop, U19A, is high in the quiescent state. Since both inputs to AND gate U18A are high the level at the  $\bar{S}$  input to U19A does not affect the flip/flop.

When the SWEEP MODE switch is placed in the SINGLE mode and the SINGLE pushbutton is pressed, the output of AND gate U18A goes low to set the Q output of U19A high. The Q output of U19A (QSS-H) stays high for the period of one sweep width. The inverted system clock at the pin 2 input of OR gate U27A cannot reset U19A because instructions RQSS-H is low during the single sweep operation.

When the single sweep operation is concluded, instruction RQSS-H goes high, is inverted by U2D and enables OR gate U27A. The next inverted system clock resets both U19A and U21A (Q goes low and  $\bar{Q}$  goes high)

When the single sweep was initiated, U19A  $\bar{Q}$  went low to cause the output of AND gate U12A to go low. The pin 6 input to NOR gate U22B is also low so the J input is high at U21A, the SW1 flip/flop. The next clock pulse will cause the Q output of U21A (SW1-H) to go high. SWON-H is also high during the time the output of U12A is low as controlled by the QSS flip/flop, U19A.

While the Q output of U21B is high the system clock is coupled through NAND gate U23D to pin 10 of NAND gate U13C. Pins 9 and 11 of U13C are high because U21B  $\bar{Q}$  is low. The system clock is coupled through NAND gate U13C to U14A. Since the D input to U14A is held high the Q output goes high on the clock pulse. The inverted system clock then causes the Q output of U14B (QSP-H) to go high. When state 0/11 is reached pin 9 of U27C goes low to permit the inverted system clock to reset U14A and U14B (Q outputs go low) to make them ready for the next system clock.

When one of the three other clock sources is to be used to drive U14A, state 0/9 is reached, pin 12 of OR gate U27D goes low, the inverted system clock at OR gate U27D pin 11 resets U21B and the output of AND gate U18D resets U14A and U14B.

## SERVICE SHEET 20 (Cont'd)

The circuits following the RPG CW and CCW outputs must detect when a manual entry has been made and also whether the input is an increase or a decrease in frequency.

AND gate U12B is driven by the output of NAND gate U25C and the CW and CCW inputs from the RPG. The output of NAND gate U25C is high in the local mode whenever the MANUAL TUNE RESOLUTION switch is set to STEP, FINE, MED, or COARSE or when the SWEEP MODE switch is set to MAN.

Assume that the RPG is to be turned in the CW direction and that initially the CW output is low. The CCW output is low when the CW output goes high. When the CCW output goes high AND gate U12B is enabled and its output is high. When the CW output goes low, PLS-H goes high to cause an add operation and the low output of AND gate U12B clocks U29A through NAND gate U28D to cause the Q output (MNE-H) to go high.

When the RPG is turned CCW, the CCW output will go high at a time when the CW output is low. 90° later CW goes high and AND gate U12B output goes high. When, 90° later, CCW goes low, U12B output goes low and clocks U29A through U28D. The CW output is still high so the output of NAND gate U28A, PLS-H, is low. A subtraction operation is directed rather than an addition operation.

The enabling input to NAND gate U28A is from a cross-connected pair flip/flop, U28B/C. TR<sub>0</sub>-L is low only during the power detect operation when the instrument is first turned on. TR<sub>0</sub>-L is also coupled back to NAND gate U23B and U3A to inhibit the front panel manual controls during power detect.

Divide-by-five counter U4 is used when the HF RF output unit is in use and the 1 MHz (COARSE) step increment is selected. This is done to provide a fine control over the 1 MHz COARSE operation. Only every fifth input from the RPG can clock the MNE-H flip/flop, and control is improved.

Option 004 instruments have a 100 Hz resolution rather than 1 Hz resolution. Part of the changes required for this change is to shift R18 from its location shown on the schematic to a point between U30D pin 13 to ground. The step increments in OPT 004 instruments are 100 Hz, 10 kHz and 1 MHz.

## SWEEP ENABLE CIRCUITS

The SW1 flip/flop, U21A, Q output (SW1-H) and SWON-H go high for all sweep operations. Selection of AUTO or MAN sweep controls the J input of U21A through AND gate U12A and U22B when enabled by state 0/0 at 19 (H). Selection of SWEEP OFF controls the K inputs for reset of U21A through NAND gate U20A.

Flip/flop U21B, also referred to as the F9 flip/flop, is the sweep rate control. When the instrument is first turned on the K input to U21B is high due to the state of the TR<sub>0</sub> flip/flop (U28B/U28C), so the  $\bar{Q}$  output is set high.

When state 0/13, 0/14 or 0/15 is reached the J input to U21B goes high and the system clock causes the Q output to go high. When U21B Q output is high NAND gate U23D is enabled and the system clock is coupled through

## SERVICE SHEET 20 (Cont'd)

to NAND gate U13C. These three states enable the sweep to step at the maximum clock rate (1 MHz) during certain parts of the sweep operation.

The  $\bar{Q}$  output of the single sweep flip/flop, U19A, is high in the quiescent state. Since both inputs to AND gate U18A are high the level at the  $\bar{S}$  input to U19A does not affect the flip/flop.

When the SWEEP MODE switch is placed in the SINGLE mode and the SINGLE pushbutton is pressed, the output of AND gate U18A goes low to set the Q output of U19A high. The Q output of U19A (QSS-H) stays high for the period of one sweep width. The inverted system clock at the pin 2 input of OR gate U27A cannot reset U19A because instructions RQSS-H is low during the single sweep operation.

When the single sweep operation is concluded, instruction RQSS-H goes high, is inverted by U2D and enables OR gate U27A. The next inverted system clock resets both U19A and U21A (Q goes low and  $\bar{Q}$  goes high).

When the single sweep was initiated, U19A  $\bar{Q}$  went low to cause the output of AND gate U12A to go low. The pin 6 input to NOR gate U22B is also low so the J input is high at U21A, the SW1 flip/flop. The next clock pulse will cause the Q output of U21A (SW1-H) to go high. SWON-H is also high during the time the output of U12A is low as controlled by the QSS flip/flop, U19A.

While the Q output of U21B is high the system clock is coupled through NAND gate U23D to pin 10 of NAND gate U13C. Pins 9 and 11 of U13C are high because U21B  $\bar{Q}$  is low. The system clock is coupled through NAND gate U13C to U14A. Since the D input to U14A is held high the Q output goes high on the clock pulse. The inverted system clock then causes the Q output of U14B (QSP-H) to go high. When state 0/11 is reached pin 9 of U27C goes low to permit the inverted system clock to reset U14A and U14B (Q outputs go low) to make them ready for the next system clock.

When one of the three other clock sources is to be used to drive U14A, state 0/9 is reached, pin 12 of OR gate U27D goes low, the inverted system clock at OR gate U27D pin 11 resets U21B and the output of AND gate U18D resets U14A and U14B.

When U21B is reset the  $\bar{Q}$  output goes high and NAND gate U23D is inhibited to prevent further system clock pulses from reaching U14A. The high output from U23D is also used to partially enable NAND gate U13C.

When the SWEEP MODE switch is set to AUTO and the SWEEP RATE switch is set to MED, the output of NAND gate U9A goes high to enable NAND gate U9D which supplies the 1 millisecond (1 kHz) clock to U9B. The pin 5 input to U9B is high because the high output of U9A is inverted and used to inhibit U9C

Pins 2 and 13 of NAND gate U13A are high so the clock path is completed through to NAND gate U13C. Pins 9 and 10 of U13C are both high so U14A is clocked and its Q output goes high

The next inverted system clock causes QSP-H to go high. This signal instructs the system to advance another sweep step. Using the inverted system clock to clock U14B ensures that the 1 millisecond clock is synchronized to the system clock. The 1 millisecond clock is derived from the system clock. However, the dividers are low power devices and the propagation delay may result in excessive phase shift. Also, during manual sweep, asynchronous pulses are received through U13B and U13C which must be synchronized.

When the FAST sweep rate is selected, operation of the circuit is the same as in the MED mode except that the output of AND gate U30B (Q100-H) is high. In this mode the sweep is 100 steps at the 1 kHz rate.

When the SLO sweep rate is selected, operation is similar to the MED mode except that the output of U9A is low, U9C is enabled, and the 10 millisecond (100 Hz) clock is used

When the SWEEP MODE switch is set to MAN, the RPG is enabled because the low level at NAND gate U25C pin 9 drives the output high to enable AND gate U12B. Operation of the RPG and associated circuits is essentially the same as it was in the MANUAL TUNE RESOLUTION mode. MNE-H is applied to the pin 5 input of NAND gate U13B, U13B pin 3 is held high by U21B  $\bar{Q}$  and U13B pin 4 is held high by QMSW-H so MNE-H is coupled through to NAND gate U13C. The other two inputs to U13C are high so U14A is clocked by MNE-H. U14B is then clocked by the next inverted system clock. This ensures that the MNE-H input is synchronized with the system clock and provides QSP-H

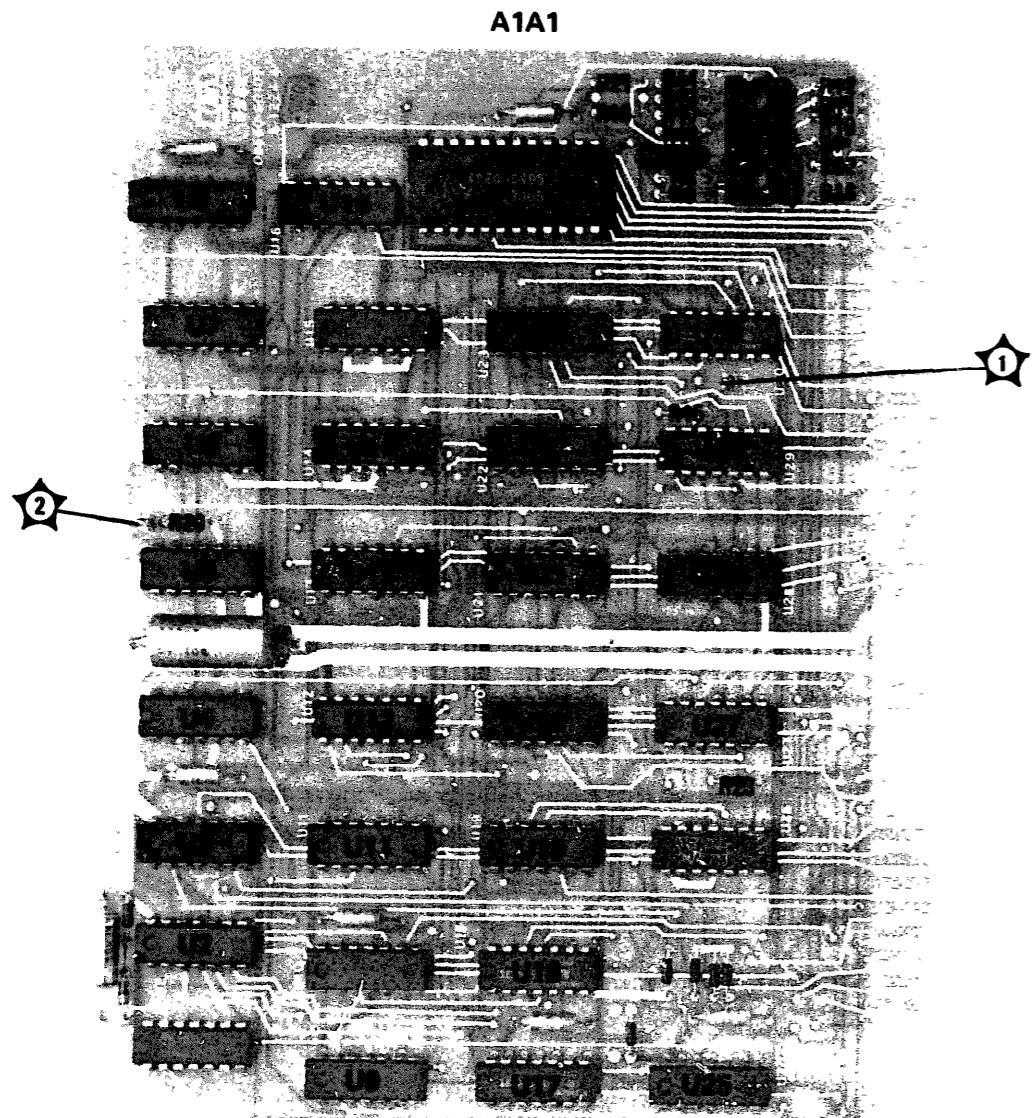


Figure 8-56. P/O A1A1 Switch Control Assy Component Locations (Part 2)

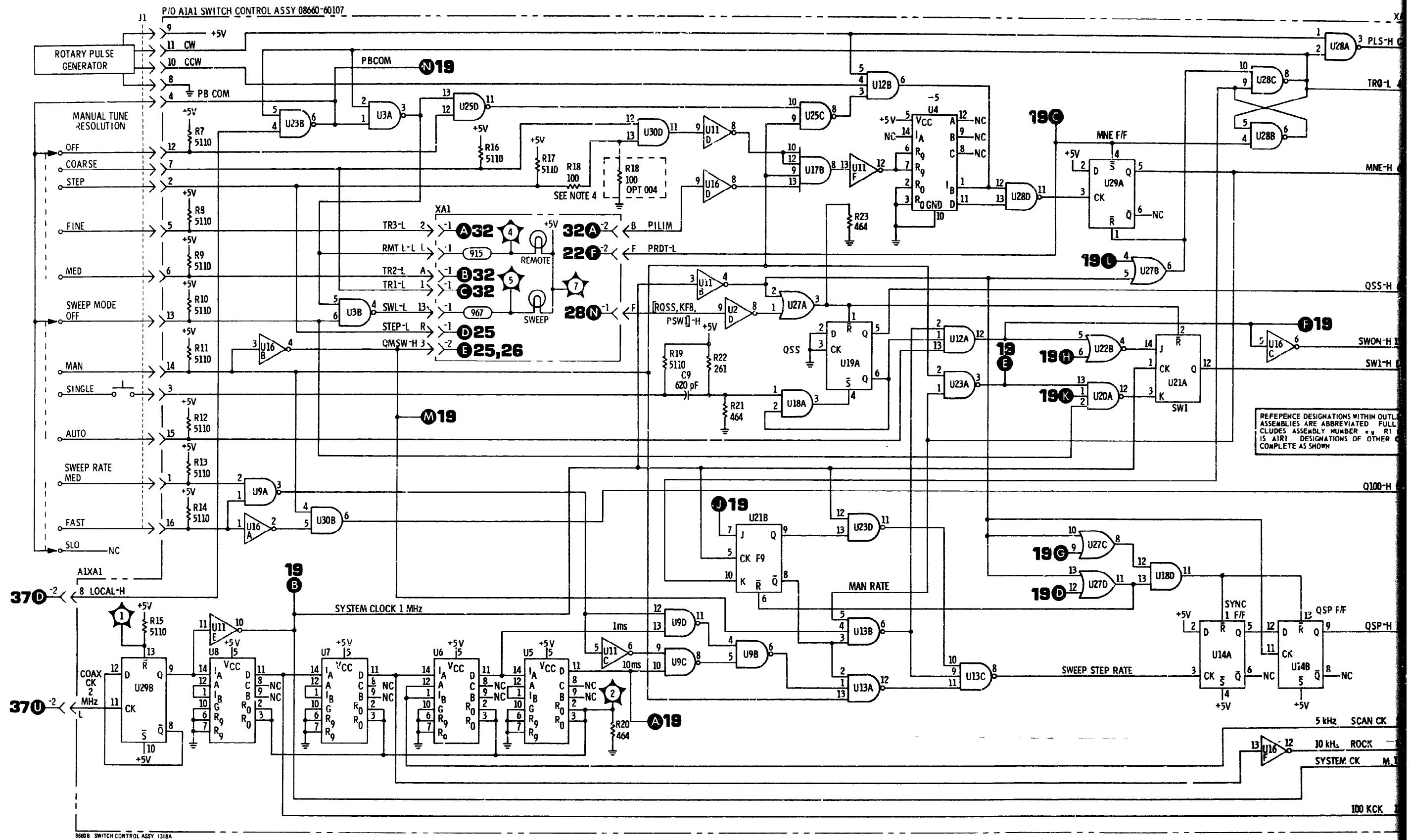


Figure 8-57 A1A1

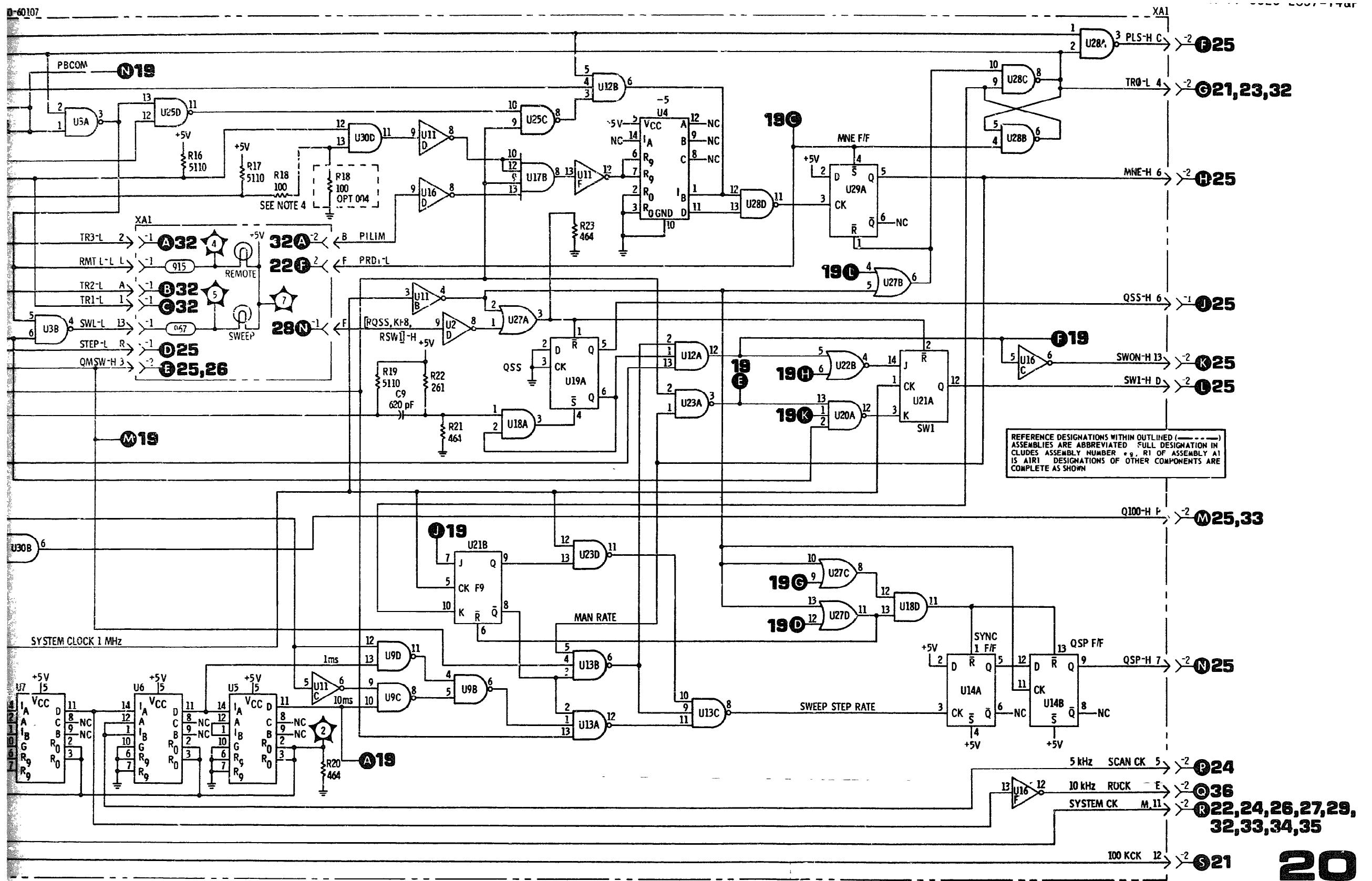


Figure 8-57. A1 A1 Switch Control Assy (Part 2)

## SERVICE SHEET 21

**P/O A1A2 KEY CONTROL ASSEMBLY AND KEYBOARD**

The circuits in the A1A2 assembly are shown schematically on Service Sheets 21 and 22. The keyboard scan, encoding circuits and the keyboard shift register are all contained in this assembly. Also shown on Service Sheet 21 is the keyboard printed circuit board schematic.

The Model 8660B keyboard is unique in that there are no mechanical contacts. Basically the keyboard consists of ten pairs of printed circuit pulse transformers with metallic spring leafs suspended adjacent to them. When a key is pressed the associated pulse transformer is inductively shorted.

The pulse transformer primaries are connected in series pairs between the 100 kHz clock pulses and a 1 of 10 selector, U26. The pulse transformer secondaries are connected in series between the inputs of a dual comparator, U20. The pulse transformer pairs are connected so that secondary currents cancel until a key is pressed.

The keyboard clock (KYB CK) is connected to all of the transformer pairs. However, only one transformer pair is selected at any given time by U26. The keys are scanned sequentially, 10 times for numeric data, then 10 times for non-numeric data. This is accomplished by clocking flip/flop U17B every time the D output of divide-by-ten U25 is active. The Q and  $\bar{Q}$  outputs of U17B determine which of the U20 comparators is being strobed. The lower comparator is the numeric key detector.

When the lower U20 comparator is being strobed, if a numeric key is pressed a positive going pulse appears at U20 E<sub>0</sub> output. This causes the one-shot U19 to change states (Q goes low). The low output of U19  $\bar{Q}$  inhibits the clock gate (U16C) to the divider (U25). U25A, B, C and D outputs retain the binary number of the key pressed. The numeric data is applied to multiplexer U12 which is shown on Service Sheet 22. Numeric data cannot affect the non-numeric data circuits because OR gates U24A, B, C and D outputs are held high by NAND gate U16B.

U19 is a monostable multivibrator which may be re-triggered during its period of about 15 microseconds. The period of U19 will be extended as long as the key is pressed since re-triggering pulses are received from U20 every 10 microseconds.

Operation when a non-numeric key is pressed is essentially the same as it is for a numeric key. The upper U20 comparator is enabled by U17B Q and both U16B inputs are high. The low level at the output of U16B enables U24A, B, C and D to couple the data through to one-of-ten selector, U23. The outputs of U23 correspond to the input binary weighted code.

U15 is a multiplexer which processes data from U23 in the local mode or from external programming circuits in the remote mode. The only data functions processed through U15 are the step up, step down and center frequency. In the local mode U15 pin 1 (select) selects inputs 1A, 1B, and 1C because the LOCAL-H line is high. In the remote mode the select line (U15 pin 1) is low so inputs 0A, 0B and 0C are selected. In either case, the Z<sub>A</sub>, Z<sub>B</sub> and Z<sub>C</sub> outputs correspond to the A, B and C inputs.

## SERVICE SHEET 21 (Cont'd)

The gating circuits to the right of U15 and U23 generate various qualifiers and instructions. As an example, if the CF key is pressed (code 8, 1000) the O<sub>8</sub> output of U23 is low, U15Z<sub>C</sub> is low and the output of U22D is high. At all other times, when the CF function has not been initiated qualifier CF-H is low.

Flip/flop U7B functions in the microprogram to prevent an entry operation from being made before a unit key is pressed. A unit key must be pressed to complete the justification process. The F3 flip/flop (U7B) K input goes high when qualifier QU1 (U21B pin 8) is high and instruction KF3-L is low which occurs in state 1/6. The next clock pulse resets U7B and qualifier F3 goes low. The F3 J input must go high in order to make the Q output go high to complete the cycle. This is accomplished when the JF3-L input (pin 11) becomes active when the machine is active in any one of four states, 1/11, 1/12, 1/13 or 1/0 and U7B is clocked. The Q output will also go high if the CLEAR KYBD key is pressed generating output O<sub>2</sub> from U23. U17A Q (KD2-L) provides a signal to the F10 flip/flop on the A1A1 assembly when a key has been pressed or when CMND-P-L goes low in the remote mode.

J-K flip/flop U7A is used in a synchronizing process, it is connected as a "D" type flip/flop. The "D" input from U19 is asynchronous since it is a response to manual press and release of a key. The synchronized KDN-H output ensures correct machine state action.

**NOTE**

For instruments with serial prefix numbers below 1310A refer to Section VII of this manual for information referring to prior use of A1A2U7.

## SERVICE SHEET 21 (Cont'd)

The gating circuits to the right of U15 and U23 generate various qualifiers and instructions. As an example, if the CF key is pressed (code 8,1000) the 08 output of U23 is low, U15ZC is low and the output of U22D is high. At all other times, when the CF function has not been initiated, qualifier CF-H is low.

Flip/flop U7B functions in the microprogram to prevent an entry operation **from being** made before a unit key is pressed. A unit key must be pressed to complete the justification process. The F3 flip/flop (U7B) K input goes high when qualifier QU1 (U21B pin 8) is high and instruction KF3-L is low which occurs in state 1/6. The next dock pulse resets U7B and qualifier F3 goes low. The F3 J input must go high in order to make the Q output go high to complete the cycle. This is accomplished when the JF3-L input (pin 11) becomes active when the machine is active in any one of four states, 1/11, 1/12, 1/13 or 1/0 and U7B is clocked. The Q output will also go high if the CLEAR KYBD key is pressed generating output 02 from U23. U17A Q (KD2-L) provides a signal to the F10 flip/flop on the A1A1 assembly when a key has been pressed or when CMND-P-L goes low in the remote mode.

J-K flip/flop U7A is used in a synchronizing process; it is connected as a "D" type flip/flop. The "D" input from U19 is asynchronous since it is a response to manual press and release of a key. The synchronized KDN-H output ensures correct machine state action.

## NOTE

For instruments with serial prefix numbers below 1310A refer to Section VII of this manual for information referring to prior use of A1A2U7.

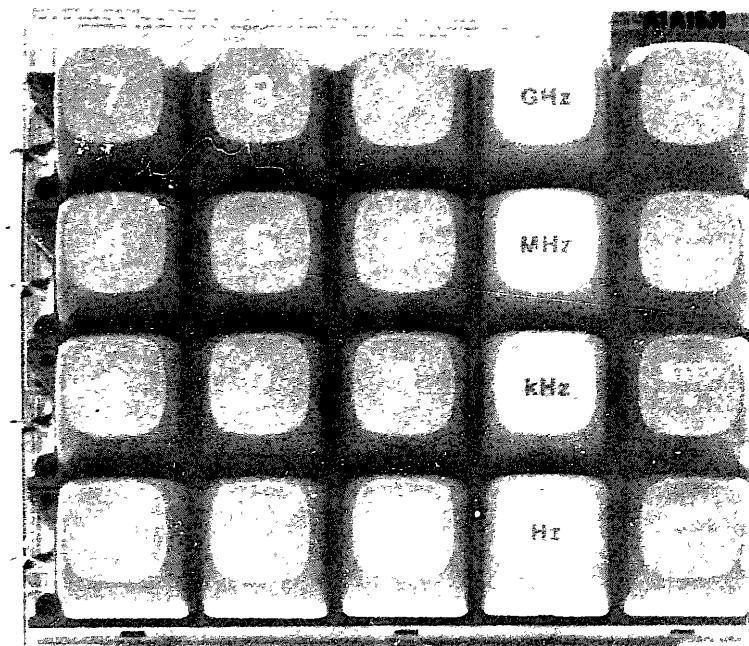


Figure 8-58. Keyboard Assembly Front View

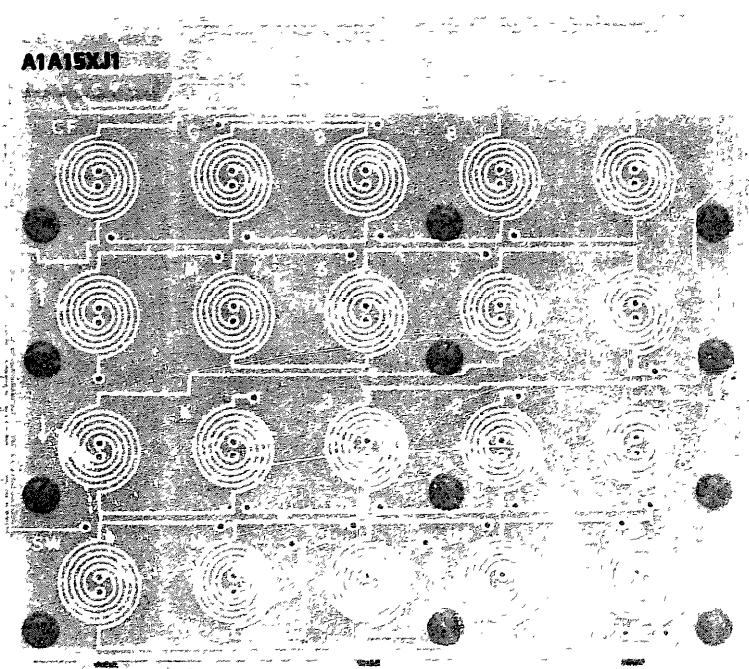


Figure 8-59. Key board Assembly Rear View

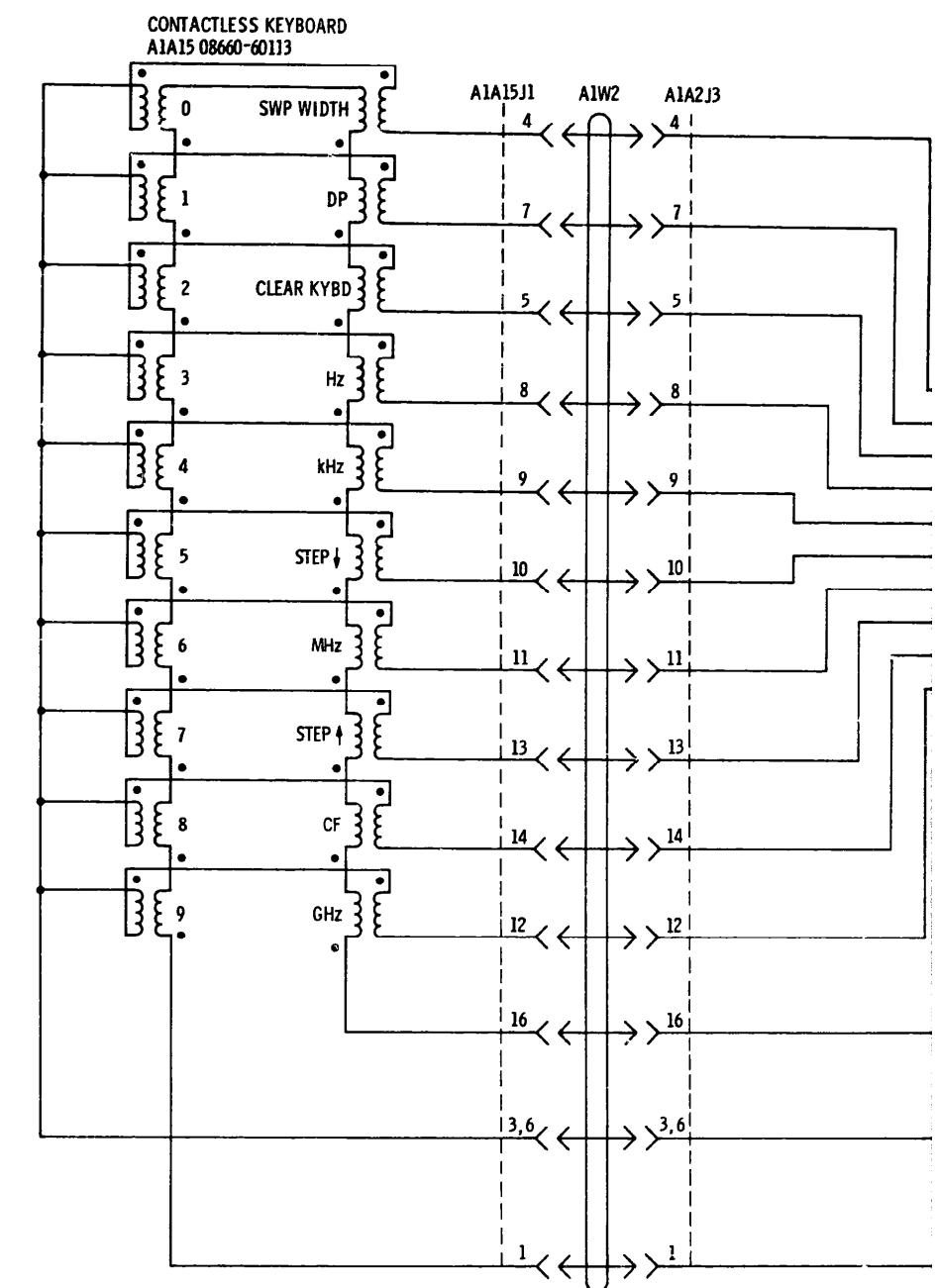
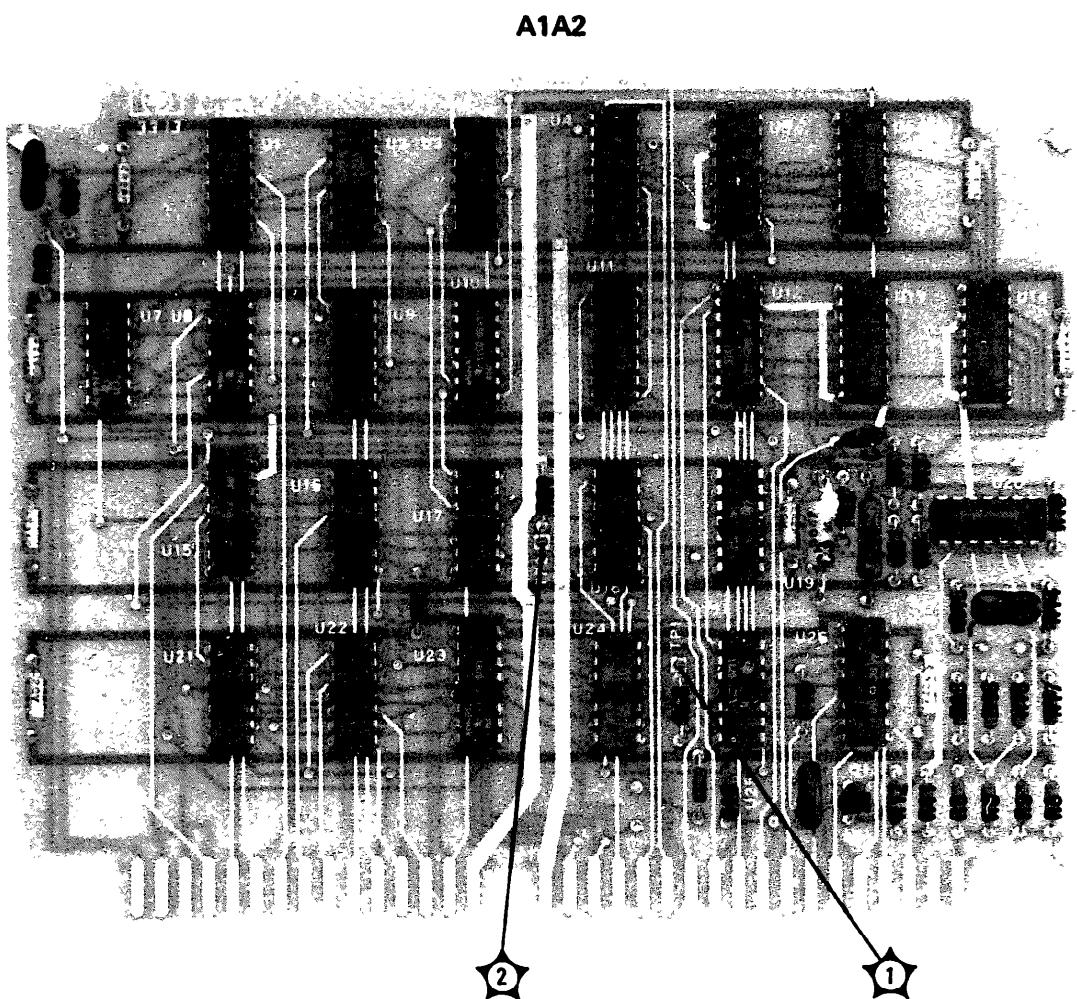
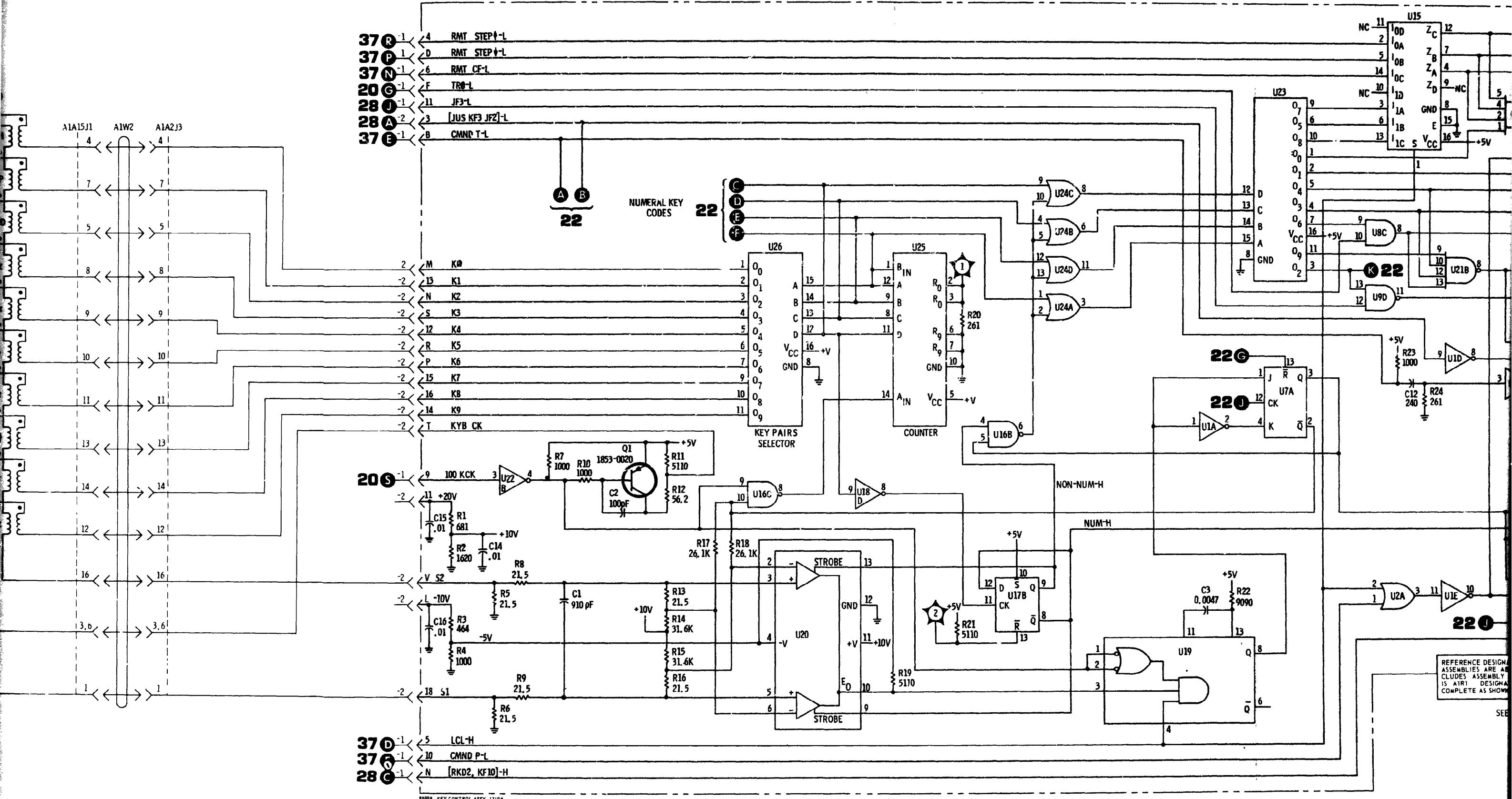
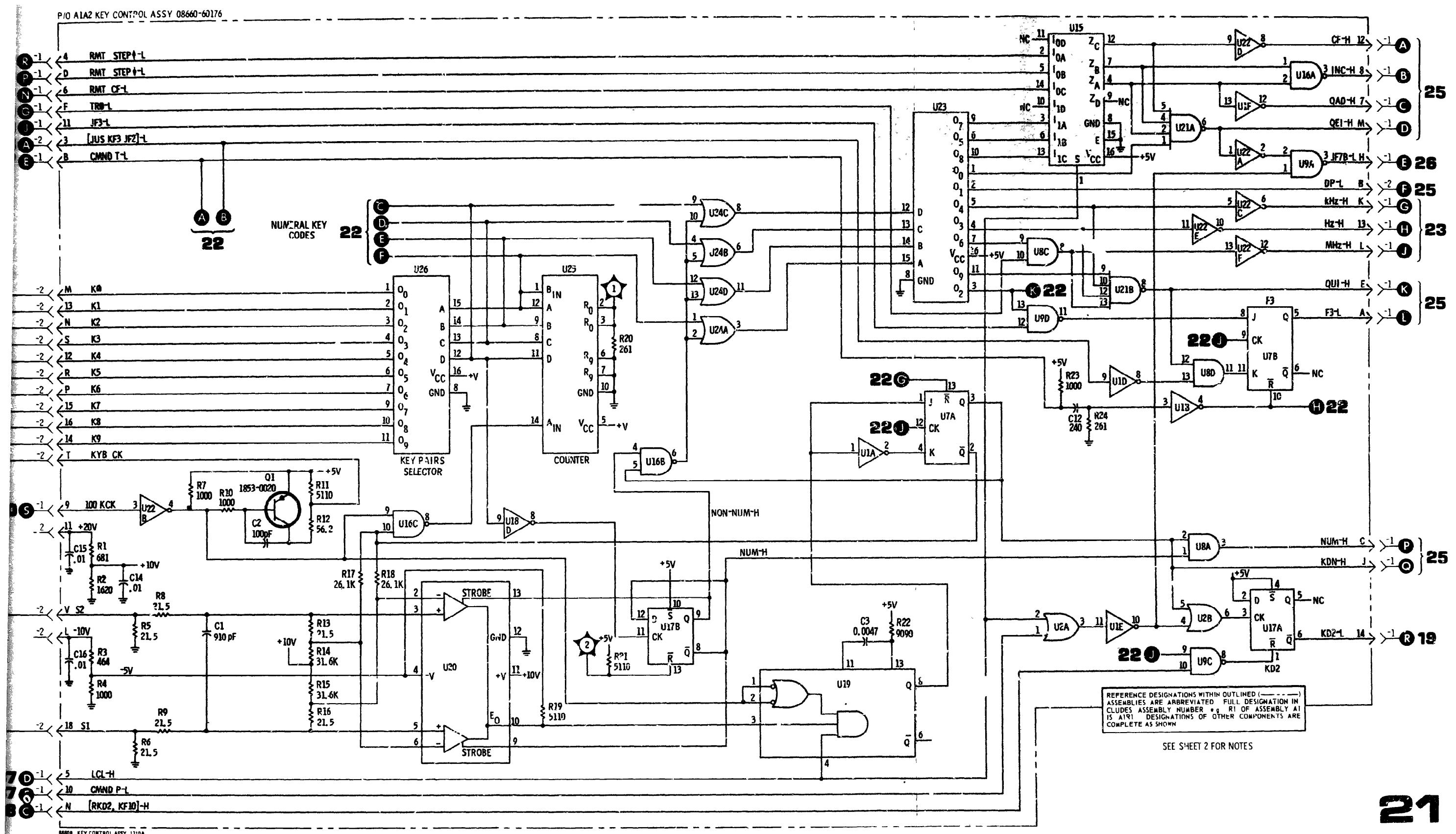


Figure 8-60. P/O A1 A2 Key Control Assy Component Locations (Part 1)

P/O A1A2 KEY CONTROL ASSY 08660-60176





*Figure 8-61. P/O A1A2 Key Control Assy (Part 1)*

**SERVICE SHEET 22**

**P/O A1A2 KEY CONTROL ASSEMBLY**

The A1A2 key control assembly circuits are shown schematically on Service Sheets 21 and 22. The circuits shown on this Service Sheet consist of the recirculating keyboard register and the circuits which control it.

Multiplexer U12, when a keyboard numeral is being entered (ETK0-L is active), couples the data to U5 which is a one digit, 4 bit-register (referred to as the K0 register).

After the data is stored in K0 a train of 10 clock pulses transfer the data to the main keyboard shift register consisting of U4, U6, U14 and U13.

U6 and U4 are dual 8 bit registers. Data bits 1 and 2 for digits 3 through 10 are stored in U6 and data

bits 4 and 8 for digits 3 through 10 are stored in U4. U14 and U13 are one digit four bit registers. U14 stores digit 2 and U13 stores digit 1.

Note that the output of the main keyboard register is coupled back to U5 through U12 while the train of 10 clock pulses is present. This is true because ETK0-L is now in the quiescent (high) state. The cycle continues until all of the required numeric entries are made. When the last digit has been entered (the least significant digit) it will be so positioned in the register that it will be the first digit clocked out. The first digit clocked in will be the last digit clocked out.

In the local mode when the keyboard data is clocked out, it is also clocked back into the main keyboard register, through multiplexer U11. U12 and U5 are bypassed.

The control gates for the keyboard register conventional.

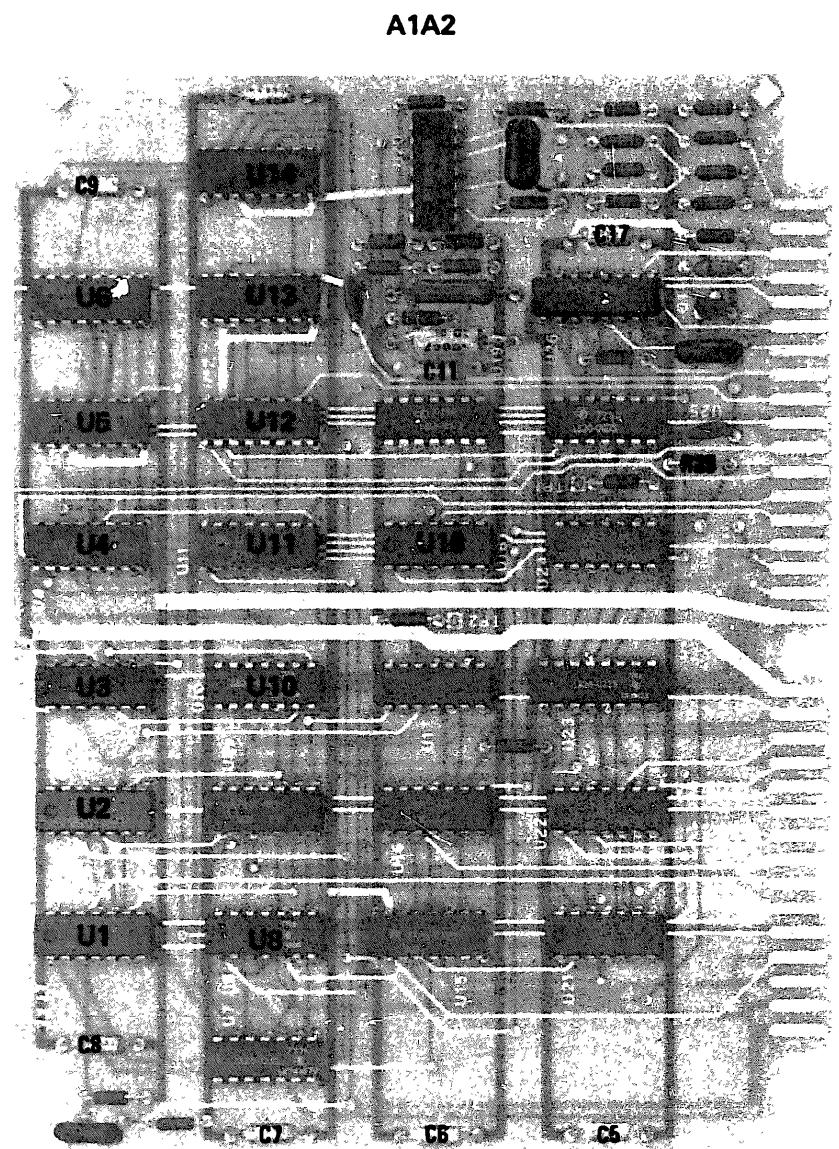
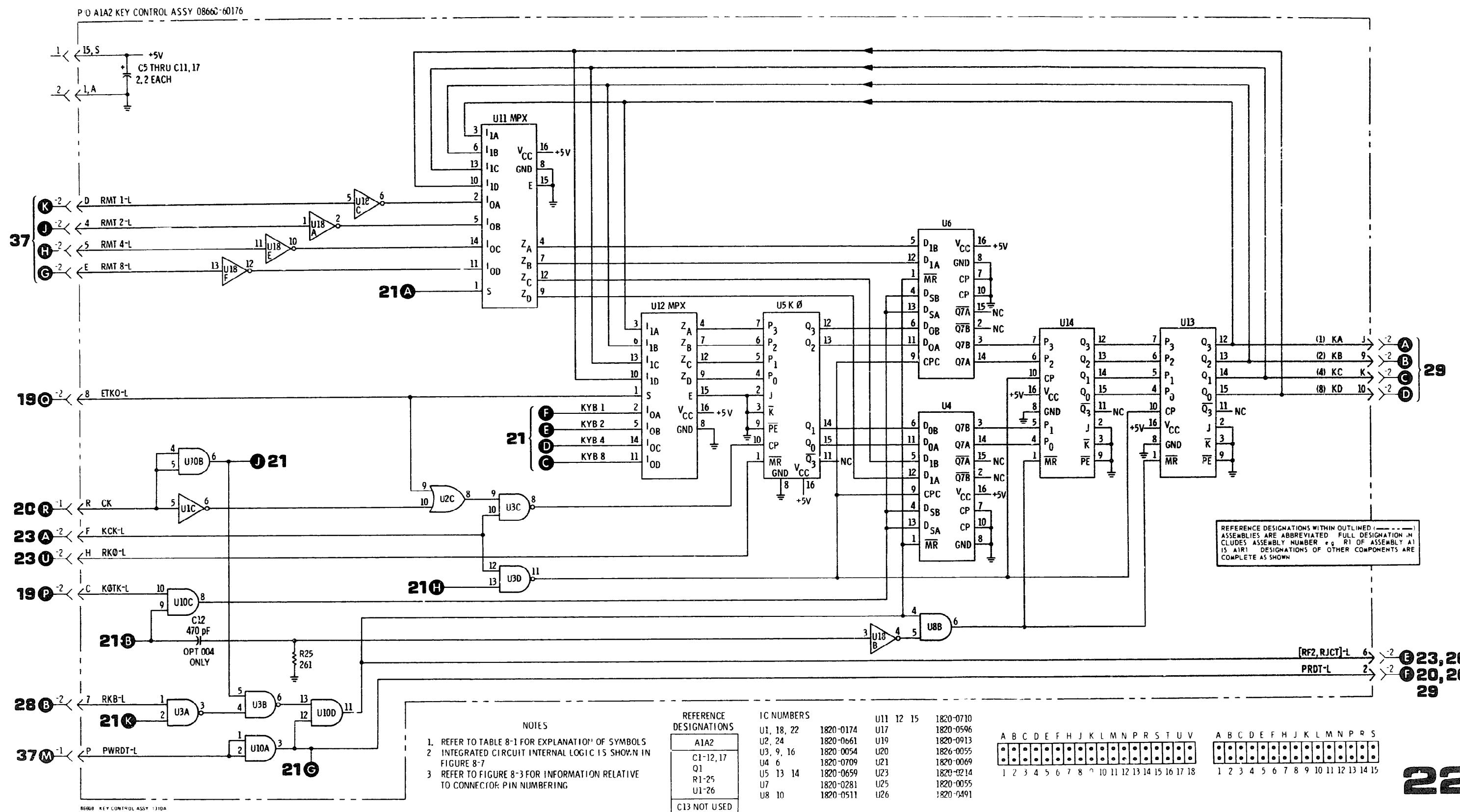


Figure 8-62. P/O A1A2 Key Control Assy Component Locations (Part 2)



**Figure 8-63. P/O A1A2 Key Control Assy (Part 2)**

## SERVICE SHEET 23

### P/O A1A3 READOUT CONTROL ASSEMBLY

Most of the circuitry shown on this service sheet is used to justify (properly locate) the decimal point in the readout. Following entry of a multidigit number, units are selected and the number is shifted left or right in the keyboard register as controlled by the following circuitry which determines position of the decimal point.

QHF-H, which is not used in the current configuration, is always low so the I<sub>0</sub> inputs to multiplexer U2 are selected. Multiplexer U2 provides a BCD code at the Z outputs which is a 9 (1001) for Hz, 6 (0110) for kHz, 3 (0011) for MHz and 0 (0000) for GHz.

As an example of circuit operation, when the Hz unit key is pressed, Hz-H goes high. This high is coupled through OR gate U12B to the I<sub>0A</sub> input of U2 and it is also directly connected to the I<sub>0D</sub> input of U2. The outputs of U2 Z pins are 1001. This verifies the code 9 for Hz.

The outputs of multiplexer U2 are applied to the B inputs of comparator U11. The A inputs to comparator U11 are from justification counter, U20. The purpose of U11 is to detect when A=B.

The justification counter, U20 is a decade counter which operates only after a decimal point or a units entry has been made.

Referring to the Algorithmic State Machine, (flow graph) assume that the first keyboard entry is a numeral and follow the machine states from 0/0 through states 4/0, 5/0, 6/0 and 6/1 to state 1/5. State 1/5 contains the first instruction that directly affects the circuits shown on Service Sheet 23.

The instructions in state 1/5 are RF2-L which resets FF2, RKB-L which resets the keyboard and RJCT-L which resets the justification flip/flop, U14A. RJCT-L is also inverted by U31C to reset the counter, U20, to nine (1001).

The next state, 0/2, contains the instruction ETK0-L. This causes the numeric data to be stored in the K0 register.

The next state, 0/3, contains instruction K0TK-L (K0 to keyboard register) and a train of 10 clock pulses. These clock pulses transfer the data from the single digit K0 register to the least significant storage in the ten digit keyboard storage register.

#### NOTE

See Service Sheets 21 and 22 for a more complete analysis of the keyboard register.

When a decimal point is entered after a numeric entry the machine state path is from state 0/0 through states 4/0, 5/0 and 5/1 to state 3/5.

In state 3/5 instruction SJCT-L (set justification counter) appears. This instruction, which has a low assertive state, is applied to NOR gate U13A pin 3. The second input to NOR gate U13A is the inverted system clock which is high when SJCT-L appears. When the inverted system clock at U13A pin 2 goes low the clock input to U14A goes high and causes the Q output to go high.

## SERVICE SHEET 23 (Cont'd)

When U14A goes high NAND gate U33A is enabled. Pin 4 of U33A is high because B9-L is not active at this time. The system clock at NAND gate U35B pin 3 is applied to U33A pin 5 when CK10 CK is high and JUS or QJO are high. Pin 2 of U33A is high because K0TK is low.

The output of NAND gate U33B is high since QJO is low and NAND gate U30D is enabled for a period of nine clock pulses. The train of clock pulses ends when B9-L goes low and inhibits U33A.

The justification counter, U20, starts at a count of 9 in the local mode. The 9 clock pulses it receives cause it to stop one count lower than where it started. In other words, the first entry after a decimal point would cause the counter output to be an 8, the next entry a 7, etc.

The output of NAND gate U35B pin 6 is also used to clock the keyboard register via line KCK-L. The output burst of 10 clock pulses shifts the new entry to the correct sequential position as described in Service Sheets 21 and 22.

So far, justification has not taken place; the justification counter has merely deducted the number of entries after the decimal point from 9. Flip/flop U14B has not yet been clocked because the JUS-L high level has been inverted by U31E to inhibit AND gate U32B.

As an example of circuit operation assume that 12.34 has been entered and the output is to be 12.34 kHz. Referring to the Algorithmic State Machine it can be seen that the UNITS path is the same as the numeral path until state 6/0 is reached. The qualifier following state 6/0, NUM-H, is not active so the next state is 0/4 which contains instruction RK0-L (reset K0 register).

RK0-L is the output of AND gate U32D. The inputs to U32D are from OR gate U21C which is high because JUS-L is not active and from AND gate U9A. ST04-L is active by virtue of being an output of state 0/4 and the low level is inverted by U24E to enable U9A. The system clock is then coupled to AND gate U32D to produce RK0-L.

Qualifier QU1-H is active for state 0/4 so the next state is 1/6 which contains instructions JUS-L, KF3-L and CK10J-L.

When JUS-L goes low it is inverted by U31E and applied to AND gates U25A and U32B. The second input to U32B is from OR gate U21D. The output of OR gate U21D is high because input pin 13 is connected to B9-L which is high.

The low to high output transition of U32B clocks U14B. Since the B inputs to U11 are a 6 (0110) and the A inputs are a 7 (0111), both A=B and A<B are low. The D input to U14B is low and clocking U14B causes the Q output to go low.

The low Q output of U14B is applied to one input of NOR gate U13B. The second input to U13B is CKB-H which is also low. The high input to OR gate U21A at pin 1 is coupled through to pin 10 of AND gate U32C. Pin 2 of OR gate U21A is also held high by the inverted low A=B level.

The second input to AND gate U32C is from AND gate U25A. U25A pin 2 is held high by the inverted JUS-L level and pin 1 is held high by the local line. The high output of U25A enables AND gate U32C and QJ0-H goes high.

## SERVICE SHEET 23 (Cont'd)

When QJ0-H goes high it holds the instrument in state 1/6 until the justification requirements are met. QJ0-H enables NAND gate U35B through OR gate U23A. QJ0-H also enables NAND gate U33B which then clocks U20 through U30D.

The clock train is again stopped after nine clock pulses by the action of B9-L and the outputs of U20 and U2 are compared by U11. Since both of the inputs to U11 are now 6 (0110), A=B goes high to cause the D input to U14B to go high.

When U11 A=B is a high the justification requirements are satisfied. However, several things must happen before state 1/6 may be left.

The A=B high level is inverted by U31A and applied to pin 2 of OR gate U21A. This does not immediately affect the output of U21A because the output of NOR gate U13B is held high by the low Q output of U14B and the CKB-H level which is low.

U14B is clocked by AND gate U32B as follows: U32B pin 5 is still held high by the inverted JUS-L low level. The second input to U32B is from OR gate U21D. When B9-L goes low, pin 13 of U21D is also low. The inverted system clock at pin 12 of U21D is high so the output of U32B remains high. On the next clock the inverted clock goes low and the output of U32B goes low. This does not clock U14B because a D type flip/flop may be triggered only on a positive going pulse. The next time the inverted clock goes high is at the beginning of the tenth clock; this clocks U14B and causes the Q output to go high.

The high Q output of U14B inhibits NOR gate U13B. Since both inputs to OR gate U21A are now low AND gate U32C is inhibited and QJ0-H goes low. The machine state progression is now through states 6/14, 1/1, 4/1, 1/9, 4/9, 4/10 and 5/10 to 0/0. The instrument is now ready for the next entry (function).

Now assume that 12.34 kHz was entered by accident, it should have been 12.34 MHz. 12.340 is still stored in the keyboard register so all that is necessary to start the justification process over is to press the MHz key.

Operation of the justification circuit is the same as it was for kHz except that now the U2 multiplexer input is a 3 (0011) and the output of U20 is a 6 (0110). QJ0-H goes high as it did in the previous example. QJ0-H stays high until three trains of clock pulses cause the output of U20 to reach 3 (0011) and once again U11 A=B is high. QJ0-H is caused to go low in the same manner as in the previous example.

For a third example assume it is decided that 12.340 kHz was, after all, the desired output frequency.

Initiation of the justification cycle is the same as it was in the previous two examples. However, the A inputs to U11 are a 3 (0011) and the B inputs are a 6 (0110) so A<B is high. This high level at pin 12 of OR gate

## SERVICE SHEET 23 (Cont'd)

U12D holds the D input of U14B high and U14B is clocked as it was before but no output change results since the Q output was already high.

The low A=B output of U11 is again inverted and applied to OR gate U21A to enable AND gate U32C and again cause QJ0-H to go high (U32C pin 9 is caused to go high in the same manner as in the previous examples).

U11 is continually comparing the outputs from U20 and U2. The first clock to U20 causes the output to go to 4 (0100), the second to 5 (0101) and the third to 6 (0110). Justification has been accomplished, A=B is high, U21A is inhibited and QJ0-H immediately goes low. The state progression back to state 0/0 is the same as it was in the previous examples.

During all of these justification counts, outputs from KCK-L to the keyboard register cause the entry to be shifted to positions consistent with units and decimal point.

It may be seen from the foregoing examples that left shifting (from kHz to MHz) takes three trains of clock pulses, while right shifting (from MHz to kHz) takes only three clock pulses.

The decimal point storage, U3, is a 4 x 4 file. It stores 4 four-bit words. These words are selected by the outputs of U22A and U22B as follows: word 1, center frequency 00; word 2, sweep width 01; word 3, step (increment) 10 and word 4, keyboard 11.

The inverted system clock is applied to pin 12 (G<sub>W</sub>) of U3 where it is used as the write clock. W<sub>A</sub> and W<sub>B</sub> (write) inputs are controlled by AND gates U22A and U22B which are, in turn, controlled by the KYBD, STEP or SWP WIDTH pushbuttons in the local mode. When these pushbuttons are all inactive the center frequency is selected.

When operating in the remote mode only the center frequency is displayed. It is displayed in MHz only. In the remote mode the LOCAL-H line is low. This low level is inverted by U31F and used to reset the justification counter, U20, to zero. OR gates U1C and U1D provide the inputs to U3 in the remote mode. Pin 10 of U1C and Pin 12 of U1D are connected directly to the output of U35A which is one half of a flip/flop. Normally, in the local mode, the output of U35A is low.

When the remote mode is selected and LOCAL-H goes low it is applied to AND gate U32A and OR gate U1B. The output of AND gate U32A goes low, is inverted and applied to AND gate U25B. The second input to AND gate U25B is QHF-H which is low. Both inputs to OR gate U1B are low so the output is also low. The low output of U1B triggers flip/flop U35A/U5C and the output of U35A goes high to drive U3 through U1C and U1D. The code then set in U3 is 3 (0011) which corresponds to MHz.

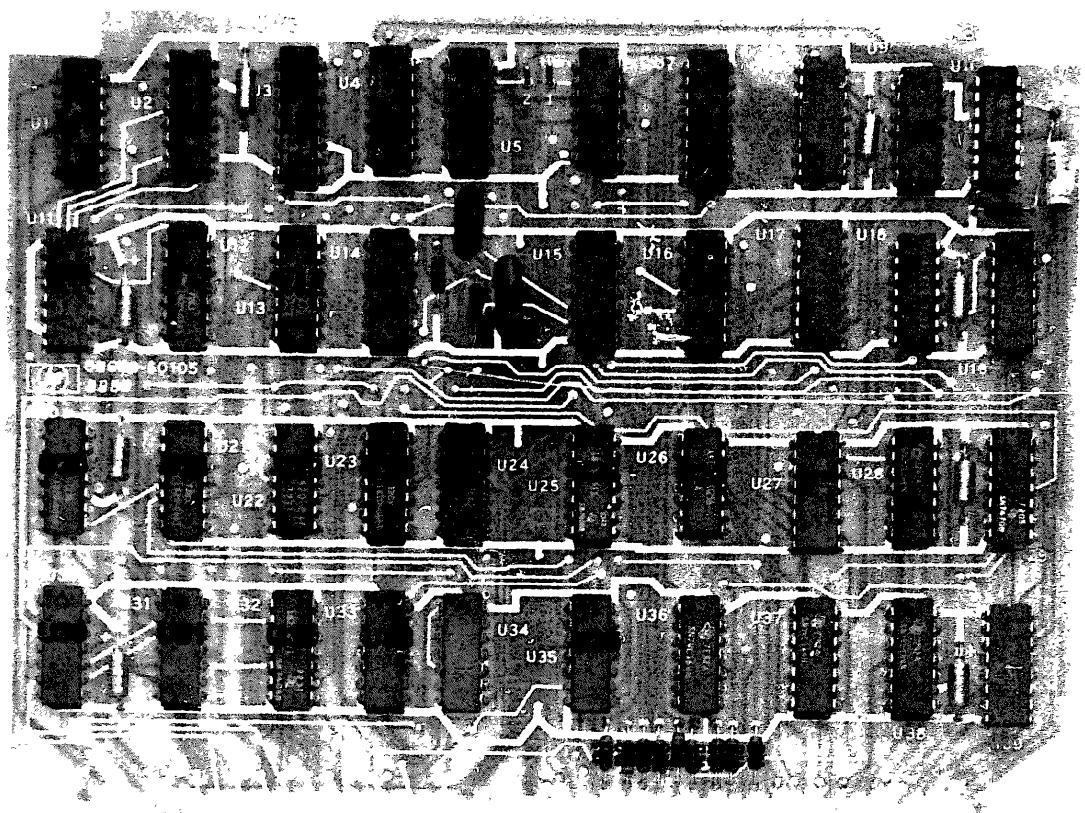
When switching from remote to local (RF2-RJCT)-L resets U35A/U5C.

Decoder U7 is a one-of-ten selector. All outputs of the decoder are high except the one selected. The outputs of the decoder directly drive the decimal point LED's in the readout (the series resistors are for current limiting).

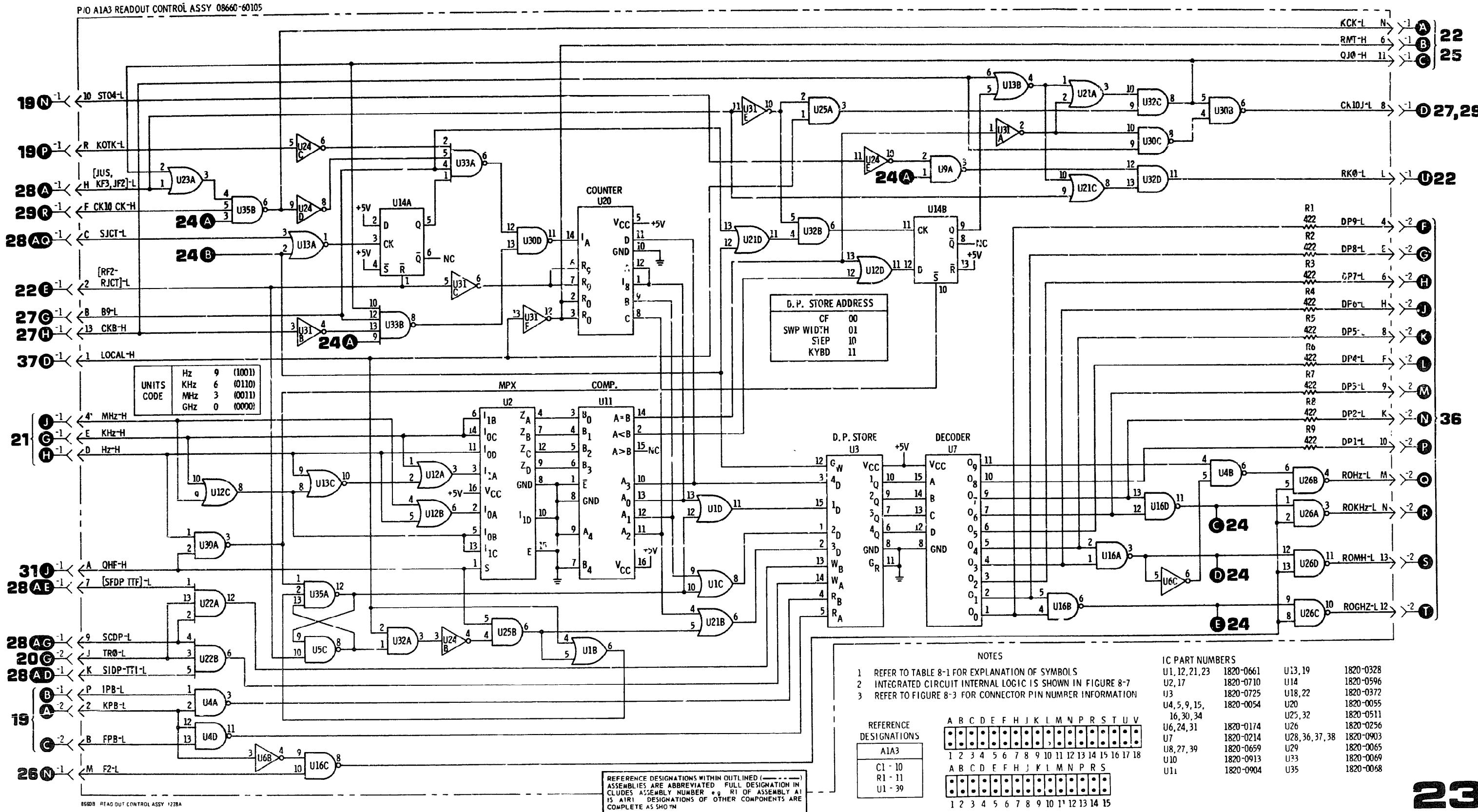
The gates shown to the right of decoder U7 are used to drive the Hz, kHz, M (M and Hz are both used to display MHz) and GHz lamps. NAND gates U26A, B, C and D are open collector lamp drivers. The common input to these gates is controlled by the combined functions of F2 and KPB. During the time when keyboard entries are being made, the KYBD pushbutton is pressed for readout of the entries, the units lamps are inhibited. When the entry is justified, F2-L goes low and the units lamps are then enabled.

**Model 8660B**

**A1A3**



*Figure 8-64. P/O A1A3 Readout Control Assy Component Locations (Part 1)*



*Figure 8-65. P/O AIA3 Readout Control Assy (Part 1)*

## SERVICE SHEET 24

### P/O READOUT CONTROL ASSEMBLY A1A3

The A1A3 assembly is shown schematically on Service Sheets 23 and 24.

The circuits shown on SS24 consist of the nine digit recirculating readout register, MSD (most significant digit) storage, scan control for the readout and a blanking control for the readout.

When new information is to be clocked into the readout register from the T bus, TTRO-L goes low at pin 4 of NAND gate U5B and U5B output goes high. OPRO-L and ROI-L are normally high. The output of NAND gate U5A goes low and the output of NAND gate U5D goes high.

When the output of NAND gate U5D is high, the I<sub>1</sub> inputs of multiplexer U17 are selected. The information on the T bus is clocked into the register consisting of U8, U27, U36, U37, U38 and U26.

Four-bit register U8 is referred to as the MSD (most significant digit) register. U8 is not in the readout recirculating loop; it directly drives the readout MSD (digit 10).

U27 is also a four-bit register with serial inputs from the multiplexer, U17. The output of U27 is applied in parallel to four 8-bit serial registers, U36, U37, U38 and U28.

While the output of NAND gate U5D is high the preset enable input (PE) to the sync register, U39, is also high. The register will function as a shift register, and, with the J input high, the first four clock pulses will cause the Q outputs of U39 to go high. These Q outputs will remain high until the recirculation cycle is started. This output of U39, a 15, (1 1 1 1) is the scan synchronizing code.

The output level of NAND gate U5D also is used to partially control clock inputs to the readout and sync registers.

Many of the gates shown in the lower left corner of the schematic function to control the clocks. The output of NAND gate U15D clocks the recirculating register including U39, the sync register.

The inputs to NAND gate U15D are from three-input NAND gate U35C and U22C/U24F which function together as a three-input NAND gate. One or the other of these inputs to U15D will be high at any given time and the other input provides the clock pulses.

When new data is being clocked in NAND gate U35C drives NAND gate U15D to clock the recirculating readout register at the system clock rate, 1 MHz. NAND gate U35C is enabled by the output of U34D and the ADDCK-H input which remains high for the period of ten clock pulses required to clock in the information. The system clock pulses are coupled through AND gate U25C and inverted by U6D. C9 and R10 form a one-shot

### SERVICE SHEET 24 (Cont'd)

which effectively delays the clock while TTRO is going low. Inverter U24A again inverts the clock before it is applied to NAND gate U34B. Since NAND gate U5D output is high the output of NAND gate U34B goes low with the positive clock pulse to trigger flip/flop U34C/U34D. The output of U34D then goes high to complete the enabling process for NAND gate U35C.

When the output of NAND gate U5D goes high the next system clock triggers one-shot U10 and the  $\bar{Q}$  output at pin 6 goes low, typically for a period of 105 microseconds. The low level at U10  $\bar{Q}$  sets the Q output of flip/flop U29 high and holds it high. The low output from U20  $\bar{Q}$  also inhibits U4C and blanks the readout through the brightness control.

When NAND gate U4C is inhibited the output goes high and enables one input to AND gate U22C. Since the Q output of flip/flop U29 is high, the inverted system clock is coupled through NAND gate U15B back to the pin 10 input of AND gate U22C.

The third input to AND gate U22C is enabled when TTRO-L goes high and causes the output of NAND gate U5D to go low. Flip/flop U34C/U34D changes state, AND gate U22C is enabled, and the system clock is coupled through inverter U24F and NAND gate U15D to clock the recirculating data. Note that the MSD register, U8, is not being clocked.

As long as the  $\bar{Q}$  output of one-shot U10 is low, (approximately 100 microseconds) AND gate U22C is enabled and the system clock drives the recirculating portion of the register including the sync register, U39. During this portion of the cycle insignificant leading zeros are blanked.

Whenever a leading zero reaches the sync register, U39, all of its outputs are low so the inputs to NOR gates U13D and U19D are low and their outputs are high. The low output of NAND gate U15A is applied to pin 5 of NOR gate U19B. Pin 6 of NOR gate U19B is also low since the QH outputs of U38 and U28 are high. The sync code (1111) has recirculated to the QH digit of the register. These two high levels are applied to NAND gate U9C which provides the low input to NOR gate U19B. The pin 10 input to AND gate U18C is high. Assume for the time being that the other two inputs to AND gate U18C and the output are all high (these inputs will be discussed later in this text). The high inputs to OR gates U23B, C and D cause the outputs to go high. The output of U18C is inverted by U6F to drive the output of AND gate U25D low. These outputs comprise the blanking code, 14 (1 1 1 0) which will recirculate in the position of a leading zero.

The information in the readout register continues to recirculate until the  $\bar{Q}$  output of U10 returns to a high state. Pin 13 ( $\bar{S}$ ) of flip/flop U29 also goes high to allow U29 to function as a J-K flip/flop. U29 Q remains high and the data continues to

### SERVICE SHEET 24 (Cont'd)

recirculate until the sync code (15) reaches the sync register, U39.

When the sync code reaches U39 all of the outputs go high to enable the K input to flip/flop U29. The next system clock causes the  $\bar{Q}$  output of U29 to go high. The scan cycle is not initiated.

When the  $\bar{Q}$  output of flip/flop U29 goes high, NAND gate U9B output goes low to enable the one-of-twelve selector, U5, on the readout assembly (SS36). The second input to NAND gate U9B at pin 4 is high because command TTRO-L is high.

The high level at the  $\bar{Q}$  output of flip/flop U10 enables NAND gate U4C to allow the 5 kHz SCANCK to be applied to AND gate U22C. The input to pin 9 of U22C is held high by flip/flop U34C/U34D and the pin 10 input is held high by the output of NAND gate U15B. The clock output of AND gate U22C is inverted and applied to NAND gate U15D. The second input to U15D is held high because flip/flop U34C/U34D inhibits NAND gate U35C.

It takes only six clock pulses at the 5 kHz rate (SCANCK) to clock the information in the readout register to the ROM's in the readout assembly.

When the six clock, 5 kHz train has clocked the nine data digits to the readout assembly the sync code (15) has recirculated to the QE output of the eight-bit registers. These outputs all go high to enable the J input of flip/flop U29. The next clock pulse causes the Q output of U29 to go high and couple the system clock through NAND gate U15B back to input pin 10 of AND gate U22C. The input to pin 11 of AND gate U22C is high because the 5 kHz clock is low. The system clock continues the recirculating process for four system clock periods at which time the sync code (15) again reaches U39. The K input to flip/flop U29 causes the  $\bar{Q}$  output of U29 to go high and restart the scan cycle.

The scan cycle continues without interruption until the readout register contents are changed by a new entry.

Blanking AND gate U18C is inhibited in several different ways in conjunction with selected frequency units.

When GHz is selected, input pin 9 of NOR gate U19C goes high, the output goes low and AND gate U18C is inhibited. Blanking of the MSD still occurs if the MSD is a zero because the low Q3 output of U8 turns off transistor switch Q1 in the readout assembly.

When MHz is selected all leading insignificant zeros are blanked until the sync code (15) reaches QE in the 8-bit registers. All

## SERVICE SHEET 24 (Cont'd)

inputs to AND gate U18A are high and the output also goes high. The high input to NOR gate U19A causes the output to go low and inhibit AND gate U18C. Blanking of zeros following the MHz decimal point is prevented.

When kHz is selected all leading zeros are blanked until a number is reached or the sync code reaches QB of the 8-bit registers. All inputs to AND gate U18B go high and the output goes high. The high input to NOR gate U19A causes the output to go low and inhibit AND gate U18C. Blanking of zeros following the kHz decimal point is prevented.

When Hz is selected all leading zeros are blanked.

Inputs OPR-L and OP>O-L are used only in option 004 (100 Hz resolution) instruments. These inputs last for two clock pulses and they force the two least significant digits to zero.

Input ROI-L establishes priority for the readout during manual sweep.

When one of the pushbuttons is pressed to call up the contents of a given register it takes priority and is displayed regardless of any change in manual sweep. When the pushbutton is released the readout will again display the manual sweep frequency.

Table 8-35. Readout Register Recirculating Cycle

ROM A										ROM B											
MSD	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>	S	MSD	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>	S		
U8	U27	U36	U37	U38	U28	U36	U37	U38	U28	U39	U8	U27	U36	U37	U38	U28	U36	U37	U38	U28	U39
0	0	0	0	1	2	3	4	5	6	S	0	0	0	1	2	3	4	5	6	S	
S	0	0	0	1	2	3	4	5	6												
6	S	0	0	0	1	2	3	4	5												
5	6	S	0	0	0	1	2	3	4												
4	5	6	S	0	0	0	1	2	3												
3	4	5	6	S	0	0	0	1	2												
2	3	4	5	6	S	0	0	0	1												
1	2	3	4	5	6	S	0	0	0												
0	1	2	3	4	5	6	S	0	0												
0	0	1	2	3	4	5	6	S	0												
0	0	0	1	2	3	4	5	6	S												

ROM A										ROM B											
MSD	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>	S	MSD	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>	S		
U8	U27	U36	U37	U38	U28	U36	U37	U38	U28	U39	U8	U27	U36	U37	U38	U28	U36	U37	U38	U28	U39
0	0	0	0	1	2	3	4	5	6	S	0	0	0	1	2	3	4	5	6	S	
S	0	0	0	1	2	3	4	5	6												
6	S	0	0	0	1	2	3	4	5												
5	6	S	0	0	0	1	2	3	4												
4	5	6	S	0	0	0	1	2	3												
3	4	5	6	S	0	0	0	1	2												
2	3	4	5	6	S	0	0	0	1												
1	2	3	4	5	6	S	0	0	0												
0	1	2	3	4	5	6	S	0	0												
0	0	1	2	3	4	5	6	S	0												
0	0	0	1	2	3	4	5	6	S												

## SERVICE SHEET 24 (Cont'd)

Table 8-36. Readout Register Leading Zero Blanking

ROM A										ROM B											
MSD	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>	S	MSD	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>	S		
U8	U27	U36	U37	U38	U28	U36	U37	U38	U28	U39	U8	U27	U36	U37	U38	U28	U36	U37	U38	U28	U39
B	0	0	0	1	2	3	4	5	6	S	Initial state Hz										
S	0	0	0	1	2	3	4	5	6												
6	S	0	0	0	1	2	3	4	5												
5	6	S	0	0	0	1	2	3	4												
4	5	6	S	0	0	0	1	2	3												
3	4	5	6	S	0	0	0	1	2												
2	3	4	5	6	S	0	0	0	1												
1	2	3	4	5	6	S	0	0	0												
0	1	2	3	4	5	6	S	0	0												
0	0	1	2	3	4	5	6	S	0												

A1A3

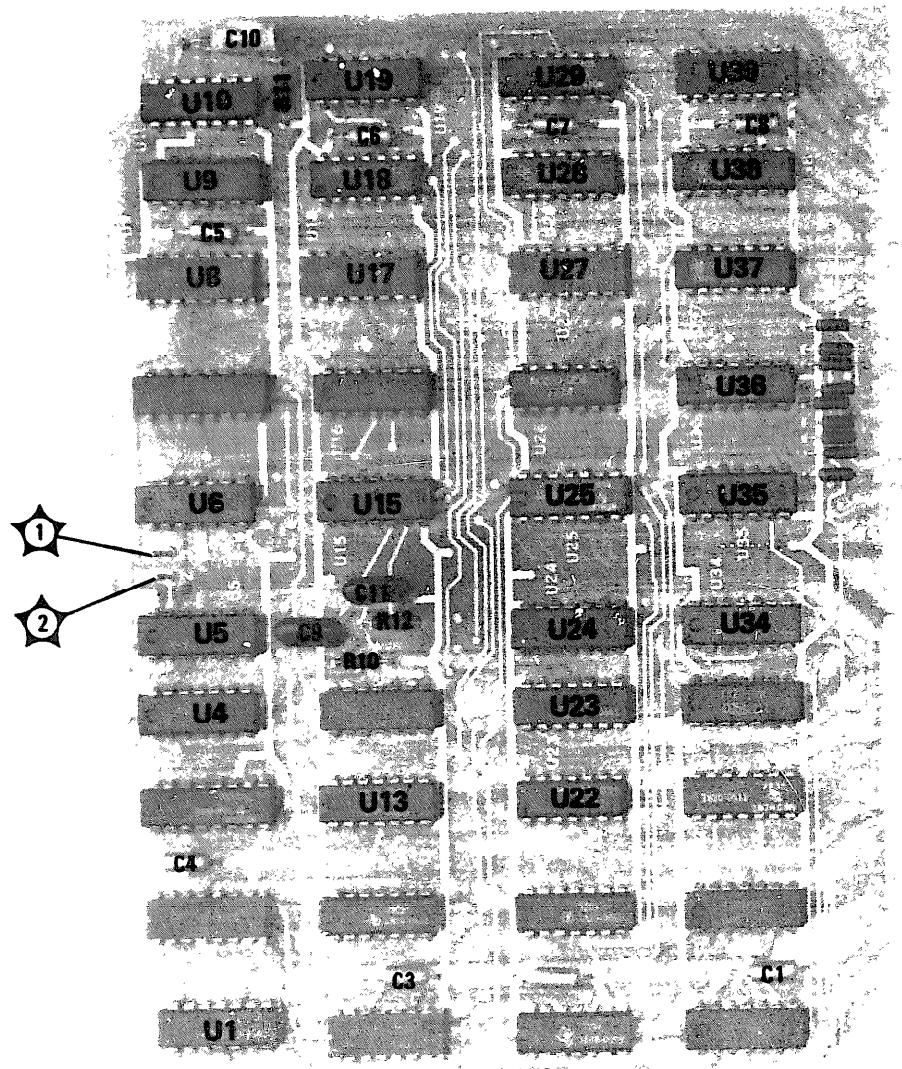
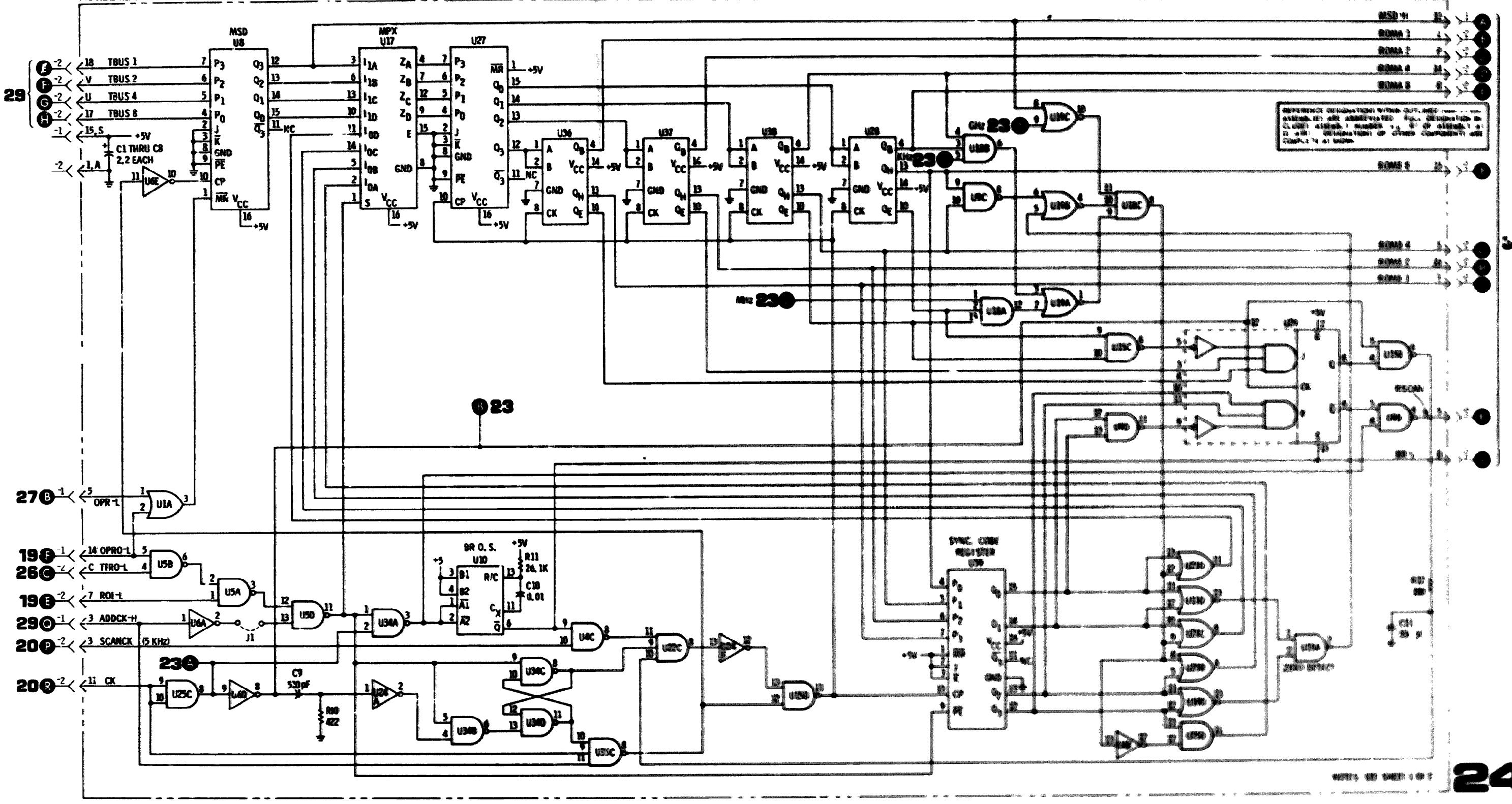


Figure 8-66. P/O A1A3 Readout Control Assy Component Locations (Part 2)

## P/O A1A3 READOUT CONTROL ASSY 08660-60105



## SERVICE SHEET 25

**P/I/O ROM INPUT ASSEMBLY A1A4**

The A1A4 (8825 and 26) and the A1A5 (8827 and 28) assemblies contain most of the micro-programming circuits that control the entire instrument.

The A1A4 assembly contains the qualifier select circuit shown on 8825 and the seven flip/flops, ROMs and qualifier flip/flops shown on 8826.

Because of the number of inputs from other assemblies to the circuit shown on 8825 the inputs are shown at the bottom of the page. The only output on 8825 is the output of U1 labeled A 26. This output provides the eighth address bit for the ROMs shown on 8826.

U18, U9, U19, U20, U21, U22 and U23 are four input one-of-sixteen selectors. The A, B, C and D inputs are positive logic binary 1 2 4 8 format from the A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub> and A<sub>3</sub> outputs of the seven state flip/flops shown on 8826. These inputs are applied to all of the selectors in parallel. However, only one of the selectors is active at any given time.

One-of-ten selector U10 (only 7 outputs are used) is controlled by the A<sub>4</sub>, A<sub>5</sub> and A<sub>6</sub> outputs of the seven state flip/flops shown on 8826. All of the U10 outputs are high except the one selected. The

D input to U20 is grounded because only three data bits are required to select the output (BCD 4, 2 and 1).

It is readily apparent from the circuit configuration that the state for any of the inputs to the code selectors is easily detected. As an example, assume that the inputs from the seven state flip/flops are all low. The U20 Q<sub>0</sub> output is low and U23 (code 0) is selected. Since the A, B, C and D inputs to U23 are all low, input S<sub>0</sub> is selected. The S<sub>0</sub> input is qualifier P1041. If an entry has not been made, P1041 is low the W output of U23 is high and the instrument is held in state 0/0. If the P1041 input is high, the W output of U23 goes low, the output of U3 goes high and the next state is selected.

In the foregoing example, assume that qualifier P1041 was high. Referring to the ASM chart it may be seen that the next state is 4/0 (100 0000). Since the input to U20 is now a 4 (100) U20 is selected. The A, B, C and D inputs to U20 are all low so once again S<sub>0</sub> input is selected. The input to S<sub>0</sub> is from the P741 flip/flop shown on 8826. It may be seen on the algorithm that if P741 is high the next state is 0/1, if low, 6/0.

AND gate U2C combines CK A 41 and CK B 41 when they are both high to provide inputs to U20 and U23. These inputs are used in states 3/1, 5/0, 5/10 and 5/12.

**Model 8660B**

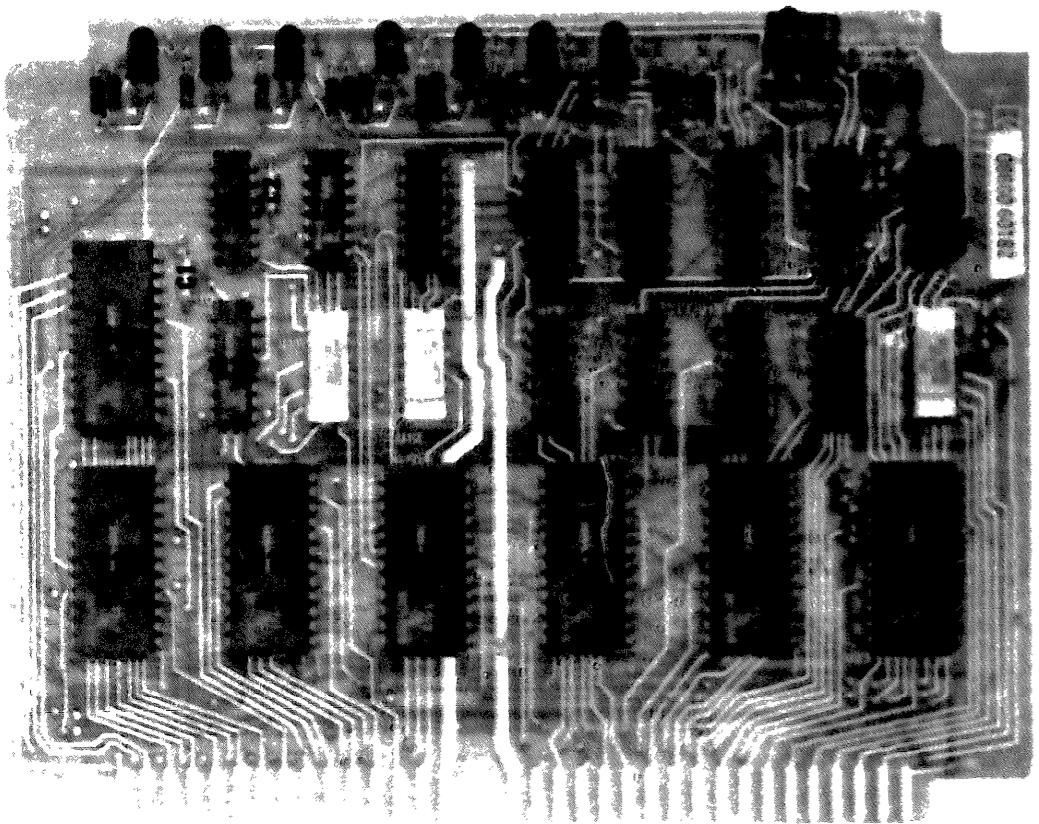


Figure 8-68. *P/O A1A4 ROM Input Assy Component Locations (Part 1)*

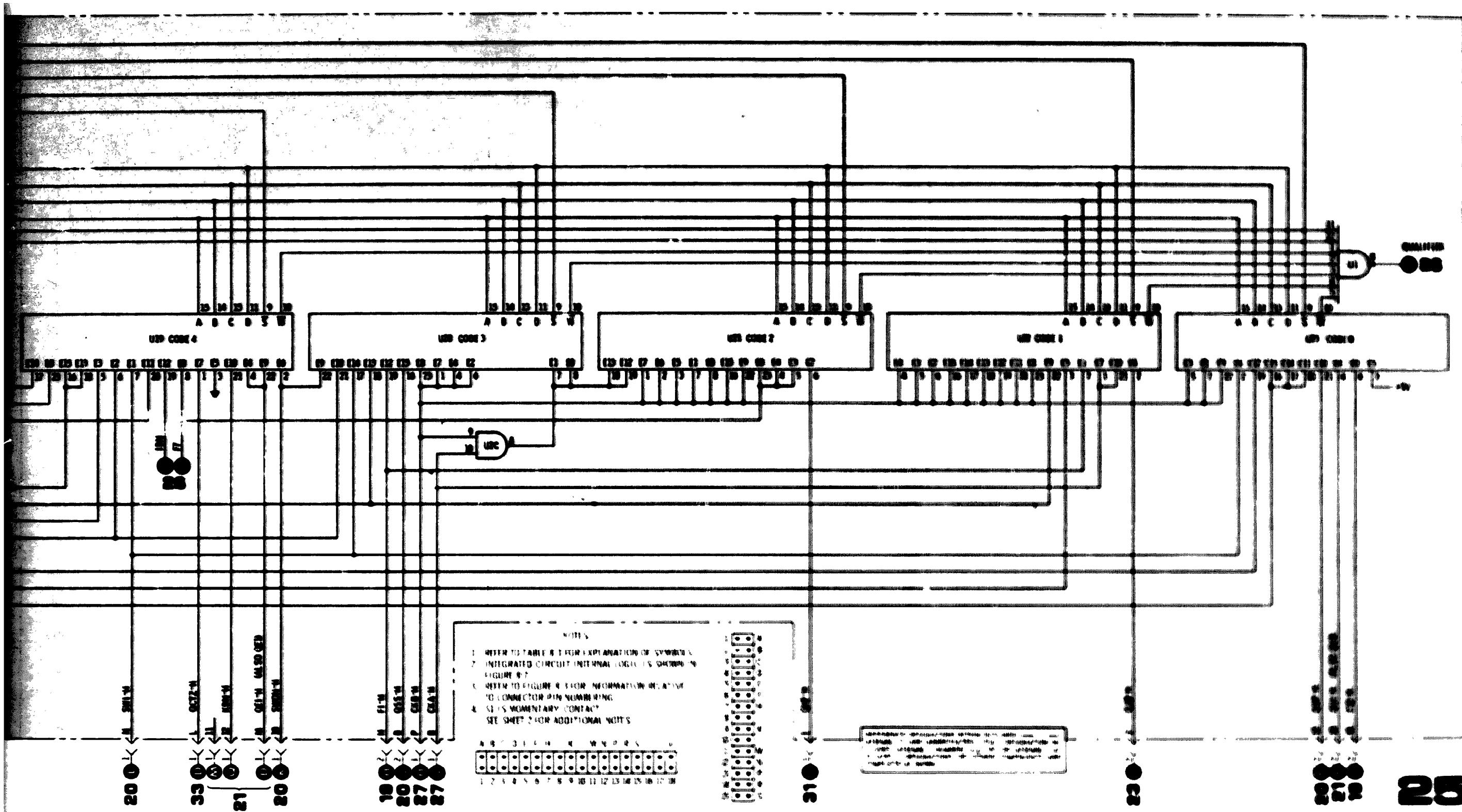


Figure 8-6b. Processing Module Input Bus Stage

## SERVICE SHEET 26

**P/O ROM INPUT ASSEMBLY A1A4**

The A1A4 (SS25 and 26) and the A1A5 (SS27 and 28) assemblies contain most of the micro-programming circuits that control the entire instrument.

The A1A4 assembly contains the qualifier select circuit shown on SS25. The seven-state flip/flops, ROM's, and qualifier flip/flops are shown on SS26.

Seven J-K flip/flops, U6A, U5A, U4A, U7B, U5B, U6B and U4B form the seven-state flip/flops. The outputs of these flip/flops provide seven of the eight address bits required to control the next state outputs of ROM's U11, U12 and U17. The outputs also control the qualifier selector circuits shown on SS25 and the output instruction selectors on SS28 and SS19.

The eighth address bit to the ROM's is supplied by the selector circuit shown on SS25. When the seven-state flip/flops are clocked all four of the outputs from ROM U11 and three of the outputs from ROM U12 determine the next machine state. The remaining output of ROM U12 and all four of the outputs from ROM U17 are used directly as output instructions.

The light emitting diodes (LED's) connected between the Q outputs of the seven-state flip/flops and +5V indicate the machine state. These LED's light when the Q outputs of the flip/flops go low. Proper utilization of these LED's in the manual test mode will enable the technician to quickly isolate the cause of a problem to the assembly or even the circuit level. In the automatic mode of operation the machine states change so rapidly that the LED's serve no useful purpose.

At the far left of the schematic, U7, a J-K flip/flop is used to set the manual test mode. When TP9 is momentarily grounded Q goes low to inhibit the clock gate, USA. Momentarily grounding TP8 will reset the flip/flop causing the Q output to go high and enable the clock gate, USA. This returns the instrument to the automatic mode. The PRDT-L (power detect) input, which is low when the instrument is first turned on ensures that the automatic mode of operation is selected.

In order to use the manual test mode facilities it is necessary to momentarily ground or pulse the manual test point, TP9. The machine state may be 0/0 (all LED's out) or may be any state in an operation sequence. If state 0/0 test point, is desired, momentarily ground or pulse the state 0/0 test point, TP10. Any machine state may now be set by momentarily grounding or pulsing the appropriate seven-state flip/flop test points.

## SERVICE SHEET 26 (Cont'd)

If, for instance, TP7, TP4 and TP1 were momentarily grounded or pulsed, the machine state would be 4/9 (100 1001). The ASM chart shows the qualifier QE1 (qualifier entry instruction) following state 4/9. If an entry instruction (CF, STEP or SWP) is being made (key held down), pressing the MAN SW microswitch should cause the next state to be 5/9 (101 1001) as shown by the LED's. If the state 5/9 is not present, the operation was incorrect. Refer to Table 8-2, Mnemonics Information, locate qualifier QE1, read across the page to determine where the qualifier originates and refer to the applicable service sheet to effect necessary repairs.

When NAND gate USA pin 1 goes low pin 3 goes high to enable AND gate U2B. The clock pulse source is now flip/flop U15B. Normally, the R and CK inputs to U15B are held low by R2 and the Q output is high. As soon as SW1 NC contacts are opened the R input to U15B goes high. When the SW1 NO contacts are closed the U15B CK goes high but this does not affect the output since J-K flip/flops are triggered by a negative-going transition. When SW1 is released it is returned to the NC position. The negative-going transition at the CK input causes U15B Q to go low. The output of AND gate U2B goes low and the outputs of inverters U13C and U13F go high. When the NC contacts of SW1 are again closed, the R input to U15B again goes low to cause the Q output to go high. AND gate U2B output goes high and the outputs of inverters U13C and U13F go low to clock the seven-state flip/flops.

AND gates U2A and U2D are used to reset the seven-state flip/flops to state 0/0 when PRDT-L is low or when TP10 is momentarily grounded or pulsed.

The J-K flip/flops shown in the lower part of the schematic provide qualifiers; most of which are used in the selector circuits shown on SS25. These flip/flops are all clocked by the system (1 MHz) clock. They are also reset (Q goes high) when PRDT-L is active or TP10 is momentarily grounded or pulsed.

Flip/flop U16A generates the P7 qualifier. The K inputs is an instruction (KP740) which appears in states 2/9 and 1/0. The J input goes high whenever JP7B-L or (JP7A, ILD)-L goes low. P7 is fundamentally the sweep flip/flop but it also functions in the remote mode.

U15A is the sweep ramp qualifier flip/flop P8. It appears in states 6/11 and 4/11.

U14B (IUP) inhibits the sweep up operation when QCTM45 (qualifier count maximum) on the sweep count assembly A1A8 goes high.

U14A (IDN) inhibits the sweep down operation when QCTZ (qualifier count zero) on the sweep count assembly A1A8 goes high.

U16B (P2) is active (Q low) only for the first keyboard entry.

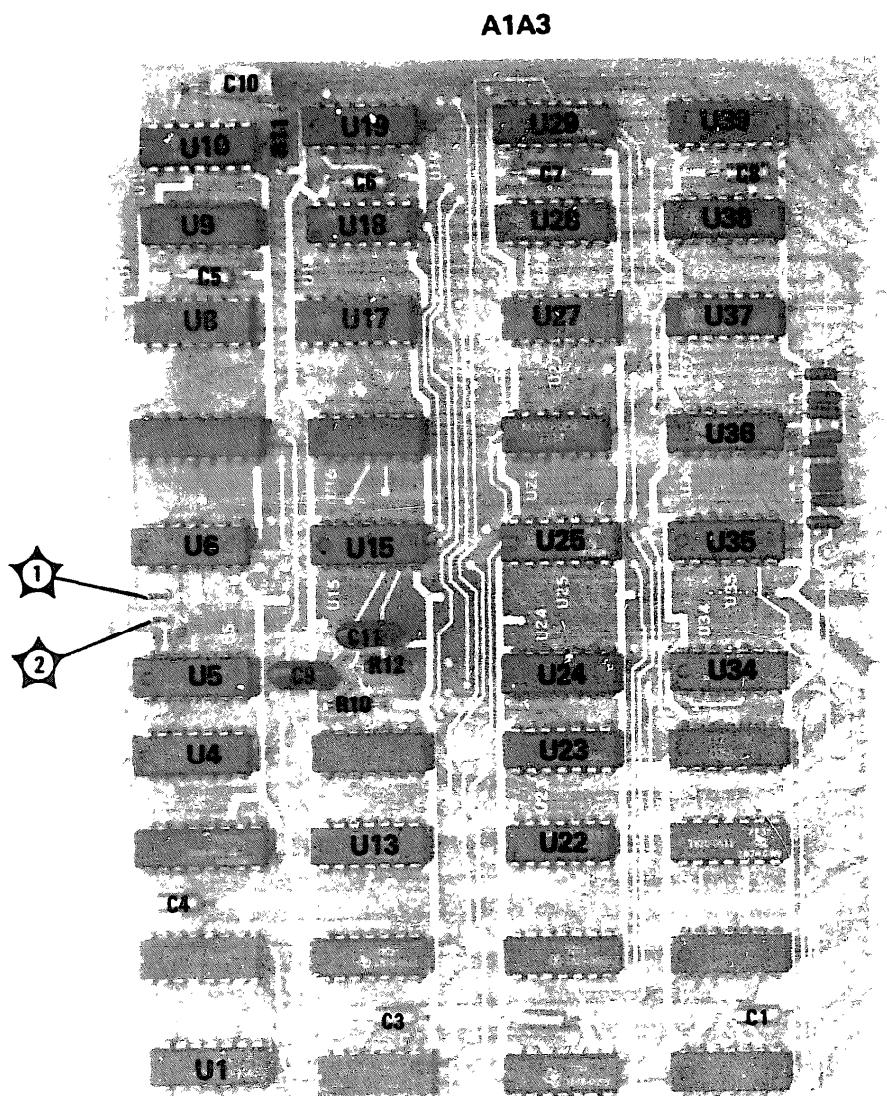


Figure 8-70. P/O A1A3 Readout Control Assy Component Locations (Part 2)

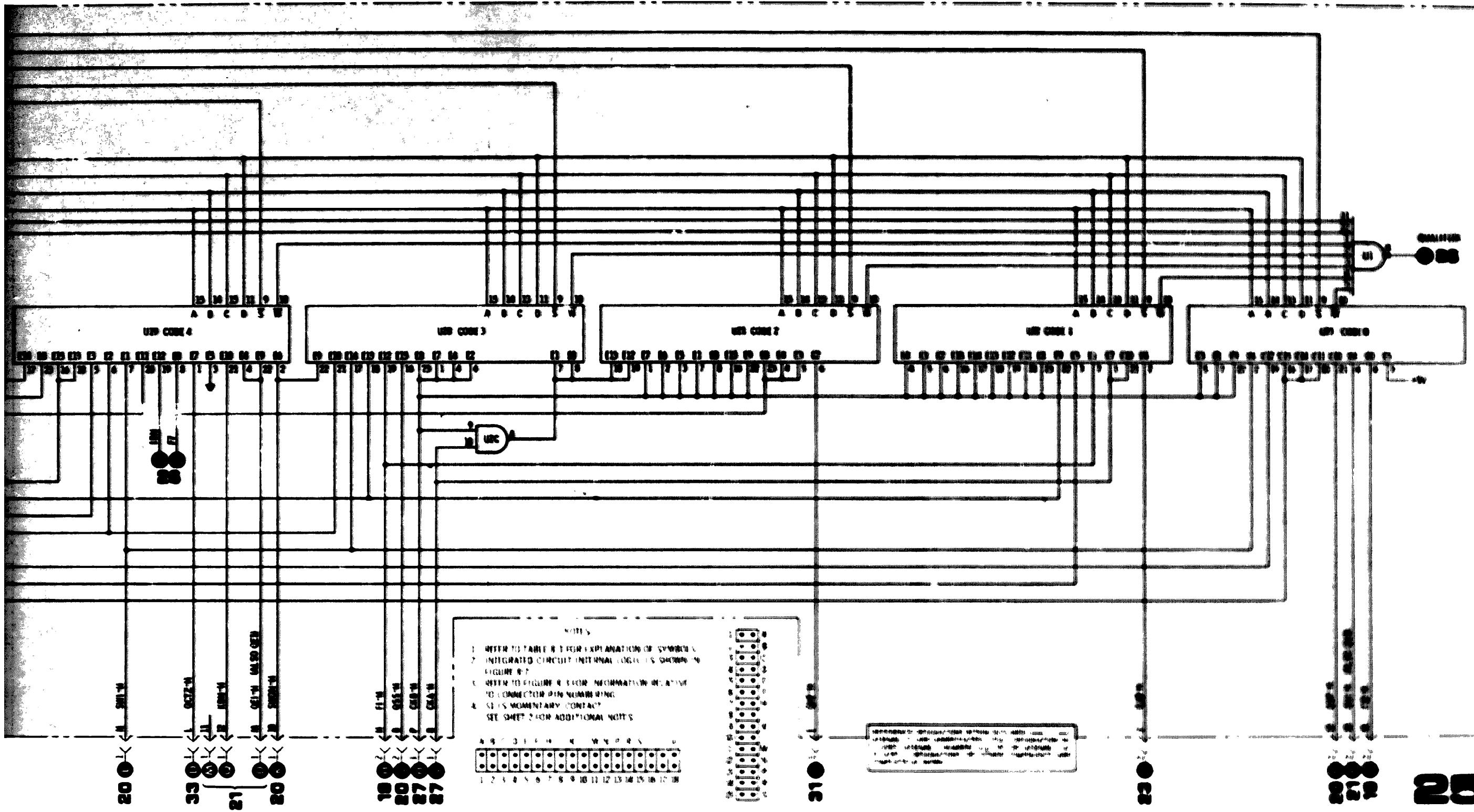


Figure 6.26 Performance of the Ingest API.

## SERVICE SHEET 27

**P/O ROM OUTPUT ASSEMBLY A1A5**

The A1A4 (SS25 and 26) and the A1A5 (SS27 and 28) assemblies contain most of the micro-programming circuits that control operation of the entire instrument.

U17, shown in the center of the schematic, is the major control element for most of the circuits shown on this service sheet. It is a preset counter but is used only as a binary counter. When U17 is not active the master reset,  $\overline{MR}$ , input is low and all of the Q outputs are held low.

Any of the clock inputs, except the system clock, will inhibit NAND gate U9B and enable binary counter U17 by removing the reset input.

As an example of circuit operation, assume that the CK12-L input goes low. The output of AND gate U11A goes low to cause the output of NAND gates U9A and U9B to go high. This inhibits the MR input to U17. Since the output of U20A is low at this time, the output of inverter U10C is high and the clock is coupled through NAND gate U9C to U17.

When CK12-L went low it was inverted by U4E and used to enable NAND gate U19A. U19A, U19B, U19C and U20A form a detect circuit which provides the CKA-H output for the binary number selected.

In the case of CK12-L, when the output of U17 reaches 12 (1100), the output of U19A goes low and causes the output of U20A to go high.

While U19 and U20A were detecting a specific binary number, U18 was also detecting counts of

10, 11 and 12. When the count of 10 (1010) is reached the output of NAND gate U18C goes low and causes the output of U18D to go high. When the count of 11 (1011) is reached the CKB-H output remains high because NAND gate U18C is still enabled. When the count of 12 is reached NAND gate U18A is enabled so CKB-H is still high. The outputs of U20A (CKA) and U18D (CKB) are ANDed together in the system, and when the 12 count is reached, the combined signal enables the state machine to go to the next state. In doing so, the CK12-L input goes high again causing reset of U17 through U11A and U9B.

If the CK13-L were selected, circuit operation would be similar, except that CKA-H would go high only on the 13th clock and CKB-H would be high for the counts of 10, 11, 12 and 13.

NAND gate U18B produces the B9-L output which goes low on the 9th clock pulse. It is used in the readout control assembly to limit a normal ten-clock train to 9 clocks.

The output labeled OPR-L is used in the readout control assembly to set the two least significant readout digits to 0 in Option 004 instruments.

Output A2TR-H enables output gates for the 12 digit portion of the A register assembly.

The A4 and A5 inputs are from the seven-state flip/flops in the switch control assembly, A1A4. The 2-bit code on these inputs is decoded by the gates shown in the lower right corner of the schematic to produce one of four outputs. Output G20 enables the code 0 instruction decoder on A1A1. The outputs labeled 28, E, F and G enable the code 1, 2 and 3 instruction decoders shown on SS28.

A1A5

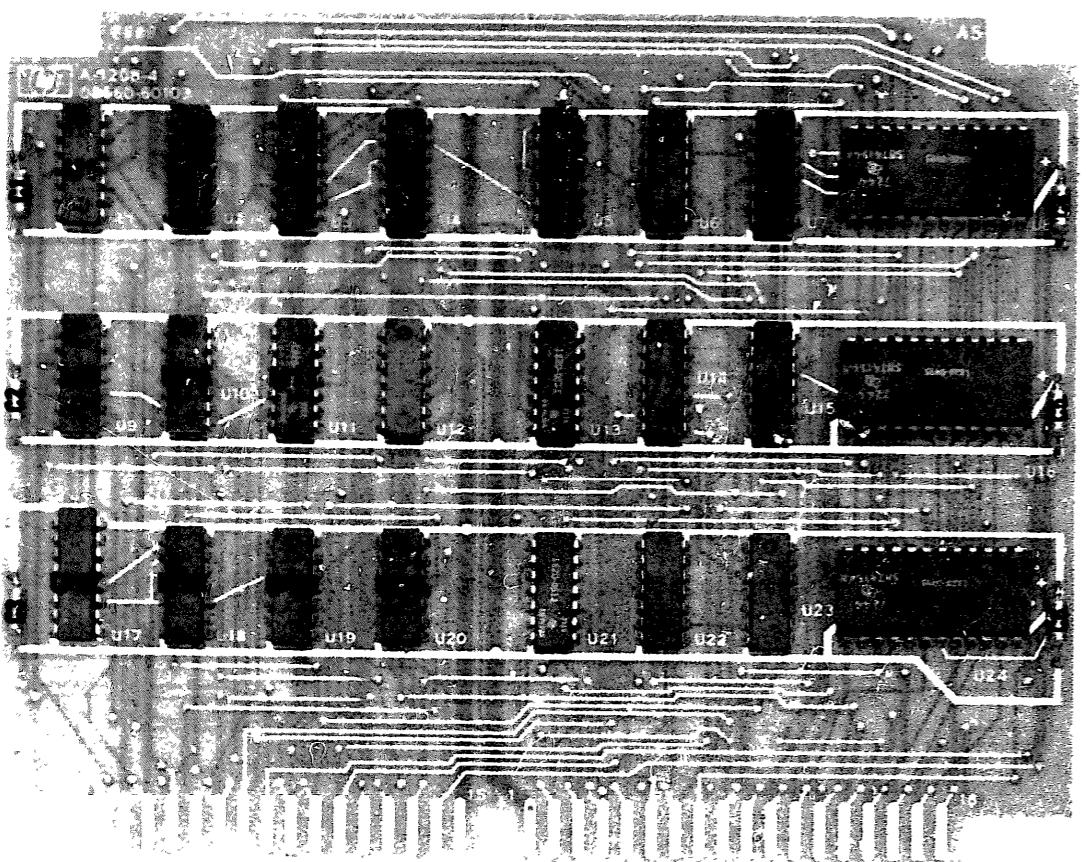
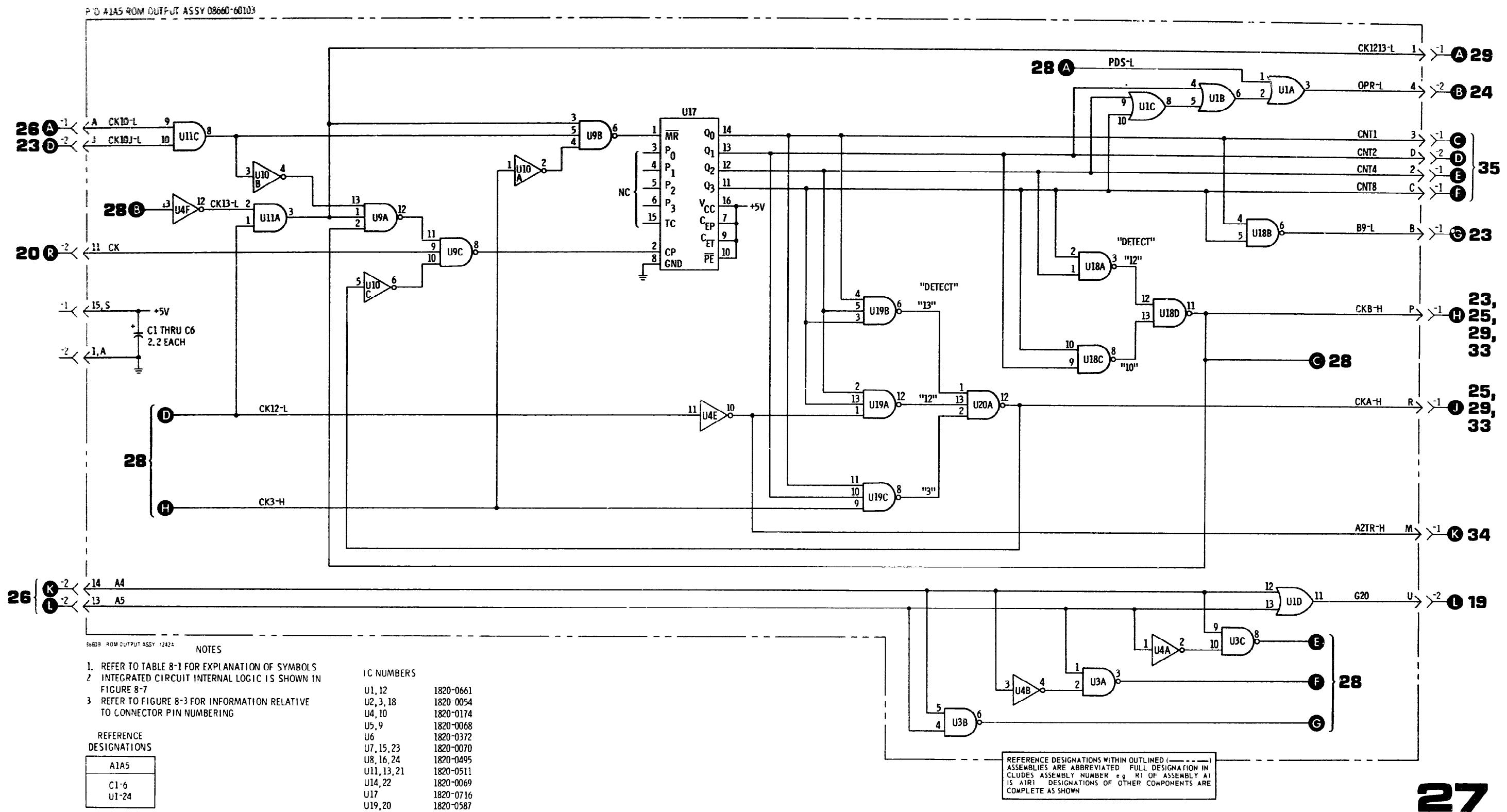


Figure 8-72. P/O A1A5 ROM Output Assy Component Locations (Part 1)



## SERVICE SHEET 28

**P/O ROM OUTPUT ASSEMBLY A1A5**

The A1A4 (SS25 and 26) and the A1A5 (SS27 and 28) assemblies contain most of the micro-programming circuits that control operation of the entire instrument.

All of the gates shown on SS28 are controlled by the 4-line-to-16-line instruction decoders U24, U16 and U8. These decoders have six inputs, all of which are required to decode to the single output. All outputs are high except the one decoded.

Note that the decoders are labeled CODE 1, CODE 2 and CODE 3. These code numbers and the output numbers of the decoders quickly reveal the machine state code as shown on the algorithm, which is the state of the seven-state flip/flops in the ROM input assembly.

The gates shown combine the decoder outputs to provide the desired instruction.

As an example, assume that output 6 of U24 is low. Decoder U24 is labeled CODE 1 (001) and the decoded output is 6 (0110). The state code is 1/6 and the outputs of the seven-state flip/flops is 001 0110. Instructions (JUS, KF3, JF2)-L are low.

The example quoted for the instructions in state 1/6 is very simple. Generation of many of the instructions is more complex when the instruction is decoded from several machine states.

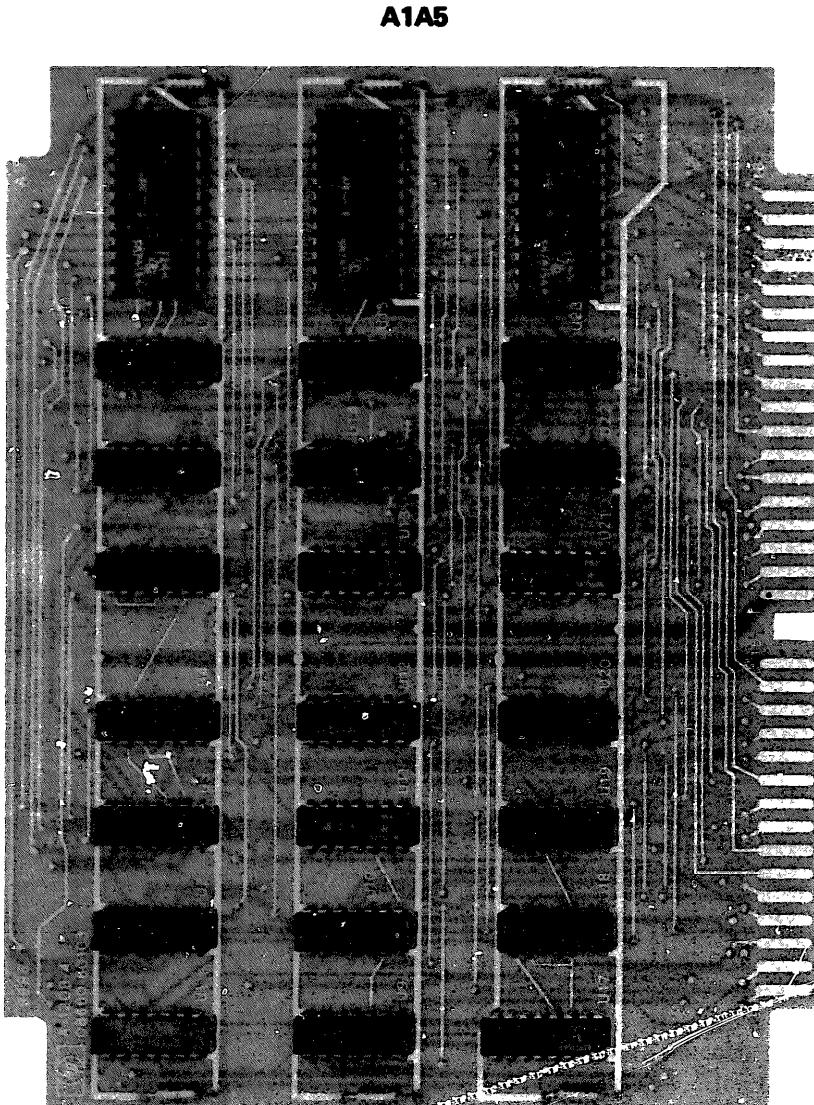
Take, as an example, state 2/5 (output 5 of U16). Following the line across the schematic leads to instruction SCDP-L, set center frequency decimal point - assertive state low. The state 2/5 low output from U16 is applied to inverter U4C and its high output causes TTC-H, T bus to center frequency register - assertive state high, to go high. The state 2/5 output from U16 is also applied to AND gate U13B, the pin 12 input to NAND gate U2D goes low and KTT-H keyboard to T bus - assertive state high, goes high.

The instruction SCDP-L occurs only in state 2/5. However, some of the other instructions generated in state 2/5 are also generated in other states.

Instruction TTC-H is also made to go high when NAND gate U22B pin 8 CTR-H goes high. This occurs when any one of the inputs to U22B goes low in states 1/15, 1/14, 2/0 or 2/1.

Instruction KTT-H also goes high when the pin 5 input to U13B goes low in state 1/4. KTT-H goes high and JF3-L goes low when any of the inputs to AND gate U6A go low in states 1/13, 1/12 or 1/11. Input pin 5 of U21B also causes JF3-L to go low in state 1/C, but does not affect KTT-H.

Any of the instruction paths may be quickly checked by setting the instrument to the manual test mode and to the state to be checked. The machine state block in the algorithm indicates all instructions required in the set state.



P/O A1A5 ROM OUTPUT ASSY 08660-60160

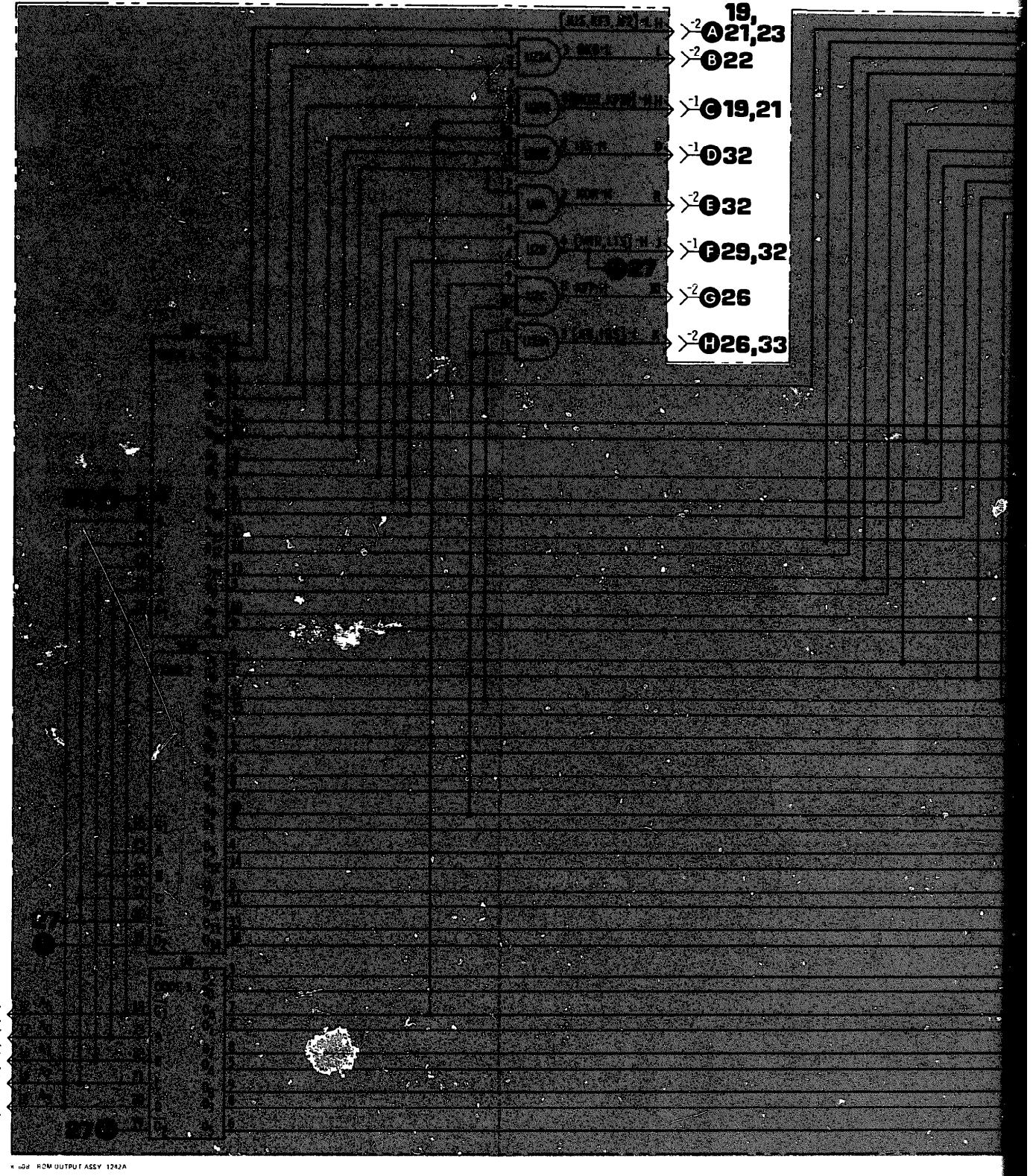


Figure 8-74. P/O A1A5 ROM Output Assy Component Locations (Part 2)