

# **Quad Low Power, Precision Comparator**

## CMP04

### **FEATURES**

High Gain: 200 V/mV Typ

Single- or Dual-Supply Operation Input Voltage Range Includes Ground

Low Power Consumption (1.5 mW/Comparator)

Low Input Bias Current: 100 nA Max Low Input Offset Current: 10 nA Max Low Offset Voltage: 1 mV Max

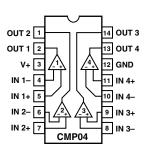
Low Output Saturation Voltage: 250 mV @ 4 mA Logic Output Compatible with TTL, DTL, ECL, MOS,

and CMOS

Directly Replaces LM139/LM239/LM339 Comparators

### PIN CONNECTIONS

14-Lead SOIC



### **GENERAL DESCRIPTION**

Four precision independent comparators comprise the CMP04. Performance highlights include a very low offset voltage, low output saturation voltage, and high gain in a single-supply design. The input voltage range includes ground for singlesupply operation and V- for split supplies. A low power supply current of 2 mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

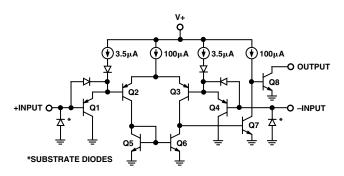


Figure 1. Simplified Schematic (1/4 CMP04)

### TYPICAL INTERFACE

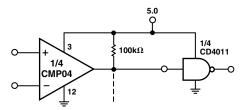


Figure 2a. Driving CMOS

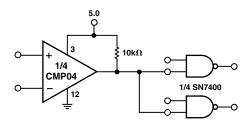


Figure 2b. Driving TTL

### REV. D

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## CMP04—SPECIFICATIONS

## **ELECTRICAL CHARACTERISTICS** (@ V+ = 5 V, T<sub>A</sub> = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Input Offset Voltage	Vos	$R_S = 0 \Omega$ , $R_L = 5.1 k\Omega$ , $V_O = 1.4 V^1$		0.4	1	mV
Input Offset Current	$I_{OS}$	$I_{IN}(+) - I_{IN}(-), R_L = 5.1 \text{ k}\Omega, V_O = 1.4 \text{ V}$		2	10	nA
Input Bias Current	$I_{\mathrm{B}}$	$I_{IN}(+)$ or $I_{IN}(-)$		25	100	nA
Voltage Gain	$A_{V}$	$R_L \ge 15 \text{ k}\Omega, V + = 15 \text{ V}^2$	80	200		V/mV
Large Signal Response Time	t <sub>r</sub>	$V_{IN}$ = TTL Logic Swing, $V_{REF}$ = 1.4 $V^3$				
		$V_{RL} = 5 \text{ V}, R_{L} = 5.1 \text{ k}\Omega$		300		ns
Small Signal Response Time	t <sub>r</sub>	$V_{IN} = 100 \text{ mV Step}^3$ , 5 mV Overdrive				
		$V_{RL} = 5 \text{ V}, R_L = 5.1 \text{ k}\Omega$		1.3		μs
Input Voltage Range	CMVR	Note 4	0		V+ - 1.5	V
Common-Mode Rejection Ratio	CMRR	Notes 2, 5	80	100		dB
Power Supply Rejection Ratio	PSRR	$V+ = 5 V \text{ to } 18 V^2$	80	100		dB
Saturation Voltage	$V_{OL}$	$V_{IN}(-) \ge 1 \text{ V}, V_{IN}(+) = 0, I_{SINK} \le 4 \text{ mA}$		250	400	mV
Output Sink Current	I <sub>SINK</sub>	$V_{IN}(-) \ge 1 \text{ V}, V_{IN}(+) = 0, V_O \le 1.5 \text{ V}$	6	16		mA
Output Leakage Current	$I_{LEAK}$	$V_{IN}(+) \ge 1 \text{ V}, V_{IN}(-) = 0, V_{O} = 30 \text{ V}$		0.1	100	nA
Supply Current	I+	$R_L = \infty$ , All Comps V+ = 30 V		0.8	2.0	mA

#### NOTES

Specifications subject to change without notice.

#### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply Voltage
Differential Input Voltage
Input Voltage0.3 V to +36 V
Operating Temperature Range
CMP04FS40°C to +85°C
Junction Temperature $(T_J)$ 65°C to +150°C
Storage Temperature Range65°C to +150°C
Input Current ( $V_{IN} < -3.0 \text{ V}$ ) 50 mA
Output Short Circuit to GNDContinuous
Lead Temperature (Soldering, 60 sec)300°C

Package Type	$\theta_{\mathrm{JA}}^{2}$	$\theta_{ m JC}$	Unit	
14-Lead SOIC	120	36	°C/W	

### NOTES

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ORDERING GUIDE**

Model	$T_A = 25^{\circ}C$	Temperature	Package	Package
	$V_{OS}$	Ranges	Descriptions	Options
CMP04FS	1 mV	−40°C to +85°C	14-Lead SOIC	R-14

#### **CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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 $<sup>^{1}</sup>$ At output switch point,  $V_{O} = 1.4 \text{ V}$ ,  $R_{S} = 0 \Omega$  with V+ from 5 V, and over the full input common-mode range (0 V to V+ -1.5 V).

<sup>&</sup>lt;sup>2</sup>Guaranteed by design.

<sup>&</sup>lt;sup>3</sup>Sample tested.

<sup>&</sup>lt;sup>4</sup>The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ – 1.5 V, but either or both inputs can go to 30 V without damage.

 $<sup>{}^{5}</sup>R_{L}$  ≥ 15 kΩ, V+ = 15 V,  $V_{CM}$  = 1.5 V to 13.5 V.

 $<sup>^2\</sup>theta_{JA}$  is specified for worst-case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device soldered to printed circuit board for SOIC package.

## **ELECTRICAL CHARACTERISTICS** (@ V+ = 5 V, $-40^{\circ}$ C $\leq$ T<sub>A</sub> $\leq$ +85°C for CMP04FS, unless otherwise noted.)

Symbol	Conditions	Min	CMP04F <sup>1</sup> Tvp	Max	Unit
-		1 11222	-JP		
V <sub>OS</sub>			1		mV
_	0		1	_	mV
los					nA
				-	nA
	$V_O = 1.4 \text{ V}$		4	20	nA
$I_{B}$	$I_{IN}(+)$ or $I_{IN}(-)$		40	200	nA
$A_{ m V}$	$R_L \ge 15 \text{ k}\Omega, V + = 15 \text{ V}^3$	70	125		V/mV
t <sub>r</sub>	$V_{IN}$ = TTL Logic Swing		300		ns
	$V_{REF} = 1.4 \text{ V}^4$		300		ns
	$V_{RL} = 5 \text{ V}, R_{L} = 5.1 \text{ k}\Omega$		300		ns
t.	$V_{IN} = 100 \text{ mV Step}^4$		1.3		μs
1	5 mV Overdrive		1.3		us us
	$V_{RI} = 5 \text{ V}, R_{I} = 5.1 \text{ k}\Omega$		1.3		μs
CMVR	Note 5	0		V+ - 1.5	V
CMRR	Notes 1, 3	60	100		dB
PSRR	V + = 5 V  to  18 V	80	100		dB
Vor	$V_{TM}(-) \ge 1 \text{ V}, V_{TM}(+) = 0,$		250	700	mV
OL	11(()		250	700	mV
Icry	011111	5			mA
-SINK					mA
ILEAN	1111		<del>-</del> -	200	nA
-LEAK	1111				nA
T+					mA
1.					mA
	t <sub>r</sub> t <sub>r</sub> CMVR  CMRR	$\begin{array}{c} V_{OS} & R_S = 0 \; \Omega,  R_L = 5.1 \; k\Omega \\ V_O = 1.4 \; V^2 \\ I_{OS} & I_{IN}(+) - I_{IN}(-) \\ R_L = 5.1 \; k\Omega \\ V_O = 1.4 \; V \\ I_B & I_{IN}(+) \; \text{or} \; I_{IN}(-) \\ A_V & R_L \geq 15 \; k\Omega,  V+ = 15 \; V^3 \\ t_r & V_{IN} = TTL \; \text{Logic Swing} \\ V_{REF} = 1.4 \; V^4 \\ V_{RL} = 5 \; V, \; R_L = 5.1 \; k\Omega \\ t_r & V_{IN} = 100 \; \text{mV Step}^4 \\ 5 \; \text{mV Overdrive} \\ V_{RL} = 5 \; V, \; R_L = 5.1 \; k\Omega \\ \text{CMVR} & \text{Note 5} \\ \text{CMRR} & \text{Notes 1, 3} \\ \text{PSRR} & V+ = 5 \; V \; \text{to 18 V} \\ V_{OL} & V_{IN}(-) \geq 1 \; V, \; V_{IN}(+) = 0, \\ I_{SINK} \leq 4 \; \text{mA} \\ I_{SINK} & V_{IN}(-) \geq 1 \; V, \\ V_{IN}(+) = 0, \; V_O \leq 1.5 \; V \\ I_{LEAK} & V_{IN}(+) \geq 1 \; V, \\ V_{IN}(-) = 0, \; V_O = 30 \; V \\ \end{array}$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$ \begin{array}{ c c c c c } \textbf{Symbol} & \textbf{Conditions} & \textbf{Min} & \textbf{Typ} \\ \hline \\ V_{OS} & R_S = 0 \ \Omega, \ R_L = 5.1 \ k\Omega \\ & V_O = 1.4 \ V^2 & 1 \\ \hline I_{OS} & I_{IN}(+) - I_{IN}(-) & 4 \\ & R_L = 5.1 \ k\Omega & 4 \\ & V_O = 1.4 \ V & 4 \\ \hline I_B & I_{IN}(+) \ or \ I_{IN}(-) & 40 \\ \hline A_V & R_L \ge 15 \ k\Omega, \ V^+ = 15 \ V^3 & 70 & 125 \\ \hline t_r & V_{IN} = TTL \ Logic \ Swing & 300 \\ \hline V_{REF} = 1.4 \ V^4 & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 300 \\ \hline V_{RL} = 5 \ V, \ R_L = 5.1 \ k\Omega & 500 \\ \hline CMRR & Notes \ I, \ 3 & 60 \ 100 \\ \hline V_{RL} = 5 \ V, \ V_{RL} = 5.1 \ k\Omega & 500 \\ \hline V_{RL} = 5 \ V, \ V_{RL} = 5.1 \ V & 500 \\ \hline I_{SINK} \ V_{RL} = 5 \ V, \ V_{RL} = 5.1 $	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

#### NOTES

Specifications subject to change without notice.

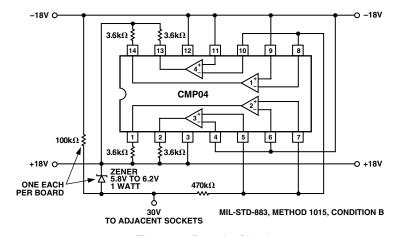


Figure 3. Burn-In Circuit

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 $<sup>^1</sup>R_L \geq$  15 kΩ, V+ = 15 V,  $V_{CM}$  = 1.5 V to 13.5 V.

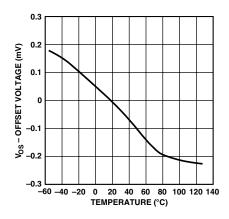
<sup>&</sup>lt;sup>2</sup>At output switch point,  $V_0 = 1.4 \text{ V}$ ,  $R_S = 0 \Omega$  with V+ from 5 V; and over the full input common-mode range (0 V to V+ -1.5 V).

<sup>&</sup>lt;sup>3</sup>Guaranteed by design.

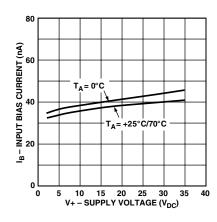
<sup>&</sup>lt;sup>4</sup>Sample tested.

 $<sup>^{5}</sup>$ The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ - 1.5 V, but either or both inputs can go to +30 V without damage.

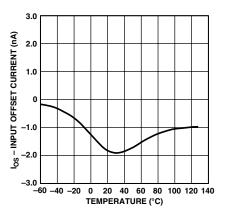
## **CMP04**—Typical Performance Characteristics



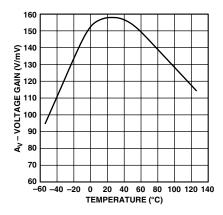
TPC 1. Offset Voltage vs. Temperature



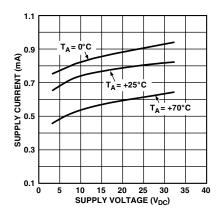
TPC 2. Input Bias Current vs. V+ and Temperature



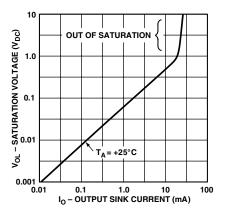
TPC 3. Input Offset Current vs. Temperature



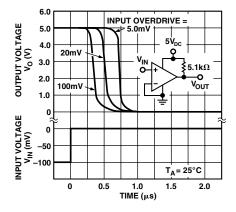
TPC 4. Voltage Gain vs. Temperature



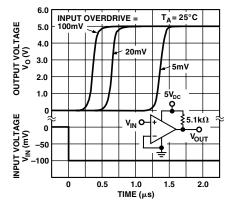
TPC 5. Supply Current vs. Supply Voltage



TPC 6. Output Voltage vs. Output Current and Temperature



TPC 7. Response Time for Various Input Overdrives—Negative Transition



TPC 8. Response Time for Various Input Overdrives—Positive Transition

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## TYPICAL APPLICATIONS

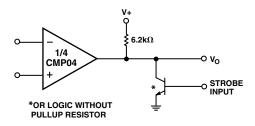


Figure 4. Output Strobing

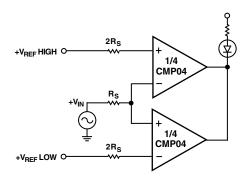


Figure 5. Limit Comparator

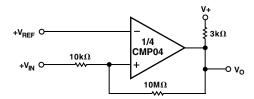


Figure 6. Noninverting Comparator with Hysteresis

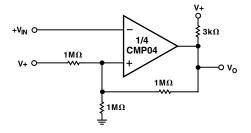


Figure 7. Inverting Comparator with Hysteresis

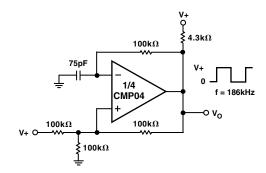


Figure 8. Square Wave Oscillator

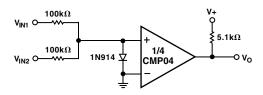


Figure 9. Comparing Input Voltages of Opposite Polarity

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## CMP04

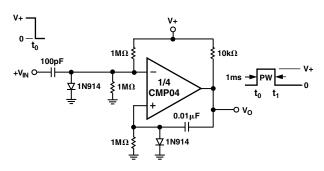


Figure 10. One-Shot Multivibrator

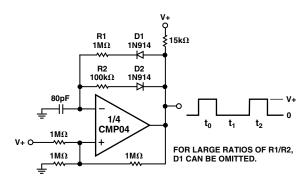


Figure 12. Pulse Generator

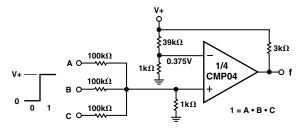


Figure 11. AND Gate

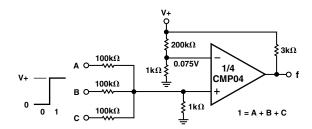


Figure 13. OR Gate

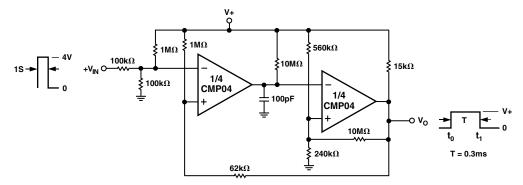


Figure 14. One-Shot Multivibrator with Input Lockout

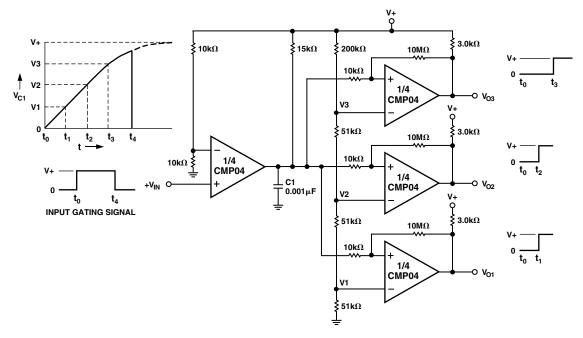


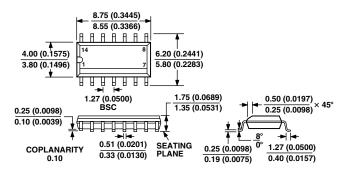
Figure 15. Time Delay Generator

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### **OUTLINE DIMENSIONS**

## 14-Lead Standard Small Outline Package [SOIC] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

## **Revision History**

Location	Page
3/03—Data Sheet changed from REV. C to REV. D.	
Renumbered TPCs and Figures	Global
Deletion of 14-Lead CERDIP and 14-Lead PDIP information	Global
Changes to FEATURES	1
Changes to PIN CONNECTIONS	1
Changes to ABSOLUTE MAXIMUM RATINGS	2
Changes to ORDERING GUIDE	2
Changes to ELECTRICAL CHARACTERISTICS	3
Removal of DICE CHARACTERISTICS, WAFER TEST LIMITS, and TYPICAL ELECTRICAL CHARACTERISTICS sections	4
Changes to TPCs 2, 5, and 6	4
Updated OUTLINE DIMENSIONS	8

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