32位移位器设计Shift.v

module shift(d,sa,right,arith,sh);

input [31:0] d;

input [4:0] sa;

input right,arith;

output [31:0] sh;

reg [31:0] sh;

always@(\*) begin

if(!right)

sh = d << sa;

else

if(!arith)

sh = d >> sa;

else

sh = $signed(d) >>> sa;

end

endmodule

寄存器堆的设计regfile.v

module regfile (rna,rnb,d,wn,we,clk,clrn,qa,qb);

input [4:0] rna,rnb,wn;

input [31:0] d;

input we,clk,clrn;

output [31:0] qa,qb;

reg [31:0] register [1:31];

assign qa = (rna == 0) ? 0 : register[rna];

assign qb = (rnb == 0) ? 0 : register[rnb];

always @ (posedge clk or negedge clrn) begin

if (clrn == 0) begin

integer i;

for (i=1; i<32; i=i+1)

register[i] <= 0;

end

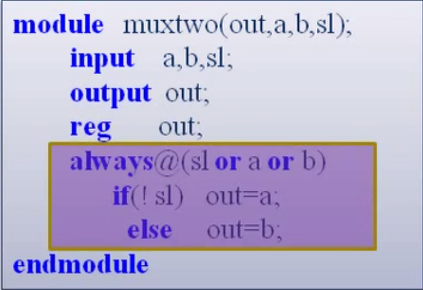
else begin

if ((wn != 0) && (we == 1))

register[wn] <= d;

end

end endmodule



Alu的设计alu.v

module alu (a,b,aluc,r,z);

input [31:0] a,b;

input [3:0] aluc;

output [31:0] r;

output z;

assign r=cal (a,b,aluc);

function [31:0] cal;

input [31:0] a,b;

input [3:0] aluc;

casex (aluc)

4'bx000: cal =a+b;

4'bx100: cal =a-b;

4'bx001: cal =a&b;

4'bx101: cal =a|b;

4'bx010: cal =a^b;

4'bx110: cal ={b[15:0],16'h0};

4'bx011: cal =b<<a[4:0];

4'b0111: cal =b>>a[4:0];

4'b1111: cal =$signed(b) >>>a[4:0];//算术右移

endcase

endfunction

endmodule