



CONFIDENTIAL

MAX8966/MAX8997 DATASHEET

FOR

SAMSUNG APPLICATION PROCESSORS C110/C111 and C210

Rev 01

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High Efficiency, Low I_Q , PMIC with Dynamic Voltage Management for Mobile Applications

1 General Description

The MAX8966/MAX8997 power management ICs are optimized for devices using Samsung S5PC110, and S5PC111/C210 ® processors, including smart cellular phones, PDAs, internet appliances, and other portable devices requiring substantial computing and multimedia capability and low power consumption.

Applications

PDA, Palmtop, and Wireless Handhelds

Smart Cell phones

Portable GPS Navigation

Personal Media Players

Digital Cameras

Features

- Optimized for Samsung C110/C111/C210 ®Processors
- 30VDC Single input Fully Integrated Linear Charger
CC, CV, and Die temperature control
- 7 Highly Efficiency Synchronous Step-Down Converters
 - Buck1 Serial Programmed for Core/ maximum
 - Buck2 Serial Programmed for Internal Memory /
 - Buck3 for Memory/ maximum
 - Buck4 for Camera Core
 - Buck5 for 3D
 - Buck6 for PA Power
 - Buck7 for low power consumption
- 21 LDO Regulators. Programmable Voltage Options for all LDOs
 - LDO1 @ 150mA
 - LDO2 @ 150mA
 - LDO3 @ 150mA
 - LDO4 @ 300mA
 - LDO5 @ 150mA
 - LDO6 @ 300mA
 - LDO7 @ 300mA
 - LDO8 @ 150mA
 - LDO9 @ 450mA
 - LDO10 @ 150mA
 - LDO11 @ 300mA
 - LDO12 @ 150mA
 - LDO13 @ 150mA
 - LDO14 @ 300mA
 - LDO15 @ 300mA
 - LDO16 @ 150mA
 - LDO17 @ 450mA
 - LDO18 @ 150mA
 - LDO19 (SAFEOUT1) 4.9V
 - LDO20 (SAFEOUT2) 4.9V
 - LDO21 (Low Voltage LDO) @ 300mA
- RTC with two alarms
- Two Buffered 32.768kHz Output

- One Back up battery charger
- Low-Battery Monitor and Reset Output
- Fuel Gauge is fully integrated
- Haptic Motor Driver
- MUIC
- Level Translators
- 12 GPIOs
- Flash LED Driver
- I2C Interface for Programming
- 169-pins 13x13 Bumps WLP Package (0.4pitch)

1.1 Ordering Information

PART	DIE-ID	PACKAGE CODE	TEMP RANGE	PIN-PACKAGE
MAX8966EWW+	PR77Z-5Z	W1695A5	-40°C to 85°C	13x13 WLP 0.4 Pitch
MAX8997EWW+	PR77Z-6Z			

Note1. PR77Z-6Z and PR77Z-5Z are for centered trimmed samples.

2 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	FLED 2	FLED 1	OUTF	LXF	PGN DF	PGN D6	LX6	INB 06A	GND M	IN MOTOR	INB 02	NC
B	FGND	FGND	D GND2	OUTF	LXF	PGND F	PGN D6	LX6	INB 06B	MDN	MDP	BUCK 2	LX2
C	XIN	XOUT	32kHz AP	32kHz CP	FLED EN	GSMB	REF INPA	BUCK 6EN	BUCK 6	M PWM	M GAIN	PGN D2	PGN D3
D	VL	SAFE OUT1	SAFE OUT2	VCC 32CP	COMP	RSOI	IRQ1\	MR2\	MR1\	IN GPIO2	IN GPIO1	BUCK 3	LX3
E	BATT	BATT	DET BAT	V COIN	PWR ON	JIG ON	SCL	GPIO 7	GPIO 6	GPIO 1	GPIO 0	INB 03	INB 07
F	DCIN	DCIN	VICH G	18 VLL	PWR HOLD	ONO	SDA	GPIO 9	GPIO 8	GPIO 3	GPIO 2	BUCK 7	LX7
G	DN1	BC	18T NC2	28T1	18R NC1	CB	SET3	GPIO 11	GPIO 10	GPIO 5	GPIO 4	PGN D 7	PGN D 7
H	DP2	SL1	UT1	28T NO2	28T COM1	28R NO1	SET2	SET1	PWR EN	GPIO GND	D GND1	A GND	GND
J	COM N1	SR2	UR2	18R1	VBAT TFG	THRM	AIN	VTT	LDO 13	LDO 12	LDO 11	LDO 17	LDO 9
K	COM P2	MIC USB	18T2	28R COM2	ALRT	VBFG	SCA FG	LDO 21	INL 21	LDO 18	LDO 14	LDO 16	LDO 15
L	UID	IDB	BOOT	28R2	SDA FG	KVSS	SNS	LDO 2	LDO 10	INL 4	INL 3	INL 2	INL 1
M	PGN D 5	BUCK 5	INB 05	BUCK 4	BUCK 1	PGN D 1	LX1	INB 01	LDO 5	INL 6	LDO 3	LDO 8	LDO 1
N	NC	LX5	INB 04	LX4	PGN D 4	PGN D 1	LX1	INB 01	LDO 7	INL 5	LDO 6	LDO 4	NC

TOP VIEW
Figure 1 Pin Map

3 Typical Operation Circuit

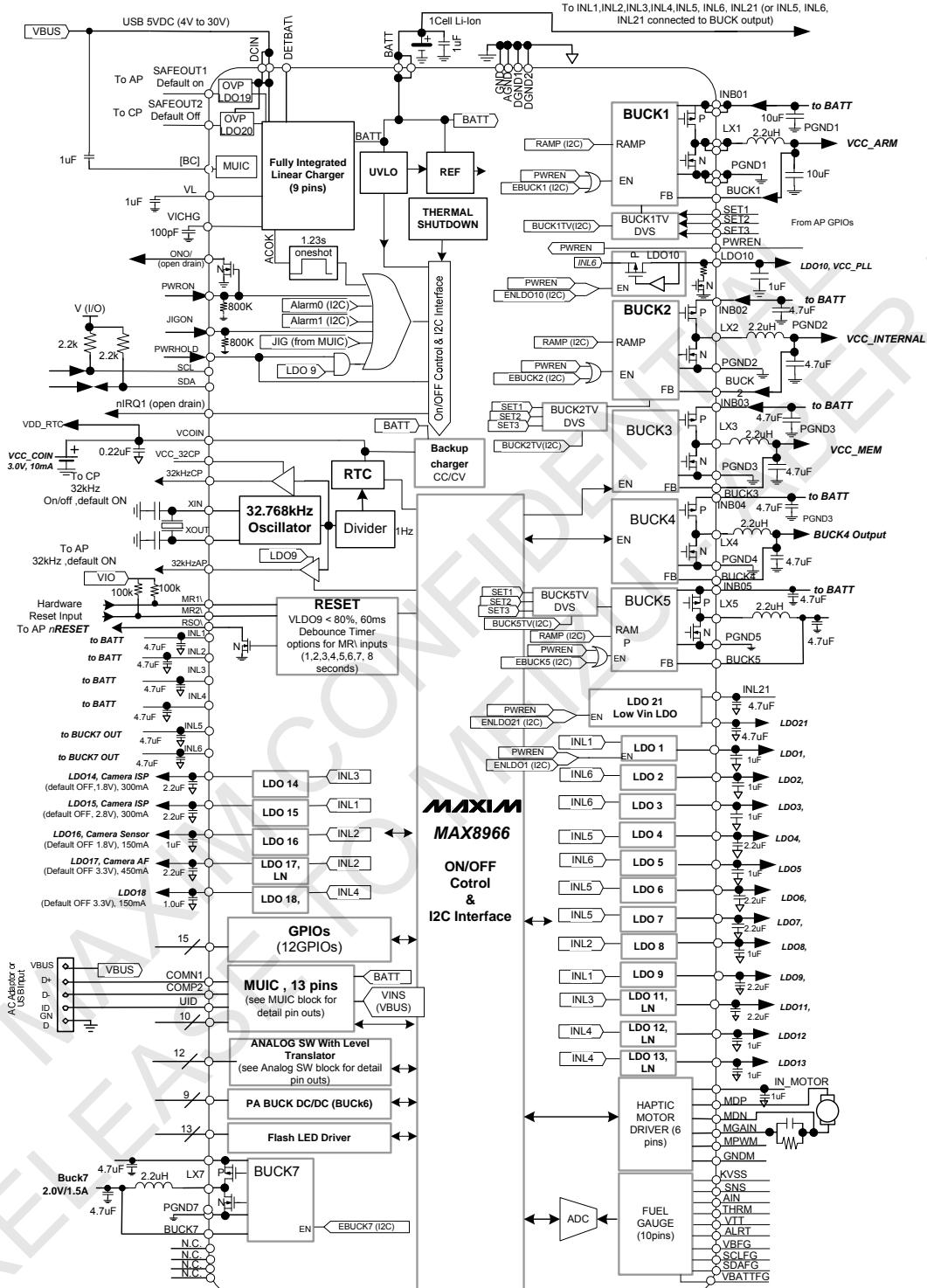


Figure 2 MAX8966 Typical Operation Circuit for C100/C110

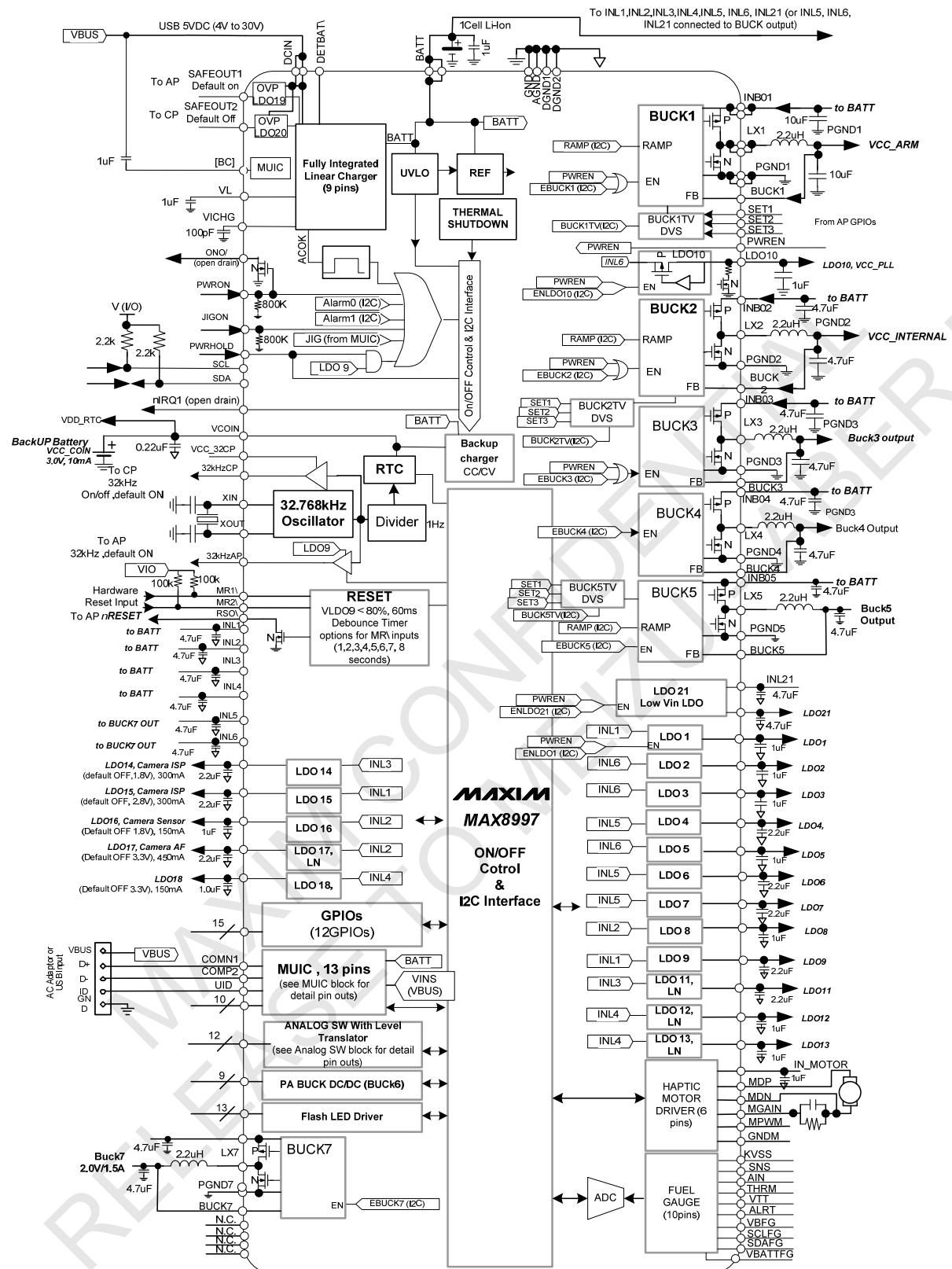


Figure 3 MAX8966 Typical Operation Circuit for C210

4 ABSOLUTE MAXIMUM RATINGS

4.1 PMIC

Vcc_32CP, BATT, INB01, INB02, INB03, INB04, INB05, INB07, INL1, INL2, INL3, INL4, INL5, INL6, INL21 JIGON, DETBAT/, SAFEOUT1 and SAFEOUT2 to AGND	-0.3V to +6.0V
VCOIN,	-0.3V to +4.0V
DCIN to GND.....	-0.3V to +30V
BUCK1 to PGND1	-0.3V to ($V_{INB01}+0.3V$)
BUCK2 to PGND2	-0.3V to ($V_{INB02}+0.3V$)
BUCK3 to PGND3	-0.3V to ($V_{INB03}+0.3V$)
BUCK4 to PGND4	-0.3V to ($V_{INB04}+0.3V$)
BUCK5 to PGND5	-0.3V to ($V_{INB05}+0.3V$)
BUCK7 to PGND7	-0.3V to ($V_{INB07}+0.3V$)
LX1 to PGND1.....	-0.3V to ($V_{INB01}+0.3V$)
LX2 to PGND2.....	-0.3V to ($V_{INB02}+0.3V$)
LX3 to PGND3.....	-0.3V to ($V_{INB03}+0.3V$)
LX4 to PGND4.....	-0.3V to ($V_{INB04}+0.3V$)
LX5 to PGND5.....	-0.3V to ($V_{INB05}+0.3V$)
LX7 to PGND7.....	-0.3V to ($V_{INB07}+0.3V$)
LX1 Continuous RMS Current (Note1).....	2.5A
LX2 Continuous RMS Current (Note1).....	2A
LX3 Continuous RMS Current (Note1).....	1.8A
LX4 Continuous RMS Current (Note1).....	0.6A
LX5 Continuous RMS Current (Note1).....	0.6A
LX7 Continuous RMS Current (Note1).....	1.5A
INL1, INL2, INL3, INL4 to BATT.....	-0.3V to +0.3V
LDO9, LDO15, LDO1 to AGND.....	-0.3V to ($V_{INL1}+0.3V$)
LDO8, LDO16, LDO17 to AGND.....	-0.3V to ($V_{INL2}+0.3V$)
LDO14, LDO11 to AGND	-0.3V to ($V_{INL3}+0.3V$)
LDO12, LDO13, LDO18 to AGND	-0.3V to ($V_{INL4}+0.3V$)
LDO7, LDO4, LDO6 to AGND	-0.3V to ($V_{INL5}+0.3V$)
LDO2, LDO3, LDO5, LDO10 to AGND	-0.3V to ($V_{INL6}+0.3V$)
LDO21 to AGND.....	-0.3V to ($V_{INL21}+0.3V$)
XIN, XOUT to AGND	-0.3V to ($V_{COIN}+0.3V$)
32kCP, to AGND	-0.3V to ($V_{CC_32CP}+0.3V$)
32kAP, to AGND	-0.3V to ($V_{LDO9}+0.3V$)
IRQ1\, PWREN, RSO\, MR1\, MR2\, SET1, SET2, SET3,\ PWRON, ONO\, PWRHOLD, SCL, SDA to AGND	-0.3V to ($V_{BATT}+0.3V$)
PGND_ to AGND	-0.3V to +0.3 V

4.2 Main Charger for Main Battery

DCIN to GND	-0.3V to +30V
SAFEOUT1, SAFEOUT2 DETBAT/, to GND	-0.3V to +6V
VL, VICHG to GND	-0.3V to +4.0V
PGND to AGND	-0.3V to +0.3V
BATT Continuous Current.....	1300mA
SAFEOUT1,SAFEOUT2 Continuous Current	+100mA

4.3 PA DC/DC BUCK CONVERTER

INB06A, INB06B, BUCK6EN to PGND6	-0.3 V to +6.0V
LX6 (1,2)	1.5ARMS
PGND6(1,2) to all other grounds	-0.3V to +0.3V
BUCK6 to PGND6	-0.3V to the lower of ($INB06+0.3V$) and +6.0V
REFINPA to AGND	-0.3V to +6.0V

4.4 LEVEL TRANSLATOR

18VLL, CB	-0.3V to +6V
18T2, 18R1, 18RNC1, 18TNC2	-0.3V to + (18VLL +0.3V)
28T1, 28R2, 28TCOM1, 28RNO1, 28RCOM2, 28TNO2	-0.3V to (LDO9 + 0.3V)

4.5 HAPTIC MOTOR DRIVER

IN_MOTOR to GNDM.....	-0.3V to +6V
MGAIN to GNDM.....	-0.3V to IN_MOTOR+0.3V
MPWM to GNDM(global ground).....	.-0.3V to min of (VBAT + 0.3V) and +6V
All other pins to GNDM.....	-0.3V to min of (IN_MOTOR + 0.3V) and +6V
Maximum Current into any Pin except IN_MOTOR, GNDM, MDP, and MDN.....	

4.6 MUIC

(All voltages referenced to GND)

BATT,	-0.3V to +6.0V
BOOT,	-0.3V to (LDO9 + 0.3V)
DCIN (Charger Mode)	-0.3V to +30V
DCIN (Microphone mode)	-0.3V to (V _{SWPOS} + 0.3V)
BC to GND.....	-0.5V to +0.5V

Switch enabled or CPEn=1

IDB, SL1, SR2, COMN1, COMP2, UID, MIC_USB,, DN1, DP2	(-2.1V) to (V _{SWPOS} + 0.3V)
UT1, UR2	-0.3 to (V _{SWPOS} + 0.3V)

Switch disabled and CPEn=0

IDB, SL1, SR2, COMN1, COMP2, UID, MIC_USB,, DN1, DP2, UT1, and UR2	-0.3V to (V _{VCCINT} + 0.3V)
Continuous Current into BC	±200mA
Continuous Current into COM_	±200mA
Continuous Current into all other pins	±100mA
Note 1; V _{SWPOS} = min((V _{VCCINT} , +3.3V)	
Note 2; V _{VCCINT} = max(V _{BAT} , min (V _{PVB} , 3.6V))	

4.7 FUEL GAUGE

VBATTFG, ALRT, SCLFG, SDAFG to AGND (global ground)	0.3V to +6V
VB to AGND (global ground)_	-0.3V to 2.2V
VTT to AGND (global ground)	-0.3V to +6V
AIN, THR to AGND(global ground)	-0.3V to VTT+0.3V
KVSS, SNS to AGND (global ground).....	-2V to +2V
Continuous Sink current, VTT, SCLFG, SDAFG, ALERT	20mA

4.8 GPIOs

IN_GPIO1, IN_GPIO2,	-0.3V to + 6V
GPIO0-5 to GND	-0.3V to IN_GPIO1+0.3V
GPIO6-11 to GND	-0.3V to IN_GPIO2+0.3V
VIN_GPIO1, VIN_GPIO2, GPIO0-11	2kV HBM ESD

4.1 Flash LED Drivers

BATT, OUTF to AGND	-0.3V to +6.0V
BATT, OUTF to AGND (Maximum of 1us)	-0.3V to +7.0V
COMP, FLED_EN, GSMB to AGND	-0.3V to BATT+0.3V
FLED1, FLED2_to FGND.....	-0.3V to OUTF+0.3V

PGND, FGND to AGND -0.3V to +0.3V
 I_{LXF} Current (rms) 3A

Continuous Power Dissipation ($T_A=+70^\circ\text{C}$) (Derate 29.4mW/ $^\circ\text{C}$ with 4L board, above 70°C) []W
 Operating Temperature Range -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
 Junction Temperature +150 $^\circ\text{C}$
 Storage Temperature Range -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
 Soldering Temperature (reflow) +260 $^\circ\text{C}$

Module Level ESD Protection (DCIN, IN1, IN2, IN3, IN4, IN5, IN6, BATT, JIGON, ; In-Circuit tested with 0.1 μF ceramic capacitor to meet 8kV).

ESD Protection for MR1\, MR2\ and PWRON is 10kV human body at modul level test with $C_{BP}=0.1\mu\text{F}$

Note 1: LX_ has internal clamp diodes to PGND_ and IN_. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

5 Electrical Characteristics

General and Logic

Operating conditions (unless otherwise specified), $V_{BATT} = V_{INBX} = V_{INX} = +3.7\text{V}$, DCIN are disconnected, $C_{BATT+\Sigma IN_} = 43.3\mu\text{F}$, $C_{REFBP} = 100\text{nF}$, $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown Supply Current 1	Backup Battery is fully charged. RTC on. All other circuits off (MUIC; LowPWR=1, AccDET=0, ADCEN=0).		20		μA
Shutdown Supply Current 2	Backup Battery is fully charged. RTC, Fuel Gauge, MUIC (LowPWR=0, CPEN=1, , VDCIN=0) are ON, All other circuits off.		105	185	μA
No Load Supply Current	MAX8966 MAX8966 Buck1, Buck2, Buck3, Buck7, LDO2, LDO3, LDO6, LDO8, LDO9, LDO10, LDO15, Battery Monitor, and Backup charger on, Fuel Gauge, MUIC are ON. The other circuits off. $V_{BATT} = V_{INBX} = V_{INX} = 4.2\text{V}$		350	700	μA
	MAX8997 MAX8997 Buck1, Buck2, Buck3, Buck5, Buck7, LDO1,LDO2,LDO3, LDO4, LDO5, LDO6, LDO7, LDO8, LDO9,LDO10, LDO21, Battery Monitor, and Backup charger, Fuel Gauge, MUIC are ON. The other circuits off. $V_{BATT} = V_{INBX} = V_{INX}$ =4.2V		450	800	μA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Light Load Supply Current (Note1)	BUCK1 to Buck5, Buck7 with 500uA load & LDO2 to LDO17, and Backup charger on, Battery Monitor on. $V_{BATT} = V_{INBX} = V_{INX} = 4.2V$		1		mA
Undervoltage Lockout (UVLO)					
Undervoltage Lockout Threshold	VBATT rising	-2%	2.7	+2%	V
Undervoltage Lockout Falling Threshold	VBATT falling..		2.3		
THERMAL SHUTDOWN (LDOs, Bucks)					
Threshold			160		°C
Hysteresis			20		°C
LOGIC AND CONTROL INPUTS					
Input Low Level	PWRHOLD, SCL, SDA, MR1\, MR2\, PWRON, JIGON, SET1, SET2, SET3, PWREN, Ta=25°C			0.4	V
Input High Level	PWRHOLD, SCL, SDA, MR1\, MR2\, PWRON, JIGON, SET1, SET2, SET3, PWREN, Ta=25°C	1.4			V
Input Hysteresis	PWRHOLD, SCL, SDA, MR1\, MR2\, PWRON, JIGON, SET1, SET2, SET3, PWREN, Ta=25°C		0.1		V
Logic Input Current PWRHOLD, SCL, SDA, , SET1, SET2, SET3, PWREN, MR1/, MR2/	T _A = 25°C 0V < Vin < MBATT	-1		1	µA
		T _A = 85°C		0.1	uA
SCL, SDA, Input capacitance				10	pF
SDA, Output Low Voltage	2.6V <= Vin <= 5.5V, Sinking 3mA			0.2	V
ONO\, RSO\, IRQ1\, Output Low Voltage	Isink = 1mA			0.4	V
ONO\, RSO\, IRQ1\, \ Output High Leakage	V _{BATT} = 5.5V	T _A = 25°C	-1	0	1
		T _A = 85°C		0.1	uA
PWRON Pull-down resistor to GND		400	800	1600	kΩ
JIGON Pull-down resistor to GND		400	800	1600	kΩ
Interrupt Debounce filter timer	LOWBAT1, LOWBAT2,		16		ms
	JIGR, JIGONR ,PWRONR, PWRONF, JIGF, JIGONF, ACOK,		16		
SMPL (Sudden Momemtary Power Loss) Timer	Set SMPL bit=1		0.5		s
WTSR (Watchdog Timeout and Software Resets) Timer	nRESET Low holding time.		58.6		ms
ONKEY1S Timer	If PWRON stays longer than 1s, IRQ\ will trigger		1		s

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RSO\ De-assert Delay			60		msec
Manual Reset Debounce Timer	The period between MR1\=MR2\=Low and Automatic reboot start	1			sec
		2			
		3			
		4			
		5			
		6			
		7 (Default)			
		8			
I²C (Note1)					
Clock Frequency		100		400	kHz
Bus-Free Time Between START and STOP		1.3			μs
Hold Time Repeated START Condition		0.6			μs
CLK Low Period		1.3			μs
CLK High Period		0.6			μs
Set-Up Time Repeated START Condition		0.6			μs
DATA Hold Time		0			μs
DATA Set-Up time		100			ns
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both DATA & CLK Signals			50		ns
Set-Up Time for STOP Condition		0.6			μs

Note1. Design guidance only, not tested during final test.

Note2. Design guidance only, not tested during final test except 200mV @ Default value for LOBAT1 & LOBAT2.

Buck 1-5,7 Converters

Electrical Characteristics: Buck 1 to Buck 5 and Buck7

V_{INBx}=3.7V, V_{BOUTx}=Default, C_{out}=4.7uF, L=1.5uH, T_A=-40°C to +85°C, unless otherwise specified, typical values are at TA=+25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT S
Step-Down Regulator						
Input Voltage Range	V _{INBx}	Guaranteed by Output Voltage Accuracy and Supply Current	2.7		5.5	V
Shutdown Current	I _{INx_SD}	Regulator Disabled, V _{INx} =4.8V, Note1		0.1		µA
Ground Current	I _{INx_Q}	Regulator Enabled, No load, no switching, Note1		25		µA
Output Voltage Range	V _{BOUTx}	BUCK1, Programmable in 25mV Steps	0.650		2.225	V
		BUCK2, Programmable in 25mV Steps	0.650		2.225	
		BUCK3, Programmable in 50mV Steps	0.75		3.90	
		BUCK4, Programmable in 25mV Steps	0.650		2.225	
		BUCK5, Programmable in 25mV Steps	0.650		2.225	
		BUCK7, Programmable in 50mV Steps	0.75		3.90	
Default Output Voltage	V _{BOUT_x_DFLT}	BUCK1		1.25		V
		BUCK2		1.1		
		BUCK3	MAX8966		1.8	
			MAX8997		1.1	
		BUCK4		1.2		
		BUCK5	Max8966		1.1	
			MAX8997		1.2	
		BUCK7 Default value		2.0		
Output Voltage Accuracy		I _{load} =100mA Min, Default, Max Output voltage	-3		+3	%

Maximum Output Current	I _{OUTBx}	BUCK1	2500			mA	
		BUCK2	1200				
		BUCK3	Max8997	1800			
			Max8966	1500			
		BUCK4	600				
		BUCK5	600				
		BUCK7	1500				
Output Load Regulation (Voltage Positioning)	Buck1	Equal to inductor DC resistance divided by four		R _L /8		V/A	
	Buck2,3,4, 5,7			R _L /4			
Output Line Regulation		INL1 to INL6, INB01 to INB07= 2.7V to 5.5V		0.3		%	
Current Limit	I _{LIMBx}	BUCK1,	PFET Switch	2700	3600	4500	mA
			NFET Rectifier	2300	3200	4100	
		Buck2	PFET Switch	1400	1850	2300	
			NFET Rectifier	1000	1450	1900	
		BUCK3,	PFET Switch (Max8997)	2000	2700	3400	
			NFET Rectifier(Max8997)	1600	2300	3000	
			PFET Switch (Max8966)	1700	2300	2900	
		Buck4, Buck5	NFET Rectifier(Max8966)	1300	1900	2500	
			PFET Switch	1000	1350	1700	
			NFET Rectifier	800	1150	1500	
On-Resistance		BUCK4, BUCK5	PFET Switch	1700	2300	2900	Ω
			NFET Rectifier	1300	1900	2500	
		Buck1, Buck2, Buck3, Buck7	PFET Switch, I _{LX} = -150mA		0.2		
			NFET Rectifier, I _{LX} = 150mA		0.1		
N-Channel Zero-Crossing Threshold		LXx = PGNDx or INBx	PFET Switch, I _{LX} = -150mA		0.15		Ω
			NFET Rectifier, I _{LX} = 150mA		0.08		
LX Leakage Current					50		mA
LX Active Discharge		Regulator Disabled, Resistance from LX _{Bx} to PGND _x			0.1	1	μ A
					1		

Startup Time			40		μs
Dynamic-Change Ramp Rate	BUCK1, BUCK2, BUCK4, BUCK5		1.00		$\text{mV}/\mu\text{s}$
			2.00		
			3.03		
			4.00		
			5.00		
			5.88		
			7.14		
			8.33		
			9.09		
			10.00		
			11.11		
			12.50		
			16.67		
			25.00		
			50.00		
			100.00		
DVSOK Timer Accuracy		DVS Target Voltage Change (Design Guide Only)	15		%
Minimum On Time	t_{ONBx}		60		ns
Minimum Off Time	t_{OFFBx}		60		ns

Note1. Design Guidance only. Not tested during final test.

Note 2. Limits are 100% production tested at $T_A=+25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.Note 3. $\pm 3\%$ limit will be valid for Vout(min), Vout(default), Vout(max) programming output values. Note 4: Design guidance only. (Cannot achieve ramp rate with existing inductor and capacitor values)**Buck6 PA DC/DC BUCK CONVERTER**

(INB06 = BATT=3.6V, REFIN = 0.6V

 $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Input Voltage	IN	2.7	5.5		V
No Load Supply Current	$I_{OUT}=0\text{A}$, NO SWITCHING (Design Guidance only)	20	40		μA
	$I_{OUT}=0\text{A}$, SWITCHING (PFM mode), (Design Guidance only)	25			
	Total Dropout supply current (Design Guidance only)	77	112		
	DC-DC step down converter dropout only (Design Guidance only)	27	42		
	Linear bypass regulator dropout only (Design Guidance only)	50	75		
	$I_{OUT}=0\text{A}$, SWITCHING (PWM mode) (Design Guidance only)	2			
Shutdown Supply Current(Design Guidance Only)	EN = AGND	$T_A=+25^\circ\text{C}$	0.7	1.5	μA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	T _A =+85°C	1			
THERMAL PROTECTION					
Thermal Shutdown	T _A rising, 20°C typical hysteresis	+160			°C
LOGIC CONTROL					
Logic Input High Voltage	2.7V ≤ V _{IN} ≤ 5.5V	1.4	IN		V
Logic Input Low Voltage	2.7V ≤ V _{IN} ≤ 5.5V		0.4		V
EN Pull Down Resistor		400	800	1600	kΩ
EN Capacitive Loading(Design Guide Only)				20	pF
Power up timing					
BUCK soft start time	t _{BUCK_SS} , C _{OUT} =2.2μF, L=3.3uH, I _{OUT} =0A Enable to OUT	20			μsec
Output transition time	OUT transition from 0.51V to 3.4V, INB06=BATT=4.2V R _{LOAD} = 5Ω, C _{OUT} = 2.2μF	10			μsec
	OUT transition from 3.4V to 0.51V , INB06=BATT=4.2V R _{LOAD} = 5Ω, C _{OUT} = 2.2μF	10			μsec
REFINPA					
REFINPA Common Mode Range		0.17	1.7		V
REFINPA to OUT Gain	REFINPA = 1.2V(Note 2) I _{LX} = 0A, (FPWM Mode)	-2.5% 3.0	2.5 +2.5%		V/V
REFINPA to OUT Gain	REFINPA = 0.3V I _{LX} = 0A, (FPWM Mode)	-7.5% 3.0	2.5 +7.5%		V/V
Input Resistance	Design guidance only	800			kΩ
REFINPA Capacitive Loading	Design guidance only		35		pF
I _{REFIN} Control Current	Design guidance only	-300	2	30	uA
REFINPA time constant	Design guidance only		0.1		μsec
V _{OUT} BYPASS Regulation					
On-Resistance	P-Channel MOSFET Bypass, I _{OUT} = 100mA	T _A = +25°C	50		mΩ
Bypass Current Limit	V _{OUT} = 1.5V	1200	1900	3000	mA

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Down Current Limit in Bypass			1300	1600	1800	mA
Total Current Limit in Bypass	$V_{OUT} = V_{LX} = 0V$		2500	3500	4800	mA
Bypass Off Leakage Current	$V_{IN} = 5.5V$, $V_{OUT} = 0V$	$T_A = +25^\circ C$		0.01	5	μA
		$T_A = +85^\circ C$		1		
Linear Bypass Regulation Threshold	Below nominal BUCK output voltage (REFINPAx3.0), $I_{out}=0mA$ I2C option for following: 0: 120mV 1: 60mV			60		mV
Linear Bypass LDO Enable Threshold in relation to REFINPA	REFINPA depended 2.5x 3x 00 OFF OFF 01 480 400 10 520 433 11 560 466			466		mV
Linear Bypass LDO Enable Threshold hysteresis				20		mV
LDO Current feedback gain(Ratio of LDO Current to offset voltage applied to REFIN voltage at Buck error comparator).	ILDO>50mA			0.125		V/A
Output Capacitor for Stable Operation	$0 < I_{VOUT} < 1200mA$ (Design Guidance Only)		2.2	4.7		μF
DC/DC Converter						
Load regulation(excludes LDO)	$I_{OUT} = 0mA$ to 650mA,			Ilx*(Rl /4)		mV
Line regulation(excludes LDO)	$V_{IN} = 2.7V$ to 4.2V			2000		ppm/V
Output voltage ripple	PFM (max Cap ESR = 10mOhms, L = 3.3uH)			15		mV_{PP}
	PWM (max Cap ESR = 10mOhms, L = 3.3uH)			5		mV_{PP}
Harmonics in V_{OUT} at min load (Design Guidance Only)	For $f > 4MHz$, $V_{OUT} = 1.0V$, $I_{OUT} = 30mA$			-43		dBm
Harmonics in V_{OUT} at max load (Design Guidance Only)	For $f > 4MHz$, $V_{OUT} = 3.4V$, $I_{OUT} = 650mA$			-47		dBm
Noise (Design Guidance Only)	40 MHz to 250 MHz			5		μ/\sqrt{Hz}
FET Scaling Transition threshold	OUT rising	Range 1 to 2		1.4		V
		Range 2 to 3		2.0		

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transition Threshold Hysteresis			50		mV
LX On-Resistance	P-channel MOSFET, Range 1, $I_{LX} = 100\text{mA}$		0.45	[]	Ω
	P-channel MOSFET, Range 2, $I_{LX} = 100\text{mA}$		0.225	[]	
	P-channel MOSFET, Range 3, $I_{LX} = 100\text{mA}$		0.15	[]	
	N-channel MOSFET, Range 1, $I_{LX} = -100\text{mA}$		0.30	[]	
	N-channel MOSFET, Range 2, $I_{LX} = -100\text{mA}$		0.15	[]	
	N-channel MOSFET, Range 3, $I_{LX} = -100\text{mA}$		0.10	0.30	
Efficiency Design Guidance Only	$V_{OUT} = 0.5\text{V}$, $I_{OUT} = 50\text{mA}$		80		%
	$1.5 < V_{OUT} < 1.8\text{V}$, $100\text{mA} < I_{OUT} < 150\text{mA}$		85		
	$3.1\text{V} < V_{OUT} < 3.4\text{V}$, $500\text{mA} < I_{OUT} < 650\text{mA}$		90		
LX Leakage Current	$EN=0\text{V}$, $V_{LX} = 0\text{V}$	$T_A = +25^\circ\text{C}$		0.1	5
		$T_A = +85^\circ\text{C}$		1	
LX Active Discharge	Regulator Disabled, Resistance from LX6 to PGND6		1		$\text{k}\Omega$
Load Current Range	Design Guidance Only	0		1200	mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
P-Channel MOSFET Peak Current Limit		1.3	1.6	1.8	A
N-Channel MOSFET Valley Current Limit		1.1	1.4	1.6	A
N-Channel MOSFET Negative Current Limit			1.6		A
Automatic Skip Mode enable threshold	I2C option for following: 00 Force PWM at all levels of OUT 01 Force PWM > 750mV 10 Force PWM > 1000mV 11 Force PWM > 1250mV		1.25		V
Automatic skip mode enable threshold hysteresis			50		mV
Zero crossing threshold			50		mA
Switching frequency	INBO6=BATT=3.7V, REFIN=0.6V, Gain=3x		3		MHz
Duty cycle (Design Guidance Only)	Skip mode	0			%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Dropout mode			100	
Minimum On- and Off-Times				75	nsec

Note 1: All devices are 100% production tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

Note 2: For $\text{REFINPA}=1.2\text{V}$, $\text{INB06}=\text{BATT}$ should greater than 4.6V in order to avoid the dropout operation.

5.1 LDO

5.1.1 LDO1 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{\text{BATT}} = V_{\text{IN}1}$ to $V_{\text{IN}6} = +3.7\text{V}$, $C_{\text{BATT}+\Sigma\text{IN}_-} = 43.3\mu\text{F}$, $C_{\text{REFBP}} = 100\text{nF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{\text{IN}} = +5.5\text{V}$	-3%	3.3	+3%	V
		150mA@ $V_{\text{IN}}=3.6\text{V}$				
Default output voltage(MAX8966)		1mA@ $V_{\text{IN}} = +5.5\text{V}$	-3%	3.3	+3%	V
		150mA@ $V_{\text{IN}}=3.6\text{V}$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{\text{IN}}=3.4\text{V}$ & $I_{\text{OUT}}=\text{Imax}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{\text{IN}}=5.5\text{V}$ & $I_{\text{OUT}}=1\text{mA}$				
		Green Mode ; $V_{\text{IN}}=3.4\text{V}$ & $I_{\text{OUT}}=\text{Imax}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{\text{IN}}=5.5\text{V}$ & $I_{\text{OUT}}=1\text{mA}$				
Output current		Normal Mode (Imax)			150	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0\text{A} < I_{\text{LDO}} < \text{Imax}$ MAX ESR < $150\text{m}\Omega$	0.7	1.0		μF
Ground current (Note1)		$I_{\text{LDO}}=500\mu\text{A}$		23	46	μA
		Green Mode		1.5	[3]	
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{\text{out}}=1\text{mA}$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1\text{mA} < I_{\text{LDO}} < 150\text{mA}$		0.05		%
		Green Mode, $1\text{mA} < I_{\text{LDO}} < 5\text{mA}$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2\text{V} < V_{\text{IN}} < 5.5\text{V}$, $I_{\text{LDO}}=100\text{mA}$		0.01		%
		Green Mode, $3.2\text{V} < V_{\text{IN}} < 5.5\text{V}$, $I_{\text{LDO}}=1\text{mA}$		0.05		%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Drop-out voltage		Normal Mode, $I_{LDO}=I_{max}$, $Vin=3.7V$, $T_A=25^\circ C$		60	[120]	mV
		Normal Mode, $I_{LDO}=I_{max}$, $Vin=1.7V$		150	[450]	mV
		Green Mode, $I_{LDO}=I_{max}$, $Vin=3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{IN}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject $\sum LDO/\sum V_{IN}$	$f=10Hz-10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO}=10\%$ of I_{max} . $Vin=V_{nom}+1V$	$f=1kHz$		79		dB
		$f=10kHz$		68		dB
		$f=100kHz$		50		dB
		$f=1MHz$		50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO} = 1\mu F$, $I_{LDO}=10\%$ or I_{max} , $Vout=V_{max}$		80		μV_{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation		40	100	us
Start-up transient overshoot (Note1)		$C_{LDO} = 1\mu F$, $I_{LDO} = 150mA$		3	50	mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		$^\circ C$
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

Note 4. Does not include ESR of the capacitance or trace resistance of the module/PCB

Note2. Design guidance only, not tested during final test.

Note 5 The Green mode does not have a current limit.

5.1.2 LDO2 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.1	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.2	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			150	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7	1.0		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$		23	46	
		Green Mode		1.5	[3]	μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)		60	120	usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^\circ C$		60	[120]	mV
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$		150	[450]	mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{max}$, $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{max}$, $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject		$f = 10Hz - 10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\% \text{ of }$	$f = 1kHz$		79	dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		I _{max} , Vin=V _{nom} +1V f=10kHz f=100kHz f=1MHz	68 50 50			dB
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or I _{max} , V _{out} =V _{max}	80			μV _{RMS}
Start-Up Ramp Rate		After Enabling	100			mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 1μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising	165			°C
		T _j Falling	150			

Note1. Design guidance only, not tested during final test.

5.1.3 LDO3 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT} = V_{IN1} to V_{IN6} = +3.7V, C_{BATT+ΣIN_} = 43.3μF, C_{REFBP} = 100nF, T_A = -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ V _{IN} = +5.5V				
		150mA@ V _{IN} =3.6V	-3%	1.1	+3%	V
Default output voltage(MAX8966)		1mA@ V _{IN} = +5.5V				
		150mA@ V _{IN} =3.6V	-3%	1.2	+3%	V
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; VIN=3.4V & IOUT=I _{max} (or 200mA)				
		Normal Mode ; VIN=5.5V & IOUT=1mA	-3		+3	%
		Green Mode ; VIN=3.4V & IOUT=I _{max} (or 200mA)				
		Green Mode ; VIN=5.5V & IOUT=1mA	-3		+3	%
Output current		Normal Mode (I _{max})			150	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		0A < I _{LDO} < I _{max} MAX ESR < 150mΩ	0.7	1.0		μF
Ground current (Note1)		I _{LDO} =500μA	23	46		
		Green Mode	1.5	[3]		μA
		LDO disabled	1			
Green Mode Transition time		GREEN MODE to Normal Mode, I _{out} =1mA(Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, 1mA < I _{LDO} < 150mA			0.05	%
		Green Mode, 1mA < I _{LDO} < 5mA			0.05	%
Line regulation (Note 1)		Normal Mode, 3.2V < V _{IN} < 5.5V I _{LDO} =100mA			0.01	%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Green Mode, $V_{IN} \geq 5.5V$, $I_{LDO}=1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO}=I_{max}$, $Vin=3.7V$, $T_A=25^\circ C$		60	[120]	mV
		Normal Mode, $I_{LDO}=I_{max}$, $Vin=1.7V$		150	[450]	mV
		Green Mode, $I_{LDO}=I_{max}$, $Vin=3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{IN}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject $\Sigma LDO/\Sigma V_{IN}$		$f=10Hz-10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO}=10\%$ of I_{max} . $Vin=V_{nom}+1V$	$f=1kHz$	79		dB
			$f=10kHz$	68		dB
			$f=100kHz$	50		dB
			$f=1MHz$	50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO}=1\mu F$, $I_{LDO}=10\%$ or I_{max} , $Vout=V_{max}$		80		μV_{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation		40	100	us
Start-up transient overshoot (Note1)		$C_{LDO} = 1\mu F$, $I_{LDO} = 150mA$		3	50	mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		Tj Rising		165		$^\circ C$
		Tj Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.4 LDO4 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			300	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	1.54	2.2		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$ No load	23	46		
		Green Mode, No load	1.5	[3]		μA
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 300mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[300]	510	[750]	mA
Output Load Transient		NError! Reference source not found.ormal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		f=10Hz-10kHz, C _{LDO} = 1μF, I _{LDO} =10% of Imax. Vin=Vnom+1V	f=1kHz	79		dB
			f=10kHz	68		dB
			f=100kHz	50		dB
			f=1MHz	50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or Imax, Vout=Vmax		80		μV _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 2.2μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		°C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.5 LDO5 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.2	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.2	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			150	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7	1.0		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$		23	46	
		Green Mode		1.5	[3]	μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		f=10Hz-10kHz, C _{LDO} = 1μF, I _{LDO} =10% of Imax. Vin=Vnom+1V	f=1kHz	79		dB
			f=10kHz	68		dB
			f=100kHz	50		dB
			f=1MHz	50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or Imax, Vout=Vmax		80		μV _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 1μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		°C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.6 LDO6 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			300	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	1.54	2.2		μF
Ground current (Note1),		$I_{LDO} = 500\mu A$ No load	23	46		
		Green Mode, No load	1.5	[3]		μA
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 300mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[300]	510	[750]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
		Green Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		f=10Hz-10kHz, C _{LDO} = 1μF, I _{LDO} =10% of Imax. Vin=Vnom+1V	f=1kHz	79		dB
		f=10kHz	68		dB	
		f=100kHz	50		dB	
		f=1MHz	50		dB	
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or Imax, Vout=Vmax		80		μV _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 2.2μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		°C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.7 LDO7 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			300	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	1.54		2.2	μF
Ground current (Note1),		$I_{LDO} = 500\mu A$ No load		23	46	
		Green Mode, No load		1.5	[3]	μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)		60	120	usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 300mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$		60	[120]	mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$		150	[450]	mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[300]	510	[750]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
		Green Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		f=10Hz-10kHz, C _{LDO} = 1μF, I _{LDO} =10% of Imax. Vin=Vnom+1V	f=1kHz	79		dB
		f=10kHz	68		dB	
		f=100kHz	50		dB	
		f=1MHz	50		dB	
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or Imax, Vout=Vmax		80		μV _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 2.2μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		°C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.8 LDO8 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	3.3	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	3.3	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			150	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7		1.0	μF
Ground current (Note1)		$I_{LDO} = 500\mu A$	23		46	μA
		Green Mode	1.5	[3]		μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60		120	usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$	0.05			%
		Green Mode, $1mA < I_{LDO} < 5mA$	0.05			%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$	0.01			%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$	0.05			%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^\circ C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject $\Sigma LDO/\Sigma V_{in}$		$f = 10Hz - 10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ of I_{max} . $V_{in} = V_{nom} + 1V$	$f = 1kHz$		79	dB
			$f = 10kHz$		68	dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		f=100kHz f=1MHz	50			dB
			50			dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ or I_{max} , $V_{out} = V_{max}$		80		μV_{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		$C_{LDO} = 1\mu F$, $I_{LDO} = 150mA$	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		$^{\circ}C$
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.9 LDO9 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			450	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	2.31	3.3		μF
Ground current (Note1),		$I_{LDO} = 500\mu A$ No load		24	48	
		Green Mode, No load		1.5	[3]	μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 450mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	450		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	300		mV
Output Current limit (Note3)		LDO output short to GND	[450]	765	[1125]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$	25	[50]		mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$	5	[10]		mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$	5	[10]		mV

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		$f=10\text{Hz}-10\text{kHz}$, $C_{LDO} = 1\mu\text{F}$, $I_{LDO}=10\%$ of Imax. $V_{in}=V_{nom}+1\text{V}$		$f=1\text{kHz}$	79		dB
				$f=10\text{kHz}$	68		dB
				$f=100\text{kHz}$	50		dB
				$f=1\text{MHz}$	50		dB
Output Noise Volt. (RMS)		$100\text{Hz}-100\text{kHz}$, $C_{LDO} = 1\mu\text{F}$, $I_{LDO}=10\%$ or Imax, $V_{out}=V_{max}$		80			μV_{RMS}
Start-Up Ramp Rate		After Enabling		100			mV/us
Soft Start Time (Note1)		From shut down to Output regulation		40	100		us
Start-up transient overshoot (Note1)		$C_{LDO} = 2.2\mu\text{F}$, $I_{LDO} = 150\text{mA}$		3	50		mV
Shutdown Output Resistance				[50]	160	[400]	Ω
Power Okay Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} Rising	92	97		%
			V_{OUT} Falling	74	77.5		
Thermal Shutdown		T_j Rising		165			$^{\circ}\text{C}$
		T_j Falling		150			

Note1. Design guidance only, not tested during final test.

5.1.10 LDO10 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.1	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.2	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})		150		mA
		Green Mode		5		mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7	1.0		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$		23	46	
		Green Mode		1.5	[3]	μA
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)		60	120	usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage ^m		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$		60	[120]	mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$		150	[450]	mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\% \text{ to } 100\%$ to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\% \text{ to } 100\%$ to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		f=10Hz-10kHz, C _{LDO} = 1μF, I _{LDO} =10% of Imax. Vin=Vnom+1V	f=1kHz	79		dB
			f=10kHz	68		dB
			f=100kHz	50		dB
			f=1MHz	50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or Imax, Vout=Vmax		80		μV _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 1μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		°C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.11 LDO11 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			300	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	1.54	2.2		μF
Ground current(Note1),		$I_{LDO} = 500\mu A$ No load	23	46		
		Green Mode, No load	1.5	[3]		μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 300mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[300]	510	[750]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
		Green Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		f=10Hz-10kHz, C _{LDO} = 1μF, I _{LDO} =10% of Imax. Vin=Vnom+1V	f=1kHz	79		dB
			f=10kHz	68		dB
			f=100kHz	50		dB
			f=1MHz	50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or Imax, Vout=Vmax		80		μV _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 2.2μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		°C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.12 LDO12 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.2	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.2	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})		150		mA
		Green Mode		5		mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7	1.0		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$		23	46	
		Green Mode		1.5	[3]	μA
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)		60	120	usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$		60	[120]	mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$		150	[450]	mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{max}$, $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{max}$, $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject $\sum LDO / \sum V_{IN}$		$f = 10Hz - 10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\% \text{ of } f = 1kHz$		79		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Imax. Vin=Vnom+1V f=10kHz	68			dB
		f=100kHz	50			dB
		f=1MHz	50			dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ or Imax, Vout=Vmax	80			μV_{RMS}
Start-Up Ramp Rate		After Enabling	100			mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		$C_{LDO} = 1\mu F$, $I_{LDO} = 150mA$	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising	165			$^{\circ}C$
		T _j Falling	150			

Note1. Design guidance only, not tested during final test.

5.1.13 LDO13 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			150	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7	1.0		μF
Ground current(Note1)		$I_{LDO} = 500\mu A$	23	46		
		Green Mode	1.5	[3]		μA
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$	0.05			%
		Green Mode, $1mA < I_{LDO} < 5mA$	0.05			%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$	0.01			%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$	0.05			%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^\circ C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$	66			mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$	25	[50]		mV
Output Line Transient		Normal Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$	5			mV
		Green Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$	5	[10]		mV
Power Supply Reject $\Sigma LDO/\Sigma V_{in}$		$f = 10Hz - 10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ of I_{max} . $V_{in} = V_{nom} + 1V$	$f = 1kHz$	79		dB
			$f = 10kHz$	68		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		f=100kHz	50			dB
		f=1MHz	50			dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ or I_{max} , $V_{out} = V_{max}$	80			μV_{RMS}
Start-Up Ramp Rate		After Enabling	100			mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100	us	
Start-up transient overshoot (Note1)		$C_{LDO} = 1\mu F$, $I_{LDO} = 150mA$	3	50	mV	
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising	165			$^{\circ}C$
		T _j Falling	150			

Note1. Design guidance only, not tested during final test.

5.1.14 LDO14 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	1.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			300	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	1.54	2.2		μF
Ground current (Note1),		$I_{LDO} = 500\mu A$ No load		23	46	
		Green Mode, No load		1.5	[3]	μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)		60	120	usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 300mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^\circ C$		60	[120]	mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$		150	[400]	mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[300]	510	[750]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
		Green Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject $\Sigma LDO / \Sigma V_{in}$		$f = 10Hz$ - $10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ of $f = 1kHz$		79		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		I _{max} , Vin=V _{nom} +1V	f=10kHz	68		dB
			f=100kHz	50		dB
			f=1MHz	50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1μF, I _{LDO} =10% or I _{max} , V _{out} =V _{max}		80		μV _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 2.2μF, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		°C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.15 LDO15 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	2.8	+3%	V
		300mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			300	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	1.54	2.2		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$ No load	23	46		
		Green Mode, No load	1.5	[3]		μA
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 300mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[300]	510	[750]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{max} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
		Green Mode, $V_{in} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Reject Σ LDO/ Σ V _{IN}		f=10Hz-10kHz, C _{LDO} = 1 μ F, I _{LDO} =10% of Imax. Vin=Vnom+1V	f=1kHz	79		dB
			f=10kHz	68		dB
			f=100kHz	50		dB
			f=1MHz	50		dB
Output Noise Volt. (RMS)		100Hz-100kHz, C _{LDO} = 1 μ F, I _{LDO} =10% or Imax, Vout=Vmax		80		μ V _{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		C _{LDO} = 2.2 μ F, I _{LDO} = 150mA	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		$^{\circ}$ C
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.16 LDO16 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	3.3	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	2.6	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})		150		mA
		Green Mode		5		mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7	1.0		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$		23	46	
		Green Mode		1.5	[3]	μA
		LDO disabled		1		
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)		60	120	usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$		60	[120]	mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$		150	[450]	mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$		150	[300]	mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{max}$, $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{max}$, $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5		mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject $\sum LDO / \sum V_{IN}$		$f = 10Hz - 10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\% \text{ of } f = 1kHz$		79		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Imax. Vin=Vnom+1V f=10kHz f=100kHz f=1MHz	68			dB
			50			dB
			50			dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ or Imax, Vout=Vmax		80		μV_{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		$C_{LDO} = 1\mu F$, $I_{LDO} = 150mA$	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		$^{\circ}C$
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.17 LDO17 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$ 300mA@ $V_{IN} = 3.6V$	-3%	3.3	+3%	V
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$ 300mA@ $V_{IN} = 3.6V$	-3%	3.3	+3%	V
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			450	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	2.31	3.3		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$ No load	24	48		μA
		Green Mode, No load	1.5	[3]		
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 450mA$		0.05		%
		Green Mode, $1mA < I_{LDO} < 5mA$		0.05		%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$		0.01		%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$		0.05		%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^\circ C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	450		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	300		mV
Output Current limit (Note3)		LDO output short to GND	[450]	765	[1125]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		66		mV
		Green Mode, $I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		25	[50]	mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
Power Supply Reject $\sum LDO / \sum V_{IN}$		$f = 10Hz - 10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\% \text{ of } f = 1kHz$		79		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Imax. Vin=Vnom+1V f=10kHz f=100kHz f=1MHz	68			dB
			50			dB
			50			dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ or Imax, Vout=Vmax		80		μV_{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		$C_{LDO} = 2.2\mu F$, $I_{LDO} = 150mA$	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		$^{\circ}C$
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.18 LDO18 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ¹		Guaranteed by Output Accuracy	1.7		5.5	V
Default output voltage(MAX8997)		1mA@ $V_{IN} = +5.5V$	-3%	3.3	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Default output voltage(MAX8966)		1mA@ $V_{IN} = +5.5V$	-3%	3.3	+3%	V
		150mA@ $V_{IN} = 3.6V$				
Output Voltage Range		Programmable in 50mV Steps	0.8		3.95	V
Output Voltage Accuracy		Normal Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Normal Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
		Green Mode ; $V_{IN} = 3.4V$ & $I_{OUT} = I_{max}$ (or 200mA)	-3	+3	%	%
		Green Mode ; $V_{IN} = 5.5V$ & $I_{OUT} = 1mA$				
Output current		Normal Mode (I_{max})			150	mA
		Green Mode			5	mA
Minimum Output Capacitor (Note1)		$0A < I_{LDO} < I_{max}$ MAX ESR < $150m\Omega$	0.7	1.0		μF
Ground current (Note1)		$I_{LDO} = 500\mu A$	23	46		μA
		Green Mode	1.5	[3]		μA
		LDO disabled			1	
Green Mode Transition time		GREEN MODE to Normal Mode, $I_{out} = 1mA$ (Note1)	60	120		usec
Load regulation (Note 1)		Normal Mode, $1mA < I_{LDO} < 150mA$	0.05			%
		Green Mode, $1mA < I_{LDO} < 5mA$	0.05			%
Line regulation (Note 1)		Normal Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 100mA$	0.01			%
		Green Mode, $3.2V < V_{IN} < 5.5V$, $I_{LDO} = 1mA$	0.05			%
Drop-out voltage		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$, $T_A = 25^{\circ}C$	60	[120]		mV
		Normal Mode, $I_{LDO} = I_{max}$, $V_{in} = 1.7V$	150	[450]		mV
		Green Mode, $I_{LDO} = I_{max}$, $V_{in} = 3.7V$	150	[300]		mV
Output Current limit (Note3)		LDO output short to GND	[150]	255	[375]	mA
Output Load Transient		Normal Mode $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{MAX}$, $t_R = t_F = 1\mu s$	66			mV
		Green Mode, $I_{LDO} = 1\% \text{ to } 100\%$ to $1\% \text{ of } I_{MAX}$, $t_R = t_F = 1\mu s$	25	[50]		mV
Output Line Transient		Normal Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$	5			mV
		Green Mode, $V_{IN} = V_{NOM} + 0.3V$ to $V_{NOM} + 0.8V$ to $V_{NOM} + 0.3V$, $t_R = t_F = 1\mu s$	5	[10]		mV
Power Supply Reject $\sum LDO/\sum V_{IN}$		$f = 10Hz - 10kHz$, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\% \text{ of } f = 1kHz$			79	dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Imax. Vin=Vnom+1V f=10kHz f=100kHz f=1MHz	68			dB
			50			dB
			50			dB
Output Noise Volt. (RMS)		100Hz-100kHz, $C_{LDO} = 1\mu F$, $I_{LDO} = 10\%$ or Imax, Vout=Vmax		80		μV_{RMS}
Start-Up Ramp Rate		After Enabling		100		mV/us
Soft Start Time (Note1)		From shut down to Output regulation	40	100		us
Start-up transient overshoot (Note1)		$C_{LDO} = 1\mu F$, $I_{LDO} = 150mA$	3	50		mV
Shutdown Output Resistance			[50]	160	[400]	Ω
Thermal Shutdown		T _j Rising		165		$^{\circ}C$
		T _j Falling		150		

Note1. Design guidance only, not tested during final test.

5.1.19 LDO21 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Guaranteed by Output Accuracy		$V_{OUT}+0.3$		5.5	V
System Voltage Range	$V_{SYS}-V_{OUT} \geq 1.5V$		2.45		5.5	V
Default output voltage(MAX8997)	1mA@ $V_{IN} = +5.5V$ 300mA@ $V_{IN} = 3.6V$		-3%	1.2	+3%	V
Default output voltage(MAX8966)	1mA@ $V_{IN} = +5.5V$ 300mA@ $V_{IN} = 3.6V$		-3%	1.2	+3%	V
Output Voltage Range	Programmable in 50mV/Step ($V_{BATT}-V_{OUT} \geq 1.5V$)		0.8		3.95	V
Output Voltage Accuracy	Normal Mode	$V_{IN}=3.4V$ & $I_{OUT}=I_{max}$ $V_{IN}=5.5V$ & $I_{OUT}=1mA$	-3		+3	%
	Green Mode	$V_{IN}=3.4V$ & $I_{OUT}=I_{max}$ $V_{IN}=5.5V$ & $I_{OUT}=1mA$	-3		+3	%
Maximum Output Current	Normal Mode (I_{max})				300	mA
	Green Mode				5	
Minimum Output Capacitance (Note 2, 4)	$0\mu A < I_{LDO} < I_{max}$, MAX ESR < 150mΩ	Normal Mode		2.2		μF
Input Supply Current(Note1)	Shutdown, $T_A=25^\circ C$			1		μA
	Normal Regulation Mode, No Load			30	[58]	
	Green Mode, No Load			1.5	[3]	
Load Regulation (Note 3)	Normal Mode	$1mA < I_{LDO} < 450mA$		0.05		%
	Green Mode	$0.1mA < I_{LDO} < 5mA$		0.05		
Line Regulation (Note 3)	Normal Mode	$V_{IN} = V_{NOM}+0.3V$ to $5.5V$, $I_{LDO}=100mA$		0.01		%
	Green Mode	$V_{IN} = V_{NOM}+0.3V$ to $5.5V$, $I_{LDO}=1mA$		0.05		%
Drop-out Voltage	Normal Mode	$I_{LDO}=I_{MAX}$, $V_{IN}-V_{OUT}=2.5V$		50	[100]	mV
		$I_{LDO}=I_{MAX}$, $V_{IN}-V_{OUT}=1.5V$		150	[450]	
	Green Mode	$I_{LDO}=5mA$, $V_{IN}=3.7V$		150	[300]	
Output Current Limit (Note 4)	LDO output short to GND		[300]	510	[900]	mA
Output Load Transient (Note3, Note 4)	Normal Mode	$I_{LDO} = 1\%$ to 100% to 1% of I_{MAX} , $t_R = t_F = 1\mu s$		66		mV
	Green Mode	$I_{LDO} = 0.05mA$ to $5mA$ to $0.05mA$, $t_R = t_F = 1\mu s$		25	[50]	
Output Line Transient (Note3, Note 4)	Normal Mode	$V_{IN}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$		5	[10]	mV
	Green Mode	$V_{IN}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$		5	[10]	
Power Supply Reject $\sum LDO/\Sigma V_{IN}$	$f=10Hz-10kHz$, $I_{LDO}=10\%$ of I_{MAX} , $V_{IN}=V_{NOM}+1V$, $V_{INAC}=50mV$		$f=1kHz$	88		dB
			$f=10kHz$	65		
			$f=100kHz$	51		
	Green Mode, $I_{LDO}=1mA$		$f=1MHz$	50		
Output Noise Volt. (RMS)	$10Hz-100kHz$, $V_{OUT} = 0.8V$ $I_{LDO}=10\%$ of I_{max}			67		μV_{RMS}
Start-up transient overshoot (Note1)	$I_{LDO} = 150mA$			3	50	mV

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Start-Up Ramp Rate	After enabling		100		mV/ μ s
Soft Start Time (Note 1)	From shutdown to Output regulation		40	100	μ s
Active-Discharge Resistance	$V_{OUT}=1V$, Regulator Disabled	[20]	30	[150]	Ω
Thermal Shutdown	T_J Rising		165		$^{\circ}$ C
	T_J Falling		150		

Note1. Design guidance only, not tested during final test.

Note 2. For stability requirements refer to the Remote Capacitor Design with Register Adjustable Compensation section.

Note 3. Does not include ESR of the capacitance or trace resistance of the module/PCB.

Note 4. Values are based on simulations and bench testing; they are not production tested.

5.2 Backup Battery charger– VCOIN

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Default output voltage VCOIN	Iload=1 μ A	-3%	3.0	+3%	V
Programmable output voltage range	Iload=1 μ A	-3%	2.5 3.0 3.3 3.5	+3%	
Constant Current Limit	V_{COIN} short to GND	80 100 200 400 600 800			μ A
Internal Series Resistor		Bypass 1 3 6			k Ω
Reverse Leakage current from Output	$V_{BATT}=0V, V_{COIN}=3.0V$			10	μ A
Regulator ground current	Iload=1 μ A (note1)		5		μ A

Note 1: Design guidance only, not tested during final test.

5.3 32kHz Clock – 32kHzCP and 32kHzAP

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output High Voltage for 32kHzCP	Internal logic supply Isource = 200 μ A	$V_{CC_32CP} - 0.2$			V
Output High Voltage for 32kHzAP	Internal logic supply Isource = 2mA	LDO9 - 0.45			
Output Low Voltage for 32kHzAP	Internal logic supply Isink = 200 μ A			0.45	V
Output Low Voltage for 32kHzCP	Internal logic supply Isink = 200 μ A			0.2	V
Output duty cycle	Note 1		50		%

Note 1: Test has no crystal so this is Not measurable.

5.4 RTC

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $C_{VCOIN} = 0.22\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage Range VCOIN	$VBATT=IN_ = OPEN$ (Note T)	1.8		3.6	V
Timekeeping Current, IBK	$VBATT=IN_ = OPEN$, $VCOIN = 3.0V$,		3	6	uA
Start-up time	(Note T)		2.5		sec
Time Accuracy	Per day (Note T)		2		sec
XIN to ground capacitance			25		pF
XOUT to ground capacitance			25		pF

Note T: Design guidance only, not tested during final test.

5.5 MAIN CHARGER

Operating conditions (unless otherwise specified) $VDCIN=5.0V$, $V_{BATT} = 4V$, $T_A = -40^\circ C$ to $+85^\circ C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DCIN					
Input Voltage Range VDCIN	(Note 1)	0		28	V
Input Operating Range	(Note 2)	4.0		7	V
VDCINOK Trip point (UVLO<VDCIN<OV P)	VDCIN – V_{BATT} , rising	(150)	250	(350)	
	VDCIN – V_{BATT} , falling	(20)	45	(100)	mV
	VDCIN – V_{BATT} , Hysteresis		205		
Input Undervoltage Threshold	VDCIN rising, 600mV Hysteresis (typ.)	3.8	3.9	4.0	V
Input Overvoltage Threshold	VDCIN rising, 200mV Hysteresis (typ.)	OTPCGHCVS=00 (default) OTPCGHCVS=01 OTPCGHCVS=10 OTPCGHCVS=11	7.2 6.0 6.5 7.0	7.5 6.0 6.5 7.0	V
Input Supply Current	$I_{BATT}=0mA$,		750	1500	µA
VL	IVL=0 to 100uA	[]	3.0	[]	V
Shutdown Input Current	MBHOSTEN = 0			500	µA
VDCIN to BATT input resistance	VDCIN=4.1V, $V_{BATT} = 4.0V$ at 450mA		0.4	(0.8)	Ω
BATT					
BATT Regulation Voltage	$I_{BATT}=100mA$ Default	$T_A=+25^\circ C$, $MBCCV=0000$ $T_A=-40^\circ C$ to $+85^\circ C$, $MBCCV=0000$	4.179 4.158	4.2 4.2	4.221 4.242
BATT Regulation Programmable Range	$I_{BATT}=100mA$	20mV step except 1111 and 4.18V to 4.28V	4.000 ($MBCCV=001$)		4.350 ($MBCCV=1111$)
BATT Restart Fast Charge Threshold	From BATT regulation Voltage (active only when AUTOSTOP is enabled)		-150		mV

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS	
BATT Restart Fast charge debounce					62		ms	
VDCIN Fast Charge Current	V _{BATT} =3.5V	MBCICHFCSET=1 MBCICHFC [3:0] VCHGR_FC =0101	0000		200		mA	
			0001		250			
			0010		300			
			0011		350			
			0100		400			
			0101 (default)	414	450	486		
			0110		500			
			0111		550			
			1000		600			
			1001		650			
			1010		700			
			1011		750			
			1100		800			
			1101		850			
			1110		900			
			1111		950			
MBCICHFCSET=0					90		mA	
VDCIN Pre-Charge Current	V _{BATT} =2V, VDCIN=5V				47.5		mA	
Soft-Start Time	Ramp Time 90mA to Fast Charge Current (Design Guidance)				1.2		ms	
Pre-Charge threshold	Default condition. Hysteresis=170mV				2.5		V	
VICHG	IBATT=50mA				75		mV	
	IBATT=500mA				750			
	IBATT=950mA				1425			
VICHG Zout					20		kΩ	
TOP-OFF								

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	
Top-Off Threshold	I _{BATT} falling, Battery is charged	ITOPOFF[3:0] 0000(Default) 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111		50 60 70 80 90 100 110 120 130 140 150 160 170 180 190 200			mA
Timer							
Timer Accuracy			-20		20	%	
Precharge watchdog timer timeout				30		mins	
Fast Charge Timer	Fast charge timer is disabled in 90mA fast charge mode	TFCH =010 (default)		5		hours	
		TFCH =011		6			
		TFCH =100		7			
		TFCH =111		Disable			
Top-off Timer				30		mins	
Debounce time on Charger interrupts	CHGINS			62		ms	
	CHGRM, DCINOPV, TOPOFFR, (interrupt3 register)			2		ms	
Thermal Loop							
Thermal Limit Temperature	Junction Temperature when the charge current is reduced, T _J rising			105		°C	
DETBAT/							
Logic Input Low Threshold					0.4	V	
Logic Input High Threshold			1.3			V	
Pull-Up Resistor	DETBAT/ to VL			470		kΩ	
SAFEOUT1							
Output Voltage (Default ON)	5.0V < V _{DCIN} < 5.5V, I _{out} =10mA SAFEOUT1=01(default)		4.8	4.9	5.0	V	
	SAFEOUT1=00			4.85		V	
	SAFEOUT1=10			4.95		V	
	SAFEOUT1=11			3.3		V	
PSRR	V _{DCIN} =5.5, F=100kHz, C _{OUT} =1uF			60		dB	
Maximum Output Current			60			mA	
Output Current Limit			70	150	250	mA	

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Dropout Voltage	$V_{DCIN}=5V$, $I_{OUT}=60mA$		120		mV
Line Regulation	$5.5V \leq V_{DCIN} \leq 7.0V$, $I_{OUT}=1mA$		1		mV
Load Regulation	$V_{DCIN} = 5.5V$, $30\mu A < I_{OUT} < 30mA$		50		mV
Quiescent Supply Current			55		μA
Output Capacitor for Stable Operation (Note1)	$0\mu A < I_{OUT} < 30mA$, MAX ESR = 50m Ω	0.7	1.0		μF
Internal Off-Discharge Resistance			100		Ω
SAFEOUT2					
Output Voltage (Default OFF)	$5.0V < V_{DCIN} < 5.5V$, $I_{OUT}=10mA$ SAFEOUT2=01(default)	4.8	4.9	5.0	V
	SAFEOUT2=00		4.85		V
	SAFEOUT2=10		4.95		V
	SAFEOUT2=11		3.3		V
PSRR	$V_{DCIN}=5.5$, $F=100kHz$, $C_{OUT}=1\mu F$		60		dB
Maximum Output Current		60			mA
Output Current Limit		70	150	250	mA
Dropout Voltage	$V_{DCIN}=5V$, $I_{OUT}=60mA$		120		mV
Line Regulation	$5.5V \leq V_{DCIN} \leq 7.0V$, $I_{OUT}=1mA$		1		mV
Load Regulation	$V_{DCIN} = 5.5V$, $30\mu A < I_{OUT} < 30mA$		50		mV
Quiescent Supply Current			55		μA
Output Capacitor for Stable Operation (Note1)	$0\mu A < I_{OUT} < 30mA$, MAX ESR = 50m Ω	0.7	1.0		μF
Internal Off-Discharge Resistance			100		Ω

Note1. Design guidance only, not tested during final test.

Note2) Guaranteed by undervoltage and overvoltage threshold testing. For complete charging, the input voltage must be greater than 4.32V.

5.6 Battery Monitor Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT} = V_{IN1}$ to $V_{IN6} = +3.7V$, $C_{BATT+\Sigma IN} = 43.3\mu F$, $C_{REFBP} = 100nF$, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Programmable Low Battery Detect (LOBAT1)					
Programmable Low Battery Detect Hysteresis (Note 2)	LB1HYST = 00 LB1HYST = 01 LB1HYST = 10 LB1HYST = 11		100 200(Default) 300 400		mV
Programmable Low Battery Detect Threshold	LB1TH = 000 LB1TH = 001 LB1TH = 010 LB1TH = 011 LB1TH = 100 LB1TH = 101 LB1TH = 110 LB1TH = 111		2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.57		V
	-3%	3.57 (Default for LOBAT1)	+3%		
Programmable Low Battery Detect (LOBAT2)					
Programmable Low Battery Detect Hysteresis (Note 2)	LB2HYST = 00 LB2HYST = 01 LB2HYST = 10 LB2HYST = 11		100 200(Default) 300 400		mV
Programmable Low Battery Detect Threshold	LB2TH = 000 LB2TH = 001 LB2TH = 010 LB2TH = 011 LB2TH = 100 LB2TH = 101 LB2TH = 110 LB2TH = 111		2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.57		V
	-3%	3.3 (Default for LOBAT2)	+3%		
Debounce time for Low Battery Detect (LOBAT1 and LOBAT2)			64		ms

5.7 FUEL GAUGE

V_{BATT} = 2.5V to 4.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{BATT}	(Note 1)	2.5		4.5	V
Supply Current (Note 2)	I_{DD0}	Shutdown Mode,		0.5		μA
	I_{DD1}	ACTIVE Mode, average current		25	42	
VB Regulation Voltage			1.5		1.9	V
Power Fail Warning Voltage	V_{PFW}			2.1	2.5	V
Measurement Error, V_{BATT}	V_{GERR}	T_A = 25°C	- 7.5		+ 7.5	mV
		T_A = 0°C to +85°C	- 20		+ 20	
		Expanded Temp Range	-35		+35	
VBATT Measurement Resolution,				0.625		mV
VBATT Measurement Range			2.5		5.12	V
Input Resistance SNS, AIN			15			MΩ
Ratio-Metric Measurement Accuracy, AIN			-0.5		+0.5	%
Ratio-Metric Measurement Resolution, AIN				0.024 4		% Full Scale
Current Register Resolution	I_{LSB}			1.562 5		μV
Current Full-Scale Magnitude	I_{FS}			±51.2		mV
Current Offset	I_{OERR}			±1.5		μV
Current Gain Error	I_{GERR}	T_A = 0°C to +85°C	- 1		+ 1	% of readin g
		Expanded Temp Range	□	□		
Time-base Accuracy (Note 2)	t_{ERR}	V_{DD} = 3.6V at +25°C	- 1		+ 1	%
		T_A = 0°C to +50°C	- 2.5		+ 2.5	
		T_A = -20°C to +70°C	- 3.5		+ 3.5	
THRM Output Drive		I_0 = 0.5mA	VTT - 0.1			V
THRM Precharge Time	t_{PRE}		8.48			μs
ALRT, SDAFG, SCLFG Input Logic High	V_{IH}		1.5			V
ALRT, SDAFG, SCLFG Input Logic Low	V_{IL}				0.5	V
ALRT, SDAFG Output Logic Low	V_{OL}	I_{OL} = 4mA			0.4	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ALRT, SDAFG Pull-down Current	I _{PD}	ACTIVE mode, V _{ALRT} = V _{SDA} = 0.4V	0.05	0.2	0.4	µA
ALRT leakage					1	µA
THRM Operating Range			2.5		V _{TT}	V
Battery Removal Detection Threshold – V _A IN rising	V _{DETR}	V _{THRM} -V _A IN (Expanded Temp Range)	40	125	200	mV
Battery Removal Detection Threshold – V _A IN falling	V _{DETF}	V _{THRM} -V _A IN (Expanded Temp Range)	70	150	230	mV
Battery Removal Detection Comparator Delay	t _{TOFF}	V _A IN step from 70 to 100% of V _{THRM} to ALRT falling Alrtp = logic 0 EnAIN = logic 1 FTHRM = logic 1			100	us
Required External AIN Capacitance		RTHM=10kohm NTC			100	nF

Note1. All voltages are referenced to GND.

Note2. Design guidance only.

2-WIRE INTERFACE					
SCLFG Clock Frequency	f _{SCL}	(Note 2)	0	400	KHz
Bus Free Time Between a STOP and START Condition	t _{BUF}		1.3		µS
Hold Time (Repeated) START Condition	t _{HD:STA}	(Note 3)	0.6		µS
Low Period of SCLFG Clock	t _{LOW}		1.3		µS
High Period of SCLFG Clock	t _{HIGH}		0.6		µS
Setup Time for a Repeated START Condition	t _{SU:STA}		0.6		µS
Data Hold Time	t _{HD:DAT}	(Note 4, 5)	0	0.9	µS
Data Setup Time	t _{SU:DAT}	(Note 4)	100		nS
Rise Time of Both SDAFG and SCLFG Signals	t _R		20 + 0.1C _B	300	nS
Fall Time of Both SDAFG and SCLFG Signals	t _F		20 + 0.1C _B	300	nS
Setup Time for STOP Condition	t _{SU:STO}		0.6		µS
Spike Pulse Widths Suppressed by Input Filter	t _{SP}	(Note 6)	0	50	nS
Capacitive Load for Each Bus Line	C _B	(Note 7)		400	pF
SCLFG, SDAFG Input Capacitance	C _{BIN}			60	pF

Note 1: All voltages are referenced to GND.

Note 2: Timing must be fast enough to prevent the device from entering shutdown mode due to bus low for a period > 45s minimum.

Note 3: fSCLFG must meet the minimum clock low time plus the rise/fall times.

Note 4: The maximum tHD:DAT has only to be met if the device does not stretch the low period (tLOW) of the SCLFG signal.

Note 5: This device internally provides a hold time of at least 100ns for the SDAFG signal (referred to the VIHin of the SCLFG signal) to bridge the undefined region of the falling edge of SCLFG.

Note 6: Filters on SDAFG and SCLFG suppress noise spikes at the input buffers and delay the sampling instant.

Note 7: CB-total capacitance of one bus line in pF.

5.8 MUIC and Level Translator

($V_{BATT} = +3.0V$ to $+5.5V$, $V_{DCIN} = +3.5V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{BAT} = 3.6V$, $V_{DCIN} = 5.0V$, $T_A = +25^{\circ}C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range V_{BUS}	V_{DCIN}		0		28	V
Supply voltage range	V_{BATT}		2.8		5.5	V
	V_{DCIN}		3.5		28	
DCIN Supply Current	I_{DCIN}	$V_{BATT}=0$, $V_{DCIN}=5V$, $CPEn=0$, No accessory attached.		350	500	μA
Internal VB regulator	V_{PVB}		3.3	4	5.5	V
MUIC Voltage Bandgap	V_{bg}			1.213		V
Internal SWPOS regulator	V_{SWPOS}		3.3	3.4	3.5	V
Internal SWNEG regulator	V_{SWNEG}		-2.0	-1.9	-1.8	V
BC on-resistance	R_{onbc}	$I_{BC} = 1mA$		0.6	1.5	Ω

CHARGER DETECTION

VB Detect Threshold	V_{VBDET}		3.3	3.5	3.7	V
VB Detect Threshold hysteresis	V_{VBDET_hyst}			50		mV
V_{DP_SRC/ DM_SRC} Voltage (source)	V_{DP_SRC}	$I_{LOAD} = 100\mu A$	0.5	0.6	0.7	V
V_{DAT_REF} Voltage (Threshold)	V_{DAT_REF}		0.25	0.3	0.35	V
V_{LGC} Voltage (Threshold)	V_{LGC}		1.15	1.24	1.3	V
I_{DM_SINK/DP_SINK} Current	I_{DM_SINK}	$0.15 \leq VDP = VDM \leq 3.6V$	55	80	115	μA
I_{DP_SRC} Current	I_{DP_SRC}	$0 \leq VDP \leq 2.5V$	5	8	10	μA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
R _{DM_DWN/DP_DWN} Resistor	R _{DM_DWN}		17	20	23	kΩ
I _{WEAK} Current	I _{WEAK}	DM voltages = 0.15V or 3.6V	0.01	0.15	0.3	uA
VBUS25 Ratio	VBUS25	Reference ratio for Special Charger as a percentage of VDCIN voltage (VDCIN=5V)(Note6)	22.5	25	27.5	%
VBUS47 Ratio	VBUS47		42.3	47	51.7	%
Weak Battery Threshold(Note7)	V _{WB}	Measured at BATT (option 1 – default)	3.6	3.7	3.8	V
		Measured at BATT (option 2)	3.4	3.5	3.6	
		Measured at BATT (option 3)	3.2	3.3	3.4	
		Measured at BATT (option 4)	3.0	3.1	3.2	
ACCESSORY DETECTION						
UID Low Power Threshold	V _{UID_LOWP}	V _{BATT} =3.5V, V _{DCIN} =0,	1.49	1.68	1.88	V
UID Low Power PullUP Resistor	R _{UID_LOWP}		2	3.4	6	MΩ
ADC_LOW Threshold	R _{ADC_LOW}		30	40	55	Ω
ADC ID pull_up currents	I _{PUP}	V(ID)=2.55V, 0.9V	-3%	2.28	+3%	uA
		V(ID)=2.50V, 0.76V	-3%	6	+3%	
		V(ID)=2.35V, 0.70V	-3%	16.7	+3%	
		V(ID)=2.20V, 0.57V	-3%	47	+3%	
		V(ID)=2.12V, 0.05V	-3%	153	+3%	
		V(ID)=2.04V, 0.05V	-5%	2500	+5%	
ADC Detection Resistors	R _{ADC}		Gnd		0.03	kΩ
			R1	1.98	2	
			R2	2.578	2.604	
			R3	3.176	3.208	
			R4	3.974	4.014	
			R5	4.772	4.82	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		R6	5.969	6.03	6.090	
		R7	7.95	8.03	8.11	
		R8	9.23	10.03	10.13	
		R9	11.91	12.03	12.15	
		R10	14.31	14.46	14.60	
		R11	17.08	17.26	17.43	
		R12	20.23	20.5	20.70	
		R13	23.92	24.07	24.31	
		R14	28.41	28.7	28.99	
		R15	33.66	34	34.34	
		R16	39.79	40.2	40.60	
		R17	49.40	49.9	50.40	
		R18	64.25	64.9	65.55	
		R19	79.26	80.07	80.87	
		R20	100.98	102	103.02	
		R21	119.79	121	122.21	
		R22	148.5	150	153	
		R23	198	200	202	
		R24	252.45	255	257.55	
		R25	297.99	301	304.07	
		R26	361.35	365	365.65	
		R27	457.56	442	446.42	
		R28	517.77	523	528.23	
		R29	612.81	619	625.19	
		R30	750	1000	1050	
		Open	1147			
USB ANALOG SWITCH (DN1, DP2)						
Analog Signal	V _{DN2,DP2}	CPEn=0 (Note1)	0		V _{CCINT}	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Range		CPEn=1	0		V_{SWPOS}	
On-Resistance	R_{ONUSB}	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $0V \leq V_{COM} \leq 3.0V$		3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONUSB}	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $V_{COM} = 400mV$			0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $0V \leq V_{COM} \leq 3.0V$		0.1	0.3	Ω
Off Leakage Current	$I_{LUSB(OFF)}$	$V_{BATT} = 4.2V$; switch open; V_{DN1} or $V_{DP2} = 0.3V$ or $+2.5V$ and $V_{COM_} = +2.5$ or $0.3V$	-360		360	nA
On Leakage Current	$I_{LUSB(ON)}$	$V_{BATT} = 4.2V$; switch closed; V_{DN1} or $V_{DP2} = 0.3V$ or $+2.5V$	-360		360	nA

UART ANALOG SWITCH (UT1, UR2)

Analog Signal Range	$V_{UT1,UR2_}$	No Accessory Attached and CPEn =0	0		V_{CCINT}	V
		Accessory Attached or CPEn =1	0		V_{SWPOS}	
On-Resistance	R_{ONUART}	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $0V \leq V_{COM} \leq 3.0V$		3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONUART}	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $V_{COM} = 1.5V$			0.5	Ω
On-Resistance Flatness	$R_{FLATUART}$	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $0V \leq V_{COM} \leq 3.0V$		0.1	0.3	Ω
Off Leakage Current	$I_{LUART(OFF)}$	$V_{BATT} = 4.2V$; switch open; V_{UT1} or $V_{UR2} = 0.3V$ or $+2.5V$ and $V_{COM_} = +2.5$ or $0.3V$	-360		360	nA
On Leakage Current	$I_{LUART(ON)}$	$V_{BATT} = 4.2V$; switch closed; V_{UT1} or $V_{UR2} = 0.3V$ or $+2.5V$	-360		360	nA

AUDIO ANALOG SWITCH (SL1, SR2)

Analog Signal Range	V_{AUDIO}	No Accessory Attached and CPEn =0 (Note1)	0		V_{CCINT}	V
		Accessory Attached or CPEn =1	V_{SWNEG}		V_{SWPOS}	
On-Resistance	R_{ONA}	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $0V \leq V_{COM} \leq 3.0V$		3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONA}	$V_{BATT} = 3.0V$, $I_{COM} = 10mA$, $V_{COM} = 1.5V$			0.5	Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
On-Resistance Flatness	R _{FLATA}	V _{BATT} = 3.0V, I _{COM} = 10mA, 0V ≤ V _{COM} ≤ 3.0V		0.1	0.3	Ω
AUDIO Off Leakage Current	I _{LA(OFF)}	V _{BATT} = 4.2V; switch open; V _{SL1} or V _{SR2} = 0.3V or +2.5V; V _{COM_} = +2.5 or 0.3V	-360		360	nA
AUDIO On Leakage Current	I _{LA(ON)}	V _{BATT} = 4.2V; switch closed; V _{SL1} or V _{SR2} = 0.3V or +2.5V	-360		360	nA
Shunt Resistor	R _{SHUNT}	I _{SHUNT} = 10mA	30	100	170	Ω

MIC ANALOG SWITCHES (MIC)

Analog Signal Range	V _{MIC}	No Accessory Attached and CPEn = 0 (Note1)	0		V _{CCINT}	V
		Accessory Attached or CPEn = 1	0		2.5V	
On-Resistance	R _{ONMI}	V _{BATT} = 3.0V, I _{MIC} = 10mA, 0.5V ≤ V _{MIC} ≤ 3.0V		30	50	Ω
On-Resistance Flatness	R _{FLATMI}	V _{BATT} = 3.0V, I _{MIC} = 10mA, 0.5V ≤ V _{MIC} ≤ 3.0V		3	5	Ω
MIC Off Leakage Current	I _{LMI(OFF)}	V _{BATT} = 4.2V; switch open; V _{MIC} = 0.3V or +2.5V and V _{DCIN} = +2.5 or 0.3V	-360		360	nA
MIC On Leakage Current	I _{LMI(ON)}	V _{BATT} = 4.2V; switch closed; V _{MIC} = 0.3V or +2.5V		32	60	uA

ID BYPASS ANALOG SWITCH (IDB)

Analog Signal Range	V _{IDB}	No Accessory Attached & CPEn = 0	0		V _{CCINT}	V
		Accessory Attached or CPEn = 1	0		3	
On-Resistance	R _{ONIDB}	V _{BATT} = 3.0V, I _{IDB} = 10mA, 0V ≤ V _{IDB} ≤ 2.5V		3	6	Ω
On-Resistance Flatness	R _{FLATV}	V _{BATT} = 3.0V, I _{IDB} = 10M, 0V ≤ V _{IDB} ≤ 2.5V		0.1	0.3	Ω
IDB Off Leakage Current	I _{LIDB(OFF)}	V _{BATT} = 4.2V; switch open; V _{IDB} = 0V or 3V and V _{UID} = +2.5 or 0.5V	-360		360	nA
IDB On Leakage Current	I _{LIDB(ON)}	V _{BATT} = 4.2V; switch closed; V _{IDB} = 0V or +3V	-360		360	nA
COMN1, COMP2 Off Leakage Current	I _{LCOM(OFF)}	V _{COM_} = -1.5V or 2.5V, switch open	-300		300	nA
UID Off Leakage Current	I _{LUID(OFF)}	V _{UID} = 0V or 2.5V, switch open	-300		300	nA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL SIGNALS (BOOT)						
Output Logic High (BOOT)	V _{OH}	I _{SOURCE} =1mA	LDO9-0.2V			V
Output Logic Low (BOOT)	V _{OL}	I _{SINK} =1mA			0.4	V
LEVEL TRANSLATOR						
1.8V Supply Voltage	V _{18V}		1.65		5.5	V
1.8V Input Logic High	V _{18IH}	18R1, 18RNC1	0.8* 18VLL			V
1.8V Input Logic Low	V _{18IL}	18R1, 18RNC1			0.4	V
2.8V Input Logic High	V _{28IH}	28R2, 28RN01, 28RCOM2	2			V
2.8V Input Logic Low	V _{28IL}	28R2, 28RN01, 28RCOM2			0.4	V
CB Input Logic High	V _{CBIH}		1.4			V
CB Input Logic Low	V _{CBIL}				0.4	V
1.8V Output Logic High	V _{180H}	18T2, 18TNC2 I _{SOURCE} = 2mA	0.85* 18VLL/			V
1.8V Output Logic Low	V _{180L}	18T2, 18TNC2 I _{SINK} = 2mA			0.3	V
2.8V Output Logic High	V _{280H}	28T1, 28TCOM1, 28TN02, 28T3 I _{SOURCE} = 2mA	0.85* LDO9			V
2.8V Output Logic Low	V _{280L}	28T1, 28TCOM1, 28TN02, 28T3 I _{SINK} = 2mA			0.3	V
Input Leakage	I _L	V _{IN} = V _{LDO9} or V _{18VLLT}	-1		+1	uA
1.8V Supply Current	I _{18VLL}	V _{IN} = 0V or 18VLL, I _{OUT} =0mA			1.5	uA
2.8V Supply Current	I ₂₈	V _{IN} = 0V or V _{LDO9} , I _{OUT} =0mA (Note8)			1.5	uA
Propagation Delay	t _{PROP}	From 50% of V _{IN} to 20% or 80% of V _{OUT}			10	ns
Input Capacitance	C _{IN}			5		pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
Analog Switch Turn On Time	t_{ON}	I2C Stop to Switch On; $R_L = 50\Omega$		0.2	0.5	ms
Analog Switch Turn Off Time	t_{OFF}	I2C Stop to Switch Off; $R_L = 50\Omega$		0.1	0.5	ms
Break-Before-Make Delay Time	t_{BBM}	$R_L = 50\Omega$; $T = +25^\circ\text{C}$ (Note 8)	0			μs
Mic Clock Period	T_{CK}			14.64		μs
Dead Battery Timer	t_{DBTMR}	Note1.			45	min
USB Charger Detect Time	t_{DPSRC_ON}	Option 1 ($D_{ChkTm}=0$)	40	50	60	ms
		Option 2 ($D_{ChkTm}=1$)	500	625	750	ms
JIG and BOOT Assertion Time	t_{JBDLY}	Resistor attached to ID till BOOT assert (Note 9)		0.5		ms
Charger detect current delay	$t_{VDPSRC_HIC_RNT}$		40		60	ms
DCIN Debounce Time	t_{MDEB}	All Comparators	20	30	40	ms
DCD Debounce Time			36	40	44	ms
DCD Time OUT			1.8	2	2.2	sec
COMN1, COMP2 On Capacitance	C_{ONCOM}	$V=0.5\text{Vp-p}$, DC bias = 0V, f=240MHz, COM_ connected to DN1,DP2		7		pF
UID On Capacitance	C_{ONUID}	$V=0.5\text{Vp-p}$, DC bias = 0V, f=240MHz, UID connected to IDB		7		pF
Off Capacitance		$F=1\text{MHz}$, $V=0.5\text{Vp-p}$, DC bias = 0V	UT1, UR2	3		pF
			DN1, DP2	3		
			MIC	3		
			IDB	3		
Off-Isolation	V_{ISO}	$R_L = 50\Omega$; $f = 20\text{kHz}$; $V_{COM_} = 0.5\text{V}_{\text{P-P}}$	UT1, UR2	-60		dB
MIC Isolation	M_{ISO}	BATT to MIC (MIC to UID switch enabled) $R_L = 600\Omega$; $f = 100\text{Hz}$ to 6kHz; $V_{BATT} = 3.6\text{V} \pm 0.5\text{V}_{\text{P-P}}$		80		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
BAT Supply PSRR		Noise from BATT to COMN1,COMP2 or MIC, $R_L = 50\Omega$; $f = 10\text{kHz}$, $V_{BAT}=3.6 \pm 0.2V$		90		dB
Cross-talk	V_{CT}	Any switch to any switch, $R_L = 50\Omega$; $f = 20\text{kHz}$; $V_{COM_} = 1V_{RMS}$;		100		dB
MIC Total Harmonic Distortion	THD	MIC Channel, $f = 20\text{Hz}$ to 20kHz , $V_{COM_} = 0.5V_{P-P}$, $R_L = 50\Omega$; DC bias=1V, $T=+25^\circ\text{C}$		0.05		%
ESD PROTECTION						
COMN1, COMP2, UID, BC		Human Body Model		± 15		kV
All Other Pins		Human Body Model		± 1.5		kV

Note1) VSWPOS = min(VCCINT, +3.3V)

Note2) VCCINT = max(VBAT, min(VBUS, +4V))

Note 5: All devices are 100% production tested at $TA = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

Note 6: BUS25 and BUS47 are the outputs of the charger detection comparators. BUS25 is high when the DN1 voltage falls 25%(typ) below VBUS. Likewise, BUS47 is high when the DN1 voltage falls 47% below VBUS.

Note7: Disabled by default. Refer to the USB Battery Charging Specification Revision 1.1 from USB.org.

Note8: Not production tested. Guaranteed by design.

Note9: The JIG and BOOT assertion time is a function of the ADC debounce time. Set the ADCDbSET bits in the CONTROL3 register to adjust this delay.

5.9 HAPTIC MOTOR DRIVER

($V_{IN_MOTOR} = 1.71V$ to $3.6V$, $V_{IN_MOTOR} = 1.71V$ to $3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, DP, DN inactive, unless otherwise noted. Typical values are at $V_{DD} = 3.3V$, $V_{DDM} = 3.3V$, $T_A = 25^{\circ}C$.) $C_{VDDM}=10\mu F$, $C_{VDD}=0.1\mu F$, LRA Mode = 128X.

PARAMETER	SYMBOL	CONDITIONS	Specifications			UNIT
			Min	Typ	Max	
PWM Input (MPWM)						
Input Frequency		Square wave input	10		50	kHz
Input Current		Pull-down to ground		10		μA
Input Logic High Voltage	V_{IH}		1.4			V
Input Logic Low Voltage	V_{IL}				0.4	V
Input Capacitance	C_{IN}	(Note 1)		10		pF
Motor Driver Outputs (MDP, MDN)						
Output Voltage	V_{DOL}	$V_{IN_MOTOR} = 3.0V$, $R_L = 30\Omega$, $T_A = 25^{\circ}C$			200	mV
Output Voltage	V_{DOH}	$V_{IN_MOTOR} = 3.0V$, $R_L = 30\Omega$, $T_A = 25^{\circ}C$	V_{IN_MO} TOR- 0.30			V
Output Current	I_L			300		mA
Wake up Time	T_{WU}	PWM=50% duty cycle, $C_F=3.9nF$			6	msec
Voltage Compliance		Guaranteed by design	0		V_{IN_M} OTOR	V
Motor Driver Feedback (MGAIN)						
Input Resistance	R_{IN}			60		k Ω
Input Capacitance	C_{IN}	(Note 1)		10		pF
Power Supply (IN_MOTOR)						
Supply Voltage	V_{IN_MOTOR}		2.7		5.5	V
Supply Current	I_{IN_MOTOR}	MEN= V_{BATT} , PWM=22.4kHz 50% duty cycle, LRA Mode, $R_L=30\Omega$, $C_1=3.9nF$ (Note 2)		6		mA
Power Down Supply Current	I_{PD}	MPWM=0V, $V_{IN_MOTOR}=2.7V$			10	μA

Note 1: Capacitance to GND or V_{DD} .

Note 2: Design Guidance Only. No production test.

5.10 GPIOs

Operating conditions (unless otherwise specified) $V_{IN_GPIO1}=V_{IN_GPIO2}=VCC$, $V_{BATT}=IN_-=+2V$ to $5.5V$, $C_{BATT+\Sigma IN}=30\mu F$, $T_A=-40^\circ C$ to $+85^\circ C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	I_{IN_GPIO}		1.6		5.5	V
Power Down Supply Current		GPIOs Open.		0.1		μA
Supply Current 1		GPIOs Open. All GPIO are in output mode,		0.1		μA
OFF State Leakage Current in Open Drain Mode	I_{OD_OFF}	$V_{IN_GPIO}=3.6V$, $T_A=+25^\circ C$		0.01		μA
		$V_{IN_GPIO}=3.6V$, $T_A=+85^\circ C$		0.1		
GPIO0-GPIO11 Logic Input Logic Low Threshold	V_{ILGPIO}	$V_{IN_GPIO}=3.6V$			0.3^* V_{IN_GPIO}	V
GPIO0-GPIO11 Logic Input High Threshold	V_{IHGPIO}	$V_{IN_GPIO}=3.6V$	0.7*	V_{IN_GPIO}		V
GPIO0-GPIO11 Output Logic Low Voltage (CMOS Push-Pull and Open Drain Modes)	V_{OLGPIO}	$V_{IN_GPIO}=1.6V$, $I_{OLGPIO}=4mA$			0.3^* V_{IN_GPIO}	V
GPIO0-GPIO11 Output Logic High Voltage (CMOS Push-Pull Mode)	V_{OHGPIO}	$V_{IN_GPIO}=1.6V$, $I_{OHGPIO}=4mA$	0.7*	V_{IN_GPIO}		V
GPIO_ Input Debounce Delay	t_{GPIO}	D7,D6=0,1		10		ms

5.1 Flash LED Driver

($V_{IN}=3.6V$, $T_A= -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. Note 1.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Voltage	(Note4)		2.7		5.5	V
LOGIC INTERFACE						
Logic Input High Voltage	$V_{IN} = 3.6V$	FLED_EN, GSMB	1.4			V
Logic Input Low Voltage	$V_{IN} = 3.6V$	FLED_EN, GSMB			0.4	V
FLED_EN and GSMB pull down resistor			400	800	1600	$K\Omega$

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Leakage Current (LED_EN, GSMB)	Flash LED driver block disabled, $V_{LED_EN} = V_{GSMB} = 0V$	$T_A = 25^\circ C$		0.1	1	
		$T_A = -40 \text{ to } 85^\circ C$		0.1		μA
STEP-UP DC/DC CONVERTER						
Input Supply Current	2MHz Switching, $V_{OUT}=5V$, no load, Note 4			15		mA
OUT Voltage Range	100mV steps		3.7		5.2	V
OUT Voltage Accuracy	$V_{OUT}=5V$, no load	$T_A=+25^\circ C$	-4	± 0.5	+4	$\%$
		$T_A=-40 \text{ to } 85^\circ C$	-8		+8	
OUT over voltage protection	when running in adaptive mode		5.2	5.35	5.6	V
Adaptive output voltage regulation threshold	$I_{FLED1} = I_{FLED2} = 492.4mA$,			150		mV
PGOOD Window Comparator	$V_{out}=5V$, in program mode		-15	-12.5	-8	$\%$
Line Regulation	$V_{IN}=2.7V \text{ to } 4.2V$ Note 4			0.1		$\%/V$
Load Regulation	$I_{OUT}=0 \text{ to } 1500mA$ Note 4			0.5		$\%/A$
Maximum OUT Current	$V_{IN} \geq 3.2V$, $V_{OUT}=5.0V$ Note 4		1550			mA
NFET Current Limit				5.0		A
LX NFET On Resistance	LX to PGND, $I_{LX}=200mA$			55	130	$m\Omega$
LX PFET On Resistance	LX to OUT, $I_{LX}=200mA$			120	200	$m\Omega$
LX Leakage	$V_{LX}=5.5V$	$T_A=+25^\circ C$		0.1	1	μA
		$T_A=+85^\circ C$		0.1		
Operating Frequency, No Load	2 MHz	$T_A= 0^\circ C \text{ to } +85^\circ C$	1.8	2	2.2	MHz
		$T_A=-40^\circ C \text{ to } +85^\circ C$	1.6		2.4	
Maximum Duty Cycle			65	75		$\%$
Minimum Duty Cycle				12		$\%$
COMP Transconductance	$V_{COMP}=750mV$			55		μS
COMP Discharge Resistance	During shutdown or UVLO, from COMP to GND			120		Ω
FLED1/FLED2 CURRENT SOURCE DRIVER						
Input Supply Current	Step-up off, FLED1/2 on, Supply Current for each current source			0.35		mA
Maximum Current Setting	Flash			750		mA
	Movie			250		mA

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Accuracy	23.44mA setting	$T_A = +25^\circ\text{C}$	-20		+5	%
	492.24mA setting	$T_A = +25^\circ\text{C}$	-4	± 0.5	+4	%
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-8		+8	%
Current Regulator Dropout	492.24mA setting, Note 2				110	mV
	93.75mA setting, 10% Dropout, Note 2			50	100	
FLED1/2_ Leakage in Shutdown	$V_{\text{FLED}} = 5.5\text{V}$	$T_A = +25^\circ\text{C}$	-1	0.1	1	μA
		$T_A = +85^\circ\text{C}$		0.1		μA
PROTECTION CIRCUITS						
Flash Duration Timer Range	Note 3, in 25ms steps		25		800	msec
Flash Duration Timer Accuracy (400 msec setting)	$T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$		360	400	440	mSec
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		320		480	
Flash Safety Timer Reset Inhibit Period	From falling edge of FLED_EN until first rising edge of FLED_EN			30		msec
Watch Dog Timer Range	In 4sec steps		4		16	Sec
Watch dog timer accuracy (4 sec setting)	$T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$		3.6	4	4.4	Sec
	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		3.2		4.8	
Open LED Detection Threshold	FLED1, FLED2 Enabled				100	mV
Shorted LED detection Threshold	FLED1, FLED2, enabled		$V_{\text{OUT}} - 1\text{V}$			V
Open and short debounce timer	From LED open or short detected until LED current regulator is disabled			10		msec
Thermal Shutdown Hysteresis				20		$^\circ\text{C}$
Thermal Shutdown				+160		$^\circ\text{C}$
MAXFLASH						
Low Battery Detect Threshold Range	33mV steps		2.5		3.4	V
Low Battery Voltage Threshold Accuracy				± 2.5		%
Low Battery Voltage Hysteresis Programmable Range			100		300	mV
Low Battery Voltage Hysteresis Step Size				100		mV
Low Battery Inhibit period	$\text{LB_TMR_R/F}[2:0]=000$		200	250	300	μSec
	$\text{LB_TMR_R/F}[1:0]=111$		1600	2000	2400	

Note 1: All devices are 100% production tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

Note 2: LED Current Regulator Dropout Voltage is defined as the voltage at which the current level drops by a certain percentage from the current level measured at 0.6V.

Note 3: Flash Duration is from rising edge of LED_EN until I_{LED} turns off (Safety Time in One-Shot mode)

Note 4: Parameter not production tested but is instead guaranteed by design through characterization.

6 Pin Description

Total 169 pins

	NAME	FUNCTION
Control and Communications		
D7	nIRQ1	PMIC Interrupt output. Open Drain Output.
D6	RSO\	Reset output signal for SS AP. Active low. Open drain output.
D9	MR1\	Manual reset input for hardware reset.
D8	MR2\	Manual reset input for hardware reset.
F5	PWRHOLD	Power hold input signal from SS AP. High-Z in off condition.
E6	JIGON	Input signal from JIGON switch. This pin has an internal 800kΩ pull-down resistor to GND.
E5	PWRON	Driving PWRON high causes MAX8966/MAX8997 booting up. -This pin has an internal 800kΩ pull-down resistor to GND.
F6	ONO\	PWRON signal indicator. Active low. Open drain output. High-Z in off condition.
F7	SDA	Data high-Z input for I ² C serial interface.
E7	SCL	Clock high-Z input for I ² C serial interface.
Clocks		
C2	XOUT	32.768kHz Crystal Pin. Oscillator Out. Connect 25pF externally.
C1	XIN	32.768kHz Crystal Pin. Oscillator input. Connect 25pF externally.
C4	32kHzCP	32.768kHz Crystal Oscillator Output for CP. 32kHzCP is a 50% duty cycle square wave buffered version of XIN that is driven between VCC_32CP and GND. Leave open if not used.
C3	32kHzAP	32.768kHz Crystal Oscillator Output for AP. 32kHzAP is a 50% duty cycle square wave buffered version of XIN that is driven between LDO9 and GND.
D4	VCC_32CP	VCC supply for 32kHzCP Buffer Output. Connect to GND if not used.
Main Charger		
F1	DCIN	High current charger input supply pin(s). Bypass to PGND with a 0.1uF ceramic capacitor. 5V input pin for Main Battery Charger
F2	DCIN	High current charger input supply pin(s). Bypass to PGND with a 0.1uF ceramic capacitor. 5V input pin for Main Battery Charger
D2	SAFEOUT1(LDO19)	4.8V Regulated LDO Output with Input Over-voltage Protection. Bypass SAFEOUT1 to GND with a 1uF or larger ceramic capacitor. SAFEOUT1 can be used to supply low voltage rated USB systems. Default ON
D3	SAFEOUT2(LDO20)	4.8V Regulated LDO Output with Input Over-voltage Protection. Bypass SAFEOUT2 to GND with a 1uF or larger ceramic capacitor. SAFEOUT2 can be used to supply low voltage rated USB systems. Default OFF
D1	VL	VL regulator output for charger internal usage. Bypass with 0.1Uf. Hi-Z in off condition.

E3	DETBAT\	Main-Battery Detect Input. If DETBAT\ is pulled to ground, this is an indication that the main battery is present therefore the main battery charger starts when the DCIN power input is valid. If DETBAT\ is driven high or left unconnected, this is an indication that the main battery is not present therefore the main battery charger does not start charging in response to a valid VAC and/or DCIN power input. DETBAT\ is internally pulled to VL through an internal 470kohm resistor.
E1	BATT	Charger Output and Main battery supply input for Reference, Bias, Power on/off logic, and internal blocks. Must have 1uF ceramic capacitor to GND. Battery positive terminal connection. Bypass to PGND with a ceramic capacitor.
E2	BATT	Charger Output and Main battery supply input for Reference, Bias, Power on/off logic, and internal blocks. Must have 1uF ceramic capacitor to GND. Battery positive terminal connection. Bypass to PGND with a ceramic capacitor.
F3	VICHG	Battery Charging Current Monitor Output. This pin will be an analog representation of the charger current and 1.5mV/mA. Low in shutdown.
Back up charger		
E4	VCOIN	Backup Battery charger output. Coin battery connects to this.
LDOs		
L13	INL1	input for LDO1, LDO9, LDO15
L12	INL2	input for LDO8, LDO16, LDO17
L11	INL3	input for LDO11, LDO14
L10	INL4	input for LDO12, LDO13, LDO18
N10	INL5	input for LDO4, LDO6, LDO7. Connect to Buck7 output or Main BATT
M10	INL6	input for LDO2, LDO3, LDO5, LDO10. Connect to Buck7 output or Main BATT
K9	IN21	input for LDO21. Connect to Buck output or Main BATT
M13	LDO1	Low Vin LDO1 output. Connect a ceramic capacitor from LDO1 to GND.
L8	LDO2	Low Vin LDO2 output. Connect a ceramic capacitor from LDO2 to GND.
M11	LDO3	Low Vin LDO3 output. Connect a ceramic capacitor from LDO3 to GND.
N12	LDO4	Low Vin LDO4 output. Connect a ceramic capacitor from LDO4 to GND.
M9	LDO5	Low Vin LDO5 output. Connect a ceramic capacitor from LDO5 to GND.
N11	LDO6	Low Vin LDO6 output. Connect a ceramic capacitor from LDO6 to GND.
N9	LDO7	Low Vin LDO7 output. Connect a ceramic capacitor from LDO7 to GND.
M12	LDO8	Low Vin LDO8 output. Connect a ceramic capacitor from LDO8 to GND.
J13	LDO9	Low Vin LDO9 output. Connect a ceramic capacitor from LDO9 to GND.
L9	LDO10	Low Vin LDO10 output. Connect a ceramic capacitor from LDO10 to GND.
J11	LDO11	Low Vin LDO11 output. Connect a ceramic capacitor from LDO11 to GND.
J10	LDO12	Low Vin LDO12 output. Connect a ceramic capacitor from LDO12 to GND.
J9	LDO13	Low Vin LDO13 output. Connect a ceramic capacitor from LDO13 to GND.
K11	LDO14	Low Vin LDO14 output. Connect a ceramic capacitor from LDO14 to GND.
K13	LDO15	Low Vin LDO15 output. Connect a ceramic capacitor from LDO15 to GND.
K12	LDO16	Low Vin LDO16 output. Connect a ceramic capacitor from LDO16 to GND.
J12	LDO17	Low Vin LDO17 output. Connect a ceramic capacitor from LDO17 to GND.
K10	LDO18	Low Vin LDO18 output. Connect a ceramic capacitor from LDO18 to GND.
K8	LDO21	Low Vin LDO21 output. Connect a ceramic capacitor from LDO21 to GND.
Bucks		
M8	INB01	Connect to Battery positive terminal, BUCK1 Input Terminal.
N8	INB01	Connect to Battery positive terminal, BUCK1 Input Terminal.
M7	LX1	Connect to Inductor. 1kohm in shutdown.
N7	LX1	Connect to Inductor. 1kohm in shutdown.
M6	PGND1	BUCK1 Power Ground

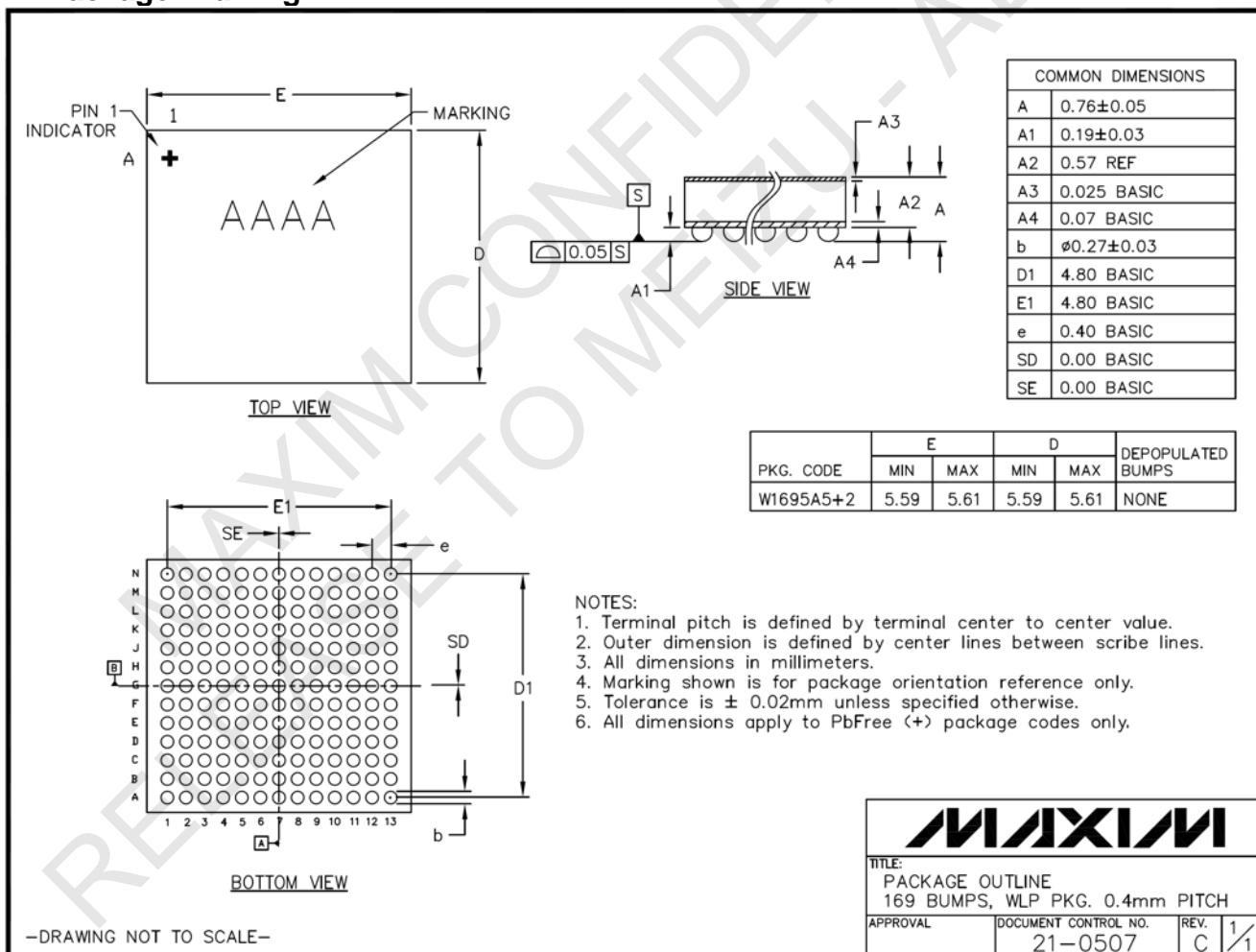
N6	PGND1	BUCK1 Power Ground
M5	BUCK1	Connect to BUCK1 output voltage
H8	SET1	Buck output selection pin. Three bits of SET1, SET2, SET3 select the output voltage of Buck1, Buck2, and Buck5. High-Z in off condition.
H7	SET2	Buck output selection pin. Three bits of SET1, SET2, SET3 select the output voltage of Buck1, Buck2, and Buck5. High-Z in off condition.
G7	SET3	Buck output selection pin. Three bits of SET1, SET2, SET3 select the output voltage of Buck1, Buck2, and Buck5. High-Z in off condition.
H9	PWREN	Enable pin for BUCK and LDO.
A12	INB02	Connect to Battery positive terminal, BUCK2 Input Terminal.
B13	LX2	Connect to Inductor. 1kohm in shutdown.
C12	PGND2	BUCK2 Power Ground
B12	BUCK2	Connect to BUCK2 output voltage.
E12	INB03	Connect to Battery positive terminal, BUCK3 Input Terminal.
D13	LX3	Connect to Inductor. 1kohm in shutdown.
C13	PGND3	BUCK3 Power Ground
D12	BUCK3	Connect to BUCK3 output voltage.
N3	INB04	Connect to Battery positive terminal, BUCK4 Input Terminal.
N4	LX4	Connect to Inductor. 1kohm in shutdown.
N5	PGND4	BUCK4 Power Ground
M4	BUCK4	Connect to BUCK4 output voltage.
M3	INB05	Connect to Battery positive terminal, BUCK5 Input Terminal.
N2	LX5	Connect to Inductor. 1kohm in shutdown.
M1	PGND5	BUCK5 Power Ground
M2	BUCK5	Connect to BUCK5 output voltage.
E13	INB07	Connect to Battery positive terminal, BUCK5 Input Terminal.
F13	LX7	Connect to Inductor. 1kohm in shutdown.
G12	PGND7	BUCK7 Power Ground
G13	PGND7	BUCK7 Power Ground
F12	BUCK7	Connect to BUCK7 output voltage.
PA Buck (Buck6)		
A9	INB06	Connect to Battery positive terminal, PA Buck Input and Bypass Input Terminal.
B9	INB06	Connect to Battery positive terminal, PA Buck Input and Bypass Input Terminal.
A8	LX6	Connect to Inductor
B8	LX6	Connect to Inductor
C7	REFINPA	DAC-Controlled Input. The output for the Step Down Converter is regulated to 3 x REFINPA.
A7	PGND6	BUCK6 Power Ground
B7	PGND6	BUCK6 Power Ground
C9	BUCK6	Output feedback input. Connect directly to BUCK6 output capacitor. BUCK6 is high impedance in shutdown. Output of Bypass LDO.
C8	BUCK6EN	BUCKPA enable pin. 800kohm pull down resistor in off condition
Fuel Gauge		
J8	VTT	Supply Input for thermistor bias switch. Connect to Main BATT if not used.
L6	KVSS	Current sense input.. Battery pack minus terminal and sense resistor sense input.
L7	SNS	Sense Resistor Connection. Ground pin for Fuel Gauge. Connect to GND
J6	THRM	Thermistor Bias Connection. Supply for Thermistor Resistor Divider. Connect to high side of the thermistor/resistor divider. THRM connects internally to VTT during temperature measurement.

J7	AIN	Auxiliary Voltage Input. Auxiliary voltage input from external thermal detection network. Bypass with 0.1uF to VSS. The input pin can be used for battery insertion/removal detection. Connect to VSS(GND) if not used.
K6	VBFG	2V Voltage Regulator Output. Bypass. 0.1uF.
K5	ALRT	Alert Indication. Open drain n-channel output. A 5K Ohm pull-up resistor to power rail is required. Alternatively, ALRT can be configured as a shutdown input, with the output function disabled.
J5	VBATTFG	Connect to the Main Battery.
K7	SCLFG	SCL for fuel Gauge.
L5	SDAFG	SDA for fuel Gauge
Haptic Motor Driver		
A11	IN_MOTOR	Motor driver power supply.
B11	MDP	Positive motor driver output
B10	MDN	Negative motor driver output
C11	MGAIN	Motor Driver Feedback.
C10	MPWM	Haptic PWM Input.
A10	GNDM	Motor driver ground.
MUIC		
J1	COMN1	Common Output 1. Connect to D- on mini/micro USB connector
K1	COMP2	Common Output 2. Connect to D+ on mini/micro USB connector
L1	UID	USB ID Input. Connect to ID on mini/micro USB connector
G2	BC	Connect the DCIN 1uF bypass capacitor to BC – allows microphone signals to be passed to the DCIN pin.
L3	BOOT	Factory Mode Select output pin. May be high, low or Hi-Z. Set based on resistor read from the ID pin or I2C register.
G1	DN1	USB Input 1 for D-
H1	DP2	USB Input 2 for D+
H3	UT1	UART TX Input 1
J3	UR2	UART RX Input 2
H2	SL1	Stereo Audio Input 1. (Negative rail capable)
J2	SR2	Stereo Audio Input 2. (Negative rail capable)
L2	IDB	USB ID pin Bypass. Used to directly sense the USB ID pin on the connector for USB OTG Transceivers.
K2	MIC_USB	Microphone Input
Level Translators		
J4	18R1	Input of LT channel 1 referenced to 18VLL
G4	28T1	Output of LT channel 1 referenced to 2.8V supply (LDO9)
K3	18T2	Output of LT channel 2 referenced to 18VLL
L4	28R2	Input of LT channel 2 referenced to 2.8V supply (LDO9)
F4	18VLL	Supply voltage Input for Level Translator channels 1 and 2 and Level Translator Switch
G3	18TNC2	Switch normally closed output 2 referenced to 18VLL
K4	28RCOM2	Switch Common channel 2 input referenced to 2.8V supply (LDO9)
H4	28TNO2	Switch normally open output 2 referenced to 2.8V supply (LDO9)
G5	18RNC1	Switch normally closed input 1 referenced to 18VLL
H5	28TCOM1	Switch Common channel 1 output referenced to 2.8V supply (LDO9)
H6	28RNO1	Switch normally open input 1 referenced to 2.8V supply (LDO9)
G6	CB	Switch control bit. Low NC connects to COM, high NO connects to COM
Ground		
H13	GND	ANALOG GROUND
H12	AGND	ANALOG GROUND

H11	DGND1	Digital Ground
B3	DGND2	Digital Ground
GPIOs		
D11	IN_GPIO1	Input pin for GPIO0 ~ GPIO5. Connect to Main BATT if not used.
D10	IN_GPIO2	Input pin for GPIO6 ~ GPIO11. Connect to Main BATT if not used.
H10	GPIO_GND	GPIO Ground
E11	GPIO0	GPIO0, Leave open if not used.
E10	GPIO1	GPIO1 , Leave open if not used.
F11	GPIO2	GPIO2, Leave open if not used.
F10	GPIO3	GPIO3, Leave open if not used.
G11	GPIO4	GPIO4, Leave open if not used.
G10	GPIO5	GPIO5, Leave open if not used.
E9	GPIO6	GPIO6, Leave open if not used.
E8	GPIO7	GPIO7, Leave open if not used.
F9	GPIO8	GPIO8, Leave open if not used.
F8	GPIO9	GPIO9, Leave open if not used.
G9	GPIO10	GPIO10, Leave open if not used.
G8	GPIO11	GPIO11, Leave open if not used.
Flash LED Driver		
B1	FGND	Flash LED Driver Ground. FLED1, FLED2 power ground, connect to PGND of IC
B2	FGND	Flash LED Driver Ground. FLED1, FLED2 power ground, connect to PGND of IC
A6	PGNDF	Power Ground for Flash LED Driver. Connect PGND to GND and to the input capacitor ground. Connect PGND to the PCB ground plane.
B6	PGNDF	Power Ground for Flash LED Driver. Connect PGND to GND and to the input capacitor ground. Connect PGND to the PCB ground plane.
A5	LXF	Flash LED driver Inductor Connection. Connect LX to the switched side of the inductor. LX is internally connected to the drains of the internal MOSFETs. LX is high impedance in shutdown. Leave open if not used.
B5	LXF	Flash LED driver Inductor Connection. Connect LX to the switched side of the inductor. LX is internally connected to the drains of the internal MOSFETs. LX is high impedance in shutdown. Leave open if not used.
A4	OUTF	Flash LED Driver Regulator Output. Bypass OUT to PGND with a 4.7uF or larger ceramic capacitor. Leave open if not used.
B4	OUTF	Flash LED Driver Regulator Output. Bypass OUT to PGND with a 4.7uF or larger ceramic capacitor. Leave open if not used.
A3	FLED1	FLED1 Current Driver. Current flowing out of FLED1 is based on the internal I ² C registers. Connect FLED1 to the Cathode of an external Flash LED or LED Module. FLED1 is high impedance during shutdown. If not used, FLED1 may be shorted to ground.
A2	FLED2	FLED2 Current Driver. Current flowing out of FLED2 is based on the internal I ² C registers. Connect FLED2 to the Cathode of an external Flash LED or LED Module. FLED2 is high impedance during shutdown. If not used, FLED2 may be shorted to ground.
D5	COMP	Compensation Input for Flash Driver. See the <i>Compensation Network Selection</i> section in Flash LED Driver for details. COMP is pulled to GND through a 180Ω resistor in shutdown. Leave open if not used.

C6	GSMB	GSM Blank Signal for Flash LED Driver. Assertion of GSMB reduces the current regulator settings according to values programmed into the GSMB_CUR register. The status of the Flash Safety timer and the Flash/Movie mode values in the current regulator registers are not affected by GSMB assertion. Connect GSMB to the PA Module Enable signal or other suitable logic signal that indicates a GSM transmit is in process. Polarity of this signal is set by bit 7 in the GSMB_CUR register (default is active high). GSMB has internal 800kΩ pull-down resistor to AGND. Connect to GND if not used.
C5	FLED_EN	This pin controls the turn-on and turn-off of FLED1, FLED2, depending on control bits read into the I2C. See the LED_EN Control Register description for an explanation of the function of this pin. LED_EN has internal 800kΩ pull-down resistor to AGND. Connect to GND if not used.
No Connection		
A1	N.C.	Not Connected internally.
A13	N.C.	Not Connected internally.
N1	N.C.	Not Connected internally.
N13	N.C.	Not Connected internally.

7 Package Drawing



-DRAWING NOT TO SCALE-

8 Technical Description

8.1 Step-Down DC-DC Converters

BUCK1 is a high efficiency 2MHz hysteretic PWM DC-DC converter that has an adjustable output voltage from 0.65V to 2.225V in 25mV increments with Dynamic Voltage Scaling (DVS).

BUCK1 has an I²C enable bit and a hardware enable pin (PWREN). See the *Buck1 and Buck2 Enable* section for more information. BUCK1 enable is ORed by PWREN and I2C. Drive PWREN high to enable BUCK1 or drive PWREN low to disable BUCK1 (EBUCK1 in I2C register must be set to 0 in order to be controlled by PWREN). The output voltage selection is made by 3 bits of GPIOs (SET1, SET2, SET3). See the Dynamic Voltage Scaling (DVS) session. Typically PWREN, SET1, SET2, SET3 are driven by general purpose output pins of the applications processor.

BUCK2 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I²C adjustable output voltage from 0.65V to 2.225V in 25mV increments with Dynamic Voltage Scaling. BUCK2 has an I²C enable bit and a hardware enable pin (PWREN). See the *Buck1 and Buck2 Enable* section for more information.

BUCK2 enable is ORed by PWREN and I2C. Drive PWREN high to enable BUCK2 or drive PWREN low to disable BUCK2. EBUCK2 in I2C register must be set to 0 in order to be controlled by PWREN. The output voltage selection is made by 3 bits of GPIOs (SET1, SET2, SET3). See the Dynamic Voltage Scaling (DVS) session. In systems based on Samsung Application processors, PWREN, SET1, SET2, SET3 are typically connected to Application Processor's GPIO pins.

BUCK3 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I²C adjustable output voltage from 0.75V to 3.9V in 50mV increments . See the I2C Register section for details on the range of programmable output voltage.

Buck4 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I²C adjustable output voltage from 0.65V to 2.225V in 25mV increments . See the I2C Register section for details on the range of programmable output voltage.

Buck5 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I²C adjustable output voltage from 0.65V to 2.225V in 25mV increments . See the I2C Register section for details on the range of programmable output voltage.

BUCK6 is a high efficiency 3MHz PWM DC-DC converter. See the PA buck Session for details.

BUCK7 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I²C adjustable output voltage from 0.75V to 3.9V in 50mV increments . See the I2C Register section for details on the range of programmable output voltage.

8.1.1 Enable Signals

As shown in Table below, the Max8966/Max8997 feature numerous enable signals for flexibility in many applications. Backup Battery Charger can be ON/OFF by a control bit in I2C register and It remains ON as long the main BATT voltage is above UVLO and BBHOSTEN bit is set to 1. All regulators are forced off during UVLO. See the Under-voltage Lockout section for more information.

Table 1 Enable Signals

Power Domain	Enable Signal		ENABLE PIN from SAMSUNG AP
	Hardware	Software	
BUCK1	PWREN	EBUCK1	
BUCK2	PWREN	EBUCK2	GPIOs & I ² C
BUCK3	PWREN (Max8997 only)	EBUCK3	I ² C
BUCK4	N/A	EBUCK4	I ² C
BUCK5	PWREN (Max8966 only)	EBUCK5	GPIOs & I ² C
BUCK6	BUCK6EN	EBUCK6	GPIOs & I ² C
BUCK7	N/A	EBUCK7	I ² C
LDO1	PWREN	EMODE1	
LDO2	N/A	EMODE2	
LDO3	N/A	EMODE3	
LDO4	N/A	EMODE4	
LDO5	N/A	EMODE5	
LDO6	N/A	EMODE6	
LDO7	N/A	EMODE7	
LDO8	N/A	EMODE8	
LDO9	N/A	EMODE9	
LDO10	PWREN	EMODE10	GPIOs & I ² C
LDO11	N/A	EMODE11	
LDO12	N/A	EMODE12	
LDO13	N/A	EMODE13	
LDO14	N/A	EMODE14	
LDO15	N/A	EMODE15	
LDO16	N/A	EMODE16	
LDO17	N/A	EMODE17	I ² C
LDO18	N/A	EMODE18	I ² C
LDO19 (SAFEOUT1)	(4.1V<DCIN<7.5V)&&(ESAFEOUT T1=LH)	ESAFEOUT1	I ² C
LDO20 (SAFEOUT2)	(4.1V<DCIN<7.5V)&&(ESAFEOUT T2=LH)	ESAFEOUT2	I ² C
LDO21	PWREN	EMODE21	I ² C
Low Battery Monitor 1	N/A	LB1EN	I ² C
Low Battery Monitor 2	N/A	LB2EN	I ² C
Main Charger	See the Main Charger Session (Charger for 1 Cell Li+)	CHGENB	I ² C
Backup Battery Charger (VCOIN)	N/A	BBCHOSTEN	I ² C
32kHzAP	N/A	EN32kHzAP	I ² C
32kHz CP	N/A	EN32kHzCP	I ² C
VICHG	N/A	ENVICHG	I ² C

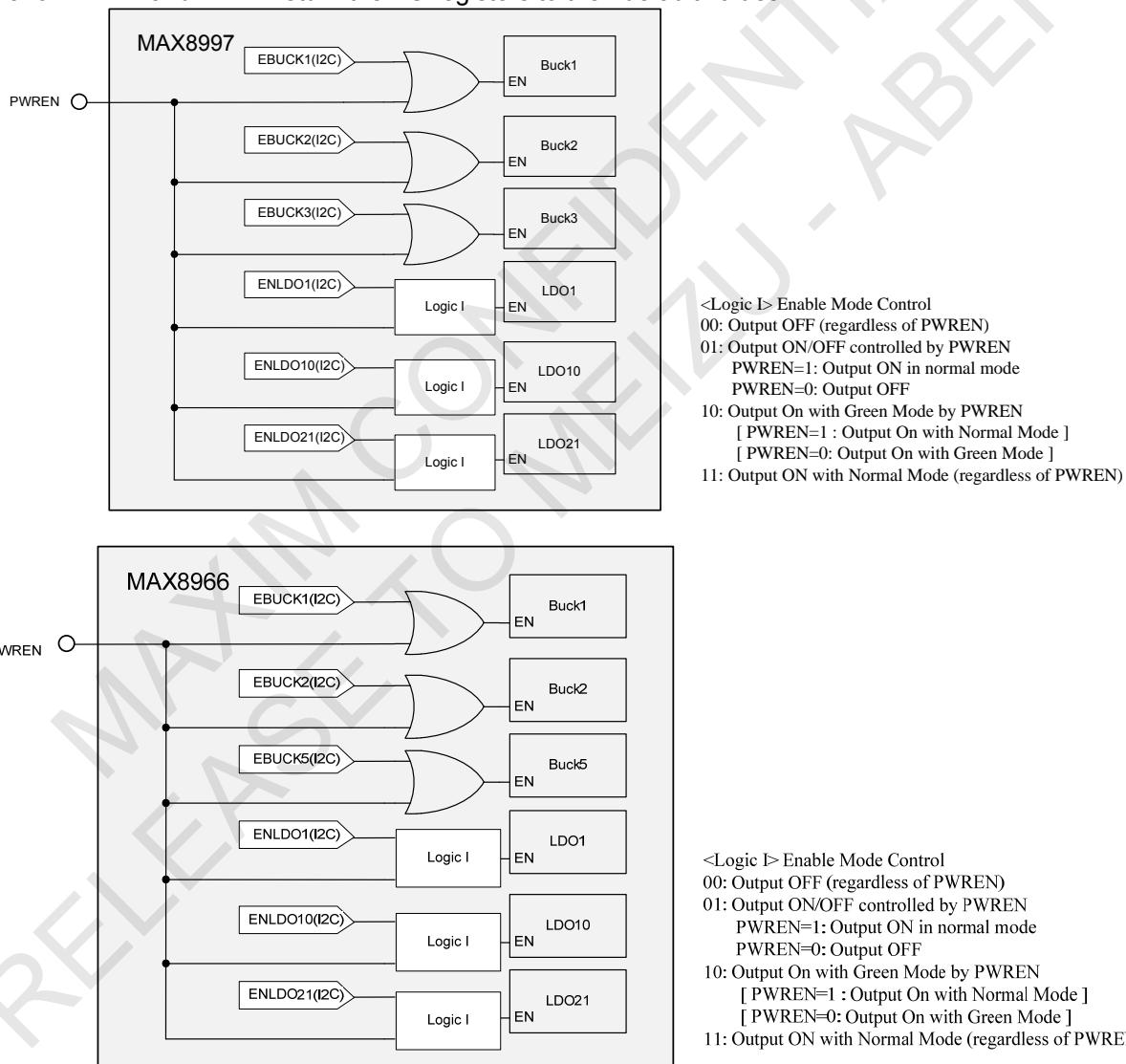
8.1.2 PWREN ENABLE SIGNALS

Buck1, Buck2, Buck3 (Max8997 only), Buck5 (for Max8966 only) have independent I²C enable bits and hardware enable pins (PWREN). Bits are logically ORed with the PWREN. The LDO1, LDO10, and LDO21 also have a control bit by PWREN. The PWREN is typically connected to Application Processor's GPIOs. Alternatively, Buck1, Buck2, Buck3 (Max8997 only) and Buck5 (Max8966 only) may be activated via the I²C interface. Note that to achieve a pure I²C enable/disable, drive hardware pins (PWREN) to ground for Buck converter. Similarly, to achieve a pure hardware enable/disable for Buck converters, leave the I²C enable bits at their OFF value (EBUCK_ = 0). Please note that the default registers are EBUCK_ = ON .

LDO1, LDO10, and LDO21 have four enable options depending upon PWREN. See the I²C register for detail. LDO1, LDO10, and LDO21 and also is able to enter Low Power Mode.

For the rest of LDOs, PWREN is able to make LDOs enter Low Power Mode.

Note: a low /MR1\ and /MR2\ return the I²C registers to their default values



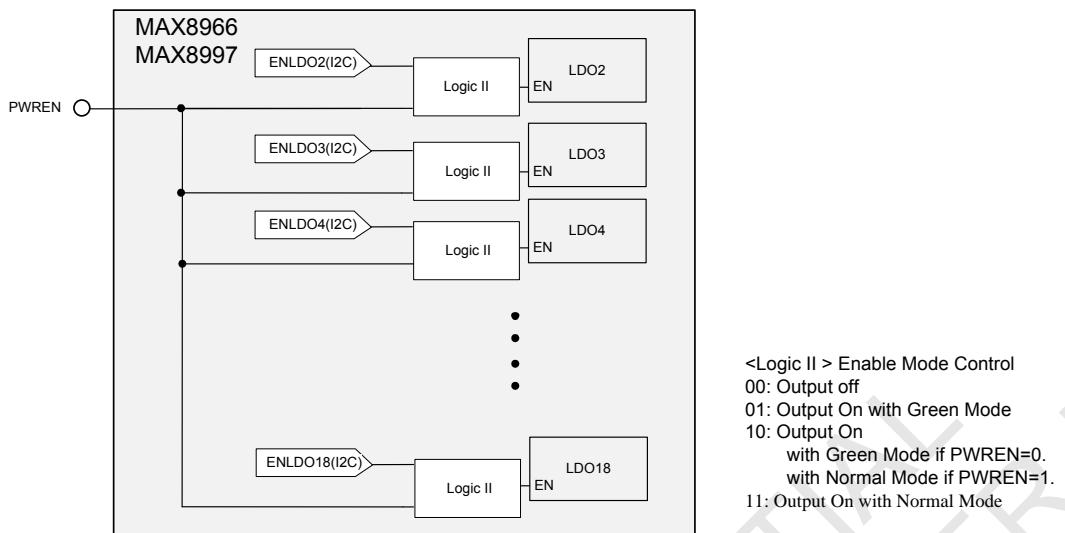


Figure 4 Enable Block Diagram

Error! Reference source not found. shows timing sequence when PWREN is asserted. The regulators are enabled or disabled by PWREN. There is 10use time delay between each regulator's turn on

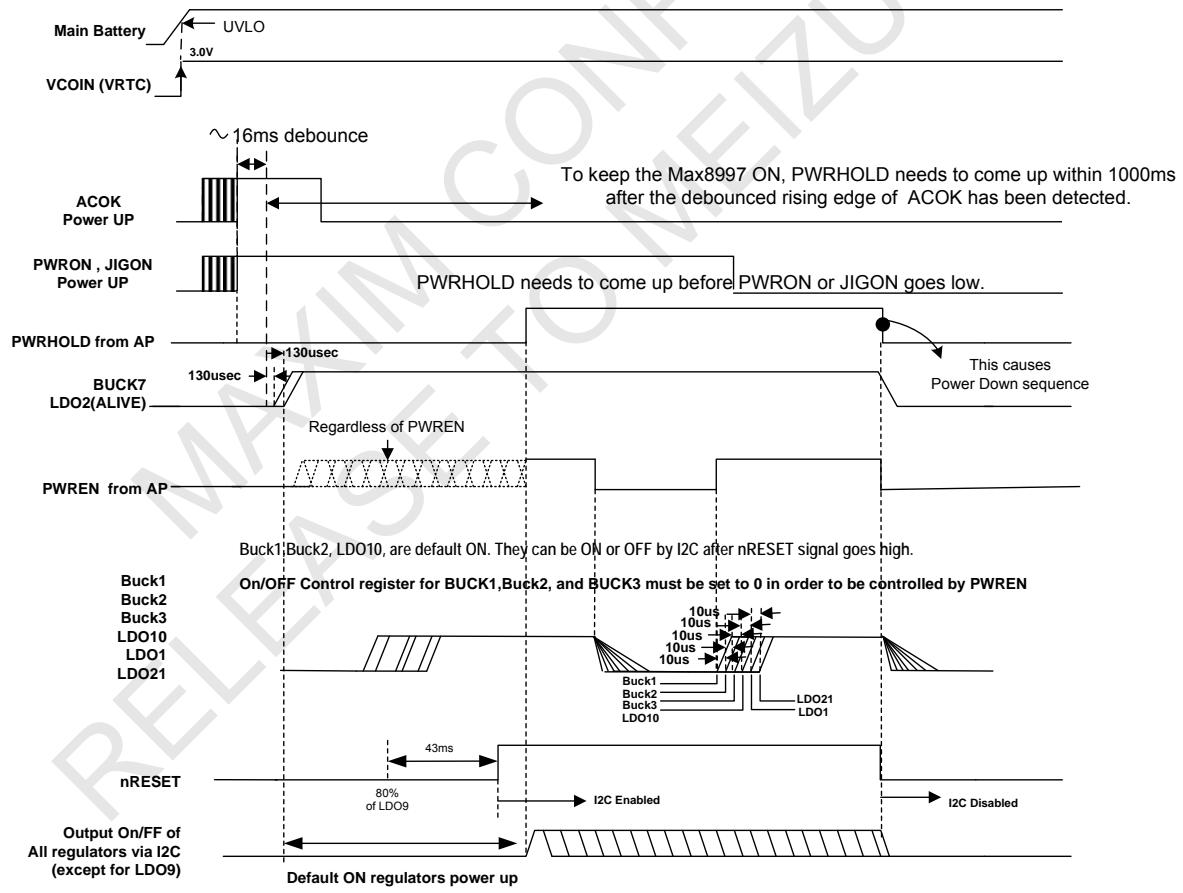


Figure 5 MAX8997 Timing Diagram of regulator ON/OFF controlled by PWREN

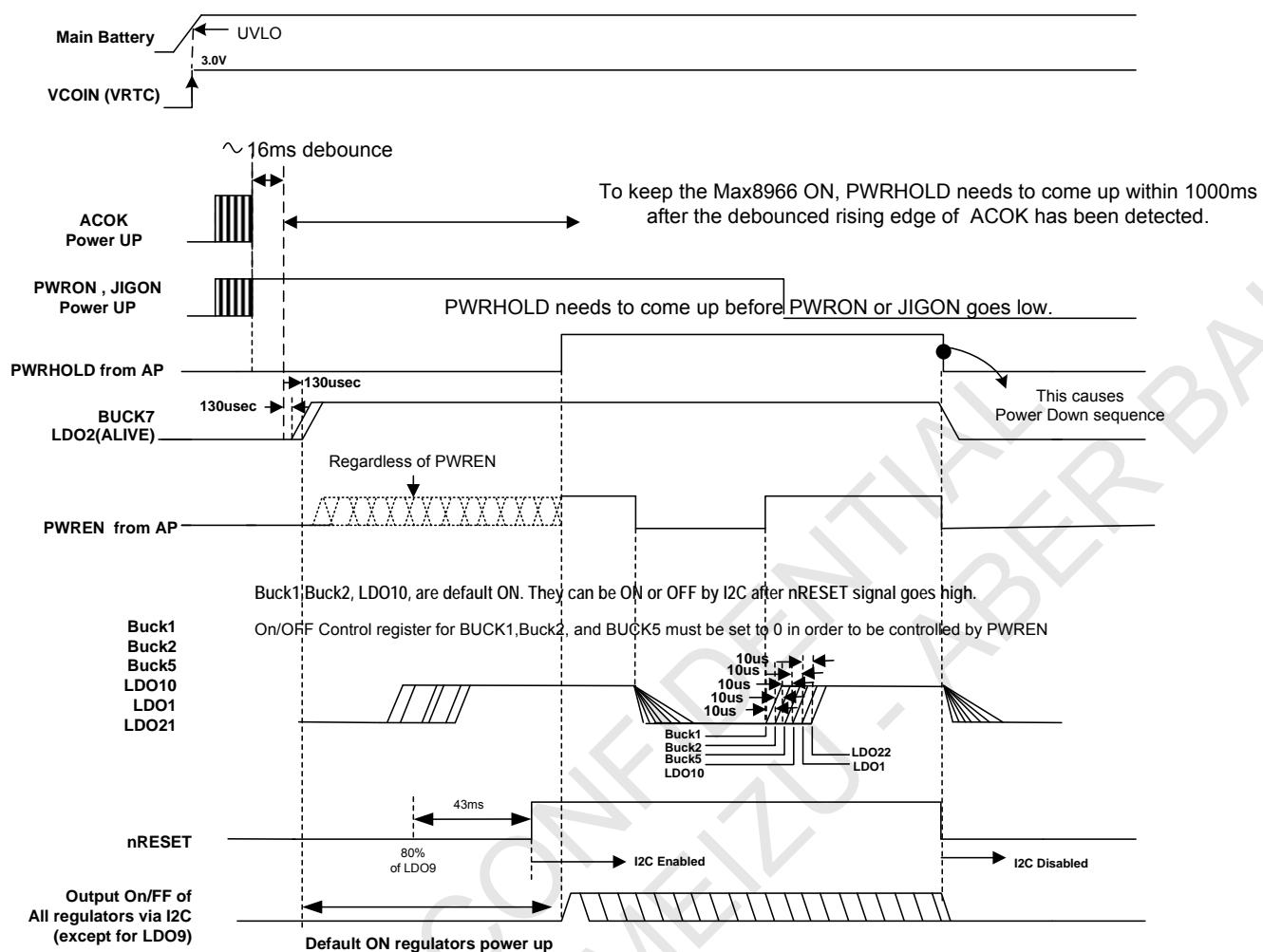


Figure 6 MAX8966 Timing Diagram of regulator ON/OFF controlled by PWREN

8.1.3 Dynamic Voltage Scaling (DVS) Modes

8.1.4 DVS Operations for Buck1, Buck2 and Buck5

In normal operation, the BUCK1, Buck2, and Buck5 output voltages are dynamically adjusted by the logic level inputs of SET1, SET2 and SET3. There are eight registers assigned respectively for Buck1 target voltage(B1_TV), Buck2 target voltage(B2_TV), Buck5 target voltage (B5_TV). The output voltages for Buck1, Buck2, and Buck5 are chosen by the SET1, SET2 and SET3.

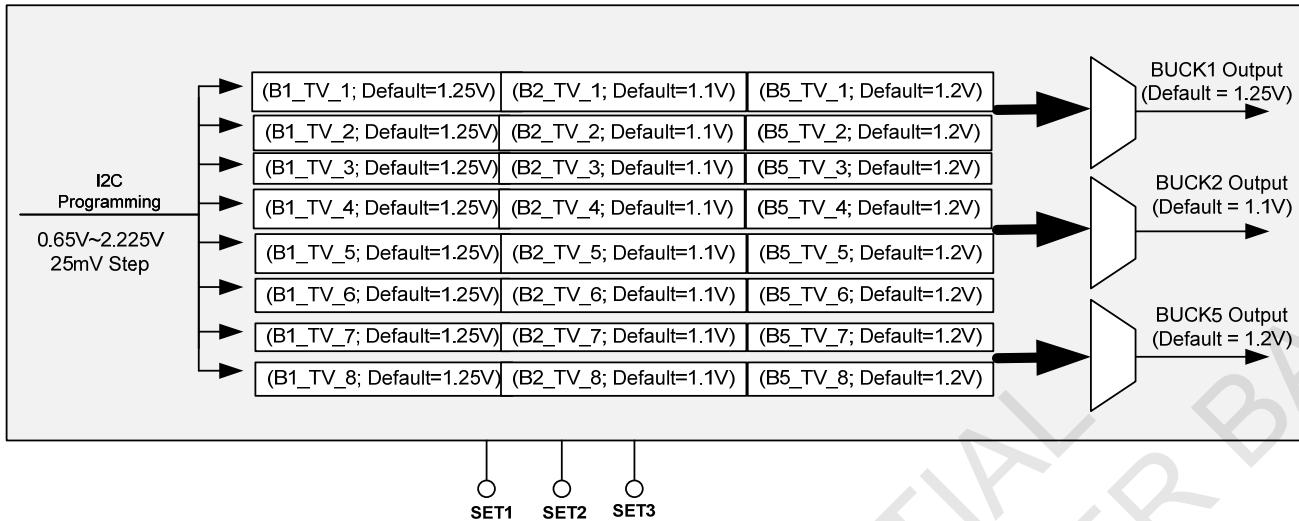


Figure 7. MAX8997 Dynamic Voltage Scaling for Buck1, Buck2, and Buck5

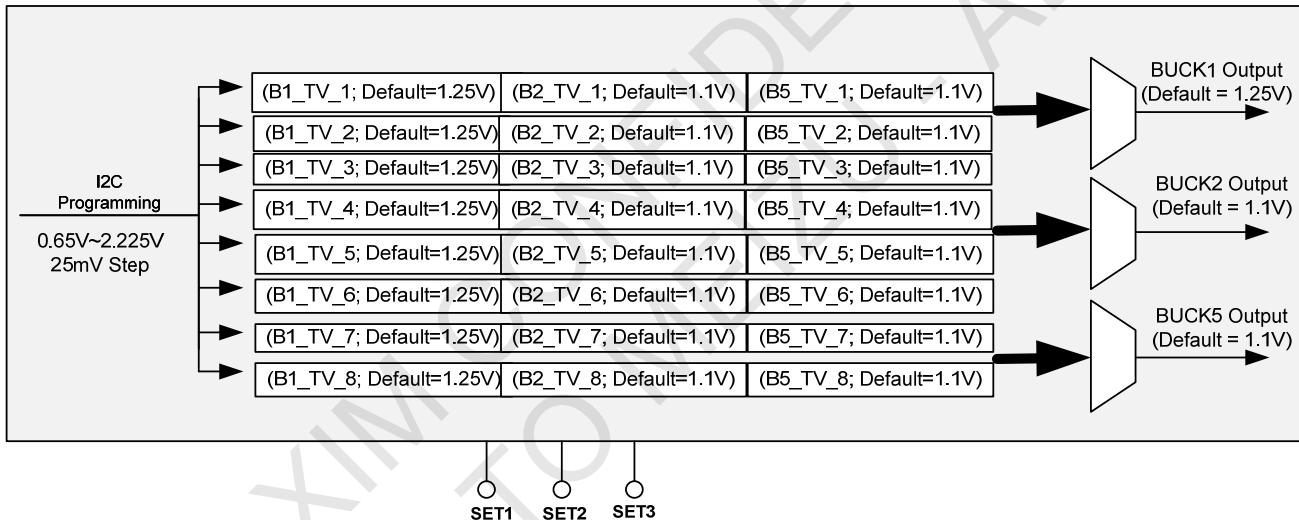


Figure 8 MAX8966 Dynamic Voltage Scaling for Buck1, Buck2, and Buck5

Table 2. SET1, SET2, SET3 and BUCK1, Buck2, Buck5 Truth Table

SET3	SET2	SET1	BUCK1	BUCK2	BUCK5
0	0	0	B1_TV_1	B2_TV_1	B5_TV_1
0	0	1	B1_TV_2	B2_TV_2	B5_TV_2
0	1	0	B1_TV_3	B2_TV_3	B5_TV_3
0	1	1	B1_TV_4	B2_TV_4	B5_TV_4
1	0	0	B1_TV_5	B2_TV_5	B5_TV_5
1	0	1	B1_TV_6	B2_TV_6	B5_TV_6
1	1	0	B1_TV_7	B2_TV_7	B5_TV_7
1	1	1	B1_TV_8	B2_TV_8	B5_TV_8

8.1.5 Buck1, Buck2, Buck4, Buck5 DVS Control with Ramp Rate (RAMP)

The output voltages of Buck1, Buck2, Buck4, Buck5 have a variable ramp rate that is set by a register (RAMP). This register controls the output voltage ramp rate during a positive voltage-change (i.e. 1.0V to 1.1V), and a

negative voltage-change (i.e. 1.1V to 1.0V). When a Buck Converter is disabled, the output voltage decays at a rate determined by the output capacitance, internal discharge resistance, and the external load.

In normal mode operation, the regulator output voltage ramps up/down at the rate set by RAMP. With small loads the regulator must sink current from the output capacitor to actively ramp down the output voltage. The regulator output voltage ramps down at the rate determined by the output capacitance and the external load; small loads result in an output voltage decay that is slower than that specified by RAMP, large loads ($> C_{OUT} \cdot RAMPRATE$) result in an output voltage decay that is no faster than that specified by RAMP.

Ramp Rate adjustment range is 1mV/us ~100mV/us.

BUCK1~BUCK5 and LDO1 ~ LDO18 have a fixed soft-start ramp that eliminates input current spikes when they are enabled.

8.1.6 DVSOK Interrupt

In order to reduce power loss in the Application Processor, the DVSOK interrupt signal is generated in the DVS Mode. If the processor gets this interrupt signal, it means that the regulator output reaches the target voltage.

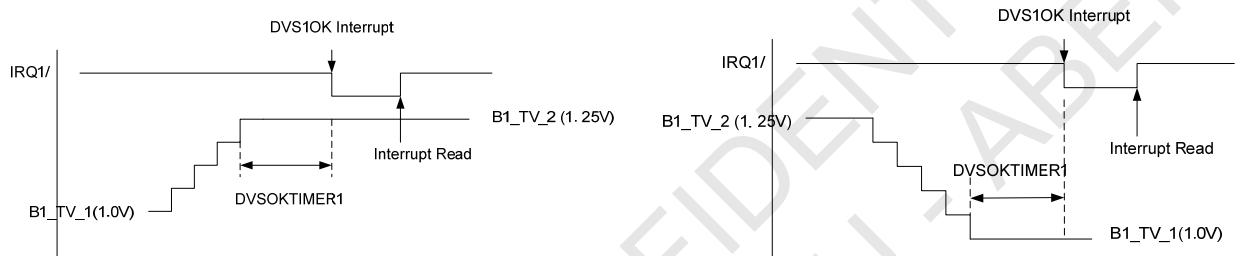


Figure 9 DVSOK interrupt example (Buck1 output voltage change)

8.1.7 BUCK6 (PA BUCK)

The PA DC/DC step-down converter is optimized for powering the RF power amplifier. The device integrates a high-efficiency PWM step-down converter for medium and low-power transmission, with a 60mOhm typical bypass regulator, in parallel with the step-down converter (providing a total bypass impedance of 45mΩ bypass impedance with a 65mΩ inductor), enabling high power transmission and fast output voltage transitions.

The DC-DC step down converter is a 3MHz, synchronous-rectified, step-down converter that delivers a guaranteed 1200mA for an output reference voltages range of 0.17V to 1.7V. The DC-DC step down converter utilizes a 3MHz control scheme with internal compensation, allowing for tiny external components and a fast transient response with exceptional load regulation. At light loads, the DC-DC step down converter automatically switches to an ultra-high efficiency pulse-skipping mode to minimize quiescent current and to maximize efficiency. The DC-DC step down converter automatically transitions to a fixed-frequency mode under moderate to heavy loading.

FET scaling reduces the quiescent current under light load conditions by disabling a fraction of the internal switches, so that the total gate capacitance of the internal switches is reduced. The PA DC/DC scales the FETs for three different ranges of operation, ensuring that efficiency is maximized for low, medium and high power transmission.

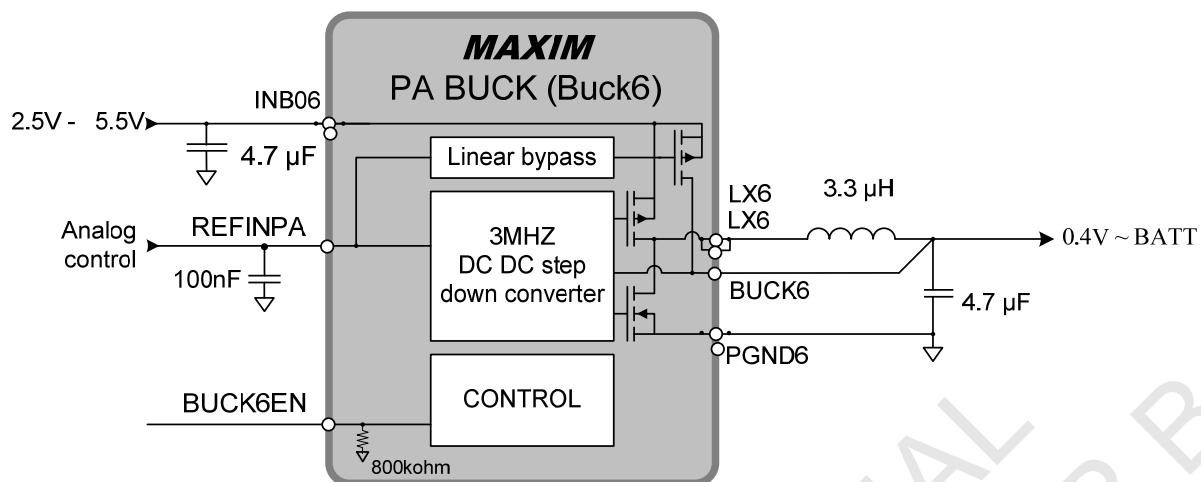


Figure 10 Typical Application Circuit of PA Buck (Buck6)

8.1.7.1 CONTROL SCHEME

Under light load conditions, the Dc-DC step down converter operates as a hysteretic converter in which the output ripple determines when switching cycles begin and end. The high side switch turns on until the inductor current reaches the skip current level, at which time the high side switch turns off, and the low side synchronous rectifier turns on. The inductor current ramps down until the zero cross threshold is reached, at which time the low side rectifier turns off. This repeats until the error amplifier has detected an output voltage at or beyond the hysteresis window. A fraction of the high and low side switches are used, so that gate capacitance is reduced, thus reducing the quiescent current consumption under light loads.

As the load current increases, the inductor current increases so that a zero-cross is no longer detected. As this occurs, the full switches are connected to maximize efficiency, and the converter transitions into a fixed frequency mode of operation with the assistance of a phase-locked loop fixed-frequency circuit which helps maintain a constant frequency. The typical switching frequency is 3MHz when the inductor current is continuous.

In most hysteretic converters, the DCR of the inductor is the primary factor in determining the load regulation. The DC-DC step down converter error amplifier compensates for the DCR of the inductor, thus significantly improving the load regulation.

8.1.7.2 Internal Synchronous Rectification

While in PWM mode, the DC-DC step down converter uses an internal low side switch as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode. Conduction time of the synchronous-rectifier body diode has been minimized, to reduced the efficiency drop caused by the body-diode conduction.

8.1.7.3 Current Limiting

A peak inductor current limit protects power switches and the input source during either overload conditions or short circuit conditions. If the output is shorted to ground the device enters a timed current limit mode where the low side switch is turned on for a longer duration until the inductor current falls below a low threshold. This allows the inductor current more time to decay.

8.1.7.4 PFM OPERATION

If the load current decreases, the converter will enter hysteretic mode operation automatically. During hysteretic mode, the converter skips switching and operates with reduced frequency and with minimum quiescent current to maintain high efficiency. The transition from PWM to hysteretic mode occurs once the inductor current in the Low-Side switch becomes zero, which indicates DCM (Discontinuous Conduction Mode).

8.1.7.5 SWITCHING FREQUENCY

The DC-DC step down converter operates in a hysteretic mode at light loads to maximize efficiency. As the load increases to moderate to heavy loads, the DC-DC step down converter operates in a hysteretic PWM

mode. In the hysteretic PWM mode, the switching frequency is fixed at 3MHz with the assistance of a fixed-frequency correction circuit phase-locked loop, which helps maintain a constant switching frequency, over changing line and load conditions.

8.1.7.6 100% DUTY-CYCLE OPERATION

The DC-DC step down converter allows operation with a low input-to-output voltage difference by operating at 100% duty cycle. In this state, the high side switch is always on and at the same time as the bypass LDO is enabled to provide the lowest possible dropout voltage.

8.1.7.7 Linear BYPASS regulation

The linear regulator is placed in parallel with the DC-DC step down converter. The purpose of the linear regulator is to extend the bandwidth of the DC-DC step down converter as well as provide lowest possible dropout condition when input is approaching the output voltage.

The linear regulator is set to have a regulation somewhat lower than the DC-DC step down converter, this is done to insure that the linear regulator is only supplementing the output in cases where the switch mode converter is no longer able to provide sufficient energy to the output.

The cases where the DC-DC step down converter is not able to provide sufficient energy to the output are:

- 1: Output is slewed faster than the bandwidth of the DC-Dc converter
- 2: Load current higher than the current limit for the converter
- 3: Insufficiency voltage headroom for the DC-DC converter

8.1.7.8 SOFT-START / SHUTDOWN MODE

The DC-DC step down converter in PA DC/DC has a soft-start circuit that limits in-rush current during start-up. Soft start is activated only if BUCK6EN goes from logic low to logic high after INB06 exceeds the UVLO threshold. The typical start-up time with 2.2 μ F output capacitor and 0mA load is 20 μ s.

Connecting BUCK6EN to logic low places the PA DC/DC in shutdown mode and reduces supply current. In shutdown, the control circuitry and internal high and low side switches turn off and an active discharge resistance of LX is enabled. Connect BUCK6EN to logic high for normal operation.

8.1.7.9 Power up timing

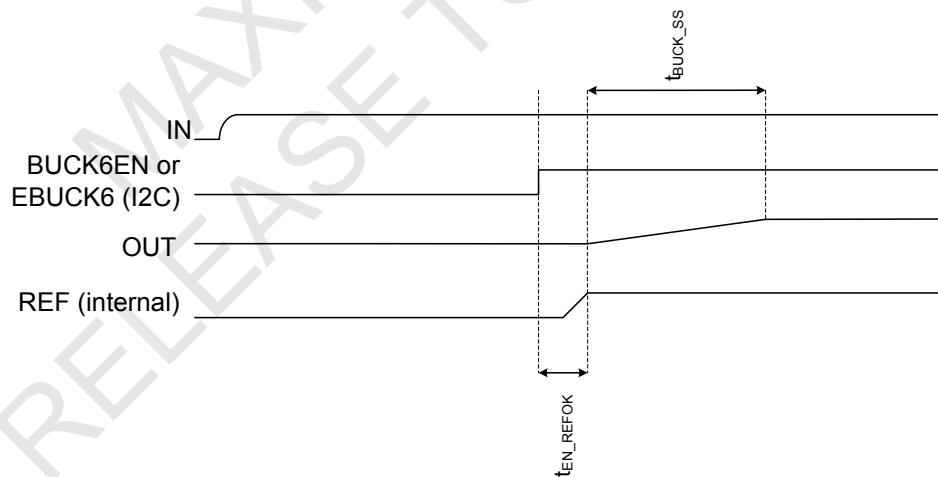


Figure 11 Power up timing diagram

8.1.7.10 Shutdown mode

Connect BUCK6EN to logic-low to place the step-down converter in shutdown mode. In shutdown, the control circuitry, internal high and low side switches turn off and LX becomes 1kohm (active discharge resistance). Connect BUCK6EN logic-high for normal operation.

8.1.7.11 Fixed-Frequency CircuitPhase Locked Loop

When the inductor current is in continuous conduction, a fixed-frequency correction circuit phase-locked loop helps maintain a constant switching frequency, unlike in a typical hysteretic control scheme, in which the switching frequency may vary significantly both with load and line variation. The fixed-frequency circuit phase-locked loop is only enabled when the inductor current is continuous; otherwise, it is disabled to minimize quiescent current consumption.

8.1.7.12 Regular Buck operation application

Buck6 may be used for a regular buck operation. The figure below shows a typical application circuit by using a LDO output. Any LDO can be used for the REFINPA. A 100nF bypass capacitor should be placed on REFINPA pin for this application.

The output voltage is given by

$$\text{BUCK6 output} = (2.5 \text{ or } 3) \times \text{REFINPA}$$

Where REFINPA is a programmable LDO output.

Figure below shows another typical application circuit by using a resistor divider. The output voltage is given by

$$\text{Buck6 output} = (R_b) * \text{LDO9_OutputV} / (R_a + R_b)$$

A 100nF bypass capacitor must be placed on REFINPA pin for this application.

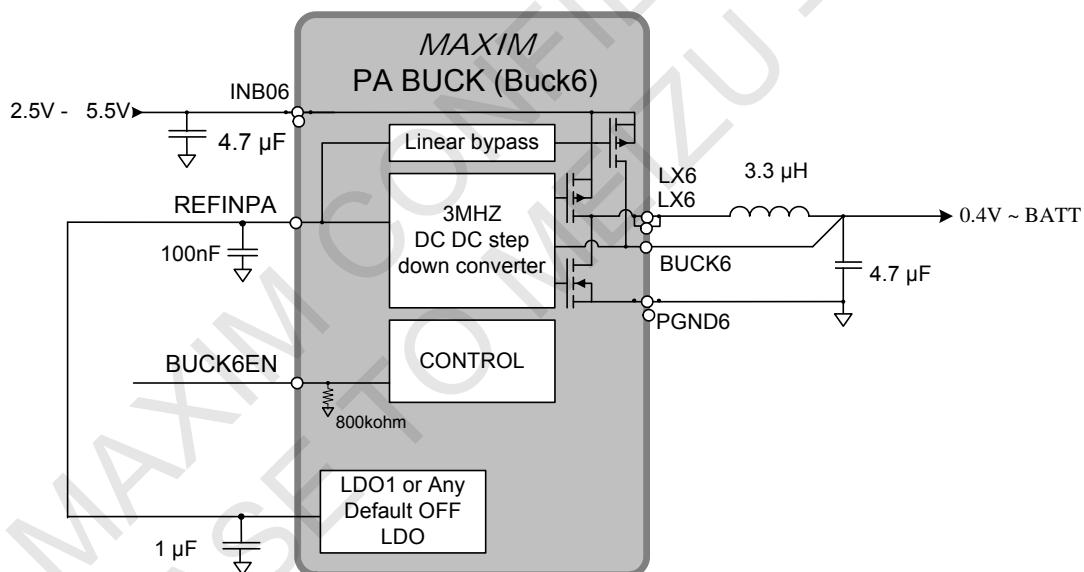


Figure 12 Typical application circuit for a regular buck operation – case 1

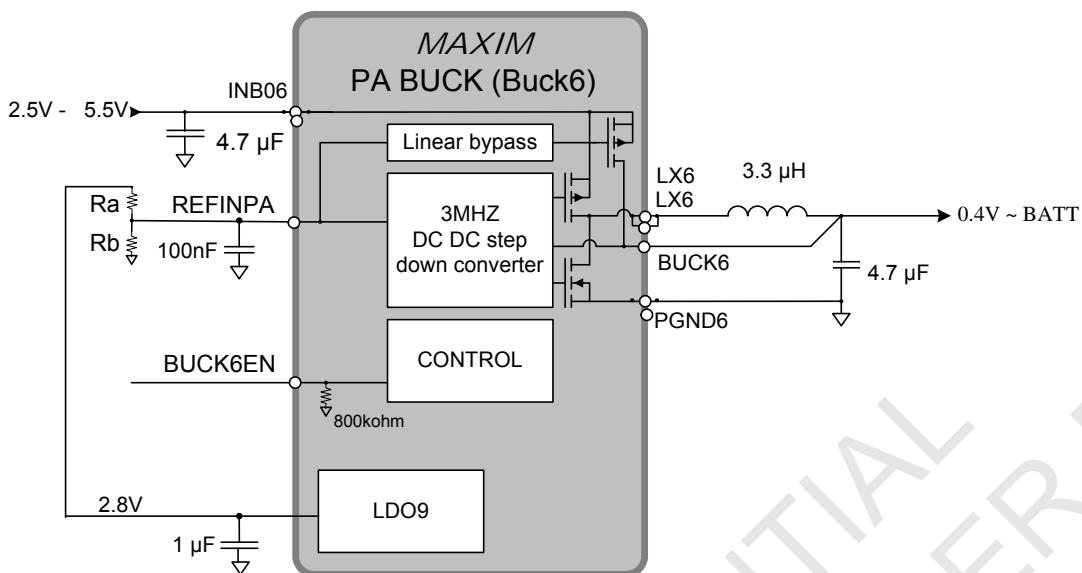


Figure 13 Typical application circuit for a regular buck operation – case 2

8.1.7.13 THERMAL SHUTDOWN

As soon as the junction temperature of the PA DC/DC exceeds +160°C, the IC goes into thermal shutdown. In this mode the internal p-channel switch and the internal n-channel synchronous rectifier are turned off. The device restarts normal operation when the junction temperature falls below 140°C.

8.1.7.14 Inductor selection

The DC-DC step-down converter operates with a switching frequency of 3MHz and utilizes a 1uH or 3.3μH inductor. The tradeoff is efficiency and size of the external inductor. Choosing a larger inductance value reduces the inductor ripple current. This means that during light load operation it also reduces the negative inductor current, hence increasing the efficiency of the converter.

The inductor's DC current rating only needs to match the maximum load of the application because the step-down converter features zero current overshoot during startup and load transients. For optimum transient response and high efficiency, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range.

8.1.7.15 Input capacitor Selection

The input capacitor reduces the current peaks drawn from the battery or input power source and reduces switching noise in the PA DC/DC. The impedance of the input capacitor at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. A 4.7μF capacitor is sufficient for the input capacitor to keep the DC-DC step down converter stable. For optimum noise immunity and low input ripple, the input capacitor value can be increased. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided.

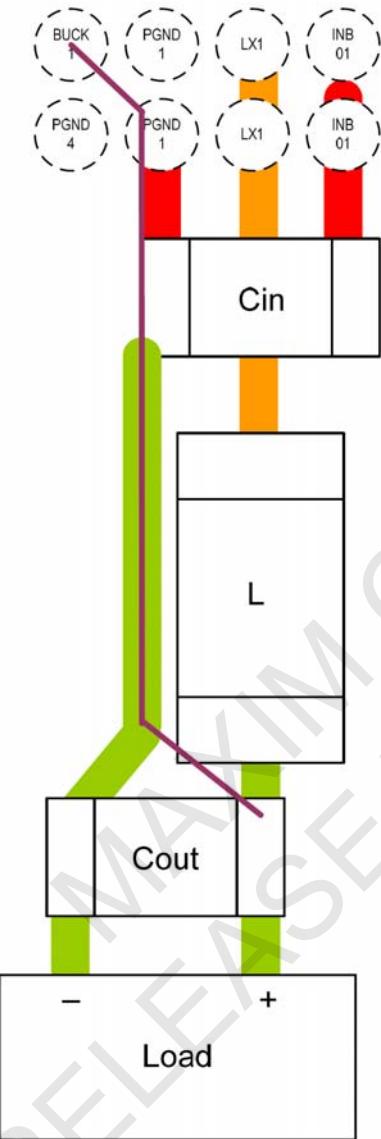
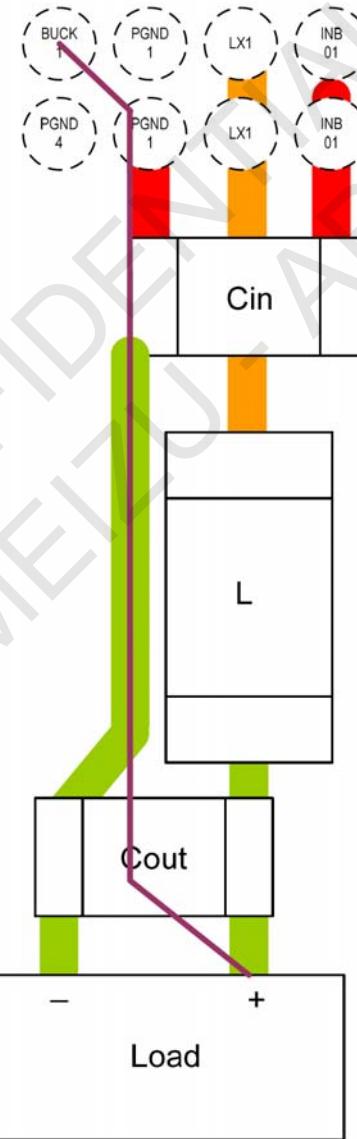
8.1.7.16 Output capacitor Selection

The output capacitor keeps the output voltage ripple small and ensures regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. A 4.7μF capacitor is sufficient for the DC-DC converter loop stability. For optimum load-transient performance and very low output ripple, the output capacitor value can be increased. Larger value output capacitors further reduce output noise and improve load-transient response, stability, and power-supply rejection. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided. These regulators are optimized for ceramic capacitors. Tantalum capacitors are not recommended.

8.1.8 Buck Converter Layout Guide

The most noisy source of buck converter is the loop between input (INB0_) and Power Ground (PGND_). The input capacitor plays very important role to reduce the switching noises. A ceramic capacitor is recommended for the input capacitor. Place the input capacitor closer to Max8966/Max8997 to minimize the current loop between PMIC and the input capacitor.

Buck Layout Guideline

Buck1, Buck3
Layout Guideline

8.2 Backup Battery Charger ; Always On

The Backup battery charger remains ON as long the main BATT voltage is above UVLO and BBHOSTEN bit is set to 1. This charger turns off if main battery voltage is below UVLO or VBATT<VCOIN. The backup battery charger is a voltage limited current source with a default $1\text{k}\Omega$ output resistor. Backup Charger has an I²C adjustable output voltage in 2.5V, 3.0V, 3.3V, or 3.5V. The default output voltage is 3.0V. The power up default is ON. See the register section for details on how to adjust the output voltage.

The charging current depends on the PMIC ON or OFF. Max8966/Max8997's back up battery charger has two mode's charging current.

PMIC ON; coin cell charging current is 67uA (= 100uA-33uA)
 PMIC OFF; coin cell charging current is 96.7uA (= 100uA-3.3uA)

Where

33uA is the supply current for the low Jitter of 32kHz clock during PMIC ON
 3.3uA is the supply current for the high jitter of 32kHz clock during PMIC OFF
 100uA is a charging current. 100uA is a default value.

Thus, the actual charging current of back up battery is either 67uA or 96.7uA depending up PMIC ON/OFF status. The charging current is programmable over I²C ranging from 80 to 800uA.

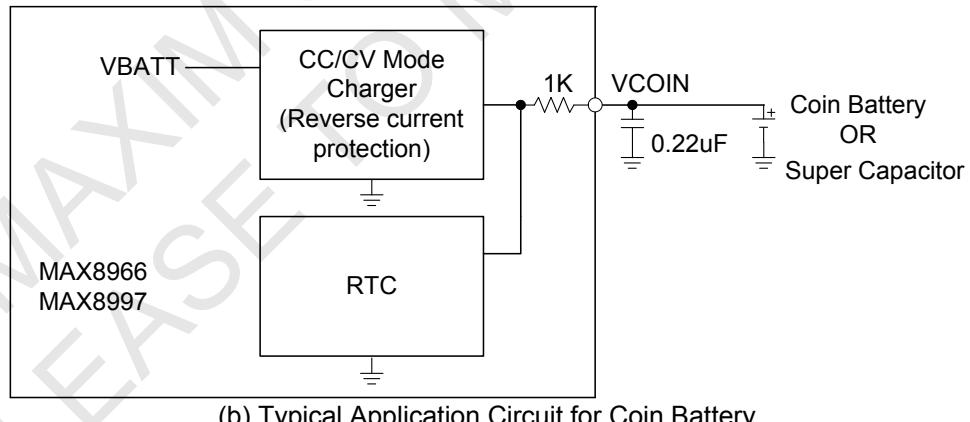
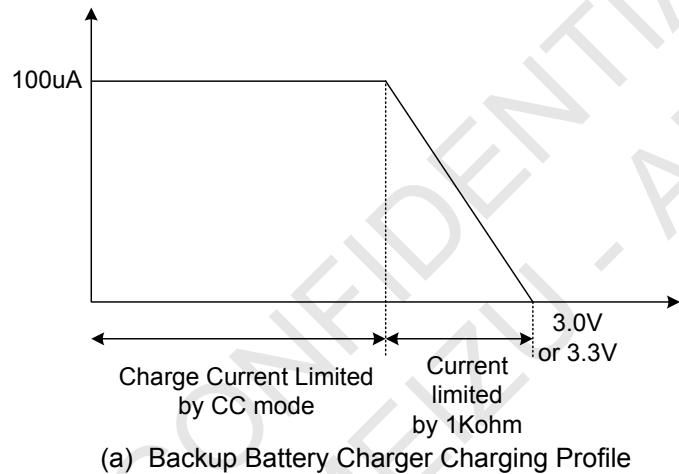


Figure Backup Battery

8.3 I²C Functional Description

The MAX8966/MAX8997 acts as a Slave Transmitter/Receiver. The MAX8966/MAX8997 has the following slave address.

Slave Address:

1. PMIC(Bucks, LDOs, Main Charger, Backup Battery Charger, Flash LED Driver, GPIOs,); 0xCCh/0xCDh
2. RTC; 0x0C/0x0D
3. MUIC; 0x4A/0x4B
4. Haptic Motor Driver; 0x90/0x91
5. Fuel Gauge; 0x6C/0x6D (See the Fuel Gauge I2C Protocol for details in Fuel Gauge sessions.)

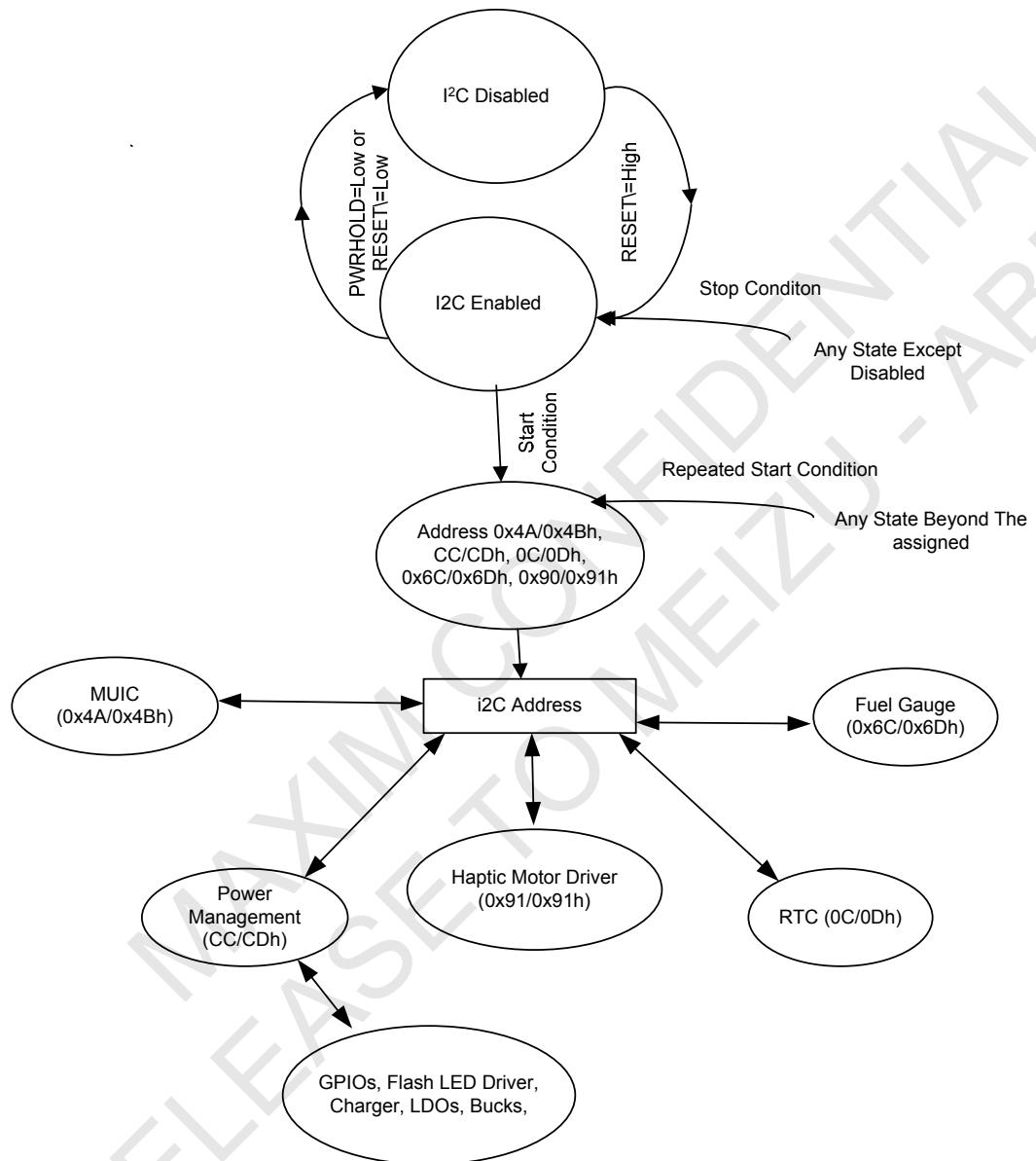
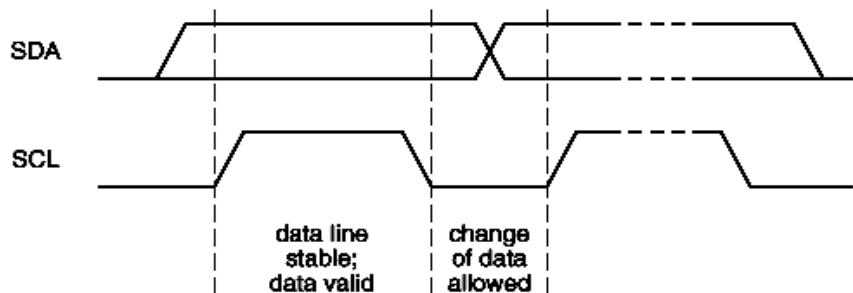


Figure 14 I2C slave address structure

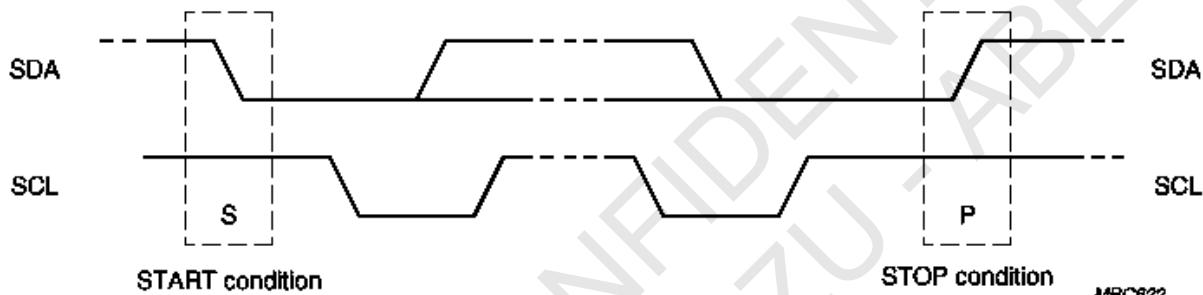
8.3.1 I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on I2CDATA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.



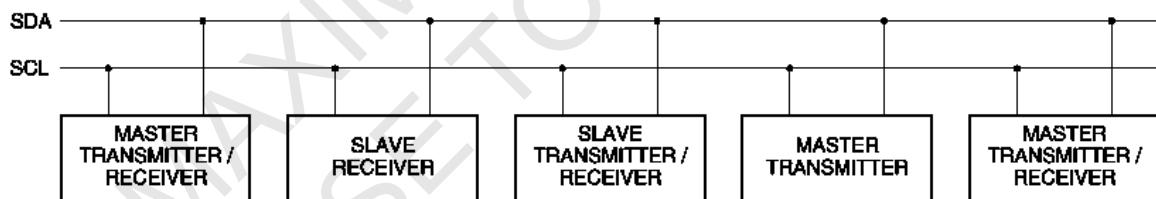
8.3.2 I²C Start And Stop Conditions

Both I2CDATA and I2CCLK remain High when the bus is not busy. A high-to-low transition of I2CDATA, while I2CCLK is high is defined as the Start (S) condition. A low-to-high transition of the data line while I2CCLK is high is defined as the Stop (P) condition.



8.3.3 I²C System Configuration

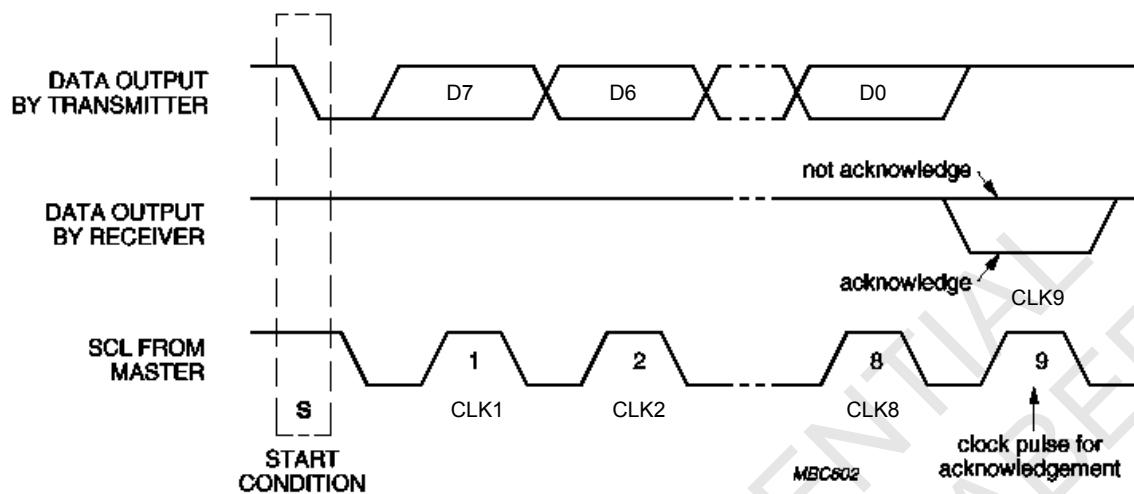
A device on the I²C Bus who generates a "message" is called a "Transmitter" and a device who receives the message is a "Receiver". The device that controls the message is the "Master" and the devices that are controlled by the "Master" are called "Slaves".



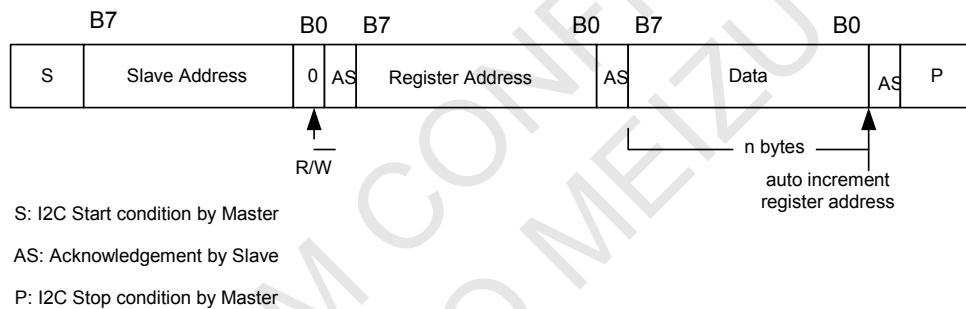
8.3.3.1 I²C Acknowledge

The number of data bytes between the start and stop conditions for the Transmitter and Receiver are unlimited. Each 8-bit byte is followed by an Acknowledge Bit. The Acknowledge Bit is a high level signal put on I2CDATA by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after each byte it receives. Also a master receiver must generate an Acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that Acknowledges must pull down the I2CDATA line during the acknowledge clock pulse, so that the I2CDATA line is stable low during the high period of the Acknowledge clock pulse (set-up and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave I2CDATA high to enable the master to generate a stop condition.



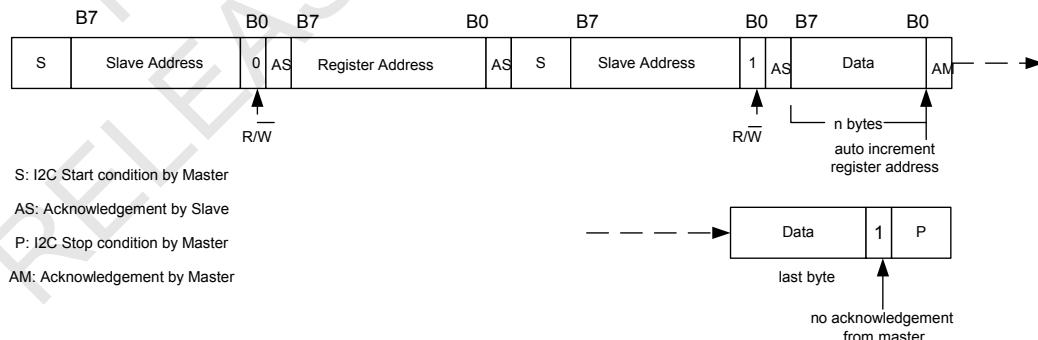
8.3.3.2 Mater transmits (Write Mode)



When master writes to slave, we use the following format.

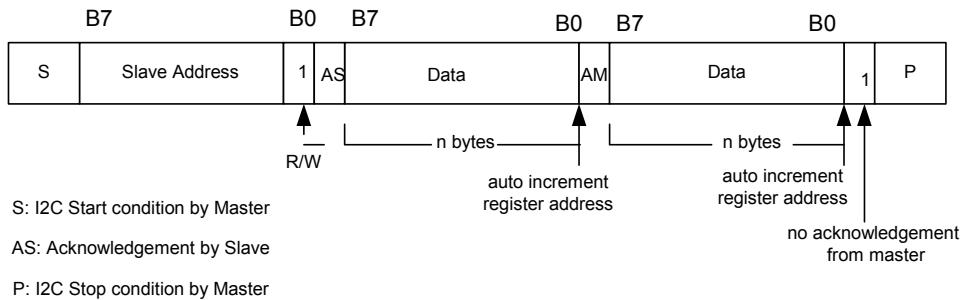
8.3.4 Master reads after setting register address (Write Register Address and Read data)

When we need to read a specific register, we use the following format.



8.3.5 Master reads register data without setting register address (Read mode)

When we read registers from first address, we can use the following format.



8.4 Power Sequencing

8.4.1 Power On/OFF

The power management circuit is able to handle all issues regarding power on/off the handset. The following determines the power on/off status of the Max8966/Max8997.

PWRON

JIGON

Factory cable detected (JIG)

PWRHOLD

DCIN

SMPL

WTSR

RTC ALARM

MR1/ and MR2/

Logic high on PWRON pin is the normal way of powering up a Max8966/Max8997. The PWRON signal is held high; default power supplies are turned on. When LDO9 reaches 90% of its final value, a 60 ms reset timer is started. The 43ms reset timer allows the AP chipset to fully reset. At the completion of the 43ms reset timer, RSO\ is allowed to rise (provided no other circuit pulls low on this WIRED-OR output). After RSO\ is asserted high; now the AP processor is initialized and will asserts PWRHOLD high. PWRHOLD maintains the power on. This allows the PWRON key to be released (return to low state) and the power remains on. If, however, PWRON is released before the PWRHOLD signal is asserted then the default power supplies are turned off. The default power supplies can be turned off by the AP processor asserting PWRHOLD low. PWRHOLD signal can also be controlled by setting EPWRHOLD bit in the I2C register.

Attaching an USB cable to DCIN can also power on the handset as long as battery voltage is greater than $3.1V_{typ}$, and the VDCIN is greater than 4.0V and less than 7.5V, and $VDCIN - VBATT >= 250mV$. When the VDCIN is greater than 4.0V and less than 7.5V, DCINOK signal is generated. The delay between the detection of valid VDCIN and the assertion of DCINOK depends whether the MAX8966/MAX8997 is configured to be USB2.0 compliant or not. The details are described in the MUIC and Main Charger technical description sessions. Connecting hands free or external power can also turn on the phone as long as JIGON input goes high if JIGON remains valid for the duration of the 16ms debounce filter.

Once the phone is powered on, MAX8966/MAX8997 can only be directly powered off when the PWRHOLD=ACOK=Low and PWRON=JIGON=low or when LDO9 falls below 80% due to overload.

If LDO9 above 90% and PWRHOLD is high and I²C is activated:

1. All LDOs and all DC-DC converters (except LDO9) can be turned on and off.
2. BUCK1, BUCK2, BUCK5(or Buck3) can be turned on and off by using I²C under the condition of (PWREN= 0).

8.4.2 ALARM INTERRUPT

An Alarm interrupt (Alarm1 or Alarm2) from the RTC also turns on the default power supplies when the phone is off. nIRQ1 interrupt pin is asserted when Alarm interrupt event occurs.

8.4.3 SMPL (Sudden Momentary Power Loss) POWER ON

SMPL (Sudden Momentary Power Loss) event could also turns on the default power supplies when the phone is off. The detailed functions are described as below:

SMPL circuits run off coin battery. It's register bit is default 0. If SMPL bit is 1, BATT UVLO falling (power loss) will start SMPL one-shot timer (default is 0.5s). If BATT UVLO rising is detected before the SMPL timer is expired, MAX8966/MAX8997 will be turned on and an interrupt will be sent. If BATT UVLO rising is detected after the SMPL timer is expired, MAX8966/MAX8997 will remain off. If SMPL bit is 0, this detection is disabled.

8.4.4 WTSR (Watchdog Timeout and Software Resets)

WTSR (Watchdog Timeout and Software Resets) event would keep the chip on and reset the chip to default power supplies. WTSR is powered from coin battery as SMPL. It is default 0. If WTSR is set to 1, PMIC will be kept on and PWRHOLD falling edge will pull RSO\ low and will trigger a 43ms timer. After 43ms timer expires, RSO\ is released high and an interrupt will be sent.

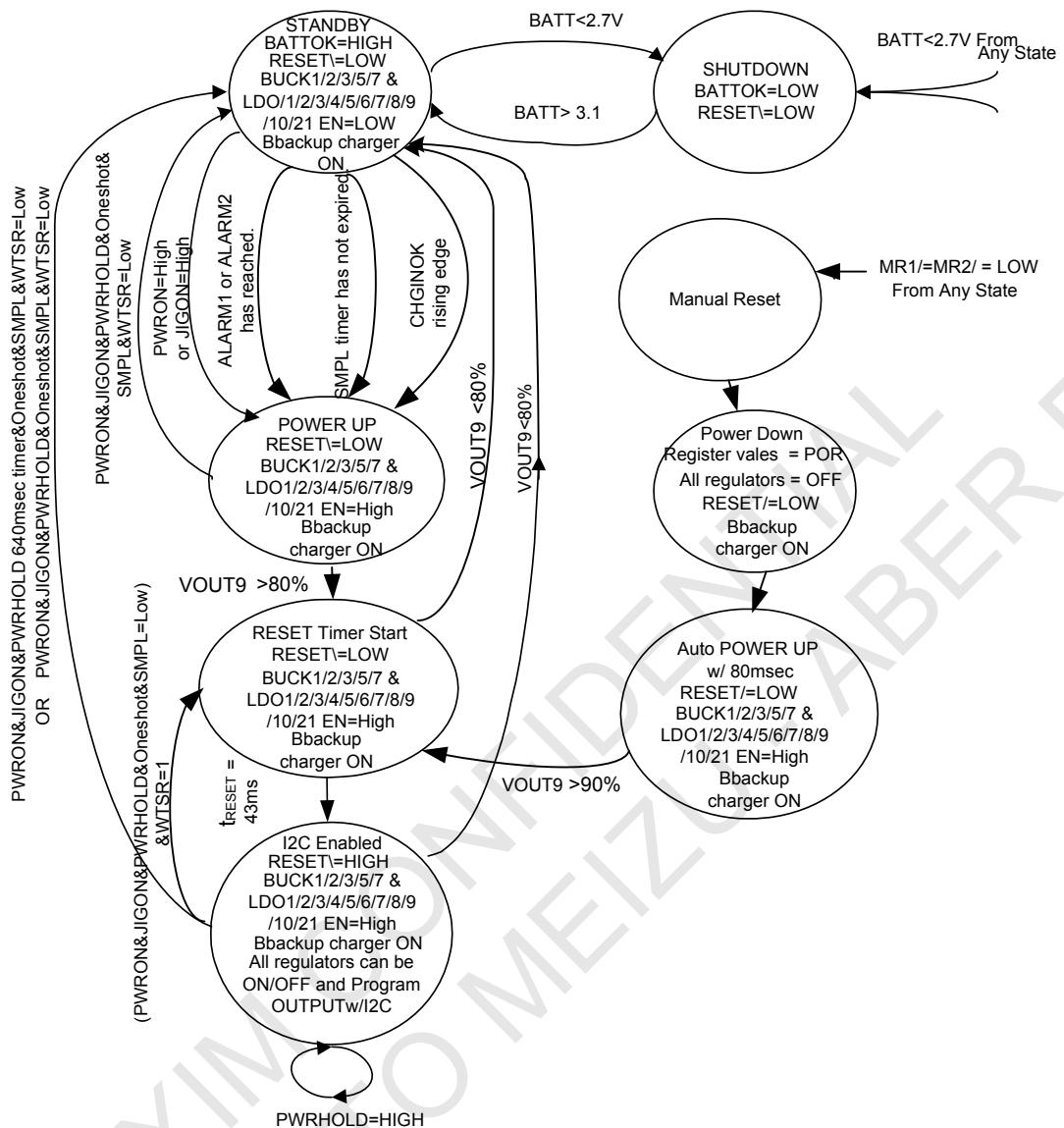


Figure 15 Power ON/OFF Control State Diagram of MAX8997

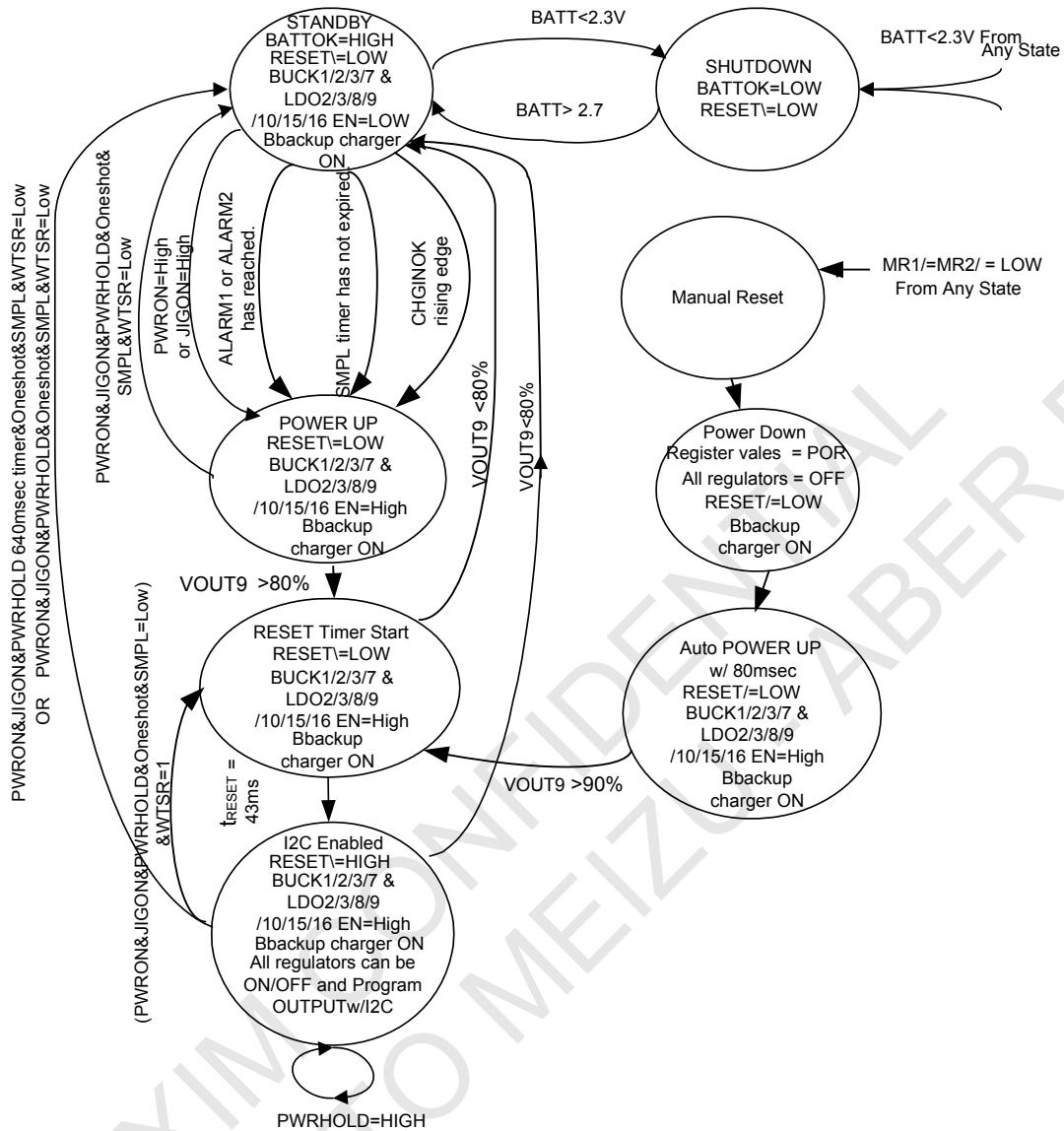


Figure 16 Power ON/OFF Control State Diagram of MAX8966

8.4.5 Power-Up and Power-Down Sequence

8.4.5.1 PWRON (or JIGON) Key Triggering Power on Sequence

High level on the PWRON (or JIGON) input (debounce time required) is the normal way of powering up a handset. This corresponds to the user pressing the power on key. When the power on key is pressed the PMIC will first look at the battery voltage, if the battery voltage is below the under voltage lockout point, the PMIC will ignore the key press since there isn't sufficient power to bring up the phone.

See Figure below for powers-up of Max8966/Max8997. After RSO/ is high, all regulators can be enabled or disabled via I2C except for LDO9.

8.4.5.2 PWRHOLD LOW Triggering Power Down Sequence

The normal way of powering off MAX8966/MAX8997 is by PWRHOLD going low. The following will trigger the PMIC to transition from ON to OFF condition

- Falling Low Threshold Level on PWRHOLD & Low Level of PWRON switch
- Falling Low Threshold Level on PWRON & Low level of PWRHOLD
- Internal temperature exceeding thermal limit
- LDO9 going out of regulation
- UVLO

If LDO9 goes out of regulation, the RSO\ is pulled low and the power-down sequence is initiated.

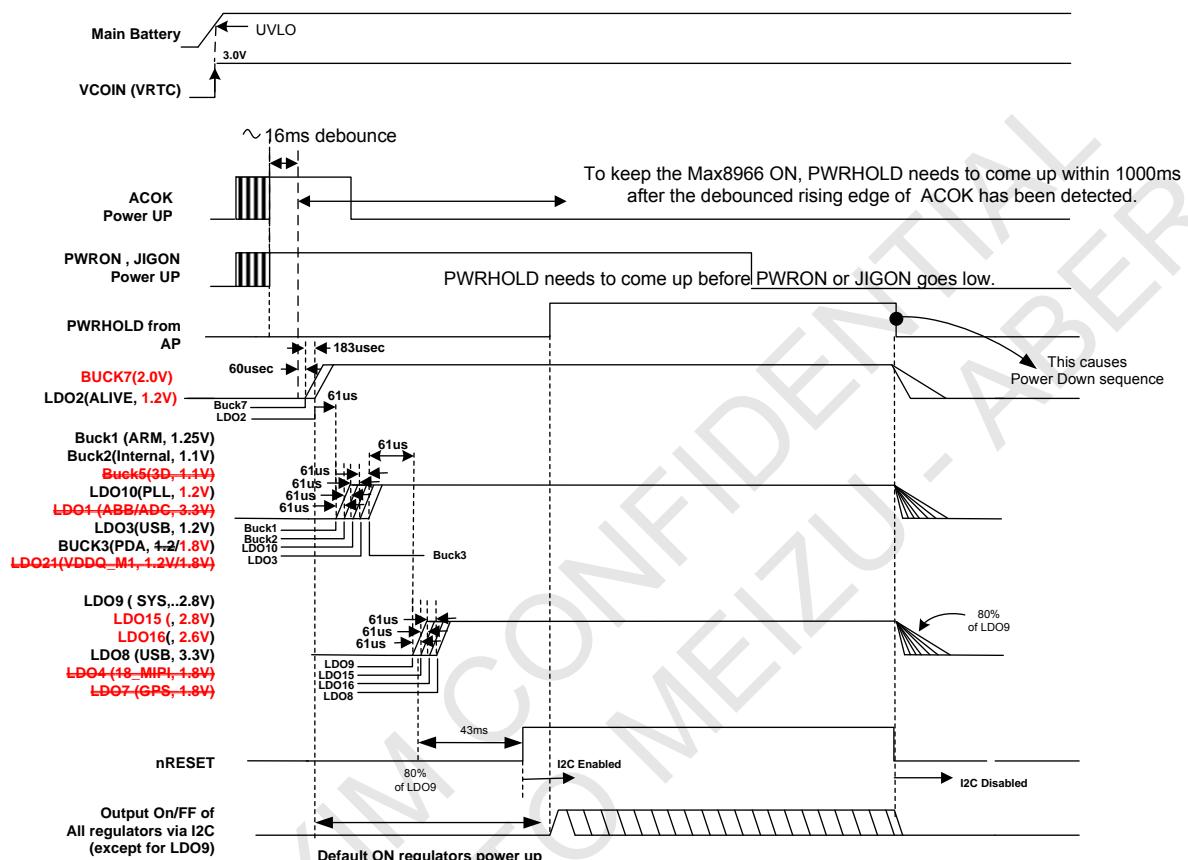


Figure 17 MAX8966 Power UP

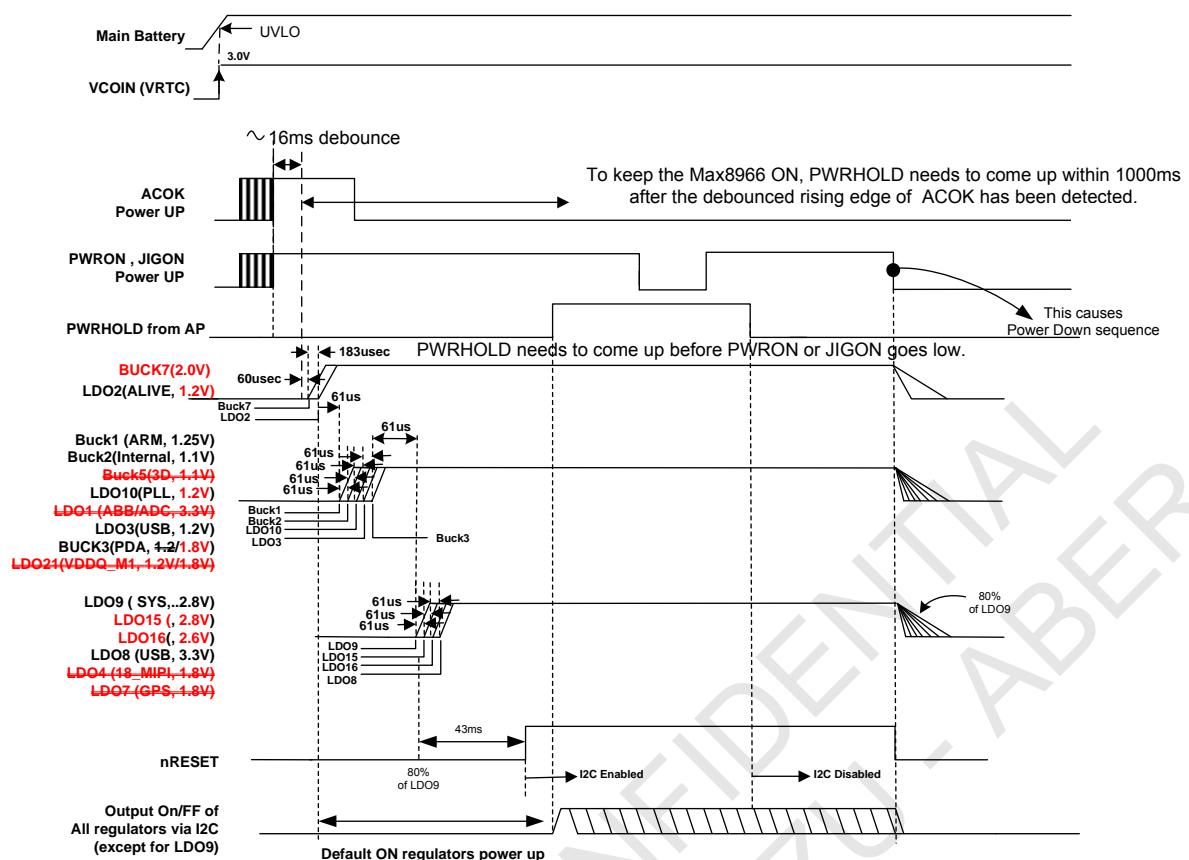


Figure 18 MAX8966 Power UP -2

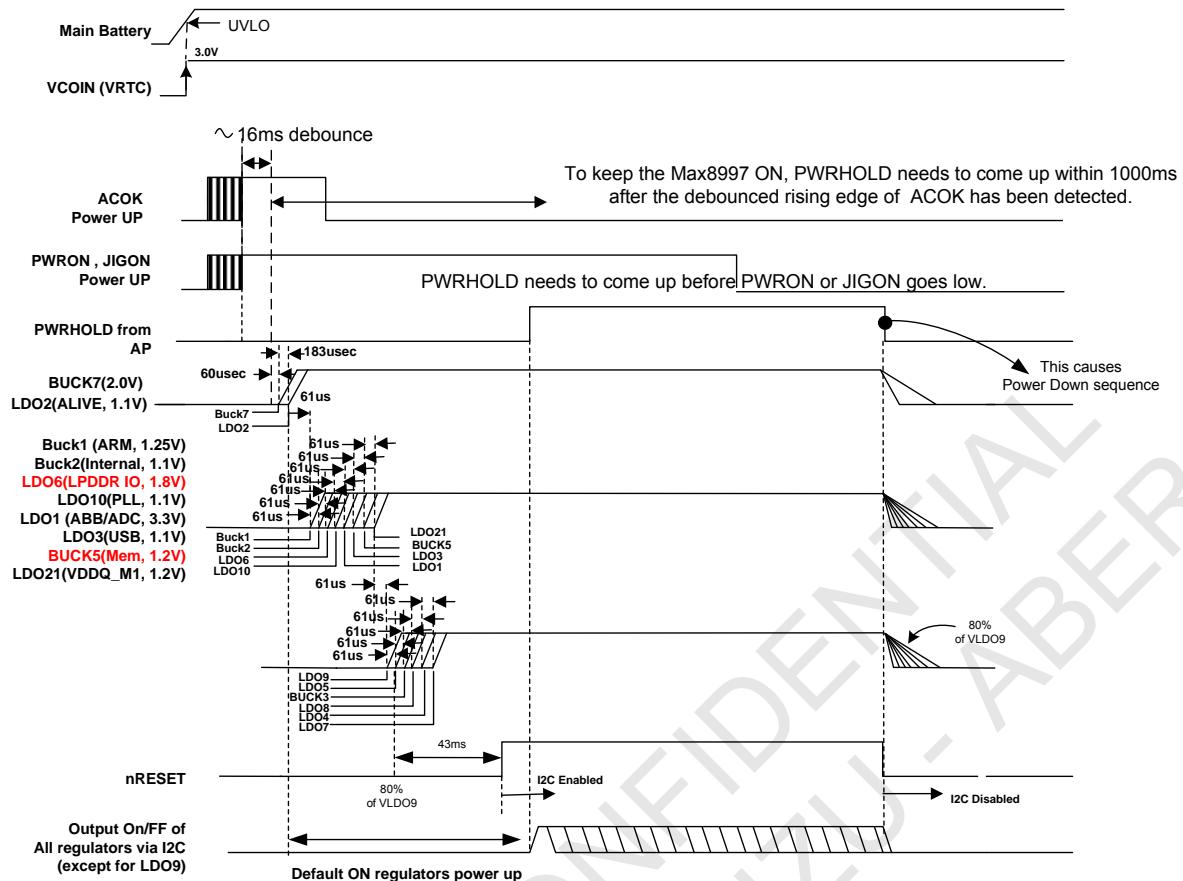


Figure 19 MAX8997 Power UP

8.5 Voltage Monitors, Reset, and Under-voltage Lockout Functions

8.5.1 Under-voltage Lockout (UVLO)

When the BATT input voltage is below V_{UVLO} , the MAX8966/MAX8997 enter its under-voltage lockout mode (UVLO). UVLO forces the device to a dormant state until the input voltage is high enough to allow the device to function reliably. In UVLO the input current is very low ($1\mu A$) and all regulators are off. $/RSO\backslash$ is forced low. The I²C does not function in UVLO and the I²C register contents are reset in UVLO.

There are two UVLOs, one for charger and one for the battery. The charger's UVLO is 4.0V. The battery UVLO threshold is set at 2.7V to turn on default-on power supplies.

8.5.2 Reset Output ($/RSO\backslash$) and $/MR1\backslash$ Input

The reset circuit is active both at power up and power down. $RSO\backslash$ is held low at power up. The reset timing starts once the LDO9 reaches 90% of its regulation voltage. The $RSO\backslash$ signal goes high 58.6ms(typ) after the voltages reach 80% of its regulation voltage. If LDO9 voltage drops below 80% of its regulation voltage, the MAX8966/MAX8997 shuts down.

$/RSO\backslash$ is an open drain reset output. A low on $RSO\backslash$ causes the application processor to enter its reset state.

$/RSO\backslash$ is forced low when one or more of the following conditions occur:

$MR1\backslash=MR2\backslash$ are logic low.

PWRHOLD goes to low.

LDO9 is below 80% of regulation

$VBATT$ is below V_{UVLO}

When MAX8966/MAX8997 goes into power down sequence.

/RSO\ is high-impedance when all of the following conditions are satisfied:

MR1\=MR2\ are logic high

LDO9 is above 80% of regulation

$V_{UVLO} < V_{BATT}$

The reset delay 58.6ms has expired.

PWRHOLD is high

When RSO\ is low, all registers (except MUIC, Fuel Gauge registers) and serially set voltage settings return to their default values.

8.5.3 Multi-Button Manual Reset

MR1\ and MR2\ are manual reset inputs for hardware reset. Falling edge of MR1\ and MR2\ and minimum 7sec (default) low initiate the automatic power reboot. The debounce time is programmable ranging from 1sec to 8sec (1sec step). After the debounce timer is expired, RSO\ asserts and all PMIC registers and serially-set voltage settings return to their default values. A logic low on MR1\ and MR2\ resets the MAX8966/MAX8997 I²C registers (except MUIC and Fuel Gauge registers) to their default values. Once it enters the automatic power up sequence, MAX8966/MAX8997 disregard another MR1\ and MR2\ signals and completes the cycle of power up sequence. Refer to the timing diagram below for the automatic power up initiated by MR\.

MR1\ and MR2\ are not a booting source. When MAX8966/MAX8997 is OFF state, MR1\=MR2\=Low does not initiate the reboot sequence. The automatic reboot is initiated only when LDO9>80%.

When the manual reset feature is not required, leave MR1 and MR2 open.

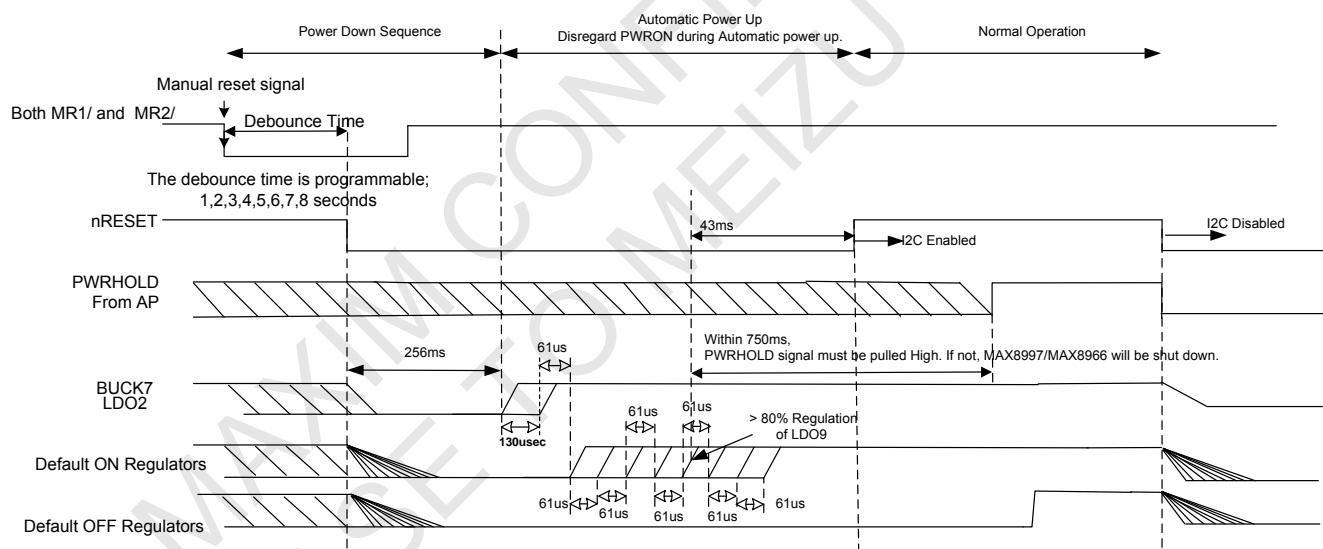


Figure 20. Timing Diagram of Automatic Power Up Caused by MR1\ and MR2\

8.5.4 Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX8966/MAX8997. When internal thermal sensors detect a die temperature in excess of +160°C, the corresponding regulator(s) are shut down, allowing the IC to cool. The regulators turn on again after the junction cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

A thermal overload on any of regulators (BUCK1~BUCK6, LDO1~LDO21) only shuts down the overloaded regulator. During thermal overload, Backup Charger is not turned off, and the I²C interface and voltage monitors remain active. The charger has an independent thermal control circuit that regulates die temperature during the charge.

8.6 32KHZ Clock oscillator

The 32.768kHz crystal oscillator provides an accurate low frequency clock for MAX8966/MAX8997 internal circuit as well as external circuitry via the 32kHzAP and 32kHzCP pins. The 32kHzAP is supplied by LDO9. 32kHzCP is supplied by an external supply PIN (VCC_32CP). **The external 32kHz X-tal is required since internal timer including power up sequence is activated by the external 32kHz x-tal.**

8.7 Charger for 1 Cell Li+ single Input

8.7.1 Detailed Description

The MAX8966/MAX8997 charger uses voltage, current, and thermal-control loops to charge a single Li+ cell and to protect the battery. When a Li+ battery with a cell voltage below 2.5V is inserted the MAX8966/MAX8997 charger enters the prequalification stage where it precharges the cell with 47.5mA. Once the cell has passed 2.5V, the charger soft-starts before it enters the fast-charge stage. The fast-charge current level is programmed through an I²C interface. As the battery voltage approaches 4.2V, the charging current is reduced. If the battery current drops to less than TOPOFF threshold current (50mAdefault), the MAX8966/MAX8997 sets the IRQ1\ low and the TOPOFFR bit in the interrupt register goes high, signaling that the battery is fully charged. The top-off current threshold can be programmed by ITOPOFF bits. At this point, 30 minutes top-off timer starts and the MAX8966/MAX8997 remains in the constant voltage regulation mode to maintain the battery at full charge. The charger can be turned off through a CHGENB=1 command. If, at any point, while charging the battery, the die temperature approaches 97°C, the MAX8966/MAX8997 reduces the charging current so the die temperature does not exceed 97°C. This feature not only protects the MAX8966/MAX8997 from overheating, but also allows the higher charge current without risking damage to the system. The charger time-out protection is programmable. After fully charged, the MAX8966/MAX8997 monitors VBATT and restarts if VBATT falls below the restart threshold voltage.

8.7.2 Soft-Start

An analog soft-start algorithm activates when entering fast-charge mode. This reduces the inrush current on the input supply

8.7.3 Prequalification State

The prequalification state occurs when the battery voltage is less than 2.5V.

In this state, the charger is on and delivering prequalification current to the battery. If the MAX8966/MAX8997 remains in this state for longer than t_{PQ} , then the MAX8966/MAX8997 transitions to the battery error state and the MAX8966/MAX8997 turns off. A normal battery typically stays in the prequalification state for several minutes or less and when the battery voltage rises above V_{PQ} , the MAX8966/MAX8997 transitions to the fast-charge constant current state.

8.7.4 Fast-Charge Constant Current State

The fast-charge constant current state occurs when the battery voltage is greater than V_{PQ} and less than V_{BATREG} . In this state the charger is on and delivering current I_{FC} to the battery. If the MAX8966/MAX8997 remains when the battery voltage rises to V_{BATREG} , the MAX8966/MAX8997 transitions to the fast-charge constant voltage state.

The MAX8966/MAX8997 dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG} , I_{FC} is reduced. If there is low input voltage headroom ($V_{IN}-V_{BAT}$), then I_{FC} decreases due to the impedance from IN to BAT.

8.7.5 Fast-Charge Constant Voltage State

The fast-charge constant voltage state occurs when the battery voltage is at the V_{BATREG} and the charge current is greater than I_{TOPOFF} . In this state the charger is on and delivering current to the battery. The MAX8966/MAX8997 maintains V_{BATREG} and monitors the charge current to detect when the battery consumes less than the I_{TOPOFF} current. When the charge current decreases below the top-off threshold, the MAX8966/MAX8997 transitions to the top-off state.

The MAX8966/MAX8997 continues to charge for 30 minutes after it detects the top-off threshold in order to fill up 2-3% more capacity.

8.7.6 Top-Off State

The top-off state occurs when the battery voltage is at V_{BATREG} and the battery current decreases below I_{TOPOFF} . In this state the charger is on and delivering current to the battery. The MAX8966/MAX8997 maintains V_{BATREG} for 30 minutes. When top off timer expires, the MAX8966/MAX8997 transitions to the done state.

8.7.7 Done State

The MAX8966/MAX8997 enters its done state after the charger has been in the top-off state for t_{TO} . In this state the charger is off and no current is delivered to the battery. If left in the done state long enough, the battery voltage will decay below the restart threshold (V_{RSTRT}) and the MAX8966/MAX8997 transitions back into the fast-charge state. There is no soft start (di/dt limiting) during the done to fast-charge state transition.

8.7.8 Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of its prequalification states is t_{PQ} . The time that the charger is allowed to remain in the fast-charge CC & CV states is t_{FC} which is programmable with TFCH[2:0]. Finally the time that the charger is in the top-off state is t_{TO} which is 30 minutes. Upon entering the timer fault state a MBCHGTMEXPD interrupt register is generated without a delay. In the timer fault state the charger is off. The charger can exit the timer fault state by programming the charger to be off and then programming it to be on again through MBCHOSTEN bit. Alternatively, the charger input can be removed and re-inserted to exit the timer fault state.

8.7.9 Thermal Shutdown State

The thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device's thermal shutdown threshold (T_{SHDN}). When T_J is close to T_{SHDN} the charger will have folded back the input current limit to 0A

In the thermal shutdown state the charger is off and timers are suspended. The charger exits the temperature suspend state and returns to the state it came from once the die temperature has cooled. The timers resume once the charger exits this state.

8.7.10 SAFEOUT with Overvoltage-Protected

SAFEOUT is a linear regulator that provides an output voltage of 4.95V and can be used to supply low voltage rated USB systems. The SAFEOUT1 linear regulator turns on when DCIN>=4.0V regardless of Charger Enable or DETBAT/. SAFEOUT_ is disabled when VIN is greater than the overvoltage threshold (7.5V typ). SAFEOUT1 is default ON. SAFEOUT2 is default OFF.

8.7.11 Main-Battery Detect Input Pin (DETBAT/)

If DETBAT is pulled to ground, this is an indication that the main battery is present therefore the main battery charger starts when the DCIN is valid. If DETBAT/ is driven high or left unconnected, this is an indication that the main battery is not present therefore the main battery charger does not start charging in response to a valid DCIN power input. The DETBAT/ is internally pulled to BATT through an internal 800kohm resistor. DETBAT/ status bit is valid when UVLO<BATT.

8.7.12 Charger Type Detection and Charger Behavior

USB_CPLNT is a signal from the MUIC to the main battery charger which indicates whether the Max8966/Max8997 is compliant to USB 2.0 specification or not.

When it is not complaint (USB_CPLNT=0), the SAFEOUT1 linear regulator turns on when 4.0V<DCIN<7.5v regardless of CHGEN\ and DETBAT\. SAFEOUT1 is disabled when VIN is greater than the overvoltage threshold (7.5V typ).

When it is compliant (USB_CPLNT=1), the SAFEOUT linear regulator turns on **when the charger detection is complete** and 4.0V<DCIN<7.5v regardless of CHGEN\ and DETBAT\. Charger detection complete is indicated when SFOUT_EN (signal from MUIC) is logic high. SAFEOUT1 is disabled when VIN is greater than the overvoltage threshold (7.5V typ).

Table 3: Charger behavior for USB_CPLNT=0 and USB_CPLNT=1

	USB_CPLNT=0	USB_CPLNT=1
CHG_TYP=000	Charger Off	Charger Off
CHG_TYP=001	Charger On Charging current = Default. Charging current can be programmed by I2C.	Charger Off, Firmware will turn on by I2C write
CHG_TYP=010	Charger On Charging current = Default. Charging current can be programmed by I2C.	Charger On Charging current = Default. Charging current can be programmed by I2C.
CHG_TYP=011	Charger On Charging current = Default. Charging current can be programmed by I2C.	Charger On Charging current = Default. Charging current can be programmed by I2C.
CHG_TYP=100	Charger On Charging current = Default. Charging current can be programmed by I2C.	Charger On Charging current = Default. Charging current can be programmed by I2C.
CHG_TYP=101	Charger On Charging current = Default. Charging current can be programmed by I2C.	Charger On Charging current = Default. Charging current can be programmed by I2C.
CHG_TYP=110	Charger On Charging current = Default. Charging current can be programmed by I2C.	Charger On Charging current = Default. Charging current can be programmed by I2C.
CHG_TYP=111	Not supported - will never occur.	(USB Dead Battery Support) Charging current = 90mA
SFOUT_LDO	Enabled by MPOR=1 && ESAFEOUT1 or ESAFEOUT2=1 (Default: ESAFEOUT1=1, ESAFEOUT2=0) SFOUT_LDO should be off when the MPOR=0.	Enabled by MPOR=1 && ESAFEOUT1 or ESAFEOUT2=1 (Default: ESAFEOUT1=1, ESAFEOUT2=0) SFOUT_LDO should be off when the MPOR=0.
MIC_ON	Charger must be shut off in a microphone signal compliant state. MIC_ON will only be high when the microphone mode is required.	Charger must be shut off in a microphone signal compliant state. MIC_ON will only be high when the microphone mode is required.

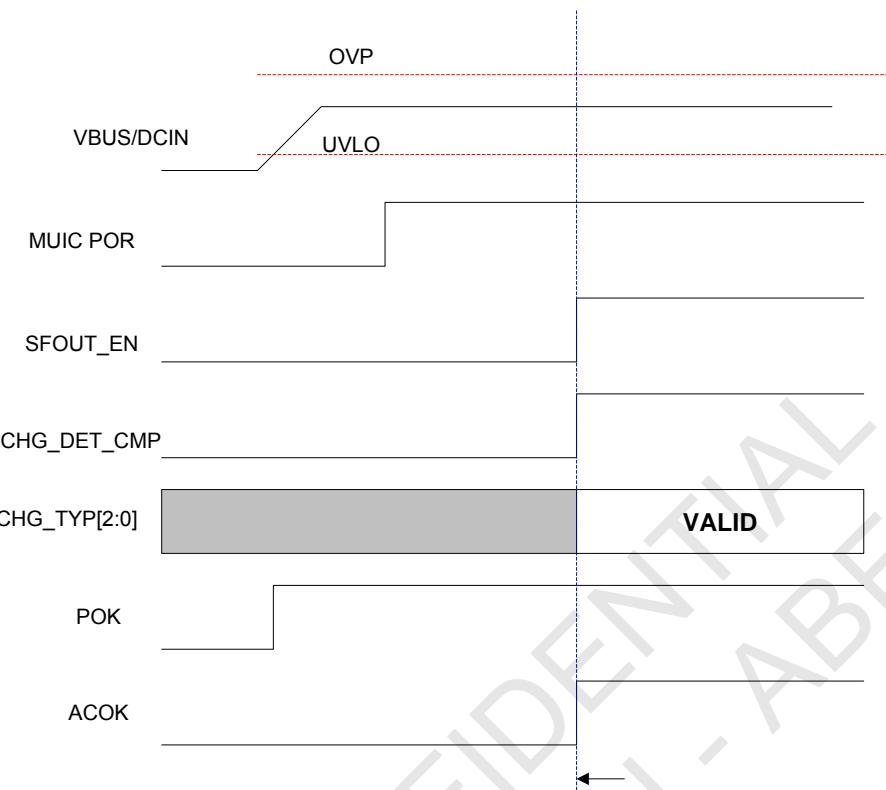


Figure 21: Charger timing diagram USB_CPLNT=1 and USB_CPLNT=0

8.7.13 Charger State Diagram and Timing Diagram

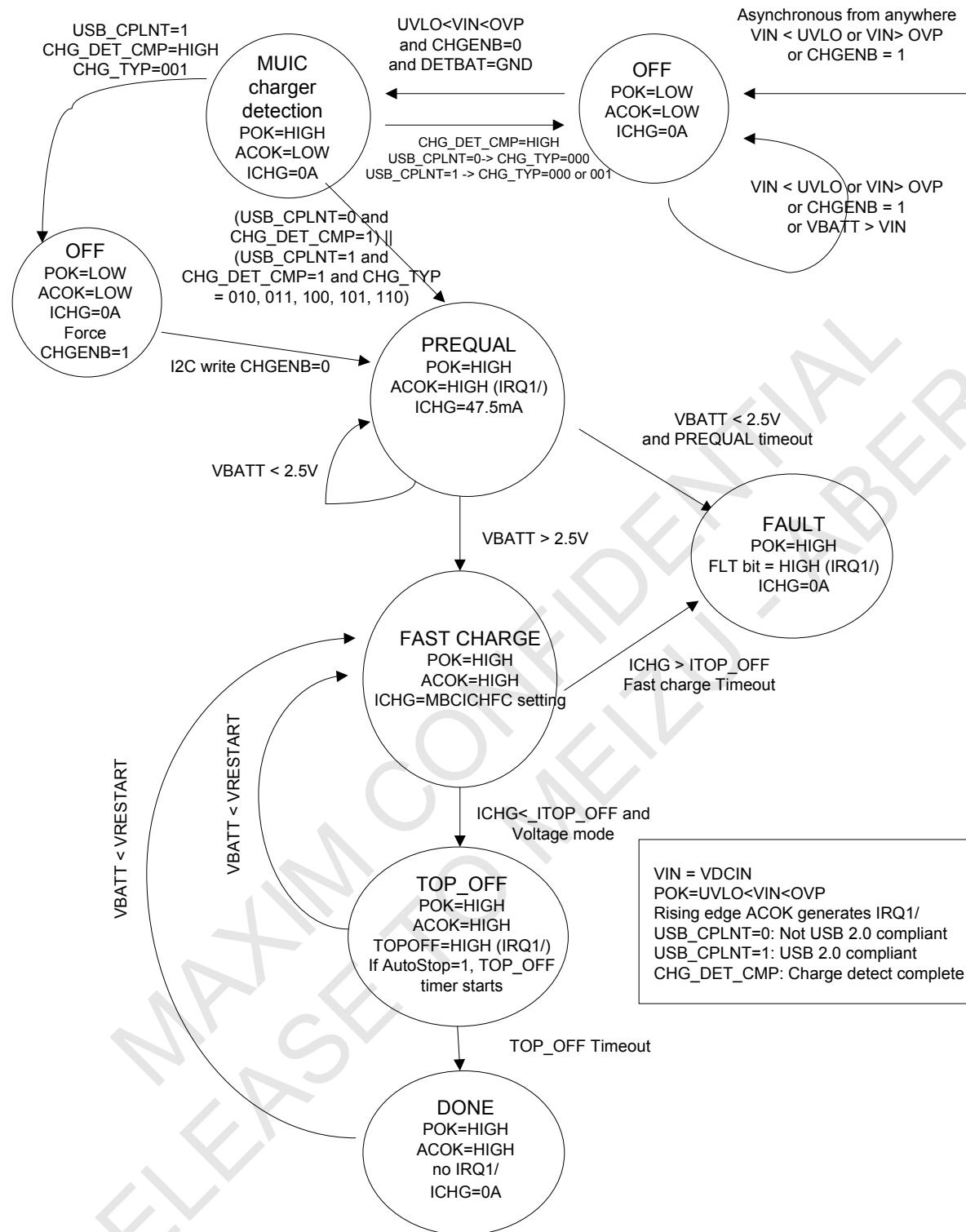


Figure 22 Charger state diagram

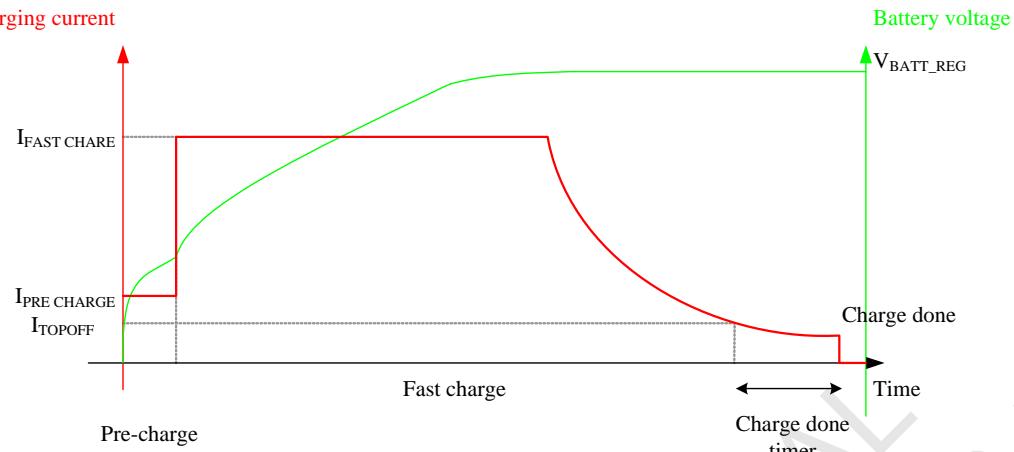


Figure 23 Main Battery Charging Profile

8.7.14 Measuring the Charge Current (VICHG)

VICHG is a buffered output that can be interpreted to the charge current.

$$VICHG = 1500mV / ICHG (1000mA)$$

Avoid adding capacitance directly to the VICHG pin that exceeds $tbdpF$.

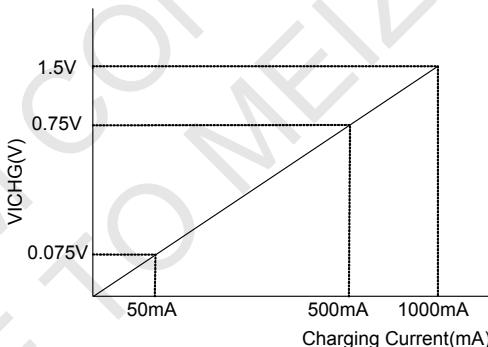


Figure 24 VICHG output voltage vs. Current

8.8 IRQ\ Description

The MAX8966/MAX8997 uses 2 interrupt pins. There are IRQ1\, and Alert. IRQ1\ is a dedicated interrupt output pin for PMIC. Alert pin is a dedicated interrupt pin for Fuel Gauge. The interrupts are to indicate to the Application processor that the status of the MAX8966/MAX8997 has changed. The IRQ1\ signal is asserted whenever one or more interrupts are toggled. The Application Processor shall read the interrupts in 2 steps. First, the Application Processor reads the INTSRC register. This is a read-only register which indicates which functional block is generating the interrupt, i.e. RTC, MUIC, Haptic Motor Driver, Fuel Gauge, Key Expnader, PMIC. Depending on the result of the read, the next step is to read the actual interrupt registers pertaining to the functional block.

For example, if the Application processor reads 0x02 from INTSRC register, it means the PMIC functional block has an interrupt generated. The next step is to read INT1 and INT2 registers of the PMIC functional block. The IRQ1\ pin becomes high (cleared) as soon as the read sequence of the last INT_ register that contains an active interrupt starts. All interrupts can be masked to prevent the IRQ\ from being asserted for masked

interrupts. A mask bit in the IRQM register implements masking. The IRQ register can still provide the actual interrupt status of the masked interrupts.

8.8.1 DVSOK interrupt;

When a Buck Output voltage reaches to +/-90% of target voltage AND the status of actual output voltage of Buck is changed from the previous target voltage in DVS mode, an interrupt (nIRQ1) is asserted.

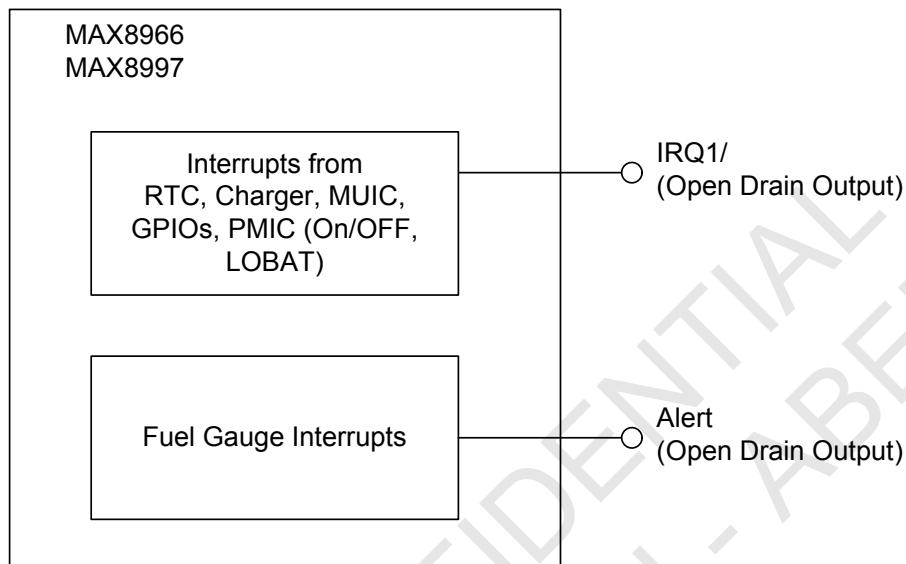


Figure 25 Interrupt Block Diagram

8.9 RTC Functional Description

The MAX8966/MAX8997 contains eight 8-bit Timekeeping registers, two sets of seven 8-bit Alarm Threshold registers, and two Alarm Configuration registers. The real time clock stores time and date data in a BCD (Binary Coded Decimal) format. A time/date programmable alarm function is provided which can be set to trigger once per second, once per minute, and at other periodic time intervals. The alarm can also be set to trigger once on a specific date. The ALARMx status in the status register remains until the user clears the alarm by reading or writing to an Alarm Threshold register or the Alarm Configuration register. The interrupt ALARM0 and ALARM1 bits directly result from the ALARM0 and ALARM1 status change from 0 to 1, in the Status register. Time information can be provided in either a 24-Hour or a 12-Hour format, with an AM/PM indicator. The date at the end of the month is automatically adjusted for months with less than 31 days, including corrections for leap year. The day-of-week register increments at midnight.

8.9.1 Timekeeping & Alarm Thresholds Registers

Time and date data is stored in the Timekeeping & Alarm Threshold registers in BCD format as shown in the Register/Address Definition table. The Weekday data in the Day register is user defined (a common format is for 1=Sunday, 2=Monday, etc.)

8.9.2 AM-PM/12-24 Mode

For both Timekeeping and Alarm Threshold Registers, D7 of the Hours Register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, D5 is the AM/PM bit with logic high being PM. In the 24-hour mode, D5 is the second 10-hour bit (20-23 hours).

8.9.3 Alarm Generation Function

The two alarm functions are configured using the Alarm registers. When the alarm is triggered, the corresponding alarm bit in the interrupt registers will be set to a high and the open-drain IRQ1\ pin will go low. If we read interrupt registers, the corresponding alarm bit and the IRQ1\ pin will be cleared after reading process is ended.

8.10 WTSR (Watchdog Timeout and Software Resets) Function:

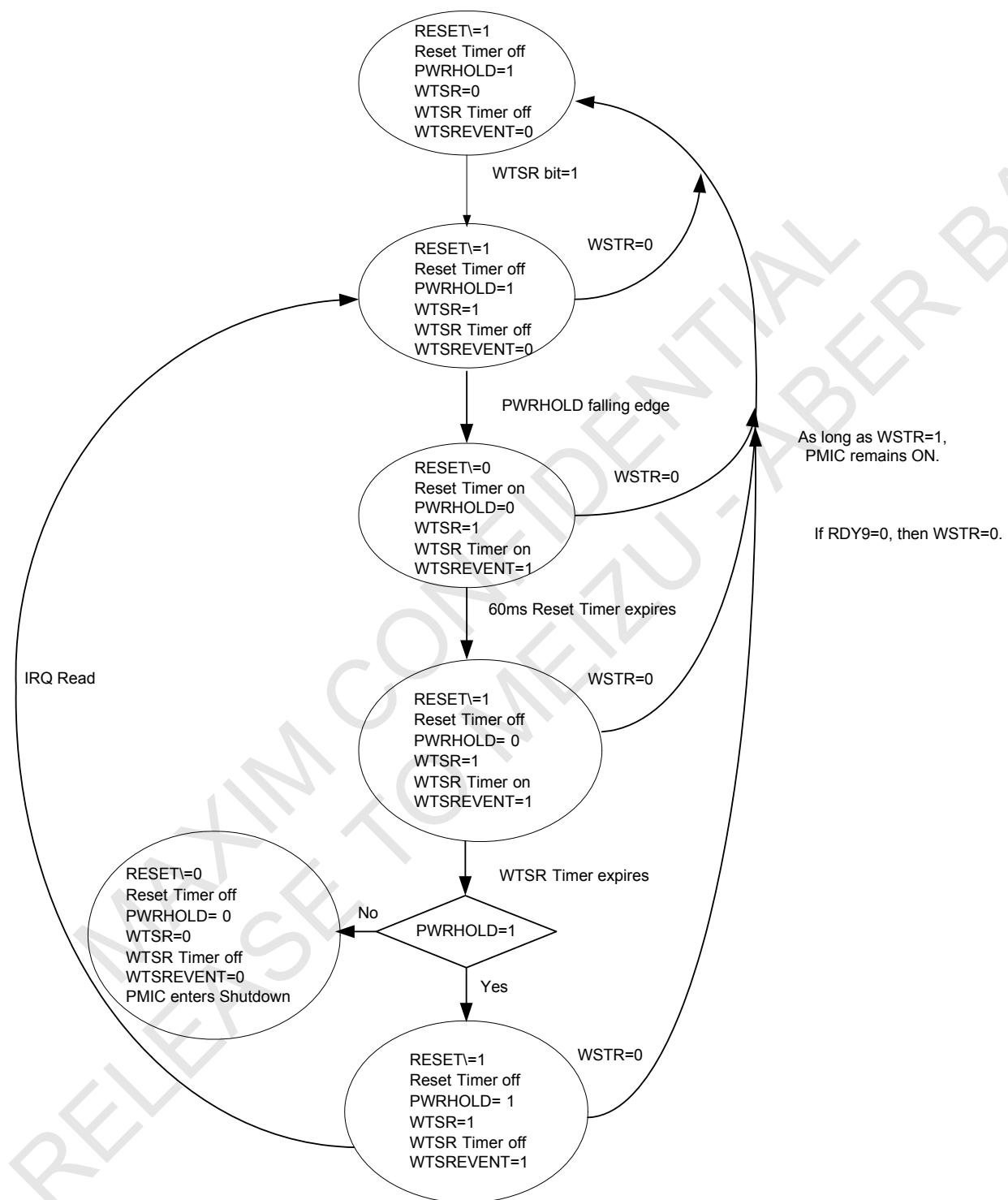


Figure 26 WTSR State Diagram

8.10.1 Reading From The Timekeeping Registers

The Timekeeping Registers (Seconds, Minutes, Hours, Date, Month, Day, Year, and Century) can be read through the I²C Bus Read Command.

When reading the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

If Single Reads are to be used to read each of the Timekeeping Registers individually then it will be necessary to do some error checking on the receiving end. The potential for error is the case when the seconds counter increments before all of the other registers are read out. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during Single Read operations of the Timekeeping Registers. Then the net data could become 14:59:59, which is erroneous real-time data. To prevent this with Single Read Operations, read the Seconds Register first (initial seconds) and store this value for future comparison. When the remaining Timekeeping registers have been read out, read the Seconds Register again (final seconds). If the "initial seconds" value is 59, check that the "final seconds" value is still 59, if not repeat the entire Single Read process for the Timekeeping registers. A comparison of the "initial seconds" value with the "final seconds" value can indicate if there was a bus delay problem in reading the timekeeping data (difference should always be 1 second or less). Using a 100kHz bus speed, and sequential Single Reads would take under 2.5mS to read all seven of the Timekeeping registers plus a second read of the Seconds Register.

The single Reads mode is not recommended.

The most accurate way to read the Timekeeping Registers is to do a sequential Read. In the sequential Read, the Main Timekeeping Registers (Seconds, Minutes, Hours, Date, Month, Day, Year, Century) are read sequentially in the order listed with the Seconds Register first. Worst case error that can occur between the "Actual" time and the "Read" time is one second.

8.10.2 Writing To The Timekeeping Registers

The Time and Date may be set by writing to the Timekeeping Registers (Seconds, Minutes, Hours, Date, Month, Day, Year, and Century).

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the MAX8966/MAX8997RTC. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 500 milliseconds. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Illogical time and date entries result in undefined operation.

8.11 SMPL (Sudden Momentary Power Loss) Function:

The SMPL function can be used to initiate a power up sequence after momentarily loosing contact to the battery pack. If the PMIC is powered down and the battery voltage is below the UVLO threshold, a SMPL timer is started in the event that the SMPL bit is set.

If the battery voltage raises about the UVLO threshold before the SMPL timer times out the PMIC is automatic booted. The SMPL timer times out before the Battery voltage raises about the UVLO threshold the PMIC remains off.

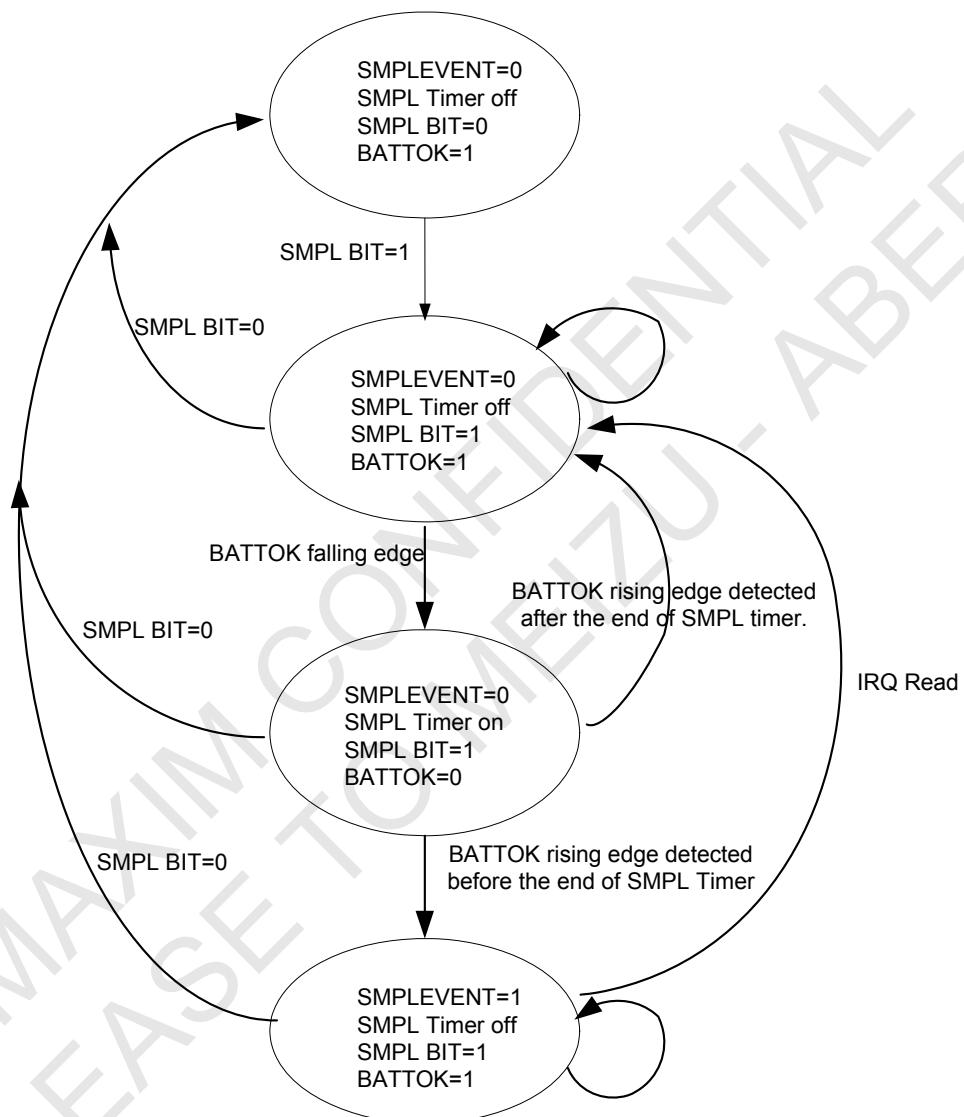


Figure 27 SMPL state diagram

9 HAPTIC MOTOR DRIVER

9.1 Features

- Drives ERM and LRA Vibration Motors Directly
- User selectable external PWM drive signal or internal register based drive signal
- External PWM input (10kHz to 50kHz)
- Internal Motor Enable Input – turns motor driver on/off
- Internal Mode Select Input – selects between ERM and LRA motors
- Low Standby Current – 1uA typical
- Gain Control Input – Sets maximum output swing
- Separate Motor Supply pins
- Selectable Filter Capacitor on Gain pin to control PWM spikes
- Fast Wake-up Time
- Nearly Rail-to-Rail output swing at maximum current

9.2 Haptic Generation

Haptic generation can occur from two sources, 1) via the PWM input (MPWM) to the motor driver block, or 2) via an I2C command using the internal registers to define the pattern (IPWM).

9.2.1 PWM Input

If the Haptic Type bit (HTYP) is set to a logic low, then the device uses the external PWM pin (MPWM) as input to the motor driver block. When this bit is a logic high the device uses an internally generated PWM signal (RPWM for Register based PWM)) to create a haptic event. If HTYP=0 and an internally generated haptic event is requested, the internally generated haptic event should occur as requested using the internally generated RPWM signal. If during the playout of an internally generated haptic event, should the user set HTYP=0, the internally generated haptic event will terminate immediately and turn control over to the external MPWM input. The haptics status bit can also be checked to determine if an internal haptic event is on-going. When an internally generated haptics event is requested, the MEN is automatically set to a valid condition (logic high). Note that in order for an externally generated haptic event to occur, the user must first turn on the motor driver and allow time for the motor driver circuitry to settle before issuing the haptic pattern sequence on the MPWM input. Note that by setting HTYP=1, this effectively disables the MPWM input pin. This can occur automatically as when an internally generated haptic event is on-going.

9.2.2 Overview

The internally generated haptic waveform pattern is constructed with the following elements: an internal PWM signal (RPWM) can be defined to control the average DC voltage on the DP and DN pins. The PWM frequency, duty cycle, and number of cycles can be programmed. The parameters are defined in registers 0x04 through 0x0F.

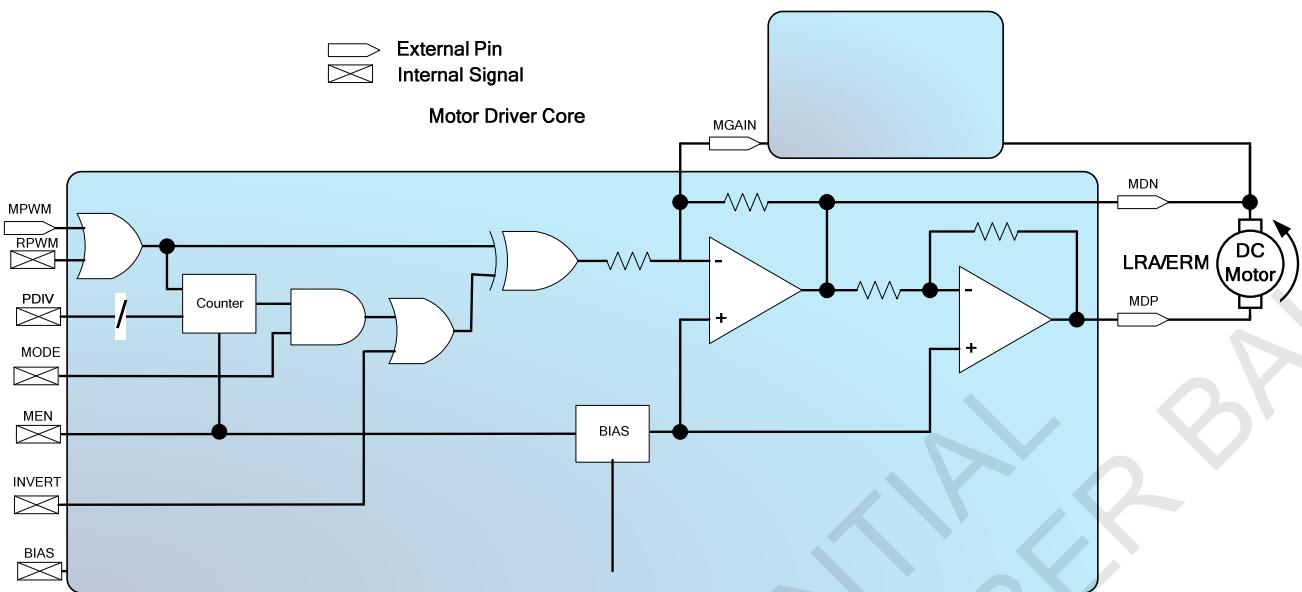


Figure 28 : Internal Vibration Motor Controller Simplified Diagram

Four different values can be chosen for each of the parameters above and stored in a lookup-table upon startup of the system. Registers 0x04 through 0x0F then define each of the parameters for the haptic outputs by selecting one of the four possible values from the lookup table using an indirect addressing scheme. Note that with the indirect addressing scheme, a user may select one value for CYC, another for SIGDC, another for SIGP, and a forth value for PWMDC. Although there are only 4 sets of registers, the indirect addressing scheme allows 256 possible combinations (4x4x4x4) by writing different values to the address register, 0x03.

Once the haptic signals are defined, writing to register 0x03 can be used to start a haptic event. The indirect addressing scheme is depicted in figure below**Error! Reference source not found.**. The two-bit addresses CYCA[1:0], SIGDCA[1:0], SIGPA[1:0], and PWMDCA[1:0] select one out of four stored values in the lookup table.

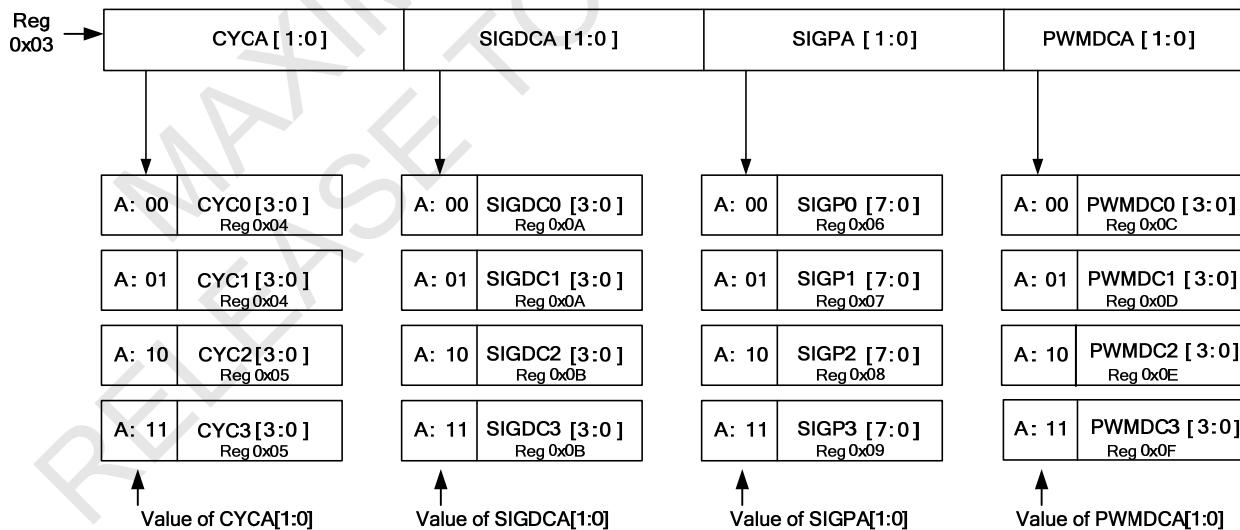


Figure 29: Indirect addressing scheme for the haptic feedback signal.

9.2.3 Definition of the Internal PWM Signal

In order to facilitate pulse width modulation, the smallest building block of the haptic signal is the internal PWM pulse. Both pulse width and duty cycle can be programmed. See the figure below.

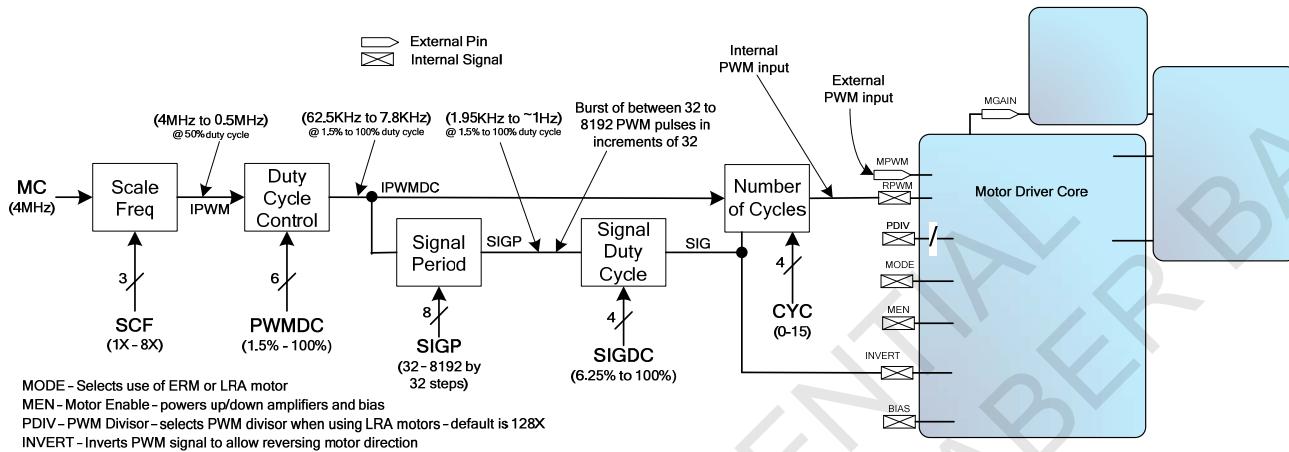


Figure 4: Simplified Block Diagram

The pulse width of the internal PWM signal is comprised of time units RPWM_UNIT, which is defined using bits SCF[2:0] (scale Frequency) in register 0x01. This value is common for all internally generated haptic feedback signals. RPWM_UNIT is defined in terms of clock cycles of the main 4MHz clock and can be programmed from one to eight master clock cycles. This provides a frequency range of 4Mhz (SCF=0) to 0.5MHz (SCF=7).

The output of the frequency scaling block is then used to create the IPWMDC signal with user programmable duty cycle. The duty cycle resolution is 6-bits. This provides a PWM frequency range of 62.5KHz (SCF=0) to 7.8KHz (SCF=7) with programmable duty cycle from ~1.56% (code 0) to 100% (code 63).

MCP = Master Clock Period (time)

IPWM_UNIT = $(SCF + 1) * MCP$

IPWM_PERIOD = $IPWM_UNIT * 64$

IPWM_HIGH = $(PWMDC + 1) * IPWM_UNIT$

IPWM_LOW = $IPWM_PERIOD - IPWM_HIGH$

(4MHz clock)

(SCF is user-defined from 0 to 7)

(Six bits give 1/64 or 1.56% step size)

(PWMDC is user defined)

Error! Reference source not found. shows the construction of a PWM signal assuming SCF=3 and PWMDC=31 (50% duty cycle).

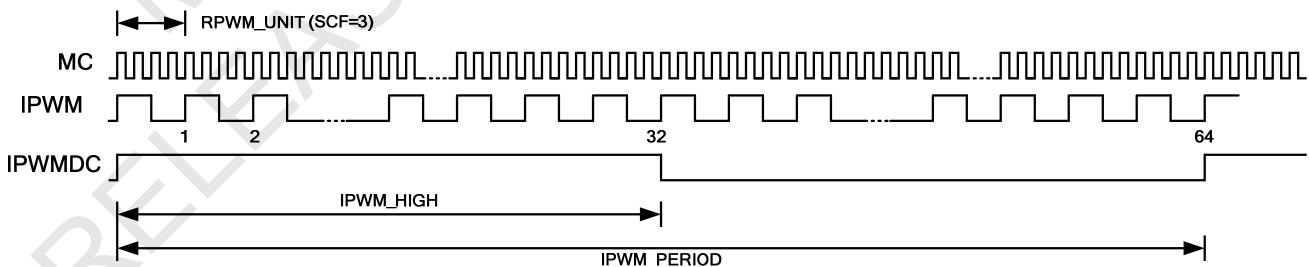


Figure 30: Generation of the IPWM signal. MC: 4MHz master clock, PWMDC: resulting IPWM signal.

9.2.4 Definition of the Haptic Feedback Signal

Similar to the definition of the IPWM signal, the period and the duty cycle of the actual haptic feedback signal can be programmed by choosing one of four SIGP[7:0] and SIGDC[3:0] values.

SIGP[7:0] determines the total time of one haptic feedback signal. A large range has to be covered to accommodate both the needs of ERM and LRA vibration motors. The time of the haptic feedback signal is given as number of IPWM_PERIOD cycles. The minimum width is 32, while the maximum is 8192, allowing programmability in 32 pulse increments. The actual signal frequency depends on the choice of SCF[2:0]. With a setting of SCF=0, a frequency range of 1.953kHz (SIGP=0) to 7.6Hz (SIGP=255) can be covered. With a setting of SCF=7, a frequency range of ~244Hz (SIGP=0) to ~1Hz (SIGP=255) can be covered.

The duty cycle can be programmed in 16 steps from 6.25% to 100% using SIGDC[3:0]. If a value of 15 is chosen (100%), the pulse is high for the entire time. This setting can be used to create long turn-on times for the motor. **Error! Reference source not found.** details the construction of the haptic feedback signal.

SIGP = Period of one haptic signal

(Measured in number of IPWMDC pulses. 8-bit number, minimum is 32 pulses, maximum is 8192 pulses, programmable in 32-pulse increments)

SIGDC = Duty cycle of SIGP

(SIGDC is user defined, four bits give 1/16 or 6.25% step size)



Figure 31: Definition of the haptic feedback signal

Finally CYC[3:0] defines how often the basic haptic feedback signal is to be repeated to form the entire haptic feedback pattern. Setting CYC[3:0] to zero effectively turns off any haptic feature. **Error! Reference source not found.** shows a full haptic feedback pattern.

CYC_PERIOD = Total duration of the haptic pattern (equals CYC * SIGP)

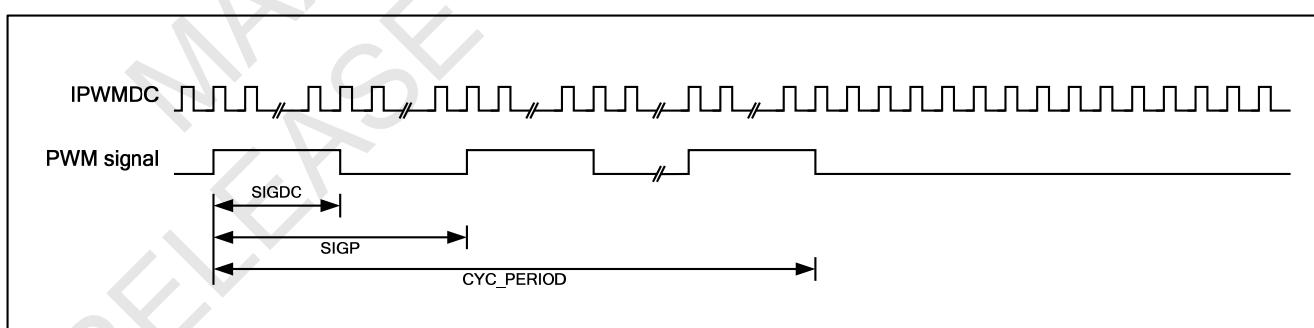


Figure 32: Total haptic feedback pattern

Figure 33 summarizes the generation of the internally generated haptic feedback waveform that is applied to the input of the motor driver core. The middle and bottom waveforms show the actual signal at the PWM input (RPWM) to the motor driver. The upper waveform, SIG, shows the signal at the INVERT input of the motor driver core. This signal is also used to determine when to drive the IPWM input at 50% duty cycle (when the

invert bit equals logic zero) and to invert the RPWM signal (when the invert bit equals logic one). The invert bit is controlled by the setting in the configuration registers.

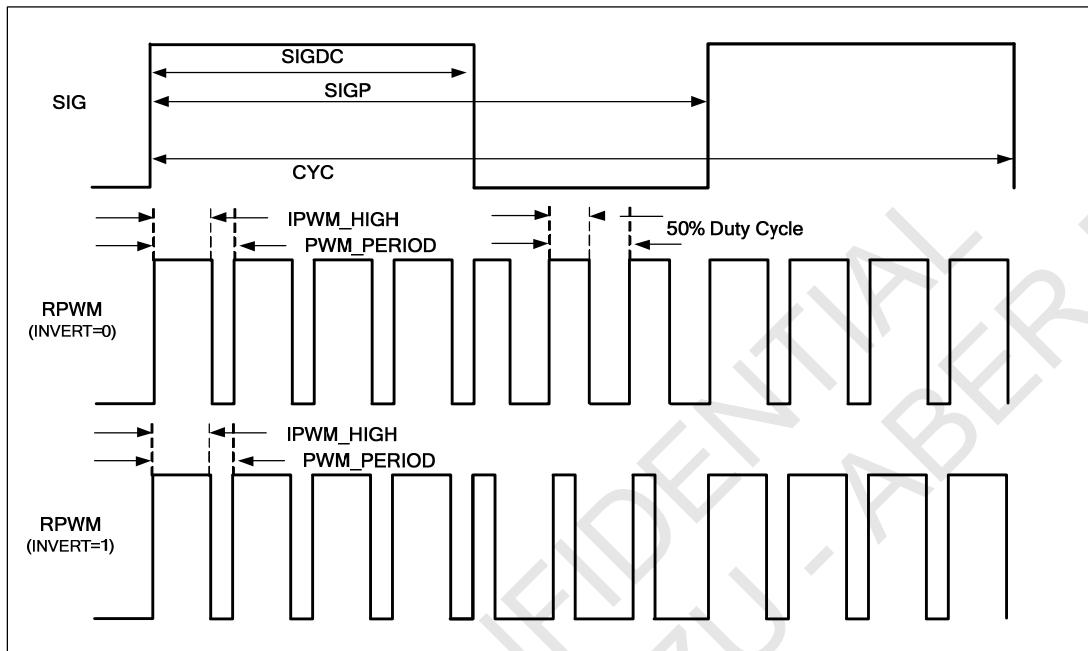


Figure 33: Summary of the haptic waveform

9.2.5 I2C Interface with Haptic Motor Driver

Haptic events can be generated using the I²C bus and internal haptic registers. The desired parameters for the haptic event should be stored in the internal haptic registers prior to issuing a haptic command. To activate a haptic event, a haptic command (0x20) is sent over the I²C interface. The contents of the byte send sent should contain the address of the desired haptic registers to use fro the pattern playout. Note that a write command must be given. The playout of the pattern will follow the values and procedure dictated by the haptic configuration registers.

10 MUIC (Micro USB Interface)

The Micro USB Block includes USB 2.0 Hi-Speed, UART, stereo audio pin with microphone, and stereo audio pin on one micro USB connector. This device features internal detection logic for determining the device connected and is controlled through the I²C interface. Audio inputs feature negative rail signal operation down to -1.9V (typ). This supports USB Charging Specification Revision 1.0.

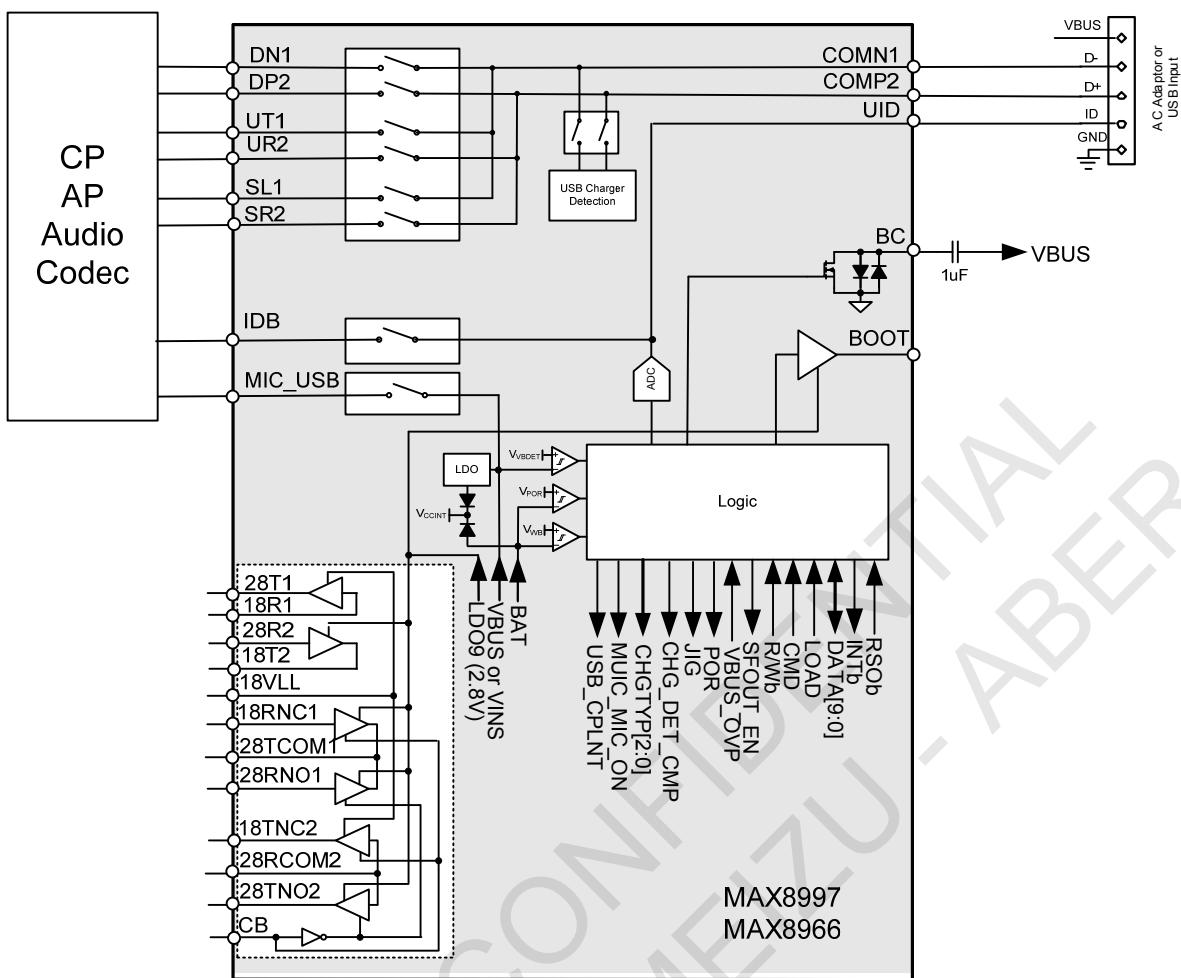


Figure 34. Functional Diagram of MUIC

RF Noise Immunity

The microphone and audio headset paths in cellular phones are susceptible to pickup of the radiated RF energy from the phone antenna due to the headset wire. The RF pickup is dependent upon the physical distance between the worse and the antenna, the radio frequency and the modulation standard. Typically the worst phone modulation is GSM because it has the highest peak radiated RF energy, the carrier frequency may be between 800-980MHz or 1.8~1.96GHz, and is modulated at the GSM packet rate of 217Hz. This means that the audio paths (COMN1, COMP2, UID, and VBUS) need to be either bypassed to GND with an effective RF short (typical 12pF to 33pF capacitor) or must be immune to the RF energy. The COMN1 and COMP2 paths can not be bypassed to GND due to the high speed USB signals so they must be immune. The applied RF signal may be high in amplitude – up to about 0dBm or higher depending on antenna placement and design.

Under-voltage Lockout (UVLO) of MUIC

The MUIC of MAX8966/MAX8997 enter its under-voltage lockout mode (UVLO) when

MUIC internal voltage supply < (BATT_UVLO and DCIN_UVLO).

UVLO forces the MUIC to a dormant state until the input voltage is high enough to allow the device to function reliably. In UVLO the input current is very low. The I²C register contents are reset in UVLO.

The rising threshold of MUIC UVLO is set as

MUIC internal voltage supply > (BATT_UVLO or DCIN_UVLO).

10.1 Factory Mode

Accessory detection is enabled at power-up (AccDet=1 in the CONHTROL2 register), enabling the factory detection state machine. The device detects accessories in the following order of priority:

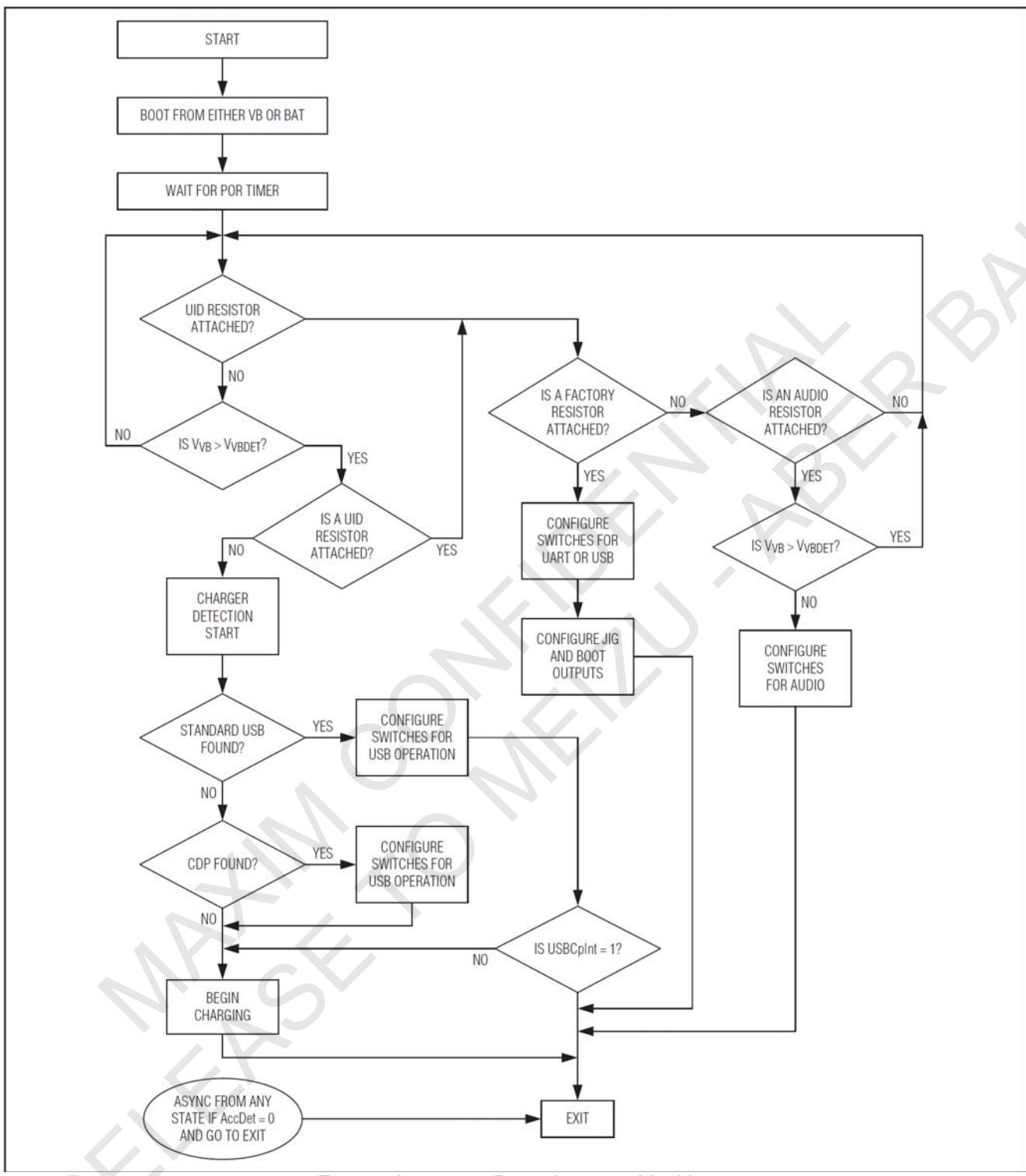
- 1) Four factory mode ID resistor values.
- 2) Audio Type 1 device. The accessory is detected as either a 1Mohm resistor or any button press resistor value when VBUS I not present.
- 3) USB cable. A USB cable is detected when UID is unconnected and the ChgTyp bits in the STATUS2 register are 001 or 010. Charging can also be enabled when ChgTyp=001 if USBCplnt=0.
- 4) Dedicated Chargers.

The device factory detection state machine detects the external accessories and automatically configures the internal switches and BOOT and JIG outputs. Set the AccDet Bit to 0 to disable automatic accessory detection. When automatic detection is disabled, the internal switch states must be manually controlled through the I2C interface.

Table 3. Factory Mode Resistor Response (R_{ID})

R_{ID}	JIG	BOOT	COMN1	COMP2
255kΩ	LOW	LOW	DN1	DP2
301kΩ	LOW	HIGH	DN1	DP2
523kΩ	LOW	LOW	UT1	UR2
619kΩ	LOW	HIGH	UT1	UR2
All other resistors	HIGH	Low	X	X

X= Don't care



Factory Accessory Detection state Machine

10.2 Input Sources

The typical micro USB connector has five signal lines: USB power, two USB signal lines (D-, D+), ID line, and ground. The USB power on the micro USB connector connects to VB (internal node of MAX8966/MAX8997). The two USB signal lines, D-/D+, connect to COMN1 and COMP2. The ID line connects to the UID input.

USB Switch (DN1,DP2): It supports Hi-Speed (480Mbps) and full-speed (12Mbps) USB signal levels between 0 and 3.3V. The USB channel is bidirectional and has low on-resistance and low on-capacitance. The low on-resistance is stable as the analog input signals are swept from ground to V_{SWPOS} for low signal distortion.

UART Switch (UT1,UR2): The UART input supports standard UART signals (typically 3.0V max). The UART channel can also be used for Hi-Speed USB signals. The UART channel is bidirectional and has low on-resistance.

Stereo Audio (SL1,SR2) and Microphone (MIC): The device supports a stereo audio amplifier with a mono microphone. Figure below shows a typical application for a cell phone headset with a pushbutton remote control through a Micro USB connector. The device routes the LEFT(SL1) and RIGHT(SR2) channel audio to the D-(COMN1) and D+(COMP2) lines. SL1 and SR2 are negative rail capable to V_{SWNEG} . Internal 100 Ω switched shunt resistors on the LEFT and RIGHT channel speaker lines can be enabled through the RCPS bit in the CONTROL 2 register to reduce pops and clicks heard when the audio amplifier is switched on. The microphone signal is routed through the VBUS line on the Micro-USB connector. SL1 and SR2 can alternatively be used to a USB high-speed signal.

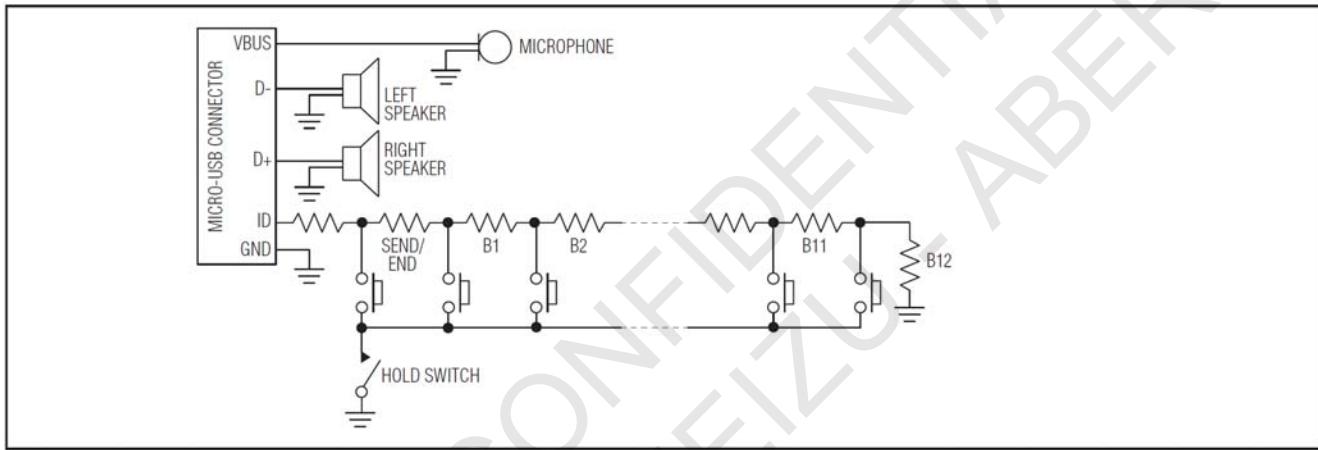


Figure 35 Headset with Remote Control

10.3 High-Impedance mode for COM switches

The device allows COMN1 and COMP2 to be set to high impedance (COMN1Sw and COMP2Sw=100 to 111) to have a safe position when a headset is inserted. If COMN1 or COMP2 are left connected to one of the three inputs, there is a possibility of having a DC voltage present causing a pop when a connection is made to a speaker.

Click and Pop Reduction

The device supports click-and-pop reduction through the RCPS bit in the CONTROL2 register. Set RCPS to 1 to connect 100ohm shunt resistors from the audio inputs (SL1 and SR2) to GND to remove any DC bias that could come from AC-coupling capacitors prior to connecting them to COMN1 or COMP2. Disable the click-and-pop shunt resistors prior to using the channel.

MAX8966/MAX8997 has an I²C setting which will set the two 3:1 mux switches to a high impedance setting. This allows the COM pins to have a “safe” position when a customer inserts a headset. If the COM switches are left connected to one of the 3 inputs, there is the possibility of having a dc voltage present which would cause a pop in the speakers.

BOOT and JIG Pins

It includes two special purpose pins which are controlled by a unique resistor value on the USB ID pin. These pins are automatically set every time a valid voltage is applied to VBUS where the state of these pins is set automatically if one of 4 unique resistor values is applied to the USB ID pin. These pins can also be manually controlled through I²C registers.

BOOT is a push pull driver referenced to VIOMUIC. It can be set to either high or low. JIG is internal signal.

10.4 Accessories Detection

The device supports multiple accessories by detecting unique characteristics including VB voltage, ID resistor, and USB charger detection.

10.4.1 Interrupts

The device generates an interrupt in response to accessory insertion and removal and to battery charger status changes. The STATUS1 (0x04), STATUS2(0x05), and STATUS3 (0x06) registers are the status bits for each interrupt source; changes of these bits set the associated interrupt bits in the INT[3:1] registers. The INT[3:1] registers are cleared after a read.

IRQ1/ is asserted when any of these bits that are set, unless masked in the INTMASK registers. Read an INT register to clear that register and deassert the IRQ1/ output. Each interrupt is independently maskable. Set any of the bits in the INTMASK1, INTMASK2, and INTMASK3 registers to mask the associated interrupts. Bits in the INT registers are set, but IRQ1/ is not asserted for masked interrupts. All interrupts are masked by default.

10.4.2 Detection Debounce

The device includes debounce timers to avoid generating multiple interrupts at the insertion of an accessory and for added noise and disturbance protection. The interrupt state must be maintained for the duration of the debounce delay before an interrupt at IRQ1/ is generated. The ADC debounce can be changed by the ADCDbSet bits in the CONTROL3 register to adjust the debounce delay during accessory insertion and removal.

10.4.3 Low Power Mode

The device contains multiple low-power modes. Set the appropriate bits (CPEN, ADCEn, or LowPwr) in the CONTROL2 register to enter low-power mode.

The CPEn bit controls the charge pump required for proper operation of the analog switches. Set CPEn to 0 to disable the charge pump. CPEn must be set to 1 anytime that a switch is enabled. Do not apply a negative-rail voltage to any switch when the charge pump is disabled. The device turns on the charge pump automatically when AccDet=1 when the switches are configured. ADCEn controls the internal ADC. Set ADCEn to 0 to disable the ADC. In this mode, the ADC bits in the STATUS1 register are set to 11111, disabling all interrupt detection. Any pending interrupts due to a change in ADC value must still be cleared by reading the INT1 register. Set the LowPwr bit to 1 to enable the low-power hibernate mode. The device enters the low-power hibernate mode only if LowPwr=1 and UID is not connected and VBUS is not present. The device does exit this mode and resumes normal operation if any of these conditions are changed.

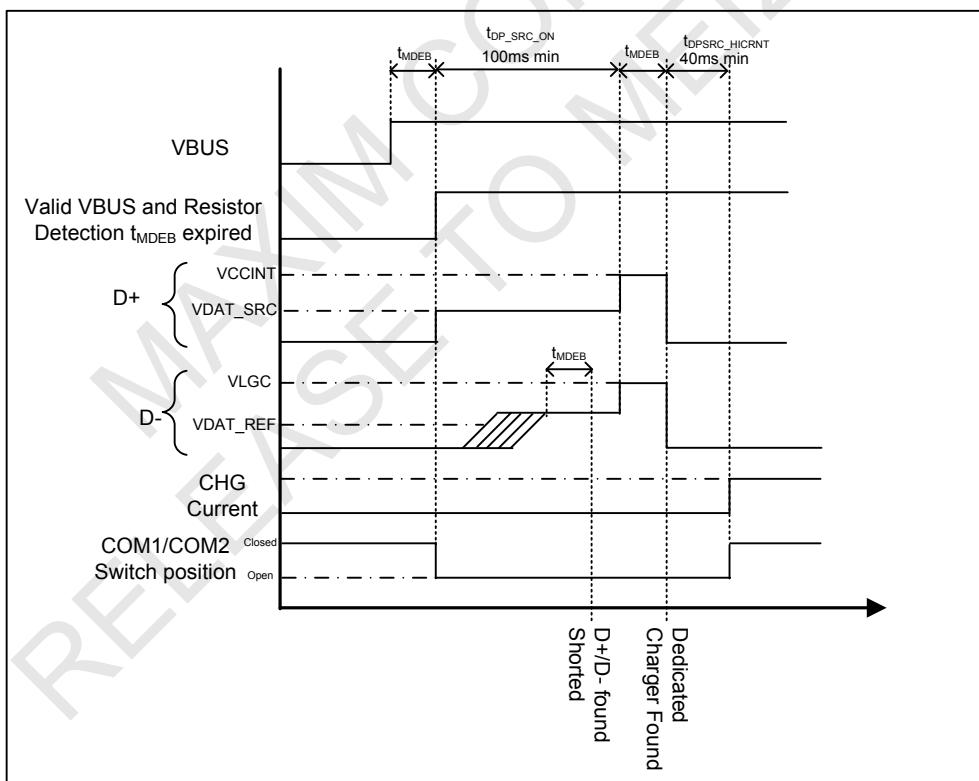
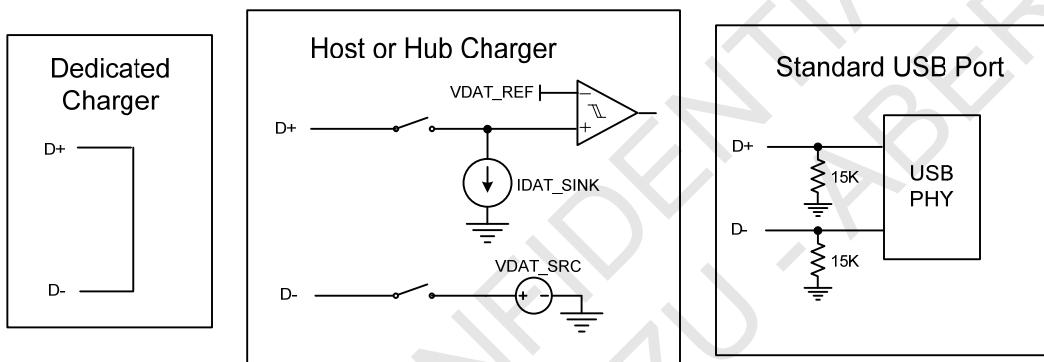
10.4.4 USB Charger Detection

The device detects battery-charging sources as defined in USB Battery Charging Specification Revision 1.1(USBBC 1.1) and can also detect two charger types typically used by Apple devices. The device can detect multiple USB battery-charging methods, including standard downstream ports (SDPs), charging downstream ports (CDPs), dedicated charging ports(DCPs), and Apple 500mA and 1000mA chargers. Connecting a valid VBUS voltage to VB when ChgDetEn=1 in the CDCTRL1 register enables automatic charger-detection mode, or set the ChgTypMan bit in the CDETCTR1 register to 1 to force a manual charge detection. After the VB debounce delay, the device opens the COMN1 and COMP2 (USB D- and D+) switches and initializes the

internal state machine to detect the type of charging source connected. While in charger-detection mode, check for battery chargers in the following order:

- 1) Either VBUS rises above the VB detect threshold or ChgTypMan=1, COMN1 and COMP2 switches are opened.
- 2) DCD: The device verifies that the USB cable is fully inserted.
- 3) Apple charger detection and DCP detection
- 4) SDP and CDP detection.
- 5) In standard operating mode, AccDet=0. COMN1 and COMP2 switches are returned to their previous state.

The ChgDetRun bit in the STATUS2 register is 1 while the state machine is running. The state machine output is indicated by the ChgTyp bits in the STATUS2 register once the detection algorithm has been completed.



10.4.5 Headset with Remote Control

The Samsung standard headset uses the VBUS pin for the microphone signal, D-/D+ for audio left and right and the ID line for an optional remote control based on variable resistor values. The simple headset will include only the SEND/END button.

Table 4 Accessory Detection Characteristics with Internal UID_R_DET Pullup Resistor

with UID_R_DET Pullup Resistor						ID Resistor	Description		
Hex	ADC Value								
	4	3	2	1	0				
0x00	0	0	0	0	0	GND	USB_OTG		
						75	Audio Video Cable with load		
0x01	0	0	0	0	1	2K	SEND/END Button		
0x02	0	0	0	1	0	2.604K	Remote S1 Button		
0x03	0	0	0	1	1	3.208K	Remote S2 Button		
0x04	0	0	1	0	0	4.014K	Remote S3 Button		
0x05	0	0	1	0	1	4.82K	Remote S4 Button		
0x06	0	0	1	1	0	6.03K	Remote S5 Button		
0x07	0	0	1	1	1	8.03K	Remote S6 Button		
0x08	0	1	0	0	0	10.03K	Remote S7 Button		
0x09	0	1	0	0	1	12.03K	Remote S8 Button		
0x0A	0	1	0	1	0	14.46K	Remote S9 Button		
0x0B	0	1	0	1	1	17.26K	Remote S10 Button		
0x0C	0	1	1	0	0	20.5K	Remote S11 Button		
0x0D	0	1	1	0	1	24.07K	Remote S12 Button		
0x0E	0	1	1	1	0	28.7K	Reserved Accessory 1		
0x0F	0	1	1	1	1	34K	Reserved Accessory 2		
0x10	1	0	0	0	0	40.2K	Reserved Accessory 3		
0x11	1	0	0	0	1	49.9K	Reserved Accessory 4		
0x12	1	0	0	1	0	64.9K	Reserved Accessory 5		
0x13	1	0	0	1	1	80.07K	Audio Device Type 2		
0x14	1	0	1	0	0	102K	Phone Powered Device		
0x15	1	0	1	0	1	121K	TTY Converter		
0x16	1	0	1	1	0	150K	UART Cable		
0x17	1	0	1	1	1	200K	CEA-936A Type 1 Charger		
0x18	1	1	0	0	0	255K	Factory Mode BOOT(off) USB		
0x19	1	1	0	0	1	301K	Factory Mode BOOT(on) USB		
0x1A	1	1	0	1	0	365K	Audio Video Cable		
0x1B	1	1	0	1	1	442K	CEA-936A Type 2 Charger		
0x1C	1	1	1	0	0	523K	Factory Mode BOOT(off) UART		
0x1D	1	1	1	0	1	619K	Factory Mode BOOT(on) UART		
0x1E	1	1	1	1	0	1000K	Audio Device Type 1 with Remote		
						1002K	Audio Device Type 1 – simple control		
0x1F	1	1	1	1	1	Open	USB, Dedicated Charger or Accessory removal		

Table 5 Accessory Detection Characteristics with Internal UID_R_VID Pullup Resistor

with UID_R_VID Pullup Resistor						ID Resistor	Description		
ADC Value									
Hex	4	3	2	1	0				
0x00	0	0	0	0	0	GND	USB_OTG		
0x01	0	0	0	0	1	75 ohms	Audio Video Cable with load		

10.4.6 MHL CABLE Detection

The device supports to detect MHL Cable indirectly.

With MHL Cable ID=1kohm and VBUS 5V, MUIC will have the following register bits. An interrupt is generated and the main charger will be turn ON. By reading the registers below, MHL cable can be recognized by host.

- VBVolt=1,
- ADCError=1,
- ADCLow=1

The MHL cable insertion will turn on main charger, but there is no auto switch configuration.

10.4.7 Application Information

Table 6 shows the supported accessories and states of the USB pins lines and the BOOT and JIG outputs.

Hi-Speed USB

Hi-Speed USB requires careful PCB layout with 45Ω single-ended / 90Ω differential controlled-impedance matched traces of equal lengths.

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to $\pm 2\text{kV}$ (Human Body Model) encountered during handling and assembly. COMN1, COMP2, and UID are further protected against ESD up to $\pm 15\text{kV}$ (Human Body Model) without damage. The VB input withstands up to $\pm 15\text{kV}$ (HBM) if bypassed with a $1\mu\text{F}$ ceramic capacitor close to the pin. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX8966/MAX8997 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

11 Uni-Direction Level Translator

The level translator is a simple logic gate with the input and output referenced to different voltages. This type of level translator may be used for UART signals and any other single direction logic signal.

The translators are organized in two groups. All the translators have one voltage level fixed to 2.8V (LDO9). Each pin name is formed of 3 parts. The first part is the supply voltage it is referenced to, the second is a letter for a receiver "R" or transmitter "T" and the third is the channel number. The two switch channels also add NO (normally open), NC (normally closed) or COM (common) to the channel number. Example 18R1 is referenced to 18VLL, a receiver (input) and channel 2. Channel 2 is formed as a receiver/transmitter pair – 18R1 and 28T2.

Group1: referenced to 18VLL

- 2 simple one IN and one OUT channels.
- 2 switch channels.
- 18VLL may be any voltage between 1.65V and 5.5V.

Each pin of level translator must be terminated either Low or High when it is used. Do not leave it open (or floating) . If not used, tie the pins as below

18VLL=CB=18R1=28R2=28RCOM2=28RN01=18RNC1=GND.

12 FLASH LED DRIVER.

The MAX8966/MAX8997 flash LED driver integrates an adaptive 1500mA PWM step-up DC-DC converter, two 750mA white LED camera flash/movie current drivers. An I²C interface controls individual on/off of all outputs, step-up output voltage setting, movie/flash current and flash timer duration settings.

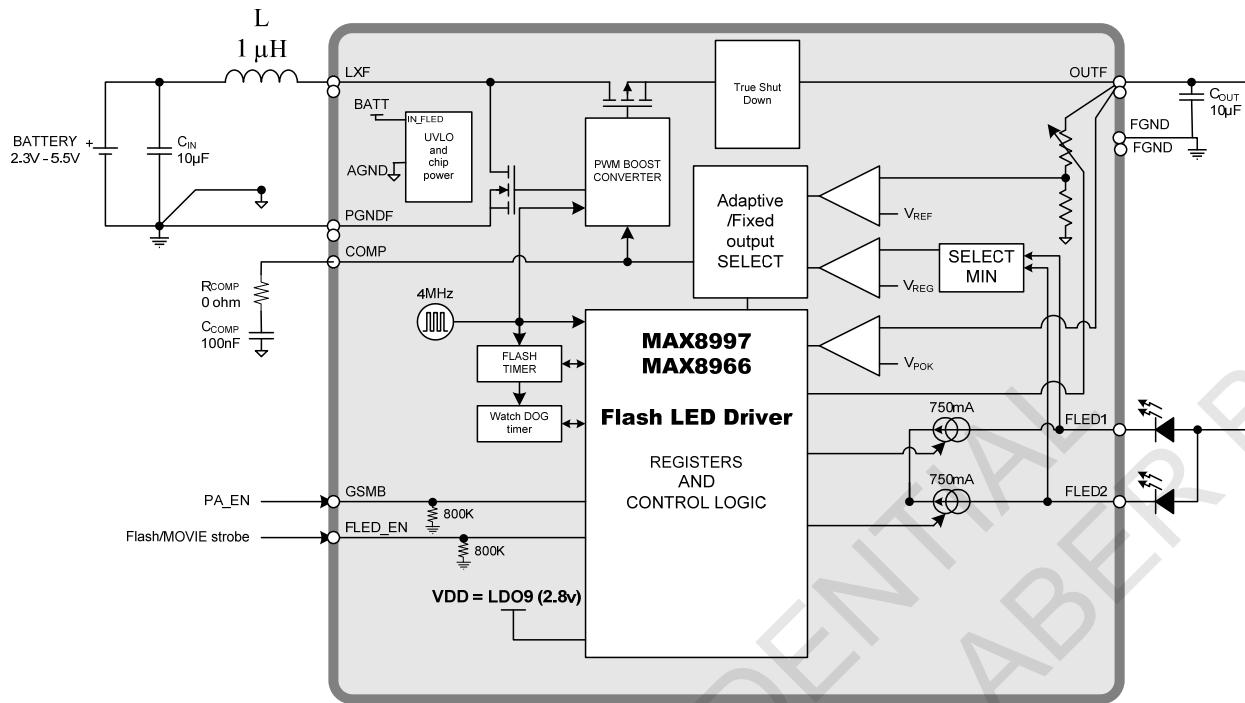


Figure 36 Flash LED Driver Block Diagram

12.1 Step-Up Converter (LXF, OUT, COMP, PGND)

The MAX8966/MAX8997 flash LED driver includes a fixed frequency, PWM Step-Up converter that supplies power to the anode of the Flash LEDs. The output voltage of the Step-Up converter is programmable from 3.7V to 5.2V (in 100mV steps) through an I²C register (BOOST_CNTL). The Step-up converter switches an internal power NFET switch and an internal synchronous rectifier at a constant 2MHz frequency with varying duty cycle up to 75% to maintain constant output voltage as the input voltage and load vary. Internal circuitry prevents any unwanted sub-harmonic switching by forcing a minimum 7% switching duty-cycle.

When the Step-up converter is set to operate in drop-out mode, the internal power NFET switch is forced off while the internal synchronous rectifier is forced on, keeping the voltage at OUT equal to the LX input. This mode provides the lowest current consumption when driving LEDs with low forward voltage.

The Step-Up converter can also be set to operate in adaptive mode where the output voltage of the Step-Up converter can be adaptively regulated based on the LED forward (Cathode) voltage.

When the Step-Up converter is set to operate in program mode, the output voltage is internally monitored for a fault condition. If the output voltage drops below 12% (typ) of the nominal programmed value, a POK fault is indicated in status register. This feature is disabled if the Step-Up converter is set to operate in adaptive mode.

12.2 Flash Current Regulator FLED1 and FLED2

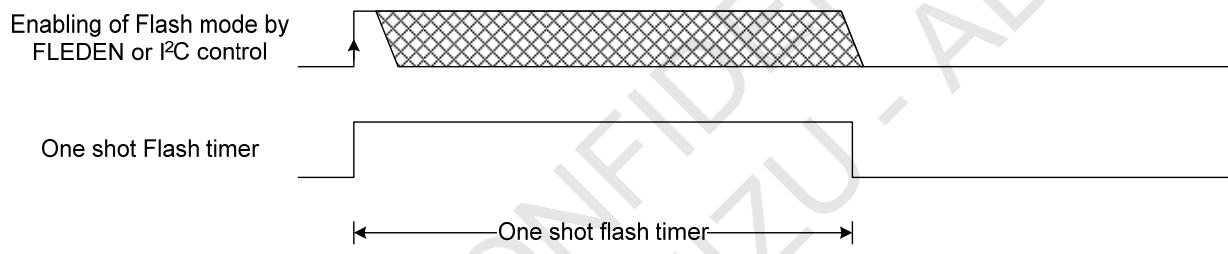
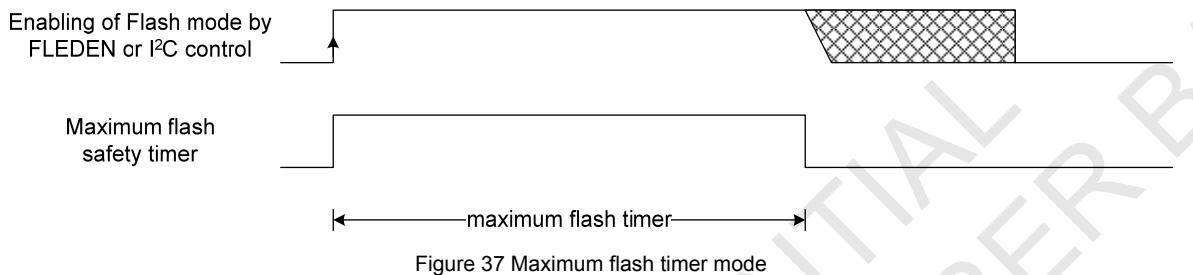
A low dropout linear current regulator from FLED1/FLED2 to FGND sinks current from the cathode terminal of the flash LED(s). The FLED1/FLED2 current is regulated to I²C programmable levels for movie mode (up to 250mA) and flash mode (up to 750mA). The movie mode provides continuous lighting when enabled via I²C or FLEDEN. When the flash mode is enabled, a flash safety timer, programmable from 25ms to 800ms through I²C, limits the duration of the flash mode. Once the flash safety timer expires, the current regulators return to movie mode. The flash mode has priority over the movie mode.

12.3 Flash LED Enable input (FLED_EN)

The FLEDEN logic input can enable/disable the FLED1 and FLED2 current regulators. It can be programmed to control movie mode, flash mode, by MOVIE_EN, and FLASH_EN bits respectively. Refer to the LED_CNTL register description for more information. If the FLED1/FLED2 is enabling for both Movie and Flash mode at the same time, flash mode has priority. Once the flash safety timer expires, the current regulator then returns to the movie mode.

12.4 Flash Safety Timer

The flash safety timer is activated any time Flash Mode is selected, either with FLEDEN or via the I²C interface. The flash safety timer, programmable from 25ms to 800ms via I²C, limits the duration of the Flash Mode in case FLEDEN is stuck high or I²C has not changed within the programmed flash safety timer duration. This timer can be configured to operate either in one-shot timer or maximum flash duration timer (see FLASH_CNTL register description). In one-shot mode, the flash function is initiated on the rising edge of FLEDEN (or I²C bit) and terminated based on the programmed value of the flash safety timer. In maximum flash timer mode, flash function remains enabled as long as FLEDEN is high, unless the pre-programmed flash safety timer times out.



Once the flash mode is disabled, by either LED_EN I²C or flash safety timer, the flash has to be off for a minimum time of, flash debounce timer, before it can be reinitiated again. This will prevent spurious events from re-enabling the flash mode.



Figure 39 Flash debounce timer

12.5 Watch Dog Timer

A watch dog timer function is included that can be programmed, using the I²C interface, in a range from 4 sec to 16 sec with a interval of 4 sec. If the Watch Dog timer expires, this will be interpreted as an indication that the system is no longer responding and enters safe mode. In safe mode, all current regulators as well as the step up DC-DC converter are disabled to prevent potential damage to the system. The I²C settings for the respective registers are not changed, therefore resetting the Watch Dog Timer will revert the flash LED driver back to the state present before entering safe mode. Setting the WDT_EN bit to 1 in the WDT_CNTL register enables the watch dog timer. Resetting the watch dog timer is achieved by the rising or falling edge of LED_EN or by setting bit 0 in the WDT_CNTL register.

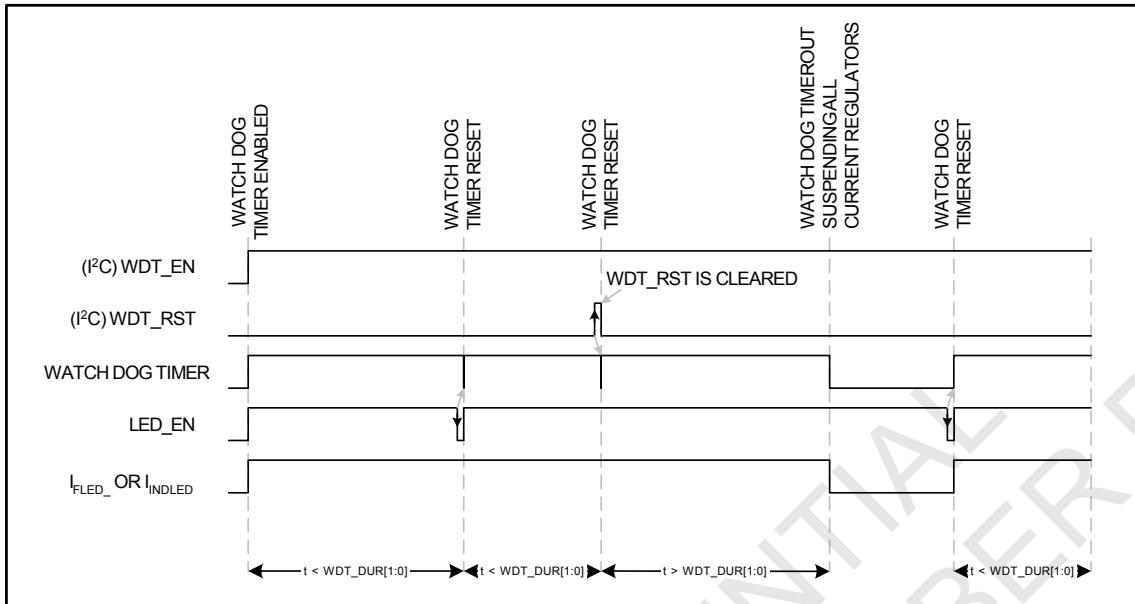


Figure 40 Watch dog timer timing diagram 1

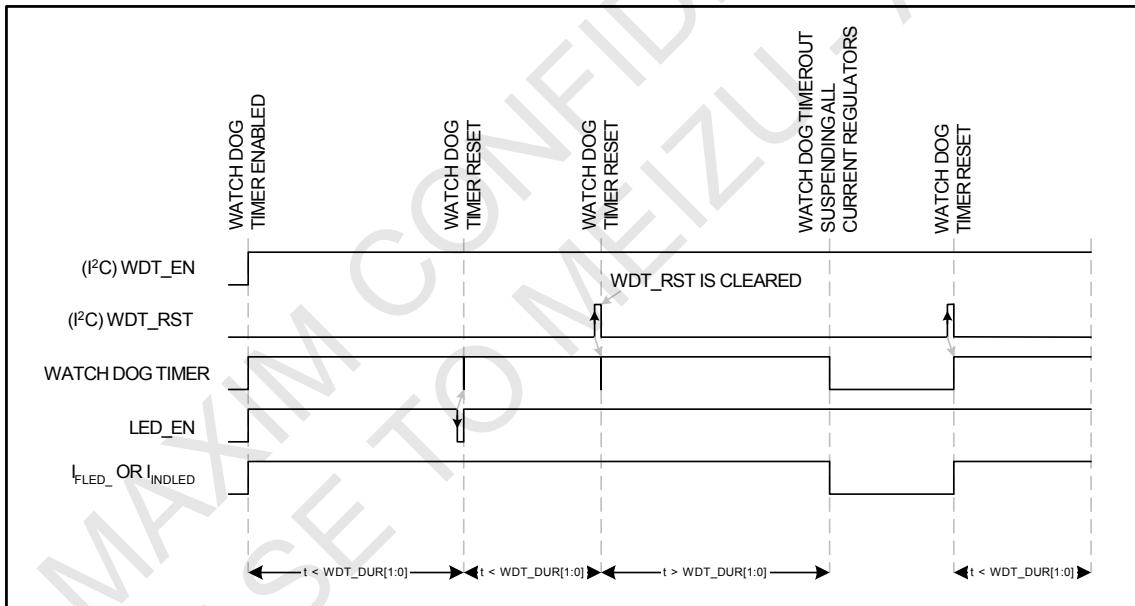


Figure 41 Watch dog timer timing diagram 2

12.6 GSM Blank Function (GSMB)

The GSMB input is provided to allow the Flash current to be momentarily reduced during a GSM transmit in order to reduce peak current draw from the battery. The current regulator value for FLED1 and FLED2 during a GSM transmit is programmed only for the Flash mode current using the GSMB_CUR register.

To use this feature connect the logic signal used to enable the PA, or equivalent, to the GSMB input. Assertion of this signal does not change the current status of the Flash Safety timer , but it does change the flash (or movie) current values stored in the I2C registers. Once the signal is de-asserted the current drivers will revert back to their previously programmed values. Polarity of this signal is controlled via bit 6 in the GSMB_CUR register (default is active high).

12.7 MAXFLASH Function

During high current loads of a battery cell, the battery voltage will momentarily drop due to the internal ESR of the battery, together with serial impedance from the battery to the load. For equipment requiring a minimum battery voltage for stable operation, the ESR of the battery needs to be calculated in order to estimate maximum current that can be drawn from the battery without making the battery cell voltage drop below this critical threshold. Due to the complicated measurement of the battery ESR, the Max8966/Max8997 Flash LED Driver features the MAXFLASH function to prevent the battery voltage from dropping below the threshold voltage.

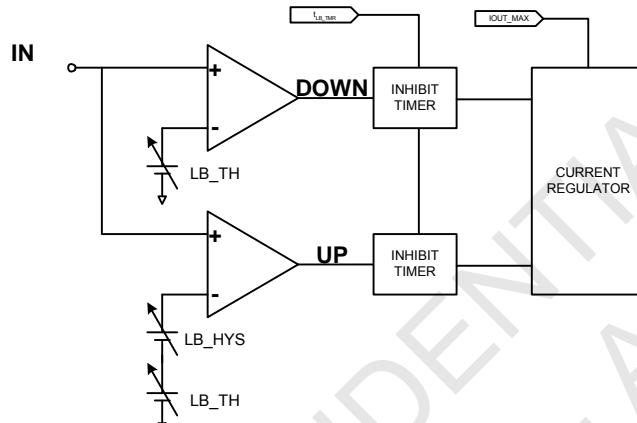


Figure 42 Block diagram of MAXFLASH function

When the MAXFLASH function is enabled, the input battery voltage is monitored during FLASH mode operation of the FLED1/FLED2 current regulators. If the input battery voltage drops below a pre-defined threshold level (LB_CNTL[4:0]), it indicates that the FLED1/FLED2 current regulators are drawing more current than the battery can support. As a reaction, the FLED1/FLED2 current regulators start reducing their pre-defined output current settings by one current step. Therefore, the current load on the battery is reduced and the input battery voltage starts to rise due to the internal battery ESR. The MAXFLASH function will then wait for a pre-defined inhibit period (LB_TMR[2:0]) before monitoring of the input battery voltage is resumed. If the input battery voltage is still below the threshold (V_{LB_TH}), then the current regulator output currents will be reduced by one step again unless the current regulator output currents are already set to their minimum available current setting. If the input battery voltage rises above the threshold (V_{LB_TH}) by a pre-defined hysteresis level (LB_HYS[1:0]), then current regulator output currents will be increased by one step unless the current regulator output currents are already set to their pre-defined current settings. While the input battery voltage stays above the threshold (V_{LB_TH}) by a value less than the hysteresis level (V_{LB_HYS}), the current regulator output currents are maintained at their reduced value. If hysteresis (V_{LB_HYS}) is disabled (LB_HYS[1:0] set to 11), then the current regulator output currents can only be reduced.

The MAXFLASH function is automatically disabled while the GSMB pin is asserted indicating that a GSM transmit is in progress. During a GSM transmit, the FLASH mode current setting of the FLED1/FLED2 current regulators is defined by the GSMB_CUR register.

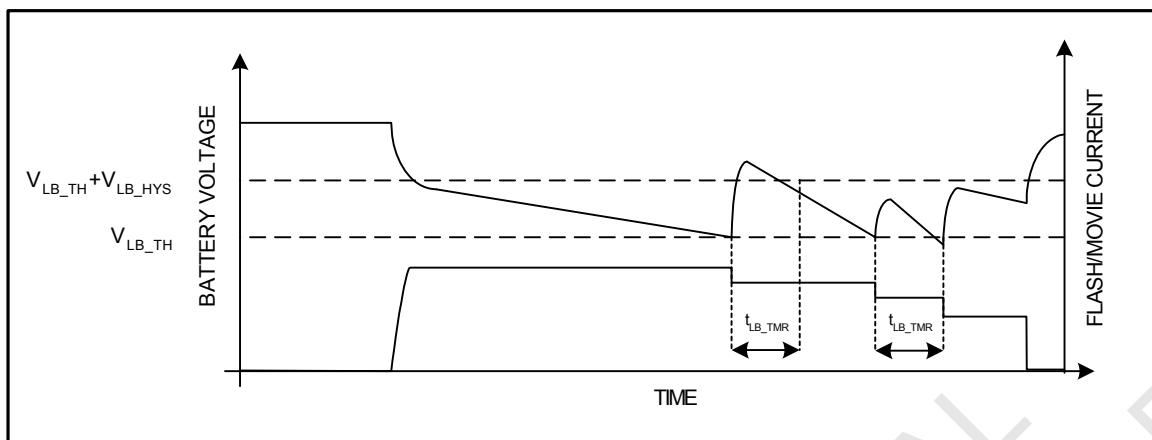


Figure 43 Example 1 of MAXFLASH function operation

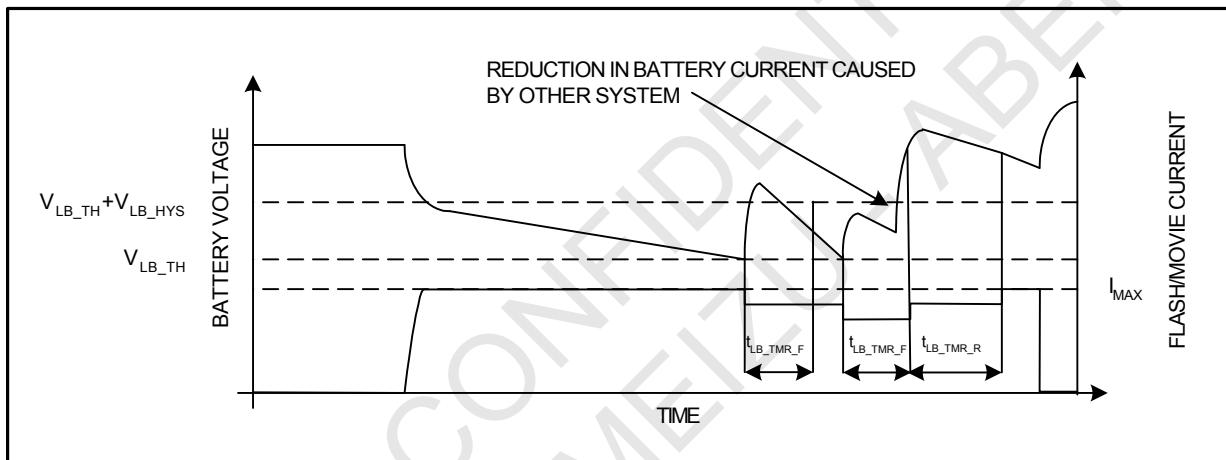


Figure 44 Example 2 of MAXFLASH function operation

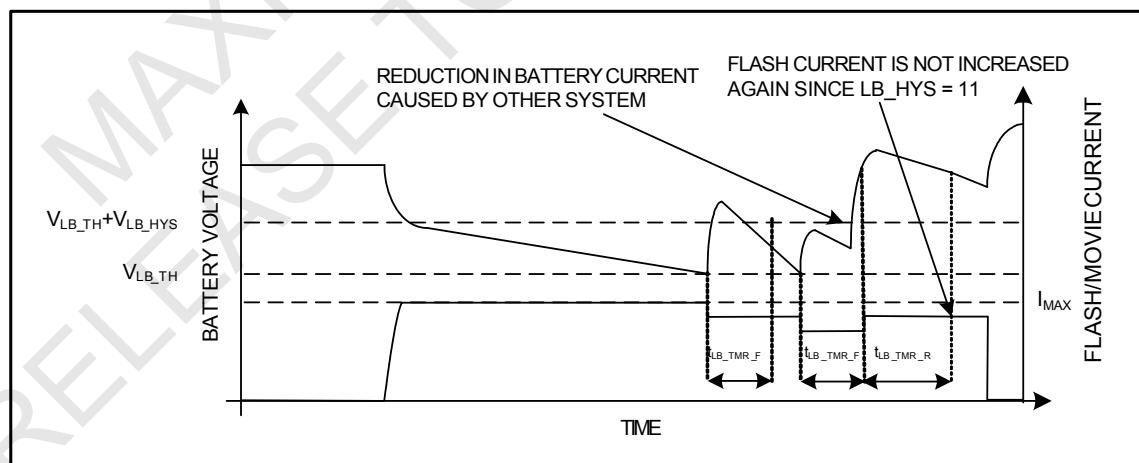


Figure 45: Example 3 of MAXFLASH Function (Hysteresis Disabled)

12.8 Soft-Start

The Step-Up Converter soft-starts by charging the capacitor on the COMP pin (C_{COMP}) with an internal $10\mu A$ (typ) current source. During this time, the internal NFET switch is switching at the minimum duty cycle. Once the voltage on the COMP pin rises above $750mV$ (typ), the switching duty cycle increases until the output voltage of the Step-Up converter reaches the desired regulation level. The COMP is discharged to GND with a 120Ω internal resistor during drop-out mode operation of the Step-Up Converter.

12.9 True Shutdown

In shutdown, the input supply current is reduced to $0.1\mu A$ (typ). The capacitor on the COMP pin (C_{COMP}) is discharged to GND with a 120Ω internal resistor whenever the Step-Up converter is disabled allowing the device to re-initiate a soft-start whenever it is re-enabled. The internal NFET switch and synchronous rectifier are both high impedance when the Step-Up converter is disabled. The LED current regulators are also high impedance in shutdown.

12.10 Parallel Connection of Current Source Regulators

The FLED_{_} current drivers can be connected in parallel as long as the system software properly sets the current regulator values for each driver. Unused current drivers may be tied to ground. The FLED_{_} regulators must be disabled via I²C to avoid a fault detection from an open or short.

12.11 Open/Short Detection

6 comparators are included to detect open or shorted LEDs on the FLED1 and FLED2 pins. One comparator on each LED pin detects when the voltage falls below the dropout voltage, indicating a shorted LED fault. Another comparator on each pin detects when the voltage rises above $V_{OUT} - 1V$, indicating an open LED fault. The fault detection comparators are enabled only when the corresponding current regulator is enabled and will provide a continuous monitor of the current regulator conditions. Once a fault is detected, each comparator provides a single bit output (1=Fault, 0= No Fault) corresponding to the appropriate LED pin.

If a open/short is detected, the current regulator is disabled and the status is latched into the fault register. This allows the processor to determine the operation condition of the LED driver.

12.12 Thermal Shutdown

Thermal shutdown limits the total power dissipation due to operation of the MAX8966/MAX8997 flash LED driver. When the junction temperature exceeds $160^{\circ}C$ (typ), the MAX8966/MAX8997 flash LED driver shuts down allowing the IC to cool. The MAX8966/MAX8997 flash LED driver turns on again when the junction temperature cools by $20^{\circ}C$. This results in a pulsed output of the Step-Up converter during continuous thermal overload conditions. A fault bit in the status register is set indicating that a thermal overload event occurred.

12.13 PCB Layout Guide for Flash LED Driver

The most noisy source of Flash converter is the loop between output (OUTF) and Flash Ground (FGND). The output capacitor plays very important role to reduce the switching noises. A ceramic capacitor is recommended for the output capacitor. Place the output capacitor cloaser to Max8966/Max8997 to minimize the current loop between PMIC and the output capacitor.

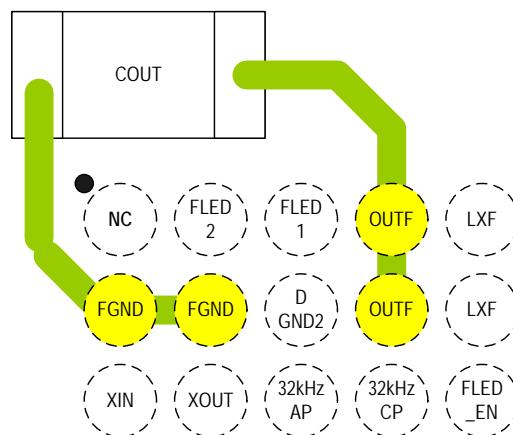


Figure 46 Flash LED Boost Converter Layout Guide

13 External Components

13.1 Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (μ H)	DC RESISTANCE (ohms typ)	CURRENT RATING (mA) -30% ($\Delta L/L$)	CURRENT RATING (mA) $\Delta T=40^\circ\text{C}$ rise	DIMENSIONS L x W x H (mm)
Toko	MDT2520-CR	1.0	0.06	800	1550	2.5 x 2.0 x 1.0
		1.5	0.08	1200	1400	
	DE2810C Flat Wire	1.5	0.06	1500	2000	3.0 x 2.8 x 1.0
		2.2	0.085	1300	1600	
		3.3	0.130	1050	1300	
		4.7	0.180	860	1100	
	DE2812C Flat Wire	1.5	0.050	2100	2600	3.0 x 2.8 x 1.2
		2.0	0.067	1800	2300	
		3.3	0.100	1400	1700	
		4.7	0.130	1200	1500	
Hitachi-Metals	KSLI-252010AG	1	0.050	600	2600	2.5 x 2.0 x 1.0
		2.2	0.100	800	1800	
Murata	LQM2HP_G0	1.0	0.055	1200	150	2.5 x 2.0 x 1.0
	LQM2MP	1.0	0.085	1100	1400	2.0 x 1.6 x 1.0
		2.2	0.110	600	1200	
		3.3	0.120	150	1200	
TDK	MLP2520S2R2M	2.2	0.090	700	1000	2.5 x 2.0 x 1.0
	MLP2520S_S	1.0	0.080	1500	1500	2.5 x 2.0 x 1.2
		2.2	0.110	900	1200	2.5 x 2.0 x 1.2
Samsung Electro- Mechanics	CIG22L1R0MNE	1.0	0.060		1500	2.5 x 2.0 x 1.0
	CIG22L2R2MNE	2.2	0.080		1300	2.5 x 2.0 x 1.0
	CIG22L3R3MNE	3.3	0.100		1200	2.5 x 2.0 x 1.0
	CIG22L4R7MNE	4.7	0.110		1100	2.5 x 2.0 x 1.0
	CIG22H1R0MNE	1.0	0.10	1.75	1500	2.5 x 2.0 x 1.2
	CIG22H2R2MNE	2.2	0.14	1.53	1200	2.5 x 2.0 x 1.2
	CIG22H3R3MNE	3.3	0.16	0.80	1000	2.5 x 2.0 x 1.2
	CIG22H4R7MNE	4.7	0.28	0.80	800	2.5 x 2.0 x 1.2

Table 4 Inductor selection guide

13.2 Output Capacitor Selection

The output capacitor, C_{BUCK} , is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{BUCK} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to

the unique feedback network, the output capacitance can be very low. For most applications a $2.2\mu\text{F}$ capacitor is sufficient. For optimum load-transient performance and very low output ripple, the output capacitor value in μF 's should be equal or larger than the inductor value in μH 's.

13.3 Input Capacitor Selection

The input capacitor, C_{IN3} , reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the MAX8966/MAX8997 step-down converter's fast soft-start, the input capacitance can be very low. For most applications a $4.7\mu\text{F}$ capacitor is sufficient.

14 GPIOs

Each GPIO has configurable Read/Write (R/W) registers allowing host processor/internal micro processor to program the functionality of each GPIO pin independent of the other GPIO pins. All GPIOs can be configured as digital input/output. Additionally each GPIO can be configured as interrupt input source. When GPIO's interrupt feature is enabled, User can set which edge is used as trigger source and set which internal interrupt bus it connects to. Each GPIO can be configured to have either pull-up resistors or pull-down registers. Nominal pull-up resistor and pull-down resister value will be 100K.

The GPIO inputs may also be used to trigger interrupts to the system controller, or may be masked out. The edge(s) that triggers interrupts are selectable. When a GPIO input interrupt is enabled, and the selected edge(s) are detected, the corresponding bit is set in the GPIOINT register, bit D4 is set in the 1st level Interrupt register, and the external interrupt signal nIRQ1 is asserted. The 2nd level interrupt bit is set by the interrupt event. The 1st level interrupt bit is asserted (by the logical OR of the 2nd level bits).The nIRQ1 pin signal is asserted (by the logical OR of the 1st level interrupt bits). When the Processor recognizes the nIRQ1pin is asserted, it reads the 1st level interrupt register. The 1st level interrupt register contains the groupings (2nd levels) with active interrupts. The Processor then reads the 2nd level interrupts for which the interrupt bit in the 1st level was asserted. When the 2nd level interrupt location is successfully read, then the interrupts set within that word are cleared. The nIRQ1 line deasserts when all active interrupts have been read (meaning all 2nd level interrupt bits are 0). When PR77Z-1Z GPIO interrupt event occurs, IRQ1 is pulled LOW.

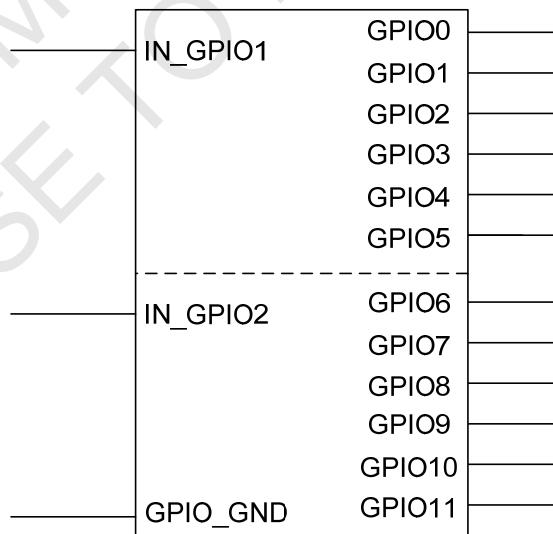


Figure 47 GPIO Block Diagram

15 FUEL GAUGE

The MAX8966/MAX8997 Fuel Gauge incorporates a Maxim ModelGauge m3 algorithm that combines the excellent short-term accuracy and linearity of a coulomb counter with the excellent long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry leading fuel-gauge accuracy. ModelGauge m3 cancels offset accumulation error in the coulomb counter, while providing better short-term accuracy than any purely voltage-based fuel gauge. Additionally, the ModelGauge m3 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time. The IC automatically compensates for aging, temperature, and discharge rate and provides accurate SOC in mHhr or % over a wide range of operating conditions. The device provides three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer.

The IC provides precision measurements of current, voltage, and temperature. Temperature of the battery pack is measured using an external thermistor supported by ratiometric measurements on an auxiliary input. A 2-wire(I2C) interface provides access to data and control registers.

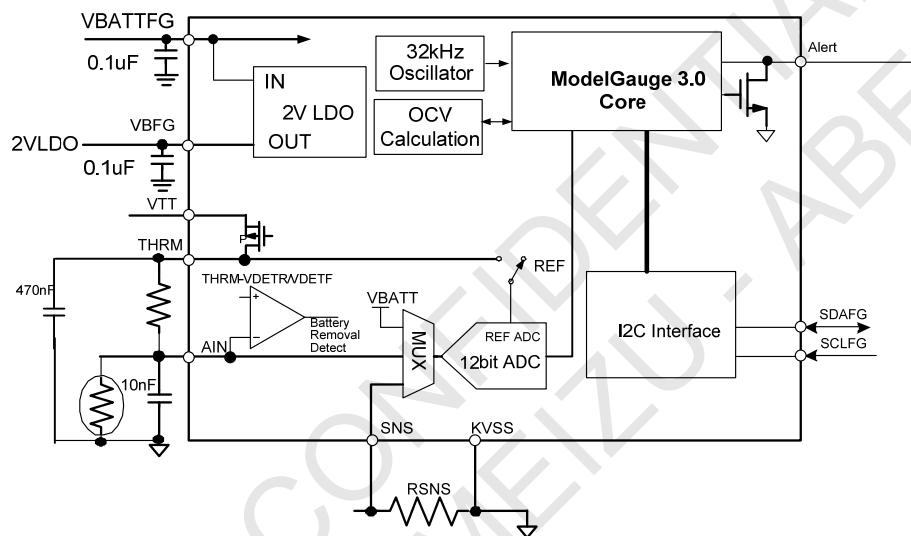


Figure 48 Fuel Gauge Block Diagram

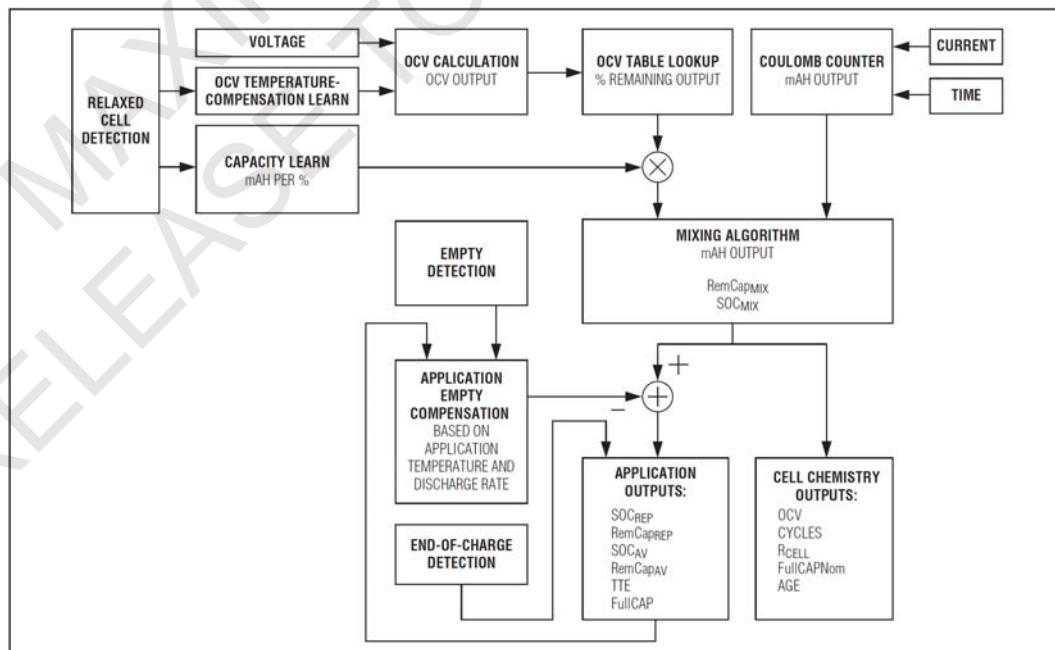


Figure 49 Model Gauge m3 Overview

The ModelGauge m3 algorithm combines a high-accuracy coulomb counter with a voltage fuel gauge. Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated, causes the reported capacity error to increase over time, and requires periodic corrections. Corrections are usually performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the true SOC based on the battery voltage after a long time of no current flow. Both have the same limitation: if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Classical voltage-measurement-based SOC estimation has poor accuracy due to inadequate cell modeling, but does not accumulate offset error over time. The device includes an advanced voltage fuel gauge, which estimates OCV, even during current flow, and simulates the nonlinear internal dynamics of an Li+ battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC based on table lookup. This OSC estimation does not accumulate offset error over time.

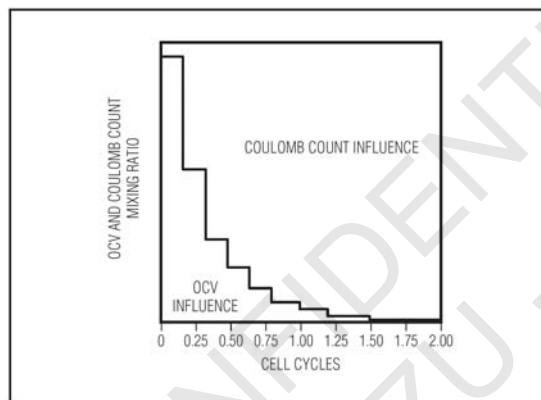


Figure 50 ModelGauge m3 OCV and Coulomb Count Mixing

The ModelGauge m3 algorithm combines a high-accuracy coulomb counter with a VFG. The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG while providing the strengths of both. A mixing algorithm weighs and combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way the VFG capacity result is used to continuously make small adjustments to the battery state, canceling the coulomb-counter drift.

The ModelGauge m3 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. The modelGauge m3 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the voltage-fuel-gauge dynamics adapt based on cell-voltage behavior in the application.

15.1 OCV Estimation and Coulomb Count Mixing

The core of the ModelGauge m3 algorithm is a mixing algorithm that combines the OCV capacity estimation with the coulomb counter. After power-on reset of the IC, coulomb-count accuracy is unknown. The OCV capacity estimation is weighted heavily compared to the coulomb-count output. As the cell progresses through cycles in the application, coulomb-counter accuracy improves and the mixing algorithm alters the weighting so that the coulomb-counter results are dominant. From this point forward, the OCV estimation output provides only microcorrections to the coulomb count to counteract the effects of offset and gain error in the current measurements.

The resulting output from the mixing algorithm does not suffer drift from current measurement offset error and is more stable than a standalone OCV estimation algorithm. Initial accuracy depends on the relaxation state of the cell. The highest initial accuracy is achieved with a fully relaxed cell.

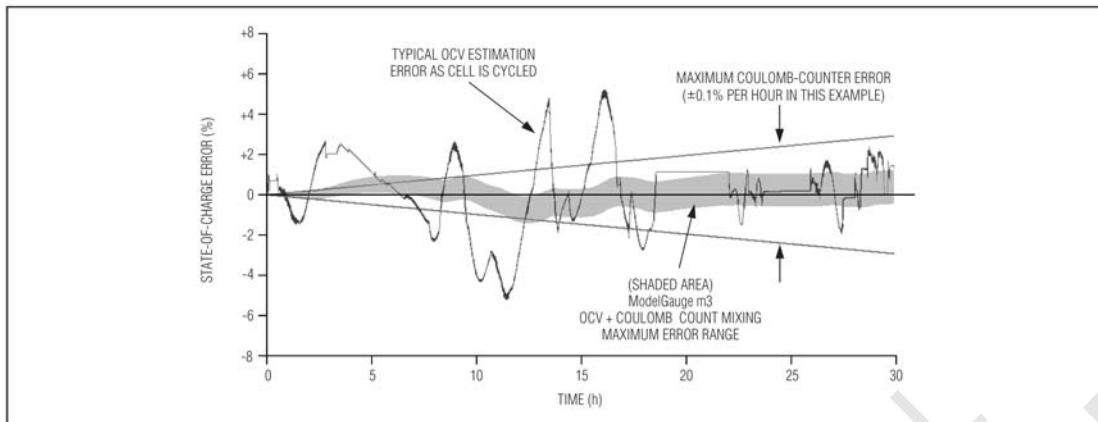


Figure 51 ModelGauge m3 typical Accuracy Example

15.2 Fuel Gauge Empty Compensation

As the temperature and discharge rate of an application changes, the amount of charge available to the application also changes. The ModelGauge m3 algorithm distinguishes between remaining capacity of the cell and remaining capacity to the application and reports both results to the user. The RemCapMIX output register tracks the charge state of the cell. This is the theoretical mAh of charge that can be removed from the cell under ideal conditions extremely low discharge current and no concern for cell voltage. This result is not affected by application conditions such as cell impedance or minimum operating voltage of the application. ModelGauge m3 continually tracks the expected empty point of the application in mAh. This is the amount of charge that cannot be removed from the cell by the application because of minimum voltage requirements and internal losses of the cell. The IC subtracts the amount of charge not available to the application from the RemCapMIX register and reports the result in RemCapAV.

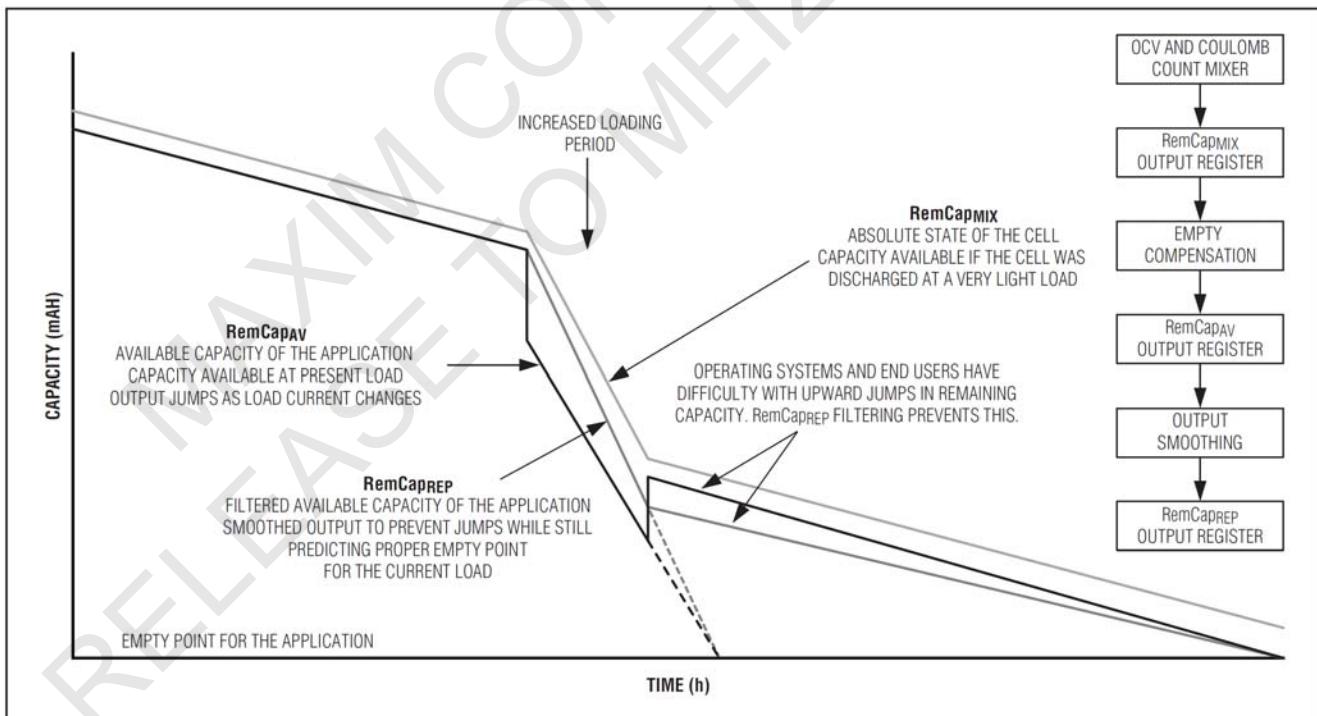


Figure 52 ModelGauge m3 Empty Compensation

Since available remaining capacity is highly dependent on discharge rate, the RemCapAV register can be subject to large instantaneous changes as the application load current changes. The result can increase, even while discharging, if the load current suddenly drops. This result, although correct, can be very counterintuitive to

the host software or end user. The RemCapREP output register contains a filtered version of RemCapAV that removes any abrupt changes in remaining capacity. RemCapREP converges with RemCapAV over time to correctly predict the application empty point while discharging or the application full point while charging.

15.3 Fuel-Gauge Learning

The IC periodically makes internal adjustment to cell characterization and application information to remove initial error and maintain accuracy as the cell ages. These adjustments always occur as small undercorrections to prevent instability of the system and prevent any noticeable jumps in the fuel-gauge outputs. Learning occurs automatically without any input from the host. To maintain learned accuracy through a power cycle, the host must periodically save learned information and then restore after the power cycle occurs.

- **Application Capacity (FullCap):** This is the total capacity available to the application at full. Through the user-defined registers, ICHGTerm and DesignCAP, the IC detects end-of-charge conditions as the cell is cycled. These points allow the IC to learn how much of the cell capacity is usable by the application depending on cell age and temperature.
- **Cell Capacity (FullCapNom):** This is the total cell capacity at full, according to the VFG. This includes some capacity that is not available to the application at high loads and/or low temperature. The IC periodically compares percent change based on OCV measurement vs. coulomb-count change as the cell charges and discharges. This information allows the IC to maintain an accurate estimation of the cell's capacity in mAh as the cell ages.
- **Voltage Fuel-Gauge Adaptation:** the IC observes the battery's relaxation response and adjusts the dynamics of the VFG.

15.4 Determining Fuel-Gauge Accuracy

To determine the true accuracy of a fuel gauge, as experienced by end users, the battery should be exercised in a dynamic manner. The end user accuracy cannot be understood with only simple cycles. To challenge a correction-based fuel gauge, such as coulomb counters, test the battery with partial loading sessions. For example, a typical use may operate the device for 10min and then stop using for an hour or more. A robust test method includes these kinds of sessions many times at various loads, temperatures, and duration. Refer to the Application Note 4799: Cell characterization Procedure for a ModelGauge m3 Fuel Gauge.

Typical Operating Circuit

The IC is designed to mount outside the cell pack that it monitors. Voltage of the battery pack is measured directly at the pack terminals by the VBATTFG and SNS connections. Current is measured by an external sense resistor placed between the SNS and KVSS pins. An external resistor-divider network allows the Fuel Gauge to measure temperature of the cell pack by monitoring the AIN pin. The THRM pin provides a strong pull-up for the resistor-divider that is internally disabled when temperature is not being measured. **A 470nF capacitor is recommended between THRM and KVSS.**

Communications to the host occurs over a standard I₂C interface. SCLFG is an input from the host, and SDAFG is an open-drain I/O pin that requires an external pull-up. The ALRT pin is an output that can be used as an external interrupt to the host processor if certain application conditions are detected. ALRT can also function as an input, allowing the host to shut down the Fuel Gauge. This pin is also open drain and requires an external pull-up resistor.

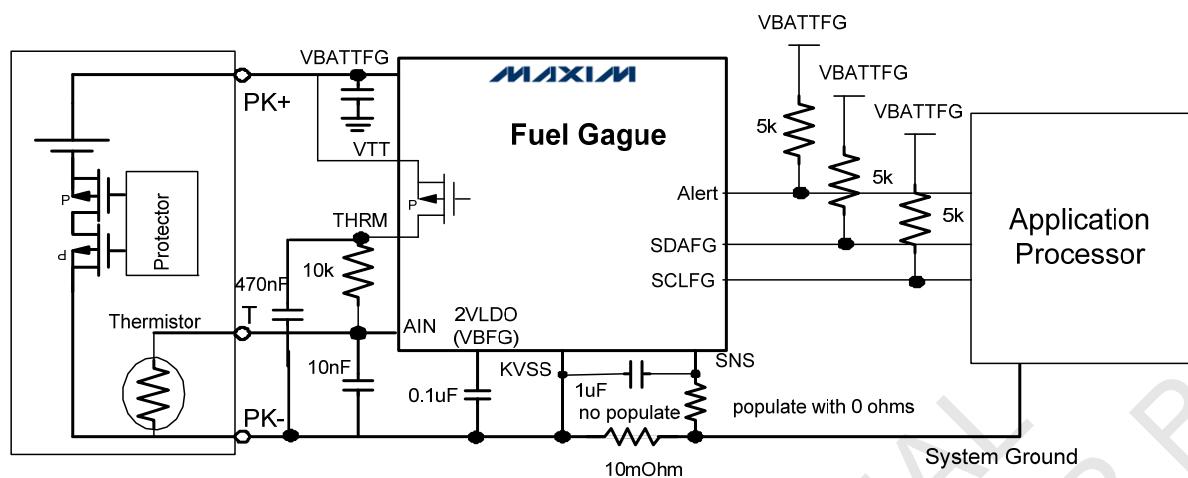


Figure 53 Typical Application Circuit for ModelGauge m3 operation.

15.5 ModelGauge m3 Registers

To calculate accurate results, ModelGauge m3 requires information about the cell, the application, and real-time information measured by the IC. The below Figure shows all inputs and outputs to the algorithm grouped by category. Analog input registers are the real-time measurements of voltage, temperature, and current performed by the IC. Application-specific registers are programmed by the customer to reflect the operation of the application. The Cell Characterization Information registers hold characterization data that models the behavior of the cell over the operating range of the application. The Algorithm Configuration registers allow the host to adjust performance of the IC for their application. The Save and Restore registers allow an application to maintain accuracy of the algorithm after the IC has been power cycled.

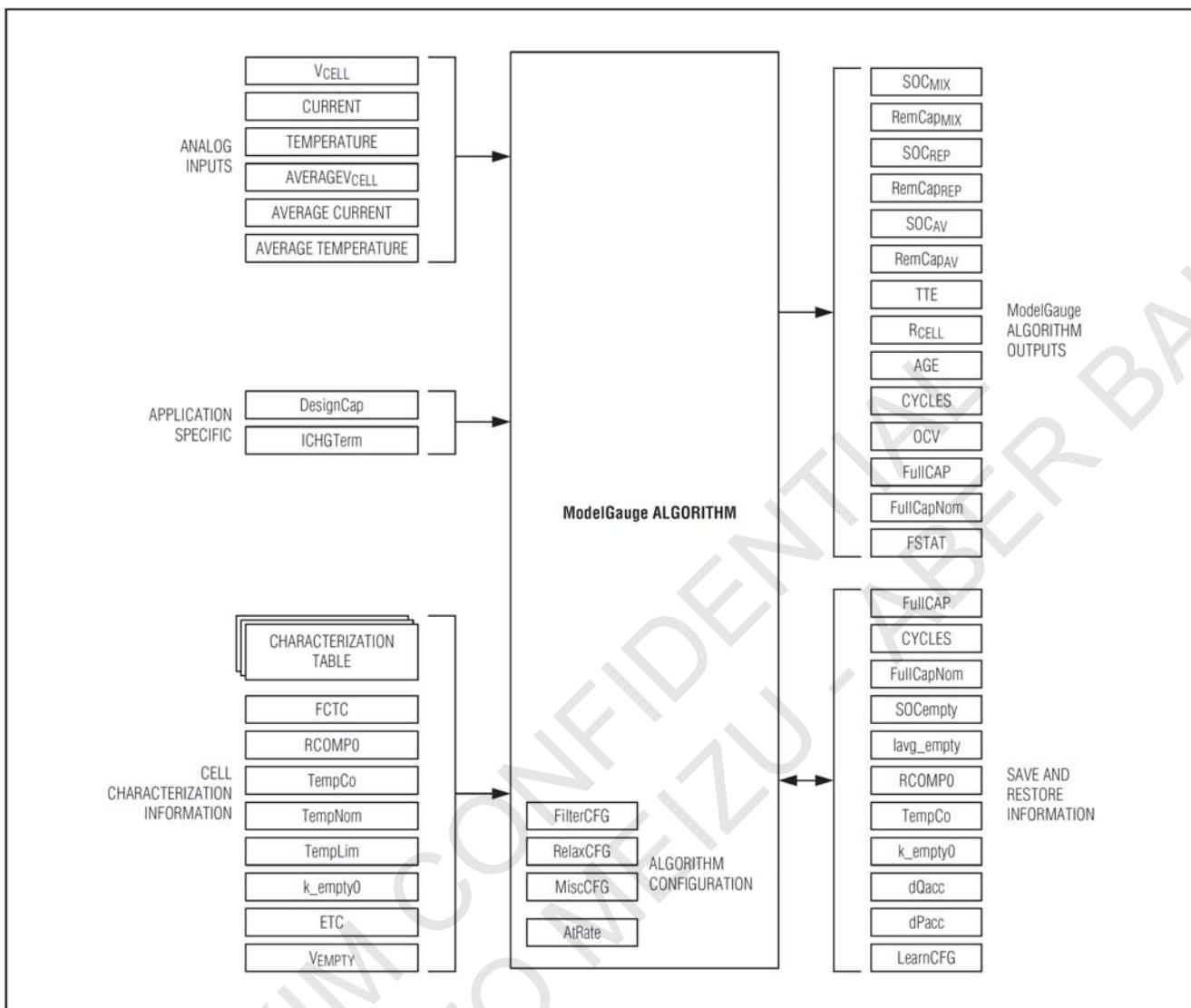


Figure 54 ModelGauge m3 Register Map

15.6 POWER MODES

The MAX8966/MAX8997 Fuel Gauge operates in one of two power modes: active and shutdown. While in active mode, the MAX8966/MAX8997 Fuel Gauge operates as a high-precision battery monitor with temperature, voltage, auxiliary inputs, current and accumulated current measurements acquired continuously and the

resulting values updated in the measurement registers. READ and WRITE access is allowed only in active mode.

In shutdown mode, the internal LDO of Fuel Gauge shuts down and all activity stops, although **volatile RAM remains preserved**. There are several options for entering shutdown:

Entering Shutdown:

- Write SHDN=1 through I2C interface, wait for longer than SHDNTIMER.
- Pack removal detected for longer than SHDNTIMER (if AINSH=1)
- I2C lines both persist low for longer than SHDNTIMER time (if I2CSH=1)
- Power Fail warning for longer than SHDNTIMER (ADC conversion < V_{PFW}, if PSH=1)
- Alert line is externally driven low for longer than SHDNTIMER (if ALSH=1 and ALRTp=1)
- Alert line is externally driven high for longer than SHDNTIMER (if ALSH=1 and ALRTp=0)

These shutdown entry modes are all programmable according to application. Shutdown events are gated by the SHDNTIMER, which allows a long delay between the shutdown event and the actual shutdown. By behaving this way, the firmware can take the best reading of the relaxation voltage.

Exiting Shutdown:

- Any edge on SCL/SDA if I2CSH=1 (stale data available 2 ms after edge, new data available after 178ms)
- Any edge on ALRT line if ALSH=1 (stale data available 2 ms after edge, new data available after 178ms)
- Power cycled at VBATT

15.7 I2C Protocol for Fuel Gauge

The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitoring the acknowledge bit for presence of the Fuel Gauge. More complex formats such as The write, Data, read Data and Function command protocols write data, read data and execute device specific operations. All bytes in each command format require the slave or the host system to return an Acknowledge bit before continuing with the next byte. Each function command definition outlines the required transaction format. The following key applies to the transaction formats.

Table 7: Protocol Key

KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave Address (7-bit)	W	R/W bit = 0
FCmd	Function Command byte	R	R/W bit = 1
MAddr	Memory Address byte	P	STOP bit
Data	Data byte written by master	Data	Data byte returned by slave
A	Acknowledge bit - Master	A	Acknowledge bit - Slave
N	No Acknowledge - Master	N	No Acknowledge - Slave

15.7.1 Basic Transaction Formats

write: S SAddr W A MAddr A DataL A DataH A P

A write transaction transfers one or more data bytes to the FUEL GAUGE. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the Acknowledge cycles.

read: S SAddr W A MAddr A Sr SAddr R A DataL A DataH N P

A read transaction transfers one or more words from the FUEL GAUGE. read transactions are composed of two parts, A write portion followed by A read portion, and is therefore inherently longer than A write transaction. The

write portion communicates the starting point for The read operation. The read portion follows immediately, beginning with a Repeated START, Slave Address with R/W set to a “1”. Control of SDA is assumed by the FUEL GAUGE beginning with the Slave Address Acknowledge cycle. Control of the SDA signal is retained by the FUEL GAUGE throughout the transaction, except for the Acknowledge cycles. The master indicates the end of A read transaction by responding to the last byte it requires with a No Acknowledge. This signals the FUEL GAUGE that control of SDA is to remain with the master following the Acknowledge clock.

15.7.2 Write Data Protocol

The write data protocol is used to write to register and shadow RAM data to the FUEL GAUGE starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1 and DataN represents the last data byte, written to MAddr + N. The master indicates the end of A write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit.

S SAddr W A MAddr A DataL0 A DataH0 A DataL1 A DataH1 A ... DataLN A DataHN A P

The MSB of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the least significant bit (LSB) of each byte is received by the FUEL GAUGE, the MSB of the data at address MAddr + 1 is can be written immediately after the acknowledgement of the data at address MAddr. If the bus master continues an auto-incremented write transaction beyond address 4Fh, the FUEL GAUGE ignores the data. Data is also ignored on writes to read-only addresses and reserved addresses, locked OTP blocks as well as A write that auto increments to the Function Command register (address FEh). Incomplete bytes and bytes that are Not Acknowledged by the FUEL GAUGE are not written to memory. As noted in the Memory Section, writes to unlocked OTP blocks modify the shadow RAM only.

15.7.3 Read Data Protocol

The read Data protocol is used to read register and shadow RAM data from the FUEL GAUGE starting at memory address specified by MAddr. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1 and DataN represents the last byte read by the master.

S SAddr W A MAddr A Sr SAddr R A DataL0 A DataH0 A DataL1 A DataH1 A ... DataLN N DataHN N P

Data is returned beginning with the most significant bit (MSB) of the data in MAddr. Because the address is automatically incremented after the least significant bit (LSB) of each byte is returned, the MSB of the data at address MAddr + 1 is available to the host system immediately after the acknowledgement of the data at address MAddr. If the bus master continues to read beyond address FFh, the FUEL GAUGE outputs data values of FFh. Addresses labeled “Reserved” in the memory map return undefined data. The bus master terminates The read transaction at any byte boundary by issuing a No Acknowledge followed by a STOP or Repeated START.

15.7.4 Function Command Protocol

The Function Command protocol executes a device specific operation by writing one of the function command values (FCmd) to memory address FEh. Table 5 lists the FUEL GAUGE FCmd values and describes the actions taken by each. A one byte write protocol is used to transmit the function command, with the MAddr set to FEh and the data byte set to the desired FCmd value. Additional data bytes are ignored. Data read from memory address FEh is undefined.

S SAddr W A MAddr=0FEh A FCmd A P

Table 8: Function commands

FUNCTION COMMAND	TARGET OTP BLOCK	FCMD VALUE	DESCRIPTION
Recall Data	0	B2h	This command recalls the contents of the targeted OTP block to its shadow RAM.
	1	B4h	

15.8 How to use ModelGauge as m1 (operation without current sense resistor)

The fuel gauge may be operated as a model gauge without a current sense resistor. This session describes the start up sequence to configure and utilize the fuel gauge function when application does not use a current sense resistor. The FuelGauge should be initialized and then loaded with a customized model and parameters at power up and then the Reported State of Charge and other useful information can be easily read by the host system over the 2-Wire Bus System and displayed to the user. Figure below is a flowchart of the power up sequence that a host controller should implement with the FuelGauge.

HARDWARE CONFIGURATION – Remove the external sense resistor and ground the SNS pin.

ALERTS – If the host wishes to generate alerts based on ModelGauge 1 State of Charge, the SOC alert configuration bits located in the MiscCFG register (2Bh) should be written to 11b.

External Temperature

ModelGauge1 can operate without an external thermistor if the host software supplies the application temperature to the algorithm. In this configuration, the external thermistor is removed from the circuit (AIN can float or is grounded) and the Tex bit in the CONFIG register (1Dh) is set to a 1. Host software is then responsible for updating the Temperature register (08h) over the I2C bus. Failure to maintain an accurate up-to-date temperature value will create error in the ModelGauge 1 SOC calculation.

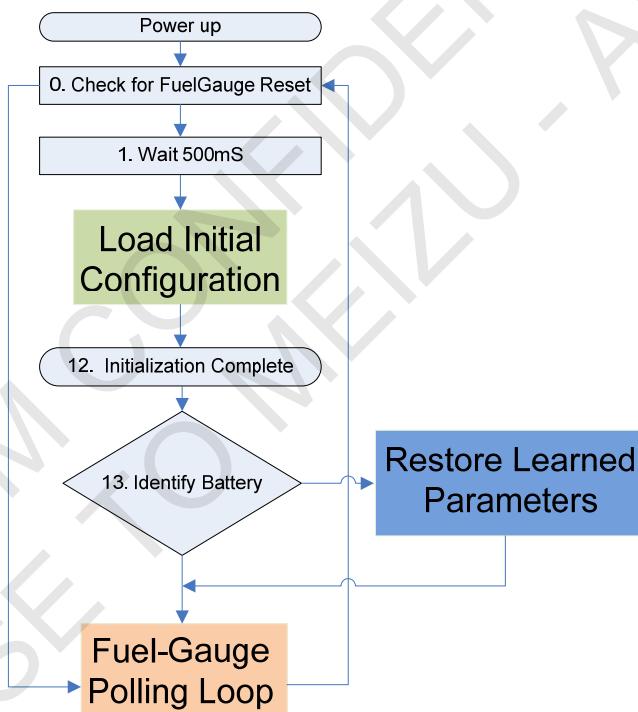


Figure 55 FuelGauge m1 Implementation Sequence

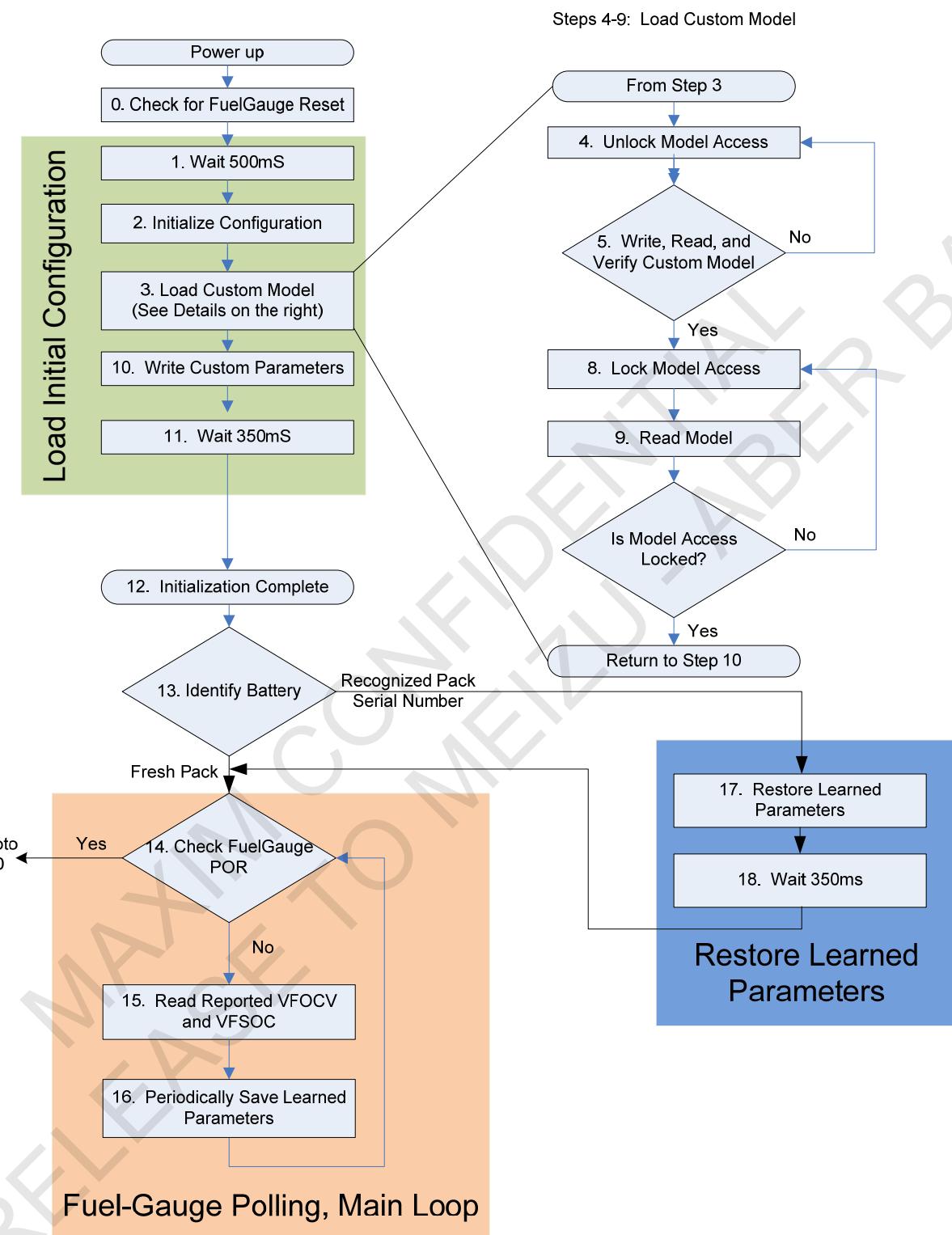


Figure 56 Detailed Flowchart of Power up Sequence for FuelGauge m1 operation (operation without current sense).

Initialize registers to recommended Configuration

The FuelGauge should be initialized prior to being used. The following three registers should be written to these values in order for the FuelGauge to perform at its best. These values are written to RAM, so they must be written to the device any time that power is applied or restored to the device. Some registers are updated internally, so it is necessary to verify that the register was written correctly to prevent data collisions.

0. Check for POR

The POR bit is bit 1 of the Status Register.

Status = ReadRegister(0x00h) //Read Status

If POR=0, then go to Step 16.

If POR=1, then do Steps 1-15.

1. Delay 500ms

After Power up, the FuelGauge requires 500mS in order to perform signal debouncing and initial VFSOC reporting.

2. Initialize Configuration

WriteRegister (0x1Dh, 0x2210h) //Write CONFIG

Load custom model and Parameters

The custom model that is stored in the FuelGauge is also written to RAM and so it must be written to the device any time that power is applied or restored to the device. When the device is powered on, the host software must first unlock write access to the model, write the model, verify the model was written properly, and then lock access to the model. After the model is loaded correctly, simply write a few registers with customized parameters that will be provided by Maxim.

4. Unlock Model Access

To unlock access to the model the host software must write the following:

WriteRegister (0x62h, 0x0059h) //Unlock Model Access
WriteRegister (0x63h, 0x00C4h)

5. Write/Read/Verify the Custom Model

Once the model is unlocked, the host software must write the 48 word model to the FuelGauge. The model is located between memory locations 0x80h and 0xAFh.

//Actual bytes to transmit will be provided by Maxim after cell characterization

Write16Registers (0x80h)

Write16Registers (0x90h)

Write16Registers (0xA0h)

The model can be read directly back from the FuelGauge. So simply read the 48 words of the model back from the device to verify if it was written correctly. If any of the values do not match, re-write the model to the device.

Read16Registers (0x80h)

Read16Registers (0x90h)

Read16Registers (0xA0h)

8. Lock Model Access

To lock access to the model the host software must write the following:

WriteRegister (0x62h, 0x0000h) //Lock Model Access
WriteRegister (0x63h, 0x0000h)

9. Verify the Model Access is locked

If the model remains unlocked, the FuelGauge will not be able to monitor the capacity of the battery. Therefore it is very critical that the Model Access is locked. To verify it is locked, simply read back the model as in Step 5.

However, this time, all values should be read as 0x00h. If any values are non-zero, repeat Step 8 to make sure the Model Access is locked.

10. Write Custom Parameters

Five additional registers should be written in this step with values that are provided by Maxim.

```
WriteAndVerifyRegister (0x38h, RCOMP0)      //Write and Verify RCOMP0
WriteAndVerifyRegister (0x39h, TempCo)        //Write and Verify TempCo
```

11. Delay at least 350mS

This delay must be at least 350mS to allow VFSOC to be calculated from the new configuration.

12. Initialization Complete

Clear the POR bit to indicate that the custom model and parameters were successfully loaded.

```
Status = ReadRegister(0x00h)                //Read Status
WriteAndVerifyRegister (0x00h, Status AND 0xFFFFDh) //Write and Verify Status with POR bit Cleared
```

13. Identify Battery

If the host recognizes the battery pack as one with a saved history, go to Step 18 to restore all of the saved parameters, otherwise continue to Step 15.

Monitor the Battery

Once the FuelGauge is initialized and customized, the host can simply read the desired information from the FuelGauge and display that information to the user. Figure 3 shows the flow to read the Reported Capacity, Reported State of Charge, and the Time to Empty.

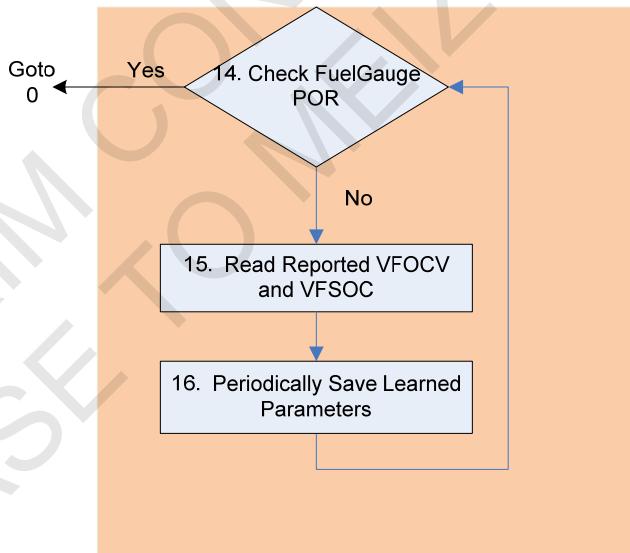


Figure 57 Flowchart of Fuel-Gauge Polling Loop for the FuelGauge

14. Check for FuelGauge Reset

```
Status = ReadRegister(0x00h)          //Read Status
If POR=0, then go to Step 16.
If POR=1, then go to Step 0.
```

read the Reported state of charge (SOC)

The FuelGauge automatically calculates and reports the state of charge of the cell in terms of percentage. The Voltage Fuelgauge State of Charge (VFSOC) ,as a percent, is read from memory location 0xFFh.

15. Read VFSOC

VFSOC = ReadRegister(0xFFh) //Read VFSOC

The VFSOC_HiByte has units 2% per LSB. The low byte reports fractional percent. This is the primary output and reports the State of Charge of the battery from the MG1 core.

16. Save Learned Parameters

It is recommended to save the learned parameters every time VFSOC changes by 64% so that if power is lost the values can easily be restored.

Saved_RCOMP0 = ReadRegister(0x38h) //Read RCOMP0
Saved_TempCo = ReadRegister(0x39h) //Read TempCo

ReSTORING Learned parameters

If power is lost, then the learned information can be easily restored with the following procedure.

17. Restore Learned Parameters

WriteAndVerifyRegister(0x38, Saved_RCOMP0) //WriteAndVerify RCOMP0
WriteAndVerifyRegister(0x39, Saved_TempCo) //WriteAndVerify TempCo

18. Wait 350mS

The FuelGauge requires that it be initialized and customized in order to provide the most accurate fuel gauging performance. Once the device is set up, then simply read and display the information that is most desired by the application

15.8.1 Typical Application Circuit for ModelGauge m1 Operation (without Current Sense)

The typical application circuit without a current sense resistor is shown below. A 470nF bypass capacitor is recommended between THRM and GND for noise immunity.

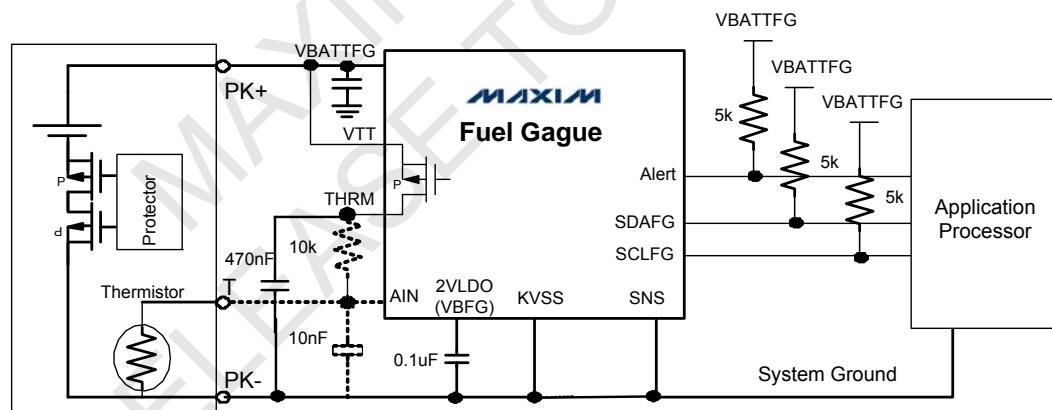
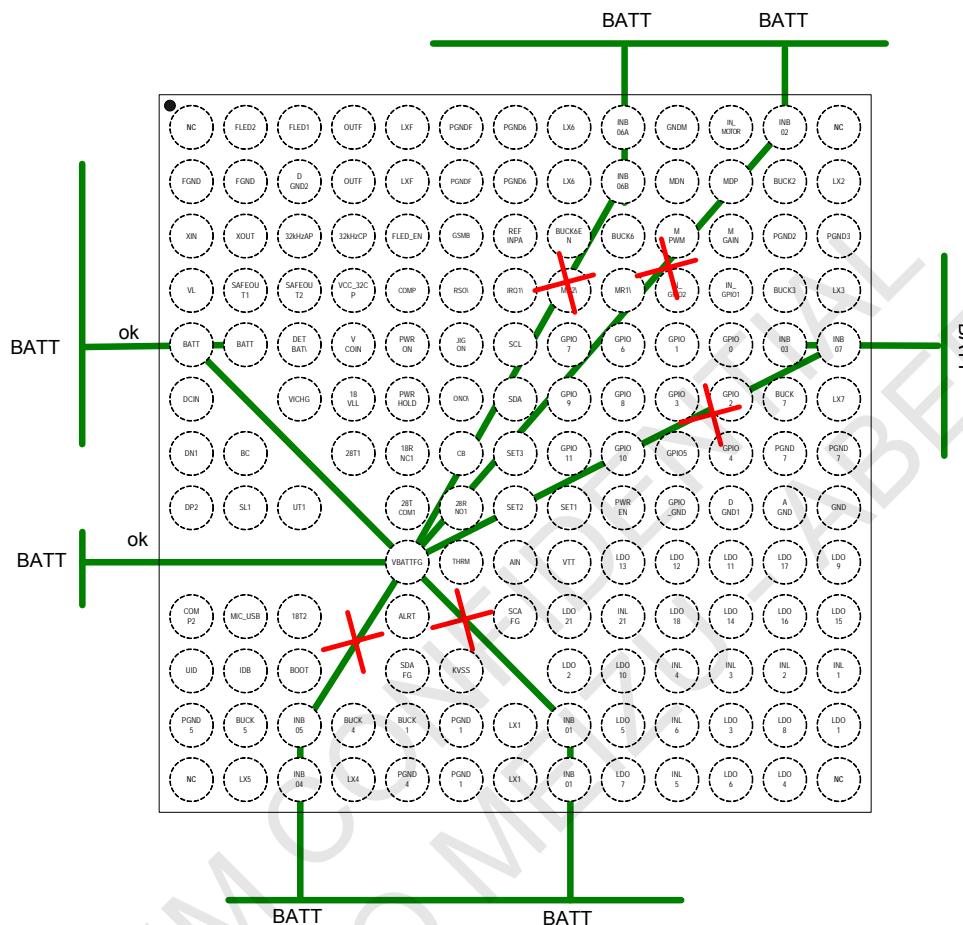


Figure 58 Typical Application Circuit for Model Gauge Operation without a current sense resistor

15.9 Fuel Gauge Layout Guide

15.9.1 VBATTFG

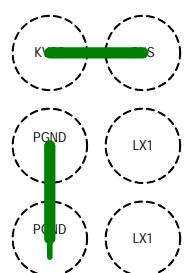
Avoid connecting VBATTFG to the buck input pin (INB0_). It is recommended to directly connect to BATT rail.



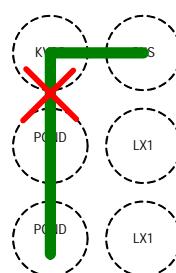
15.9.2 Ground Pins

Fuel Gauge Ground (KVSS and SNS) when SNS is not used as a current sense needs to be separated from PGND.

Recommended

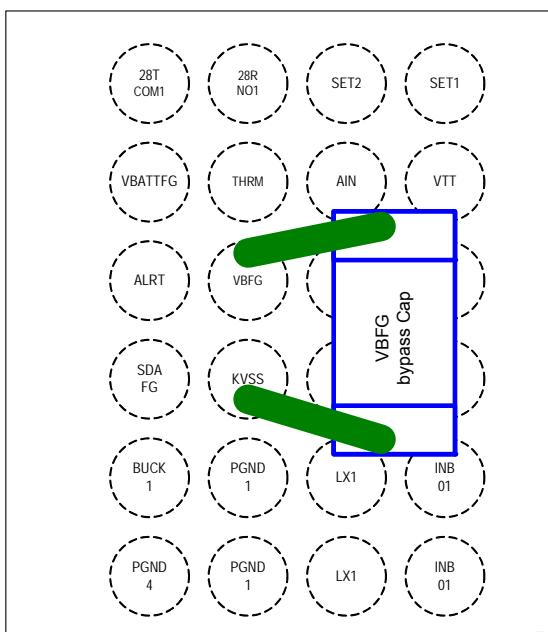


Not Recommended



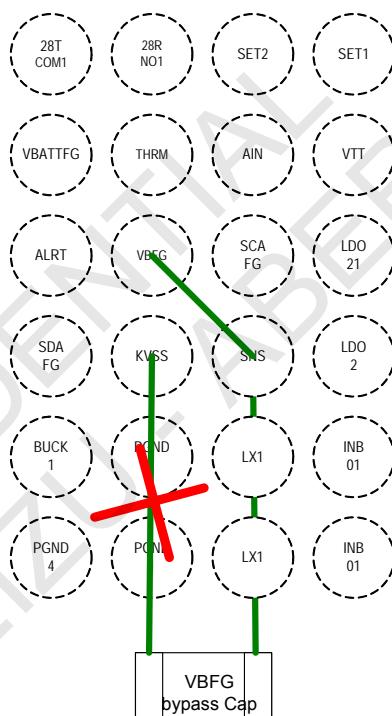
15.9.3 Bypass Capacitor of VBFG

It is recommended to place a bypass capacitor closer to IC (See figure below). If it is not possible to place the bypass capacitor to the other side of PCB through via holes, then avoid connecting the return ground path to any noise ground sources (PGND of buck or switching regulator).

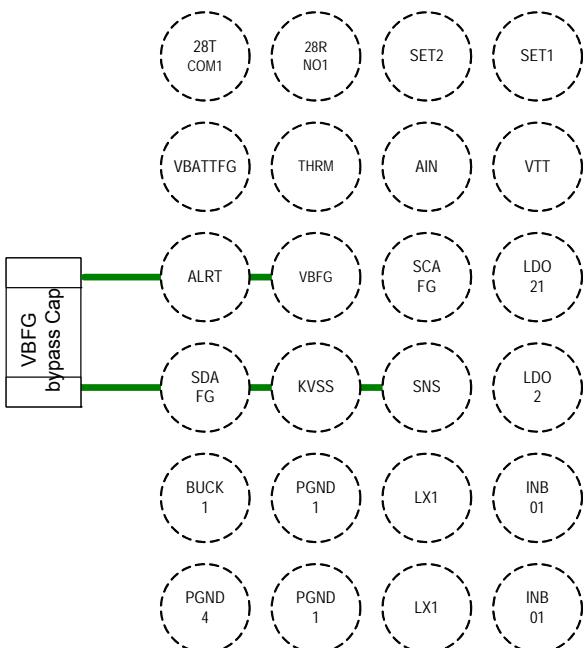


Place a VBFG bypass capacitor on the other side of the PCB through via.

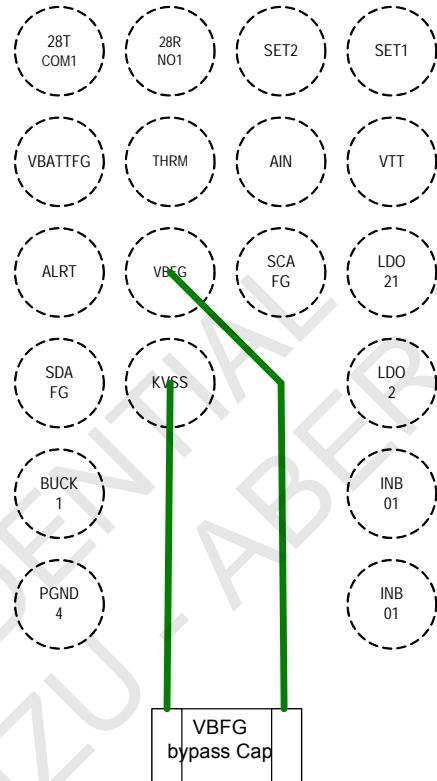
Not Recommended



Recommended



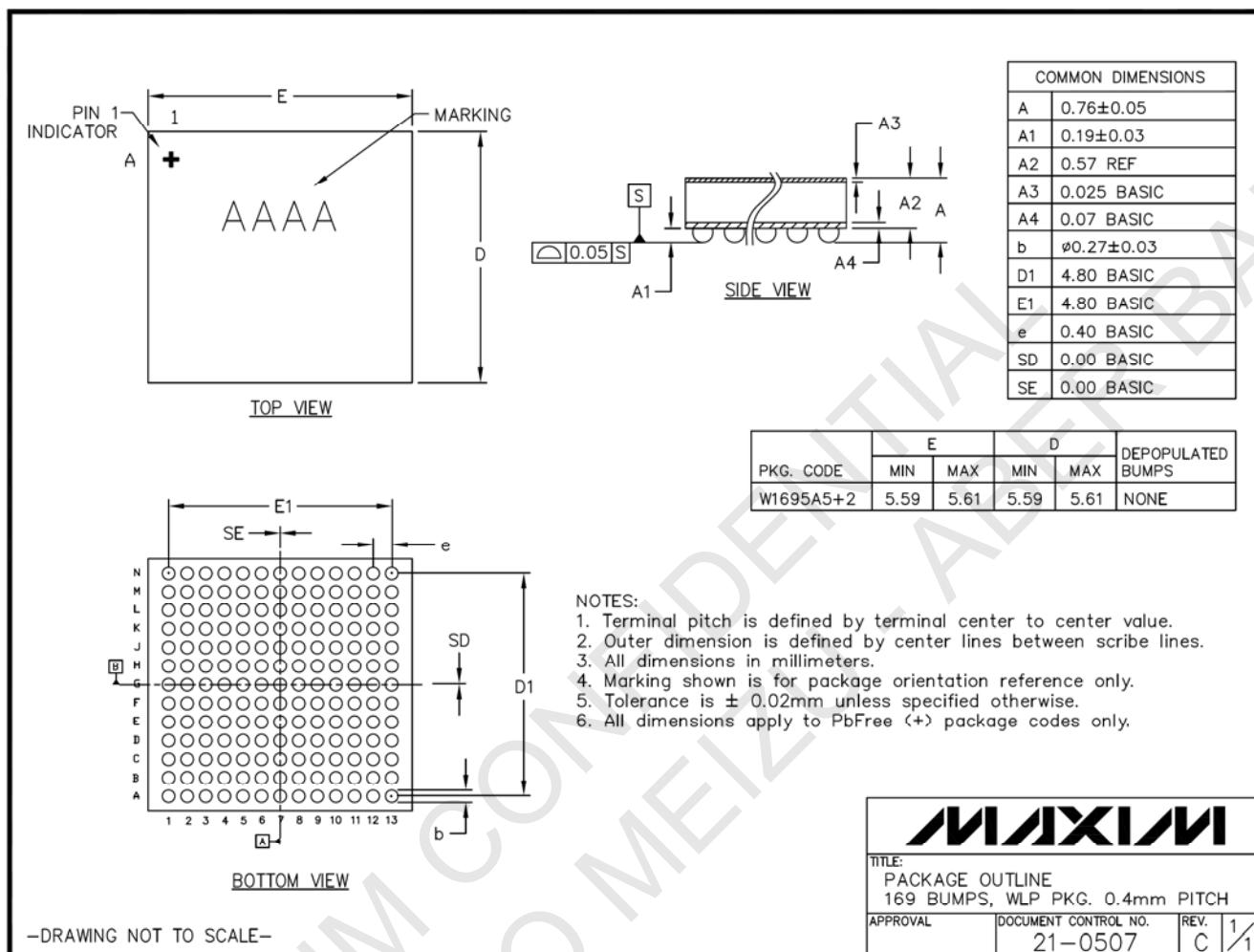
Recommended



Place the bypass cap
closer to the IC.

Place the bypass cap
closer to the IC.

16 Package



-DRAWING NOT TO SCALE-

17 I²C address and Registers for the MAX8966/MAX8997

The MAX8966/MAX8997 acts as a Slave Transmitter/Receiver. The MAX8966/MAX8997 has the following slave address.

Slave Address:

6. PMIC(Bucks, LDOs, Main Charger, Backup Battery Charger, Flash LED Driver, GPIOs,); 0xCCh/0xCDh
7. RTC; 0x0C/0x0D
8. MUIC; 0x4A/0x4B
9. Haptic Motor Driver; 0x90/0x91
10. Fuel Gauge; 0x6C/0x6D

Register Reset Conditions in R column

Type S: Registers are reset each time when $V_{COIN} < V_{COIN\ UVLO}$ (= $\sim 1.55V$) and $BATT < BATT_{UVLO}$

Type S1: Registers are reset each time when $VBATT < 1.55V$.

Type O: Registers are reset each time when $BATT < BATT_{UVLO}$ or MAX8966/MAX8997 transitions from on to off state or PWRHOLD is logic level low.

Type M: Registers are reset each time when BATT and DCIN are $< V_{MUICUVLO}$

18 PMIC Registers

The Slave address of the MAX8966/MAX8997 PMIC is 0xCCh/0xCDh.

PMIC REGISTER SUMMARY

ADDRESS [HEX]	RESET [HEX]	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	FUNCTION	SUB BLOCK
00	77	ID								PMIC ID	PMIC
01	02	VER				REV				PMIC ID	PMIC
02	00	x	x	Flash	GPIO	MUIC	x	PMIC /RTC	x	Interrupt Source	PMIC
03	00	Lowbat1	Lowbat2	JIGONF	JIGONR	PWRON1 SEC	x	PWRONF	PWRONR	Interrupt 1	PMIC
04	00	x	DVS5OK	DVS4OK	DVS2OK	DVS1OK	MR	JIGF	JIGR	Interrupt 2	PMIC
05	00	MBCHGTM EXPD	x	CHGRSTF	x	TOPOFFR	DCINOPV	CHGRM	CHGINS	Interrupt 3 Charger	PMIC
06	00	x	x	WTSR	RTC1S	SMPL_INT	RTCA2	RTCA1	RTC60S	Interrupt 4 RTC	PMIC
07	00	x	x	x	x	x	x	x	x	Reserved	
08	00	Lowbat1m	Lowbat2m	JIGONFm	JIGONRm	PWRON1 SECm	x	PWRONFm	PWRONRm	Interrupt Mask 1	PMIC
09	78	x	DVS5OKm	DVS4OKm	DVS2OKm	DVS1OKm	MRm	JIGFm	JIGRm	Interrupt Mask 2	PMIC
0A	00	MBCHGTM EXPDm	x	CHGRSTFm	x	TOPOFFR m	DCINOPV m	CHGRMm	CHGINSm	Interrupt Mask 3	PMIC
0B	00	x	x	WTSRm	RTC1Sm	SMPL_INT m	RTCA2m	RTCA1m	RTC60Sm	Interrupt Mask 3	PMIC
0C	00	x	x	x	x	x	x	x	x	Reserved	
0D	n/a	WTSREVNT	SMPLEVN T	RTCA2	RTCA1	LOWBAT2	LOWBAT1	JIGON	PWRON	Status 1	PMIC
0E	n/a	SET3	SET2	SET1	PWREN	X	MR/2	MR/1	JIG	Status 2	PMIC
0F	n/a	x	x	x	x	DVS5OK	DVS4OK	DVS2OK	DVS1OK	Status 3	PMIC
10	n/a	x	DCINOPV	PQL	FCHG	CHGON	DETBAT/	DCINOK	DONE	Status 4	PMIC
11	n/a	X	X	X	X	X	X	X	X	Reserved	
12	n/a	X	X	X	X	X	X	X	X	Reserved	
13	03	X	x	x	x	x	EPWRHO LD	EN32KHZC P	EN32KHZ A P	Main Control1	PMIC
14	06	x	x	x	x	x	MRDBTMER			Main Control2	PMIC
15	09	ENRAMPBU CK5	ENRAMPB UCK4	ENRAMPBU CK2	ENRAMPB UCK1	BUCKRAMP				BUCK RAMP	BUCK
16	N/A	X	X	X	x	x	x	x	x	Reserved	
17	N/A	X	X	X	X	X	X	X	X	Reserved	
18	0B	X	X	X	X	ActiveDisc charge	PWM	DVSBUCK1	EBCUK1	BUCK1CTRL	BUCK
19	18	X	X	B1_TV_1						BUCK1 DVS TV1	BUCK
1A	18	X	X	B1_TV_2						BUCK1 DVS TV2	BUCK
1B	18	X	X	B1_TV_3						BUCK1 DVS TV3	BUCK
1C	18	X	X	B1_TV_4						BUCK1 DVS TV4	BUCK
1D	18	X	X	B1_TV_5						BUCK1 DVS TV5	BUCK

1E	18	X	X	B1_TV_6						BUCK1 DVS TV6	BUCK
1F	18	X	X	B1_TV_7						BUCK1 DVS TV7	BUCK
20	18	X	X	B1_TV_8						BUCK1 DVS TV8	BUCK
21	0B	X	X	X	X	ActiveDisc charge	PWM	DVSBUCK2	EBUCK2	BUCK2 CTRL	BUCK
22	12	X	X	B2_TV_1						BUCK2 DVS TV1	BUCK
23	12	X	X	B1_TV_2						BUCK2 DVS TV2	BUCK
24	12	X	X	B1_TV_3						BUCK2 DVS TV3	BUCK
25	12	X	X	B1_TV_4						BUCK2 DVS TV4	BUCK
26	12	X	X	B1_TV_5						BUCK2 DVS TV5	BUCK
27	12	X	X	B1_TV_6						BUCK2 DVS TV6	BUCK
28	12	X	X	B1_TV_7						BUCK2 DVS TV7	BUCK
29	12	X	X	B1_TV_8						BUCK2 DVS TV8	BUCK
2A	0B	X	X	X	X	ACTIVEDI SCHARGE	PWM	X	EBUCK3	BUCK3 CTRL	BUCK
2B	15 /09	X	X	B3_TV						BUCK3 DVS TV	BUCK
2C	08	X	X	X	X	ACTIVEDI SCHARGE	PWM	X	EBUCK4	BUCK4 CTRL	BUCK
2D	16	X	X	B4_TV						BUCK4 DVS TV	BUCK
2E	0B/0A	X	X	X	X	ACTIVEDI SCHARGE	PWM	DVSBUCK5	EBUCK5	BUCK5 CTRL	BUCK
2F	12	X	X	B5_TV_1						BUCK5 DVS TV1	BUCK
30	12	X	X	B5_TV_2						BUCK5 DVS TV2	BUCK
31	12	X	X	B5_TV_3						BUCK5 DVS TV3	BUCK
32	12	X	X	B5_TV_4						BUCK5 DVS TV4	BUCK
33	12	X	X	B5_TV_5						BUCK5 DVS TV5	BUCK
34	12	X	X	B5_TV_6						BUCK5 DVS TV6	BUCK
35	12	X	X	B5_TV_7						BUCK5 DVS TV7	BUCK
36	12	X	X	B5_TV_8						BUCK5 DVS TV8	BUCK
37	14	X	X	X	X	X	GNSLC T	ENMODE	EBUCK6	BUCK6(PA BUCK) CTRL1	BUCK
38	73	X	LBPSTH	ENTHR		X	X	FRCEPWM		BUCK6 PA BUCK CONTROL2	BUCK
39	0B	X	X	X	X	ACTIVEDI SCHARGE	PWM	X	EBUCK7	BUCK7 CTRL	BUCK
3A	19	X	X	B7_TV						BUCK7 DVS TV	BUCK
3B	F2/32	EMODE1		OUT1						LDO1CTRL	LDO

3C	C6/C8	EMODE2	OUT 2						LDO2CTRL	LDO
3D	C6/C8	EMODE3	OUT 3						LDO3CTRL	LDO
3E	D4/14	EMODE4	OUT 4						LDO4CTRL	LDO
3F	C8/08	EMODE5	OUT 5						LDO5CTRL	LDO
40	D4	EMODE6	OUT 6						LDO6CTRL	LDO
41	D4/14	EMODE7	OUT 7						LDO7CTRL	LDO
42	F2	EMODE8	OUT 8						LDO8CTRL	LDO
43	E8	EMODE9	OUT 9						LDO9CTRL	LDO
44	C6/C8	EMODE10	OUT 10						LDO10CTRL	LDO
45	28	EMODE11	OUT11						LDO11CTRL	LDO
46	08	EMODE12	OUT 12						LDO12CTRL	LDO
47	28	EMODE13	OUT 13						LDO13CTRL	LDO
48	14	EMODE14	OUT 14						LDO14CTRL	LDO
49	28/E8	EMODE15	OUT 15						LDO15CTRL	LDO
4A	32/24	EMODE16	OUT 16						LDO16CTRL	LDO
4B	32	EMODE17	OUT 17						LDO17CTRL	LDO
4C	32	EMODE18	OUT 18						LDO18CTRL	LDO
4D	C8/08	EMODE21	OUT21						LDO21CTRL	LDO
4E	X	X	X	X	X	X	X	X	RESERVED	
4F	X	X	X	X	X	X	X	X	RESERVED	
50	A4	ENVICHG	TFCH			X	X	X	MBCCTRL1 MAIN CHARGER	CHARGER
51	D4	VCHGR_FC	MBCHOST EN	X	X	X	X	X	MBCCTRL2 MAIN CHARGER	CHARGER
52	A0	X	X	X	X	MBCCV				MBCCTRL3 MAXIN CHARGER
53	15	X	X	X	MBCICHF CSET	MBCICHFC				MBCCTRL4 MAIN CHARGER
54	20	X	X	X	X	ITOPOFF				MBCCTRL5 MAIN CHARGER
55	71	X	X	AUTOSTOP	X	X	X	X	MBCCTRL6 MAIN CHARGER	CHARGER
56	00	X	X	X	X	X	X	OTPCGHCVS	OTPCGHCVS MAIN CHARGER	CHARGER
57	X	X	X	X	X	X	X	X	RESERVED	
58	X	X	X	X	X	X	X	X	RESERVED	
59	X	X	X	X	X	X	X	X	RESERVED	

5A	75	ENSAFEOU T2	ENSAFEO UT1	ACTDISSA FEO2	ACTDISSA FEO1	SAFEOUT2		SAFEOUT1		SAFEOUT CTRL	SAFEOUT
5B	X	X	X	X	X	X	X	X	X	RESERVED	
5C	X	X	X	X	X	X	X	X	X	RESERVED	
5D	X	X	X	X	X	X	X	X	X	RESERVED	
5E	D7	LB1DAC_E N	LB1EN	LB1HYST		X	LB1TH			LBCNFG1 LOW BATTERY MONITOR	BATT MONITOR
5F	D4	LB2DAC_E N	LB2EN	LB2HYST		X	LB2TH			LBCNFG2 LOW BATTERY MONITOR	BATT MONITOR
60	4F	BBCRS1,BBCRS		BBCLOWEN	BBCVS		BBCS		BBCHOST EN	BBCCTRL BACKUP BATTERY CHARGER	BACK UP BATTERY CHARGER
61	X	X	X	X	X	X	X	X	X	RESERVED	
62	X	X	X	X	X	X	X	X	X	RESERVED	
63	00	FLASH1					X	X	X	FLASH1_CUR	FLASH
64	00	FLASH2					X	X	X	FLASH2_CUR	FLASH
65	00	MOVIE				X	X	X	X	MOVIE_CUR	FLASH
66	C0	GSMB_EN	GSMB_PO L	GSMB				X	X	GSMB_CUR	FLASH
67	00	X	BOOST_E N	BOOST_MODE		BOOST_CNTL				BOOST_CNTL	FLASH
68	00	X	X	MOVIE_EN			FLASH_EN			LEN_CNTL	FLASH
69	00	TMP_CNTR L	TMR_MO DE	X	TMP_DUR					FLASH_CNTL	FLASH
6A	00	WDT_EN	WDT_DUR		WDT_RST	X	X	X	X	WDT_CNTL	FLASH
6B	00	LB_EN	LB_CNTL					LB_HYS		MAXFLASH1	FLASH
6C	00	X	X	LB_TMR_R			LB_TMR_F			MAXFLASH2	FLASH
6D	00	MAXFLASH	GSMB	POK_FLT	ADAPT_F LT	OVER_TE MP	ILIM_FLT	FLED2_FLT	FLED1_FLT	INTERRUPT/STA TUS	FLASH
6E	FF	MAXFLASH m	GSMBm	POK_FLTm	ADAPT_F LTm	OVER_TE MPm	ILIM_FLT m	FLED2_FLT m	FLED1_FLT m	STATUS MASK	FLASH
6F	00	X	X	X	X	X	X	X	X	RESERVED	
70	08	GPIDBNC		INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL0	GPIO
71	08	GPIDBNC		INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL1	GPIO
72	08	GPIDBNC		INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL2	GPIO
73	08	GPIDBNC		INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL3	GPIO
74	08	GPIDBNC		INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL4	GPIO
75	08	GPIDBNC		INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL5	GPIO
76	08	GPIDBNC		INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL6	GPIO

77	08	GPIDBNC	INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL7	GPIO
78	08	GPIDBNC	INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL8	GPIO
79	08	GPIDBNC	INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL9	GPIO
7A	08	GPIDBNC	INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL10	GPIO
7B	08	GPIDBNC	INTCNT		DATAOUT	DATAIN	DIR	DRV	GPIOCNTL11	GPIO
7C	N/A	X	X	X	X	X	X	X	RESERVED	
7D	00	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	GPIO INTEERUPT1
7E	00	X	X	X	X	GPIO11	GPIO10	GPIO9	GPIO8	GPIO INTEERUPT1
7F	N/A	X	X	X	X	X	X	X	RESERVED	
80	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO1CONFIG
81	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO2CONFIG
82	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO3CONFIG
83	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO4CONFIG
84	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO5CONFIG
85	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO6CONFIG
86	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO7CONFIG
87	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO8CONFIG
88	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO9CONFIG
89	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO10CONFIG
8A	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO11CONFIG
8B	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO12CONFIG
8C	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO13CONFIG
8D	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO14CONFIG
8E	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO15CONFIG
8F	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO16CONFIG
90	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO17CONFIG
91	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO18CONFIG
92	A2	LDOOVCLM PEN	X	LDO_COMP		LDOPOK	X	LDOADE	X	LDO21CONFIG
93		x	x	x	x	x	x	x	Reserved	
94		x	x	x	x	x	x	x	Reserved	

95		x	x	x	x	x	x	x	x	Reserved	
96		x	x	x	x	x	x	x	x	Reserved	
97	03	x	x	x	DVSOKTIMER1						DVSOKTIMER1 Buck1
98	03	x	x	x	DVSOKTIMER2						DVSOKTIMER2 Buck2
99	03	x	x	x	DVSOKTIMER4						DVSOKTIMER4 Buck4
9A	03	x	x	x	DVSOKTIMER5						DVSOKTIMER5 Buck5

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18.1 PMIC REGISTER DETAILS

18.2 PMIC ID – PMIC ID and revision register

PMIC ID – PMIC ID and revision register			Addr:0x00	R: O	Reset: 77hex
BIT	Mode	Name	Reset	Description	
3:0	R	ID	7	ID of MAX8966/MAX8997	
7:4	R	ID	7		

PMIC ID – revision register			Addr:0x01	R: O	Reset: 02hex
BIT	Mode	Name	Reset	Description	
3:0	R	REV	N/A	<i>Pass</i> 0b000 = pass 1 0b001 = pass 2 0b010 = pass 3	
7:4	R	VERSION		<i>Version</i> 0b000 = (MAX8997) 0b001 = (MAX8966) 0b010 = xmo	

18.3 INTERRUPTS

18.3.1 INTSRC – Interrupt register for Subblocks

INTSRC – Interrupt source register			Addr: 0x02	R:O	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R	Reserved	0		
1	R	PMIC and_RTC	0	1: PMIC and RTC interrupt is detected. (IRQ1/)	
2	R	Fuel Gauge Reserved	0	1: Fuel Gauge interrupt is detected. (Alert) Reserved	
3	R	MUIC	0	1: MUIC interrupt is detected (IRQ1/)	
4	R	GPIO	0	1: GPIO interrupt is detected. (IRQ1/)	
5	R	Flash	0	1: Flash interrupt is detected (IRQ1/)	
6	R	Reserved	0		
7	R	Reserved	0		

18.3.2 INT1 – ON/OFF Control Interrupt register- PMIC

INT1 – Interrupt 1 register			Addr:0x03	R: S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R&C	PWRONR	0	<i>I: PWRON Key Rising edge is detected. Debounced.</i>	
1	R&C	PWRONF	0	<i>I: PWRON Key Falling edge is detected. Debounced.</i>	
2	R&C	Reserved	0	Reserved	
3	R&C	PWRON1SEC	0	<i>I: PWRON high for longer than 1sec</i>	
4	R&C	JIGONR	0	<i>I: JIGON rising edge is detected. Debounced.</i>	
5	R&C	JIGONF	0	1: JIGON falling edge is detected. Debounced.	
6	R&C	LOWBAT2	0	1; Low Battery 2nd warning is detected. The main battery	

				voltage falling detection. (See LBTH2)
7	R&C	LOWBAT1	0	1; Low Battery 1st warning is detected. (The main battery voltage falling detection. (See LBTH1))

18.3.3 INT2- ON/OFF Control Interrupt register-PMIC

INT2 – Interrupt 2 register			Addr:0x04	R: S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R&C	JIGR	0	<i>I: JIG from MUIC rising edge. Debounced.</i>	
1	R&C	JIGF	0	1: JIG from MUIC falling edge. Debounced.	
2	R&C	MR	0	1: MR1/ and MR2/ logic low for longer than Manual Reset Debounce time (MRDBTMER).	
3	R&C	DVS1OK	0	1: Buck1 DVS Timer is expired in DVS mode.	
4	R&C	DVS2OK	0	1: Buck2 DVS Timer is expired in DVS mode.	
5	R&C	DVS4OK	0	1: Buck4 DVS Timer is expired in DVS mode.	
6	R&C	DVS5OK	0	<i>I: Buck5 DVS Timer is expired in DVS mode.</i>	
7	R&C	Reserved	0		

18.3.4 INT3 – Main Charger Interrupt register (CHGINT1)-PMIC

INT3 – Interrupt 3 register			Addr:0x05	R: S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R&C	CHGINS	0	Charger Input Source insertion VDCIN>UVLO and (VDCIN-VBATT)>250mV and VDCIN<OVP	
1	R&C	CHGRM	0	Charger Input Source removal	
2	R&C	DCINOVP	0	1: Charger Input voltage is greater than the Over-Voltage threshold.	
3	R&C	TOPOFFR	0	1: End of charge threshold (Top-off threshold) has reached. (Charger current falls below TOPOFF threshold).	
4	R&C	Reserved	0	reserved	
5	R&C	CHGRSTF	0	1: Charger restart threshold falling edge is detected.	
6	R&C	Reserved	0	reserved	
7	R&C	MBCHGTMEXPD	0	1: Main battery Fast charging timer or Prequal timer is expired.	

18.3.5 INT4 – RTC Interrupt register

INT4 – Interrupt 4 register			Addr: 0x06	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R&C	RTC60S	0	RTC periodic 60s event	
1	R&C	RTCA1	0	RTC alarm1	
2	R&C	RTCA2	0	RTC alarm2	
3	R&C	SMPL_INT	0	SMPL interrupt to host controller	
4	R&C	RTC1S	0	RTC periodic 1s event	
5	R&C	WTSR	0	1:WTSR event interrupt	
6	R&C	Reserved	0	X	
7	Reserved	Reserved	0	X	

Reserved 0x07 Register

18.3.6 INT1MSK – ON/OFF Control Interrupt mask register - PMIC

INT1MSK – Interrupt 1 mask register			Addr: 0x08	R: S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	PWRONRm	0	PWRON rising event 0: Not masked 1: Masked	
1	R/W	PWRONFm	0	PWRON falling event 0: Not masked 1: Masked	
2	R/W	Reserved	0	Reserved	
3	R/W	PWRON1SECm	0	PWRON1SEC event 0: Not masked 1: Masked	
4	R/W	JIGONRm	0	JIGONR event 0: Not masked 1: Masked	
5	R/W	JIGONFm	0	JIGONF event 0: Not masked 1: Masked	
6	R/W	LOWBAT2m	0	LOBAT2 event 0: Not masked 1: Masked	
7	R/W	LOWBAT1m	0	LOBAT1 event 0: Not masked 1: Masked	

18.3.7 INT2MSK – ON/OFF Control Interrupt mask register - PMIC

INT2MSK – Interrupt2 mask register			Addr0x09	R:S	Reset: 78hex
BIT	Mode	Name	Reset	Description	
0	R/W	JIGRm	0	JIGR event 0: Not masked 1: Masked	
1	R/W	JIGFm	0	JIGF event 0: Not masked 1: Masked	
2	R/W	MRm	0	MR1/ and MR2/ manual reset event 0: Not masked 1: Masked	
3	R/W	DVS1OKm	1	DVS1 OK event 0: Not masked 1: Masked	
4	R/W	DVS2OKm	1	DVS2 OK event 0: Not masked 1: Masked	
5	R/W	DVS4OKm	1	DVS4 OK event 0: Not masked 1: Masked	
6	R/W	DVS5OKm	1	DVS5 OK event 0: Not masked 1: Masked	
7	R/W	Reserved	0	X	

18.3.8 INT3MSK – Main Charger Interrupt mask register (CHGINT1_MASK)-PMIC

INT3MSK – Interrupt 3 mask register	Addr:0x0A	R: S	Reset: 00hex
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BIT	Mode	Name	Reset	Description
0	R&W	CHGINSm	0	CHGINS event 0: Not masked 1: Masked
1	R&W	CHGRMm	0	CHGRM event 0: Not masked 1: Masked
2	R&W	DCINOPVm	0	DCINOPV event 0: Not masked 1: Masked
3	R&W	TOPOFFRm	0	TOPOFFR event 0: Not masked 1: Masked
4	R&W	Reserved	0	
5	R&W	CHGRSTFm	0	CHGRSTF event 0: Not masked 1: Masked
6	R&W	reserved	0	
7	R&W	MBCHGTMEXPDm	0	MGCHGTMEXPD event 0: Not masked 1: Masked

18.3.9 INT4MSK – RTC interrupt mask register

INT4MSK – Interrupt 4 mask register			Addr:0x0B	R: S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	RTC60Sm	0	RTC periodic 60s event 0: Not masked 1: Masked	
1	R/W	RTCA1m	0	RTC alarm1 0: Not masked 1: Masked	
2	R/W	RTCA2m	0	RTC alarm2 0: Not masked 1: Masked	
3	R/W	SMPL_INTm	0	SMPL interrupt to host controller 0: Not masked 1: Masked	
4	R/W	RTC1Sm	0	RTC periodic 1s event 0: Not masked 1: Masked	
5	R/W	WTSRm	0	WTSR event 0: Not masked 1: Masked	
6	Reserved	Reserved	0	x	
7	Reserved	Reserved	0	x	

Reserved 0x0C Register

18.4 STATUS REGISTERS

18.4.1 STATUS1 – ON/OFF Control Status register-PMIC

STATUS1 – Status 1 register			Addr:0xD	R: O	Reset: N/A
BIT	Mode	Name	Reset	Description	
0	R	PWRON	N/A	0: PWRON is low (not pressed), 1: PWRON is high (pressed)	
1	R	JIGON	N/A	0: JIGON is low (no input), 1: JIGON is high (input present)	

2	R	LOWBAT1	N/A	0: The main battery voltage is below Battery Voltage Monitor Threshold (LBTH1) 1: The main battery voltage is above Battery Voltage Monitor Threshold(LBTH1)
3	R	LOWBAT2	N/A	0: The main battery voltage is below Battery Voltage Monitor Threshold (LBTH2) 1: The main battery voltage is above Battery Voltage Monitor Threshold (LBTH2)
4	R	RTCA1	N/A	<i>0: RTC ALARM1 is not reached</i> 1: RTC ALARM1 has reached
5	R	RTCA2	N/A	<i>0: RTC ALARM2 is not reached</i> 1: RTC ALARM2 has reached
6	R	SMPLEVNT	N/A	<i>0: SMPL event hasn't happened.</i> 1: SMPL event has happened.
7	R	WTSREVNT	N/A	<i>0: WTSR event hasn't happened.</i> <i>1: WTSR event has happened.</i>

18.4.2 STATUS2 – ON/OFF Control Status register-PMIC

STATUS2 – Status 2 register			Addr: 0x0E	R: O	Reset: N/Ahex
BIT	Mode	Name	Reset	Description	
0	R	JIG	N/A	JIG is internal booting source coming from MUIC block. 0; JIG is not detected. 1; JIG is detected.	
1	R	MR/1	N/A	MR/1 pin status without debounce timer 0; MR/1 is Low. 1; MR/1 is High.	
2	R	MR/2	N/A	MR/2 pin status without debounce timer. 0; MR/2 is Low. 1; MR/2 is High.	
3	R	Reserved	n/A		
4	R	PWREN	N/A	0; PWREN is Low. 1; PWREN is High.	
5	R	SET1	N/A	0; SET1 is Low. 1; SET1 is High.	
6	R	SET2	N/A	0; SET2 is Low. 1; SET2 is High.	
7	R	SET3	N/A	0; SET3 is Low. 1; SET3 is High.	

18.4.3 STATUS3 – ON/OFF Control Status register-PMIC

STATUS3 – Status 3 register			Addr: 0x0F	R: O	Reset: N/Ahex
BIT	Mode	Name	Reset	Description	
0	R	DVS1OK	N/A	Buck1 DVS Completion 0; Buck1 DVS output voltage event is not completed. 1; Buck1 DVS output voltage event is completed..	
1	R	DVS2OK	N/A	Buck2 DVS Completion 0; Buck2 DVS output voltage event is not completed. 1; Buck2 DVS output voltage event is completed..	
2	R	DVS4OK	N/A	Buck4 DVS Completion 0; Buck4 DVS output voltage event is not completed. 1; Buck4 DVS output voltage event is completed..	
3	R	DVS5OK	N/A	Buck5 DVS Completion 0; Buck5 DVS output voltage event is not completed. 1; Buck5 DVS output voltage event is completed..	
4	R	Reserved	N/A		
5	R	Reserved	N/A		
6	R	Reserved	N/A		
7	R	Reserved	N/A		

18.4.4 STATUS4 – Main Charger Status register – PMIC

STATUS4 – Status 4 register			Addr:0x10	R: O	Reset: N/A
BIT	Mode	Name	Reset	Description	
0	R	DONE	N/A	<i>0: Charger is not in the DONE state 1: Charger is in the DONE state</i>	
1	R	DCINOK	N/A	<i>0: VDCIN is below UVLO or above OVP 1: VDCIN is greater than UVLO and less than OVP</i>	
2	R	DETBAT/	N/A	<i>0: Main Battery is detected.(when DETBAT/= GND) 1: Main Battery is not detected. (Charger is disabled when DETBAT=high or float)</i>	
3	R	CHGON	N/A	<i>0: Charger FET is disabled 1: charger FET is enabled</i>	
4	R	FCHG	N/A	<i>0: Charger is not in the fast charge mode 1: Charger is in the fast charge mode</i>	
5	R	PQL	N/A	<i>0: Charger is not in the prequalification mode 1: Charger is in the prequalification mode.</i>	
6	R	DCINOVP	N/A	<i>0: Charger Input voltage is lower than the Over-Voltage threshold. 1: Charger Input voltage is greater than the Over-Voltage threshold.</i>	
7	R	reserved	N/A	Reserved	

Reserve 0x11 Register
Reserved 0x12 Register

18.5 Main Control 1

Main Control1			Addr:0x13	R: O	Reset: 03 hex
BIT	Mode	Name	Reset	Description	
0	R/W	EN32KHZAP	1	<i>1: Turn 32kHzAP on. 0: Turn 32kHzAP off.</i>	
1	R/W	EN32KHZCP	1	<i>1: Turn 32kHzCP on. 0: Turn 32kHzCP off.</i>	
2	R/W	EPWRHOLD	0	<i>1: Internal PWRHOLD Logic High 0: Internal PWRHOLD Logic Low (EPWRHOLD and PWRHOLD are internally ORed)</i>	
3	R/W	Reserved	0		
4	R/W	Reserved	0	Reserved	
5	R/W	Reserved	0	Reserved	
6	R/W	Reserved	0	Reserved	
7	R/W	Reserved	0	Reserved	

18.6 Main Control 2

Main Control2			Addr: 0x14	R: O	Reset: 06 hex
BIT	Mode	Name	Reset	Description	
0	R/W	MRDBTMR		Manual Reset Debounce Timer when MR1/ = MR2/ = Logic	

1	R/W		110 (7sec)	Low 000; 1 sec 001; 2sec 010; 3sec 011; 4sec 100; 5sec 101; 6sec 110; 7sec 111 ; 8sec	
2	R/W				
3	R/W	RESERVED	0		
4	R/W	RSERVED	0		
5	R/W	RSERVED	0		
6	R/W	RSERVED	0		
7	R/W	RSERVED	0		

18.7 BUCK RAMP Register for BUCK1, BUCK2, BUCK4, and BUCK5- PMIC

BUCKRAMP Control register			Addr 0x15	R: O	Reset: 09 hex
BIT	Mode	Name	Reset	Description	
3:0	R/W	BUCKRAMP[4:0]]	1001	<p>0000: 1.00mV/us 0001: 2.00 mV/us 0010: 3.03mV/us 0011: 4.00 mV/us 0100: 5.00 mV/us 0101: 5.88 mV/us 0110: 7.14 mV/us 0111: 8.33 mV/us 1000: 9.09 mV/us 1001: 10.00 mV/us (default) 1010: 11.11 mV/us 1011: 12.50 mV/us 1100; 16.67mV/us 1101: 25mV/us 1110: 50mV/us 1111: 100mV/us</p>	
4	R/W	ENRAMPBUCK 1	0	Ramp Control ON/OFF For BUCK1 0: Turn off Ramp Control of BUCK1 1: Turn on Ramp Control of BUCK1	
5	R/W	ENRAMPBUCK 2	0	Ramp Control ON/OFF For BUCK2 0: Turn off Ramp Control of BUCK2 1: Turn on Ramp Control of BUCK2	
6	R/W	ENRAMPBUCK 4	0	Ramp Control ON/OFF For BUCK4 0: Turn off Ramp Control of BUCK4 1: Turn on Ramp Control of BUCK4	
7	R/W	ENRAMPBUCK 5	0	Ramp Control ON/OFF For BUCK5 0: Turn off Ramp Control of BUCK5 1: Turn on Ramp Control of BUCK5	

Reserved 0x16 Register

Reserved 0x17 Register

18.8 BUCK1CTRL

BUCK1CTRL – Buck1 switching regulator control register			Addr: 0x18	R: O	Reset: 0Bhex
BIT	Mode	Name	Reset	Description	
0	R/W	EBUCK1	1	<p><i>1: Turn Buck1 on (when EBUCK1=1 or PWREN=1, Buck1 regulator is on).</i> 0: Turn Buck1 off (When EBUCK1=0 and PWREN=0, Buck1 regulator is off).</p>	
1	R/W	DVSBUCK1	1	<p>0: DVS OFF (output voltage is set by B1_TV_1[5:0]) 1: DVS ON (BUCK1 output is chosen by SET1, SET2 and SET3)</p>	
2	R/W	PWM	0	<p>Forced PWM <i>1: Turn Forced PWM on</i> 0: Turn Forced PWM off</p>	
3	R/W	Active Discharge	1	<p>Active Discharge of LX1 0: No active discharge 1: Active discharge</p>	
4	R/W	Reserved			
5	R/W	Reserved			
7:6	R/W	Reserved			

18.9 BUCK1TV_DVS

BUCK1DVS Target Voltage			Addr:0x19 Addr: 0x1A Addr:0x1B Addr: 0x1C Addr;0x1D Addr;0x1E Addr;0x1F Addr;0x20	R: O	Reset: 18hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	B1_TV_1[5:0] B1_TV_2[5:0] B1_TV_3[5:0] B1_TV_4[5:0] B1_TV_5[5:0] B1_TV_6[5:0] B1_TV_7[5:0] B1_TV_8[5:0]	011000 (1.25V)	<p>BUCK1 DVS output voltage option 000000: 0.650V 000001: 0.675V 000010: 0.700V 000011: 0.725V 000100: 0.750V 000101: 0.775V 000110: 0.800V 000111: 0.825V 001000: 0.850V 001001: 0.875V 001010: 0.900V 001011: 0.925V 001100: 0.950V 001101: 0.975V 001110: 1.000V 001111: 1.025V 010000: 1.050V 010001: 1.075V</p>	

				010010: 1.100V 010011: 1.125V 010100: 1.150V 010101: 1.175V 010110: 1.200V 010111: 1.225V 011000: 1.250V 011001: 1.275V 011010: 1.300V 011011: 1.325V 011100: 1.350V 011101: 1.375V 011110: 1.400V 011111: 1.425V 100000: 1.450V 100001: 1.475V 100010: 1.500V 100011: 1.525V 100100: 1.550V 100101: 1.575V 100110: 1.600V 100111: 1.625V 101000: 1.650V 101001: 1.675V 101010: 1.700V 101011: 1.725V 101100: 1.750V 101101: 1.775V 101110: 1.800V 101111: 1.825V 110000: 1.850V 110001: 1.875V 110010: 1.900V 110011: 1.925V 110100: 1.950V 110101: 1.975V 110110: 2.000V 110111: 2.025V 111000: 2.050V 111001: 2.075V 111010: 2.100V 111011: 2.125V 111100: 2.150V 111101: 2.175V 111110: 2.200V 111111: 2.225V
6-7	R/W	Resvred		

18.10 BUCK2CTRL

BUCK2– Buck2switching regulator control register			Addr0x:0x21	R: O	Reset: 0Bhx
BIT	Mode	Name	Reset	Description	
0	R/W	EBUCK2	1	<i>I: Turn Buck2 on (when PWREN=1 or EBUCK2=1, Buck2 regulator is on).</i> 0: Turn Buck2 off (When PWREN=0 and EBUCK2=0, Buck2 regulator is off).	

1	R/W	DVSBUCK2	1	0: DVS OFF (output voltage is set by B2_TV_1[5:0])1: DVS ON (BUCK2 output is chosen by SET1, SET2, SET3)
2	R/W	PWM	0	Forced PWM <i>1: Turn Forced PWM on</i> 0: Turn Forced PWM off
3	R/W	Active Discharge	1	Active Discharge of LX2 0: No active discharge 1: Active discharge
4	R/W	Reserved	0	
5	R/W	Reserved	0	
7:6	R/W	Reserved	0	

18.11 BUCK2TV_DVS

BUCK2DVS Target Voltage			Addr:0x22 Addr:0x23 Addr:0x24 Addr:0x25 Addr:0x26 Addr:0x27 Addr:0x28 Addr:0x29	R: O	Reset: 12hex	
BIT	Mode	Name	Reset	Description		
5:0	R/W	B2_TV_1[5:0] B2_TV_2[5:0] B2_TV_3[5:0] B2_TV_4[5:0] B2_TV_5[5:0] B2_TV_6[5:0] B2_TV_7[5:0] B2_TV_8[5:0]	010010 (1.1V)	BUCK2 DVS output voltage option 000000: 0.650V 000001: 0.675V 000010: 0.700V 000011: 0.725V 000100: 0.750V 000101: 0.775V 000110: 0.800V 000111: 0.825V 001000: 0.850V 001001: 0.875V 001010: 0.900V 001011: 0.925V 001100: 0.950V 001101: 0.975V 001110: 1.000V 001111: 1.025V 010000: 1.050V 010001: 1.075V 010010: 1.100V 010011: 1.125V 010100: 1.150V 010101: 1.175V 010110: 1.200V 010111: 1.225V 011000: 1.250V 011001: 1.275V		

				011010: 1.300V 011011: 1.325V 011100: 1.350V 011101: 1.375V 011110: 1.400V 011111: 1.425V 100000: 1.450V 100001: 1.475V 100010: 1.500V 100011: 1.525V 100100: 1.550V 100101: 1.575V 100110: 1.600V 100111: 1.625V 101000: 1.650V 101001: 1.675V 101010: 1.700V 101011: 1.725V 101100: 1.750V 101101: 1.775V 101110: 1.800V 101111: 1.825V 110000: 1.850V 110001: 1.875V 110010: 1.900V 110011: 1.925V 110100: 1.950V 110101: 1.975V 110110: 2.000V 110111: 2.025V 111000: 2.050V 111001: 2.075V 111010: 2.100V 111011: 2.125V 111100: 2.150V 111101: 2.175V 111110: 2.200V 111111: 2.225V
6-7	R/W	Reserved		

18.12 BUCK3CTRL

BUCK3CTRL – Buck3 switching regulator control register			Addr:- 0x2A	R: O	Reset: 0Bhex
BIT	Mode	Name	Reset	Description	
0	R/W	EBUCK3	1	MAX8966; 1: Turn Buck3 on 0: Turn Buck3 off MAX8997 1: Turn Buck3 on (when EBUCK3=1 or PWREN=1) 0: Turn Buck3 off (When EBUCK3=0 and PWREN=0)	
1	R/W	Reserved	1	Reserved	
2	R/W	PWM	0	Forced PWM 1: Turn Forced PWM on 0: Turn Forced PWM off	

3	R/W	Active Discharge	1	Active Discharge of LX3 0: No active discharge 1: Active discharge
4	R/W	Reserved		
5	R/W	Reserved		
7:6	R/W	Reserved		

18.13 BUCK3TV_DVS

BUCK3 Target Voltage			Addr: 0x2B	R: O Reset: 15hex for MAX8966 09hex for MAX8997
BIT	Mode	Name	Reset	Description
5:0	R/W	B3_TV[5:0]	010101(1.8V) for MAX8966 001001(1.2V) for MAX8997	BUCK3 Target Output Voltage 000000: 0.750V 000001: 0.800V 000010: 0.850V 000011: 0.900V 000100: 0.950V 000101: 1.000V 000110: 1.050V 000111: 1.100V 001000: 1.150V 001001: 1.200V 001010: 1.250V 001011: 1.300V 001100: 1.350V 001101: 1.400V 001110: 1.450V 001111: 1.500V 010000: 1.550V 010001: 1.600V 010010: 1.650V 010011: 1.700V 010100: 1.750V 010101: 1.800V 010110: 1.850V 010111: 1.900V 011000: 1.950V 011001: 2.000V 011010: 2.050V 011011: 2.100V 011100: 2.150V 011101: 2.200V 011110: 2.250V 011111: 2.300V 100000: 2.350V 100001: 2.400V 100010: 2.450V 100011: 2.500V 100100: 2.550V 100101: 2.600V 100110: 2.650V 100111: 2.700V 101000: 2.750V

				101001: 2.800V 101010: 2.850V 101011: 2.900V 101100: 2.950V 101101: 3.000V 101110: 3.050V 101111: 3.100V 110000: 3.150V 110001: 3.200V 110010: 3.250V 110011: 3.300V 110100: 3.350V 110101: 3.400V 110110: 3.450V 110111: 3.500V 111000: 3.550V 111001: 3.600V 111010: 3.650V 111011: 3.700V 111100: 3.750V 111101: 3.800V 111110: 3.850V 111111: 3.900V
6-7	R/W	Reserved		

18.14 BUCK4CTRL

BUCK4CTRL – Buck4 switching regulator control register			Addr: 0x2C	R: O	Reset: 08hex
BIT	Mode	Name	Reset	Description	
0	R/W	EBUCK4	0	<i>I: Turn Buck4 on</i> 0: Turn Buck4 off	
1	R/W	Reserved	0	Reserved	
2	R/W	PWM	0	Forced PWM <i>I: Turn Forced PWM on</i> 0: Turn Forced PWM off	
3	R/W	Active Discharge	1	Active Discharge of LX4 0: No active discharge 1: Active discharge	
4	R/W	Reserved	0		
5	R/W	Reserved	0		
7:6	R/W	Reserved	00		

18.15 BUCK4TV_DVS

BUCK4 Target Voltage			Addr: 0x2D	R: O	Reset: 16hex
BIT	Mode	Name	Reset	Description	

5:0	R/W	B4_TV[5:0]	010110	BUCK4 Target Output Voltage 000000: 0.650V 000001: 0.675V 000010: 0.700V 000011: 0.725V 000100: 0.750V 000101: 0.775V 000110: 0.800V 000111: 0.825V 001000: 0.850V 001001: 0.875V 001010: 0.900V 001011: 0.925V 001100: 0.950V 001101: 0.975V 001110: 1.000V 001111: 1.025V 010000: 1.050V 010001: 1.075V 010010: 1.100V 010011: 1.125V 010100: 1.150V 010101: 1.175V 010110: 1.200V 010111: 1.225V 011000: 1.250V 011001: 1.275V 011010: 1.300V 011011: 1.325V 011100: 1.350V 011101: 1.375V 011110: 1.400V 011111: 1.425V 100000: 1.450V 100001: 1.475V 100010: 1.500V 100011: 1.525V 100100: 1.550V 100101: 1.575V 100110: 1.600V 100111: 1.625V 101000: 1.650V 101001: 1.675V 101010: 1.700V 101011: 1.725V 101100: 1.750V 101101: 1.775V 101110: 1.800V 101111: 1.825V 110000: 1.850V 110001: 1.875V 110010: 1.900V 110011: 1.925V 110100: 1.950V 110101: 1.975V 110110: 2.000V 110111: 2.025V 111000: 2.050V 111001: 2.075V 111010: 2.100V 111011: 2.125V 111100: 2.150V 111101: 2.175V 111110: 2.200V 111111: 2.225V
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6-7	R/W	Resreve		
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18.16 BUCK5CTRL

BUCK5CTRL – Buck5 switching regulator control register			Addr:0x2E	R: O Reset: 0Bhex:MAX8997 0Ahex:MAX8966
BIT	Mode	Name	Reset	Description
0	R/W	EBUCK5	1:MAX8997 0:MAX8966	MAX8966; 1: Turn Buck5 on (when EBUCK5=1 or PWREN=1) 0: Turn Buck5 off (When EBUCK5=0 and PWREN=0) MAX8997; 1:Turn Buck5 on 0: Turn Buck5off
1	R/W	DVSBUCK5	1	0: DVS OFF(output voltage is set by B5_TV_1[5:0]) 1: DVS ON (BUCK5 output is chosen by SET1, SET2 and SET3)
2	R/W	PWM	0	Forced PWM 1: Turn Forced PWM on 0: Turn Forced PWM off
3	R/W	Active Discharge	1	Active Discharge of LX5 0: No active discharge 1: Active discharge
4	R/W	Reserved	0	reserved
5	R/W	Reserved	0	
7:6	R/W	Reserved	00	

18.17 BUCK5TV_DVS

BUCK5 Target Voltage			Addr: 0x2F Addr: 0x30 Addr: 0x31 Addr: 0x32 Addr:0x33 Addr:0x34 Addr:0x35 Addr:0x36	R: O	Reset: 12hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	B5_TV_1[5:0] B5_TV_2[5:0] B5_TV_3[5:0] B5_TV_4[5:0] B5_TV_5[5:0] B5_TV_6[5:0] B5_TV_7[5:0] B5_TV_8[5:0]	010010 (1.1V)	BUCK5 Target Output Voltage 000000: 0.650V 000001: 0.675V 000010: 0.700V 000011: 0.725V 000100: 0.750V 000101: 0.775V 000110: 0.800V 000111: 0.825V 001000: 0.850V 001001: 0.875V	

				001010: 0.900V 001011: 0.925V 001100: 0.950V 001101: 0.975V 001110: 1.000V 001111: 1.025V 010000: 1.050V 010001: 1.075V 010010: 1.100V 010011: 1.125V 010100: 1.150V 010101: 1.175V 010110: 1.200V 010111: 1.225V 011000: 1.250V 011001: 1.275V 011010: 1.300V 011011: 1.325V 011100: 1.350V 011101: 1.375V 011110: 1.400V 011111: 1.425V 100000: 1.450V 100001: 1.475V 100010: 1.500V 100011: 1.525V 100100: 1.550V 100101: 1.575V 100110: 1.600V 100111: 1.625V 101000: 1.650V 101001: 1.675V 101010: 1.700V 101011: 1.725V 101100: 1.750V 101101: 1.775V 101110: 1.800V 101111: 1.825V 110000: 1.850V 110001: 1.875V 110010: 1.900V 110011: 1.925V 110100: 1.950V 110101: 1.975V 110110: 2.000V 110111: 2.025V 111000: 2.050V 111001: 2.075V 111010: 2.100V 111011: 2.125V 111100: 2.150V 111101: 2.175V 111110: 2.200V 111111: 2.225V
6-7	R/W	Resreveed		

18.18 BUCK6 PA Buck Main Control Register

BUCK6CTRL – Buck6 switching regulator control register		Addr:0x37	R: O	Reset: 0x14 hex
BIT	Mode	Name	Reset	Description

0	R/W	EBUCK6	0	<i>I: Turn Buck6 on</i> 0: Turn Buck6 off
1	R/W	ENMODE	0	Enable selection 0: Buck6 output is On/OFF by BUCK6EN (hardware pin) 1: Buck6 output is On/OFF by ENBUCK6 bit
2	R/W	GNSLCT	1	REFIN to OUT gain selection 0: 2.5X 1:3.0X
3	R/W	Reserved	0	Reserved
4	R/W	Reserved	0	Reserved
5:7	R/W	Reserved	000	Reserved

18.19 BUCK6 PA Buck Bypass and Skip Mode Control Register

BUCK6BPSKIPCTRL – Buck6 control register for bypass and skip modes.			Addr:0x38	R: O	Reset: 0x73
BIT	Mode	Name	Reset	Description	
1:0	R/W	FRCEPWM	11	00: Force PWM at all levels of REFIN 01: Force PWM REFIN > 300mV 10: Force PWM REFIN > 400mV 11: Force PWM REFIN > 500mV	
2	R/W	Reserved	0		
3	R/W	Reserved	0		
5:4	R/W	ENTHR	11	Linear Bypass Regulation Enable Threshold 00(Bypass LDO disabled for all REFIN) 2.5x OFF 01(REFIN=1.2/Gain) 480 400 10(REFIN=1.3/Gain) 520 433 11(REFIN=1.4/Gain) 560 466	
6	R/W	LBPSTH	1	Linear Bypass Regulation Threshold 0: 120mV below Buck6 regulation voltage; 1: 60mV below Buck6 regulation voltage;	
7	R/W	Reserved	0		

18.20 BUCK7CTRL

BUCK7CTRL – Buck7 switching regulator control register			Addr:- 0x39	R: O	Reset: 0Bhex
BIT	Mode	Name	Reset	Description	
0	R/W	EBUCK7	1	<i>I: Turn Buck7 on</i> 0: Turn Buck7 off	

1	R/W	Reserved	1	Reserved
2	R/W	PWM	0	Forced PWM 1: Turn Forced PWM on 0: Turn Forced PWM off
3	R/W	Active Discharge	1	Active Discharge of LX7 0: No active discharge 1: Active discharge
4	R/W	Reserved	0	
5	R/W	Reserved	0	
7:6	R/W	Reserved	0	

18.21 BUCK7TV_DVS

BUCK7 Target Voltage			Addr: 0x3A	R: O	Reset: 19hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	B7_TV[5:0]	011001 (2.0V)	BUCK7 Target Output Voltage 000000: 0.750V 000001: 0.800V 000010: 0.850V 000011: 0.900V 000100: 0.950V 000101: 1.000V 000110: 1.050V 000111: 1.100V 001000: 1.150V 001001: 1.200V 001010: 1.250V 001011: 1.300V 001100: 1.350V 001101: 1.400V 001110: 1.450V 001111: 1.500V 010000: 1.550V 010001: 1.600V 010010: 1.650V 010011: 1.700V 010100: 1.750V 010101: 1.800V 010110: 1.850V 010111: 1.900V 011000: 1.950V 011001: 2.000V 011010: 2.050V 011011: 2.100V 011100: 2.150V 011101: 2.200V 011110: 2.250V 011111: 2.300V 100000: 2.350V 100001: 2.400V 100010: 2.450V 100011: 2.500V	

				100100: 2.550V 100101: 2.600V 100110: 2.650V 100111: 2.700V 101000: 2.750V 101001: 2.800V 101010: 2.850V 101011: 2.900V 101100: 2.950V 101101: 3.000V 101110: 3.050V 101111: 3.100V 110000: 3.150V 110001: 3.200V 110010: 3.250V 110011: 3.300V 110100: 3.350V 110101: 3.400V 110110: 3.450V 110111: 3.500V 111000: 3.550V 111001: 3.600V 111010: 3.650V 111011: 3.700V 111100: 3.750V 111101: 3.800V 111110: 3.850V 111111: 3.900V
6-7	R/W	Reserved		

18.22 LDO1CTRL

LDO1 Control Register		Addr:0x3B	R:O	Reset: MAX8997: 0xF2hex MAX8966: 0x32hex
BIT	Mode	Name	Reset	Description

5:0	R/W	OUT1[5:0]	0x32 (3.3V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE1	11: MAX8997 00: MAX8966	Enable Mode Control. 00: Output OFF (regardless of PWREN) 01: Output ON/OFF controlled by PWREN PWREN=1: Output ON in normal mode PWREN=0: Output OFF 10: Output On with Green Mode by PWREN [PWREN=1 : Output On with Normal Mode] [PWREN=0: Output On with Low Power Mode] 11: Output ON with Normal Mode (regardless of PWREN)				

18.23 LDO2CTRL

LDO2 Control Register			Addr:0x3C	R:O	Reset: MAX8997: 0xC6hex MAX8966: 0xC8hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT2[5:0]	MAX8997: 0x06 (1.1V) MAX8966: 0x08 (1.2V)	0x00: 0.80V (1.1V)	0x10: 1.60V 2.40V	0x20: 3.20V	0x30: 3.20V	
				0x01: 0.85V (1.2V)	0x11: 1.65V 2.45V	0x21: 3.25V	0x31: 3.25V	
				0x02: 0.90V 1.1V	0x12: 1.70V 2.50V	0x22: 3.30V	0x32: 3.30V	
				0x03: 0.95V 1.15V	0x13: 1.75V 2.55V	0x23: 3.35V	0x33: 3.35V	
				0x04: 1.00V 1.20V	0x14: 1.80V 2.00V	0x24: 3.40V	0x34: 3.60V	
				0x05: 1.05V 1.25V	0x15: 1.85V 2.05V	0x25: 3.45V	0x35: 3.65V	
				0x06: 1.10V 1.30V	0x16: 1.90V 2.10V	0x26: 3.50V	0x36: 3.70V	
				0x07: 1.15V 1.35V	0x17: 1.95V 2.15V	0x27: 3.55V	0x37: 3.75V	
				0x08: 1.20V 1.40V	0x18: 2.00V 2.20V	0x28: 3.60V	0x38: 3.80V	
				0x09: 1.25V 1.45V	0x19: 2.05V 2.25V	0x29: 3.65V	0x39: 3.85V	
				0x0A: 1.30V 1.50V	0x1A: 2.10V 2.30V	0x2A: 3.70V	0x3A: 3.90V	
				0x0B: 1.35V 1.55V	0x1B: 2.15V 2.35V	0x2B: 3.75V	0x3B: 3.95V	
				0x0C: 1.40V 1.60V	0x1C: 2.20V 2.40V	0x2C: 3.80V	0x3C: 4.00V	
				0x0D: 1.45V 1.70V	0x1D: 2.25V 2.50V	0x2D: 3.85V	0x3D: 4.00V	
				0x0E: 1.50V 1.80V	0x1E: 2.30V 2.60V	0x2E: 3.90V	0x3E: 4.10V	
				0x0F: 1.55V 1.90V	0x1F: 2.35V 2.70V	0x2F: 3.95V	0x3F: 4.10V	
7:6	R/W	EMODE2	11	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.24 LDO3CTRL

LDO3 Control Register			Addr:0x3D	R:O	Reset: MAX8997: 0xC6hex MAX8966: 0xC8hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT3[5:0]	MAX8997: 0x06 (1.1V)	0x00:	0x10:	0x20:	0x30:	
				0.80V	1.60V	2.40V	3.20V	
				0x01:	0x11:	0x21:	0x31:	
				0.85V	1.65V	2.45V	3.25V	
				0x02:	0x12:	0x22:	0x32:	
				0.90V	1.70V	2.50V	3.30V	
				0x03:	0x13:	0x23:	0x33:	
				0.95V	1.75V	2.55V	3.35V	
				0x04:	0x14:	0x24:	0x34:	
				1.00V	1.80V	2.60V	3.40V	
				0x05:	0x15:	0x25:	0x35:	
				1.05V	1.85V	2.65V	3.45V	
				0x06:	0x16:	0x26:	0x36:	
				1.10V	1.90V	2.70V	3.50V	
				0x07:	0x17:	0x27:	0x37:	
7:6	R/W	EMODE3	11	1.15V	1.95V	2.75V	3.55V	
				0x08:	0x18:	0x28:	0x38:	
				1.20V	2.00V	2.80V	3.60V	
				0x09:	0x19:	0x29:	0x39:	
				1.25V	2.05V	2.85V	3.65V	
				0x0A:	0x1A:	0x2A:	0x3A:	
				1.30V	2.10V	2.90V	3.70V	
				0x0B:	0x1B:	0x2B:	0x3B:	
				1.35V	2.15V	2.95V	3.75V	
				0x0C:	0x1C:	0x2C:	0x3C:	
				1.40V	2.20V	3.00V	3.80V	
				0x0D:	0x1D:	0x2D:	0x3D:	
				1.45V	2.25V	3.05V	3.85V	
				0x0E:	0x1E:	0x2E:	0x3E:	
				1.50V	2.30V	3.10V	3.90V	
				0x0F:	0x1F:	0x2F:	0x3F:	
				1.55V	2.35V	3.15V	3.95V	

18.25 LDO4CTRL

LDO4 Control Register			Addr: 0x3E	R:O	Reset: MAX8997: 0xD4hex MAX8966: 0x14hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT4[5:0]	0x14 (1.8V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE4	MAX8997: 11 MAX8966: 00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.26 LDO5CTRL

LDO5 Control Register			Addr: 0x3F	R:O	Reset: MAX8997: 0xC8hex MAX8966: 0x08hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT5[5:0]	0x08 (1.2V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE5	MAX8997: 11 MAX8966: 00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.27 LDO6CTRL

LDO6 Control Register			Addr: 0x40	R:O	Reset: 0xD4 hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT6[5:0]	0x14 (1.8V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE6	11	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0 with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.28 LDO7CTRL

LDO7 Control Register			Addr:0x41	R:O	Reset: MAX8997: 0xD4hex MAX8966: 0x14hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT7[5:0]	0x14 (1.8V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE7	MAX8997:11 MAX8966:00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.29 LDO8CTRL

LDO8 Control Register			Addr:0x42	R:O	Reset: 0xF2hex		
BIT	Mode	Name	Reset	Description			
5:0	R/W	OUT8[5:0]	0x32 (3.3V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V
7:6	R/W	EMODE8	11	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode			

18.30 LDO9CTRL

LDO9 Control Register			Addr: 0x43	R:O	Reset: 0xE8 hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT9[5:0]	0x28 (2.8V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE9	11	Enable Mode Control 00: OFF is not available (always ON) 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.31 LDO10CTRL

LDO10 Control Register	Addr: 0x44	R: O	Reset: MAX8997: 0xC6hex MAX8966: 0xC8hex
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BIT	Mode	Name	Reset	Description			
5:0	R/W	OUT10[5:0]	MAX8997: 0x06 (1.1V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
			MAX8966: 0x08 (1.2V)	0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V
7:6	R/W	EMODE10	11	Enable Mode Control. 00: Output OFF (regardless of PWREN) 01: Output ON/OFF controlled by PWREN PWREN=1: Output ON in normal mode PWREN=0: Output OFF 10: Output On with Green Mode by PWREN [PWREN=1 : Output On with Normal Mode] [PWREN=0: Output On with Green Mode] 11: Output ON with Normal Mode (regardless of PWREN)			

18.32 LDO11CTRL

LDO11 Control Register		Addr: 0x45	R: O	Reset: 0x28 hex
BIT	Mode	Name	Reset	Description

5:0	R/W	OUT11[5:0]	0x28 (2.8V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE11	00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.33 LDO12CTRL

LDO12 Control Register			Addr: 0x46	R: O	Reset: 0x08 hex
BIT	Mode	Name	Reset	Description	

5:0	R/W	OUT12[5:0]	0x08 (1.2V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE12	00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.34 LDO13CTRL

LDO13 Control Register			Addr: 0x47	R: O	Reset: 0x28 hex
BIT	Mode	Name	Reset	Description	

5:0	R/W	OUT13[5:0]	0x28 (2.8V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE13	00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.35 LDO14CTRL

LDO14 Control Register			Addr:0x48	R: O	Reset: 0x14 hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	OUT14[5:0]	0x14 (1.8V)		

				0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE14	00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.36 LDO15CTRL

LDO15 Control Register			Addr: 0x49	R:O	Reset MAX8997: 0x28hex MAX8966: 0xE8hex			
BIT	Mode	Name	Reset	Description				
5:0	R/W	OUT15[5:0]	0x28 (2.8V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE15	MAX8997:00 MAX8966:11	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.37 LDO16CTRL

LDO6 Control Register	Addr:0x4A	R: O	Reset: MAX8997: 0x32hex MAX8966: 0x24hex
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BIT	Mode	Name	Reset	Description			
5:0	R/W	OUT16[5:0]	MAX8997; 0x32h (3.3V) MAX8966: 0x24h (2.6V)	0x00:	0x10:	0x20:	0x30:
				0.80V	1.60V	2.40V	3.20V
				0x01:	0x11:	0x21:	0x31:
				0.85V	1.65V	2.45V	3.25V
				0x02:	0x12:	0x22:	0x32:
				0.90V	1.70V	2.50V	3.30V
				0x03:	0x13:	0x23:	0x33:
				0.95V	1.75V	2.55V	3.35V
				0x04:	0x14:	0x24:	0x34:
				1.00V	1.80V	2.60V	3.40V
				0x05:	0x15:	0x25:	0x35:
				1.05V	1.85V	2.65V	3.45V
				0x06:	0x16:	0x26:	0x36:
				1.10V	1.90V	2.70V	3.50V
				0x07:	0x17:	0x27:	0x37:
				1.15V	1.95V	2.75V	3.55V
7:6	R/W	EMODE16	00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode			

18.38 LDO17CTRL

LDO17 Control Register		Addr: 0x4B	R: O	Reset: 0x32 hex
BIT	Mode	Name	Reset	Description

5:0	R/W	OUT17[5:0]	0x32 (3.3V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE17	00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.39 LDO18CTRL

LDO18 Control Register			Addr:0x4C	R: O	Reset: 0x32 hex
BIT	Mode	Name	Reset	Description	

5:0	R/W	OUT18[5:0]	0x32 (3.3V)	0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V	
				0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V	
				0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V	
				0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V	
				0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V	
				0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V	
				0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V	
				0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V	
				0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V	
				0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V	
				0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V	
				0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V	
				0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V	
				0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V	
				0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V	
				0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V	
7:6	R/W	EMODE18	00	Enable Mode Control 00: Output off 01: Output On with Green Mode 10: Output On with Green Mode if PWREN=0. with Normal Mode if PWREN=1. 11: Output On with Normal Mode				

18.40 LDO21CTRL

LDO21 Control Register			Addr:0x4D	R: O	Reset: MAX8997: 0xC8hex MAX8966: 0x08hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	OUT21[5:0]	0x08 (1.2V)		

			0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V		
			0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V		
			0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V		
			0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V		
			0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V		
			0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V		
			0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V		
			0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V		
			0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V		
			0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V		
			0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V		
			0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V		
			0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V		
			0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V		
			0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V		
			0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V		
7:6	R/W	EMODE21	MAX8997: 11 MAX8966: 00	Enable Mode Control. 00: Output OFF (regardless of PWREN) 01: Output ON/OFF controlled by PWREN PWREN=1: Output ON in normal mode PWREN=0: Output OFF 10: Output On with Green Mode by PWREN [PWREN=1 : Output On with Normal Mode] [PWREN=0: Output On with Green Mode] 11: Output ON with Normal Mode (regardless of PWREN)				

Reserved 0x4E Register

Reserved 0x4F Register

18.41 MBCCTRL1-Main Battery Control Register1

MBCCTRL1 – Main battery control register 1			Addr:0x50	R: O	Reset; A4hex
BIT	Mode	Name	Reset	Description	
2:0	R	Not used	100	Not used	
3	R	Not used	0	Not used	
6:4	R/W	TFCH[2:0]	010	Fast charge timer setting for fast charging process 010: 5hr 011: 6hr 100: 7hr 111: disable the total charge timer. None of above: 5hr	
7	R/W	ENVICHG	1	Enable VICHG 0: Disable VICHG 1: Enable VICHG	

18.42 MBCCTRL2 – Main battery control register 2

MBCCTRL2 – Main battery control register 2			Addr:0x51	R: O	Reset; D4hex
BIT	Mode	Name	Reset	Description	
2:0	R	Not used	100	Not used	
5:3	R	Not used	010	Not used	
6	R/W	MBCHOSTEN *note	1	MBC enable from host 1: enable 0: disable	
7	R/W	VCHGR_FC	1	Charger Fast Charge enable from the host: 1: enable Fast Charge 0: disable Fast Charge and stay at prequalification current	

Note: Reset values will be restored if PMU exits HOSTON state.

18.43 MBCCTRL3 – Main battery control register 3

MBCCTRL3 – Main battery control register 3			Addr:0x52	R: O	Reset; A0hex
BIT	Mode	Name	Reset	Description	
3:0	R/W	MBCCV[3:0]	0000	Charger CV mode regulated voltage selection, controlled by software. 0000: 4.20V (for normal RC2 mode) 0001: 4.00V 0010: 4.02V 0011: 4.04V 0100: 4.06V 0101: 4.08V . . 1110: 4.28V 1111: 4.35V	
7:4	R	Not used	1010	Not used	

18.44 MBCCTRL4 – Main battery control register 4

MBCCTRL4 – Main battery control register 4			Addr:0x53	R: O	Reset; 15hex
BIT	Mode	Name	Reset	Description	
3:0	R/W	MBCICHFC[3:0]	0101	0000: 200mA 0001: 250mA 0010: 300mA 0011: 350mA 0100: 400mA 0101: 450mA 0110: 500mA 0111: 550mA 1000: 600mA 1001: 650mA 1010: 700mA 1011: 750mA 1100: 800mA 1101: 850mA 1110: 900mA 1111: 950mA	
4	R/W	MBCICHFCSET	1	1: 200mA to 950mA settings 0: 90mA	
7-5	R	Not used	000	Not used	

18.45 MBCCTRL5 – Main battery control register 5

MBCCTRL5 – Main battery control register 5			Addr: 0x54	R:O	Reset;20hex
BIT	Mode	Name	Reset	Description	
3:0	R/W	ITOPOFF[3:0]	0000	TOP OFF Current. End of charge current threshold level (typical case). 0000: 50mA 0001: 60mA 0010: 70mA 0011: 80mA 0100: 90mA 0101: 100mA 0110: 110mA 0111: 120mA 1000: 130mA 1001: 140mA 1010: 150mA 1011: 160mA 1100: 170mA 1101: 180mA 1110: 190mA 1111: 200mA	
7-4	R	Not used	0010	Not used	

18.46 MBCCTRL6 – Main battery control register 6

MBCCTRL6– Main battery control register 6			Addr: 0x55	R: O	Reset;71hex
BIT	Mode	Name	Reset	Description	
4:0	R	Not used	10001	Not used	

5	R/W	AUTOSTOP	1	AUTOSTOP Pause of charging process enable/disable 0: Pause of charging disabled. 1: Pause of charging enabled.
7-6	R	Not used	01	Not used

18.47 OTPCGHCVS – Charger Input OVP threshold

OTPCGHCVS – Charger Input OVP threshold			Addr: 0x56	R: S	Reset: 00hex
1:0	R/W	OTPCGHCVS[1:0]	00	00: 7.5V 01: 6.0V 10: 6.5V 11: 7.0V	
7:2	R	Reserved	000000	Reserved	

Reserved ;0x57h

Reserved ;0x58h

Reserved ;0x59h

18.48 SAFEOUTCTRL

SAFEOUT Linear regulator control register			Addr: 0x5A	R: S1	Reset: 75 hex
BIT	Mode	Name	Reset	Description	
1:0	R/W	SAFEOUT1[1:0]	01	SAFEOUT1 output voltage 00: 4.85V. 01: 4.90V 10: 4.95V 11: 3.3V.	
3:2	R/W	SAFEOUT2[3:2]	01	SAFEOUT2 Output voltage 00: 4.85V. 01: 4.90V 10: 4.95V 11: 3.3V.	
4	R/W	ACTDISSAFE0 1	1	SAFEOUT1 active discharger 0: No active discharge 1: Active discharge	
5	R/W	ACTDISSAFE0 2	1	SAFEOUT2 active discharger 0: No active discharge 1: Active discharge	
6	R/W	ENSAFEOUT1	1	SAFEOUT1 Enable bit 0; Disable SAFEOUT1 1; Enable SAFEOUT1	
7	R/W	ENSAFEOUT2	0	SAFEOUT2 Enable bit 0; Disable SAFEOUT2 1; Enable SAFEOUT2	

Reserved 0x5B Register

Reserved 0x5C Register

Reserved 0x5D Register

18.49 LBCNFG1

LBCNFG1			Addr:0x5E	R: O	Reset: 0xD7
BIT	Mode	Name	Reset	Description	
0	R/W	<i>LBITH</i>	1	<i>Low Main-Battery 1st threshold voltage (V_{BATT_falling})</i> <i>0b000=2.9V</i> <i>0b001=3.0V</i> <i>0b010=3.1V</i> <i>0b011=3.2V</i> <i>0b100=3.3V</i> <i>0b101=3.4V</i> <i>0b110=3.5V</i> <i>0b111=3.57V (Default)</i>	
1	R/W		1		
2	R/W		1		
3	R/W	Reserved	0		
4	R/W	<i>LB1HYST</i>	1	<i>Low Main-Battery 1st Comparator Hysteresis</i> <i>0b00=100mV</i> <i>0b01=200mV (Default)</i> <i>0b10=300mV</i> <i>0b11=400mV</i>	
5	R/W		0		
6	R/W	LB1EN	1	<i>Low Main-Battery Comparator Enable</i> <i>0 = Comparator Disabled</i> <i>1 = Comparator Enabled</i>	
7	R/W	LB1DAC_EN	1	<i>Low Main-Battery DAC Enable</i> <i>0 = DAC Disabled</i> <i>1 = DAC Enabled</i>	

18.50 LBCNFG2

LBCNFG2			Addr:0x5F	R: O	Reset: 0xD4
BIT	Mode	Name	Reset	Description	
0	R/W	<i>LB2TH</i>	0	<i>Low Main-Battery 2nd threshold voltage (V_{BATT_falling})</i> <i>0b000=2.9V</i> <i>0b001=3.0V</i> <i>0b010=3.1V</i> <i>0b011=3.2V</i> <i>0b100=3.3V (Default)</i> <i>0b101=3.4V</i> <i>0b110=3.5V</i> <i>0b111=3.57V</i>	
1	R/W		0		
2	R/W		1		
3	R/W	Reserved	0		
4	R/W	<i>LB2HYST</i>	1	<i>Low Main-Battery 2nd Comparator Hysteresis</i> <i>0b00=100mV</i> <i>0b01=200mV (Default)</i> <i>0b10=300mV</i> <i>0b11=400mV</i>	
5	R/W		0		
6	R/W	LB2EN	1	<i>Low Main-Battery Comparator Enable</i> <i>0 = Comparator Disabled</i> <i>1 = Comparator Enabled</i>	
7	R/W	LB2DAC_EN	1	<i>Low Main-Battery DAC Enable</i> <i>0 = DAC Disabled</i> <i>1 = DAC Enabled</i>	

18.51 BBCCTRL – Backup battery charger control register

BBCCTRL – Backup battery charger control register			Addr: 0x60	R: S	4Fhex
BIT	Mode	Name	Reset	Description	
0	R/W	BBCHOSTEN	1	HOST enable backup battery charger (overwrite the MBCEN in MBC controllers) 0: backup battery charger off	

				1: backup battery charger on
2:1	R/W	BBCCS[1:0]	11	Charging current setting BBCLOWIEN = 0 00: 80uA 01: 80uA 10: 80uA 11: 100uA (Default) BBCLOWIEN = 1 00: 200uA 01: 600uA 10: 800uA 11: 400uA
4:3	R/W	BBCVS[1:0]	01	Limit voltage setting 00: 2.5V 01: 3.0V (default) 10: 3.3V 11: 3.5V
5	R/W	BBCLOWIEN	0	Low charging current enable 0:enable 1:disable
7:6	R/W	BBCRS1, BBCRS	01	Output Resistor {BBCRS1, BBCRS} combination 00: Bypass 1K 01: 1K (default) 10: 3K 11: 6K

Reserved 0x61 Register

Reserved 0x62 Register

18.52 FLASH LED DRIVER

18.52.1 FLASH1_CUR

This register contains FLED1 Flash mode current control values

FLASH1 CURRENT control register			Addr: 0x63	R: O	Reset: 00 hex
BIT	Mode	Name	Reset	Description	
0	R/W	RESERVED	0		
1	R/W	RESERVED	0		
2	R/W	RESERVED	0		
3	R/W	FLASH1	00000	FLED1 Flash mode current setting	
4	R/W			00000 23.44 mA(Default)	
5	R/W			00001 46.88 mA	
6	R/W			00010 70.32 mA	
7	R/W			00011 93.76 mA	
				...	
				11100 679.68 mA	
				11101 703.12 mA	
				11110 726.56 mA	
				11111 750.000 mA	

18.52.2 FLASH2_CUR

This register contains FLED2 Flash mode current control values

FLASH2 CURRENT control register			Addr: 0x64	R: O	Reset: 00 hex

BIT	Mode	Name	Reset	Description
0	R/W	RESERVED	0	
1	R/W	RESERVED	0	
2	R/W	RESERVED	0	
3	R/W	FLASH2	00000	FLED2 Flash mode current setting 00000 23.44 mA(Default) 00001 46.88 mA 00010 70.32 mA 00011 93.76 mA ... 11100 679.68 mA 11101 703.12 mA 11110 726.56 mA 11111 750.000 mA
4	R/W			
5	R/W			
6	R/W			
7	R/W			

18.52.3 MOVIE_CUR

This register contains FLED1 and FLED2 Movie mode current values

MOVIE CURRENT register			Addr:0x65	R: O	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	RESERVED	0		
1	R/W	RESERVED	0		
2	R/W	RESERVED	0		
3	R/W	RESERVED	0		
4	R/W	MOVIE	0000	FLED1/FLED2 Movie mode current	
5	R/W			0000 15.625 mA (Default)	
6	R/W			0001 31.250 mA	
7	R/W			0010 49.875 mA	
				0011 62.500 mA	
				0100 78.125 mA	
				0101 93.750 mA	
				0110 109.375 mA	
				0111 125.000 mA	
				1000 140.625 mA	
				1001 156.250 mA	
				1010 171.875 mA	
				1011 187.500 mA	
				1100 203.125 mA	
				1101 218.750 mA	
				1110 234.375 mA	
				1111 250.000 mA	

18.52.4 GSMB_CUR

This register contains FLED1 and FLED2 Flash Mode current control values for the GSMB function

GSMB control register			Addr: 0x66	R: O	Reset: C0 hex
BIT	Mode	Name	Reset	Description	
0	R/W	RESERVED	0		

1	R/W	RESERVED	0	
2	R/W			GSMB current setting for FLED1/FLED2 current driver. 0000 15.625 mA (Default) 0001 31.250 mA 0010 49.875 mA 0011 62.500 mA 0100 78.125 mA 0101 93.750 mA 0110 109.375 mA 0111 125.000 mA 1000 140.625 mA 1001 156.250 mA 1010 171.875 mA 1011 187.500 mA 1100 203.125 mA 1101 218.750 mA 1110 234.375 mA 1111 250.000 mA
3	R/W	GSMB	0000	
4	R/W			GSM blank polarity control 0 GSMB is active low 1 GSMB is active high (Default)
5	R/W			GSM blank Enable 0 GSMB input is disabled 1 GSMB input is enabled (Default)
6	R/W	GSMB_POL	1	
7	R/W	GSMB_EN	1	

18.52.5 BOOST_CNTL

This register contains Boost converter control values

FLASH BOOST CONVERTER Control Register			Addr: 0x67	R: O	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	BOOST_CNTL	0000	Boost Converter Output Voltage	
				0000	3.7 V
				0001	3.8 V
				0010	3.9 V
				0011	4.0 V
				0100	4.1 V
				0101	4.2 V
				0110	4.3 V
				0111	4.4 V
				1000	4.5 V
				1001	4.6 V
				1010	4.7 V
				1011	4.8 V
				1100	4.9 V
				1101	5.0 V
				1110	5.1 V
				1111	5.2 V
4	R/W	BOOST_MODE	00	00	Boost voltage set adaptive(Default)
				01	Boost voltage set programmatically according to BOOST_CNTL[3:0]
				10	Boost converter runs in drop-out
				11	Reserved for future use
6	R/W	BOOST_EN	0	BOOST CONVERTER enable 0: Boost converter off 1: Boost converter on	
				Boost Converter must be ON for Flash or Movie event	
7	R/W	RESERVED	0		

18.52.6 LED_CNTL

This register contains FLED1, FLED2 on/off and mode control

LED ON/OFF control register			Addr: 0x68	R: O	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	FLASH_EN	000	FLASH mode current driver enable (FLED1/FLED2)	
				000 FLED1 and FLED2 FLASH Disabled	
1	R/W			001 FLED1 FLASH mode enabled, FLED2 Flash mode disabled	
				010 FLED2 FLASH mode enabled, FLED1 FLASH mode disabled	
2	R/W			011 FLED1 and FLED2 FLASH mode enabled	
				100 Not Valid	
				101 FLED1 Flash mode controlled by FLED_EN, FLED2 Flash mode disabled	
				110 FLED2 Flash mode controlled by FLED_EN, FLED1 Flash mode disabled	
				111 FLED1 and FLED2 FLASH mode controlled by FLED_EN	
3	R/W	MOVIE_EN	000	MOVIE mode current driver enable of FLED1/FLED2 Current Driver	
				000 FLED1 and FLED2 MOVIE mode disabled	
4	R/W			001 FLED1 MOVIE mode enabled, FLED2 MOVIE mode disabled	
				010 FLED2 MOVIE mode enabled, FLED1 MOVIE mode disabled	
5	R/W			011 FLED1 and FLED2 MOVIE mode enabled	
				100 Not Valid	
				101 FLED1 MOVIE mode controlled by FLED_EN, FLED2 MOVIE mode disabled	
				110 FLED2 MOVIE mode controlled by FLED_EN, FLED1 MOVIE mode disabled	
				111 FLED1 and FLED2 MOVIE mode controlled by FLED_EN	
6	R/W	RESERVED	0		
7	R/W	RESERVED	0		

18.52.7 FLASH_CNTL

This register contains Flash Safety Timer function control values

FLASH TIMER control register			Addr: 0x69	R: O	Reset: 00 hex
BIT	Mode	Name	Reset	Description	
0	R/W	TMR_DUR	00000	Flash Safety timer duration control 00000 25 msec (Default) 00001 50 msec 00010 75 msec 00011 100 msec ... 11100 725 msec 11101 750 msec 11110 775 msec 11111 800 msec	
1	R/W				
2	R/W				
3	R/W				
4	R/W				
5	R/W	RESERVED	0		
6	R/W	TMR_MODE	0	Flash Safety timer control 0: One-Shot Mode, this will generate a flash pulse with a duration time defined in TMR_DUR[4:0] regardless of FLED_EN, and I ² C setting. (Default) 1: Maximum timer mode, this will insure that Flash duration time doesn't exceed the timer defined in TMR_DUR[4:0].	
7	R/W	TMR_CNTL	0	Flash Safety Timer Reset Control 0: Enable Flash Safety Reset Timer. Only valid when FLASH mode is enabled using the FLED_EN. FLED_EN needs to be pulled low for minimum 30ms (typ) to reset the flash safety. (Default) 1: Disable Flash Safety Reset Timer. Flash safety timer is reset as soon as FLED_EN is pulled low.	

18.52.8 WDT_CNTL

This register contains Watch Dog Timer function control values

WATCH DOG TIMER control register			Addr: 0x6A	R: O	Reset: 00 hex
BIT	Mode	Name	Reset	Description	
0	R/W	RESERVED	0		
1	R/W	RESERVED	0		
2	R/W	RESERVED	0		
3	R/W	RESERVED	0		
4	R/W	WDT_RST	0	Watch Dog Timer Reset 0 (Default) 1 Writing a "1" will reset the Watch Dog Timer, after writing a "1" this bit will be cleared upon Watch Dog Timer resetting.	
5	R/W	WDT_DUR	00	Watch Dog Timer Duration 00 4 sec 01 8 sec 10 12 sec 11 16 sec	
6	R/W				

7	R/W	WDT_EN	0	Enable/Disable of Watch Dog Timer function 0 WDT disabled (Default) 1 WDT enabled
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18.52.9 MAXFLASH1

This register contains MAXFLASH control functions

MAXFLASH1 control register			Addr: 0x6B	R: O	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	LB_HYS	00	Low battery detection hysteresis	
1	R/W			00 100mV 01 200mV 10 300mV 11 Hysteresis disabled. Flash current is only reduced.	
2	R/W	LB_CNTL	00000	LOW battery detection threshold	
3	R/W			00000 2.400V 00001 2.433V 00010 2.466V 00011 2.500V 00100 2.533V 00101 2.566V 00110 2.600V 00111 2.633V 01000 2.666V 01001 2.700V 01010 2.733V 01011 2.766V 01100 2.800V 01101 2.833V 01110 2.866V 01111 2.900V 10000 2.933V 10001 2.966V 10010 3.000V 10011 3.033V 10100 3.066V 10101 3.100V 10110 3.133V 10111 3.166V 11000 3.200V 11001 3.233V 11010 3.266V 11011 3.300V 11100 3.333V 11101 3.366V 11110 3.400V 11111 3.433V	
4	R/W				
5	R/W				
6	R/W				
7	R/W	LB_EN	0	MAXFLASH function enable 0: Disabled (Default) 1: Enabled	

18.52.10 MAXFLASH2

This register contains MAXFLASH control functions

MAXFLASH2 control register			Addr: 0x6C	R: O	Reset: 00 hex
BIT	Mode	Name	Reset	Description	
0	R/W	LB_TMR_F	000	Low battery falling inhibit period 000 250 usec (Default)	

1	R/W			001 500 usec 010 750 usec 011 1000 usec 100 1250 usec 101 1500 usec 110 1750 usec 111 2000 usec
2	R/W			Low battery rising inhibit period 000 250 usec (Default) 001 500 usec 010 750 usec 011 1000 usec 100 1250 usec 101 1500 usec 110 1750 usec 111 2000 usec
3	R/W	LB_TMR_R	000	Low battery rising inhibit period 000 250 usec (Default) 001 500 usec 010 750 usec 011 1000 usec 100 1250 usec 101 1500 usec 110 1750 usec 111 2000 usec
4	R/W			
5	R/W			
6	R/W	RESERVED	0	
7	R/W	RESERVED	0	

18.52.11 INTERRUPT/STATUS

This register contains flash driver interrupt and status information

FLASH STATUS control register			Addr: 0x6D	R: O	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/C	FLED1_FLT	0	FLED1 status read back 0 FLED1 status OK (Default) 1 Fault (open/short) occurred on FLED1	
1	R/C	FLED2_FLT	0	FLED2 status read back 0 FLED2 status OK (Default) 1 Fault (open/short) occurred on FLED2	
2	R/C	ILIM_FLT	0	Current Limit status read back. 0 Boost current within limit (Default) 1 Boost current exceeds limit	
3	R/C	OVER_TEMP	0	Die temperature over load condition status read back 0 Die temp within spec (Default) 1 Die over-temp event occurred	
4	R/C	ADAPT_FLT	0	Adaptive mode regulation status read back. 0 LED cathode voltage is regulated (Default) 1 LED cathode voltage regulation fault occurred	
5	R/C	POK_FLT	0	POK window cooperator status read back 0 Output voltage is within POK window (Default) 1 POK fault occurred	
6	R/C	GSMB	0	GSMB status read back 0 GSMB event has not occurred (Default) 1 GSMB event has occurred	
7	R/C	MAXFLASH	0	MAXFLASH function status read back 0 MAXFLASH event has not occurred (Default) 1 MAXFLASH event has occurred.	

Note: All faults are latched. Bit(s) are cleared after reading register contents.

This register can be used for Status Register when interrupt is masked.

18.52.12 STATUS MASK

This register contains status information

STATUS MASK register			Addr: 0x6E	R: O	Reset: 00 hex
BIT	Mode	Name	Reset	Description	
0	R/W	FLED1_FLTm	0	0: not masked 1: masked	
1	R/W	FLED2_FLTm	0	0: not masked 1: masked	
2	R/W	ILIM_FLTm	0	0: not masked 1: masked	
3	R/W	OVER_TEMPm	0	0: not masked 1: masked	
4	R/W	ADAPT_FLTm	0	0: not masked 1: masked	
5	R/W	POK_FLTm	0	0: not masked 1: masked	
6	R/W	GSMBm	0	0: not masked 1: masked	
7	R/W	MAXFLASHm	0	0: not masked 1: masked	

Reserved 0x6F register

18.53 GPIOs

GPIO0 Configuration Register

GPIOCNTL0			Addr: 0x70h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN_</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0). 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.	
5	R/W				
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u> 00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms	
7	R/W				

GPIO1 Configuration Register

GPIOCNTL1			Addr: 0x71h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN_</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system	

				controller. 0: Electrical low 1: Electrical high
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> <i>When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0).</i> 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.
5	R/W			
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u> 00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms
7	R/W			

GPIO2 Configuration Register

GPIOCTL2			Addr: 0x72h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated.</i> When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> <i>When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0).</i> 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin	

5	R/W			(2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u>
7	R/W			00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms

GPIO3 Configuration Register

GPIOCTL3			Addr: 0x73h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0). 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.	
5	R/W				
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u>	
7	R/W			00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms	

GPIO4 Configuration Register

GPIOCNTL4			Addr: 0x74h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN_</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0). 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read.	
5	R/W			00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.	
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u> 00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms	
7	R/W				

GPIO5 Configuration Register

GPIOCNTL5			Addr: 0x75h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN_</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller.	

				0: Electrical low 1: Electrical high
3	R/W	DATAOUT	1	<p>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</p> <p>When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0).</p> <p>0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)</p>
4	R/W	INTCNT	00	<p>These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to</p> <p>(1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source.</p> <p>This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read.</p> <p>00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.</p>
5	R/W			
6	R/W	GPIDBNC	00	<p>When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u></p> <p>00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms</p>
7	R/W			

GPIO6 Configuration Register

GPIOCTL6			Addr: 0x76h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<p>DATAIN_: When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated.</p> <p>When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller.</p> <p>0: Electrical low 1: Electrical high</p>	
3	R/W	DATAOUT	1	<p>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</p> <p>When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0).</p> <p>0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)</p>	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to	
				(1) set interrupt at PR77 IRQ1 pin	

5	R/W			(2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u>
7	R/W			00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms

GPIO7 Configuration Register

GPIOCTL7			Addr: 0x77h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN_</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0). 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.	
5	R/W				
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u>	
7	R/W			00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms	

				11: Debounce edge(s) per D5,D4 for 30ms
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GPIO8 Configuration Register

GPIOCNTL8			Addr: 0x78h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> <i>When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0).</i> 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read.	
5	R/W			00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.	
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u>	
7	R/W			00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms	

GPIO9 Configuration Register

GPIOCNTL9			Addr: 0x79h	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not	

				required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_. When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0). 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)</i>
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.
5	R/W			
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u> 00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms
7	R/W			

GPIO10 Configuration Register

GPIOCTL10			Addr: 0x7Ah	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN_</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_. When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0). 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)</i>	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin	

5	R/W			(2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u>
7	R/W			00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms

GPIO11 Configuration Register

GPIOCTL11			Addr: 0x7Bh	R: O	Reset: 0x08hex
BIT	Mode	Name	Reset	Description	
0	R/W	DRV	0	This bit is used to set the type of GPIO output stage. 0: Open Drain Output 1: CMOS (Push-Pull) Output	
1	R/W	DIR	0	This bit is used to assign a GPIO either as input or output. 0: Output 1: Input	
2	R/W	DATAIN	0	<i>DATAIN_</i> : When DIRECTION Bit D1= 1 (Input Mode), the value in the DATAIN bit reflects the electrical state of GPIO_ at the time the register read was initiated. When DIRECTION Bit D1= 0 (Output Mode), the content of this bit is not required to be updated on reads and is assumed to be invalid by the system controller. 0: Electrical low 1: Electrical high	
3	R/W	DATAOUT	1	<i>When DIRECTION Bit D1= 0 (Output Mode), the value in the DATA_OUT bit reflects the desired electrical output state of the GPIO_.</i> When DIRECTION Bit D1= 1 (Input Mode), the contents of this bit may still be read or written, but it is not reflected to the output until the GPIOx module is set to output mode (Bit D1= 0). 0: Electrical low 1: Electrical high (Push-pull) or High Impedance (open drain)	
4	R/W	INTCNT	00	These bits set the interrupt definition. The MASK determines if the corresponding interrupt flag bit is set or not on an interrupt. Logic 01, 10 or 11 sets the flag in the GPIOINT register. GPIO interrupt signal to (1) set interrupt at PR77 IRQ1 pin (2) go to bit 4 of INTSRC register (0x02/TBD) for host to read INT source. This signal is cleared to 0 when GPIOINT1 and/or GPIOINT2 are read. 00: Mask Interrupt 01: Interrupt on the falling edge 10: Interrupt on the rising edge 11: Interrupt on both rising and falling edges.	
5	R/W				
6	R/W	GPIDBNC	00	When configured as an input, the input signal should be debounced as specified by bits D7,D6 to insure a clean transition. <u>If debounce is enable (GPIDBNC !=0), both edges of input signal are debounced.</u>	
7	R/W			00: No debounce 01: Debounce edge(s) per D5,D4 for 10ms 10: Debounce edge(s) per D5,D4 for 20ms 11: Debounce edge(s) per D5,D4 for 30ms	

GPIO INTERRUPT REGISTER 1

GPIOINT1			Addr: 0x7Dh	R: O	Reset: 0x00h
BIT	Mode	Name	Reset	Description	
0	R/C	GPIO0	0	When a GPIO input interrupt is enabled in its GPIOCTL register, and the selected edge(s) are detected, the corresponding bit is set in the GPIOINT register. Reading this register will clear this register to 0. Reading GPIOINT2 also clear GPIO interrupt signal.	
1	R/C	GPIO1	0		
2	R/C	GPIO2	0		
3	R/C	GPIO3	0		
4	R/C	GPIO4	0		
5	R/C	GPIO5	0		
6	R/C	GPIO6	0		
7	R/C	GPIO7	0		

GPIO INTERRUPT REGISTER 2

GPIOINT1			Addr: 0x7Eh	R: O	Reset: 0x00h
BIT	Mode	Name	Reset	Description	
0	R/C	GPIO8	0	When a GPIO input interrupt is enabled in its GPIOCTL register, and the selected edge(s) are detected, the corresponding bit is set in the GPIOINT register. Reading this register will clear this register to 0. Reading GPIOINT1 also clear GPIO interrupt signal.	
1	R/C	GPIO9	0		
2	R/C	GPIO10	0		
3	R/C	GPIO11	0		
4	R/C	Reserved	0		
5	R/C	Reserved	0		
6	R/C	Reserved	0		
7	R/C	Reserved	0		

18.54 LDO1CONFIG

LDO1 Configure Register			Addr: 0x80	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0		

3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.
4	R/W			LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)
5	R/W	LDO_COMP [5:4]	01	10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.55 LDO2CONFIG

LDO2 Configure Register			Addr: 0x81	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	

5	R/W			<p>IC pin)</p> <p>10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin)</p> <p>11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD</p> <p>Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.</p>
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	<p>Overvoltage Clamp Enable</p> <p>0: disable</p> <p>1: Enable</p>

18.56 LDO3CONFIG

LDO3 Configure Register			Addr: 0x82	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W			10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.	
6	R/W	Reserved	0		

7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable
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18.57 LDO4CONFIG

LDO4 Configure Register			Addr: 0x83	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W			10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD	
		Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.			
6	R/W	Reserved	0		
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable	

18.58 LDO5CONFIG

LDO5 Configure Register			Addr: 0x84	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	

3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.
4	R/W			LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)
5	R/W	LDO_COMP [5:4]	01	10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Ovvoltage Clamp Enable 0: disable 1: Enable

18.59 LDO6CONFIG

LDO6 Configure Register			Addr: 0x85	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin) 10 = assume 500mOhms / 35nH trace impedance to	

5	R/W			remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.60 LDO7CONFIG

LDO7 Configure Register			Addr: 0x86	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W			10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.	
6	R/W	Reserved	0		
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable	

18.61 LDO8CONFIG

LDO8 Configure Register			Addr: 0x87	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W			10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.	
6	R/W	Reserved	0		
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable	

18.62 LDO9CONFIG

LDO9 Configure Register			Addr: 0x88	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	

4	R/W			LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 100mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)
5	R/W	LDO_COMP [5:4]	01	10 = assume 300mOhms / 30nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 600mOhm / 50nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.63 LDO10CONFIG

LDO10 Configure Register			Addr: 0x89	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W			LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W	LDO_COMP [5:4]	01	10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD	

				Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.64 LDO11CONFIG

LDO11 Configure Register			Addr: 0x8A	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W			10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD	
		Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.			
6	R/W	Reserved	0		
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable	

18.65 LDO12CONFIG

LDO12 Configure Register			Addr: 0x8B	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	

0	R/W	Reserved	0	
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable
2	R/W	Reserved	0	Reserved
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.
4	R/W			LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin) 10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD
5	R/W	LDO_COMP [5:4]	01	Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Ovoltage Clamp Enable 0: disable 1: Enable

18.66 LDO13CONFIG

LDO13 Configure Register			Addr: 0x8C	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote	

				capacitor – Load transient is 55mV typical (at the IC pin)
5	R/W			01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)
				10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin)
				11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD
				Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.67 LDO14CONFIG

LDO14 Configure Register			Addr: 0x8D	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin) 10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD	
5	R/W			Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.	

6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.68 LDO15CONFIG

LDO15 Configure Register			Addr: 0x8E	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W			 10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD	
6	R/W	Reserved	0		
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable	

18.69 LDO16CONFIG

LDO16 Configure Register			Addr: 0x8F	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		

1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable
2	R/W	Reserved	0	Reserved
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.
4	R/W			LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)
5	R/W	LDO_COMP [5:4]	01	10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Ovvoltage Clamp Enable 0: disable 1: Enable

18.70 LDO17CONFIG

LDO17 Configure Register			Addr: 0x90	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	

4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 100mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)
5	R/W			10 = assume 300mOhms / 30nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 600mOhm / 50nH trace impedance to remote capacitor – load transient TBD Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.71 LDO18CONFIG

LDO18 Configure Register			Addr: 0x91	R: O	Reset: A2 hex
BIT	Mode	Name	Reset	Description	
0	R/W	Reserved	0		
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable	
2	R/W	Reserved	0	Reserved	
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled.	
4	R/W	LDO_COMP [5:4]	01	LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)	
5	R/W			10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD	

				Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

18.72 LDO21CONFIG

LDO21 Configure Register			Addr: 0x92	R: O Reset: A2 hex
BIT	Mode	Name	Reset	Description
0	R/W	Reserved	0	
1	R/W	LDO_ADE	1	Active Discharge 0: disable 1: Enable
2	R/W	Reserved	0	Reserved
3	R	LDO_POK	0	Voltage OK status bit 0: LDO output is less than POK threshold and the device is in normal mode. 1: LDO output is above POK threshold or LDO is operating in its low-power mode , or LDO is disabled. LDO compensation scheme 00 = assume 50mOhm / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) 01 = assume 150mOhms / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin) 10 = assume 500mOhms / 35nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 1000mOhm / 35nH trace impedance to remote capacitor – load transient TBD
5	R/W	LDO_COMP [5:4]	01	Note that the LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.
6	R/W	Reserved	0	
7	R/W	LDO_OVCM:P_EN	1	Overvoltage Clamp Enable 0: disable 1: Enable

Reserved 0x93 Register

Reserved 0x94 Register

Reserved 0x95 Register

Reserved 0x96 Register

18.73 DVSOK TIMER for BUCK1

DVSOKTimer1 register			Addr 0x97	R: O	Reset: 03hex			
BIT	Mode	Name	Reset	Description				
4:0	R/W	DVSOKTIMER1 [4:0]	03	00000	0us	10000	128us	
				00001	8us	10001	136us	
				00010	16us	10010	144us	
				00011	24us	10011	152us	
				00100	32us	10100	160us	
				00101	40us	10101	168us	
				00110	48us	10110	176us	
				00111	56us	10111	184us	
				01000	64us	11000	192us	
				01001	72us	11001	200us	
				01010	80us	11010	208us	
				01011	88us	11011	216us	
				01100	96us	11100	224us	
				01101	104us	11101	232us	
				01110	112us	11110	240us	
				01111	120us	11111	248us	
5	R/W	Reserved	0					
6	R/W	Reserved	0					
7	R/W	Reserved	0					

Notes: Typical Buck1 inductor=1uH, Capacitor=10uF, time constant = root(LC)=3.162us
 6 x time constant = 18.97 us, Default I2C bit setting: 00011, 24us

18.74 DVSOK TIMER for BUCK2

DVSOKTimer2 register			Addr 0x98	R: O	Reset: 03hex			
BIT	Mode	Name	Reset	Description				
4:0	R/W	DVSOKTIMER2 [4:0]	03	00000	0us	10000	128us	
				00001	8us	10001	136us	
				00010	16us	10010	144us	
				00011	24us	10011	152us	
				00100	32us	10100	160us	
				00101	40us	10101	168us	
				00110	48us	10110	176us	
				00111	56us	10111	184us	
				01000	64us	11000	192us	
				01001	72us	11001	200us	
				01010	80us	11010	208us	
				01011	88us	11011	216us	
				01100	96us	11100	224us	
				01101	104us	11101	232us	
				01110	112us	11110	240us	
				01111	120us	11111	248us	
5	R/W	Reserved	0					

6	R/W	Reserved	0	
7	R/W	Reserved	0	

Notes: For Buck2,4 and 5 inductor=2.2uH, Capacitor=4.7uF, time constant = $\sqrt{LC} = 3.215\text{us}$
 $6 \times \text{time constant} = 20\text{us}$, Default I2C bit setting: 00011, 24us

18.75 DVSOK TIMER for BUCK4

DVSOKTimer4 register			Addr 0x99	R: O	Reset: 03hex			
BIT	Mode	Name	Reset	Description				
4:0	R/W	DVSOKTIMER4 [4:0]	03	00000	0us	10000	128us	
				00001	8us	10001	136us	
				00010	16us	10010	144us	
				00011	24us	10011	152us	
				00100	32us	10100	160us	
				00101	40us	10101	168us	
				00110	48us	10110	176us	
				00111	56us	10111	184us	
				01000	64us	11000	192us	
				01001	72us	11001	200us	
				01010	80us	11010	208us	
				01011	88us	11011	216us	
				01100	96us	11100	224us	
				01101	104us	11101	232us	
				01110	112us	11110	240us	
				01111	120us	11111	248us	
5	R/W	Reserved	0					
6	R/W	Reserved	0					
7	R/W	Reserved	0					

18.76 DVSOK TIMER for BUCK5

DVSOKTimer5 register			Addr 0x9A	R: O	Reset: 03hex			
BIT	Mode	Name	Reset	Description				
4:0	R/W	DVSOKTIMER5 [4:0]	03	00000	0us	10000	128us	
				00001	8us	10001	136us	
				00010	16us	10010	144us	
				00011	24us	10011	152us	
				00100	32us	10100	160us	
				00101	40us	10101	168us	
				00110	48us	10110	176us	
				00111	56us	10111	184us	
				01000	64us	11000	192us	
				01001	72us	11001	200us	
				01010	80us	11010	208us	
				01011	88us	11011	216us	
				01100	96us	11100	224us	
				01101	104us	11101	232us	
				01110	112us	11110	240us	
				01111	120us	11111	248us	

				01111	120us	11111	248us
5	R/W	Reserved	0				
6	R/W	Reserved	0				
7	R/W	Reserved	0				

19 MUIC Registers

The Slave address of the MAX8966/MAX8997's MUIC is 0100101x(**4Ahex/4Bhex**). The least significant bit is the read/write\ indicator.

19.1 Hex I2C Register Summary for MUIC section (POR: VBUS&&VBATT<VMUIC UVLO)

Address	NAME	Shared bus mode	b7	b6	b5	b4	b3	b2	b1	b0
0x00	ID									VENDOR_ID
										CHIP_REV
0x01	INT1	functional	0	0	0	0	0	ADCError	ADCLow	ADC
0x02	INT2	functional	0	0	0	VBVolt	DBChg	DCDTmr	ChgDetRun	ChgTyp
0x03	INT3	functional	0	0	0	0	MBCCHGERR	OVP	CGMBC	EOC
0x04	STATUS1	functional	0	ADCError	ADCLow					ADC
0x05	STATUS2	functional	0	VBVolt	DBChg	DCDTmr	ChgDetRun			ChgTyp
0x06	STATUS3	functional	0	0	0	0	MBCCHGERR	OVP	CGMBC	EOC
0x07	INTMASK1	functional	0	0	0	0	0	ADCErrorM	ADCLowM	ADCM
0x08	INTMASK2	functional	0	0	0	VBVoltM	DBChgM	DCDTmrM	ChgDetRunM	ChgTypM
0x09	INTMASK3	functional	0	0	0	0	MBCCHGERRM	OVP	CGMBCM	EOCM
0x0A	CDETCTRL1	functional	CDPDet	DBIdle	DBExit	DChkTm	DCD2sCt	DCDEn	ChgTypM	ChgDetEn
0x0B	RESERVED	functional	0	0	0	0	0	0	0	0
0x0C	CONTROL1	functional	IDBEN	MicEn			COMP2Sw			COMN1Sw
0x0D	CONTROL2	functional	RCPS	USBCplnt	AccDet	SFOutOrd	SFOutAsrt	CPEN	ADCEn	LowPwr
0x0E	CONTROL3	functional		WBTh		ADCDbSet	BOOTSet			JIGSet

Device ID 0x00

Bit	7	6	5	4	3	2	1	0
Name	DeviceID							VendorID
Reset Value	0	0	1	0	1	1	0	1
DeviceID	Device ID							
VendorID	Vendor Identification Maxim = 101							

INT1 0x01 (All bits are cleared after a read)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	ADCError	ADCLow	ADC
Reset Value	0	0	0	0	0	0	0	0
RESERVED								
ADCError	ADC Error Interrupt 0 = No Interrupt 1 = Interrupt							
ADCLow	ADC Low bit change Interrupt 0 = No Interrupt 1 = Interrupt							
ADC	ADC Change Interrupt 0 = No Interrupt 1 = Interrupt							

INT2 0x02 (All bits are cleared after a read)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	VBVolt	DBChg	DCDTmr	ChgDetRun	ChgTyp
Reset Value	0	0	0	0	0	0	0	0
Reserved								
VBVolt	VB Voltage Interrupt 0 = No Interrupt 1 = Interrupt							
DBChg	Dead Battery Charging Interrupt 0 = No Interrupt 1 = Interrupt							
DCDTmr	DCD Timer Interrupt 0 = No Interrupt 1 = Interrupt							
ChgDetRun	Charger Detection Running Status Interrupt 0 = No Interrupt 1 = Interrupt							
ChgTyp	Charge Type Interrupt 0 = No Interrupt 1 = Interrupt							

INT3 0x03 (All bits are cleared after a read)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved		OVP		
Reset Value	0	0	0	0	0	0	0	0
RESERVED								
OVP	VB Over Voltage Protection Interrupt 0 = No Interrupt 1 = Interrupt							
RESERVED								
RESERVED								

STATUS1 0x04

Bit	7	6	5	4	3	2	1	0
Name		ADCError	ADCLow			ADC		
Reset Value	0	0	1	1	1	1	1	1
RESERVED								
ADCError	ADC detection error has occurred— ADC cannot converge on a value due to noise or other interference 0 = ADC Detection Error has not occurred 1 = ADC Detection Error has occurred							
ADCLow	Low bit of ADC 0 = UID resistance < TBD ohms 1 = UID resistance ≥ TBD ohms							
ADC	Output of ADC 00000 = gnd 00001 = 2 00010 = 2.604 00011 = 3.208 00100 = 4.014 00101 = 4.82 00110 = 6.03 00111 = 8.03 01000 = 10.03 01001 = 12.03 01010 = 14.46							
	01011 = 17.26 01100 = 20.5 01101 = 24.07 01110 = 28.7 01111 = 34 10000 = 40.2 10001 = 49.9 10010 = 64.9 10011 = 80.07 10100 = 102 10101 = 121							
	10110 = 150 10111 = 200 11000 = 255 11001 = 301 11010 = 365 11011 = 442 11100 = 523 11101 = 619 11110 = 1000 or 1002 11111 = open							

STATUS2 0x05

Bit	7	6	5	4	3	2	1	0
Name		VBVolt	DBChg	DCDTmr	ChgDetRun	ChgTyp		
Reset Value	0	0	0	0	0	0	0	0
RESERVED								
VBVolt	Output of VB detection comparator 0 = $V_{VB} < V_{VBDET}$ 1 = $V_{VB} \geq V_{VBDET}$							
DBChg	Dead Battery Charger Mode. If DBChg=1, 45min timer is running and is not expired 0 = Not in Dead Battery Charge Mode 1 = In Dead Battery Charge Mode							
DCDTmr	Data Contact Detect Time Wait. 0 = Data Contact Detection timer not expired or not running 1 = Data Contact Detection running for >2s min							
ChgDetRun	Charger Detection State Machine Running 0 = Not Running 1 = Running							
ChgTyp	Output of USB Charger Detection 000 = nothing attached 001 = USB Cable attached. 010 = Charging Downstream port: current depends on USB operating speed 011 = dedicated charger: current up to 1.8A 100 = Special 500mA charger: Current 500mA max 101 = Special 1A charger: Current up to 1A 110 = Reserved for Future Use 111 = Dead Battery Charging – 100mA max							

STATUS3 0x06

Bit	7	6	5	4	3	2	1	0
Name						OVP		
Reset Value	0	0	0	0	0	0	0	0
RESERVED								
OVP	VB Overvoltage Protection Trip Level Indication 0 = $V_{VB} \leq V_{VBPROT}$ 1 = $V_{VB} > V_{VBPROT}$							

INTMASK1 0x07

Bit	7	6	5	4	3	2	1	0
Name						ADCErrorM	ADCLowM	ADCM
Reset Value	0	0	0	0	0	0	0	0
RESERVED								
ADCErrorM	ADC Error Interrupt Masks 0 = No Interrupt 1 = Interrupt							
ADCLowM	ADC Low bit change Interrupt Mask 0 = No Interrupt 1 = Interrupt							
ADCM	ADC Change Interrupt Mask 0 = No Interrupt 1 = Interrupt							

INTMASK2 0x08

Bit	7	6	5	4	3	2	1	0
Name				VBVoltM	DBChgM	DCDTmrM	ChgDetRunM	ChgTypM
Reset Value	0	0	0	0	0	0	0	0
RESERVED								
VBVoltM	VB Voltage Interrupt Mask 0 = No Interrupt 1 = Interrupt							
DBChgM	Dead Battery Charging Interrupt Mask 0 = No Interrupt 1 = Interrupt							
DCDTmrM	DCD Timer Interrupt Mask 0 = No Interrupt 1 = Interrupt							
ChgDetRunM	Charger Detection Running Status Interrupt Mask 0 = No Interrupt 1 = Interrupt							
ChgTypM	Charge Type Interrupt Mask 0 = No Interrupt 1 = Interrupt							

INTMASK3 0x09

Bit	7	6	5	4	3	2	1	0
Name						OVPM		
Reset Value	0	0	0	0	0	0	0	0
RESERVED								
OVPM	VB Over Voltage Protection Interrupt Mask 0 = Mask 1 = Not Masked							

CDETCTRL 0x0A

Bit	7	6	5	4	3	2	1	0
Name	CDPDet	DBIdle	DBExit	DChkTm	DCD2sCt	DCDEn	ChgTypM	ChgDetEn
Reset Value	0	0	0	0	1	1	0	1
CDPDet	USB Charger Downstream Detection method 0 = Use VDP_SRC to drive D- (reverse of D+/D- short) 1 = Use weak pull up method							
DBIdle	Dead Battery Mode Idle 0 = Normal Dead Battery Mode 1 = Idle Dead Battery Mode and Start/Restart 5sec Dead Battery Watchdog timer							
DBExit	Exit Dead Battery Charge Mode. If DBChg=1, setting DBExit =1 stops 45min timer, sets DBChg=0 and sets ChgTyp=001. DBExit is automatically reset to 0 if system reset signal asserts (RSOb asserts low). 0 = Not Exit Dead Battery Mode 1 = Exit Dead Battery Mode							
DChkTm	Sets Time for Charger Type Detection 0 = t_{DPSRC_ON} =50ms 1 = t_{DPSRC_ON} =620ms							
DCD2sCt	Automatically exit Data Contact Detection when 2s interrupt is set. 0 = Stay in DCD until normal exit 1 = always exit DCD when 2s interrupt asserts							
DCDEn	Enable Data Contact Detect State Machine. If DCD is enabled, then before D+/D- is tested for a short, DCD must pass. If set to disable, DCD is skipped and D+/D- short detection begins. If DCD is stuck (DCDTmr=1 after 2s), setting DCDEn=0 will bypass DCD and D+/D- short detection begins. 0 = Disable 1 = Enable							
ChgTypM	Charger Type Manual Detection. Set to 1 to force the internal logic to Open the COM switches and perform a charger type detection. After the detection state machine completes, this bit will reset to 0. 0 = Disabled 1 = Force a Manual Charge Detection							
ChgDetEn	Enables the USB Charger Detection for a rising edge on VB. 0 = Disabled 1 = Enabled							

CONTROL1 0x0C

Bit	7	6	5	4	3	2	1	0
Name	IDBEn	MicEn	COMP2Sw			COMN1Sw		
Reset Value	0	0	0	0	0	0	0	0
IDBEn	Connects IDB to UID 0 = Open 1 = IDB Connected to UID							
MicEn	Connects MIC to VB Note 1 0 = Open 1 = MIC Connected to VB (set MUIC_MIC_ON control line to 1)							
COMP2Sw	Control of COMP2 Switches Note 1 000 = Open 001 = COMP2 connected to DN2(USB) 010 = COMP2 connected to SR2 (Audio Right) 011 = COMP2 connected to UT2 (UART TX) 100 to 111 = Open							
COMN1Sw	Control of COMN1 Switches Note 1 000 = Open 001 = COMN1 connected to DN1(USB) 010 = COMN1 connected to SL1 (Audio Left) 011 = COMN1 connected to UT1 (UART TX) 100 to 111 = Open							

CONTROL2 0x0D

Bit	7	6	5	4	3	2	1	0
Name	RCPS	USBCplnt	AccDet	SFOutOrd	SFOutAsrt	CPEn	ADCEn	LowPwr
Reset Value	0	0	1	1	0	0	1	0
RCPS	Sets the position of the click/pop resistors on both SL1 and SR2 0 = Disabled 1 = Enabled							
USBCplnt	Sets if Battery Charger is USB2.0 compliant 0 = Not USB2.0 Compliant 1 = USB2.0 Compliant							
AccDet	Enables Factory Accessory Detection State Machine. This bit must be set to 0 when Firmware takes control of the accessory detection and configuration 0 = Disable Factory Accessory Detection State Machine 1 = Enable Factory Accessory Detection State Machine Description; 0: Normal operation mode. When firmware boots in a phone, it must set AccDet=0 and take over manual control of the MUIC. Factory Automatic mode can not be used for production ready phones. 1; Factory automatic mode. This mode is used when the phone is in factory test and to help engineers in the lab when debugging the phone design. This mode is enabled by default (AccDet=1).							
SFOutOrd	SFOUT Override control 0 = Force SFOUT to off 1 = SFOUT is automatically controlled by VB voltage present and SFOutAsrt option.							
SFOutAsrt	Time when SFOUT asserts 0 = SFOUT asserts only after a complete run of the charger detection state machine or after a correct detection of a factory cable 1 = SFOUT assert asserts always after a valid VBUS voltage detection with no wait							
CPEn	Controls the charge pump required for analog switch operation. FW can change this bit at any time. The Factory Accessory State Machine will set CPEn=1 automatically when switches are configured. 0 = Disabled 1 = Enabled							
ADCEn	Manual Control of ADC enable 0 = ADC Disabled 1 = ADC Enabled							
LowPwr	Enables no accessory low power pulse mode for ADC 0 = disable low power mode 1 = enable low power mode							

CONTROL3 0x0E

Bit	7	6	5	4	3	2	1	0						
Name	WBTh		ADCDbSet		BOOTSet		JIGSet							
Reset Value	00		00		00		00							
WBTh	USB Battery Charging Dead Battery Support weak battery threshold. 00 = 3.7V 01 = 3.5V 10 = 3.3V 11 = 3.1V													
ADCDbSet	Manual Control of ADC Debounce Time (OTP default selectable) 00 = 0.5ms 01 = 10ms 10 = 25ms 11 = 38.62ms													
BOOTSet	Manual control of BOOT pin (The initial power up value may be different depending on the resistor present on ID – factory mode) Note 2 00 = BOOT pin controlled by Auto detection 01 = BOOT pin Output Low 10 = BOOT pin output high (connected to VIO) 11 = BOOT pin Hi-Impedance													
JIGSet	Manual control of the JIG pin (The initial power up value may be different depending on the resistor present on ID – factory mode) Note 2 00 = JIG pin controlled by Auto detection 01 = JIG pin asserted (Logic High output) 10 to 11 = JIG pin not asserted (Logic low output)													

Note 1: These registers reflect the actual setting of the switches even if they are changed by a factory mode ID resistor.

Note 2: These registers reflect the actual setting of the BOOTSet and JIGSet even if they are changed by Auto Accessory detection FSM

20 Fuel Gauge

The MAX8966/MAX8997 acts as a Slave Transmitter/Receiver. The Slave address of the MAX8966/MAX8997 Fuel Gauge is 0x6Ch/0x6Dh. The least significant bit is the read/write\ indicator.

Register setting for Model Gauge 1 operation (Without current sense).

The followings are all customer need to se for Model Gauge 1 operation (Without current sense)

CGAIN(address 2E)= 0000h

MiscCFG(address 2Bh)= 0003h

LearnCFG(address 28h)=0007h

STATUS			Addr:0x00	Type:	Reset: 0002h
BIT	Mode	Name	Reset	Description	
0	R/W	X	0	POR ; Power-On Reset. This bit is set to a 1 when the IC detects that a software or hardware POR event has occurred. If the host detects that the POR bit has been set, the IC should be reconfigured. See the Power-up and Power-On Reset section. This bit must be cleared by system software to detect the next POR event. POR is set to 1 at power-up.	
1		POR	1		
2		X	0		
3		Bst	0	<i>Bst indicates if the battery is currently absent (1) or present (0).</i>	
4		X	0		
5		X	0		
6		X	0		
7		X	0		
8		Vmn	0	Smn, Tmn, and Vmn indicate that the minimum threshold was exceeded. Minimum VALrt Threshold exceeded. This bit is set to a 1 whenever a Vcell register reading is below the minimum VALRT value. This bit may or may not need to be cleared by system software to detect the next event. See the CONFIG register settings. VMN is set to 0 at power-up.	
9		Tmn	0	<i>Smn, Tmn, and Vmn indicate that the minimum threshold was exceeded. Minimum Talrt Threshold Exceeded. This bit is set to a 1 whenever a Temperature register reading is below the minimum TALRT value. This bit may or may not need to be cleared by system software to detect the next event. See the CONFIG register settings. Tmn is set to 0 at power-up.</i>	
10		Smn	0	<i>Smn, Tmn, and Vmn indicate that the minimum threshold was exceeded. Minimum SOCALRT Threshold Exceeded. This bit is set to a 1 whenever SOC fails below the minimum SOCALRT value. This bit may or may not need to be cleared by system software to detect the next event. See the CONFIG and MiscCFG register settings. Smn is set to 0 at power-up.</i>	
11		Bi	0	Bi indicates that a battery insertion event was detected. This bit is set to a 1 when the IC detects that a battery has been inserted into the system by monitoring the AIN pin. This bit must be cleared by system software to detect the next insertion event.	
12		Vmx	0	<i>Smx, Tmx, and Vmx indicate that the maximum threshold (RepSOC, Temperature, and Voltage) was exceeded. Maximum VALRT Threshold Exceeded. This bit is set to a 1 whenever a VCELL register reading is above the maximum VALRT value. This bit may or may not need to be cleared by system software to detect the next event. See the CONFIG and MiscCFG register settings. Smx is set to 0 at power-up.</i>	

			<i>be cleared by system software to detect the next event. See the CONFIG register settings. VMx is set to 0 at power-up.</i>
13	Tmx	0	<i>Smx, Tmx, and Vmx indicate that the maximum threshold (RepSOC, Temperature, and Voltage) was exceeded. Maximum TALRT Threshold Exceeded. This bit is set to a 1 whenever a Temperature register reading is above the maximum TALRT value. This bit may or may not need to be cleared by system software to detect the next event. See CONFIG register settings. Tmx is set to 0 at power up.</i>
14	Smx	0	<i>Smx, Tmx, and Vmx indicate that the maximum threshold (RepSOC, Temperature, and Voltage) was exceeded. Maximum SOCALRT Threshold Exceeded. This bit is set to a 1 whenever SOC rises above the maximum SOCALRT value. This bit may or may not need to be cleared by system software to detect the next event. See CONFIG and MiscCFG register settings.</i>
15	Br	0	<i>Battery Removal. This bit is set to a 1 when the IC detects that a battery has been removed from the system. This bit must be cleared by system software to detect the next insertion event.</i>

VALRT_Th			Addr:0x01	Type:	Reset: FF00h
BIT	Mode	Name	Reset	Description	
7:0	R&W	MinVoltageAirt	0x00	<i>Sets an alert threshold for minimum and maximum voltage. Set Max=0xFF and Min=0x00 to disable. VALRT Threshold register sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the VCELL register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 20mV resolution over the full operating range of the VCELL register. At power-up, the thresholds default to their maximum settings – FF00h(Disabled).</i>	
15:8	R&W	MaxVoltageAirt	0xFF		

TALRT_Th			Addr:0x02	Type:	Reset: FF00h
BIT	Mode	Name	Reset	Description	
7:0	R&W	MinVoltage	0x00	<i>Sets an alert threshold for minimum and maximum temperature. Set Max=0xFF and Min=0x00 to disable. The TALRT Threshold register sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the Temperature register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are stored in two's complement format and are selectable with 1oC resolution over the full operating range of the Temperature register. At power up, the thresholds default to their maximum settings- 7F80h (disabled).</i>	
15:8	R&W	MaxVoltage	0xFF		

SOCALRT_Th			Addr:0x03	Type:	Reset: FF00h
BIT	Mode	Name	Reset	Description	
7:0	R&W	MinVoltage	0x00	<i>Sets an alert for minimum and maximum SOC. This may be used for charge/discharge termination, or for power-management near empty. Set Max=0xFF and Min=0x00 to disable. The SALRT Threshold register sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the selected SOCREP, SOCAV, SOCMIX, or</i>	
15:8	R&W	MaxVoltage	0xFF		

				<p>SOCVF register values. See the SACFG bits in the MiscCFG register description for details. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 1% resolution over the full operating range of the selected SOC register.</p>
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AtRate - Rate for Empty Calculation			Addr:0x04	Type: Reset: 0000h
BIT	Mode	Name	Reset	Description
11:0	R/W	AtRate	0x0000	<p>Specifies a current rate at which to calculate AvCAP, AvSOC and TTE. 12 bit value unsigned value. Units 12.5uV/Rsns in D3. The AtRate register also host software to estimate remaining capacity, SOC, and time to empty for a theoretical load current. Whenever the AtRate register is programmed to 0 or a positive value, the IC uses A/D measurements for determining the SOCAV, RemCapAC, and TTE register values. Whenever the AtRate register is programmed to a negative value indicating a desired discharge current, the SOCAV, RemCapAV, and TTE registers calculate their values for the AtRate register theoretical current instead. The AtRate register holds a two's complement 16-bit value. Do not write this register to 8000h.</p>

RemCapREP - Report Capacity			Addr:0x05	Type: Reset: 03E8h
BIT	Mode	Name	Reset	Description
15:0	R	RemCapREP	03E8h (500mAh)	<p>RemCapREP is a filtered version of the RemCapAV register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in load current. The value is stored in terms of uVh and must be divided by the application sense-resistor value to determine remaining capacity in mAh.</p>

SOCRep - Report State of Charge in %			Addr:0x06	Type: Reset: 3200h
BIT	Mode	Name	Reset	Description
15:0	R	SOCRep	0x3200 (50%)	<p>SOCREP is a filtered version of the SOCAV register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in load current. The register value is stored as a percentage with a resolution of 0.0039% per LSB. If an 8-bit SOC value is desired, the host can read only the upper byte of the register with a resolution of 1.0%.</p>

Age - Capacity measure of age			Addr:0x07	Type: Reset: 6400h
BIT	Mode	Name	Reset	Description
15:0	R	Age	0x6400 (100%)	<p>The Age register contains a calculated percentage value of the application's present cell capacity compared to its expected capacity. The result can be used by the host to gauge the cell's health as compared to a new cell of the same type. The result is displayed as a percentage value from 0 to 256% with a 0.0039% LSb. The equation for the register output is</p> $\text{Age Register} = 100\% \times (\text{FullCAP Register}/\text{DesignCapRegister}).$

Temperature (input or output)			Addr:0x08	Type:	Reset: 1600h
BIT	Mode	Name	Reset	Description	
15:0	R/W	Temperature	0x1600 (22C)	<i>While in Active mode and TEX=0 and TEN=1 in the CONFIG register, the IC converts the AIN register value into a singed two's complement temperature value. See the TGAIN and TOFF configuration registers. The resulting data is placed in the Temperature register every 1.4sec with a resolution of +0.0039oC. If an 8-bit temperature reading is desired, the host can read only the upper byte of the Temperature register with a resolution of +1.0oC. Contents of the Temperature register are indeterminate for the first conversion cycle time period after IC power up. The last value of the Temperature register is maintained when the IC enters shutdown mode.</i>	

VCELL Register - Trimmed Cell Voltage in mV			Addr:0x09	Type:	Reset: B400h
BIT	Mode	Name	Reset	Description	
15:0	R	Vcell	0xB400 (3.6V)	<i>While in Active mode, the IC periodically measures the voltage between V_BATTFG and SNS pins over a 0 to 5.12V range. The resulting data is placed in the VCELL register every 175.8ms with an LSb value of 0.625mV. Voltages above the maximum register value are reported as the maximum value. The lower 3 bits for the VCELL register are don't care bits.</i>	

Current Register			Addr:0x0A	Type:	Reset: 0000h
BIT	Mode	Name	Reset	Description	
15:0	R	Current	0x0000	<i>While in active mode, the IC periodically measures the voltage between the SNS and KVSS pins over a +/-51.2mV range. The resulting data is stored as a two's complement value in the Current register every 175.8ms with an LSb value of 1.5625uV. Voltages outside the minimum and maximum register values are reported as the minimum or maximum value.</i>	

AverageCurrent Register			Addr:0x0B	Type:	Reset: 0000h
BIT	Mode	Name	Reset	Description	
15:0	R	AvgCurrent	0x0000	<i>The AverageCurrent register reports an average of current-register readings over a configurable 0.7s to 6.4h time period. See the FilterCFG register description for details on setting the time filter. The resulting average is placed in the AverageCurrent register with an LSb value of 1.5625uV. The first Current register reading after IC power-up sets the starting point of the AverageCurrent filter. The last value of the AverageCurrent register is maintained when the IC enters Shutdown mode.</i>	

SOCMIX - State of Charge in %			Addr:0x0D	Type:	Reset: 3200h
BIT	Mode	Name	Reset	Description	
15:0	R	SOCMIX	3200h (50%)	<i>SOCMIX register holds the calculated present state of charge of the cell before any empty compensation adjustments are performed. The register value is stored as a percentage with a resolution of 0.0039% percent per LSb. If an 8-bit state of charge value is desired, the host can read only the upper byte of the register with a</i>	

				<i>resolution of 1.0%.</i>
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SOCAv			Addr:0x0E	Type: Reset: 0x3200
BIT	Mode	Name	Reset	Description
15:0	R	SOCAv	0x3200 (50%)	SOCAv register holdsthe calculated present state of charge of the cell based on all inputs from the ModelGauge m3 algorithm including empty compensation. The register value is stored as a percentage with a resolution of 0.0039% per LSb. If an 8-bit state of charge value is desired, the host can read only the upper byte of the register with a resolution of 1.0%. The SOCAv register value is an unfiltered calculation. Jumps in the reported value can be caused by changes in the application such as a abrupt changes in load current.

RemCapMIX			Addr:0x0F	Type: Reset: 03E8h
BIT	Mode	Name	Reset	Description
15:0	R	RemCap	03E8h (500mAhr)	This is the remaining capacity with coulomb-counter + Voltage-Fuel-Gauge mixing. This does not include empty compensation, and includes any capacity which may be unavailable because of the discharge rate. Current results are accumulated every 175.8ms. <i>. The high word has 0.5mAh per LSB with 10mΩ sense resistor.</i>

FullCAP - Full Capacity			Addr:0x10	Type: Reset: 07D0h
BIT	Mode	Name	Reset	Description
15:0	R/W	FullCAP	07D0h (1000mAhr)	<i>This register holds the temperature compensated full capacity value. This also compensates for the temperature dependence of charge termination. The FullCapNom value is multiplied by a temperature correction factor (FCTC) and the result is stored in this register. 0.5mAh per LSB with 10mΩ sense resistor. This is the total capacity available to the application at full. Through the user-defined registers, ICHGTerm and DesignCap, the IC detects end-of-charge conditions as the cell is cycled. These points allow the IC to learn how much of the cell capacity is usable by the application depending on cell age and temperature.</i>

TTE - Time To Empty			Addr:0x11	Type: Reset: 0000h
BIT	Mode	Name	Reset	Description
15:0	R	TTE	0000h	Remaining Time To Empty is calculated as (AvCap) / AvgCurrent When enabled, the AtRate value is substituted for AvgCurrent in this calculation. 16 bit value. Units are 5.625 second. The TTE register holds the estimated time to empty for the application under present conditions. The TTE value is determined by dividing the RemCapAV register by the AverageCurrent register. The result is stored in the TTE register with a resolution of 5.625sec per LSb. Alternatively; the TTE register can be used to estimate time to empty for any given current load. Whenever the AtRate register is programmed to a negative number, representing a discharge current, the TTE register displays the estimated time to empty

				for the application based on the AtRate register value.
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Vempty			Addr:0x12	Type: Reset: A05Ah
BIT	Mode	Name	Reset	Description
7:0	R/W	V_Recover8	A05Ah	V_Recover₈ is the voltage at which the fuel-gauge has cleared the empty condition and is ready to detect another empty condition. Typically set V_Recover ₈ about 0.6V higher than V_Empty to avoid false “double-empty” detects. V_Recover is adjustable in 40mV increments.
15:8		V_Empty8		V_EMPTY ₈ is the system minimum voltage. It is used to manage empty compensation. 9-bit value. V_Empty is in resolution of ??mV/LSB.

RCELL – Slow Battery Impedance			Addr:0x14	Type: Reset: 0290h
BIT	Mode	Name	Reset	Description
15:0	R	RCELL	0290h (160.1mOhm)	This reports the battery's slow internal resistance. 16 bit value. Units of LSbit are 2⁻¹²Ω with 10mΩ sense resistor

AverageTempearture			Addr:0x16	Type: Reset: 1600h
BIT	Mode	Name	Reset	Description
15:0	R	Average Temperature	0x1600 (22C)	The AverageTemperature register reports an average of temperature register readings over a configurable 6min to 12h time period. See the filter CFG register 29H description for details on setting the time filter. The resulting average is placed in the AverageTemperature register with an LSb value of 0.0039°C. The first Temperature reigser reading after IC power-up sets the starting point of the AverageTemperature filter. The last value of the AveragTemperature regisrer is maintained when the IC enters Shutdown mode. This is the 6min to 12hr (configurable) IIR average of the Temperature. Units of LSbit are 0.0039°C. The upper byte has units 1°C. The average is set equal to Temp upon startup.

Cycles - Cycle Counter			Addr:0x17	Type: Reset: 0000h
BIT	Mode	Name	Reset	Description
15:0	R/W	Cycles	0x0000	The Cycles register maintains a total count of the number of charge/discharge cycles of the cell that have occurred. The result is stored as a percentage of a full cycle. For example, a full charge/discharge cycle results in the cycles register incrementing by 100%. The Cycles register has a full range of 0 to 65535% with a 1% LSb. This register is reset to 0%at power-up. To maintain the lifetime cycle count of the cell, this register must be periodically saved by the host and rewritten to the IC at power up. Odometer style accumulation of battery cycles. 16 bit value. The LSB indicates 1% of a battery cycle (1% charge + 1% discharge). One cycle (Cycles=100%) indicates 100% charge and discharge.

DesignCAP - The intended capacity of the battery			Addr:0x18	Type: Reset: 07D0h
BIT	Mode	Name	Reset	Description

15:0	R/W	DesignCAP	07D0h 1000mAh	<p><i>The DesignCap register holds the expected capacity of the cell. This value is used to determine age and health of the cell by comparing against the calculated present capacity stored in the FullCAP register. DesignCap has a LS b equal to 5.0uVh and a full range of 0 to 327.68mVh. The user should multiply the mAh capacity of the cell by the sense register value to determine the uVh value to store in the Design Cap register.</i></p> <p><i>DesignCap₁₆ is used to relate to FullCap₁₆, to help measure the age of the battery. Units are 0.5mA with 10mΩ sense resistor</i></p>
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AverageVCELL- Average VCELL voltage			Addr:0x19	Type:	Reset: B400h
BIT	Mode	Name	Reset	Description	
15:0	R	AverageVCELL	0xB400 (3.6V)	<p>The AverageVCELL register reports an average of VCELL register readings over a configurable 12s to 24min time period. See the FilterCFG register description for details on setting the time filter. The resulting average is placed in the AverageVCELL REGISTER WITH AN lsB VALUE OF 0.625mV. The lower 3 bits of the AverageVCELL register are don't care bits. The first VCELL register reading after IC power up sets the starting point of the AverageVCELL filter. Note that when a cell relaxation event is detected, the averaging period for the AverageVCELL register changes to the period defined by dt3:dt0 in the RelaxCFG register. AverageVCELL reverts back to its normal averaging period when a charge or discharge current is detected. This reports the 12s to 24min (configurable) IIR average of VCELL. AvgVCELL has 78.125uV per LSB</p> <p><i>The average is set equal to VCELL at startup.</i></p>	

MaxMinTemperature			Addr:0x1A	Type:	Reset: 807Fh
BIT	Mode	Name	Reset	Description	
7:0	R/W	MinTemp	0x7F (+127C)	<p>The MaxMinTemperature register maintains the maximum and minimum Temperature register values since the last fuel gauge reset or until cleared by host software. Each time the Temperature register updates. It is compared against these values. If the reading is larger than the maximum or less than the minimum, the corresponding values are replaced with the new reading. At power up, the MaxTemperature value is set to 80h(minimum) and the MinTemperature value is set to 7Fh(maximum). Therefore, both values are changed to the Temperature register reading after the first update. Host software can reset this register by writing it to its power up value of 807Fh. The maximum and minimum temperatures are each stored as two's complement 8 bit values with 1oC resolution.</p> <p>Records the maximum and minimum observed temperature. Units of LSB are 1°C</p>	
15:8		MaxTemp	0x80 (-128C)		

MaxMinVCELL			Addr:0x1B	Type:	Reset: 0x00FF
BIT	Mode	Name	Reset	Description	
7:0	R/W	MinVoltage	0xFF (5.1V)	<p>The MaxMinVCELL register maintains the maximum and minimum VCELL register values since the last fuel gauge reset or until reset by host software. Each time the VCELL register updates, it is compared against these values. If VCELL is larger than the maximum or less than the</p>	
15:8		MaxVoltage	0x00 (0V)		

			<p>minimum, the corresponding value is replaced with the new reading. At power up, the MaxVCELL value is set to 00h(the minimum) and the Min VCELL value is set to FFh(the maximum). Therefore, both values are changed to the VCELL register reading after the first update. Host software can reset this register by writing it to its power up value of 00FFh. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution. Records the maximum and minimum voltage. Units of LSB are 20mV</p>
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MaxMinCurrent			Addr:0x1C	Type:	Reset: 807Fh
BIT	Mode	Name	Reset	Description	
7:0	R/W	Max DISCHARGE Current	0x7F (+5.11A)	<p>The MaxMinCurrent register maintains the maximum and minimum Current register values since the last fuel gauge reset or until cleared by host software. Each time the Current register updates, it is compared against these values. If the reading is larger than the maximum or less than the minimum, the corresponding value is replaced with the new reading. At power up, the MaxCurrent value is set to 80h(the minimum) and the MinCurrent value is set to 7Fh(the maximum). Therefore, both values are changed to the Current register reading after the first update. Host software can reset this register by writing it to its power up value of 807Fh. The maximum and minimum voltages are each stored as two's complement 8-bit values with 0.4mV/RSENSE resolution. Records the maximum charge and discharge current</p>	
15:8		Max CHARGE Current	0x80 (-5.12A)		

CONFIG - General Firmware Configuration Register			Addr:0x1D	Type:	Reset: 2350h
BIT	Mode	Name	Reset	Description	
0	R/W	Ber	0	<p>Enable alert on battery removal. When Ber=1 , a battery-removal condition, as detected by the AIN pin voltage, triggers an alert. Set to 0 at power up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the IC to enter Shutdown mode. The battery insertion/removal alert is always “sticky”, and is edge sensitive only.</p>	
1		Bei	0	<p>Enable alert on battery insertion. When Bei=1, a battery insertion condition, as detected by the AIN pin voltage, triggers an alert. Set to 0 at power up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the IC to enter Shutdown mode.</p> <p>Set Bei=1 to enable battery insertion to trigger an alert. The battery insertion/removal alert is always “sticky”, and is edge sensitive only.</p>	
2	R/W	Aen	0	<p>Enable alert on fuel gauge, outputs. When Aen=1, violation of any of the alert threshold register values by temperature, voltage or SOC triggers an alert. This bit affects the ALRT pin operation only. The Smx, Smn, Tmx, Tmn, Vmx, and Vmn bits are not disabled. This bit is set to 0 at power up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the IC to enter shutdown mode.</p> <p>Aen enables Temperature, Voltage, and SOC alerts to affect the ALRT pin. Smx, Tmx, Vmx, Smn, Tmn, and Vmn continue to function even if Aen=0</p>	
3		FTHRM	0	<p>FTHRM: Force thermistor bias switch. Set FTHRM=1 to always enable the thermistor bias switch. This allows the</p>	

				<i>firmware to control the bias of the thermistor switch. This bit is set to 0 at power-up.</i>
4	R/W	ETHRM	1	<i>ETHRM: Enable thermistor. Set to logic 1 to enable the automatic THRM output bias and AIN measurement every 1.4sec. This bit is set to 1 at power up.</i>
5	R/W	ALSH	1	ALRT shutdown. Set to logic 1 and clear the Aen, Ber, and Bei bits to configure the ALRT pin as an input to control Shutdown mode of the IC. The IC enters shutdown if the ALRT pin is held active for longer than timeout of the SHDNTIMER register. The IC enters Active mode immediately on the opposite edge of the ALRT pin. When set to logic 0, the ALRT pin can function as an interrupt output. This bbit is set to 0 at power up. Note that if this bit is set to 1, the Bei, Ber, and Aen bits should be set to 0 to prevent an alert condition from causing the IC to enter Shutdown mode.
6	R/W	I2CSH	1	Set I2CSH=1 to enable automatic shutdown when the SCLFG and SDAFG are held low for longer than timeout of the SHDNTIMER register. This also configures the IC to wake up on a rising edge of either SDAFG or SCLFG. Set to 1 at power-up. Note that if I2CSCH and AINSH are both set to 0, the IC wakes up an edge of any of the SDAFG, SCLFG or ALRT pins.
7	R/W	SHDN	0	Shutdown. Write this bit to logic 1 to force a shutdown of the IC after timeout of the SHDNTIMER register. SHDN is reset to 0 at power-up and upon exiting Shutdown mode.
8	R/W	Tex	1	Temperature external. When set to 1, the fuel gauge requires external temperature measurements to be written from the host. When set to 0, measurements on the AIN pin are converted to a temperature value and stored in the Temperature register instead. Tex is set to 1 at power-up.
9	R/W	Ten	1	<i>Enable temperature channel. Set to 1 and set ETHRM or FTHRM to 1 to enable measurements on the AIN pin. Ten is set to 1 at power-up.</i>
10	R/W	AINSH	0	<i>AIN pin shutdown. Set to 1 to enable IC shutdown when the battery is removed (AIN reading > V_{THRM}-V_{DETR}). This also configures the IC to wake up when AIN is pulled low on cell insertion. AINSH is set to 0 at power-up. Note that if I2CSCH and AINSH are both set to 0, the IC wakes up an edge of any of the SDAFG, SCLFG, or ALRT pins.</i>
11	R/W	ALRTp	0	ALRT pin polarity. Regardless if ALRT is being used as an input or output, if ALRTp=0, the ALRT pin is active low; if ALRTp=1, the ALRT pin is active high. ALRTp is set to 0 at power-up.
12	R/W	Vs	0	<i>Voltage ALRT Sticky. When VS=1, voltage alerts can only be cleared through software. When Vs=0, voltage alerts are cleared automatically when the threshold is no longer exceeded. Vs is set to 0 at power-up.</i>
13	R/W	Ts	1	<i>Temperature ALRT Sticky. When Ts=1, temperature alerts can only be cleared through software. When Ts=0, temperature alerts are cleared automatically when the threshold is no longer exceeded. Ts is set to 1 at power-up.</i>
14	R/W	Ss	0	SOC ALRT Sticky. When Ss=1, SOC alerts can only be cleared through software. When Ss=0, SOC alerts are cleared automatically when the threshold is no longer exceeded. Ss is set to 0 at power-up.
15	R/W	PSH	0	Power-fail shutdown. Set to 1 to enable IC shutdown when VBATT voltage falls below minimum operating voltage. PSH is set to 0 at power-up.

ICHGTerm	Addr:0x1E	Type:	Reset: 0280h
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BIT	Mode	Name	Reset	Description
15:0	R/W	ICHGTerm	0280h (100mA)	<i>The ICHGTerm register allows the IC to detect when a charge cycle of the cell has completed. The host should set the ICHGTerm register value equal to the exact charge termination current used in the application. Values are stored in uV. Multiply the termination current by the sense resistor to determine the desired register value. This register has the same range and resolution as the Current register.</i> Units: 1.5625uV/Rsense

RemCapAV			Addr:0x1F	Type:	Reset: 03E8h
BIT	Mode	Name	Reset	Description	
15:0	R	RemCAPAV	03E8h (500mAhr)	<i>The RemCapAV register holds the calculated remaining capacity of the cell based on all inputs from the Model Gauge m3 algorithm including empty compensation. The value is stored in terms of uVh and must be divided by the application sense-resistor value to determine the remaining capacity in mAh. The register value is an unfiltered calculation. Jumps in the reported value can be caused by changes in the application such as abrupt changes in load current. This is the remaining capacity with coulomb-counter + Voltage-Fuel-Gauge mixing, after accounting for capacity that is unavailable due to the discharge rate. 16-bit value. 0.5mAh per LSB with 10mΩ sense resistor. 2⁰ UNITS: 5.0uVh/Rsense</i>	

Version			Addr:0x21	Type:	Reset: 0092h
BIT	Mode	Name	Reset	Description	
15:0	R	Version	0092h	Firmware version	

FullCAPNom - Nominal Full Capacity			Addr:0x23	Type:	Reset:07D0h
BIT	Mode	Name	Reset	Description	
15:0	R/W	FullCAPNom	07D0h (1000mAhr)	<i>The register holds the calculated full capacity of the cell, not including temperature and empty compensation. A new full-capacity nominal value is calculated at the end of every charge cycle in the application. The value is stored in terms of uVh and must be divided by the application sense resistor value to determine capacity in mAh. This register is used to calculate the outputs of the ModelGauge m3 algorithm and is available to the use only for debug and save and restore purposes. To maintain the lifetime cycle count of the cell, this register must be periodically saved by the host and rewritten to the IC at power-up.</i> <i>FullCapNom is the internally measured value of the nominal full capacity estimated for room temperature. It is measured by one of the 3 defined full capacity learning methods (Relax-to-Relax, Relax-to-Relax zigzag, or Continual). 0.5mAh per LSB with 10mΩ sense resistor. 2⁰ Units: 5.0uVh/Rsense.</i>	

TempNom		Addr:0x24	Type:	Reset: 1400h

BIT	Mode	Name	Reset	Description
15:0	R/W	TempNom	0x1400 (20C)	<p>Value defining the temperature break between hot and cold. When Temperature measurements are hotter than TempNom, the VBATTFG is compensated using TempCoHot. When Temperature measurements are colder than TempNom, the VBATTFG is compensated using TempCoCold. 10 bit value in bits D15 through D6. The MSbit in D15 represents sign which is useful for values in degrees C but should always be set to 0 for ratiometric values.</p> <p><i>the LSB is 0.0039°C and the upper Byte has units 1°C. This is a signed register</i></p>

TempLim - Temperature Limits			Addr:0x25	Type: Reset: 2305h
BIT	Mode	Name	Reset	Description
7:0	R/W	TempCold	0x05 (5C)	<p>Defines the temperature range between which RCOMP0 learning will occur. Upper Byte is TempHot. Lower Byte is TempCold.</p> <p><i>. Units are 1°C. .RCOMP0 will be learned when TempCold<AvgTA<TempHot. TempCoHot will be learned when (TempNom+TempHot)/2<AvgTA<TempHot. TempCoCold will be learned when TempCold<AvgTA,(TempNom+TempCold)/2</i></p>
15:8	R/W	TempHot	0x23 (35C)	<p>Defines the temperature range between which RCOMP0 learning will occur. Upper Byte is TempHot. Lower Byte is TempCold.</p> <p><i>. Units are 1°C. .RCOMP0 will be learned when TempCold<AvgTA<TempHot. TempCoHot will be learned when (TempNom+TempHot)/2<AvgTA<TempHot. TempCoCold will be learned when TempCold<AvgTA,(TempNom+TempCold)/2</i></p>

Reserved			Addr:0x26	Type: Reset: 1600h
BIT	Mode	Name	Reset	Description
15:0	-	Reserved	0x1600 (22C)	Reserved

AIN - Trimmed AIN measurement			Addr:0x27	Type: Reset: 88D0h
BIT	Mode	Name	Reset	Description
15:0	R	AIN	0x88D0 (53.4% 22C)	<p><i>While in Active mode and TEN=1 in the CONFIG register, the IC periodically measures the voltage between pins AIN and CSP and compares the result to the voltage of the THRM pin. The IC stores the result, a ratiometric value from 0 to 100%. The resulting data is placed in the AIN register every 1.4s with an LSB of 0.0244%. Contents of the AIN register are indeterminate for the first conversion cycle time period after IC power-up. The last value of the Temperature register is maintained when the IC enters Shutdown mode or if TEN=0 in the CONFIG register.</i></p> <p><i>This is the most recent trimmed ratiometric AIN measurement, which is generally used for measuring temperature. AIN is an unsigned register where 0xFFFF indicates 100% ratio between AIN/THRM. Lsb is 2^-16</i></p>

LearnCFG			Addr:0x28	Type:	Reset: 2606h
BIT	Mode	Name	Reset	Description	
0	R/W	X	2606h		
1		MixEn			
2		FiltEmpty			
3		X			
6:4		FCLrnStage			
7		FCx			
9:8		FCLrn			
12:10		LearnTCO			
15:13		LearnRCOMP			

FilterCFG			Addr:0x29	Type:	Reset: 8EA4h
BIT	Mode	Name	Reset	Description	
3:0	R/W	NCURR	0x4	The FilterCFG register sets the averaging time period for all A/D readings, for mixing OCV results and coulomb-count results, and for learning empty compensation. It is recommended that these values are not changed unless absolutely required by the application.	
6:4		NAVGVCELL	0x3		
10:7		NMIX	0xD		
13:11		NTEMP	0x1		
15:14		NEMPTY	0x2		

RelaxCFG			Addr:0x2A	Type:	Reset: 103Bh
BIT	Mode	Name	Reset	Description	
3:0	R/W	dt		<p>The RelaxCFG register defines how the IC detects if the cell is in a relaxed state. For a cell to be considered relaxed, current flow through the cell must be kept at a minimum while the change in the cell's voltage over time, dV/dt, shows little or no change. If AverageCurrent remains below the load threshold while VCELL changes less than the dV threshold over a period of dt, the cell is considered relaxed.</p> <p>Load6:Load0- Sets the threshold which the AverageCurrent register is compared against. The AverageCurrent register must remain below this threshold value of the cell to be considered unloaded. Load is an unsigned 7-bit value where 1 LSb=50uV.</p> <p>dV4:dV0- Sets the threshold which VCELL is compared against. If the cell's voltage changes by less than dV over a period set by dt, the cell is considered relaxed; dV has a range of 0 to 40mV where 1 LSb=1.25mV.</p> <p>dt3:dt0- Sets the time period over which change in VCELL is compared against dV. If the Cell's voltage changes by less than dV over a period set by dt, the cell is considered relaxed. The comparison period is calculated as:</p> <p>Relaxation Period = $2^{dt} \times 0.1758s$.</p> <p>The LSb is 5mA for 10mΩ sense resistor. LOAD⁰ UNITS:</p>	
8:4		dV			
		Load			
15:9					

		50uV/Rsense	
--	--	-------------	--

MiscCFG			Addr:0x2B	Type:	Reset: 0810h
BIT	Mode	Name	Reset	Description	
1:0	R/W	SACFG		<p>The MiscCFG control register enables various other functions of the IC. The MiscCFG register default values should not be changed unless specifically required by the application.</p> <p>0 – bit must be written 0. Do Not write 1.</p> <p>1 – Bit must be written 1. Do not write 0.</p> <p>X- Don't care. Bit may read 0 or 1.</p> <p>SACFG1:SACFG0 – SOC Alert Config. SOC Alerts can be generated by monitoring any of the SOC registers as follows. SACFG defaults to 00 at power-up:</p> <p>00; SOC Alerts are generated based on the SOCREP register.</p> <p>01: SOC Alerts are generated based on the SOCAV register.</p> <p>10: SOC Alerts are generated based on the SOCMIX register.</p> <p>01: SOC Alerts are generated based on the SOCVF register.</p> <p>Vex – Enable external voltage measurement. Write this bit to 1 to disable voltage measurements by the IC. In this mode, external voltage measurements must be written by the host for the fuel gauge to operate. This bit is written to 0 at power-up.</p> <p>enBi1-Enable reset on battery-insertion detection. Set this bit to 1 to force a reset of the fuel gauge whenever a battery insertion is detected based on AIN pin monitoring. This bit is written to 1 at power-up.</p> <p>enBi2</p>	
2		Vex			
3		vttl	0		
4		RdFCLrn	1		
5		X			
6		X			
7		X			
8		X			
9		X			
10		InitVFG	0		
11		enBi1			
12		RmCT	X		
13		RdACT	X		
14		Bei2	0		
15		enBi2	0		

TGAIN - Temperature Gain Compensation			Addr:0x2C	Type:	Reset: E3E1h
BIT	Mode	Name	Reset	Description	
15:0	R/W	TGAIN	E3E1h	<p>TGAIN and TOFF registers adjust the gain and offset of the temperature measurement A/D on the AIN pin to convert the result of a temperature value by the following equation:</p> <p>Temperature Register=(AIN Register x TGAIN Register / 16384) + (TOFF Register x 2)</p> <p>Both these registers are signed two's complement. These registers allow for accurate temperature conversions when using a variety of external NTC thermistors.</p> <p>TGAIN is a signed value with units of °C/64</p>	

TOFF - Temperature Offset Compensation			Addr:0x2D	Type:	Reset: 290Eh
BIT	Mode	Name	Reset	Description	
15:0	R/W	TOFF	290Eh	<p>TGAIN and TOFF registers adjust the gain and offset of the temperature measurement A/D on the AIN pin to convert the result to a temperature value by the following equation:</p> <p>Temperature Register=(AIN Register x TGAIN Register / 16384) + (TOFF Register x 2)</p>	

				Both these registers are signed two's complement. These registers allow for accurate temperature conversions when using a variety of external NTC thermistors. <i>TOFF is a signed value with units of 2^7 in the LSb. Note that these units are 2X the TEMP register. 2^7 UNIT: +0.0078°C</i>
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CGAIN - Current Gain Compensation			Addr:0x2E	Type: Reset: 4000h
BIT	Mode	Name	Reset	Description
15:0	R/W	CGAIN	4000h	<p>The CGAIN and COFF registers adjust the gain and offset of the current measurement result. The current measurement A/D is factory trimmed to data-sheet accuracy without the need for the user to make further adjustments. The default power-up settings for CGAIN and COFF apply no adjustments to the Current register reading. For specific application requirements. The CGAIN and COFF registers can be used to adjust readings as follows:</p> <p>Current Register=Current A/D Reading x (CGAIN Register/16384) + (COFF Register x 2)</p> <p>Both these registers are signed two's complement. The default values of 4000h for CGAIN and 0000h for COFF preserve factory calibration and unit values (1.5625uV). 2^0UNIT: 0.0061%</p>

COFF - Current Offset Compensation			Addr:0x2F	Type: Reset: 0000h
BIT	Mode	Name	Reset	Description
15:0	R/W	COFF	0000h	<p>The CGAIN and COFF registers adjust the gain and offset of the current measurement result. The current measurement A/D is factory trimmed to data-sheet accuracy without the need for the user to make further adjustments. The default power-up settings for CGAIN and COFF apply no adjustments to the Current register reading. For specific application requirements. The CGAIN and COFF registers can be used to adjust readings as follows:</p> <p>Current Register=Current A/D Reading x (CGAIN Register/16384) + (COFF Register x 2)</p> <p>Both these registers are signed two's complement. The default values of 4000h for CGAIN and 0000h for COFF preserve factory calibration and unit values (1.5625uV). UNITS: 3.125uV/Rsense</p>

lavg_empty			Addr:0x36	Type: Reset: 0100h
BIT	Mode	Name	Reset	Description
15:0	R/W	lavg_empty	0100h	

FCTC - Full Capacity Temperature Correction factor			Addr:0x37	Type: Reset: 05E0h
BIT	Mode	Name	Reset	Description

15:0	R/W	FCTC	0x05E0	<i>This temperature correction factor is used to calculate the FullCap as a function of FullCapNom and the present temperature (TA). Units are 1/2²¹C</i>
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RCOMP0 - Resistance Compensation Register for VFG			Addr:0x38	Type: Reset: 004Bh
BIT	Mode	Name	Reset	Description
15:0	R/W	RCOMP0	0x004B	This is the RCOMP value that is appropriate at Temperature = TempNom <i>Adjust RCOMP0 as you would adjust RCOMP in ModelGauge 1.0 parts</i>

TempCo - Temperature Compensation for VFG			Addr:0x39	Type: Reset: 262Bh
BIT	Mode	Name	Reset	Description
7:0		TempCoCold	0x00	<i>Upper byte holds TempCoHot with units of 0.03125counts/°C. Lower byte holds TempCoCold with units of 0.125counts/°C</i>
15:8		TempCoHot	0x00	<i>Upper byte holds TempCoHot with units of 0.03125counts/°C. Lower byte holds TempCoCold with units of 0.125counts/°C</i>

k_empty0 - Empty Time Constant for Nominal Temperature			Addr:0x3B	Type: Reset: 0600h
BIT	Mode	Name	Reset	Description
15:0	R/W	K_empty0	0x0600 (4.5min)	This represents the temperature normalized empty time constant. 16 bit value. Units of LSb are tbd

FSTAT			Addr:0x3D	Type: Reset: 0x0001
BIT	Mode	Name	Reset	Description
0	R		X	The FSTAT register is a read-only register that monitors the status of the ModelGauge m3 algorithm detects that the cell is in a fully relaxed state. This bit is cleared to 0 whenever the cell is no longer in a relaxed state.
1			X	
2			X	
3			X	
4			X	
5			X	
6			X	
7			X	
8			X	
9		RelDt	0	RelDt - Relaxed cell detection. This bit is set to a 1 whenever the ModelGauge m3 algorithm detects that the cell is in a fully relaxed state. This bit is cleared to 0 whenever the cell is no longer in a relaxed state.
10			X	
11			X	
12			X	
13			X	
14			X	
15			X	X- Don't care. This bit is undefined and can be logic 0 or 1.

SHDNTIMER			Addr:0x3F	Type:	Reset: E000h
BIT	Mode	Name	Reset	Description	
12:0	R/W	CTR	0x000	<i>The SHDNTIMER register sets the timeout period from when a shutdown event is detected until the IC disables the LDO and enters low-power mode.</i>	
15:13		THR	0x7	<i>CTR12:CTR0- Shutdown counter. This register counts the total amount of elapsed time since the shutdown trigger event. This counter value stops and resets to 0 when the shutdown timeout completes. The counter LSb is 1.4s.</i> <i>THR2:THR0- Sets the shutdown timeout period from a minimum of 45s to a maximum of 1.6h. The default POR value of 7h gives a shutdown delay of 1.6h. The equation setting the period is</i> <i>Shutdown Timeout Period = 175.8ms × 2^(8+THR)</i>	

dQacc			Addr:0x45h	Type:	Reset: 01F4h
BIT	Mode	Name	Reset	Description	
15:0	R/W	dQacc	01F4h		

dPacc			Addr:0x46h	Type:	Reset: 3200h
BIT	Mode	Name	Reset	Description	
15:0	R/W	dPacc	3200h		

Characterization Table			Addr:0x80 – 0xAFh	Type:	Reset:
BIT	Mode	Name	Reset	Description	
15:0	R/W		n/A		

OCV			Addr:0xEEh	Type:	Reset: 0000h
BIT	Mode	Name	Reset	Description	
15:0	R	OCV	0000h	<i>The OCV register contains the calculated open-circuit voltage of the cell as determined by the ModelGauge m3 algorithm. This value is used in other internal calculations. The result is a 12-bit value ranging from 2.5V to 5.119V where 1 LSb is 1.25mV. The bottom 4 bits of this register are don't care bits.</i> <i>2⁸ UNIT: 1.25mV, X=Don't care</i>	

SOC _{VF}			Addr:0xFFh	Type:	Reset: 0000h
BIT	Mode	Name	Reset	Description	
15:0	R	SOC _{VF}		<i>The SOCVF register holds the calculated present SOC of the battery according to the voltage fuel gauge. The register value is stored as a percentage with a resolution of 0.0039% per LSb. If an 8-bit SOC value is desired, the host can read only the upper byte of the register with a resolution of 1.0%.</i> <i>2⁸ UNIT: 0.0039%</i> <i>2⁰ UNIT: 1.0%</i>	

21 Haptic Motor Driver

The MAX8966/MAX8997 acts as a Slave Transmitter/Receiver. The Slave address of the MAX8966/MAX8997 Haptic Motor Driver is 0x90h/0x91h. The least significant bit is the read/write\ indicator.

Note: All Haptic registers are reset type O.

The user status and configuration registers are located in block 0x00 to 0x10.

HEX	R7	R6	R5	R4	R3	R2	R1	R0	ACCESS	DATA LENGTH	FUNCTION
0x00	0	0	0	0	0	0	0	0	R	8	General Status
0x01	0	0	0	0	0	0	0	1	R/W	8	General Configuration 1
0x02	0	0		0	0	0	1	0	R/W	8	General Configuration 2
0x03	0	0	0	0	0	0	1	1	R/W	8	Haptic Definition Config 1
0x04	0	0	0	0	0	1	0	0	R/W	8	Haptic Cycle Configuration 1
0x05	0	0	0	0	0	1	0	1	R/W	8	Haptic Cycle Configuration 2
0x06	0	0	0	0	0	1	1	0	R/W	8	Haptic Signal Configuration 1
0x07	0	0	0	0	0	1	1	1	R/W	8	Haptic Signal Configuration 2
0x08	0	0	0	0	1	0	0	0	R/W	8	Haptic Signal Configuration 3
0x09	0	0	0	0	1	0	0	1	R/W	8	Haptic Signal Configuration 4
0x0A	0	0	0	0	1	0	1	0	R/W	8	Haptic Duty Cycle 1
0x0B	0	0	0	0	1	0	1	1	R/W	8	Haptic Duty Cycle 2
0x0C	0	0	0	0	1	1	0	0	R/W	8	Haptic PWM 1
0x0D	0	0	0	0	1	1	0	1	R/W	8	Haptic PWM 2
0x0E	0	0	0	0	1	1	1	0	R/W	8	Haptic PWM 3
0x0F	0	0	0	0	1	1	1	1	R/W	8	Haptic PWM 4
0x10	0	0	0	1	0	0	0	0	R	8	Part Revision Code

0x00: General Status (Read Only)

	7	6	5	4	3	2	1	0
Name								HBUSY
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:1		Reserved
0	HBUSY	Busy Status for motor actuator. When HTYP= 0 (external PWM input enabled), the bit is interpreted as follows: 0: Motor driver off (as dictated by MEN) 1: Motor Driver on When HTYP= 1 (Internal Motor Driver Registers) 0: No internal haptic feedback signal 1: Internal haptic feedback signal is active

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0x01: Haptic Configuration 1 (Read/Write)

	7	6	5	4	3	2	1	0
Name	INV	CONT	MSU[2:0]			SCF[2:0]		
Default	0	0	0	0	0	0	1	1

Bit	Name	Description
7	INV	Invert bit 0: Use 50% Duty cycle during low period of signal SIG 1: Invert PWM signal during low period of signal SIG
6	CONT	Continuous Mode 0: Follow normal haptic pattern protocol 1: Output a continuous haptic pattern – the continuous pattern will be the pattern specified in register 0x03
5:3	MSU[2:0]	Motor start-up pulse: forces MDP and MDN to VIN_MOTOR and GNDM, respectively. Only used if HTYP in register 0x02 is set to logic high. 000: 0ms (feature switched off) 001: 2ms 010: 4ms 111: 14ms
2:0	SCF[2:0]	If HTYP= 1, SCF[2:0] sets the scale frequency parameter. Number of clock cycles for PWM_DC_RES: 000: 1 clock cycle $f_{PWM} = 62.5\text{kHz}$ 001: 2 clock cycles $f_{PWM} = 41.67\text{kHz}$ 010: 3 clock cycles $f_{PWM} = 31.25\text{kHz}$ 111: 8 clock cycles $f_{PWM} = 7.8\text{kHz}$

0x02: Haptic Configuration 2 (Read/Write)

	7	6	5	4	3	2	1	0
Name	MODE	MEN	HTYP					PDIV[1:0]
Default	0	0	0	0	0	0	1	0

Bit	Name	Description
7	MODE	Selects type of Motor 0: ERM motor attached, do not use PWM divisor 1: LRA motor attached, use PWM divisor
6	MEN	Haptic Enable 0: Disable motor driver 1: Enable motor driver
5	HTYP	Haptic Input Select 0: Use External PWM input - MPWM 1: Use Internal Motor Driver Registers (IPWM)
4:2		Reserved
1:0	PDIV[1:0]	PWM Frequency Divisor – divides down the PWM signal 00: 32 01: 64 10: 128 11: 256

0x03: Haptic Driver Configuration Channel (Read/Write)

	7	6	5	4	3	2	1	0
Name	CYCA[1:0]		SIGPA[1:0]		SIGDCA[1:0]		PWMDCA[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:6	CYCA[1:0]	00-11: Number of Cycle Patterns 3...0
5:4	SIGPA[1:0]	00-11: Signal Period Patterns 3...0
3:2	SIGDCA[1:0]	00-11: Signal Duty Cycle Patterns 3...0
1:0	PWMDCA[1:0]	00-11: PWM Duty Cycle Patterns 3...0

Note: Writing to register 0x03 starts an internally created PWM sequence.

0x04: Haptic Cycle Configuration 1 (Read/Write)

	7	6	5	4	3	2	1	0
Name	CYC0[3:0]				CYC1[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	CYC0[3:0]	If HTYP is set to 1 CYC0[3:0] defines the number of cycles of the haptic feedback waveform – Pattern 0: 0000: 0 cycles (turns off any haptic feedback) 0001: 1 cycle 1111: 15 cycles
3:0	CYC1[3:0]	Number of Cycles of Haptic Feedback Waveform – Pattern 1: 0000: 0 cycles (turns off any haptic feedback) 0001: 1 cycle 1111: 15 cycles

0x05: Haptic Cycle Configuration 2 (Read/Write)

	7	6	5	4	3	2	1	0
Name	CYC2[3:0]				CYC3[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	CYC2[3:0]	Number of Cycles of Haptic Feedback Waveform – Pattern 2: 0000: 0 cycles (turns off any haptic feedback) 0001: 1 cycle 1111: 15 cycles
3:0	CYC3[3:0]	Number of Cycles of Haptic Feedback Waveform – Pattern 3: 0000: 0 cycles (turns off any haptic feedback) 0001: 1 cycle 1111: 15 cycles

0x06: Haptic Signal Configuration 1 (Read/Write)

	7	6	5	4	3	2	1	0
Name	SIGP0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	SIGP0[7:0]	Period of Haptic Feedback Waveform (Measured in Number of PWM Pulses) – Pattern 0: 00000000: 32 PWM Pulses 00000001: 64 PWM Pulses 00000010: 96 PWM Pulses 11111110: 8160 PWM Pulses 11111111: 8192 PWM Pulses

0x07: Haptic Signal Configuration 2 (Read/Write)

	7	6	5	4	3	2	1	0
Name	SIGP1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	SIGP1[7:0]	Period of Haptic Feedback Waveform (Measured in Number of PWM Pulses) – Pattern 1: 00000000: 32 PWM Pulses 00000001: 64 PWM Pulses 00000010: 96 PWM Pulses 11111110: 8160 PWM Pulses 11111111: 8192 PWM Pulses

0x08: Haptic Signal Configuration 3 (Read/Write)

	7	6	5	4	3	2	1	0
Name	SIGP2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	SIGP2[7:0]	Period of Haptic Feedback Waveform (Measured in Number of PWM Pulses) – Pattern 2: 00000000: 32 PWM Pulses 00000001: 64 PWM Pulses 00000010: 96 PWM Pulses 11111110: 8160 PWM Pulses 11111111: 8192 PWM Pulses

0x09: Haptic Signal Configuration 4 (Read/Write)

	7	6	5	4	3	2	1	0
Name	SIGP3[7:0]							
Default	0	0	0	0	0	0	0	0

Default	0	0	0	0	0	0	0	0
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Bit	Name	Description
7:0	SIGP3[7:0]	Period of Haptic Feedback Waveform (Measured in Number of PWM Pulses) – Pattern 3: 00000000: 32 PWM Pulses 00000001: 64 PWM Pulses 00000010: 96 PWM Pulses 11111111: 8192 PWM Pulses

0x0A: Haptic Signal Duty Cycle Configuration 1 (Read/Write)

	7	6	5	4	3	2	1	0
Name	SIGDC0[3:0]						SIGDC1[3:0]	
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	SIGDC0[3:0]	Duty Cycle of Haptic Feedback Waveform – Pattern 0: 0000: 1/16 or 6.25% 0001: 2/16 or 12.5% 1111: 16/16 or 100%
3:0	SIGDC1[3:0]	Duty Cycle of Haptic Feedback Waveform – Pattern 1: 0000: 1/16 or 6.25% 0001: 2/16 or 12.5% 1111: 16/16 or 100%

0x0B: Haptic Signal Duty Cycle Configuration 2 (Read/Write)

	7	6	5	4	3	2	1	0
Name	SIGDC2[3:0]						SIGDC3[3:0]	
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	SIGDC2[3:0]	Duty Cycle of Haptic Feedback Waveform – Pattern 2: 0000: 1/16 or 6.25% 0001: 2/16 or 12.5% 1111: 16/16 or 100%
3:0	SIGDC3[3:0]	Duty Cycle of Haptic Feedback Waveform – Pattern 3: 0000: 1/16 or 6.25% 0001: 2/16 or 12.5% 1111: 16/16 or 100%

0x0C: Haptic Signal PWM Duty Cycle Configuration 1 (Read/Write)

	7	6	5	4	3	2	1	0
Name	PWMDC0[3:0]							

Default	1	1	1	1	1	1	1	1
----------------	---	---	---	---	---	---	---	---

Bit	Name	Description
7:6		
5:0	PWMDC1[5:0]	Duty Cycle of Haptic Feedback PWM Signal – Pattern 1: 000000: 1/64 or 1.56% 000001: 2/64 or 3.10% 111111: 64/64 or 100%

0x0D: Haptic Signal PWM Duty Cycle Configuration 2 (Read/Write)

	7	6	5	4	3	2	1	0
Name						PWMDC1[3:0]		
Default	1	1	1	1	1	1	1	1

Bit	Name	Description
7:6		
5:0	PWMDC1[5:0]	Duty Cycle of Haptic Feedback PWM Signal – Pattern 2: 000000: 1/64 or 1.56% 000001: 2/64 or 3.10% 111111: 64/64 or 100%

0x0E: Haptic Signal PWM Duty Cycle Configuration 3 (Read/Write)

	7	6	5	4	3	2	1	0
Name						PWMDC2[3:0]		
Default	1	1	1	1	1	1	1	1

Bit	Name	Description
7:6		
5:0	PWMDC2[5:0]	Duty Cycle of Haptic Feedback PWM Signal – Pattern 3: 000000: 1/64 or 1.56% 000001: 2/64 or 3.10% 111111: 64/64 or 100%

0x0F: Haptic Signal PWM Duty Cycle Configuration 4 (Read/Write)

	7	6	5	4	3	2	1	0
Name						PWMDC3[3:0]		
Default	1	1	1	1	1	1	1	1

Bit	Name	Description
7:6		
5:0	PWMDC3[5:0]	Duty Cycle of Haptic Feedback PWM Signal – Pattern 4: 000000: 1/64 or 1.56% 000001: 2/64 or 3.10%

		111111: 64/64 or 100%
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0x10: Part Revision Code (Read only)

	7	6	5	4	3	2	1	0
Name	MTR_REV[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	MTR_REV[7:0]	Read-Only vector that contains revision information. The first revision should have the code 0000 0000. Programming is accomplished via metal changes.

22 RTC SEC Register

I²C address and Register Map for the MAX8966/MAX8997 RTC Section

The MAX8966/MAX8997 acts as a Slave Transmitter/Receiver. The Slave address of the MAX8966/MAX8997 RTC is 0x0Ch/0x0Dh . The least significant bit is the read/write\ indicator.

22.1 HEX REGISTER ADDRESS/DESCRIPTION SUMMARY for RTC section

ADDR ESS	RESE T	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	FUNCTION			
00H	00	x	x	WTSR	RTC1S	SMPL_IN_T	RTCA2	RTCA1	RTC60S	Interrupt			
01H	00	x	x	WTSRm	RTC1Sm	SMPL_IN_Tm	RTCA2m	RTCA1m	RTC60Sm	Interrupt Mask			
02H	03	x	x	x	x	x	x	Mode24_12nm	BCDm	Control Mask			
03H	00	x	x	x	x	x	x	Mode24_12n	BCD	Control			
04H	02	x	x	x	x	x	FREEZE_SEC	FCUR	UDR	Update1			
05H	00	x	x	x	x	x	x	RBUDF_UDF		Update2			
06H	00	SMPL	WTSR	x	x	SMPLT		WTSRT		WTSR/SMPL			
10H	00	x				Seconds					SEC Alarm1		
11H	00	x				Minutes					MIN Alarm1		
12H	00	x	AMPM			HourA					HOUR Alarm1		
13H	01	x	Sat	Fri	Thur	Wed	Tues	Mon	Sun		Day of Week Alarm1		
14H	01	x	x	x		Month					Month Alarm1		
15H	00					Year					Year Alarm1		
16H	01	x	x			Day					Day of Month Alarm1		
17H	00	AE				Seconds					SEC Alarm1		
18H	00	AE				Minutes					MIN Alarm1		
19H	00	AE	AMPM			Hour					Hour Alarm1		
1AH	00	AE	Sat	Fri	Thur	Wed	Tues	Mon	Sun		Day of Week Alarm1		
1BH	00	AE	x	x		Month					Month Alarm1		
1CH	00	AE				Year					Year Alarm1		
1DH	01	AE	x			Day of Month					Day of Month Alarm1		
1EH	00	AE				Seconds					SEC Alarm2		
1FH	00	AE				Minutes					MIN Alarm2		
20H	00	AE	AMPM			Hour					Hour Alarm2		
21H	00	AE	Sat	Fri	Thur	Wed	Tues	Mon	Sun		Day of Week Alarm2		
22H	00	AE	x	x		Month					Month Alarm2		
23H	00	AE				Year					Year Alarm2		
24H	01	AE	x			Day of Month					Day of Month Alarm2		

22.1.1 RTC Interrupt

INT – Interrupt register			Addr: 0x00	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R&C	RTC60S	0	1: RTC periodic 60s event is detected. 0: RTC periodic 60s event is not detected.	
1	R&C	RTCA1	0	1: RTC alarm1 is detected. 0: RTC alarm1event is not detected.	
2	R&C	RTCA2	0	1: RTC alarm2 is detected. 0: RTC alarm2event is not detected.	
3	R&C	SMPL_INT	0	1: SMPL interrupt to host controller is detected. 0: SMPL event is not detected.	
4	R&C	RTC1S	0	1: RTC periodic 1s event is detected. 0: RTC periodic 1s event is not detected.	
5	R&C	WTSR	0	1:WTSR event interrupt is detected. 0: WTSR event is not detected.	
6	R&C	Reserved	0	x	
7	Reserved	Reserved	0	x	

22.1.2 RTC Interrupt Mask

Interrupt Mask register			Addr: 0x01	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	RTC60Sm	0	RTC periodic 60s event 0: Not masked 1: Masked	
1	R/W	RTCA1m	0	RTC alarm1 0: Not masked 1: Masked	
2	R/W	RTCA2m	0	RTC alarm2 0: Not masked 1: Masked	
3	R/W	SMPL_INTm	0	SMPL interrupt to host controller 0: Not masked 1: Masked	
4	R/W	RTC1Sm	0	RTC periodic 1s event 0: Not masked 1: Masked	
5	R/W	WTSRm	0	WTSR event 0: Not masked 1: Masked	
6	Reserved	Reserved	0	x	
7	Reserved	Reserved	0	x	

22.1.3 RTC Control Register Mask

RTC Control Register Mask			Addr: 02hex	R:S	Reset: 03hex
BIT	Mode	Name	Reset	Description	
0	R/W	BCDm	1	Access control of BCD bit in register RTC Control Register(0x03h) 0: Writes to bit 0 (BCD) of register address 0x03 not allowed 1: Writes to bit 0 (BCD) of register address 0x03 allowed	
1	R/W	Mode24_12nm	1	Access control of Mode24_12n bit in register RTC Control Register 0: Writes to bit 1 of register address 0x03 not allowed 1: Writes to bit 1 of register address 0x03 allowed	
6-2	R/W	reserved			

22.1.4 RTC Control Register

Control Register			Addr: 03hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	BCD	0	Data mode for Time and Calendar Updates 0: Binary 1: BCD (Binary Coded Decimal) If BCDM=0, writes to BCD are not allowed.	
1	R/W	Mode24_12n	0	Hour Format Control 0: 12 hour mode 1: 24 hour mode Note that AMPM bit defined for the HOUR. HOURA register only make sense for the 12-hr mode as the 24hr mode already has AM/PM applied. If Mode24_12nm=0, writing to Model24_12n is not allowed. When switching between 12-hour and 24-hour mode, the registers do not automatically update. User must reprogram all registers.	
6-2	reserved				

22.1.5 RTC Update Register1

Update Register 1			Addr: 04hex	R:S	Reset: 02hex
BIT	Mode	Name	Reset	Description	
0	R/W	UDR	0	Access Control to Update RTC registers by transferring data from the "Write Buffers" to the actual registers 0: No action 1: Update register. Maximum transfer time from write buffers to the timekeeper counters is 10msec after UDR is set. UDR is internally cleared to after the registers data has been transferred.	
1	R/W	FCUR	1	Flags Cleared Upon Read Control Bit 0: User must write 0 to clear interrupt 1: Flags interrupt cleared upon read.	
2	R/W	FREEZE_SEC	0	This bit freezes the SEC counter from incrementing 0: SEC counter increments normally 1: SEC counter stops incrementing which stops all subsequent registers in the timer string (MIN, HOUR, DAY, etc). This setting effectively stops the clock.	
3	R/W	Reserved	0		
4	R/W	Reserved	0		
5	R/W	Reserved	0		
6	R	Reserved	0		
7	reserved				

22.1.6 RTC Update Register2

Update Register 2			Addr: 05hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/C	UDF	0	Update flag: This bit is an Update Flag that indicates when an actual transfer of data from the “Write Buffers” to the corresponding register occurs. When this bit is 1, then the user can initiate a new write operation, otherwise it is not safe to do so. 0: Update Not Done 1: Update Done	
1	R/C	RBUDF	0	This bit is an Update Flag that indicates when an actual transfer of data from the actual registers to “Read Buffers” occurs. When this bit is 1, then the user can initiate a new read operation, otherwise it is not safe to do so. 0: Update Not Done 1: Update Done Maximum update time is 10msec after the UDR bit is set. If FCUR bit is 1, this bit is automatically cleared after a read operation. If FCUR is 0, the user must write a 0 to clear it.	
2:7		Reserved		Reserved	

22.1.7 WTSR and SMPL Register

WTSR and SMPL Register			Addr: 06hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
1:0	R/W	WTSRT	00	Time to keep Default-On Regulaotrs ON. 00: 250msec 01: 500msec 10: 750msec 11: 1000msec	
3:2	R/W	SMPLT	00	Set the SMPL timer Threshold 00: 0.5s 01: 1s 10: 1.5s 11: 2s	
4	R	Reserved	0		
5	R	Reserved	0		
6	R/W	WTSR	0	1: WTSR enabled 0: WTSR disabled	
7	R/W	SMPL	0	1: SMPL enabled 0: SMPL disabled	

22.1.8 SEC Register

SEC Register			Addr: 10 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Seconds	0	In Binary format, valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0	

				through 5, and valid data for B3 through B0 are 0 through 9.
7	R/W	Reserved	0	

22.1.9 MIN Register

MIN Register			Addr: 11 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Minutes	0	In Binary format, valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9	
7	R/W	Reserved	0		

22.1.10 HOUR Register

HOUR Register			Addr: 12 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	HourA	0	<p>“Mode24_12n” bit is set to 1 (24 hours mode):</p> <ul style="list-style-type: none"> a. Binary Mode: B5 is zero, and B4 through B0 valid values are 0 through 23. b. BCD Mode: Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 23) c. When in the 24 hr mode, the AM/PM bit is ignored. d. <p>“Mode24_12n” bit is set to 0 (12 hours mode)</p> <ul style="list-style-type: none"> a. Binary Mode: B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12 b. BCD Mode: Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 12) 	
6	R/W	AMPM	0	0: AM 1: PM	
7	R/W	Reserved	0		

22.1.11 DAY OF WEEK Register

It is imperative to realize that there is no BCD representation for B6 through B0, and thus no conversion from BCD to Binary will be performed by the logic.

DAY OF WEEK Register			Addr: 13 hex	R:S	Reset: 01hex
BIT	Mode	Name	Reset	Description	

0	R/W	Sun	1	B[6:0] = 000_0001 represents Sunday
1	R/W	Mon	0	B[6:0] = 000_0010 represents Monday
2	R/W	Tue	0	B[6:0] = 000_0100 represents Tuesday
3	R/W	Wed	0	B[6:0] = 000_1000 represents Wednesday
4	R/W	Thu	0	B[6:0] = 001_0000 represents Thursday
5	R/W	Fri	0	B[6:0] = 010_0000 represents Friday
6	R/W	Sat	0	B[6:0] = 100_0000 represents Saturday
7	R/W	Reserved	0	

22.1.12 MONTH Register

MONTH Register			Addr: 14 hex	R:S	Reset: 01hex
BIT	Mode	Name	Reset	Description	
4:0	R/W	Month	00001	In Binary format, valid values for B4 through B0 are 1 through 12. In BCD format, valid data for B4 is either 0 or 1, and valid data for B3 through B0 are 0 through 9 (the full value in BCD format should not exceed 12 and must be greater than zero). Month of January is represented by 1, while December is shown as 12.	
5	R	Reserved	0		
6	R	Reserved	0		
7	R	Reserved	0		

22.1.13 YEAR Register

YEAR Register			Addr: 15 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
7:0	R/W	Year	00 hex	In Binary format, valid values for B7 through B0 are 0 through 99. In BCD format, valid data for B7 through B4 are 0 through 9, and similarly valid data for B3 through B0 are 0 through 9.	

22.1.14 DAY of MONTH Register

DAY of MONTH Register			Addr: 16 hex	R:S	Reset: 01hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	Day	000001	<p>In Binary format, valid values for B6 through B0 are 1 through 31. In BCD format, valid data for B3 through B4 are 0 through 3, and valid data for B3 through B0 are 0 through 9 (the full value should not exceed 31).</p> <p>Furthermore, there is a restriction on chosen number of days in a month according to the selected month and year as shown below:</p> <ol style="list-style-type: none"> 1. For months (MONTH register; address 0x14) 1, 3, 5, 7, 8, 10, and 12 the selected value for B5 through B0 must be 1 through 31. 2. For months (MONTH register; address 0x14) 4, 6, 9, and 11 the selected value for B5 through B0 must be 1 through 30. 3. For month (MONTH register; address 0x14) 2, or month of Feb., the selected value for B5 through B0 must be 1 through 28 for normal years (YEAR register; address 0x15), or must be 1 through 29 for leap years (YEAR register; address 0x15 where the YEAR value is divisible by 4) 	
6	R	Reserved	0		
7	R	Reserved	0		

22.1.15 SEC Alarm1

SEC Alarm1			Addr: 17 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Seconds	000000	If equal to bit[6:0] of SEC register and AE is 1, interrupt is generated.	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.16 MIN Alarm1

MIN Alarm1			Addr: 18 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Minutes	000000	If equal to bit[6:0] of MIN register and AE is 1, interrupt is generated.	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.17 HOUR Alarm1

HOUR Alarm1			Addr: 19 hex	R:S	Reset: 00hex

BIT	Mode	Name	Reset	Description
5:0	R/W	Hour	000000	<p>“Mode24_12n” bit is set to 1 (24 hours mode):</p> <ul style="list-style-type: none"> a. Binary Mode: B5 is zero, and B4 through B0 valid values are 0 through 23. b. BCD Mode: Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 23) <p>“Mode24_12n” bit is set to 0 (12 hours mode)</p> <ul style="list-style-type: none"> a. Binary Mode: B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12 b. BCD Mode: Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 12)
6	R/W	AMPM	0	0: AM 1: PM
7	R/W	AE	0	1: Alarm enable 0: Alarm disable

22.1.18 DAY OF WEEK Alarm1

DAY OF WEEK Alarm1			Addr: 1A hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	Sun	1		
1	R/W	Mon	0		
2	R/W	Tue	0		
3	R/W	Wed	0		
4	R/W	Thur	0		
5	R/W	Fri	0		
6	R/W	Sat	0		
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.19 MONTH Alarm1

MONTH Alarm1			Addr: 1Bhex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
4:0	R/W	Month	00000	In Binary format, valid values for B4 through B0 are 1 through 12. In BCD format, valid data for B4 are either 0 or 1, and	

				valid data for B3 through B0 are 0 through 9 (B4 through B0 cannot be 0).
5	R	Reserved	0	
6	R	Reserved	0	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable

22.1.20 YEAR Alarm1

YEAR Alarm1			Addr: 1C hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Year	00 hex	Year	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.21 DAY of MONTH Alarm1

DAY of MONTH Alarm1			Addr: 1D hex	R:S	Reset: 01hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	Day_of_month	000001	Day of Month	
6	R	Reserved	0		
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.22 SEC Alarm2

SEC Alarm2			Addr: 1E hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Seconds	000000	If equal to bit[6:0] of SEC register and AE is 1, interrupt is generated.	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.23 MIN Alarm2

MIN Alarm2			Addr: 1F hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Minutes	000000	If equal to bit[6:0] of MIN register and AE is 1, interrupt is generated.	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.24 HOUR Alarm2

HOUR Alarm2			Addr: 20 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	Hour	000000	<p>“Mode24_12n” bit is set to 1 (24 hours mode):</p> <ul style="list-style-type: none"> c. Binary Mode: B5 is zero, and B4 through B0 valid values are 0 through 23. d. BCD Mode: Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 23) <p>“Mode24_12n” bit is set to 0 (12 hours mode)</p> <ul style="list-style-type: none"> c. Binary Mode: B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12 d. BCD Mode: Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 12) 	
6	R/W	AMPM	0	0: AM 1: PM	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.25 DAY OF WEEK Alarm2

DAY OF WEEK Alarm2			Addr: 21 hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
0	R/W	Sun	1		
1	R/W	Mon	0		
2	R/W	Tue	0		
3	R/W	Wed	0		
4	R/W	Thur	0		
5	R/W	Fri	0		
6	R/W	Sat	0		
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.26 MONTH Alarm2

MONTH Alarm2			Addr: 22hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	

4:0	R/W	Month	00000	Month
5	R	Reserved	0	
6	R	Reserved	0	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable

22.1.27 YEAR Alarm2

YEAR Alarm2			Addr: 23hex	R:S	Reset: 00hex
BIT	Mode	Name	Reset	Description	
6:0	R/W	Year	00 hex	Year	
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	

22.1.28 DAY of MONTH Alarm2

DAY of MONTH Alarm2			Addr: 24 hex	R:S	Reset: 01hex
BIT	Mode	Name	Reset	Description	
5:0	R/W	Day_of_month	000001	Day of Month	
6	R	Reserved	0		
7	R/W	AE	0	1: Alarm enable 0: Alarm disable	