

# Cheatsheet External Interrupts

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## EICRA EICRB

*External Interrupt Controll Register A B*

| Bit    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| EICRA: | ISC31 | ISC30 | ISC21 | ISC20 | ISC11 | ISC10 | ISC01 | ISC00 |

| Bit    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| EICRB: | ISC71 | ISC70 | ISC61 | ISC60 | ISC51 | ISC50 | ISC41 | ISC40 |

## ISCn0 ISCn1

*Interrupt Source Control*

| Bit<br>ISCn1 | Bit<br>ISCn1 | Bedeutung:  |
|--------------|--------------|---|
| 0            | 0            | Low-Level: Der Low-Pegel am Pin INTn erzeugt den Interrupt (level-triggered Interrupt).             |
| 0            | 1            | Any Edge: Sowohl eine steigende als auch eine fallende Flanke am Pin INTn erzeugen einen Interrupt. |
| 1            | 0            | Falling edge: Die fallende Flanke am Pin INTn erzeugt einen Interrupt                               |
| 1            | 1            | Rising edge: Die steigene Flanke am Pin INTn erzeugt einen Interrupt.                               |

## EIMSK

*External Interrupt Mask Register*

| Bit    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------|------|------|------|------|------|------|------|------|
| EIMSK: | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 |

## **INTn**

- **1** aktiviert den externen Interrupt
- **0** deaktiviert den externen Interrupt

## **Interrupt Vektor**

*INT0\_vect, INT1\_vect, INT2\_vect, ....*