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from litex.build.generic_platform import *
from litex.build.altera import AlteraPlatform
from litex.build.altera.programmer import USBBlaster

# IOs ----------------------------------------------------------------------------------------------

_io = [
    ("clk50", 0, Pins("V11"), IOStandard("3.3-V LVTTL")),

    ("user_led", 0, Pins("W15"), IOStandard("3.3-V LVTTL")),
    ("user_led", 1, Pins("AA24"), IOStandard("3.3-V LVTTL")),
    ("user_led", 2, Pins("V16"), IOStandard("3.3-V LVTTL")),
    ("user_led", 3, Pins("V15"), IOStandard("3.3-V LVTTL")),
    ("user_led", 4, Pins("AF26"), IOStandard("3.3-V LVTTL")),
    ("user_led", 5, Pins("AE26"), IOStandard("3.3-V LVTTL")),
    ("user_led", 6, Pins("Y`6"), IOStandard("3.3-V LVTTL")),
    ("user_led", 7, Pins("AA23"), IOStandard("3.3-V LVTTL")),

    ("key", 0, Pins("AH17"), IOStandard("3.3-V LVTTL")),
    ("key", 1, Pins("AH16"), IOStandard("3.3-V LVTTL")),

    ("sw", 0, Pins("Y24"), IOStandard("3.3-V LVTTL")),
    ("sw", 1, Pins("W24"), IOStandard("3.3-V LVTTL")),
    ("sw", 2, Pins("W21"), IOStandard("3.3-V LVTTL")),
    ("sw", 3, Pins("W20"), IOStandard("3.3-V LVTTL")),

    ("serial", 0,
        Subsignal("tx", Pins("B21"), IOStandard("3.3-V LVTTL")),                                    #
        UART pins in documentation B21 (HPS_GPIO49) general GPIO pin Y15
        Subsignal("rx", Pins("A22"), IOStandard("3.3-V LVTTL"))                                     #
        UART pins in documentation A22 (HPS_GPIO50) general GPIO pin AC24
    ),

    ("sdram_clock", 0, Pins("AD20"), IOStandard("3.3-V LVTTL")),                                    #
    ALLOW_SYNCH_CTRL_USAGE OFF -to *|SDRAM_*
    ("sdram", 0,
        Subsignal("a", Pins("Y11 AA26 AA13 AA11 W11 Y19 AB23 AC23 AC22 C12 AB26 AD17 D12")),        #
        FAST_OUTPUT_REGISTER ON -to SDRAM_A*
        Subsignal("ba", Pins("Y17 AB25")),                                                          #
        FAST_OUTPUT_REGISTER ON -to SDRAM_BA*
        Subsignal("cs_n", Pins("Y18")),                                                             #
        FAST_OUTPUT_REGISTER ON -to SDRAM_n*
        Subsignal("cke", Pins("AG10")),                                                             #
        FAST_OUTPUT_REGISTER ON -to SDRAM_n*
        Subsignal("ras_n", Pins("W14")),                                                            #
        FAST_OUTPUT_REGISTER ON -to SDRAM_n*
        Subsignal("cas_n", Pins("AA18")),                                                           #
        FAST_OUTPUT_REGISTER ON -to SDRAM_n*
        Subsignal("we_n", Pins("AA19")),                                                            #
        FAST_OUTPUT_REGISTER ON -to SDRAM_n*
        Subsignal("dq", Pins("E8 V12 D11 W12 AH13 D8 AH14 AF7 AE24 AD23 AE6 AE23 AG14 AD5 AF4 AH3")),  #
        FAST_OUTPUT_REGISTER ON -to SDRAM_DQ[*] FAST_OUTPUT_ENABLE_REGISTER ON -to SDRAM_DQ[*]
        Subsignal("dm", Pins("AG13 AF13")),                                                         #
        FAST_OUTPUT_REGISTER ON -to SDRAM_DQM*
        IOStandard("3.3-V LVTTL")
    ),

#    ("epcs", 0,
#        Subsignal("data0", Pins("H2")),
#        Subsignal("dclk", Pins("H1")),
#        Subsignal("ncs0", Pins("D2")),
#        Subsignal("asd0", Pins("C1")),
#        IOStandard("3.3-V LVTTL")
#    ),

#    ("i2c", 0,
#        Subsignal("sclk", Pins("F2")),
#        Subsignal("sdat", Pins("F1")),
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#         IOStandard("3.3-V LVTTL")
#     ),

#     ("g_sensor", 0,
#         Subsignal("cs_n", Pins("G5")),
#         Subsignal("int", Pins("M2")),
#         IOStandard("3.3-V LVTTL")
#     ),

#     ("adc", 0,
#         Subsignal("cs_n", Pins("A10")),
#         Subsignal("saddr", Pins("B10")),
#         Subsignal("sclk", Pins("B14")),
#         Subsignal("sdat", Pins("A9")),
#         IOStandard("3.3-V LVTTL")
#     ),

    ("gpio_0", 0,
        Pins("Y15 AC24 AA15 AD26 AG28  AF28 AE25 AF27 AG26 AH27 AG25 AH26 AH24 AF25 AG23 AF23 AG24 AH22 AH21
        AG21 AH23 AA20 AF22 AE22 AG20 AF21 AG19 AH19 AG18 AH18 AF18 AF20 AG15 AE20 AE19 AE17"),
        IOStandard("3.3-V LVTTL")
    ),
#     ("gpio_1", 0,
#         Pins("AG13 AF13 AG10 AG9 U14 U13 AG8 AH8 AF17 AE15 AF15 AG16 AH11 AH12 AH9 AG11"),
#         IOStandard("3.3-V LVTTL")
#     ),
]

# Platform -----------------------------------------------------------------------------------------

class Platform(AlteraPlatform):
    default_clk_name = "clk50"
    default_clk_period = 1e9/50e6

    def __init__(self):
        AlteraPlatform.__init__(self, "5CSEBA6U23I7", _io)

    def create_programmer(self):
        return USBBlaster()
```