Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Bachelor's Thesis, Forschungspraxis, Assistant (Student)

Porting OpenASIP Custom Operations to CoreDSL Syntax

The goal of this project ist to evaluate the large pool of custom operations supported by the OpenASIP2.0 Co-Design toolchain on our instruction set simulator (ISS) named ETISS using the CoreDSL ecosystem.

Steps:

1. Literature Research
2. Familiarize with involved tools (OpenASIP, CoreDSL, CoreDSL)
3. Collect list of all custom OpenASIP operations
4. Develop methodology for translating the custom OpenASIP operations to the CoreDSL syntax
5. Generate ETISS architectures using the new instructions
6. Evaluate/Test/Benchmark the custom operations
7. Optional: Allow ETISS to be used as OpenASIP2.0 target architecture.

Related Literature/Tools:

- https://riscv-europe.org/summit/2023/media/proceedings/posters/2023-06-07-Karsten-EMRICH-abs
- https://www.researchgate.net/profile/Ulf-Schlichtmann/publication/322673899_The_extendable_trans
- https://github.com/tum-ei-eda/etiss
- https://github.com/Minres/CoreDSL/wiki/CoreDSL-2-programmer's-manual
- http://openasip.org/release_2_0.html
- https://zenodo.org/records/6670559
- https://github.com/cpc/openasip

Prerequisites

- Experience with RISC-V ISA (Assembly & Microarchitecture)
- Deep knowledge about Python programming
- Moderate C/C++ experience

Contact

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Advisors

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