Electronic Design Automation
TUM Department of Electrical and Computer Engineering
Technical University of Munich

Forschungspraxis

DVCon Challenge 2025: Precise Power Estimation of SoC in SystemC

Precise power estimates enable more efficient designs and give directions for energy saving. This enhances battery cycles and limits the need for cooling setups. However, currently power estimates are mostly based on date from late stages in the design process. However, the largest knobs for improvements in the system architecture exist in early design stages on the high level design, which can be modeled for example with SystemC.

This area is tackled by this year's challenge of the DVCon in Munich in October 2025:

How well can you predict and analyze power consumption of a small application with a compact SystemC model? Help developers with your ideas! (https://dvconchallenge.de/). In this project, you should take the DVConf challenge and participate with your ideas and solutions in this contest. At the end of this contest, you will be credited with the credits for the FP/IDP.

Prerequisites

- interest in power dissipation modeling and the high level design stage

- very profound knowledge on SystemC

- basic knowledge on CMOS power dissipation

- ability to work independently

- willingness to submit your solution to the DVcon Challenge and to present it at the conference

Contact

If you are interested in this topic, you can send me your application to: philipp.fengler@tum.de

Advisors

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