SRN: _ _ _ _ _ _ _ _ _ _ _ _

# PES University, Bangalore

(established under Karnataka Act No. 16 of 2013)

## End Semester Assessment (ESA) B. Tech. 3rd Semester, Dec. 2017

## UE16CS201: Digital Design and Computer Organization (Autonomy)

Time: 3 hours | All questions to be answered | Max. marks: 100

1. (a) How many boolean functions of $n$ inputs are there? (3)

   (b) Use K-map technique to obtain minimized SOP formula for the following boolean function:

   $$F(a, b, c, d) = \Sigma(1, 2, 3, 5, 6, 7, 12, 13, 14, 15)$$

   (6)

   (c) Draw a 4-bit adder subtracter circuit. In addition to four bit inputs a and b, another input is sub. When sub is high, the output is a-b, else the output is a+b. In addition to above four bit output, cout, the carry out of the MSB bit is another output. Try to minimize logic used. (5)

   (d) A *symmetrical* boolean function is a boolean function whose value does not depend on the permutation (ordering) of its input bits, i.e., it depends only on the number of ones in the input. For example XOR is a symmetrical boolean function. As another example, for a 3 input symmetrical boolean function, the output for inputs 001,010 and 100 must be the same. How many symmetrical boolean functions of $n$ inputs are there? (6)

2. (a) Draw the diagram of a 4:1 mux constructed using 2:1 muxes, using a minimum of 2:1 muxes. (2)

   (b) Draw the diagram of a 6:1 mux constructed using 2:1 muxes, using a minimum of 2:1 muxes. (4)

   (c) Add the numbers 11010110, 00101011 and 10011110 using carry save technique (reducing the three numbers to two and then producing the final sum). (3)

   (d) Draw the Wallace tree diagram for adding five 8-bit numbers, labelling each wire with its width and each node (box) with number of CSAs it contains. (4)

   (e) A two's complement adder takes in two n-bit numbers and produces an n-bit output and cout, the carry out of the MSB (assume other carry bits are also available for use). What logic is required to compute the overflow? (3)

   (f) Consider twos complement addition of two numbers. Under what circumstances would the overflow signal go high? Explain in terms of signs of the two input numbers (both negative, both positive, one negative and other positive). (4)

3. (a) Draw the logic circuit of a D latch with load enable input. Using two such D latches (with enable input) draw the logic circuit for an edge triggered D flip-flop. (4)

   (b) Draw the logic circuit for a simple (not twisted) 8-bit ring counter using three flip-flops and whatever combinational logic is required. The inputs are count and clk, the circuit counting only when count is high at a positive clk edge. (4)

(c) Consider a microprocessor that needs to perform, in a single clock cycle, an arithmetic or logic operation (add, sub, and etc.) on value stored in its registers. The two inputs and the output can come from or go to any of the registers. To achieve the single cycle operation, the register file of the microprocessor requires how many read and write ports? (4)

(d) How does a synchronous counter differ from other types? Which is considered better and why? (4)

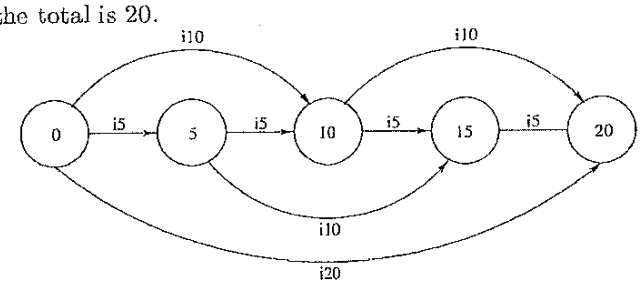
(e) What is the key property of the Gray code sequence? Why is it useful? (4)

4. (a) Sketch the logic circuit block diagram of a shift and add multiplier that multiplies two 32-bit numbers to produce a 64-bit result. Label the wire widths, sizes of registers and adder(s), and shift capabilities required of any registers. (5)

(b) 7 bits of data was encoded with Hamming code (no SECDED) and the resulting 11-bit number was stored in memory. When read back from memory, the value was 00111010101. Bits are numbered with leftmost bit being 1 (LSB) and rightmost bit being bit 11 (MSB) with parity bits in usual positions. Compute the corrected sequence and extract the data bits from it. (5)

(c) Sketch the block diagrams of Mealy and Moore Machines. State the key difference between them. (4)

(d) Consider a vending machine taking rupee notes of 5, 10 and 20 denomination so that the total adds to 20. Since notes may be entered in any sequence, the following FSM can be used to ensure the total is 20.




Design an OHE (One Hot Encoding) based logic to implement above FSM. The inputs to the FSM are i5, i10 and i20 which, if one, indicate current note has a denomination of 5, 10, or 20 respectively. No need to implement any outputs (output would be taken from flip-flops). You can assume that initially only the flip-flop corresponding to the '5' state stores a 1. (6)

5. (a) I/O processing can be done using either polling (busy waiting) or interrupts. Which is better? Why? (2)

(b) What are the four key components of a microprocessor? (4)

(c) For a modern microprocessor, the shift and add multiplier is too slow and so a more high performance multiplier design is used. What are the three key components of the faster multiplier? (3)

(d) While designing the format of floating point numbers, a certain number of the bits are used for the mantissa while the rest are used for the exponent. What is the advantage of allocating more bits to the mantissa at the expense of the exponent? What is the advantage of allocating more bits to the exponent at the expense of the mantissa? (3)



P2/3