1.4 Memory:

Uses 32-bit words of 4 bytes each

memory is circular, so the max address is adjacent to address zero

the fetch stage is an implicit read

lw and sw are explicit memory accesses

the execution environment determines where in the memory implicit and explicit accesses are allowed. These areas can overlap

An implicit access that has no exceptions or side effects can occur arbitrarily early, meaning that in theory the whole instruction memory can be read before a single line is executed.

See chapter 17 for a memory consistency model

1.5 Instruction Length Encoding:

instructions are 32 bit and word aligned

IALIGN refers to the standard 32 bit instruction size

ILEN is max instruction length (32 for base riscv)

32 bit instructions have their lowest two bits set to 11

encoding with [15:0] = 0 is illegal

encoding with [ILEN-1:0] = 1 is illegal

instructions are little-endian (MSB is the rightmost bit)

1.6 Exceptions, Traps, and Interrupts:

Exceptions are defined as unusual conditions occurring at runtime

Interrupts are defined as external asynchronous events that may cause an unexpected transfer of control

A trap is when control is transferred to a trap handler in the case of an exception or interrupt

from the perspective of software running in the environment, traps can be handled in four ways with differing levels of visibility

1. Contained Trap: Trap is visible to, and handled by the software

2. Requested Trap: Synchronous exception that is an explicit call to the execution environment on behalf of software (ex. A System Call). Execution may not resume until the requested action is taken by the system environment

3. Invisible Trap: Trap is handled transparently by the execution environment and execution resumes normally after the trap is handled. The software running inside the environment is not aware of the trap.

4. Fatal Trap: Trap represents a fatal failure and causes the execution environment to terminate execution.

1.7 Unspecified behaviors and values:

The architecture defines what implementations must do and any constraints on what they must do, but places where the implementation is left to the user, the term UNSPECIFED is used.

2.1 Base integer ISA:

32 registers 32 bits wide labeled x0-x31

register x0 is hardwired with all bits = 0

registers x1-x31 are general purpose and can hold a collection of Boolean values or two's complement signed binary integers

there is one additional register pc that holds the instruction address

There is no dedicated stack pointer or subroutine return address, but convention states that...

x1 holds the return address for a call

x5 is available as an alternate link register

x2 is the stack pointer

2.2 Base Instruction Formats:

in the base RV321 ISA, there are four core instruction formats (R/I/S/U)

all instructions are 32 bits in length and are word aligned

the behavior upon decoding a reserved instruction (special opcode) is UNDEFINED

source and destination registers (rs1, rs2, rd) are at the same position in all formats to simplify decoding

A group of colorful rectangular objects

AI-generated content may be incorrect.

Immediates are always sign extended, and are generally packed towards the leftmost available bits in the instruction.

Immediates are labeled with the bit position in the immediate value being produced (ex. For s-type the immediate is split into two locations, but results in one number)