littleBits

HDK Manual

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1.0.0 Documentation Conventions

1.0.1 Standard text. This is the standard typeface.

1.0.2 *Italics represent information that may change depending on the design.*

1.0.3 The pound sign # represents indeterminate numerals.

1.0.4 "ALL CAPS" in quotations are references to specific elements of software tools like EagleCAD.

The littleBits company will be represented by the abbreviation "LB".

2.0.0 Required Engineering Deliverables

2.0.1 Product Requirements Document (PRD) conforming to LB standards as described in

this document. Template PRDs are provided by LB (**HDK-hardware-dev-manual/Design/Templates for PRD**).

2.0.2 Schematic Diagram (SCH) conforming to LB standards as described in this document. Template SCHs are provided by LB in the **HDK-eagle-templates-libraries/Eagle Templates for SCH and BRD** folder of the HDK. A completed example SCH is included in the /pcb folder of the Complete Example Project included in the HDK (**rtmTemplate**).

2.0.3 PCB Layout (PCB) conforming to LB standards as described in this document. Template PCBs are provided by LB in the **HDK-eagle-templates-libraries/Eagle Templates for SCH and BRD** folder of the HDK. A completed example PCB (.brd file) is included in the /pcb folder of the Complete Example Project included in the HDK (**rtmTemplate**).

2.0.4 Gerber files (GRB) conforming to LB standards as described in this document. A completed example is included in the /gerbs folder of the Complete Example Project included in the HDK (**rtmTemplate**).

2.0.5 Bill of Materials (BOM) conforming to LB standards as described in this document. Template BOMs are provided by LB in the **HDK-hardware-dev-manual/Design/Templates for BOM** folder of the HDK. A completed example BOM is included in the Complete Example Project included in the HDK.

2.0.6 Fab drawing (FAB) conforming to LB standards as described in this document. An example FAB is included in the gerbs folder in the Complete Example Project (**rtmTemplate**) included in the HDK.

2.0.7 Assembly Drawing (ASY) conforming to LB standards as described in this document. An example ASY is included in the docs/assy folder in the Complete Example Project (**rtmTemplate**) included in the HDK.

2.0.8 Test Procedure and Test Data (TST) conforming to LB standards as described in this document.

2.0.9 Datasheets for all unique parts in the design which are not already included in the SCH, PCB, and BOM templates.

2.1.0 Delivery of Items to littleBits

2.1.1 Deliverables must be organized into folders in a way that follows the Complete Example Project included in the HDK.

2.1.2 Once organized, the deliverables should be compressed into a single .zip file with the format: *moduleType##_moduleName*-v03(*#_#x*)

3.0.0Design Requirements

3.0.1 System Parameters:
VCC = 5VDC
BitSnap connector max current = 1A
Nominal temperature range = 10C to 40C

3.0.2 Female bitSnap connector pinout:
Pin 1: GND (ground, 0VDC)
Pin 2: SIG (signal, 0 to 5 V continuous)
Pin 3: VCC (power, 5VDC)

3.0.3 Male bitSnap connector pinout:
Pin 1: VCC (power, 5VDC)
Pin 2: SIG (signal, 0 to 5 V continuous)
Pin 3: GND (ground, 0VDC)

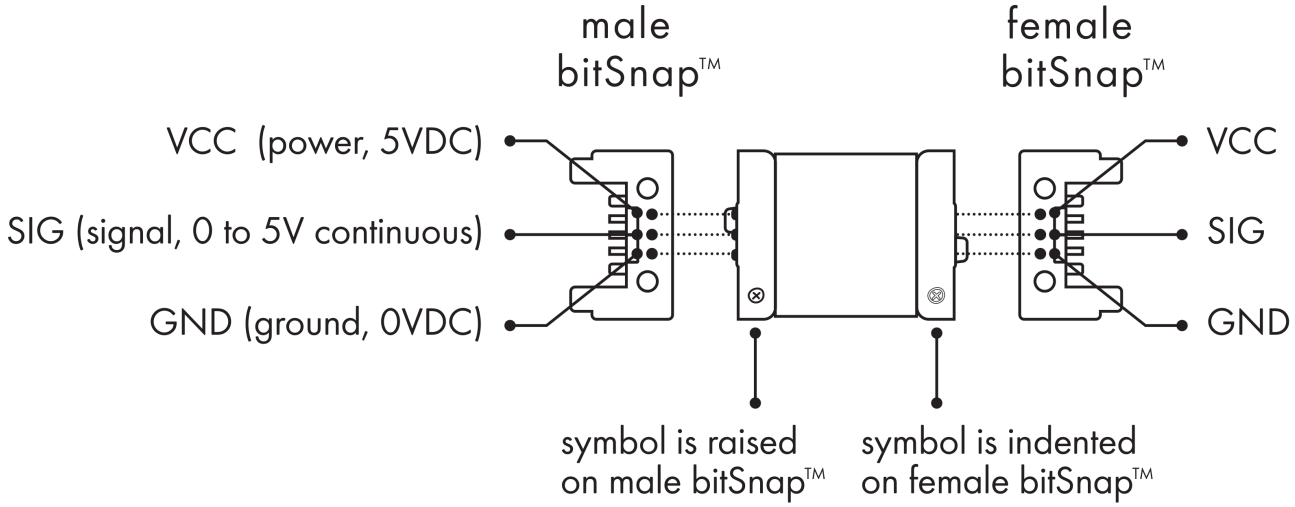

Figure 1: Male and female bitSnap™ connector pinouts

3.0.4 All inputs must be high impedance. The preferred input impedance must be equal to or greater than 1 MΩ (megOhm). It is acceptable to have a lower impedance if

the circuit design does not permit 1 MΩ. In these cases, the input impedance may be no lower than 100 KΩ.

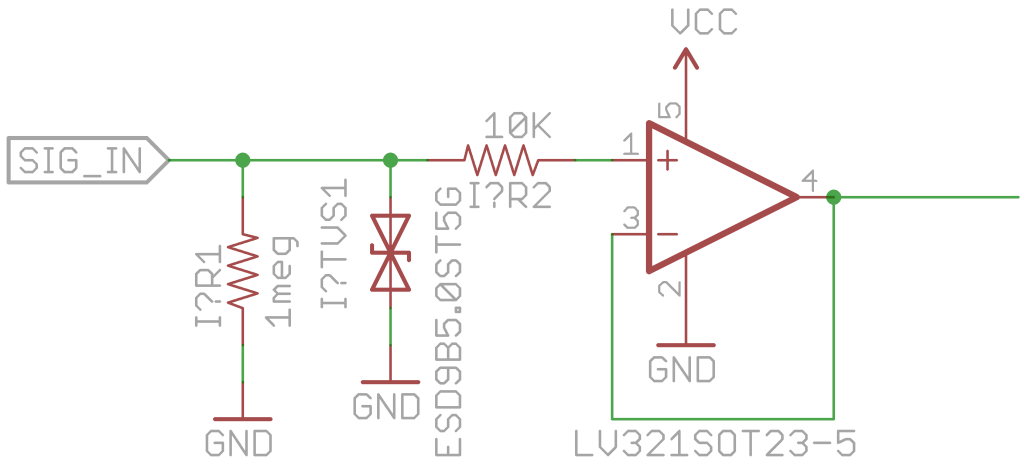

Figure 2: Example of an input stage, included in the Eagle templates

3.0.5 All outputs must be low impedance, with symmetric drive characteristics (yields same performance when either sinking or sourcing current.) The output impedance must be less than 100 ohms. This is typically achieved by using a buffer or follower circuit at the output. Outputs must never be allowed to float. Outputs must be rail-to-rail.

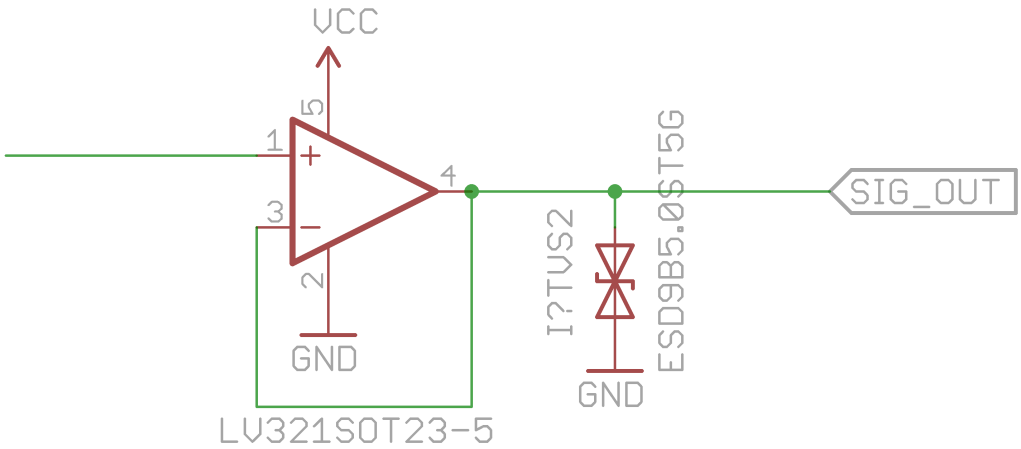

Figure 3: Example of an output stage, included in the Eagle templates

3.0.6 Polarity conventions must be observed unless otherwise specified. If output polarity is inverted with respect to inputs and/or violates reasonable expectations, consultation with littleBits for guidance is required.

3.0.7 The design must faithfully execute the letter and intent of the PRD. If there are any ambiguities, consultation with littleBits is required.

3.0.8 All ICs must have at least one 0.1 uF bypass capacitor on every IC power supply. Some designs will require additional bypassing.

3.0.9 Inputs: Every bitSnap input must have a series 10K current limiting resistor on the SIG line (see Figure 2).

3.0.10 Inputs: Every bitSnap input must have a shunt TVS diode, or equivalent ESD countermeasures (see Figure 2).

3.0.11 Inputs: Floating bitSnap inputs are **not** permitted. For this reason, every input needs to have a pull-down, pull-up, or reference network. To maintain high input impedance, this network must usually be greater or equal to 1 MΩ. In most cases, this will consist of a single 1 MΩ pull-down resistor, which keeps the input at ground potential if the input is not connected. The second most common configuration will have a 1 MΩ pull-up.

3.0.12 Preferred Parts. littleBits recommends the use of specific part numbers for typical functions such as opamps, switches, potentiometers, and others. A list of these preferred parts can be found in libraries/lbPreferredParts.xlsx

4.0.0 Preparations

4.0.1 Download and install the following from the HDK-eagle-templates-libraries repository

Parts Libraries:
libraries/LITTLEBITS140915.lbr
Cam Processor Job Files:
libraries/LB-gerb274x_140813.cam //for 2-layer boards
libraries/LB-gerb274x4LAYER_140813.cam //for 4-layer boards
Design Rules Files:
libraries/littleBitsDRC_140813.dru //for 2-layer boards
libraries/littleBits4-LAYERDRC_140813.dru //for 4-layer boards
Drill Processing ULP:
libraries/lbdrl120906.ulp

5.0.0Product Design Requirement (PRD)

5.0.1 The PRD should be created by the developer from the Design/Templates for PRD/prd_template.xls template provided by LB.

5.0.2 The PRD should contain the following sections:

OVERVIEW:

PRODUCT TYPE: May be either WIRE, POWER, INPUT or OUTPUT.

DESCRIPTION OF PRODUCT: A concise but complete description of the functionality of the bit.

FEATURE LIST: A numbered list of all the features of this bit.

CRITICAL COMPONENTS: A numbered list of all parts critical to the functionality of the Bit that may not be easily substituted or may have long lead times for ordering.

MECH. REQUIREMENTS:

SIZE: parameter must be included. Should match the size of the template being used: **SMALL**, **MEDIUM**, **LARGE**, **XLARGE**, **XLARGEWIDE**, or **XLARGEWIDE BIT SIZE.** If board sizes will not suit intended design, contact littleBits for guidance.

INPUT and **OUTPUT**: both parameters must list the number of Input and Output bitSnaps.

Additional parameters should be added if the bit contains additional mechanical parts.

For a quick comparison of bits modules sizes, refer to the Standard and Custom Size References in Design/Eagle Templates for SCH and BRD.

ELECT. REQUIREMENTS:

All requirements should remain as set in the template unless there is a specific reason to change or add to them. Consult with LB with any questions.

DESIGN REQUIREMENTS:

All requirements should remain as set in the template unless there is a specific reason to change or add to them. Consult with LB with any questions.

ACCESSORIES: For internal LB use only.

RELATED PRODUCTS: For internal LB use only.

LAYOUT PROPOSALS: For internal LB use only.

5.0.3 Save the PRD in the bit's **docs/prd** directory with the format: ***moduleType#-moduleName*.xls**

6.0.0Schematic (SCH)

6.0.1 The schematic must be designed in EagleCAD version 6 or later.

6.0.2 File name must be in this format:

***moduleType##-moduleName*-v03(*#_#x*).sch**

- **(*#_#x*)** =
  - first digit: schematic revision number
  - second digit: PCB revision number
  - the "x" connotes that the design is in progress and has not been released for manufacturing.
- **v03** = the littleBits system is version 0.3
- ***moduleName*** = the name of the module

moduleType## = module type is one of the following: p (power), i (input), o (output), or w (wire), followed by a one or 2-digit number.

Example: i21_MICROPHONE-v03(4_4x).sch

6.0.3 The ***moduleName*** and the number following ***moduleType*** will be provided by LB.

6.0.4 The schematic should be based on one of the SCH templates provided by LB, found in **Design/Eagle Templates for SCH and BRD**.

6.0.5 Schematic grid must be set to 0.1 inch.

6.0.6 The design must contain a FRAME-LETTER from the LITTLEBITS140915.lbr library placed at position (0,0). This is included in all the templates. All the other parts of the design must be placed within the bounds of this frame.

6.0.7 All schematic symbols used must be from the LITTLEBITS140915.lbr littleBits Eagle library. If specific device does not exist it must be created and verified by littleBits.

6.0.8 The circuit should read from left to right when possible.

6.0.9 Male bitSnap connectors are inputs, and must be placed on the left side of the frame. Female bitSnap connectors are outputs, and must be located on the right side of the frame.

6.0.10 The bitSnap symbol terminals are labeled VCC, SIG, and GND. Each of these pins must be connected to the NET corresponding to those labels.

6.0.11 Each Net connection should leave space to see the green Net line.

6.0.12 Every schematic symbol should have a reference designator in the "NAME" field.

6.0.13 Every schematic symbol must have information in the "VALUE" field. For passives, the value should be the component value (i.e., resistance in ohms, or capacitance in microFarads, etc.) and semiconductors should list the manufacturer's part number (i.e., LV321 for our littleBits standard op amp).

6.0.14 "NAME" and "VALUE" fields must all be visible on the schematic. The text should be legible and not overlap with other text or symbols.

6.0.15 The Net GND must represent ground and the Net VCC must represent Power.

6.0.16 GND symbols should face downward and VCC symbols should face upward whenever possible.

6.0.17 Functions of interface elements (switches etc.) should be labeled on the info layer.

6.0.18 Nets that are not directly connecting two points should be labeled. SIG net should always be flagged with a cross-reference label.

7.0.0 Printed Circuit Board (PCB)

7.0.1 The PCB layout must be designed in EagleCAD version 6 or later.

7.0.2 File name must be in this format:

***moduleType##-moduleName*-v03(#_#x).sch**

- **(#_#x)** =
  - first digit: schematic revision number
  - second digit: PCB revision number
  - the "x" connotes that the design is in progress and has not been released for manufacturing.
- **v03** = the littleBits system is version 0.3
- ***moduleName*** = the name of the module

moduleType## = module type is one of the following: p (power), i

(input), o (output), or w (wire), followed by a one or 2-digit number.

7.0.3 The ***moduleName*** and the number following ***moduleType*** will be provided by LB.

7.0.4 Set the PCB layout primary grid to 0.05mm. Set the alternate grid to 0.01mm.

7.0.5 The .brd file must be generated from the .sch file, by using the FILE□SWITCH TO BOARD menu command in the schematic editor.

7.0.6 The origin of the FRAME-LETTER package must be set to coordinates (0, 0). All the other parts of the design must be placed within the bounds of this frame.

7.0.7 The board outline and the dimension layer must not be altered.

7.0.8 All packages used must be from the LITTLEBITS140915.lbr littleBits Eagle library. If specific device does not exist it must be created and verified by littleBits.

7.0.9 Minimum track width shall be 0.008 inches (0.2032mm). The default width is 0.016 inches (0.4064mm). The default width should generally be used when possible. There should also be a 1mm track from the VCC pin of the input bitSnap(s) to the VCC pin of the output bitSnap(s) as exemplified in the templates.

7.0.10 Minimum clearance requirement shall be 0.008 inches (0.2032mm).

7.0.11 To assure that vias and polygons are rendered properly the Design Rules File listed in the Preparations section (4.0.0) should be loaded and an initial check run before the PCB is routed. If this is not completed, EagleCAD will follow its default design rules and can create problems later on in the design process.

7.1.0 Component Choice and Placement

7.1.1 bitSnap connectors must not be moved from their original positions in the templates.

7.1.2 All components besides bitSnap connectors which are included in the templates may be moved and their traces rerouted if necessary.

7.1.3 Resistors, capacitors, inductors, and other 2-lead passives should be SMD0603 chip devices unless design requirements do not allow it.

7.1.4 BGA packages are not allowed; QFNs are acceptable but LB

recommends SOICs as they are easier to work with. IC packages should be as small as necessary, but no smaller. Use good judgment, and consult littleBits with any questions.

7.1.5 Pad spacing from component to component should be no less than 0.024 inches (0.6096mm) unless design requirements do not permit it. This spacing allows routing of a minimum width 0.008-inch (0.2032mm) trace between the pads without violating the minimum clearance requirement.

7.1.6 Top layer components must be placed according to the layout proposal found in the PRD.

7.1.7 Bottom layer components should be placed with electrical performance in mind but with attention paid to maintaining balance and symmetry between the X and Y-axis of the PCB. See reference layouts in Appendix A.

7.1.8 Placing components over bottom layer silkscreen is acceptable. Neat component placement takes priority. See figures 1 and 2, and refer to section 7.3.0 for more information on the silkscreen layers.

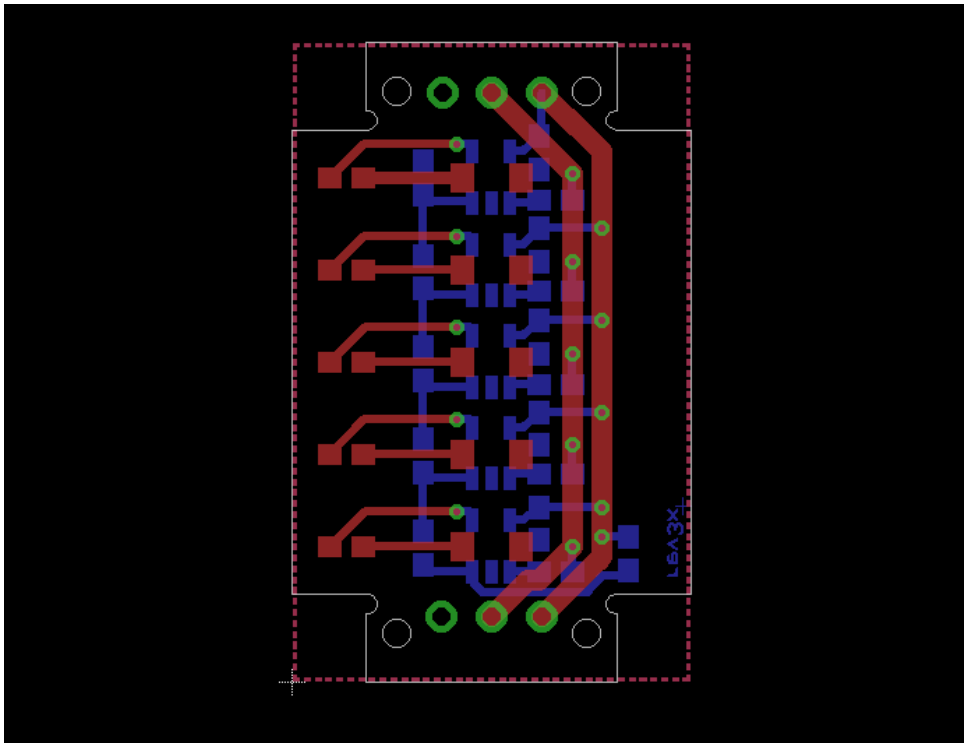

Figure 4: Example of neat component placement. Note how components are placed in line with each other.

7.1.9 Components should be placed in 90 orientations and in line with other components when possible.

7.1.10 Reference designators should be legibly placed around components. Smash parts as needed. Names should generally be placed along the long side of the component (lengthwise) and the value along the short side (widthwise). This can be reversed if the length of the text is inversely proportional and the values are longer than the names.

7.2.0 Routing

7.2.1 The traces which are already routed in the templates may be altered if necessary.

7.2.2 Minimum track width is 0.008 inches (0.2032mm). Default track width is 0.016 inches (0.4064mm).

7.2.3 Minimum clearance requirement is 0.008 inches (0.2032mm).

7.2.4 Traces should run at 90 and 45˚angles with routes running parallel. Avoid other angles and arcs.

7.2.5 Vias must be round, and have a 0.4064mm drill diameter. Avoid placing vias directly on the silkscreen text on the top side of the board.

7.2.6 There should be a Ground Pour on both layers unless a VCC plane is needed.

Polygon settings:
Width = 0.008inches (0.2032mm)
Polygon Pour = Solid
Isolate = 0 (the isolate dimension is set in the Design Rules)
Thermals On
Orphans Off

7.2.7 The PCB revision number (the second number in parentheses in the file name from section 6.0.2 above) must be placed on the bottom copper layer in bottom right corner (screen view). Font specifications are:

Size = 0.8128mm
Ratio = 12%
Font = vector

This text is already placed in the PCB templates. Change the X in "revX" to the PCB revision number.

7.3.0 **Silkscreen**

7.3.1 Silkscreen layers are **tPlace** (top layer), **bPlace** (bottom layer)

7.3.2 Bottom layer silkscreen including littleBits and OSHW logos are positioned and locked in the standard PCB outline templates, and must not be altered.

7.3.3 Company logos should be placed top and center on the underside of the PCB. Please keep your logo within the dimensions of 10mm x 6mm on the PCB.

7.3.4 The module number and name must be placed on the tPlace layer. They should be centered on the X-axis and the highest point of the text should be 0.7mm from the right edge of the PCB. The number and name should be spelled out using any vector font.

7.4.0 Design Rule Check

7.4.1 Board layouts must be verified using the littleBits DRC file provided.

7.4.2 The DRC file must be run with only layers 1 to 20 turned on.

7.4.3 Width error of revision number copper text can be ignored.

7.5.0 Drills

7.5.1 The littleBits drill ULP (lbdrl120906.ulp) should be run at the completion of circuit design.

7.5.2 The chart created by running the drill ULP should be placed below the PCB (see Figure 5).

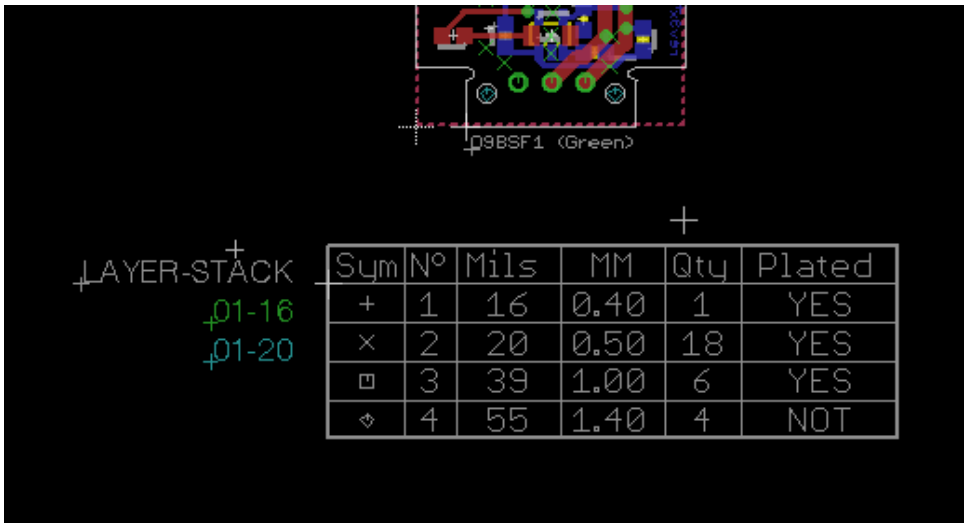

Figure 5: Example of a chart created by the drill ULP on the .brd file.

8.0.0Gerber Files (GRB)

8.0.1 Gerber files must be generated using the littleBits CAM processor job file (LB-gerb274x_140813.cam).

8.0.2 Gerber files should be placed in the bit's **/gerbs** folder.

9.0.0Bill of Materials (BOM)

9.0.1 A BOM should be built from one of the .xls templates provided by LB. Each BOM template contains all of the components present in its corresponding PCB template.

9.0.2 All items in the BOM must follow the same format as those in the template:

ITEM: must be numbered sequentially with the format: *moduleType#-itemNumber*
littleBits Part Number – must be as it appears in list of approved parts provided by LB, with the exception of the PCB, which should be named: ***moduleType#-moduleName*-v03**
Description: the part's description
Rev: for bitSnaps Rev is **v0.3**, for PCB Rev is the PCB rev#, for all others rev is **na**.
Qty Per: Quantity of item per bit.
MFG: Manufacturer name
Mfr Part Number: Manufacturer Part Number
Ref Loc: reference location or locations of the part in the PCB and schematic.
SUB ALLOWED?: **NO** for all items.

9.0.3 BOM Revisions are lettered rather than numbered.

9.0.4 A new Revision occurs every time a bit changes form or function. Any addition or removal of components warrants a new Revision. Any change in a component's value other than a change in Manufacturer warrants a new Revision.

9.0.5 A record of all Revisions should be kept in the Revision History.

9.0.6 The Approvals section of the BOM is for internal LB use only.

9.0.7 File name should be in the format:
***moduleType##_moduleName*_BOM_rev#.xls**

10.0.0 Creating Fab Drawings (FAB)

In Eagle:

10.1.1 Run ERC. Confirm there are no errors.

10.1.2 Activate only layers 0-20 and run a DRC **(HDK-eagle-templates-libraries\Libraries\littleBits DRC)**. Confirm there are no errors (besides the acceptable "rev" text error).

10.1.3 Confirm there are no unrouted air wires.

10.1.4 Activate only layers: **Pads, Vias, Dimensions, Milling, Measures, dxf, DrillLegend, DrillLegend_01-16, DrillLegend_01-20**.

10.1.5 Export as PDF (FILE PRINT). Set parameters as follows:
Printer = Print to File (PDF))
Output File = **/gerbs/*moduleType##_moduleName*-v03(rev#_#x).pdf**
Paper = A4 (210x297 mm, 8.3x11.7 inch)
Orientation = Landscape
Alignment = Center
Area = Full
Options = all off
Scale Scale Factor = 1.3
Scale Page limit = 1
Calibrate X = 1
Calibrate Y = 1
Border Left = 8.5mm
Border Right = 14.2mm
Border Top = 8.5mm
Border Bottom = 8.5mm

10.1.6 File name should be in the format: ***moduleType##_moduleName*-v03(#_#x)FAB.pdf**

10.1.7 Place the PDF in the appropriate **/gerbs** subfolder.

11.0.0 Creating Assembly Drawings (ASY)

11.1.1 All component reference designators should be arranged to optimize legibility. Generally, names should be placed lengthwise along the longest side of the board, next to their respective components; values should be placed widthwise.

11.1.2 User Interface should be set to white. On the menu toolbar, click OPTIONS USER INTERFACE, and specify Layout Background as

white.

11.1.3 Top Side

In Eagle:

Activate only layers: **dimension, tPlace, tNames, tValues, and tDocu**. Ensure that all appropriate silkscreen text, components and their names and values are visible in these layers and legible.

Zoom in as much as possible with the entire FRAME-LETTER still visible.

Export Image (FILE EXPORT IMAGE) with the following parameters:

File = *moduleType#_moduleName*-v03 TOP.png

Monochrome = on

DPI = 1000

Area = Window

In Preview or other image-editing software:

Crop image about the PCB

Label connectors (name and color), e.g. "O6BSM1 (Green) " for a male connector.

11.1.4 Bottom Side

In Eagle:

Activate **dimension, bNames, bValues, and bDocu.** Ensure that all appropriate silkscreen text, components and their names and values are visible in these layers and legible.

All components should have bDocu outlines/indicators.

Zoom in as much as possible with the entire FRAME-LETTER still visible.

Export Image (FILE EXPORT IMAGE) with the following parameters:

File = *moduleType#_moduleName*-v03 BOTTOM.png

Monochrome = on

DPI = 1000

Area = Window

In Preview or other image-editing software:

Crop image about the PCB.

Flip board horizontally.

11.1.5 Insert generated PNGs into the ASY template file and complete necessary information (assembly drawing number, description, rev).

Include any special notes for assembly and final packaging.

11.1.6 Save the completed assembly drawing with the format:
moduleType#_moduleName-v03_ASY_rev#.docx

12.0.0 Test

12.0.1 It is difficult to make generalizations about testing, because the test requirements will sometimes vary greatly from design to design. Nevertheless, it is important that every design be tested to ensure adequate safety, performance, and reliability. The following sections outline some minimal test considerations. Modification or supplementation of these requirements will be considered on an individual basis as required. An example test form with explicit details about some of the relevant tests can be found in: MFG/Test Doc/EVTtestForm02.xlsx
Please submit this test document along with all other required documents.

12.0.2 Basic Electrical Requirements:
Verify functionality matches PRD requirements.
Verify nominal performance over VCC range from 4.0 to 5.5 VDC.
Confirm ESD protection/invulnerability on inputs and outputs.
Confirm 10K current limiting Rs on IC inputs.
Confirm 1M (preferred) input impedance.
Unused IC sections must have inputs tied high or low.
Run Electrical Rule Check (ERC) in Eagle.
Verify nominal performance with an input range from 0 to 5.5VDC.
Verify output range of 0 to 5.0VDC.

12.0.3 Bench Testing:
Amplitude sweeps of the inputs.
Frequency sweeps of the inputs.
Pulse stress test. Apply -0.3V to 5.3V squarewaves to all inputs and outputs, and to VCC. Sweep frequencies from 100Hz to 10kHz. Sweep duty cycles from 5% to 95%.
Thermal maximum test. Create worst case conditions, and TOUCH ALL THE COMPONENTS with your fingers. They should not exceed a thermal level to where you cannot keep a finger on any component.
O-scope testing. Apply 0-5V inputs or other appropriate inputs, and observe outputs for appropriate behavior. Consult the PRD for appropriate output behaviors.
4 corners testing– thermal and voltage max and min. The thermal range is 10C to

40C. The VCC range is 4.0V to 5.5V.

12.0.4 Operational Testing:

Operate the new design in every conceivable module configuration, to verify compatibility with existing modules.

A list of module configurations is provided in /Test/ EVTtestForm02.xlsx, but it should not be construed as complete. Depending on the design, and how it is likely to be used, how it interacts with different modules, etc., it may be necessary to test many more configurations. The intent here is to discover any interaction problems with any of the modules already in the system.

12.0.5 Endurance – EMI Testing:

Operate the module under worst case conditions for 24 hours minimum.

Using a piezo ignition element or other surge generator, send electric discharge into the input of the bitsnap and the input of IC chips and check for nominal functionality.