Roll No .....

CS - 605

B.E. VI Semester

Examination, June 2016

Advance Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each questions are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

Unit - I

1. a) Briefly describe hardware and software parallelism.
   b) Define latency and throughput of pipeline.
   c) What is the need of higher performance computers?
   d) Explain Flynn's classification based on multiplicity of instruction streams and data streams.

   OR

   Distinguish between multiprocessors and multicomputers based on their structure, resource sharing and interprocessor communication.

Unit - II

2. a) How many types of vector instruction are there?
   b) What is the importance of memory consistency model?
   c) Define the terms: Access time, bandwidth.

   d) Discuss and compare the characteristics of RISC and CISC architecture.

   OR

   What is the basic concept of VLIW approach?

Unit - III

3. a) What is pipeline CPI?
   b) Explain multifunctional arithmetic pipelines.
   c) Explain Tomasulo's algorithm.
   d) Discuss different pipeline design for processor.

   OR

   Explain about data and control hazards and internal forwarding and register tagging.

Unit - IV

4. a) Describe the two levels of threads.
   b) Discuss the directory based cache coherence protocol.
   c) Explain the models of memory consistency.
   d) List two approaches to cache coherence protocol.

   OR

   What are snoopy protocols? When is it used?

Unit - V

5. a) Discuss the features of parallel language.
   b) State and prove Amdahl's law.
   c) Explain Array processing.
   d) Discuss about deterministic scheduling models for multiprocessor system.

   OR

   Explain the various pipeline vector processing methods.

******