Roll No .....

MCIT - 203

M.E./M.Tech., II Semester

Examination, July 2015

Advance Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note : Total number of Eight questions. All questions carry equal marks. Attempt any five questions. Assume missing data, if any, suitably.

1. a) Explain, how instruction set, compiler technology, CPU implementation and control affect the CPU performance?
   b) Compare Flynn's and Handler's classification for parallel computing structures.

2. a) Compare control flow, data flow, and reduction computers in terms of the program flow mechanism used.
   b) What are the main parameters to design Pipeline? Explain it with example.

3. a) Explain Hazard and their types. What are the Hazards resolving methods?
   b) Why are reservation stations or reorder buffers needed in a super scalar processor?

4. a) Distinguish between scalar RISC and superscalar RISC in terms of instruction issue, pipeline architecture and processor performance.
   b) Differentiate between shared-memory multiprocessors and distributed memory multicomputer.

5. a) Explain the architecture of VLIW processor and its pipeline operations with the help of diagrams.
   b) Why are distributed memory chosen over shared memory in design of multicomputer system?

6. a) Explain the Network partitioning for multicast communication in a message passing network.
   b) Draw and explain 2 state-transition graphs for a cache block using write invalidate snoopy protocols.

7. a) What are the main issues for load balancing in a Multiprocessor system?
   b) What are the Array Processors? Write their main characteristics.

8. a) Describe different multiprocessing control algorithms with suitable example.
   b) Distinguish between spin lock and suspend locks for sole access to a critical section.

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