Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

MEVD-102

M.E./M.Tech., I Semester

Examination, December 2016

CMOS VLSI Design

Time : Three Hours

Maximum Marks :70

Note: i) Answer any five questions. Out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data, if required.

1. a) Explain the second order effects. Draw and explain the sub threshold region.
   b) Draw and explain the CMOS inverter noise margin. Explain its characteristics.

2. a) Draw and explain the accumulation, depletion and inversion function of V_{gs} in MOS capacitor characteristics.
   b) Write down different design rules for layout circuit.

3. a) Give an introductory note on CAD Tools. How this tool is beneficial for designing MOS circuits.
   b) Explain the concept of Power Dissipation. Explain the difference between static and dynamic dissipation. Derive its expressions.

4. a) Explain the designing of ALU subsystem. What is its significances in a circuit? Explain with a suitable example.
   b) Draw and explain the accumulation, depletion and inversion function of V_{gs} in MOS capacitor characteristics.

5. a) Explain the principle of Latch up. Discuss about its physical origin, its triggering and its prevention methods.
   b) Derive an expression for channel resistance in voltage current characteristics of MOS transistor.

6. a) Draw and explain the graphical derivation of CMOS inverter characteristic.
   b) Write an introductory note on VLSI design flow. Explain the concept of design quality.

7. a) Give an introductory note on dynamic register element. Give its applications also.
   b) Discuss the designing of clocked sequential circuits. Explain the principle of two phase clocking. Explain it with a suitable example.

8. a) Is there any difference between the designing of PLA and PAL. Explain.
   b) Explain FPGA. Write its applications. What is the role of FPGA in field designing?

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