Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

MEDC-104

M.E./M.Tech., I Semester

Examination, December 2017

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any Five questions.
ii) All questions carry equal marks.

1. a) List out differences between CMOS and bipolar technologies.
   b) Briefly discuss about the CMOS process enhancements and layout design rules.

2. a) Derive an expression for the rise time, fall time and propagation delay of a CMOS inverter.
   b) Explain the various ways to minimize the static and dynamic power dissipation.

3. a) Explain clocked CMOS logic, Domino logic and n-PCMOS logic.
   b) Explain the basic operation of CMOS logic gate.

4. a) Describe the simulation of circuit interconnects.
   b) What are design rules? Why is metal-metal spacing larger than poly-poly spacing?

5. a) Draw the typical standard cell structure showing regular-power cell and explain it.
   b) Draw the typical architecture of PLA and explain its operation.

6. a) Describe the FPGA block structure and its components.
   b) Explain three main approaches to design for testability in detail.

7. a) Draw the physical layout for the following Boolean expression $Y = \overline{(a+b)} + c + de$
   b) Discuss in detail about the resistive and capacitive delay estimation of a CMOS inverter circuit.

8. Write short note on (any two):
   a) Reprogrammable gate array
   b) logic synthesis
   c) CMOS Chip design
   d) Memory and control strategies.

******

107