UNIT-1

MICROPROCESSOR AND MICROPROCESSOR DEVELOPMENT SYSTEM

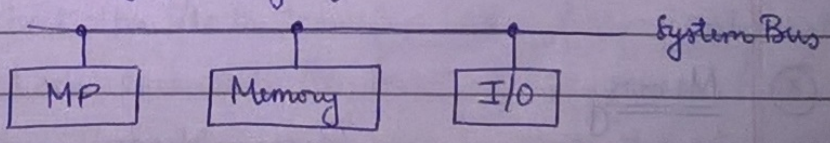
(1) Evolution of Microprocessor -

Chip	Introduction	
4004	1971	4 bit
4040	1971	
8008	1972	8 bit
8080	1974	
8085	1976	
8086	1978	16 bit
8088	1979	
80286	1982	
80386	1984	32 bit
80486	1986	
Pentium	1993	
Pentium Pro	1995	
Pentium 2	1996	
Pentium 3	1998	
Pentium 4	2000	
Core 2 Duo	2006	64 bit
Core i7	2008	
Core i5	2009	
Core i3	2010	

(2) Microprocessor architecture and its operation -

Computer system consists of primary of -

(1) Microprocessor
(2) Memory
(3) Input
(4) Output



Internal logic design of the microprocessor called its architecture. Microprocessor is programmable logic device designed with registers, flip-flops and timing elements.

Microprocessor operations are -
(1) Microprocessor initiated operations
(2) Internal Data operations
(3) Peripheral (or externally) initiated operations.

Microprocessor initiated operations -
→ Memory Read (Read data from memory)
→ Memory Writes (Write data into memory)
→ I/O Read (Accept data to output device)
→ I/O Writes (Sends data to output device)

Internal Data Operations -
→ Store 8-bit data
→ Performed arithmetic and logical operations
→ Test for conditions
→ Sequence the execution of instructions
→ Store data temporarily during execution in the defined R/W memory locations called the stack.

Peripheral or Externally Initiated operations -
→ RESET (all internal operations are suspended and program counter is cleared)
→ Interrupt (execute "service routine" (emergency) instructions)
→ READY (low → MP enters into wait state)
→ HOLD (MP relinquishes control buses and allow external peripheral to use)

③ Memory -

(i) Primary Memory
- RAM
  - Magnetic core
  - Semiconductor
    - Static
    - Dynamic
- ROM
  - Bipolar
    - Mask ROM
    - PROM
  - MOS
    - Mask ROM
    - PROM
    - EPROM AND EEPROM

(ii) Secondary Memory.

④ Input/Output (I/O) –

Two different methods by which MPU identifies and communicates with I/O devices –

(1) Direct I/O (Peripheral)

(2) Memory-mapped I/O

Direct I/O (Peripheral)	Memory-mapped I/O
→ 8 address lines to send the address of I/O device	→ 16 address lines to send the address of I/O device.
→ Can identify $2^8 = 256$ input and output devices	→ Can identify $2^{16} = 64K$ input and output devices
→ I/O Read ($\overline{IOR}$) & I/O Write ($\overline{IOW}$) control signals used to enable the device	→ $\overline{MEMR}$ and $\overline{MEMW}$ control signals used to enable the device.

⑤ Data Transfer Schemes –

Parallel Data transfer:

(1) Program controlled I/O or ~~interrupt driven I/O~~ polling control ~~I/O~~

(2) Interrupt program controlled I/O or interrupt driven I/O

(3) Hardware controlled I/O or DMA transfer

Serial Data Transfer:

(4) ~~Hardware~~ I/O controlled by handshake signals.

(5) I/O controlled by ready signals.

Program controlled I/O or polling control –

Data transfer is completely under the control of the microprocessor program. This means that the data transfer takes place only when an I/O transfer instructions executed. In most of the cases it is necessary to check whether the device is ready for data transfer or not. To check this, microprocessor polls the status bit associated with the I/O device.

Interrupt driven I/O -

When I/O data transfer is initiated by the external I/O device (i.e. device sends an interrupt signal to the microprocessor), the microprocessor stops the execution of the program and transfers the program control to an interrupt service routine. The interrupt service routine performs the data transfer. After the data transfer, it returns control to the main program at the point it was interrupted.

Hardware controlled I/O - (increase the speed of data transfer)

In response of HOLD signal (sent by DMA controller to initiate data transfer), microprocessor releases its data, address and control buses to the DMA controller.

I/O control by handshake signals -

The status of handshaking signals are checked between the microprocessor and an I/O device and when both are ready, the actual data is transferred.

I/O control by READY signal - (between slower I/O device and microprocessor)

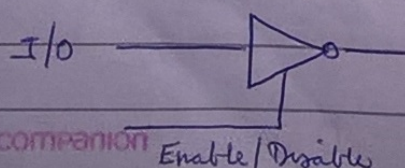
If READY pin is high, the I/O device is ready for data transfer otherwise microprocessor enters WAIT state(s). These WAIT states elongate the read/write cycle timings and prepare ~~8085~~ microprocessor to communicate with slower I/O devices.

⑥ Interfacing Devices -

Interfacing of the processor with one or more peripheral devices for the purpose of communication with the environment.

Tri-state device -

It has three states (logic 1, logic 0 and high impedance)



Decoder - It is a logic circuit that identifies each combination of the signals present at its input.

Latch - A latch is a D-flip flop, used commonly to interface output device.

→ Gates, shift registers and buffers are also a interfacing devices.

⑦ Architectural Advancements of microprocessors -

Memory Management, Multitasking, pipelining, multiprocessing, and virtual memory and cache memory are main architectural ~~advent~~ advancements of microprocessors.

⑧ Microprocessor development systems -

It is a tool that allows the designer to develop, debug and integrate error-free application software in microprocessor system

It falls on two categories -

(1) Non-universal systems (Intel, Motorola, RCA)

(2) Universal systems (Hewlett-Packard, Tektronix)

Typical microprocessor - Intel ~~8085~~ MP & Motorola MP

Microprocessor are being extensively used in wide variety of applications. Typical application includes dedicated controllers, personal workstations, and real-time robotics control.