

UNIT - IV

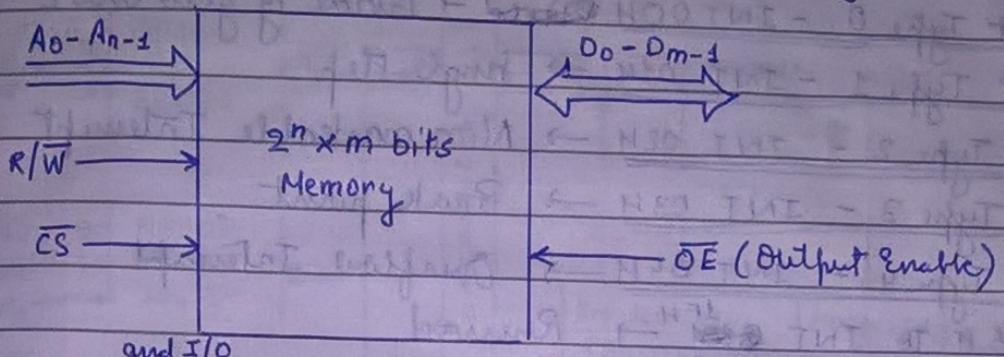
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I/O and Memory Interfacing using 8085/8086

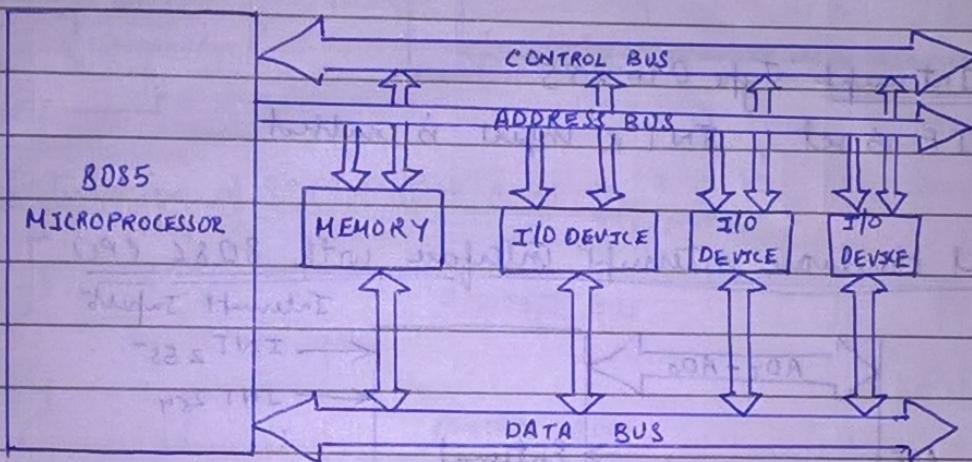
I/O and Memory Interfacing using 8085/8086 -

① Memory Interfacing -

→ Memory Organization → Memory map, Address decoding



→ Memory Interfacing to microprocessor



② Interrupts of 8085 microprocessor

INTR → Interrupt Request

RST 5.5 - 002CH address

maskable interrupt

RST 6.5 - 0034H address

RST 7.5 - 003CH address

TRAP - Non-maskable interrupt (Used for power failure or emergency shut down)

0024H address

→ RIM Instruction - (Read Interrupt Mask) → load accumulator with 8-bit

SID	P7.5	P6.5	P5.5	IE	M7.5	M6.5	M5.5
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

→ SIM Instruction = (set Interrupt Mask) → load accumulator with

SOD	SDE	XXX	R7.5	MSE	M7.5	M6.5	M5.5
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

MSE → Mask Set Enable, SDE → Serial Data Enable.

③ Interrupts of 8086 microprocessor -

(1) Software Interrupts - 256 Interrupts from INT 00H to INT FFH

Interrupt Type 0 - INT 00H → Divide by zero error

Interrupt Type 1 - INT 01H → Single step

Interrupt Type 2 - INT 02H → Non maskable Interrupt

Interrupt Type 3 - INT 03H → Break point

Interrupt Type 4 - INT 04H → Overflow Interrupt

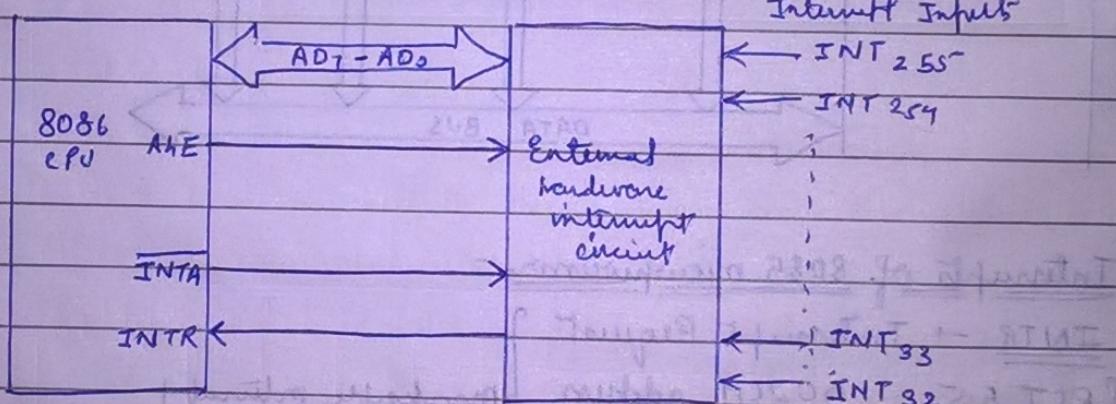
INT 05H to INT 0FH → Reserved

INT 0BH to INT FFH → User defined

(2) INTR Interrupt → Type 0 to 255

When IF is set, INTR input is enabled

(3) External Hardware interrupt interface with 8086 CPU -



(4) Priority of 8086 Interrupts -

→ Reset

→ Internal Interrupts

→ Software Interrupts

→ Nonmaskable Interrupts

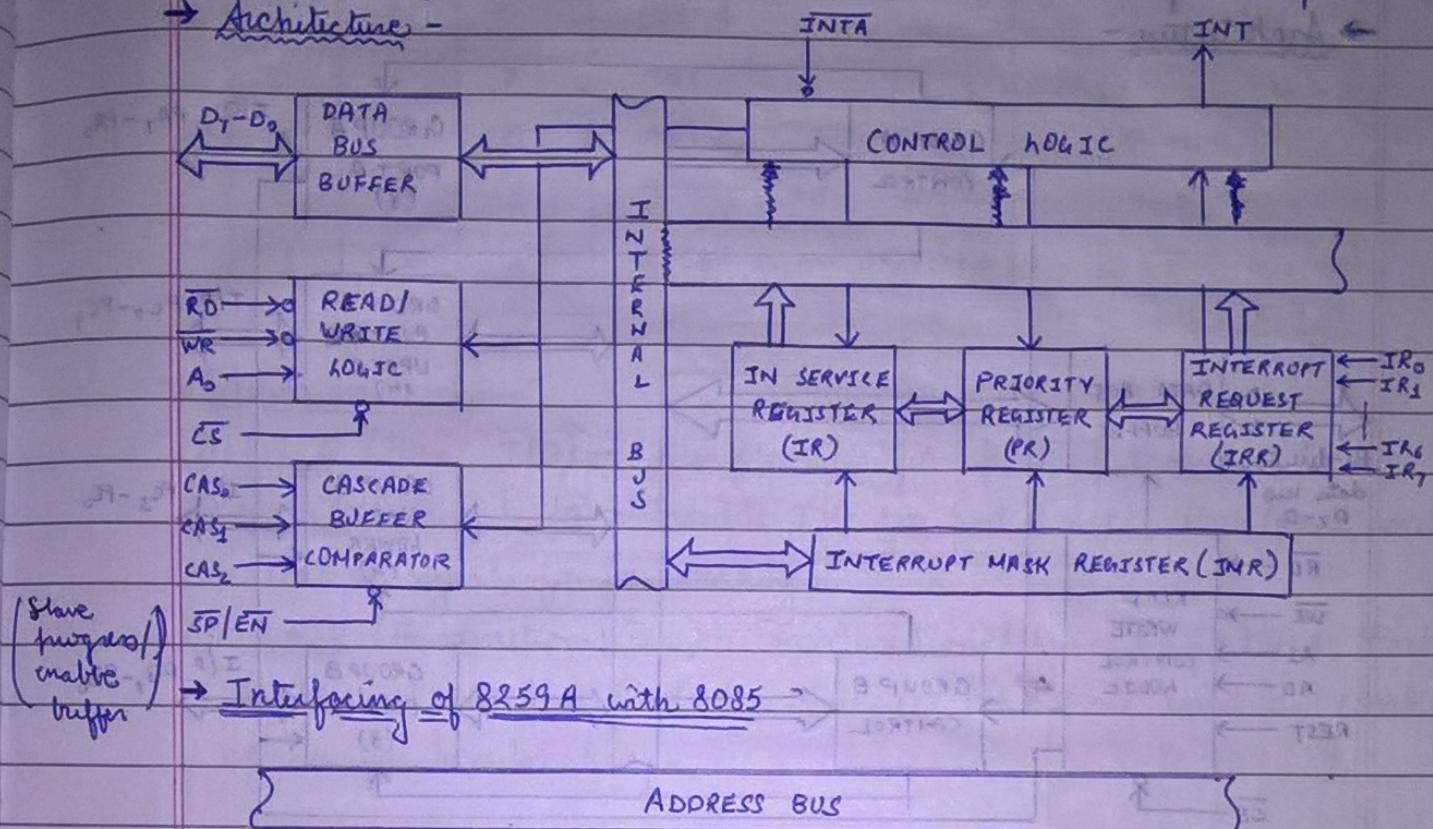
→ Hardware Interrupts

(5) Interrupt Instructions of 8086 - CLI (Clear Interrupt Instruction)

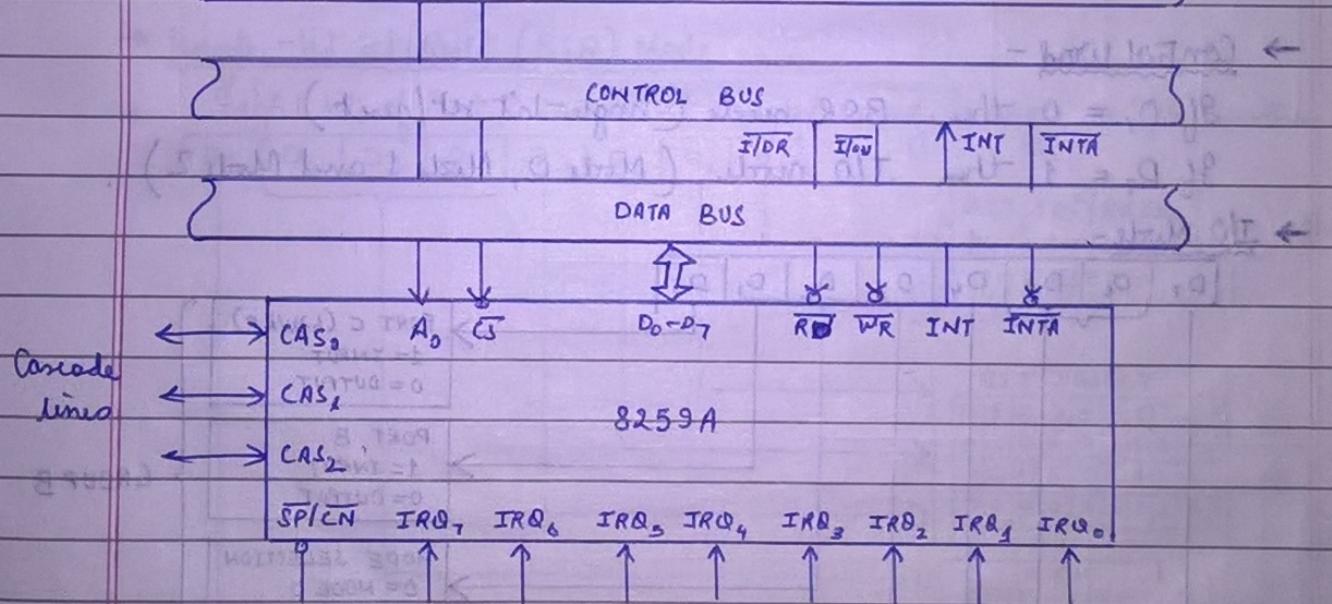
STI (Set Interrupt flag), IRET (Interrupt Return), INTO (Interrupt overflow), HLT, WAIT

④ 8259A Programmable Interrupt Controller (PIC) - [28 pins]

→ Architecture -



→ Interfacing of 8259A with 8085 -



Two types of command words -

Initial Command words (ICWs) and Operation command words (OCWs)

↳ four types (ICW_1 , ICW_2 , ICW_3 & ICW_4)
↳ three types (OCW_1 , OCW_2 and OCW_3)

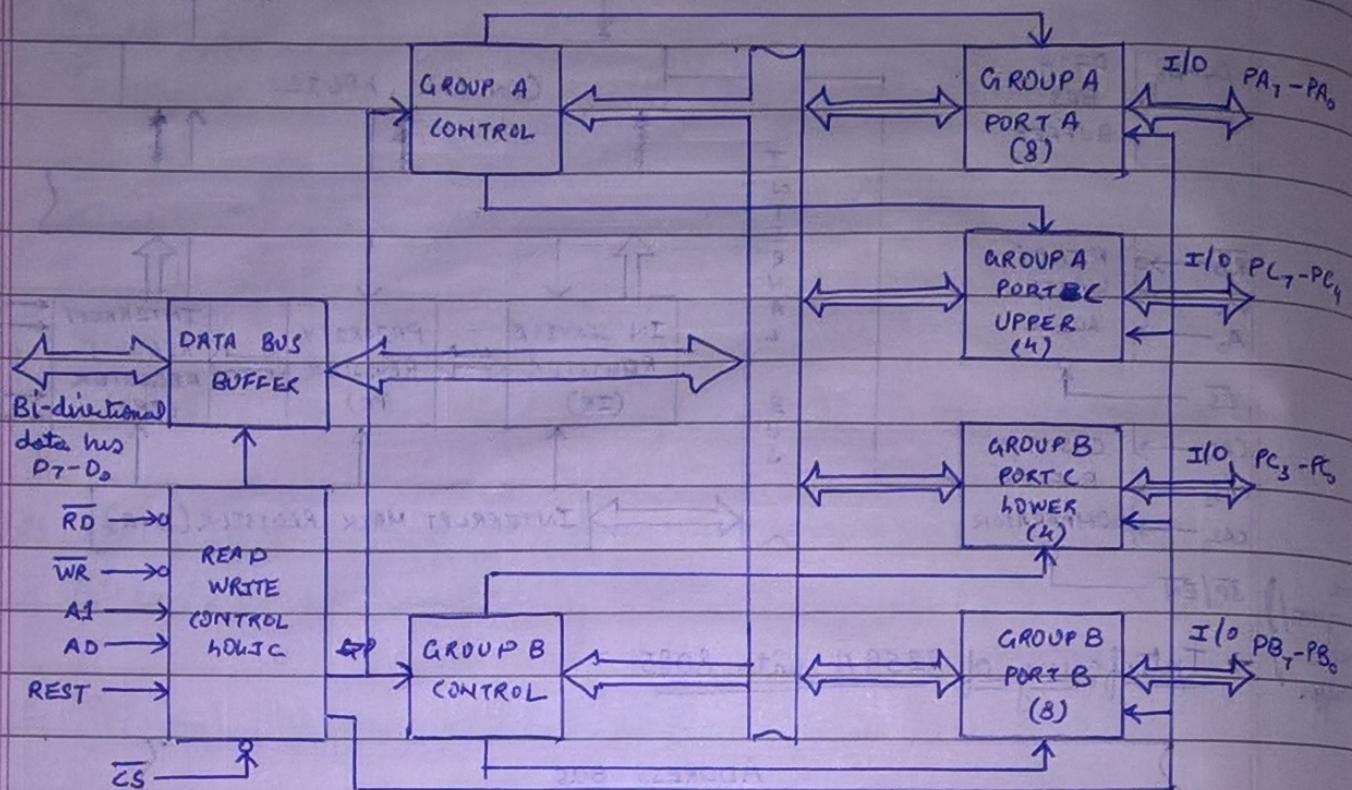
always send

in cascade mode

Special operations

⑤ 8255A Programmable Peripheral Interface (PPI) - [10 pins]

→ Architecture-

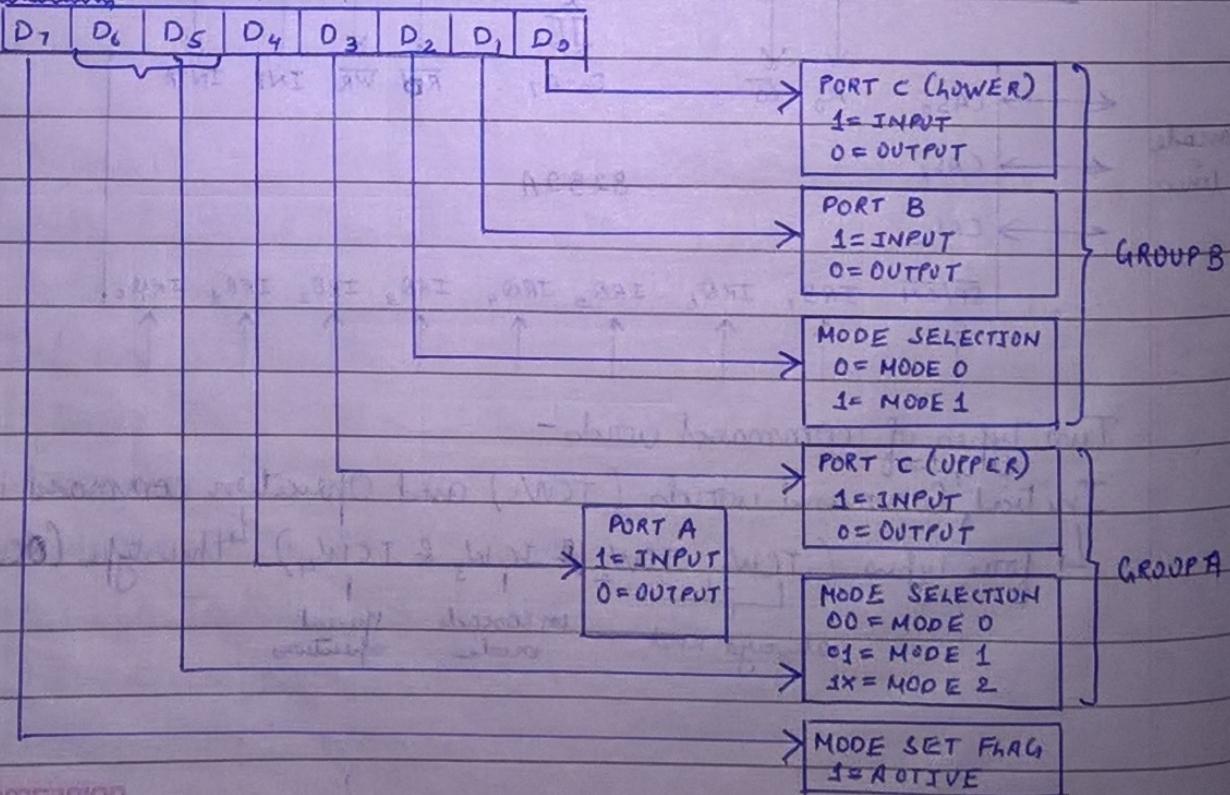


→ Control Word -

If D7 = 0 then BSR mode (single-bit set/reset)

If D7 = 1 then I/O mode (Mode 0, Mode 1 and Mode 2).

→ I/O Modes -



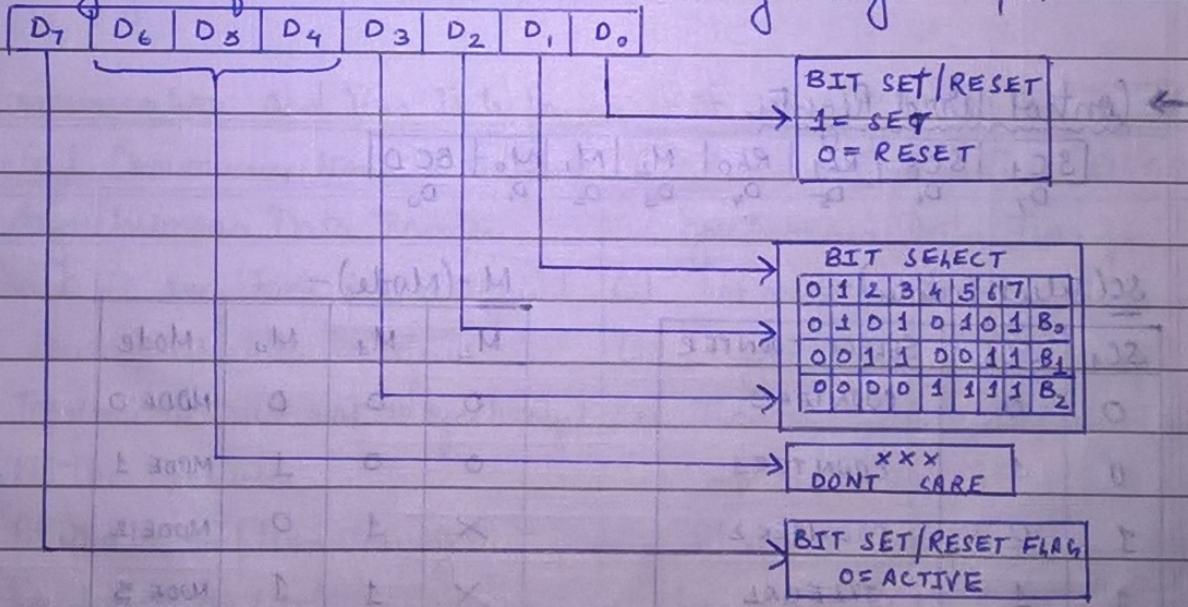
\bar{CS}	A_3	A_2	SELECTION
0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	CONTROL WORD
1	X	X	8255A IS NOT SELECTED

→ Operation modes -

- ① Mode 0 (Banc I/O) - Simple I/O for port A, B and C.
 - ② Mode 1 (Strobed I/O) - Simple I/O for port A and B, Port C are used as control signals for handshaking.
 - ③ Mode 2 (Bi-directional Bus) - Bi-directional bus for port A & B. Port C can be used in either Mode 1 or Mode 0. Port C are used as control signals for handshaking.

→ Single-bit Set/Reset (BSR) Mode

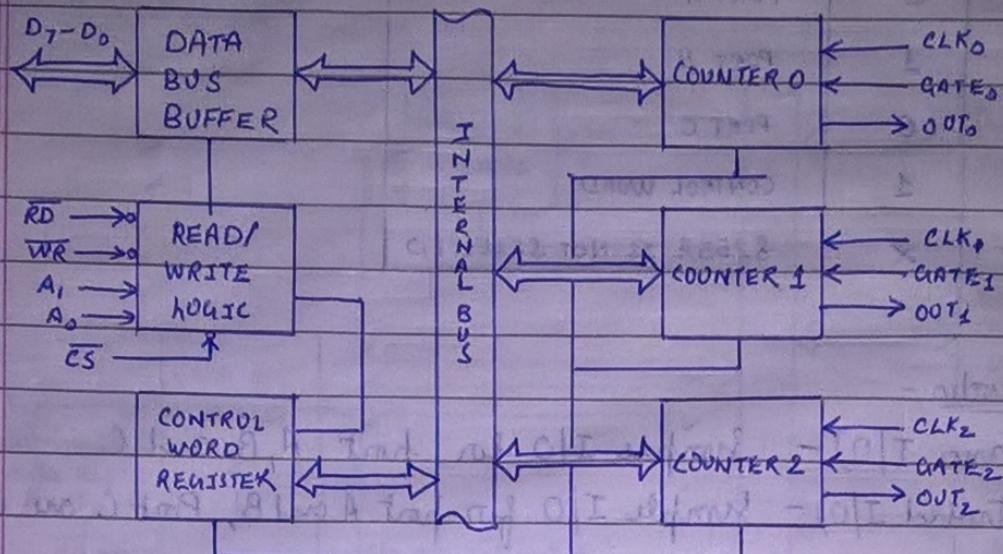
Eight bits of Port C can be set or reset using a single output instruction.



→ Applications of PPI -

Putting on LED as specified by the designer, Generating a square wave at port A, Interfacing A/D Converter, Keyboard operation, Sequential switching of lights, Traffic light control.

⑥ 8253 Programmable Counter / Interval Timer - [24 pins]



CS	A ₁	A ₀	SELECTION
0	0	0	COUNTER 0
0	0	1	COUNTER 1
0	1	0	COUNTER 2
0	1	1	NO OPERATION
1	x	x	8253 IS NOT SELECTED

→ Control Word Register -

SC ₁	SC ₀	R _{L1}	R _{H0}	M ₂	M ₁	M ₀	BCD
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

SC (Select Counter) -

SC ₁	SC ₀	SELECT COUNTER
0	0	COUNTER 0
0	1	COUNTER 1
1	0	COUNTER 2
1	1	ILLEGAL

M - (Mode) -

M ₂	M ₁	M ₀	Mode
0	0	0	MODE 0
0	0	1	MODE 1
X	1	0	MODE 2
X	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

BCD -

0 → Binary Counter (16 bits)

1 → Binary Coded Decimal (BCD) counter (4 decades)

RL (Read / Load) -

RL ₁	RL ₀	READ / LOAD
0	0	Counter latching operation
0	1	Read / Load least significant byte only
1	0	Read / Load most significant byte only
1	1	Read / Load least significant byte first, then most significant byte

MODE 0 - Interrupt on Terminal Count (GATE = 1)

MODE 1 - Programmable one shot (GATE = $\frac{1}{2}$ half + 1 & 2nd half \rightarrow 0)

MODE 2 - Rate Generator (OUT_{PUT} = 1 for (N-1) pulses)

MODE 3 - Square-wave Generator (if N is even, OUT = $\frac{1}{2}$ half + $\frac{1}{2}$ 2nd half \rightarrow 0)

If N is even, high for N/2 pulses and low for next N/2 clock pulses.

If N is odd, output high for N+1 pulses and low for remaining clock pulses.

MODE 4 - Software Triggered Shutter (GATE = 1, OUT = 1 for N then one low pulse and then again OUT = 1 for N and so on).

MODE 5 - Hardware Triggered Shutter (Whenever GATE = 1 then it starts counting back like MODE 4)

Communication and Bus Interfacing with 8085/8086 Microcontroller -

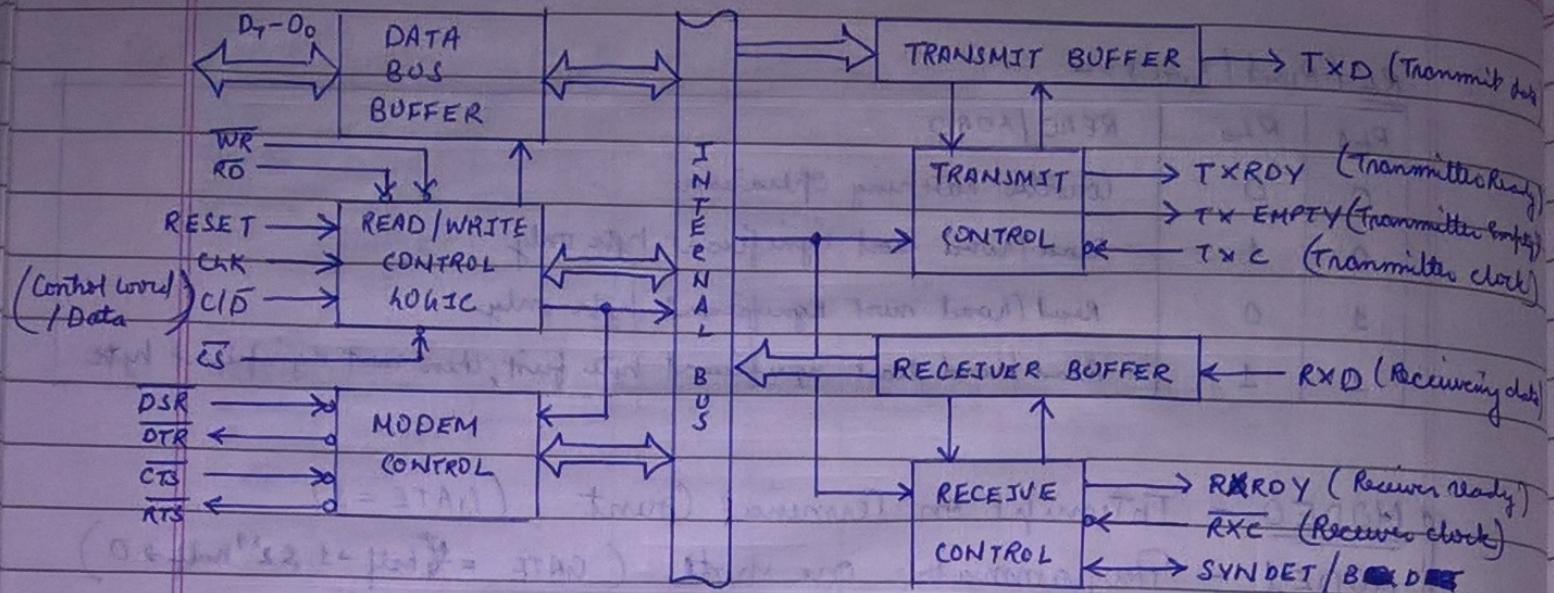
⑦ Serial Communication Interface 8251 - [28 pins] (USART)

Asynchronous Data Transfer

- (1) Start bit and Stop bit is required
- (2) low-speed data transfer
- (3) Transmitter need not be synchronized with the receiver
- (4) It can be implemented by hardware and software
- (5) Data can be sent one character at a time

Synchronous Data Transfer

- (1) No need; Block header is used.
- (2) High speed data transfer
- (3) Transmitter is synchronized with the receiver.
- (4) It can be implemented by hardware only.
- (5) Used for transferring large amounts of data.

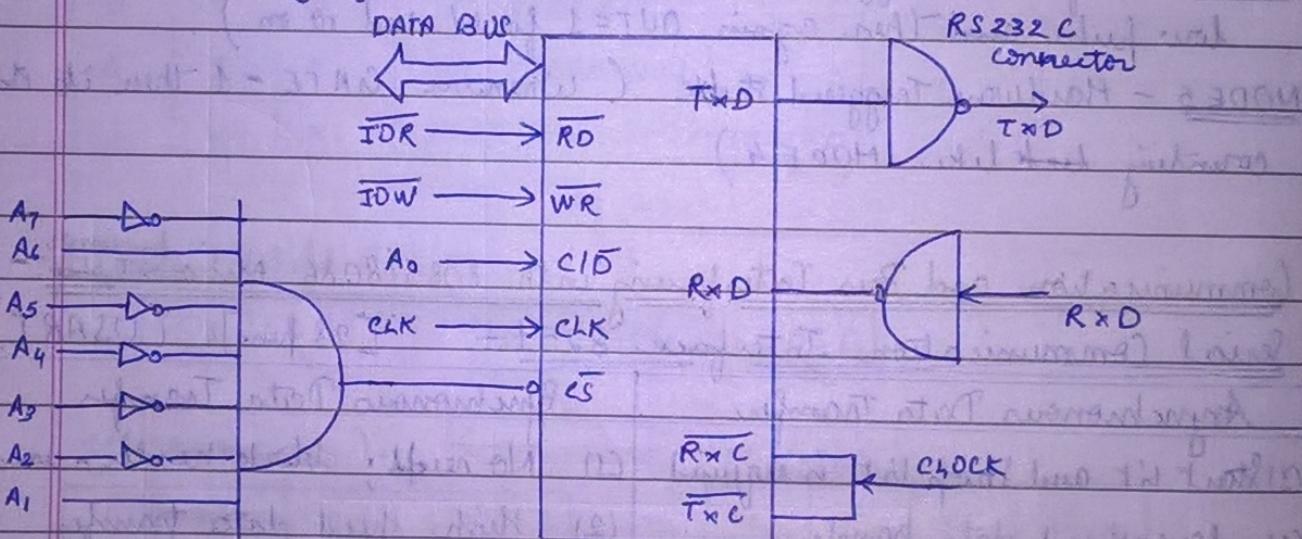


DSR → Data Set Ready, DTR → Data Terminal Ready.

CTS → Clear to send, RTS → Request to send.

SYNDET/BOD → Synchronous Detect / Break Detect.

Interfacing of 8251 with microprocessor -



→ Two function types -

(1) Mode Instruction Control Word -

	D ₇	S ₂	S ₁	EP	PEN	L ₂	L ₁	B ₂	B ₁	D ₀
Stop bit selection		S ₂	S ₁							
Invalid	0	0	1-Even parity	1-Parity enable		0	0	5 bits	0	0
1 bit	0	1	0-Odd parity	0-disable		0	1	6 bits	0	1
1½ bit	1	0				1	0	7 bits	1	0
2 bits	1	1				1	1	8 bits	1	1
										Band Rate

(2) Command Instruction words -

D ₇	EH	IR	RTS	ER	SBRK	RXE	DTR	TXEN	D ₀
----------------	----	----	-----	----	------	-----	-----	------	----------------

TXEN → Transmit Enable → 1, Disable → 0.

DTR → Data Terminal Read, $\overline{DTR} = 0$.

RXE → Receive Enable → 1, Disable → 0

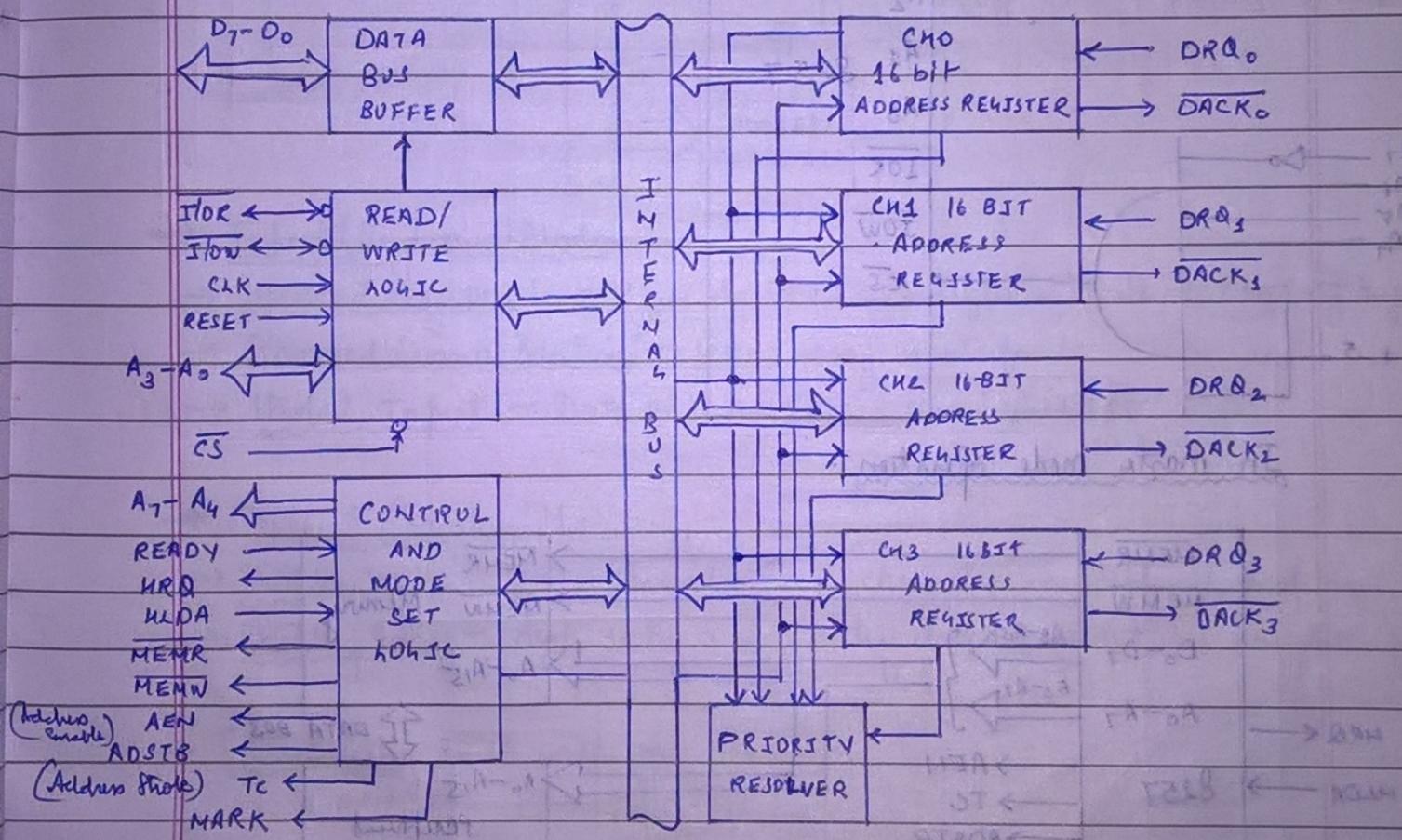
SBRK → Send Break Character.

ER → Request Error flags

RTS → Request to send

IR → Internal Reset

EH → Hunt for sync character.

(8) Direct Memory Access (DMA) Controller 8257 - [40 Pins]

Terminal Count Register (TC) → (16 bit register)

Store no. of bytes which will be transferred through a DMA channel.

Mode Set Register -

Auto load	TC Stop	Extended WR	Rotate Priority	EHC13	EHC12	EHC11	EHC10
D ₇	D ₆	D ₅ DNA	D ₄	D ₃	D ₂	D ₁	D ₀

EHC_x (enable channel - x)

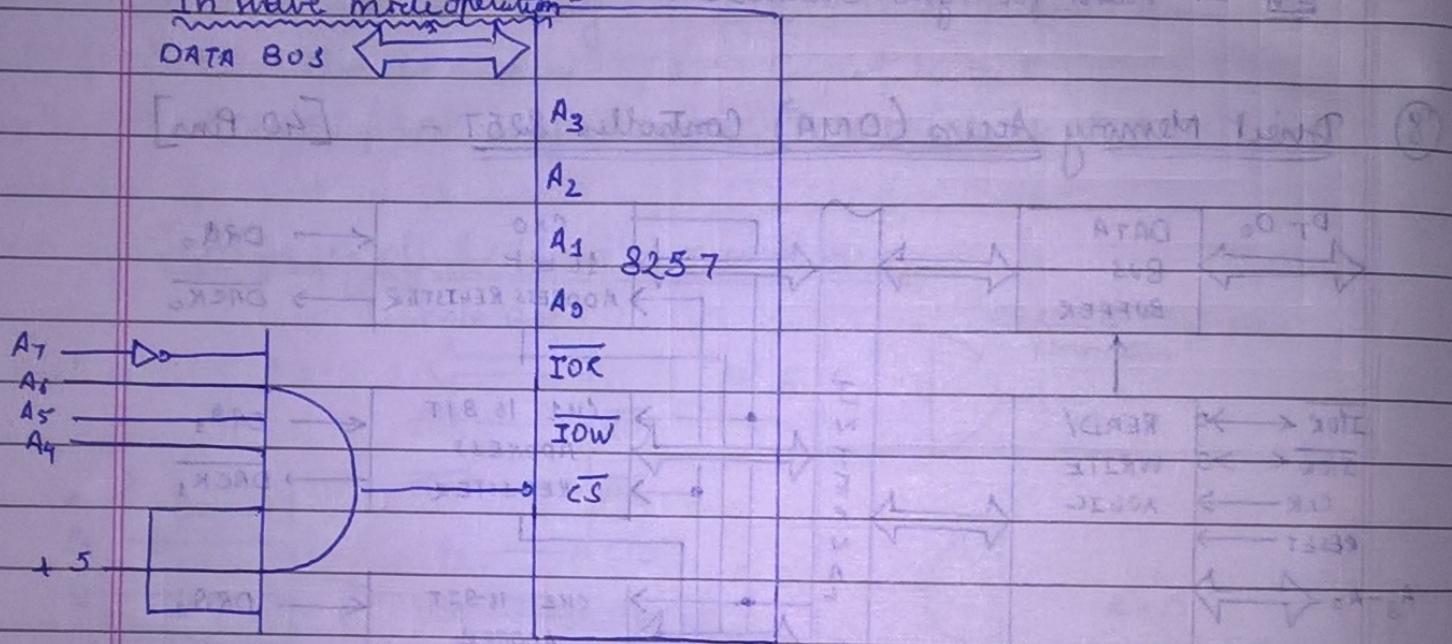
Status Register -

0	0	0	Update Flag	TCSC0	TCSC1	TCSC2	TCSC3
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

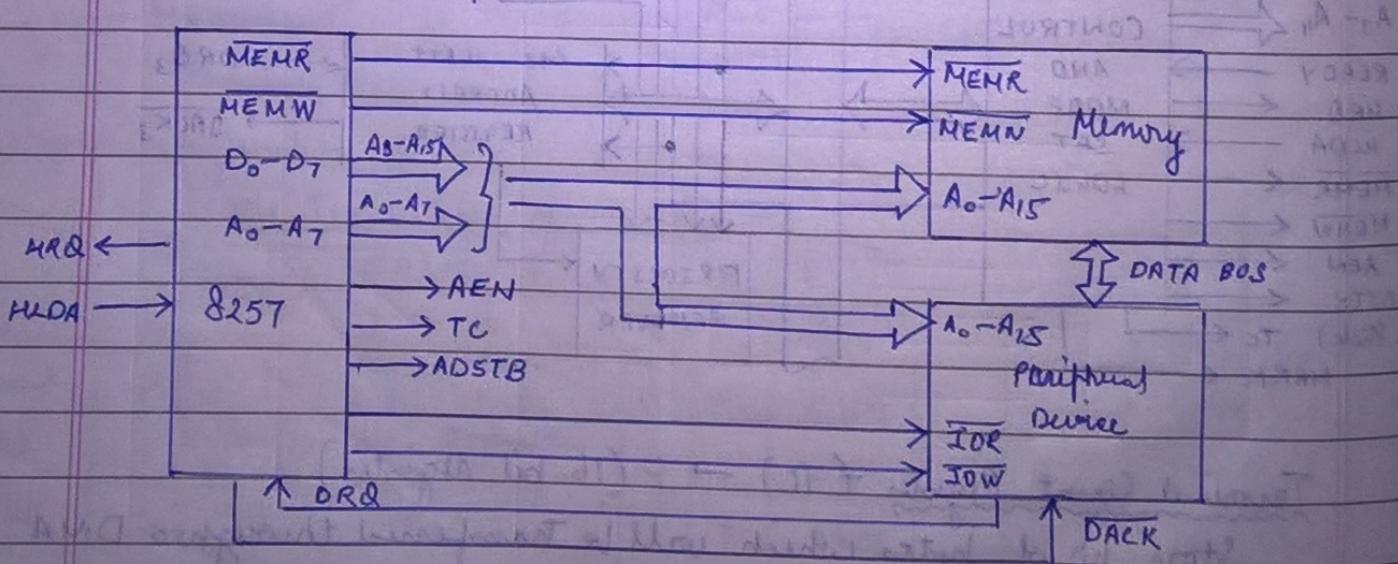
TCSC_x (TC Status of Channel x)

→ Interfacing of 8257 with 8085 microprocessor -

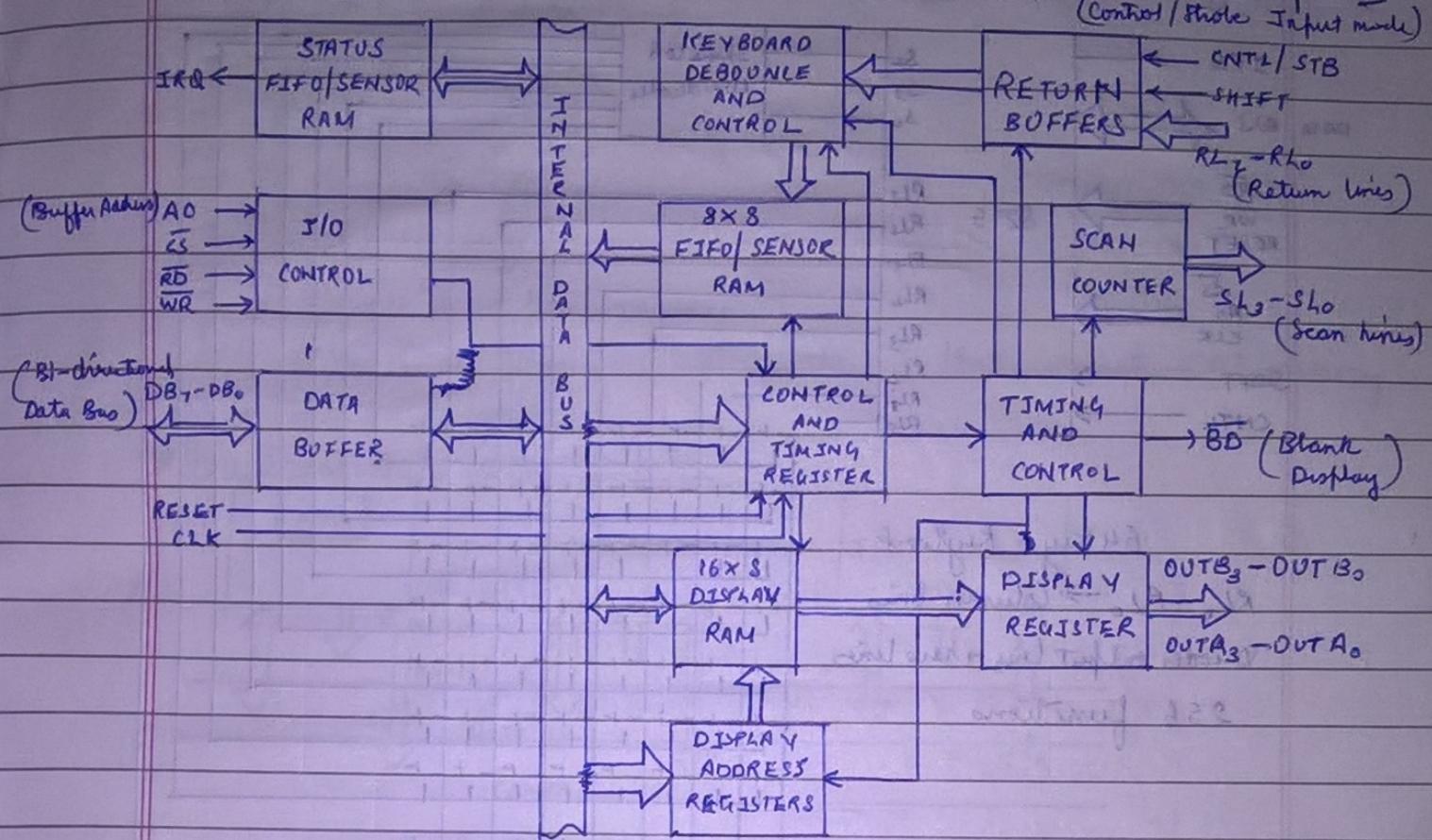
In slave mode operation -



In master mode operation -



⑨ 8279 - Programmable Keyboard and Display I/O Interface - [40 pins]



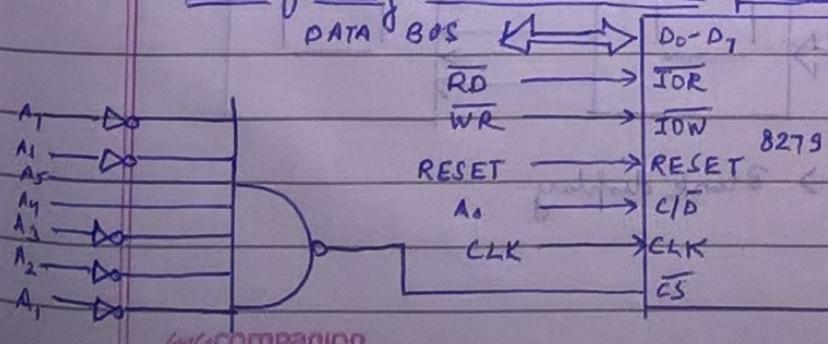
→ Input (Keyboard) Modes

- Scanned Keyboard → Encode (8x8 key keyboard) & decode (4x8 key keyboard)
- Scanned Sensor Matrix → sensor array is interfaced
- Shaded Input → Data on return lines stored in FIFO

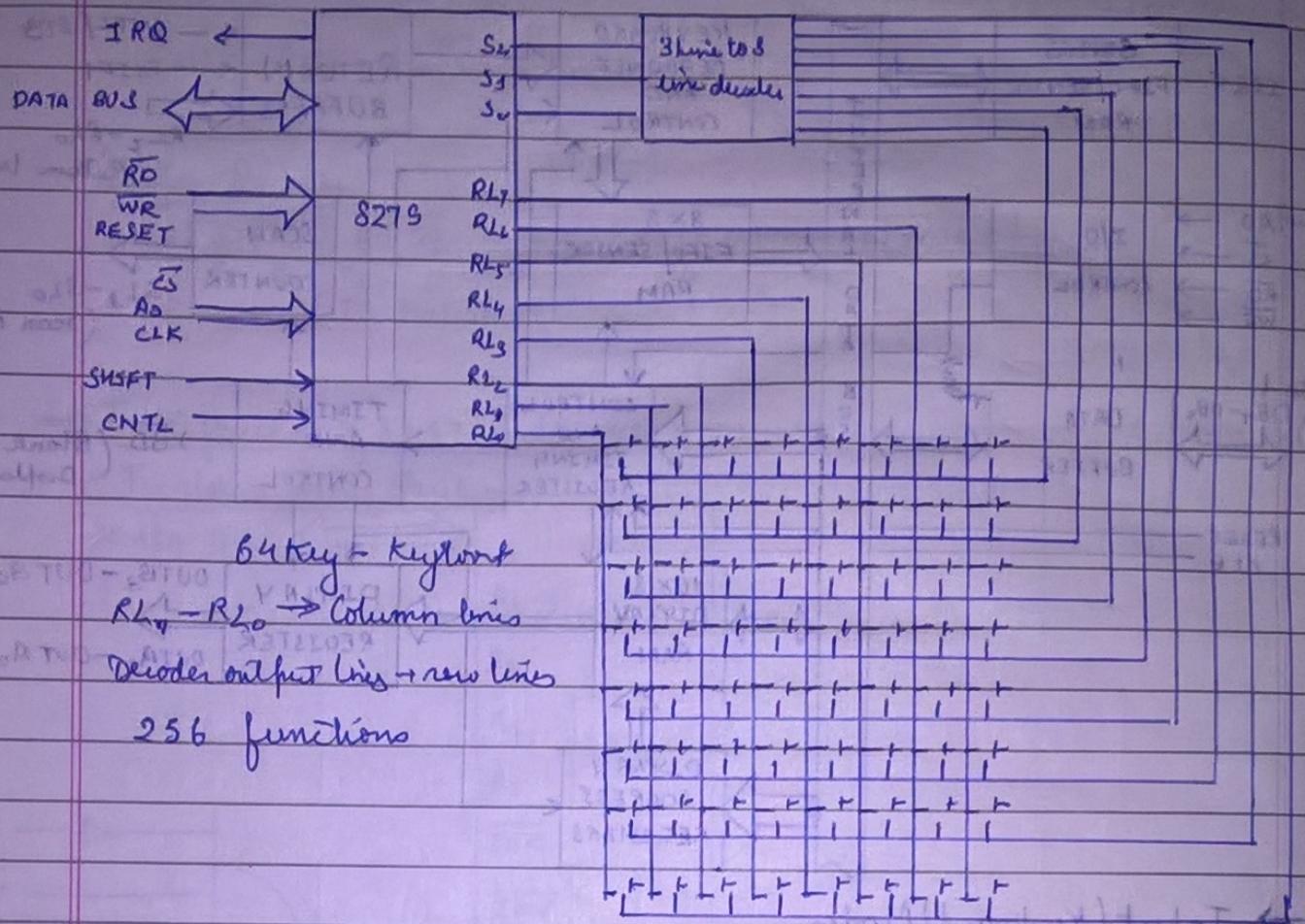
→ Output (Display) Modes

- Display Scan - 8279 provide 8 or 16 characters multiplexed display
- Display Entry - High entry a left entry display format are executable for 8279

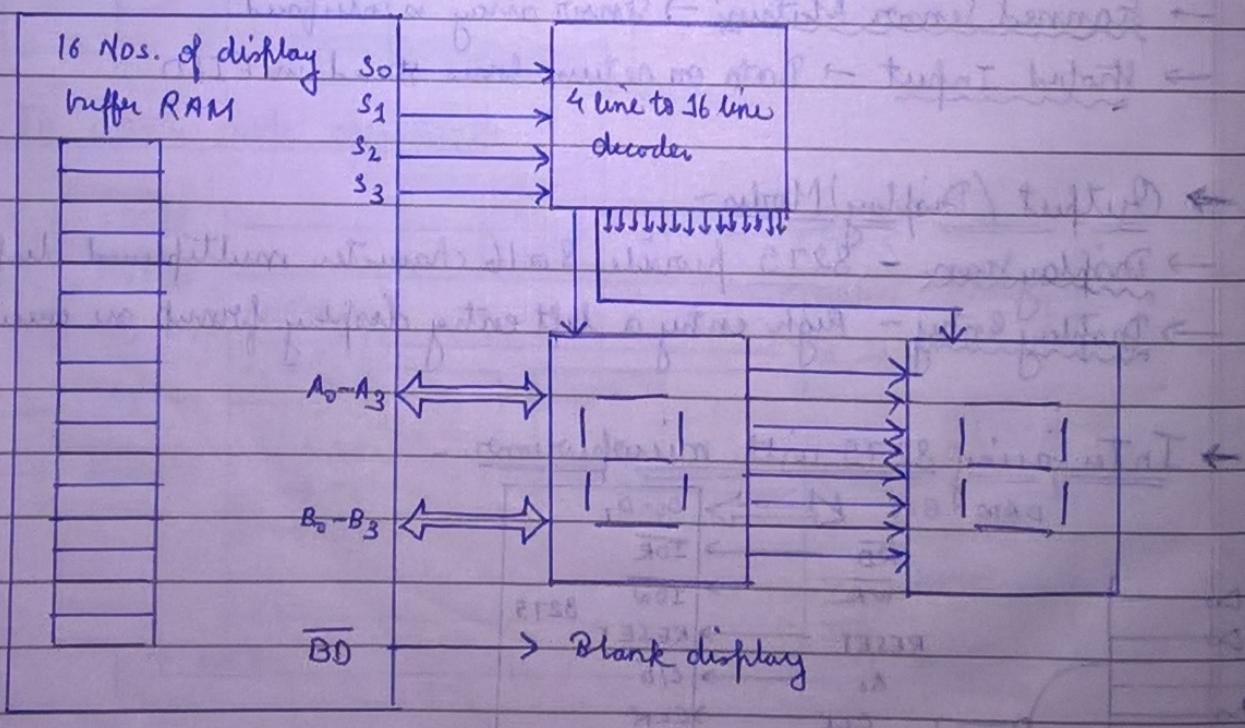
→ Interfacing 8279 with microprocessor



→ Keyboard Interface of 8279 -



→ Sixteen digit display interface with 8279



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Bus Interface -

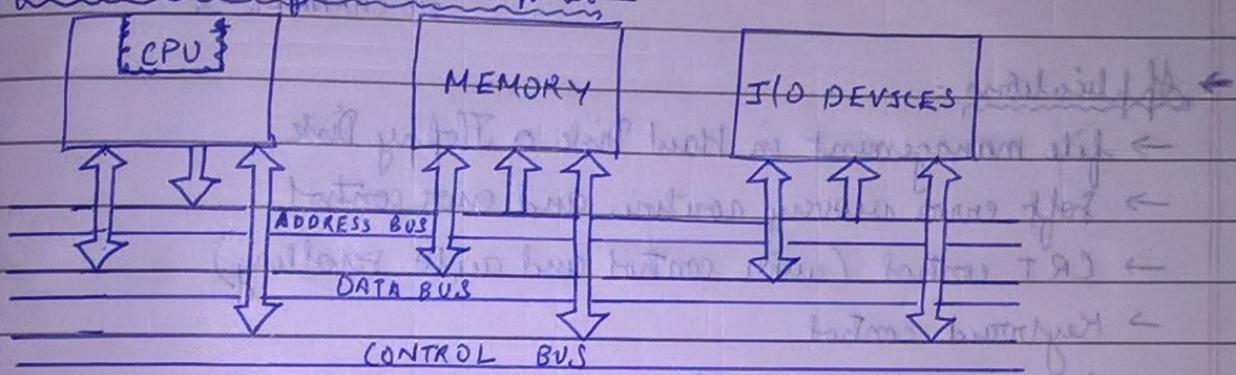
Different types of data transfer -

- Memory devices to CPU
- CPU to memory devices
- I/O devices to CPU
- CPU to I/O devices

→ I/O devices to or from memory.

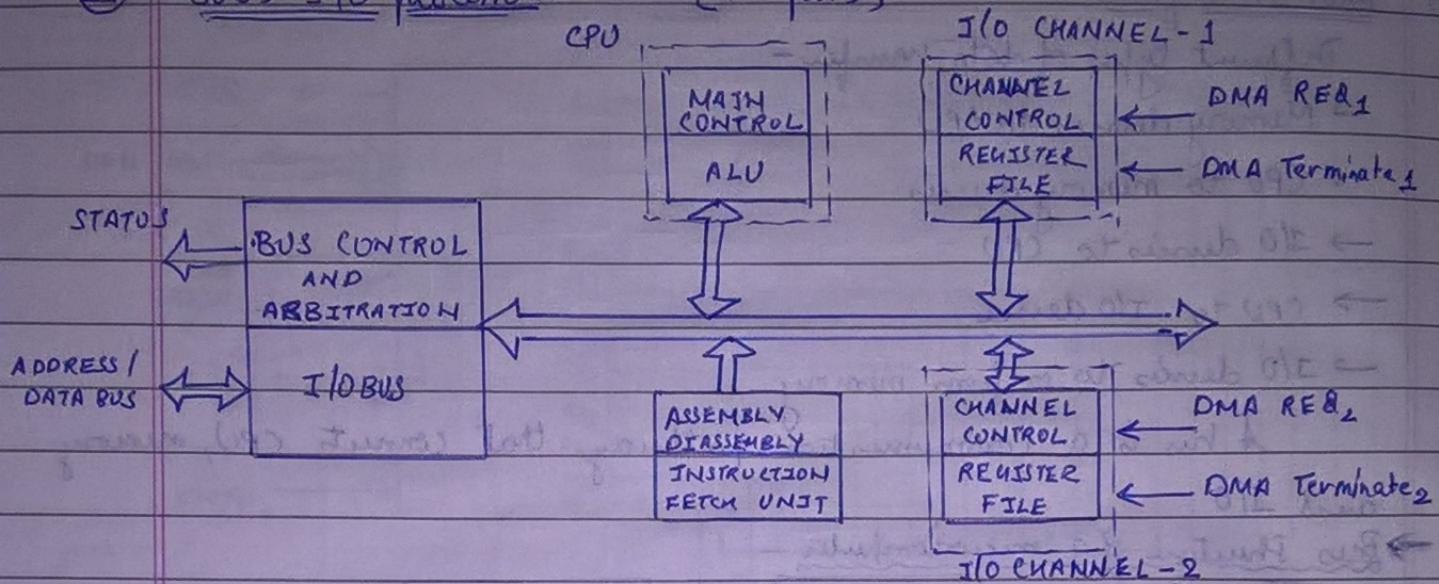
It has is a communication pathway that connects CPU, memory and I/O.

→ Bus Structure of a microcomputer -



- ISA (Industry Standard Architecture) → by IBM in 1979
- EISA (Extended ISA) → by HP, AST, Compaq in 1987
- MCA (Micro Channel Architecture) → by IBM in 1987
- VESA (Video electronic Standard association) → developed in 1990
- PCI (Peripheral Component Interconnect) → by Intel in 1993
- AHP (Accelerated Graphics port) → by Intel in 1998
- USB (Universal Serial Bus) → by group of companies in mid 1990's
- Parallel Printer Interface → by IBM in 1981
- RS-232C → by EIA in 1960's
- IEEE -488 Bus → General Purpose Interface Bus (GPIB) by HP

⑪ 8089 I/O processor - [40 pins]



→ Applications -

- file management in Hard Disk & Floppy Disk
 - soft error recovery routine and error control
 - CRT control (cursor control and auto scrolling)
 - Keyboard control
 - Communication control
 - General I/O applications