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Roll No.

EX-8402

B. E. (Eighth Semester) EXAMINATION, June, 2012 (Electrical & Electronics Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN-II

(Elective-IV)

(EX-8402)

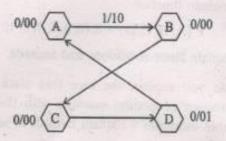
Time: Three Hours

Maximum Marks: 100

Minimum Pass Marks: 35

Note: Attempt any five questions. All questions carry equal marks.

- (a) Explain the parity bit generator with the help of state table and state diagram.
 - (b) Convert the following Mealy machine to Moore machine. 10



 A long sequence of pulses enters a two-ouput synchronous sequential circuit, which is required to produce an output P. T. O.

- pulse Z = 1 whenever the sequence 1110 occurs.

 Overlapping sequences are accepted: 20
- (i) Draw a state diagram.
- (ii) Select an assignment and show the excitation.
- (iii) Write down the excitation function of SR flip-flops and draw logic diagram
- Using VHDL describe a binary-to-decimal converter that has a four-bit input vector and the output in the BCD representation.
- 4. What do you understand by essential hazards? Show that the following machine has essential hazard: 20

Y ₁ Y ₂ Y ₃	X	
	0	1
010	110	010
110	110	111
111	101	111
101	101	111

 (a) Find a circuit that has no hazards and implements the Boolean function:

$$F(A, B, C, D) = \Sigma(0, 3, 6, 7, 8, 10)$$

10

20

- (b) Explain Race conditions and hazards.
- 6. How do you explain the race free state assignment of asynchronous sequential machine with the help of three flow table examples? Explain hazards in sequential circuit or machine.
- (a) What is the fundamental concept of hardware/ firmware algorithm? Explain.
 - (b) Draw the ASM chart of sequence recognizer to recognize the input sequence of pair $X_1 X_2 = 01, 01, 11, 00.$
- 8. Explain in short (any three) of the following:
 - (i) PLA (iii) GAL
 - (ii) XILINX (iv) VHDI