Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal

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MEDC-104

M.E./M.Tech. (First Semester)

EXAMINATION, Dec 2010

(Grading/Non-Grading)

VLSI DESIGN

Time: Three Hours

Maximum Marks: GS:70

Note: Attempt any five questions.

1. (a) Obtain the nMOS enhancement transistor threshold voltage equation.
   (b) Calculate native threshold voltage for a n-transistor at 300^0K for a process with a Si substrate with $N_A = 1.5 \times 10^{16}$ cm^{-3}, a SiO_2 gate oxide with thickness 200 Å. { Assume φ_{ms} (work function) = - 0.9, $\varphi_{fc} = 0$ }.

2. (a) What are the various processes of fabrication of CMOS? Explain any *one* of them with neat diagram.
   (b) Explain the following:
      i. Oxidation
      ii. Ion implantation in brief

3. (a) Explain various power dissipations in a CMOS circuit.
   (b) What is Transistor Sizing? Explain with examples.

4. (a) Explain noise margin of an invertor circuit with suitable diagram and expression.
   (b) Explain what is "yield" in the manufacture of VLSI structures. How do the various parameters affect it?

5. (a) Draw the architecture of field programmable gate arrays (FPGAs) and explain the following:
      i. Programmable interconnects
      ii. IOBs
      iii. CLBs
   (b) Give the applications of FPGAs.

6. (a) Explain the following:
      i. Pass Transistor Logic
      ii. Dynamic Logic
      iii. Pseudo-nMOS Logic

7. (a) Explain the data path operations in CMOS sub-system design.
   (b) Design a 32 bit parallel adder optimized for speed, single cycle operation and regularity of layout.

8. Write short notes on any *three* of the following:
   i. MOS capacitor
   ii. Sea of gates
   iii. FSM
   iv. Network Isomorphism
   v. NAND and NOR logic gate design using CMOS