*Total No. of Questions :8]* *[Total No. of Printed Pages :2*

 **Roll No.....**

# MEVD-103

## M.E./M.Tech. I Semester

Examination, June 2017

## Advanced Logic Design

***Time : Three Hours***

***Maximum Marks : 70***

***Note:*** i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) How does a programmable logic device differ from a fixed logic device? What are advantages of PLD. 7
   b) What is a hardware description language? What are the requirements of a good HDL? Briefly explain the features of Verilog. 7

2. a) With the help of relevant circuit diagram briefly explain the operation of CMOS NAND and NOR gates. 7
   b) With suitable examples explain the process of double pushing in digital circuits. 7



3. a) Explain data types and operators of Verilog HDL. 7
   b) Write a short note on Verilog behavioral model. 7

4. a) Differentiate Gate level and Data flow modeling of Verilog HDL. 7





   b) Write an HDL gate level description of the BCD to excess-3 converter. 7



5. a) What do you understand by finite state machine? Explain in detail. 7
   b) Write a short note on Model sim. 7

6. a) Differentiate combinational and sequential digital circuits. 7
   b) Using manual method, obtain the logic diagram of a three bit counter that counts in the sequence 0, 2, 4, 6, 0, ... 7

7. a) Define the terms Fan-in and Fan-out. 7
   b) Draw and explain D-flip flop and write its characteristics table and equation. 7

8. Write short notes on any two: 14
   i) Karnaugh maps
   ii) Verilog behavioral model
   iii) Shift registers
   iv) Metastability



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