

Roll No

CS/IT-402

B.E. IV Semester

Examination, December 2016

Computer System Organization

Time : Three Hours

Maximum Marks : 70

- Note:* i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.
ii) All parts of each question are to be attempted at one place.
iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.
iv) Except numericals, Derivation, Design and Drawing etc.

Unit - I

1. a) Write the functions of MAR and MDR registers of CPU.
b) Write the names of flags found in 8085 microprocessor.
c) Draw Von-Neumann architecture of computer.
d) What do you understand by micro-operation? List types of micro-operations and explain them.

OR

Write and explain various addressing modes of basic computer.

Unit - II

2. a) Name three ways in which we can represent signed binary numbers.
b) Take a suitable example and find 2's complement of a 8 bit binary number.
c) Explain fixed point and floating point representation of a number.
d) Differentiate Hardwired and micro programmed control unit.

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OR

Explain how addition and subtraction are performed in fixed-point numbers?

Unit - III

3. a) Write any two instructions of 8085.
b) Explain Universal Serial Bus (USB) interface.
c) What do you mean by Asynchronous data transfer?
d) What is program controlled I/O system? Explain with the help of a diagram.

OR

Differentiate :

- i) Non-vector and vectored interrupt
- ii) Maskable and non-maskable interrupt
- iii) Hardware and software interrupt

Unit - IV

4. a) Draw memory Hierarchy.
b) What is the advantage of using cache memory in a computer?
c) What do you mean by paging?
d) Explain direct mapping technique of cache organization.

OR

Define the different page replacement algorithms of cache memory.

Unit - V

5. a) What is parallel processing? Write its advantage.
b) What are the advantages of pipelining?
c) Why does pipeline improve performance?
d) What are the pipeline hazards? How do they affect the speedup?

OR

Explain SIMD array processor along with its architectural diagram.
