Total No. of Questions : 10] [Total No. of Printed Pages : 4

Roll No. .....

401

B. E. (Fourth Semester) EXAMINATION, June, 2009

(New Scheme)

(Common for CS, EC & IT Engg.)

COMPUTER SYSTEM ORGANIZATION

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Total questions to be attempted should be *five*. Attempt *one* question from each Unit.

Unit – I

1. (a) Explain with the help of neat diagram Von-Newman model of a computer. Also explain the main components of central processing unit. 10

   (b) What are the different registers of a basic computer ? Draw the block diagram of the hardware that implements the following register transfer statement : 10

$$y\,T_2 : R2 \leftarrow R1,\ R1 \leftarrow R2$$

Or

2. (a) Draw and explain the internal architecture of 8085 microprocessor. 10

P. T. O.

(b) Explain the following terms : 10

(i) Instruction code and Operation code

(ii) Direct and Indirect address instructions

(iii) Fetch and Execution cycle

(iv) Register and Memory Reference Instructions

(v) Addressing modes of a computer

Unit – II

3. (a) Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwire control associated with a control memory ? 10

(b) Define the following terms : 10

(i) Microoperation

(ii) Microinstruction

(iii) Microprogram

(iv) Microcode

Or

4. (a) Explain with the help of diagram arithmetic circuit using full adders. 10

(b) Explain how address sequencing of control memory is achieved in a microprogrammed control unit. 10

Unit – III

5. (a) What is the difference between isolated I/O and memory-mapped I/O ? What are the advantages and disadvantages of each ? 10

(b) Explain how an IOP have direct memory access capability that communicates with I/O devices. 10

Or

6. (a) Explain simplex, half duplex and full-duplex modes of communication. What is the difference between serial and parallel communication ? 10

   (b) Explain the Daisy chaining method of establishing priority interrupt in an interrupt driven I/O. 10

Unit – IV

7. (a) What are the three memory mapping procedures of cache memory ? Explain giving examples. 10

   (b) Discuss the different RAM and ROM. Also explain what is meant by content addressable memory. 10

Or

8. (a) What is meant by address and memory space in a virtual memory ? How virtual address is mapped in virtual memory ? 10

   (b) A virtual memory system has an address space of 8 K words, a memory space of 4 K words and page and block sizes of 1 K words. The following page reference changes occur during a given time interval (only page changes are listed. If the same page is referenced again it is not listed time) : 10

   4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

   Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is (i) FIFO (ii) LRU.

Unit – V

9. Explain how pipelining speed ups the processing of an operation. Explain the working of a four segment instruction pipeline. 20

P. T. O.

Or

10. Write short notes on any *two* of the following : 10 each

(a) Interprocess Communication

(b) Interconnection structure

(c) Supercomputers

(d) Attached array processor