Roll No .....

EC - 302

B.E. III Semester

Examination, December 2015

Computer System Organization

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

Unit - I

1. a) What is memory reference instruction?
   b) Write the differences between address bus and the data bus.
   c) Draw Von-Neumann architecture. What is meant by Von Neumann bottleneck?
   d) What is instruction cycle? Explain different phases of instruction cycle and show flow chart for instruction cycle.

   OR

   What is register? Explain various types of register.

Unit - II

2. a) Draw flow chart for decimal multiplication.
   b) What is Hardwired control unit?
   c) Write a brief notes on shift micro operation.

   d) With neat block diagram, explain working principal of micro program sequencer.

   OR

   Draw flow chart to explain how addition and subtraction of two fixed point number can be done.

Unit - III

3. a) What is Priority interrupt?
   b) List the features of IOP.
   c) Write the difference between programmed I/O and interrupt-driven I/O.
   d) Draw the block diagram of DMA transfer in computer system and explain.

   OR

   Explain in brief programmed I/O and interrupt initiated I/O.

Unit - IV

4. a) What is memory hierarchy?
   b) What is Content Addressable Memory? What are its advantages?
   c) Explain hit ratio in cache organization.
   d) Give short notes on virtual memory organization.

   OR

   Define the following terms:-

   i) Write through cache ii) Direct mapping

Unit - V

5. a) What is Flynn's Taxonomy?

   b) Write the characteristics of multiprocessor.
   c) Differentiate between loosely coupled and closely coupled multiprocessor configuration.
   d) Write the various performance issues in pipelining.

   OR

   What are Interconnection structure? Explain the scheme crossbar switch in detail.

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