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Roll No .....

MEVD-103

M.E./M.Tech., I Semester

Examination, December 2016

Advanced Logic Design

Time : Three Hours

Maximum Marks :70

Note : i) Attempt any five questions out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data, if required.

1. a) Draw and explain the circuit diagram, simplified circuit diagram and graphical symbols of EX OR gate built using CMOS technology.
   b) Explain the Karnaugh Map using literal, implicant and prime implicant with the help of a suitable example.

2. a) A four variable logic function that is equal to 1 if any three or all four of its variables are equal to 1 is called a majority function. Design a maximum cost POS circuit that implements this majority function.
   b) Design a circuit that generates the 9's complement of a BCD digit. Note that the 9's complement of d is 9-d.

3. a) For $V_{IH} = 4V, V_{OH} = 4.5V, V_{IL} = 1V, V_{OL} = 0.3V$ and $V_{DD} = 5V$, calculate the noise margins of NM_H and NM_L.
   b) Consider an eight input NAND gate built using NMOS technology. If the voltage drop across each transistor is 0.1V, What is V_{OL}? What is the corresponding NM_L using the other parameters from part (a).

4. a) SR flip flop is a flip flop that has set and rest inputs like a gated SR latch. Show how SR flip flop can be constructed using a D flip flop and other logic gates.
   b) Design a counter that counts pulses on line *w* and displays the count in the sequence 0, 3, 1, 2, 0, 3..... Use T flip flops in your circuit.

5. a) Write verilog code that represents a modulo 12 up counter with synchronous reset.
   b) Determine the number of gates needed to implement an eight bit carry look ahead adder, assuming no fan in constraints. Use AND, OR and XOR gates with any number of inputs.

6. a) What do you mean by metastability state? Explain with a suitable example.
   b) Give any five differences between the master slave and edge triggered flip flop.

7. Derive a minimal state table for an FSM that acts as a three bit parity generator. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates the parity bit p = 1 if and only if the number of 1s in the three bit sequence is odd.

8. Write short notes :
   a) Noise margins
   b) Factoring
   c) Bubble pushing
   d) Model Sim

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