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EX-8402(NGS)

B.E. VIII Semester Examination, June 2014

Digital Electronics and Logic Design - II (Elective-IV)

Time : Three Hours

Maximum Marks : 70

Note: Attempt any two part in each unit. Each unit contains equal marks.

UNIT-I

1. a) Determine the number of flip-flop required to design a sequence generator to generate 1101110.
   b) Construct a mealy state diagram that will detect a serial input sequence of 10110.
   c) Explain mealy and moore machines with the help of example.

UNIT-II

2. a) Design an iterative array which gives output 1 when ci '0' after 3 consecutive 1's is received.
   b) Describe three types of modeling in VHDL.
   c) Write the VHDL code for the following function $f(x, y, z, w) = w + z(x'y + xy') + z'xw$.

UNIT-III

3. a) Boolean expression for the circuit is given by following equation

$$y_1 = x_1x_2 + x_1y'_2 + x'_2\,y_1$$
$$y_2 = x_2 + x_1y'_1\,y_2 + x_1y'_1$$
$$z = x_2 + y_1$$

Where y_1, y_2 are internal states and z is output find flow table for circuit.

   b) What do you mean by hazards? Explain method of removal of hazards in sequential circuit design.
   c) Differentiate between synchronous and asynchronous sequential machines.

UNIT-IV

4. a) What is ASM chart compare ASM chart with state diagram? Explain with suitable example.
   b) Design a vending machine controller, machine accept the coin of Rs. 1,2,5,10 and gives a milk bottle of 10Rs. and return the extra money in the form of 1Rs. coin.
   c) Derive ASM chart for '0101' sequence detector.

UNIT-V

5. a) Implement the following functions by PROM
      i) $f_1 = \sum m(1,4,6)$
      ii) $f_2 = \sum m(2,3,4,6)$
      iii) $f_3 = \sum m(0,3,7)$
   b) Implement BCD to excess - 3 code converter by using PAL.
   c) Explain the following
      i) Xilinx.
      ii) Hard array logic.
      iii) FPGA.

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