Total No. of Questions: 10] [Total No. of Printed Pages: 4

Roll No.

EC-802

B. E. (Eighth Semester) EXAMINATION, June, 2012 (Electronics & Communication Engg. Branch)

CMOS CIRCUIT DESIGN

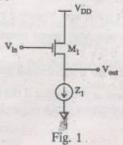
(EC-802)

Time: Three Hours Maximum Marks: 100 Minimum Pass Marks: 35

Note: Attempt one question from each Unit. All questions carry equal marks.

Unit-I

- (a) Discuss the small signal equivalent model for source follower. Derive equation for voltage gain of the source follower circuit.
 - (b) Calculate the V_{out} of source follower circuit as shown in the following figure with: $(\dot{W}/L)_{M_1} = 20/0.5$, $I_1 = 200 \,\mu$ A, $V_{TH_0} = 0.6 \,V$, $2 \,\phi \, F = 0.7 \,\nu$, $\mu_n \cos = 50 \,\mu$ A/ ν^2 and $\gamma = 0.4 \,\nu^2$ and $V_{in} = 1.2 \,\nu$.



P. T. O.

- 2. (a) Discuss the high frequency model of a cascode stage. 10
 - (b) Explain the effect of high frequency supply noise in differential pair. 10

Unit-II

 The circuit shown in the following figure uses a resistor rather than a current source to define a tail current of 1 mA.

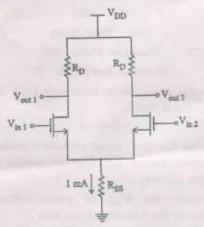


Fig. 2

Assume $(W/L)_{M_1 M_2} = 25/0.5$, $\mu_n \cos = 50 \mu A/v^2$, $V_{TH} = 0.6 v$, $\lambda = \gamma = 0$ and $V_{DD} = 3 v$:

- (a) What is the required input common mode for which R_{SS} sustain 0.5 v?
- (b) Calculate RD for a differential gain of 5.
- (c) What happens at the output if the input common mode level is 50 mV higher than the part (a) of this problem?

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		Or			
4,	(a)	Explain in brief the different properties of circuit.	feedback 10		
	(b)	Explain the voltage to voltage type of topologies.	feedback 10		
		Unit-III			
5.	osci	clain why a single common source stage late if it is placed in a unity gain loop. Illation be generated? Explain three-s llator. Or	How can		
6.	(n)	Discuss the mathematical model of voltage	controlled		
	(4)	oscillator.	10		
	(b)	Explain the block diagram of simple phase	lock loop.		
			10		
		Unit-IV			
7.	200	Design and explain positive edge tri	10		
	(b)	Explain the architecture of programmable	logic array		
		(PLA) with a neat diagram.	10		
8.	Wri	Write short notes on the following: 20			
	(a)	Serial Access Memory			
	(b)	Content Addressable Memory			
		Unit-V			
9.	(a)	Design a 4-bit adder/subtractor using operator.	data path 10 P. T. O.		

(b)	Design the following circuits:	10
	(i) 8-bit one/zero detector	
	(ii) 4-bit comparator	
	Or	
10. (a)	Design a 4 × 4 array multiplier.	10
(b)	Design and explain 3-bit increamentor circuit.	10

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