Total No. of Questions: 10] [Total No. of Printed Pages: 3 Roll No. 303(N) B. E. (Third Semester) EXAMINATION, Feb., 2010 (New Scheme) (Common for CS, EI & BM Engg. Branch) DIGITAL CIRCUITS AND SYSTEMS Time: Three Hours Maximum Marks: 100 Minimum Pass Marks: 35 Attempt any one question from each Unit. All questions carry equal marks. Assume and mention suitable missing data if any. Unit-I. 1. (a) Minimize the following function using K-map and implement the reduced expression using NAND gates only: $Y = \overline{ABC} + \overline{ACD} + \overline{AB} + \overline{ABCD} + \overline{ABC}$ (b) Reduce the following expression using Boolean algebra: (i) AB + ABC + A(B + AB)(ii) AB + AB + AB + ABOr 2. (a) Obtain M-N using 1's complement and complement if: 10

> M = 10110101, N = 00101101(ii) M = 00101101, N = 11101011

> > P. T. O.

(i)

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| (b) | (i) Convert the Gray code 110101 to binary form. | 1(|
| | (ii) Multiply (1 AB) ₁₆ by (89) ₁₆ . | |
| | Unit-II | |
| (a) | Implement a full adder circuit using two half add | er |
| | and an OR gate. | 1(|
| (b) | Simplify the following function using NOR-gates: | 10 |
| | (i) ABCD + A'BD + AB'C' | |
| | (ii) ABC + A'B + AC | |
| | Or | . 6 |
| (a) | Design a 4-bit adder with carry look ahead. | 1(|
| (b) | Design and explain the working of 4-bit BCD adde | er. |
| | O very series of the later of t | 1(|
| | Unit-III | |
| (a) | Show the circuit of a four input NAND gate us CMOS transistor. | ing |
| (b) | Sketch circuit of Schmitt trigger and explain | |
| | operation. What is hysteresis? | 10 |
| | . Or | |
| (a) | In an astable multivibrator, the base resistor are | 0 |
| | 12.5 k Ω and the capacitors are of 0.01 μ | F |
| 9 | Determine the PRR (pulse repetition ratio). | 1(|
| (b) | Calculate the noise margin of the ECL gate. | 10 |
| | Unit-IV | |
| (a) | Design a counter with the following repeated bin | arı |

sequence: 0, 1, 2, 4, 6. Use D flip-flops.

(b) What is a shift register? Explain serial in parallel out shift register. 10

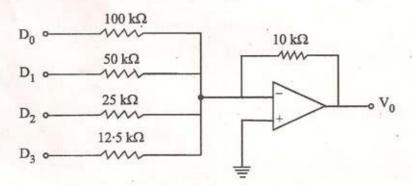
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- (a) What is ROM? Explain the meaning of (32 × 8)
 ROM and describe it.
 - (b) Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable.

Unit-V

- (a) Discuss the performance characteristics of D to A converter.
 - (b) Fig. below shows a D to A converter along with Op-Amp. Find the output of Op-Amp. if the input digital signal is 1011. Assume that binary 1 represents 5 V.



Or

- (a) Explain in detail successive approximation analog to digital converter.
 - (b) Determine the output voltage caused by each bit in a 16-bit ladder if the input levels are 0 = 0 V and 1 = +16 V.

Determine the resolution and full-scale output of this circuit. Find out the voltage from the above ladder for a digital input of 101011.

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