[Total No. of Questions : 5] [Total No. of Printed Pages : 3

Roll No. .....

CS/EC/IT–403

B. E. (Fourth Semester) EXAMINATION, June, 2009

(Old Scheme)

(Common for CS, EC & IT Engg.)

COMPUTER SYSTEM AND ORGANIZATION

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt all questions. There is internal choice in every question.

1. (a) Explain different phases of an instruction cycle with flow diagram. 10

   (b) Explain the function of the following registers in a processor : 10

   (i) Instruction Register

   (ii) Program Counter

   (iii) Accumulator

   (iv) Memory address register

   (v) Memory data register

Or

(a) Describe in detail Displacement addressing and Stack addressing. 8

(b) Explain the bus interconnection scheme. 6

(c) Explain Interrupt mechanism. 6

P. T. O.

2. (a) Explain the hard wired implementation of a control unit. 10

   (b) What is the relationship between instructions and micro-operations ? 5

   (c) What basic task does a control unit perform ? List the control signals required to perform the tasks. 5

Or

Explain the following terms : 20

(i) Microinstruction format

(ii) Control memory

(iii) Microprogram sequencing

(iv) Microinstruction encoding

3. (a) Draw and explain the flowchart for floating point addition and subtraction. 14

   (b) Draw the block diagram for the hardware implementation of addition and subtraction. 6

Or

(a) Divide − 145 by 13 in binary twos complement notation, using 12 bit word. Use binary division algorithm. 10

(b) Explain Booth's algorithm with example. 10

4. (a) In how many ways data can be transferred from I/O devices to memory ? Explain. 10

   (b) What do you understand by priority interrupt ? Explain Daisy chaining priority interrupt with a neat diagram. 10

Or

(a) Differentiate between memory mapped I/O and I/O mapped I/O. 8

(b) Draw and explain the block diagram of a typical DMA controller. 12

5. Write short notes on any *four* of the following : 20

(i) Memory Management Unit

(ii) Instruction pipelining

(iii) Cache memory mapping

(iv) RAM and ROM

(v) Virtual memory

(vi) Parallel Processing