Total No. of Questions : 8] *[Total No. of Printed Pages :2*

Roll No .....

EC-705 (GS)

B.E. VII Semester

Examination, December 2017

Grading System (GS)

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions.
ii) All questions carry equal marks.
iii) Assume suitable data if required.

1. a) Clearly explain various diffusion effects in silicon with emphasis on VLSI application.
   b) With neat sketches explain oxidation process in IC fabrication.

2. a) What is the need for design rules? Explain different types of design rules.
   b) Discuss the square law model of FET.

3. a) Derive a relation for the Sub threshold operations. How we can implement this operation on short channel devices.
   b) Draw and explain all the MOSFET Models for digital applications with the help of a suitable diagram.

4. a) Compare the high-frequency model of BJT and MOSSFET.
   b) What is stick diagram? Explain about different symbols used for components in stick diagram.

5. a) Explain Level 2 Large Signal Model and compare it with the high frequency model.
   b) What is Algotronix? Explain its architecture with detail.

6. a) Explain the principle of Micro coded controllers. Give any one practical application.
   b) Explain and differentiate the random logic forms and stridulated logic forms.

7. a) Discuss about latch up's physical origin, its triggering and its prevention methods.
   b) Explain the twin tub method of CMOSIC fabrication.

8. a) Write short notes on interconnects and circuit elements in VLSI circuits.
   b) Explain various triggering methods of latch up and how can it be prevented.

******