Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

EC-605 (GS)

B.E. VI Semester

Examination, December 2017

Grading System (GS)

VLSI Circuits and Systems

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) Explain different design strategies. Also draw and elaborate each part of Y-chart.
   b) Write and explain the various steps of CAD tool design process.

2. a) Describe the following with the help of CMOS logic:
      i) Inverter
      ii) Compound gates
      iii) Multiplexers
   b) State the difference between Mealy and Moore machine. Give simple example and draw the state transition diagram for them.

3. a) How minimization of state table is achieved for incompletely specified sequential machines? Explain with example.
   b) What are the timing conditions for proper operation of combinational circuit.

70

4. a) Explain the races and hazards in asynchronous sequential machine.
   b) Explain the fundamental mode and pulse mode asynchronous sequential machine.

5. a) Find the hazard in network which realizes the function: $y = (x_1 + x_2)(x'_2 + x_3)$. Eliminate it.
   b) What is system controller? Discuss the design aspect of controller phases. Design a controller for binary multiplier.

6. a) What is the concept of hardware and firmware algorithm? What is "Algorithmic state machine"? Explain.
   b) Explain fault detection using path sensitization method.

7. a) Using PLA, implement a combinational circuit which takes 4 inputs and produces gray code.
   b) Differentiate between CPLD and FPGA.

8. Write short notes on (any three)
   a) PALASM
   b) Secondary state assignments in asynchronous sequential machine
   c) VLSI design flow
   d) Data system designing
   e) ASM chart

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71