Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MEDC-104

M.E./M.Tech. I Semester

Examination, December 2016

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data, if required.

1. a) Discuss about the fundamental design for digital CMOS circuits with the help of any one example.
   b) Explain the basic concept of integrated circuits and its manufacturing technologies. Discuss about any one technology in detail with the help of suitable example.

2. a) Discuss about the ECL and Low voltage swing pads. Explain the similarity between the two.
   b) Explain the terms "setup time" and "hold time" in relation to a CMOS D register. If a clock is delayed to a register with regard to the data input, which of these parameters varies and how?

3. a) Draw and explain NP domino logic (Zipper CMOS). Write the advantages of dynamic logic styles.
   b) Draw and explain the CMOS complementary logic. Write its advantages and disadvantages.

4. a) Explain the difference between programmable logic and programmable logic structures with the help of suitable structure.

   b) Discuss about the dissipated power. Write down its classification and explain them in brief.

5. a) Write an introductory note on Algotronix. Explain its CAL logic cell functions.
   b) Explain the concept of sea of gates and gate array design with example.

6. a) Explain the design process which elaborates its capture, simulation and verification of any logic structure.
   b) Explain the memory and control strategies for subsystem design operations. Write an example.

7. a) Explain the effective implementation of PLA and ROM on CMOS sub-system design operations.
   b) Discuss about the Design abstraction and circuit validation of CMOS circuits.

8. Write short note on any two:
   a) Routing and Placement techniques.
   b) Timing analysis
   c) Fault tolerance
   d) Optimization

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