Total No. of Questions : 5] *[Total No. of Printed Pages : 2*

Roll No .....

EI/IC-602

B.E. VI Semester

Examination, December 2016

VLSI Technology

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.
ii) All parts of each question are to be attempted at one place.
iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.
iv) Except Numericals, Derivation, Design and Drawing etc.

1. a) Define crystal pulling mechanism.
   b) How is Electronic Grade Silicon formed from metallurgical grade Silicon?
   c) What is dislocation in a cubic silicon lattice?
   d) With the help of neat diagram discuss Bridgeman Technique and why the different temperatures are required at different stages of this technique.

   OR

   Why CZ technique is preferred over other techniques in Silicon processing.

2. a) Define Thermal oxidation.
   b) What are the interface trapped charges?
   c) Differentiate between film deposition and dielectric deposition.
   d) In a plasma deposited silicon dioxide the hydrogen contents is 6×10^{21} atoms/cm^3. The film density is 2.5g/cm^3. Find the atom density and at %H if the molecular weight of silicon dioxide is 60 and number of atoms per molecule or SiO_2 is 3.

   OR

Calculate the oxide thickness when it is grown by wet oxidation and when it is grown by dry oxidation at a temperature of 1000°C. Assume for wet oxidation $A = 0.226\mu m$, $B = 0.287\mu m^2/h$, $\tau = 0$ and for dry oxidation $A = 0.165\mu m$, $B = 0.047\mu m^2/h$ $\tau = 0.37h$.

3. a) What is the significance of resolution property in optical lithography?
   b) Define plasma formation.
   c) Explain simulation and integration process with flow chart.
   d) Calculate the four moments of Pearson distribution.

   OR

   Write about diffusion model with explanation of each step.

4. a) Discuss Micron and Lambda rules of design of any fabricated circuits.
   b) Write about layout levels and physical features for design consideration.
   c) Draw and explain stick diagram of layout of 2-input NOR gate.
   d) Compare nMOS load device characteristics for depletion load with and without body effect.

   OR

   Draw and discuss stick diagram of nMOS shift register and its layout using λ based diagram rules.

5. a) State Bottom up approach of design flow.
   b) What are multilevel gate Networks?
   c) Design 4-bit arithmetic circuit using combinational modules.
   d) Design a common bus system (4-bits) so that data can read and written from registers using MUX modules and register modules.

   OR

   Implement a two digit decimal counter using a register and a ROM.

******