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MCSE–103

M. E./M. Tech. (First Semester)
EXAMINATION, March, 2010

ADVANCED COMPUTER ARCHITECTURE

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) What is balancing of subsystem bandwidth ? Explain how the different balancing techniques improve the parallelism ? 8

   (b) Derive the expressions for efficiency, through put and speedup for k stage pipeline for n tasks. 8

   (c) Describe the characteristics of vector processing. 4

2. (a) Bring out the differences, merits and demerits of rearrangeable, non-blocking, blocking and networks. Give an example of commercial network for each one of them. 14

   (b) Compare the various multistage SIMD networks. 6

P. T. O.

3. (a) Given below is a reservation table with four stages :

	0	1	2	3	4	5	6	7
S_1	×							×
S_2		×	×					
S_3				×	×		×	
S_4						×	×	

(i) List the set of forbidden latencies between task initiations. 2

(ii) Give the collision vector C. 2

(iii) Draw the state diagram which shows all possible latency cycles. 4

(iv) List all simple cycles from the state diagram. 2

(v) List all greedy cycles from the state diagram. 2

(vi) Determine the minimal average latency (MAL). 2

(b) Explain static and dynamic pipeline. 6

4. (a) With a block diagram explain the working of a unidirectional bus interconnection network for multiprocessors system. What are its advantages and drawbacks ? 12

(b) Explain briefly the following bus arbitration algorithms and give their relative merits : 8

(i) The dynamic priority algorithm.

(ii) The first-come first-served algorithm.

5. (a) Diagrammatically represent dynamic coherence check for fetch operation in a multi cache memory organization and explain all four rights in brief. 10

(b) Lets consider a multiprocessor system with private cache has a memory block of 1024 K and L = 16 lines. 10

Calculate :

(i) Modules (N) in each line.

(ii) Words in each module.

(iii) Minimum length of a block of data for effective memory utilization.

(iv) If line i and module j be represented by L_i and M_j respectively, where would be Kth word of the block of data exist on line i ?

6. (a) Draw a 8 × 8 Omega network. 6

(b) Compare and contrast fork-join and co-begin co-end statements with examples. 8

(c) Depict graphically cost versus no. of processors and performance versus no. of processors for bus, cross bar switch and multistage network. 6

7. (a) Explain hierarchical structured multiprocessor system. 10

(b) Describe processor characteristics for multiprocessing systems. 10

8. Write short notes on any *two* of the following : 10 each

(i) Flynn's and Handler's architectural classification

(ii) S-access and C-access memory organisation

(iii) Multistage networks