Roll No .....

EC - 302

B.E. III Semester

Examination, December 2012

Computer System Organization

Time : Three Hours

Maximum Marks : 70/100

Note: *1. Attempt one question from each unit.*
2. All questions carry equal marks.

Unit - I

1. a) What are various subsystems of computer? Explain each.

   b) What is instruction cycle? Explain different phases of instruction cycle and show flow chart for instruction cycle.

OR

2. a) What are various types of addressing modes? Explain them in short them with example.

   b) Show the hardware implementation for the following statements. The registers are 4-bit in length.

   $T_0 : A \leftarrow R_0$

   $T_1 : A \leftarrow R_1$

   $T_2 : A \leftarrow R_2$

   $T_3 : A \leftarrow R_3$

Unit - II

3. a) What is the purpose of micro program sequencer? Explain its functioning.

   b) Define the following terms:

   i) Control Memory

   ii) Micro operation

   iii) Register transfer language

   iv) Micro instruction

OR

4. a) Draw the block diagram for selection of neat address for a control memory. Explain the function of each block.

   b) Draw the flowchart and explain how division of two lined-point binary numbers in sign-magnitude representation is carried out.

Unit - III

5. a) Explain in short programmed I/O and interrupt initiated I/O.

   b) Differentiate between the following:

   i) I/O program controlled transfer and DMA transfer.

   ii) Isolated I/O and memory mapped I/O.

OR

6. a) What do you mean by interrupt? What are various interrupt handling techniques? Explain.

   b) What do you mean by serial transmission and parallel transmission of data? Compare them.

Unit - IV

7. a) What is the need of virtual memory in computer system? Explain how the page map table is organized in virtual memory system.

   b) What are various mapping methods used with cache memory organisation? Explain set associative memory mapping.

OR

8. a) What is associative memory? Explain the concept of match-logic for associative memories.

   b) Consider a cache consisting of 256 block of 16word each, for a total of 4096 (4k) words, and assume that the main memory is addressed by a 16-bit address and it consist of 4K blocks. How many bits are there in each of the TAG, BLOCK/SET and word field for different mapping techniques?

Unit - V

9. a) Write explanatory note on parallel processing.

   b) What do you mean by pipeline? Explain various pipeline conflicts.

OR

10. a) What is an interconnection network? Explain different types of interconnection network.

    b) Write short note on array processor.

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