MEDC–104

M. E./M. Tech. (First Semester) EXAMINATION, Dec., 2011

(Grading/Non-Grading System)

VLSI DESIGN

(MEDC–104)

Time : Three Hours

Maximum Marks : { *GS : 70* / *NGS : 100* }

Note : Attempt any *five* questions. All questions carry equal marks. Assume and mention suitable missing data if any.

1. (a) For a CMOS invertor calculate the shift in the transfer characteristics when the β_n/β_p ratio is varied from 1/1 to 10/1.

   (b) Explain twin-tub process for CMOS fabrication.

2. For a Pseudo-n MOS invertor :

   (a) What $V_{open\ loop}$ must be choosen such that the pull down transistor of a subsequent Pseudo-n MOS gate will be off when the invertors output is logic 1 ?

   (b) What is the ratio $W_p/L_{pp}/W_n/L_n$ required to achieve the output voltage ?

3. (a) What are various techniques used to minimize the power dissipation in CMOS logic.

   (b) Derive the expression for fall time and rise time in a CMOS invertor.

4. (a) What is the relationship between a truth table and the pattern of programming tabs in a PLA's AND and OR planes ?

   (b) Implement the function $Y = X^2$ for two bit input with the help of ROM.

5. Explain the following terms with respect to CMOS-Chip design :

   Hierarchy, regularity, modularity and locality

   Give an example of each.

6. What is scan based test technique ? Write briefly differences between serial and parallel scan based test techniques.

7. (a) Explain the following terms :

   Observability, Controllability and Fault coverage

   (b) What do you mean by routing of the chip ? Explain Global routing.

8. Summarize the differences between a SOG chip and a standard-cell chip. What benefits does each implementation style have ?