## EX-403 DIGITAL ELECTRONICS LOGIC DESIGN-I

**Unit I**

Number Systems and Codes : Digital number systems, base conversion, Binary, Decimal, octal, Hexadecimal, number system with radix r, Gray codes.Alphanumeric codes – ASCII code and EBCDIC codes, Hollerith code, concept of parity, complement r's & (r-1)'s, subtraction with complements, signed Binary numbers, Error Detecting & Correcting codes. Basic Theorems & Properties of Boolean Algebra: AND, OR, NOT operators, laws of Boolean Algebra, Demorgon's theorem, Boolean expression & logic diagram. Negative logic, Alternate logic gate representation (concept of bubbled gates) canonical and standard Forms (Minterms & Maxterms), sum of minterms & product of maxterms, conversion between canonical forms. Truth table & maps, 2,3,4,5 and 6 variable maps, Solving digital problems using Maps, Don't care conditions, Tabular minimization. Sum of product & product of sum reduction, Exclusive OR & Exclusive NOR circuits, Parity generator & checkers.

**Unit II**

Combinational Circuits : Design procedure, Adders (half and Full), subtractor (half and full) code convertors, Analysis of design, Universal building blocks, Implementation of any logic circuit with only NAND gates or with only NOR gates, Binary serial adder, parallel adder, serial/parallel adder, look ahead carry generator, BCD adder, Binary multiplier, Magnitude comparator, Decoder, Demultiplexer, Encoders, priority encoder, Multiplexers & implementation of combinational logic diagram, HDL for combinational circuit.

**Unit III**

Sequential Logic Circuit : Latches, SR latch with NAND & NOR gates, D latch, edge triggered flip flop, J-K flip flop, T flip flop, Master slave flip flop, Analysis of clocked sequential circuit, state table, state diagram, state reduction state equations, state assignments, flip flop excitation table & characteristic equations, Design procedure for sequential circuits, Design with state reduction, Applications of flip flop.

**Unit IV**

Registers and Counters : Asynchronous and Synchronous counter, counters with MOD numbers, Down counter, UP/DOWN counter, propagation delay in ripple counter, programmable counter, Pre-settable counter, BCD counter, cascading, counter applications, Decoding in counter, Decoding glitches, Ring Counter, Johnson counter, Rotate left & Rotate right counter, Registers – Buffer, Shift left, shift right, shift left/Right registers, parallel in parallel out, serial in serial out, parallel in serial out, serial in parallel out registers.

**Unit V**

Random Access Memory, Timing waveform, Memory Decoding, Internal Construction, Coincident decoding, Address multiplexing, Read only memory – Combinational circuit implementation, Type of ROMs, combinational PLDs, Programmable Logic Array (PLA), Programmable Array Logic (PAL), sequential programmable device. Analog to digital conversion – Ramp type, dual slope, integration, successive approximation, parallel conversion, parallel/ serial conversion, convertor specifications, Digital to Analog convertors – Binary weighted & R/2R D to A convertors.

**References:**


1. Mano; Digital design; Pearson Education Asia
2. Thomas Blakeslee; Digital Design with standard MSI and LSI; Wiley Interscience
3. Jain RP; Modern digital electronics; TMH
4. -M.Mano; Digital logic & Computer Design; PHI
5. Tocci ; Digital Systems Principle & applications; Pearson Education Asia
6. Gothmann; Digital Electronics; PHI
7. R.H.Gour; Digital Electronics and Micro Computer - (Dhanpat Rai)
8. –Malvino, Leech; Digital Principles and applications –(TMH)
9. Floyad; Digital Fundamentals (UBS)
10. Nripendra N. Biswas; Logic Design Theory (PHI)
11. D.C. Green; Digital Electronics (Pearson Education Asia)


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**List of Experiments (Expandable):**

1. Verification of all the logic gates.
2. Design of BCD to Excess-3 code converter.
3. Implementation of NAND & NOR as Universal gate.
4. Design of RS, JK, T& D Flip flop.
5. Multiplexer /Demultipexer based boolean function
6. Design of combinational circuit for the
    (i) Half adder
    (ii) Full adder
    (iii) Half subtractor
    (iv) Full subtractor
7. Design various A-D & D-A convertors.

**NOTE-** - All experiments (wherever applicable) should be performed through the following steps.

**Step1: Circuit should be designed/ drafted on paper.**

**Step 2**: Where ever applicable the designed/drafted circuit should be simulated using Simulation S/W (TINA-V7/ PSPICE/ Labview/ CIRCUIT MAKER etc.).

**Step 3**: The designed/drafted circuit should be tested on the bread board and compare the results with the simulated results.

**Step 4**: Where ever required the bread board circuit should be fabricated on PCB.

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