Total No. of Questions : 10] [Total No. of Printed Pages : 4

Roll No. .....

CS–605(N)

B. E. (Sixth Semester) EXAMINATION, June, 2011

(Computer Science & Engg. Branch)

ADVANCE COMPUTER ARCHITECTURE

[CS–605(N)]

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt *one* question from each Unit. All questions carry equal marks.

Unit–I

1. (a) Explain Flynn's classification based on multiplicity of instruction stream and data stream. 10

   (b) Explain the following terms to measure performance of computer system : 10

   (i) Clock rate and CPI (Cycle Per Instruction)

   (ii) MIPS (Million Instruction Per Second) rate

   (iii) Throughput rate

   (iv) Performance factor

2. (a) Explain the architectural operations of SIMD and MIMD computers. Distinguish between multiprocessor and multicomputers based on their structure. 10

P. T. O.

(b) What is Interconnection Network ? Explain different interconnection network architectures comparing their architectural features. 10

Unit – II

(a) Explain the following terms associated with cache design : 10

(i) Write through verses write back cache

(ii) Factors affecting cache hit ratios

(b) Discuss arbitration, transaction and interrupt w. r. to backplane bus system. 10

(a) Explain Interleaved memory organization. Justify the use of interleaved memory organization. 10

(b) Explain MESI protocol for cache coherence with suitable example. 10

Unit – III

(a) Explain the following approaches to the branch problem in pipeline processor : 10

(i) Branch elimination

(ii) Branch prediction

(iii) Branch target

(b) Distinguish between the following : 10

(i) Arithmetic and instruction pipeline

(ii) Unifunctional and multifunctional pipeline

(iii) Static and dynamic pipeline

(iv) Scalar and vector pipeline

(a) Explain the working of arithmetic pipeline with suitable example. 10

(b) Consider the following reservation table for 4 stage pipeline with clock cycle P = 20 ns : 10

	1	2	3	4	5	6
S_1	×					×
S_2		×		×		
S_3			×			
S_4				×	×	

(i) What are the forbidden latencies and initial collision vector ?

(ii) Draw state transition diagram.

(iii) Determine the MAL associated with the shortest greedy cycle.

(iv) Determine the pipeline throughput corresponding to the MAL and given P.

Unit–IV

7. (a) Compare distributed and shared memory model. 10

(b) What is vector processing ? Explain the characteristics of vector processing. 10

8. (a) Explain message routing schemes in multicomputer network. 10

(b) Explain Snoopy coherency protocol. 10

Unit–V

9. (a) Explain various parallel programming models. 10

(b) Write in brief on parallel languages and explain the features of parallel language for parallelism. 10

10 Write short notes on the following : 20

(i) Parallel software tools

(ii) Object oriented parallel programming model

(iii) Parallel programming environment

(iv) Vector access memory schemes