Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal

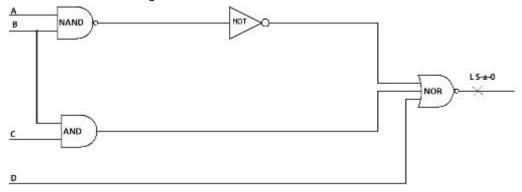
www.rgpvonline.com

M.E./M.Tech. (Second Semester)
EXAMINATION, June 2012
(Grading/Non-Grading)
VLSI TEST AND TEST ABILITY

Time: Three Hours Maximum Marks: GS:70

Note: Attempt *two* sections from each question. Section (a) is compulsory.

- 1. (a) What do you understand by testing? Explain the importance of testing in VLSI system.
 - (b) Discuss different types of faults in VLSI circuits during fabrication and packaging.
 - (c) Explain IC production test process and burn-in-board.
- 2. (a) Describe the importance of stack-at-faults and bringing faults in fault detection process.
 - (b) Briefly discuss various faults which occur in RAM.
 - (c) What is simulation? Explain parallel and detective fault simulation.
- 3. (a) Explain BIST implementation in hardware design.
 - (b) Discuss I_{DDO} testing with importance in VLSI design.
 - (c) Discuss ATPG for a sequential digital circuit taking a suitable example.
- 4. (a) Explain path sensitization method and its limitation.
 - (b) Find the test vectors using FAN and PODEM for L-s-a-0.



- (c) Discuss the architecture of RAM-BIST.
- 5. (a) Describe Boolean difference method to find out test vectors.
 - (b) Explain PODEM and D-algorithm with suitable example.
 - (c) List various methods for delay fault testing. Elaborate any one of them giving suitable example.