Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

CS-222

B.E., III Semester

Examination, December 2016

Choice Based Credit System (CBCS)

Digital Circuit and Design

Time : Three Hours

Maximum Marks : 60

Note: i) Attempt any five questions out of given eight questions.
ii) All questions carry equal marks.

1. a) Do as directed
   i) $(56)_{16}=(?)_{10}$
   ii) $(32)_{10}=(?)_{2}$
   iii) Bubbled OR gate is also called _____.
   iv) What is Karnaugh Map?
   b) i) State the distributive property of Boolean algebra.
   ii) Obtain the truth table of the function:
   $F = xy + xy' + y'z$

2. a) i) Why NAND gate is known as universal gate?
   ii) Show that (A+C) (A+D) (B+C) (B+D) = AB+CD
   b) Explain full adder and design a full adder circuit using 3 to 8 decoder and two OR gates.

3. a) Reduce the expression $F=\Sigma_m(0, 2, 3, 4, 5, 6)$ using K-map and implement using NAND gates only.
   b) Design a synchronous BCD counter with JK flip-flops.

4. a) Explain two input CMOS NAND gate with neat diagram.
   b) Explain Look Ahead Carry generator.

5. a) Give classification of logic families. Also list the characteristics of digital IC.
   b) Show the circuit of four-input NAND gates using CMOS transistors.

6. a) Write short note on Read Only Memory (ROM).
   b) Explain the Emitter-Coupled Logic (ECL) in detail.

7. a) How does a counter works as frequency divider? Explain with suitable example.
   b) A combinational logic circuit is defined by the functions: $F_1 = \Sigma(3, 5, 6, 7)$ and $F_2 = \Sigma(0, 2, 4, 7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs.

8. a) Explain Analog to Digital converter.
   b) Write short notes on sample and hold circuits.

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