MCSE-103

M. Tech. (CSE) (First Semester)

EXAMINATION, Dec., 2010

ADVANCED COMPUTER ARCHITECTURE (MCSE-103)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks. : 40



Note : Attempt any five questions. All questions carry equal marks.

1. (a) Discuss the Flynn's classification scheme of computer architectures. 10

(b) Define the following performance factors of a system : 10

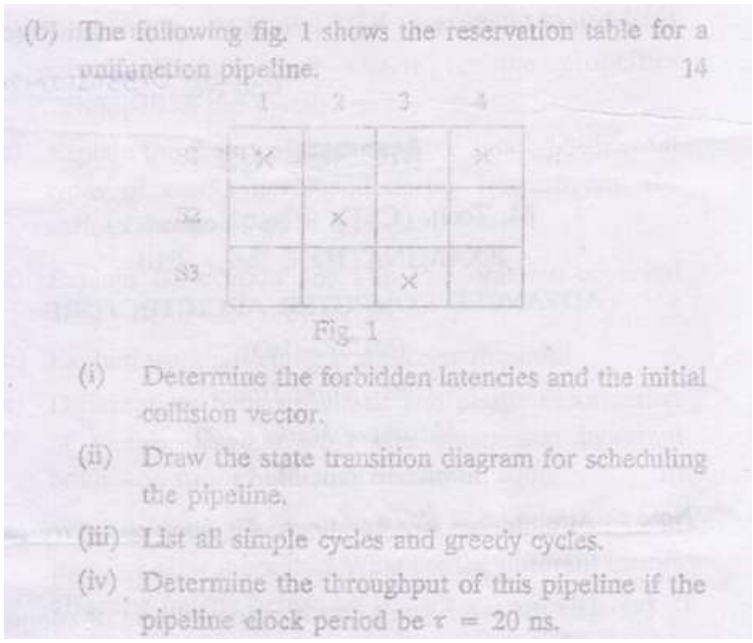
(i) MIPS rate (ii) Throughput rate (iii) CPI

2. (a) What is vector processing ? Discuss the various vector instruction types. 10

(b) Discuss the different data dependent hazards. How can these hazards be avoided ? 10

3. (a) Draw the basic structure of a linear pipeline processor. Define the following terms related to linear pipeline : 6

(i) Speed up (ii) Efficiency



(b) The following fig. 1 shows the reservation table for a unifunction pipeline. 14

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| S1 | × | | | × |
| S2 | | × | | |
| S3 | | | × | |

Fig. 1

(i) Determine the forbidden latencies and the initial collision vector.

(ii) Draw the state transition diagram for scheduling the pipeline.

(iii) List all simple cycles and greedy cycles.

(iv) Determine the throughput of this pipeline if the pipeline clock period be $\tau$ = 20 ns.

4. (a) Differentiate between UMW, and NUMA models of shared memory multiprocessor. 10

(b) Define the following terms for various systeni interconnect architectures : 10

(i) Node degree (ii) Network diameter (iii) Bisection bandwidth

(iv) Static connection network (v) Dynamic connection network

5. (a) Explain the SHAD parallel algorithm 0 (n2) for SIMD matrix multiplication. 10

(b) What is associative memory ? 'List the various associative search algorithms. 10

6. Write the four conditions under which deadlock occurs. are the different solutions to deadlock problem?

7. (a) discuss the effect of branching on an instruction pipline.

(b) Discuss the classification of pipeline processors .

8 Write short notes on any three of the following

(a) cache coherence problem

(b) Control flow versus data flow mechanism

(c) messagepassing mechanisms

(d) Itneinal forwarding and register tagging