Total No. of Questions :5] *[Total No. of Printed Pages : 2*

Roll No .....

EI/IC - 602

B.E. VI Semester

Examination, June 2016

VLSI Technology

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

1. a) What is water terminology?
   b) What are crystal defects?
   c) Draw the flow diagram of typical VLSI design flow.
   d) How is NMOS transistor fabricated? Illustrate with proper diagrams.

   OR

   What is CZ method? Explain, with proper diagram, czochralski process.

2. a) Give the name of methods of Epitaxial growth.
   b) Explain different types of oxidation.
   c) What is thin film fabrication?
   d) What is metalization? Explain briefly and what kind of material is best suited for metalization.

Or

Write the function of metallization in monolithic IC processing. Explain sputtering process used in metallization.

3. a) What is x-ray lithography?
   b) What is solid state diffusion?
   c) Explain doping mechanism.
   d) Explain ion implantation process and draw its diagram. Write the advantages of ion implantation process.

   OR

   Explain oxidation process in detail.

4. a) Define lambda rules.
   b) What is clean room?
   c) Explain EDA tools.
   d) Discuss the slicing and non-slicing floorplanning with necessary diagram.

   OR

   Draw the stick diagram of a NMOS inverter. Explain it and justify the role of stick diagram in IC fabrication.

5. a) What are Flash memories?
   b) What is latch-up?
   c) Explain non-volatile RAM.
   d) What are data path circuits? How is an adder implemented in sub-systems design?

   OR

   How the latch-up can be eliminated in CMOS technology?

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