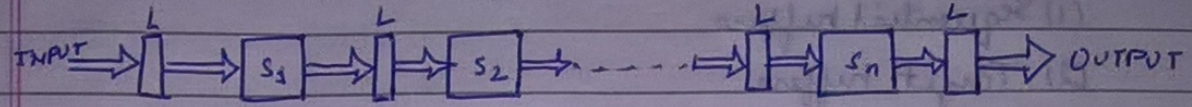
UNIT- 3

PIPELINE PROCESSOR

A The concept of processing problem in overlapped manner is called pipeline processing.

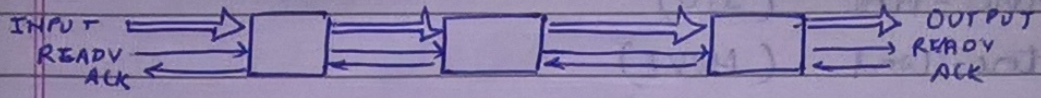
① Linear Pipeline Processor -

A sequence of subtasks with linear precedence.

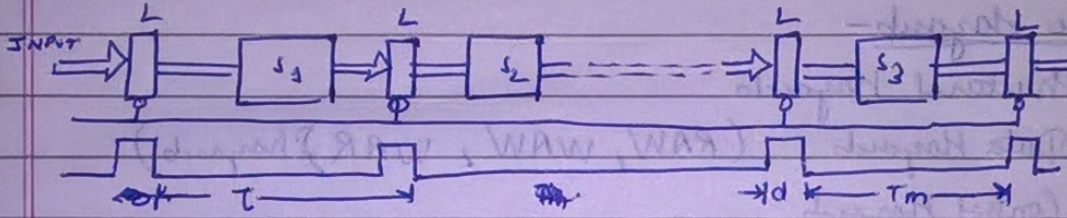


L - latch , S → Stages.

Asynchronous model -



Synchronous model -



n → inputs
K → stages.

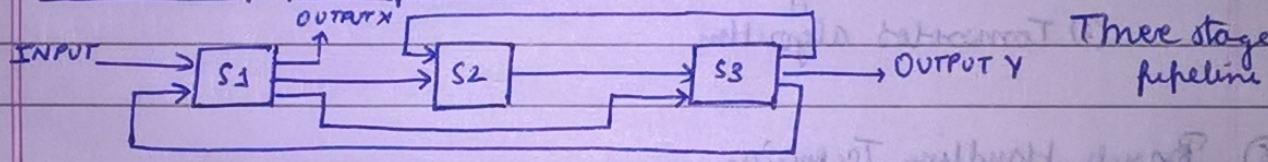
$f = \frac{1}{\tau}$

$$\text{Speedup} = \frac{nk}{k+n-1}$$

$$\text{Efficiency} = \frac{n}{k+n-1}$$

$$\text{Throughput} = \frac{Nf}{k+n-1}$$

② Nonlinear pipeline processor -



Three stage pipeline

Reservation table → show the path of data flow in pipeline

latency → No. of time units between two initiations of a pipeline

latency that cause collision is called forbidden latency.

Numerical → Collision vector, State Diagram, MAL (Minimum Average latency)

Greedy cycles, average latency

③ Instruction pipeline design -

→ Instruction execution phases -

(1) Instruction fetch
(2) Decode
(3) Operand fetch
(4) Execute
(5) Write back phase.

ILP → Instruction level parallelism

→ Mechanism for instruction pipeline -

→ Pre-fetch buffers -

(1) Sequential buffers

(2) Target buffers

(3) Loop buffers

→ Internal data forwarding -

(1) Store - Store (STO)

(2) Store - Load (MOVE)

(3) Load - Load (MOVE)

④ Pipelining Hazards -

(1) Structural Hazards

(2) Data Hazards (RAW, WAW, WAR Hazards)

(3) Control Hazards

⑤ Dynamic Instruction scheduling -

(1) Score - boarding

(2) Tomasulo algorithm

⑥ Branch Handling Techniques -

(1) Dynamic Branch Prediction

(2) Branch Target Buffers

(3) Delayed branch.

⑦ Arithmetic Pipeline design -

(1) Static arithmetic pipeline (fixed arithmetic operation)

(2) Multifunctional arithmetic pipelines (More than one arithmetic operations)

⑧ Superscalar Pipeline design - m instruction issue rate, m ILP to fully utilize the pipeline

⑨ Superpipeline processor design -