Total No. of Questions : 5] [Total No. of Printed Pages : 3

Roll No. .....

EC–505(N)

B. E. (Fifth Semester) EXAMINATION, Dec., 2010

(New Scheme)

(Electronics & Communication Engg. Branch)

CMOS VLSI DESIGN

[EC–505(N)]

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt any *five* questions Attempt one question from each Unit. All questions carry equal marks.

Unit–I

1. (a) Draw the stick diagram for : 6
   (i) An Inverter
   (ii) 2 Input Nand Gate

   (b) What are second order effect ? Explain briefly. 6

   (c) Calculate the threshold voltage V_{to} for $V_{CB} = 0$ for a P channel Mosfet with the following parameters : 8

   Substrate doping = $10^{15}/cm^3$

   Polysilicon gate doping density = $10^{20}/cm^3$

   Gate oxide thickness = 650 Å

   Oxide Interface fixed charge density = $2 \times 10^{10}/cm^2$

P. T. O.

Or

Explain the different mode of operation of NMOS device in brief and derive the relationship between gate to source voltage (V_{gs}) and drain current (I_D) in linear and saturation region. 20

Unit – II

(a) What are VLSI Interconnects ? How interconnects are developed during IC fabrication ? 12

(b) What is Scribe Line ? What is its use in fabrication of CMOS transistor ? 8

Or

(a) Explain a basic N-well CMOS process for fabrication of MOS transistor. 10

(b) Explain the photolithographic process during the fabrication of MOS devices. 10

Unit – III

(a) What is power dissipation in CMOS ? Explain its cause and explain how we can reduce them. 12

(b) Explain the following terms with respect to CMOS chip design : 2 each

(i) Supply voltage

(ii) Process variation

(iii) Reliability

(iv) Design corner

Or

(a) List various types of scaling techniques and explain the effect of scaling factor on drain current (I_D), power dissipation and area for constant field scaling. 12

(b) Explain the following terms : 4 each

(i) Parasitic delay

(ii) Transistor sizing

Unit – IV

7. What are Current Mirrors ? Explain them and also derive expression for it. 20

Or

8. (a) Explain how CMOS inverter can be used as an amplifier. 10

(b) With the help of diagram explain the working of : 10

(i) CMOS operational amplifier

(ii) Differential pairs

Unit – V

9. With the help of diagram explain the working of BICMOS circuit. Explain the advantage and drawback of BICMOS over CMOS logic and also derive the expression for switching delay in BICMOS logic. 20

Or

10. Explain the following terms : 4 each

(i) Cell hierarchies

(ii) Cell libraries

(iii) Cell shapes

(iv) Library entries

(v) Boot strapping