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# EI - 602

## B.E. VI Semester

Examination, December 2014

## VLSI Technology

*Time : Three Hours*

*Maximum Marks : 70*

*Note:* Attempt five questions. One question from each unit. Assume suitable missing data, if any.

### Unit - I

1. a) Draw the flow diagram of typical VLSI design flow and explain. 7
   b) Write a brief note on crystalline orientations and crystal defects. 7

OR

2. a) What is CZ method? Explain, with proper diagram, czochralski process. 7
   b) How is a NMOS transistor fabricated? Illustrate with proper diagrams. 7

### Unit - II

3. a) Draw a horizontal Epitaxial reactor and explain the epitaxial process. 7
   b) What is thin film fabrication? Explain any one method of deposition of thin film. 7

OR

4. a) How is the silicon wafer oxidized? What is the purpose of this oxidation layer? 7







   b) Write the function of metallization in monolithic IC processing. Explain sputtering process used in metallization. 7

### Unit - III

5. a) Explain photolithography process with proper diagrams. 7
   b) Explain ion implantation process and draw its diagram. Write the advantages of ion implantation process. 7

OR

6. a) Write a short note on X-ray lithography. 7
   b) What do you mean by diffusion? Explain the process of diffusing n-type impurities into silicon wafer. 7

### Unit - IV

7. a) Write the goals and objectives of Floorplanning. 7
   b) What is a clean room? Define class number. Describe briefly how you can achieve the desired clean room condition necessary for IC fabrication. 7

OR

8. a) Draw the stick diagram of a NMOS inverter. Explain it and justify the role of stick diagram in IC fabrication. 7
   b) Discuss the slicing and non-slicing floorplanning with necessary diagram. 7

### Unit - V

9. a) What are data path circuits? How is an adder implemented in sub-system design? 7
   b) Write a short note on non-volatile RAM. 7

OR

10. Describe, in detail, latch-up phenomena in CMOS circuits. 14

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