d) Design and explain the working of an 4-bit parallel counter.

OR

Design a counter to count the sequence 0, 1, 2, 3, 4, 5, 6 ..... using SR FF's

5. a) Distinguish between PAL and PLA.
   b) Write the advantages of E^2 PROM over an EPROM.
   c) Implement EX-OR function using PROM.
   d) Briefly describe the principle of operation of a flash-type A/D converter. What are the merits and demerits of this type of converter?

OR

Realized BCD to Excess-3 code using ROM array.

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Total No. of Questions :5] *[Total No. of Printed Pages :4*

Roll No .....

EX-403

B.E. IV Semester

Examination, December 2016

Digital Electronics Logic Design - I

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.
ii) All parts of each question are to be attempted at one place.
iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.
iv) Except numericals, Derivation, Design and Drawing etc.

1. a) Convert the following :
   i) $(13A7)_{16} = (\quad)_{10}$
   ii) $(3F2)_{16} = (\quad)_2$
   b) Find the Gray code equivalent of decimal 13.
   c) Draw logic implementation of two-input EX-OR using NAND only.
   d) Minimize the Boolean function.

   f (A, B, C, D) = π (0, 4, 5, 6, 7, 10, 14) using K-map method.

OR

Using tabulation method simplify the Boolean function

$$F = \sum(0,1,2,8,10,11,14,15)$$

2. a) Implement the following function using suitable multiplexer $F = \sum m(0,2,5,7)$.

   b) Write an expression for borrow and difference in a full subtractor circuit.

   c) Design a two-bit magnitude comparator. Also, write relevant Boolean expressions.

   d) Draw the logic diagram of a 2-bit by 2-bit binary multiplier and explain its operation.

OR

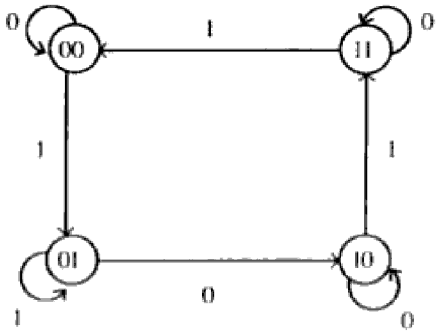
Design a BCD to Gray code converter. Uses don't care.

3. a) What is race around condition? How do you eliminate it?

   b) Draw a NAND based logic diagram of Master slave JK FF.

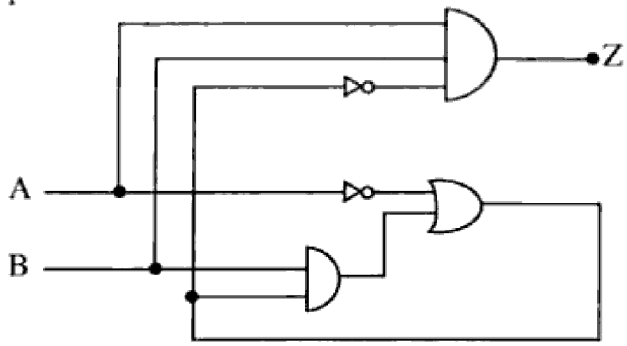
   c) Convert T-flip flop into a JK flip flop.

   d) For the state diagram shown in below figure, design a synchronous sequential circuit using JK flip flops.

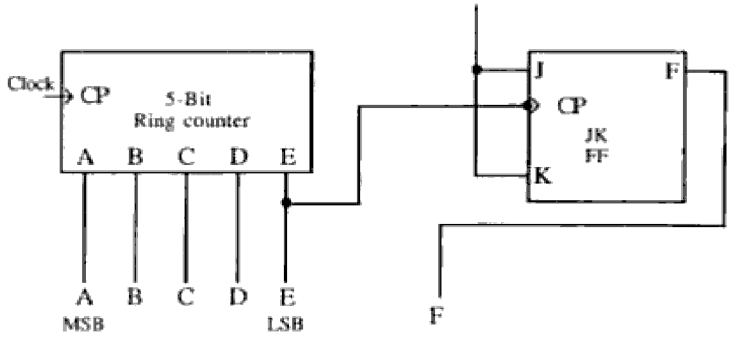


OR

Analyze the circuit shown in figure below by producing the transition table and output map, the flow table and finally the state diagram. What function does the circuit perform?



4. a) Determine the modulus of the counter shown in below figure and write the counting sequence.



   b) The flip-flops used in a 4-bit binary ripple counter have a High-to-Low and Low-to-High propagation delay of 25 and 10ns. respectively. Determine the maximum usable clock frequency of this counter.

   c) How can presettable counter be used to construct counters with variable modulus?