Total No. of Questions : 8] [Total No. of Printed Pages : 3

CS/IT–7102

B. E. (Seventh Semester) EXAMINATION, June, 2007

(Common for CS & IT Engg.)

ADVANCE COMPUTER ARCHITECTURE

(Elective – I)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Explain the cache performance issues. 10
   (b) Explain the direct mapping cache organization and set associative cache organization. 10

2. Define the following terms associated with memory hierarchy design : 2 each
   (i) Virtual address space
   (ii) Physical address space
   (iii) Address mapping
   (iv) Cache blocks
   (v) Multilevel page tables
   (vi) Page fault
   (vii) Hit ratio
   (viii) Hashing function

   (ix) Inverted page table
   (x) Memory replacement policies

3. (a) Explain the following terms related to vector processing : 10
   (i) Vector and scalar balance point
   (ii) Vectorization ratio in user code
   (iii) Vectorization compiler
   (iv) Gather and scatter instructions
   (b) Explain the following memory organization for vector accesses : 10
   (i) S-access memory organization
   (ii) C-access memory organization

4. (a) Draw architecture details of a typical vector processor with multiple functional pipes. Describe each block. 10
   (b) Explain the Data Flow Computer and Control Flow Computer. 10

5. (a) Explain the scheduling of dynamic pipelines. 10
   (b) Find the set of distances and the collision vector for the reservation table shown : 10

	0	1	2	3	4	5	6	7
S_1	1			1		1		
S_2		1	1		1			
S_3				1				1

6. (a) What are the different criteria of classification of connection networks ? 10

(b) What is meant by a single stage and multistage network ? 5

(c) What is the meaning of mutual exclusion between processors ? 5

7. (a) Write the criteria to design parallel algorithms. 10

(b) Explain the delta network and its construction. 10

8. Write short notes on any *two* of the following : 10 each

(i) Memory bounded speedup model

(ii) Message passing mechanisms

(iii) Cache coherence

(iv) Cluster computers