Total No. of Questions : 10] [Total No. of Printed Pages : 3

Roll No. .....

EC–403

B. E. (Fourth Semester) EXAMINATION, June, 2009

(New Scheme)

(Electronics & Communication Engg. Branch)

DIGITAL ELECTRONICS

(EC – 403)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt any *five* questions. All questions carry equal makrs.

Unit – I

1. (a) Convert the following : 10

(i) $[1001011]_{gray} = [\quad]_2$

(ii) $[10110110 \cdot 0011]_2 = [\quad]_{BCD}$

(iii) $[10110101]_{2421} = [\quad]_{10}$

(iv) $[57621]_8 = [\quad]_{16}$

(v) $[76]_{10} = [\quad]_{gray}$

(b) Simplify the following : 5

(i) $Y = AB + \overline{AC} + A\overline{B}C\,(AB + C)$

(ii) $Y = \overline{\overline{AB} + ABC} + A\,(B + \overline{AB})$

(c) Using K map simplify the following function : 5

$f(a, b, c, d) = \Sigma\,(0, 1, 6, 8, 9, 12, 13) + \Sigma_d\,(4, 10, 14)$

P. T. O.

Or

2. (a) Realise the function

$$Y = (A + C)(A + \overline{D})(A + B + \overline{C})$$

using NOR gates. 5

(b) Realise the function $Y = \overline{AB} + A + \overline{(B + C)}$ using NAND gates. 5

(c) Find the minimal sum of products for the Boolean expression $f = \Sigma$ (1, 2, 3, 7, 8, 9, 10, 11, 14, 15) using the Quine-McCluskey method. 10

Unit – II

3. (a) Explain the working of 4-bit serial adder/substractor. 10

(b) Implement the function F (A, B, C, D) = Σ (0, 1, 3, 4, 8, 9, 15) using multiplexers. 10

Or

4. (a) Explain the look ahead carry generator and discuss its utility in adders. 10

(b) Design a BCD to excess-3 converter with a BCD to decimal decoder and four OR gates. 10

Unit – III

5. (a) Explain the working of Monostable multivibrator using 555 timer. 10

(b) Discuss the race around condition in J-K flip-flop and how it could be eliminated ? 10

Or

6. Design a MOD-12 binary counter using J-K flip-flop. 20

Unit – IV

7. (a) Explain the organisation and construction of RAM BUS ROM. 10

   (b) Design a combinational circuit that gives a binary output equal to the square of binary code decimal number 0 through 9 using diode matrix. 10

Or

8. (a) With the help of logic diagram and circuit diagram explain static RAM cell. 10

   (b) Explain the working of PAL. 10

Unit – V

9. (a) With the help of circuit diagram explain the working of HTL Nand gate. Also discuss the advantages and disadvantages of HTL family. 10

   (b) With the help of basic circuit of TTL NAND gate explain tristate output. 10

Or

10. (a) Explain the principle of IIL logic family. 10

    (b) Explain the working of NAND gate using *n*-channel MOS logic circuits. 10