d) Explain the following terms:

i) Shared-variable communication.

ii) Multiprogramming.

iii) Protected access.

OR

Briefly discuss about the followings:

i) Multiprogramming system.

ii) Time sharing system.

******

Total No. of Questions :5] *[Total No. of Printed Pages :4*

Roll No .....

MCSE-103

M.E./M.Tech., I Semester

Examination, December 2016

Advanced Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each questions are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

1. a) Explain the SIMD computer model.

b) Define the term grain size and latency.

c) Write short note on followings:

i) Hardware parallelism.

ii) Software parallelism.

d) Compare Control-flow, Data flow and reduction computers in terms of the program flow mechanism used.

OR

Describe briefly the multistage network for interconnection of multi processor.

2. a) What is instruction set?

b) What are the difference between superscalar and VLIW architecture?

c) Describe memory coherence property in a multilevel memory hierarchy.

d) What is arbitration? Explain central arbitration scheme. Also explain arbitration scheme using independent request and grants, distributed arbitration.

OR

Explain interleaved memory organization. How does it provide pipelined Allen of the parallel memory modules?

3. a) What is pipelining?

b) Prove that a K-stage linear pipeline can be at most K-times faster than that of non-pipelined serial processor.

c) Write short notes on the following:
   i) Reservation table
   ii) Latincy

d) Consider the following pipeline reservation table

	1	2	3	4
S_1	X			X
S_2		X		
S_3			X	

i) What are the forbidden latencies?

ii) Draw the state transition diagram.

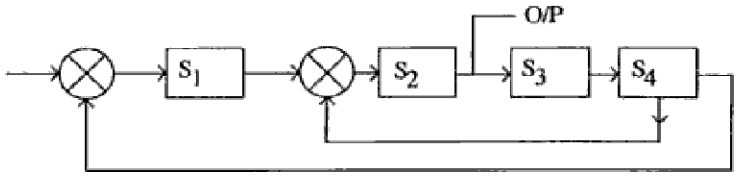
iii) List all simple cycles and greedy cycles.

iv) Determine the optimal constant latency cycle and minimal average latency.

v) Let the pipeline clock period be T=20ns. Determine the throughput of this pipeline.

OR

Consider the following pipeline processor with 4stages. All successor stages after each stage must be used in successive clock periods.



Answer the following questions:

i) Write down the reservation table.

ii) Explain Collision vectors and forbidden latencies.

iii) Explain the state diagram.

iv) Maximum throughput of this pipeline.

4. a) Discuss the concept of virtual channels

b) How Asynchronous pipelining is done in flits in a packet?

c) Give the time comparison between store and forward and wormhole routed network.

d) What is vector processing? Give some typical examples of vector processing.

OR

Compare distributed memory model and shared memory model.

5. a) Give some features of parallelism.

b) Explain logical model of parallel computer.

c) Discuss software tool types for parallel programming.