Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

MCIT-203

M.E./M.Tech., II Semester

Examination, June 2017

Advance Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) Explain an asynchronous pipeline model with appropriate diagram.
   b) Derive the equation for finding the actual speedup from pipelining.

2. a) Describe the speedup factors and the optimal number of pipeline stages for a linear pipeline unit.
   b) Discuss Flynn's classification of computer architecture.

3. a) What is hazards? Explain data hazard with examples.
   b) Discuss the superscalar and super pipelined processing. Also estimate the performance of super pipelined super scalar processor of degree (m, n).

4. a) Discuss branch handling strategies for a pipelined processor under hierarchical memory system.
   b) Briefly describe any techniques to reduce the control hazard stalls.

5. a) Describe the modular construction of butterfly switches network with 8 × 8 cross bar switches.
   b) Explain the parallel algorithm with respect to time complexity.

6. a) Give an efficient EREW algorithm to compute preorder and inorder numberings for an arbitrary tree.
   b) Explain in detail the steps of Tomasulo's algorithm assuming proper data structures.

7. a) Explain task dependencies in detail.
   b) Describe diffusion-based load balancing briefly.

8. a) What is scheduling? Explain different types of scheduling.
   b) What is dynamic scheduling? Explain with suitable examples the Tomasulo's algorithm for MIPS processor.

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