Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MEVD - 102

M.E./M. Tech., I Semester

Examination, June 2014

CMOS VLSI Design

Time : Three Hours

Max. Marks : 70

Note: i) Attempt any five questions.
ii) Assume suitable data if required.

1. a) Draw and explain the Y-chart which describes the different design methodologies for VLSI circuits.
   b) Explain any one design style of CMOS VLSI circuits. Write down its consequences which elaborates the design quality.

2 a) What do you mean by Transistor Sizing? Explain its characteristics with the help of suitable example.
   b) Elaborate the power dissipation techniques in any of the CMOS VLSI circuit with the help of suitable example.

3. a) What do you mean by Interconnects? Explain any one interconnect in detail.
   b) What do you mean by Latch up? Explain Latch up triggering and Latch up prevention technology with suitable example.

4. a) CAD technology proves to be very helping in CMOS VLSI design issues. Write down there different issues and elaborate any one.

   b) Write down the various rules which gives the final stick diagram result for any CMOS circuit.

5. a) Write down any five differences between the dynamic register element and dynamic shift register.
   b) Explain any one memory elements. How does it prove beneficial for the CMOS circuit elements?

6. a) What do you mean by PLD's? Give a brief classification of PLD's and explain each one of them.
   b) Write down the brief note on Gate Array Design and explain any one structure with the help of suitable example.

7. a) Write down the second order effects in VLSI design methodologies and explain its consequences.
   b) What are the different clocked sequential circuits? Differentiate them with suitable examples.

8. Write short notes (any four)
   i) FPGA
   ii) Sea of Gates
   iii) Inverter DC characteristics
   iv) Clocking strategies
   v) Multipliers
   vi) Adders

******