Roll No .....

EC - 404

B.E. IV Semester Examination, June 2014

Electronics Circuits

Time : Three Hours

Maximum Marks : 70

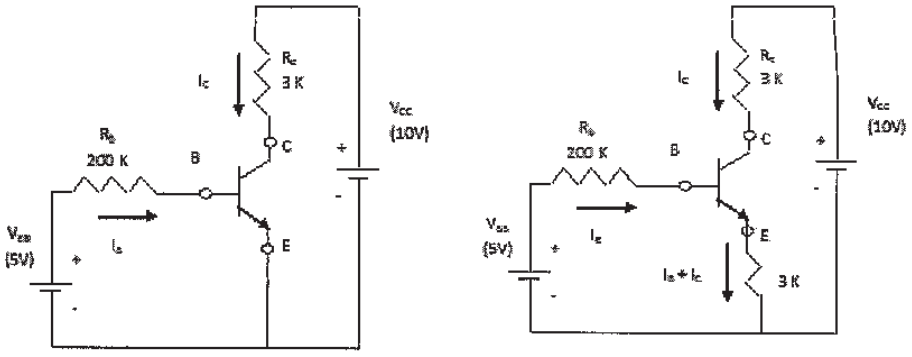
Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.
ii) All parts of each question are to be attempted at one place.
iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.
iv) Except numericals, Derivation, Design and Drawing etc.

1. a) For a p-n-p transistor in the active region, what is the sign (positive or negative) of I_E,I_C,I_B,V_{CE} and V_{EB}.

   b) Draw the circuit of transistor in the CB configuration. Sketch the output characteristics and indicate the active, saturation, and cuttoff region.

   c) Explain the base-width modulation (the Early effect) with the aid of plots of potential and minority concentration throughout the base region.

   d) Find the transistor currents in the circuit (a) as shown below. A silicon transistor with β=100 and $I_{CO} = 2\times10^{-5}$ mA is under consideration. (b) Repeat part a if 2-K emitter resistor is added to the circuit as shown in figure (b) as shown below.



OR

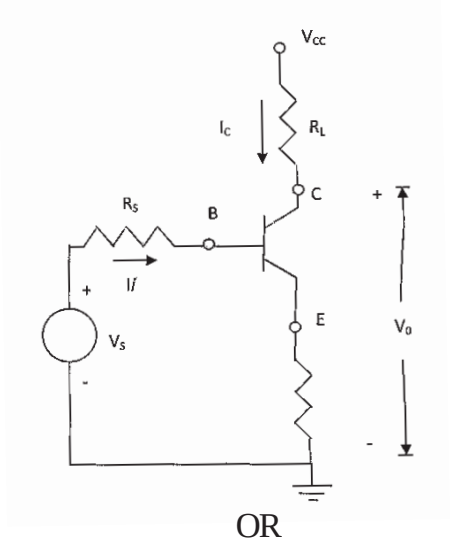
Explain the Ebers-Moll model. Write the Ebers and Moll equations. Sketch the circuit model and satisfy these equations.

2. a) Define Negative feedback. What are its advantages?

   b) What are the three conditions that must be satisfied for the feedback network?

   c) Define desensitivity D. For large values of D, what is the gain with feedback A_f? What is the significance of this result?

d) The circuit given below is to have an overall trans-conductance gain of -1 mA/V, a voltage gain of -4, and desensitivity of 50. If R_S = 1 K, h_{fe} = 150, and r_{bb} is negligible. Find (i) R_e (ii) R_L (iii) R_{if} and (iv) quiescent collector current I_C at room temperature.



OR

i) Explain and sketch the circuit of Wien bridge oscillator. What determines the frequency of oscillation and derive it.

ii) Will oscillations take place if the bridge is balance? Explain

3. a) Define intermodulation distortion.

b) Explain why even harmonics are not present in a push-pull amplifier.

c) Draw the diagram of transformer-coupled single-transistor output stage and explain the need for impedance matching.

d) For a class B transformer-coupled amplifier, write equations for dc input power to the output stage, ac power delivered to the transformer primary, and circuit efficiency. Show that the maximum theoretical efficiency of a class B amplifier is 78.6%.

OR

A class B transformer-coupled amplifier is to supply 4W to 16 Ω load. The available supply voltage is VCC=30 V. Specify the output tranformer and the output transistor. Assume a transformer efficiency of 80%.

4. a) Why is R_e (emitter resistance) in an emitter-coupled DIFF AMP replaced by a constant-current source?

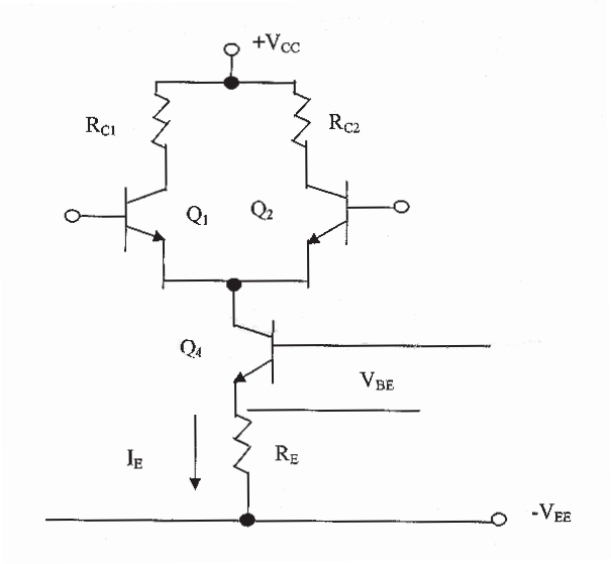
b) Explain why the CMRR is infinite if a true constant-current source is used in a symmetrical emitter-coupled DIFF AMP.

c) What will be the effect on the bandwidth, if the amplifiers are arranged in cascaded. Justify your answer.

d) Draw and explain the working of boot strapped Darlington circuit. Deduce the equivalent circuit of it.

OR

The differential amplifier shown in figure below has $R_{C1} = R_{C2} = 10k\Omega$ and $R_E = 3.9k\Omega$. The supply voltage V_{CC} is ± 12 V, and the voltage at the base of Q_4 is –3.5V. If the bases of Q_1 and Q_2 are grounded, calculate the voltages at the collector of Q_1 and Q_2. Assume that the Q_1 and Q_2 are perfectly matched and that for each transistor, $V_{BE} = 0.7V$.



5. a) Define and explain the Power Supply Rejection Ratio with reference to OP-AMP.

   b) Explain how to measure Open-Loop Differential Voltage Gain (A_V) in OP-AMP.

   c) Explain the balancing arrangement for an inverting OP-AMP.

   d) Sketch an Operational amplifier Schmitt trigger circuit. Explain the circuit operation, and sketch the input/output characteristics. Write an equation for the trigger voltage.

OR

Design a non-inverting amplifier circuit using a 741 operational amplifier. The output voltage is to be approximately 2V when the input is 50mV.

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