

MEVD-103

M.E./M.Tech. (First Semester)

EXAMINATION, Dec 2011

(Grading/Non-Grading)

ADVANCED LOGIC DESIGN

Time: Three Hours

Maximum Marks: GS:70

**Note:** Attempt any five questions.

1. (a) Write verilog code to implement the function:  
 $f(x_1, x_2, x_3) = \sum m(0, 1, 3, 4, 5, 6)$   
using the continuous assignment.  
(b) Implement the following logic function using three 2:1 multiplexers and one 2 input OR gate, assuming that variables, logic level high and logic level low are directly available as input:  $F(A, B, C, D) = (A \cdot B) + (B' \cdot C) + D$
2. (a) Derive a CMOS complex gate for the logic function  $f = xy + xz + yz$ . Use as few transistors as possible.  
(b) Define Disjoint decomposition and Non-disjoint decomposition. Using functional decomposition realize an Exclusive-Nor (XNOR) logic using four NOR gates.
3. (a) Explain the following verilog operators with examples:
  - i. Shift
  - ii. Concatention
  - iii. Logical
  - iv. Reduction  
(b) A 4bit parallel shift register has I/O pins as shown in fig.1. Write the module definition for this module shift register. Include the list of ports and port declarations.

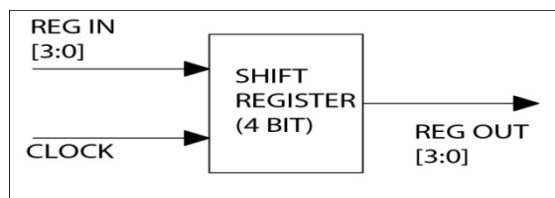


Fig. 1

4. (a) Write verilog code for an 8 to 3 binary encoder.  
(b) Using gate level modeling, write the verilog description for a full adder described as below:



Fig.2

5. (a) Show a circuit that implements the gated SR latch using NAND gates only.  
(b) Write verilog code that represents a module 10 up counter with synchronous reset.
6. (a) Explain and differentiate Mealy type and Moore type finite state machines.  
(b) Explain the following terms:
- Metastability
  - Noise margin
  - Power dissipation
  - Fan out
  - Fan in
7. (a) Describe static and dynamic hazard. Boolean function of a combinational circuit is given as
- $$F(x_1, x_2, x_3) = (x_1 + x_2')(x_2 + x_3)$$
- Which static hazard is present in the circuit
  - For what values of  $x_1$ ,  $x_2$  and  $x_3$  the hazard will occur
  - Form the hazard free circuit
- (b) Design a two input, two output synchronous sequential circuit which produces an output  $z=1$ . Whenever any of the following input sequences occur: 1100 1010 or 1001  
The circuit resets to its initial state after a 1 output has been generated. Form the state diagram of Mealy type FSM.
8. Write short notes on any two of the following:
- Programmable logic devices
  - Model sim
  - Karnaugh maps
  - Time simulation/scheduler
  - Asynchronous sequential circuit design