Roll No .....

MEVD - 102

M.E./M.Tech., I Semester

Examination, December 2014

CMOS VLSI Design

Time : Three Hours

Maximum Marks :70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each questions are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.

iv) Except numericals. Derivation, Design and Drawing etc.

Unit - I

1. a) Write an introductory note on VLSI Design flow.
   b) Explain the concept of design quality.
   c) Explain the second order effects. Draw and explain the sub threshold region.
   d) Draw and explain the graphical derivation of CMOS inverter characteristic.

   Or

   Draw and explain the CMOS inverter noise margin. Explain its characteristics.

Unit - II

2. a) Explain the parasitic effects in Integrated circuits.
   b) Derive an expression for channel resistance in voltage current characteristics of MOS transistor.
   c) Explain the concept of capacitance estimation in MOS systems.
   d) Draw and explain the accumulation, depletion and inversion function of V_{gs} in MOS capacitor characteristics.

   Or

Explain the concept of Power Dissipation. Explain the difference between static and dynamic dissipation. Derive its expressions.

Unit - III

3. a) What do you mean by Interconnect?
   b) Write and explain all circuit elements.
   c) Write down different design rules for layout circuit.
   d) Explain the principle of Latch up. Discuss about its physical origin, its triggering and its prevention methods.

   Or

   Give an introductory note on CAD Tools. How this tool is beneficial for designing MOS circuits?

Unit - IV

4. a) Discuss the designing of combinational logic parity generator.
   b) Write and explain different types of code generators.
   c) Give an introductory note on dynamic register element. Give its applications also.
   d) Explain the designing of ALU subsystem. What is its significances in a circuit? Explain with a suitable example.

   Or

   Discuss the designing of clocked sequential circuits. Explain the principle of two phase clocking. Explain it with a suitable example.

Unit - V

5. a) Explain the evolution of Programmable Logic Devices.
   b) Is there any difference between the designing of PLA and PAL? Explain.
   c) Explain FPGA. Write its applications. What is the role of FPGA in field designing?
   d) Explain the chip layout architecture of Sea of gates. Explain the wired structure which together showing routes over unused transistors.

   Or

   Write the differences between the SPLD's, CPLD's and FPGA.

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