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EE/EX-4003 (CBGS)

B.E. IV Semester

Examination, May 2018

Choice Based Grading System (CBGS)

Digital Electronics Logic Design

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions.

ii) All questions carry equal marks.

1. a) Convert the following:
   i) $(0.828125)_{10} = (?)_2$
   ii) $(18.6)_9 = (?)_{11}$
   iii) $(234)_{10} = (?)_8$
   iv) $(AF.16C)_{16} = (?)_8$
   v) $(4163)_{10} + (7520)_8 = (?)_2$

   b) Explain error detecting and correcting codes with examples. rgpvonline.com

2. a) Implement $f(x, y, z) = \sum m\,(0, 3, 4, 5, 7)$ in NAND logic.

   b) Design a 32101 multiplexer using 8 to 1 multiplexers having an active LOW ENABLE input and a 2-to-4 decoder.

3. a) Explain how to convert serial data to parallel and parallel data to serial using shift registers.

   b) Realize D and T flip flops using JK flip flops.

4. a) Design a 3-bit synchronous up/down modulo 5 counter.

   b With neat sketch, explain the operation of a 3-bit universal shift register.

5. a) What is memory expansion? Explain.

   b) Design a 3×8 decoder and implement it using a suitable PLA.

6. a) Design a magnitude comparator to compare two 3-bit numbers:
   $A = A_2 A_1 A_0$ and $B = B_2 B_1 B_0$

   b) Design a 3×3 Binary (array) multiplier.

7. a) State and prove De-morgen's theorem.

   b) Minimize the following function using K-map:
   $f(A, B, C, D, E) = \sum m\,(1, 3, 5, 8, 9, 11, 15) + d\,(2, 13)$

8. Write short notes on any two :
   a) PLA
   b) Synchronous MOD-6 counter
   c) FPGA

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