Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

MCA-104

M.C.A. I Semester

Examination, November 2018

Computer Organization and Assembly Language Programming

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) What is a Multiplexer? Give block diagram, truth table and logic diagram of a 4×1 multiplexer.
   b) Draw the logic diagram of RS Flip-flop along with its characteristic table and excitation table. Explain various state transitions.

2. a) Simplify the following expression using Karnaugh map in sum of the products form:

   $F(A,B,C,D) = \Sigma(1,3,5,7,9,11,13,15)$

   Also draw the logic circuit for the simplified expression.
   b) What do you mean by MOD counter? Write the steps and design a MOD 10 counter.

3. a) Explain the hardware implementation of 4-bit arithmetic circuit which can perform all the arithmetic micro-operations.
   b) What are the various categories of micro operations? Explain with suitable examples.

4. a) What is DMA controller? Explain how it transfers the data in a computer system.
   b) List all the methods of data transfer. What is program Controlled I/O system? Explain with the help of diagram.

5. a) Explain the instruction set of 8086 in Assembly Language programming. Define the loops and comparisons with example.
   b) Define the Pin diagram of 8086 with the help of suitable diagram.

6. a) Explain the 8086 microprocessor addressing modes with the help of an example.
   b) A memory has a capacity of 1024×8 bit.
      i) How many data input and data output lines does it have?
      ii) How many address lines does it have?
      iii) What is its Capacity in bytes?

7. a) Define the concept of cache memory. Name all the memory mapping methods. Explain direct mapping method.
   b) Explain the difference between the following:
      i) Static and Dynamic RAM
      ii) Auxiliary memory and Associative memory

8. Define the following terms:
   a) Seek time
   b) Latency time
   c) Hit ratio in cache
   d) Memory hierarchy

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