Roll No .....

MEMT-104

M.E./M.Tech., I Semester

Examination, December 2014

Advanced Digital Circuit and PLC

Time : Three Hours

Maximum Marks : 70

Note: Attempt any five questions. All questions carry equal marks.

1. a) With the help of block diagram explain the working principle of Mealy and Moore machine.
   b) Discuss about the capabilities and limitations of finite state machine.

2. The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x_1 changes from 0 to 1 while $x_2 = 1$. The output is to change from 1 to 0 only when x_1 changes from 1 to 0 while $x_2 = 1$.
   a) Find a minimum row reduced flow table. The output should be fast and flicker-free.
   b) Show a valid assignment and write a set of (static) hazard-free excitation and output equations.

3. a) Explain about Races and cycles in state assignment in asynchronous sequential circuits.
   b) With the help of example synthesis a synchronous system and represent through VHDL language.

4. Explain about the digital system implementation using algorithms state machine concept.

5. a) Explain about the semiconductor memories and PLA.
   b) Discuss about the PLA based control unit design.

6. a) Discuss briefly about high speed computational hardware.
   b) Discuss the testing methods of digital hardware.

7. Discuss the application of PLC in control rooms of power plants.

8. Write short notes on any two of the following:
   a) Clocking and control
   b) PAL and Gate array
   c) Fault tolerance

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