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## MEMT - 104
### M.E./M. Tech., I Semester
Examination, June 2014
### Advance Digital Circuit and PLC

*Time : Three Hours*

*Max. Marks : 70*

*Note:* i)　Attempt any five questions.

ii)　All questions carry equal marks.

1. a)　Classify and explain types of finite state machine.

   b)　Discuss the concept of combinational output process using Moore concept. Also design this FSM in VHDL.

2. a)　Represent asynchronous system through VHDL.

   b)　Design a 4 bit asynchronous clock down counter (Moore) in VHDL.

3. a)　With a suitable example explain the VHDL implementation of Mealy machine.

   b)　Give the VHDL implementation of waveform generator.

4. a)　Discuss the concept of algorithmic state machine.

   b)　Discuss briefly about register -transfer level design.

5. a)　With the help of logical internal structure of RAM explain the bit storage in it.

   b)　Classify and explain the principle of bit storage in different types of ROM.

6. a)　Explain about PAL and Gate array.

   b)　Discuss the working of micro programmed control unit.

7. Give the application of PLC in control rooms of process plants and power plants.

8. Write short notes on the following:

   a)　PLA

   b)　Fault tolerance

   c)　Testing of digital hardware

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