Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

EI/IC-701 (GS)

B.E. VII Semester

Examination, December 2017

Grading System (GS)

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Answer any five questions.
ii) All questions carry equal marks.

1. a) Draw and explain nMOS transistor demonstrating cutoff, linear and saturation regions of operation.
   b) Design a 3 input minority gate using CMOS NAND's, NOR's and inverters.

2. a) Explain simple MOS capacitance models.
   b) Explain complementary CMOS inverter DC characteristic.

3. a) Define Body Effect and does the body effect of a process limit the number of transistors that can be placed in series in a CMOS gate at low frequencies.
   b) Explain the working of BiCMOS inverter also enlist its merits and demerits.

4. a) Explain twin tube CMOS technology.
   b) An *n* well process has thin oxide, *n* well and *n* plus mask layers, in addition to the other regular layers. Draw the mask combination to obtain an *n*-transistor contact, a *p*-transistor contact, a V_{DD} contact and a V_{SS} contact.

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5. a) Enlist set of lambda rules for a p-well process and an SOI process.
   b) Draw and explain the switching characteristic of CMOS Inverter.

6. a) Elaborate switching performance of the pseudo nMOS inverter.
   b) Briefly explain the components that establish the amount of power dissipated in a CMOS circuit.

7. a) Explain designing strategies for CMOS circuit.
   b) Discuss exiting programmable gate array.

8. Write Short Notes on (any two) :
   a) BICMOS Inverter
   b) PMOS enhancement transistor
   c) Capacitance Estimation.

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