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Roll No. .....

EX–403(N)

B. E. (Fourth Semester) EXAMINATION, June, 2010

(New Scheme)

(Electrical & Electronics Engg. Branch)

DIGITAL ELECTRONICS LOGIC DESIGN – I

[EX–403(N)]

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) (i) Differentiate between Binary and BCD code. 4
   (ii) Convert 010110 in binary to gray. 2
   (iii) Use 2's complement to subtract 72532 – 03250. 4
   (b) (i) Using K map → F = Σ (0, 1, 2, 6, 8, 9, 10). 3
   (ii) What do you understand by negative logic ? Explain. 3
   (iii) Explain parity generators and parity checkers. 4

Or

2. (a) Prove that : 6
   (i) $x + x = x$
   (ii) $x \cdot x = x$
   (iii) $x + 1 = 1$
   (iv) $x \cdot 0 = 0$

   (v) Convert to POS form $F(x, y, z) = \Sigma(1, 3, 7)$. 2
   (vi) Implement $F = xy + \bar{x}\bar{y} + \bar{y}z$ using OR and NOT gates only. 2
   (b) Using tabulation method, simplify the Boolean function F = Σ (0, 1, 2, 8, 10, 11, 14, 15). 10

3. (a) Explain a BCD adder and obtain its block diagram. 10
   (b) What is a multiplexer ? Explain implement :
   $F(A, B, C, D) = \Sigma\ (1, 3, 5, 7, 9, 11, 13)$
   using a multiplexer. 10

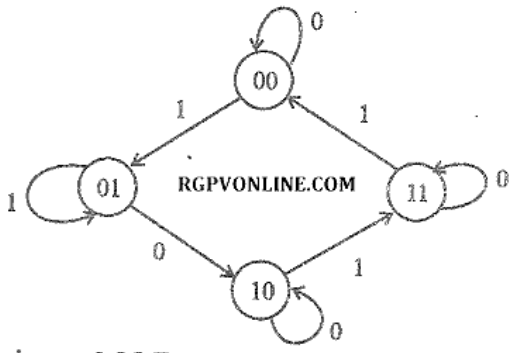
Or

4. (a) (i) Construct a 5 × 32 decoder with four 3 × 8 decoder/demultiplexer and a 2 × 4 decoder. Use block diagram construction. 5
   (ii) Explain a 2 bit magnitude comparator. 5
   (b) (i) A combinational circuit is defined by means of equation :
   $F_1(x, y) = \Sigma(0, 3)$, $F_2(x, y) = \Sigma(1, 2, 3)$
   Implement it using decoder and external NAND gates. 6
   (ii) Obtain NAND implementation of : 4
   $F = (A + \bar{B} + D)(\bar{A} + B + \bar{D})(C + D)(\bar{C} + \bar{D})$
   Assume inputs are available in complemented and uncomplemented form.

5. (a) Explain JK flip-flop. Obtain its truth table, characteristic equation and excitation table. What is the disadvantage of JK flip-flop ? 10
   (b) Define the following and explain : 10
   (i) State diagram
   (ii) State equation
   (iii) State reduction
   (iv) State assignment

Or

6. Design a clocked sequential circuit for the state diagram in figure. Use JK flip-flop. 20



7. (a) Obtain a MOD-5 ripple counter using JK flip-flop. Also give the waveforms at the output of each flip-flop. 10

(b) Explain Johnson counter. 10

Or

8. (a) Design a synchronous counter that counts in strict binary sequence 1, 3, 5, 7 using T flip-flops. 10

(b) Explain D flip-flop. What is the difference between a D latch and a D flip-flop ? 10

9. (a) Explain R/2R digital to analog converter. 10

(b) What is PAL ? Explain. Name some PAL devices. 10

Or

10. (a) Obtain a combinational circuit implementation with ROM of the equations : 10

$$F_1 (A_1, A_0) = \Sigma (1, 2, 3)$$

$$F_2 (A_1, A_0) = \Sigma (0, 2)$$

(b) Explain successive approximation analog to digital converter. 10