Total No. of Questions :8] *[Total No. of Printed Pages :2*

 Roll No .....

CS - 605

B.E. VI Semester

Examination, June 2017

Advance Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions.
ii) All questions carry equal marks.

1. What do you understand by the performance of the pipeline? What are the measures used for measuring the program.

2. What is data parallel architecture? How it is important in uniprocessor and multiprocessor architecture?

3. Explain the inclusion property and memory coherence requirements in a multilevel memory hierarchy. Distinguish between write through and write back policies in maintaining coherence in adjacent levels.

4. Explain the following terms associated with cache and memory architectures.
   a) Low order Memory Interleaving
   b) Physical address cache versus virtual address cache.

5. What do you understand by the performance of the pipeline? What are the measures used for measuring the program.

6. Explain in detail the various pipeline hazards and methods to overcome.

7. Explain how thread level parallelism within a processor can be exploited? With suitable diagrams, explain simultaneous multithreading, its design challenges and potential performance enhancement.

8. Answer any four of the following:
   a) Define the various parallel processing levels?
   b) Explain the difference between super scalar and VLIW architecture in terms of hardware and software requirements.
   c) Write a short note on multifunction arithmetic pipelines.
   d) Explain the term gather, scatter and masking instructions related to vector processing.
   e) What is the language features for parallelism?
   f) What do you mean by tuple space model of parallel programming? Write a Linda program for any task graph you assume.

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