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EE/EX-226

B.E. IV Semester

Examination, June 2017

Choice Based Credit System (CBCS)

Digital Electronics Logic Design

Time : Three Hours

Maximum Marks : 60

Note: i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) Calculate A + B, A − B, A × B and A ÷ B for the following pairs of a members.
   i) 10101, 1011
   ii) 372, 156
   iii) 2CF3, 2B
   iv) 1000, 777
   b) Draw logic implementation of an inverter using two-input NOR.

2. a) Design a 4-bit decimal adder using 4-bit binary address.
   b) Implement the full subtractor using demultiplexer.

3. a) Explain the operation of master slave flip-flop and show how the race around condition is eliminated.
   b) Explain the operation of JK flip-flop with neat diagram.

4. Design a 3-bit synchronous counter using D-flip-flop.

5. Implement the following Boolean function using 8 × 1 multiplexers
   $F(A, B, C, D) = \Sigma (1, 3, 4, 11, 12, 13, 14, 15)$

6. a) Explain the principle working of sample and hold circuits.
   b) Design a NAND gate using CMOS logic and explain its working.

7. a) Design a 4-bit Johnson counter.
   b) What is ROM? Explain the meaning of (32 × 8) ROM and describe it.

8. Write a short notes on any two of the following:
   a) PLA
   b) V-F counter
   c) Decoding glitches

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