Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MCIT-203

M.E./M.Tech., II Semester

Examination, December 2016

Advance Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note : Attempt any five questions. All questions carry equal marks.

1. a) With state diagrams, explain the transmission diagram for a pipeline unit.
   b) Explain delayed branch scheme to reduce pipeline branch penalties.

2. a) Explain the features of nonlinear pipeline processors with feed forward and feed backward connections.
   b) Explain how hardware supports for exposing more parallelism at compile time?

3. a) What is hazards? Explain structural hazards with examples.
   b) Explain possible data hazards with its resolving techniques.

4. Consider a binary integer multiply pipeline with five stages. If the stages delays are $Z_1 = Z_2 = Z_3 = Z_4 =$ gons $Z_5 =$ zons and the latch delay is zons then
   a) Determine the maximal clock rate of the pipe line.
   b) What is the maximum throughput of this pipeline in terms of the number of 36-bit results generated per seconds.

5. a) Give an O(logn)-time EREW algorithm to perform the prefix computation on an array x [1..... n].
   b) Explain a loop based example using Tomasulo's algorithm.

6. The following overlayed reservation table corresponds to a two-function pipeline :

	1	2	3	4	5
S_1	A	B		A	B
S_2		A		B	A
S_3	B		AB		

   a) List all four cross forbidden lists of latencies and corresponding cross collision. Matrices.
   b) Draw the state diagram for the two-functional pipeline.

7. a) What is DAG scheduling? Explain in detail.
   b) What is synchronisation? Explain multiprocessors synchronisation techniques.

8. Explain different types of multiprocessor based on different operating systems.

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