Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

EC-605 (GS)

B.E. VI Semester

Examination, May 2018

Grading System (GS)

VLSI Circuits and Systems

Time : Three Hours

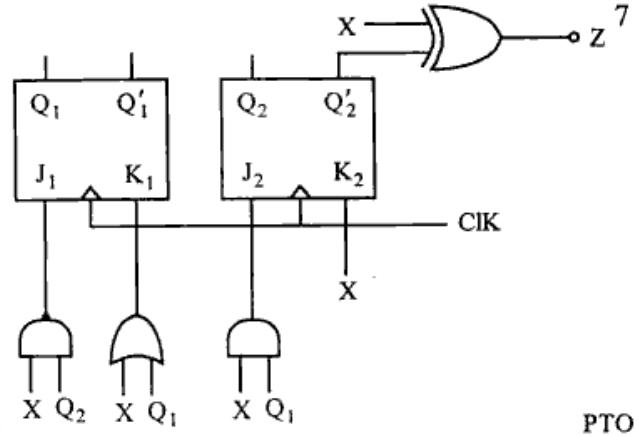
Maximum Marks : 70

Note: i) Attempt any five questions.
ii) All questions carry equal marks.
iii) Assume any missing data.

1. a) What do you know about the following domain elaborate in a proper fashion. 7
   i) Behavioural domain
   ii) Structural domain
   iii) Geometrical layout domain
   b) Implement following digital function using CMOS gate
   i) $Y = a+bc'$
   ii) $Y = (a+b) \cdot (c+d) \cdot e'$

   7

2. a) Construct a stable table and graph for the given network. 7



   b) Define a "strongly connected sequential machine" and illustrate the same with example. 7

3. a) Find the hazard free realization of the following function
   $F(A, B, C, D) = \Sigma_m (0, 2, 6, 7, 8, 10, 12, 13)$ 7
   b) Boolean expression for the circuit is given by following equations. 7

   $Y_1 = x_1' x_2 + x_2 y_1$

   $Y_2 = x_1 y_2 + x_2$

   find flow table for the circuit.

4. a) How an SM chart can be realize by using a MUX and PLA. 7
   b) Draw the ASM chart of a sequence recognizer to recognize the input sequence of pairs $xy = 11, 01, 11, 00$. 7

5. a) Design a Binary to Gray code converter using 7
   i) PROM ii) PLA iii) PAL
   b) How ROM's can be used to implement combinational circuits? 7

6. a) Explain the basic principles of the path-sensitization method. 7
   b) Differentiate between struck-at-zero and struck-at-one fault. 7

7. a) Explain the state assignments using partitions. 7
   b) Design a sequence detectors which produces a output '1' on 10010 sequence, otherwise zero output. 7

8. Briefly explain the following. 14
   a) Inflammation Loss-less machines
   b) FPGA technologies
   c) Test Vector

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