Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No.....

MEVD-102

M.E./M.Tech. I Semester

Examination, December 2017

CMOS VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Answer any five questions.
ii) All questions carry equal marks.

1. a) Discuss about Regularity, Modularity and Locality.
   b) Discuss about VLSI packaging technology.

2. a) Discuss about MOS device design equations and second order effects.
   b) Design an inverter with complementary MOS and explain its DC characteristic.

3. a) Explain Resistance, Inductance and Capacitance estimation.
   b) Explain CMOS Gate transistor sizing.

4. a) Discuss CMOS logic structures.
   b) Discuss layout design rules.

5. a) Explain Latch up triggering and latch up prevention.
   b) Discuss about structured design of combinational logic parity generator.

6. a) Discuss about designing multiplexer and code converters.
   b) Discuss designing of ALU sub-system.

7. a) Discuss about user programmable switch technology.
   b) Discuss about programmable logic structures.

8. Write short notes on any two of the following:
   a) Clocking strategies
   b) CAD
   c) Gate array design

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