Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MEVD - 103

M.E./M.Tech., I Semester

Examination, June 2016

Advanced Logic Design

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) Write down the advantages of programmable logic devices. Also discuss their classification.
   b) What do you mean by canonical representation? Explain with a suitable example.

2. a) Discuss the steps involved in verilog implementation.
   b) Draw simplified circuit diagram of EX-OR gate using NMOS, NAND gate.

3. a) List the different circuit issues associated with verilog implementation.
   b) Design a CMOS NOR gate and discuss its working principle using 2 inputs.

4. a) Write a verilog code for full adder.
   b) Define briefly:
      i) Noise margin
      ii) Metastability concept
      iii) Clock skew

5. a) What do you understand by shift registers? Also discuss about SISO. Give the list of applications of shift registers.
   b) What is the difference between level and edge triggered? Which one we should use in verilog implementation and why?

6. a) Drive a CMOS design for logic function $f = (x + y).(y + z).(x + z)$. Restrict your number of transistors.
   b) What is FSM? Explain with a suitable example.

7. a) Write the differences between Mealy and Moore representations, along with their block diagrams.
   b) Differentiate between synchronous and asynchronous circuit design.

8. Write short notes on any two:
   i) Simulator/scheduler
   ii) Verilog behavioral models
   iii) Verilog data types and operators
   iv) Hazards and glitches

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