MEVD-103

M.E./M.Tech., I Semester

Examination, December 2014

Advanced Logic Design

Time : Three Hours

Maximum Marks :70

Note : 1. Attempt any five questions out of eight questions.

2. All questions carry equal marks.

3. Assume suitable data, if required.

1. a) For V_{IH}=4V, V_{OH}=4.5V, V_{LL}=1V, V_{OL}=0.3V and V_{DD}=5V, calculate the noise margins of NM_H, and NM_L.

   b) Consider an eight input NAND gate built using NMOS technology. If the voltage drop across each transistor is 0.1V, what is V_{OL}? What is the corresponding NM_L using the other parameters from part (a).

2. a) Draw and explain the circuit diagram, simplified circuit diagram and graphical symbols of NOT gate built using NMOS technology.

   b) Draw and explain the circuit diagram, simplified circuit diagram, graphical symbols and truth table of NMOS realization of a NOR gate.

3. a) Explain the Karnaugh Map using literal, implicant and prime implicant with the help of a suitable example.

   b) A four variable logic function that is equal to 1 if any three or all four of its variables are equal to 1 is called a majority function. Design a minimum cost SOP circuit that implements this majority function.

4. a) Determine the number of gates needed to implement an eight bit carry look ahead adder, assuming no fan in constraints. Use AND, OR and XOR gates with any number of inputs.

   b) Design a circuit that generates the 9's complement of a BCD digit. Note that the 9's complement of d is 9-d.

5. a) SR flip flop is a flip flop that has set and rest inputs like a gated SR latch. Show how SR flip flop can be constructed using a D flip flop and other logic gates.

   b) Show how a JK flip flop can be constructed using a T flip flop and other logic gates.

6. a) Write verilog code that represents a T flip flop with an asynchronous clear input. Use behavioral code, rather than structural code.

   b) Write verilog code that represents a modulo 12 up counter with synchronous reset.

7. a) What do you mean by metastability state? Explain with a suitable example.

   b) Design a counter that counts pulses on line w and displays the count in the sequence 0, 2, 1, 3, 0, 2 Use D flip flop in your circuit.

8. Derive a minimal state table for an FSM that acts as a three bit parity generator. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates the parity bit p = 1 if and only if the number of 1 s in the three bit sequence is odd.