No. of Questions : 8] *[Total No. of Printed Pages : 3*

Roll No.....

MEVD-103

M.E./M.Tech. I Semester

Examination, December 2017

Advanced Logic Design

Time : Three Hours

Maximum Marks : 70

Note: i) Answer any five questions.

ii) All questions carry equal marks.

1. a) Design the minimum-cost product-of-sums expression for the function

$f(x_1, x_2, x_3, x_4) = \sum m\ (0, 2, 4, 5, 6, 7, 8, 10, 12, 14, 15)$

b) Find the simplest realization of the function

$f(x_1, \ldots, x_4) = \sum m\ (0, 3, 4, 7, 9, 10, 13, 14)$, assuming that the logic gates have a maximum fan-in of two.

2. a) Use functional decomposition to find the best implementation of the function

$f(x_1,..., x_5) = \Sigma m\ (1,2,7,9,10,18,19,25,31) + D\ (0,15,20,26)$

193 How does your implementation compare with the lowest-cost SOP implementation? Give the costs.

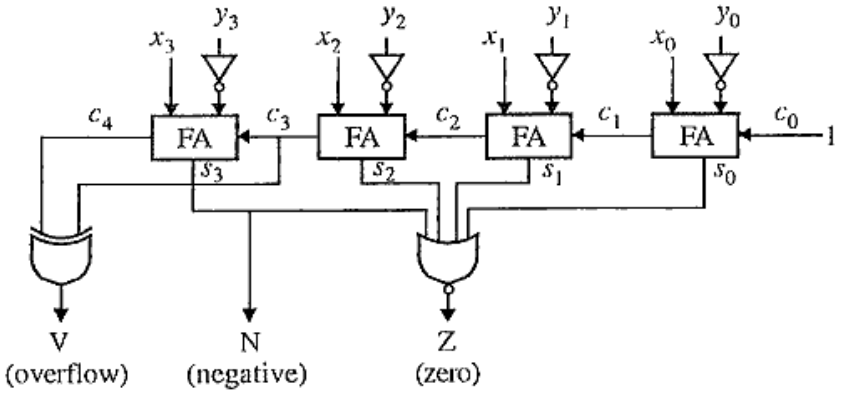
b) Show that the following distributive-like rules is valid:

3. a) Prove the validity of the expression Overflow $= c_n \oplus c_{n-1}$ for addition of n-bit signed numbers.

b) Determine the number of gates needed to implement an eight-bit carry-lookahead adder assuming that the maximum fan-in for the gates is four.

4. a) Prove that the XOR operation is associative, which means that $x_i \oplus (y_i \oplus z_i) = (x_i \oplus y_i) \oplus z_i$.

b) Write Verilog code to specify the circuit in Figure (Comparator Circuit) 4.1



5. a) Implement the function

$f(w_1, w_2, w_3, w_4, w_5) = \overline{w}_1\overline{w}_2\overline{w}_4\overline{w}_5 + w_1w_2 + w_1w_3 + w_1w_4 + w_3w_4w_5$ by using a 4-to-1 multiplexer and as few other gates as possible. Assume that only the uncomplemented inputs w_1, w_2, w_3, w_4 and w_5 are available.

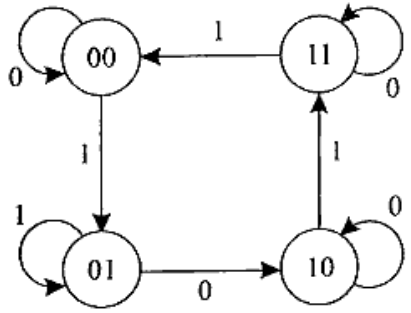
b) Write Verilog code for a 4-to-2 binary encoder.

[3]

6. a) A universal shift register can shift in both the left-to-right and right-to-left directions, and it has parallel-load capability. Draw a circuit for such a shift register.

   b) Derive the state diagram for an FSM that has an input w and an output z. The machine has to generate $z = 1$ when the previous four values of w were 1001 or 1111; otherwise, $z = 0$. Overlapping input patterns are allowed.

7. a) Design a synchronous sequential circuit whose state diagram is shown in Figure. The type of flip-flop to be use is J-K.



   b) Design a clocked synchronous state machine with two inputs, X and Y and one output, Z. The output should be 1 if the number of 1 input on X and Y since reset is a multiple of 4 and 0 otherwise.

8. a) Derive a hazard-free minimum-cost SOP implementation for the function

$$f(x_1,\ldots,x_5) = \sum m(2,3,14,17,19,25,26,30) + D\ (10,23,27,31).$$

   b) Explain the metastability problem and its solution.