Total No of Question :8] [Total No of Printed Pages:1]

MEVD-203 A

ME/M.Tech (Second Semester) MEVD EXAMINATION, July/August, 2008

VLSI Test & Testability

Time: Three Hours
Maximum Marks:100
Minimum Pass Marks: 40

Note: Attempt any Five Questions. All questions carry equal marks.

Q.1a) Explain the VLSI design flow using Gajsiki Y-Chart.
b) Explain the different types of faults and failure.

Q.2a) What is stuck-at-fault? How do you model them.
b) Explain different levels of testing. Also discuss design for testability.

Q.3a) Explain the different parameters used in Reliability modeling.
b) How the CAD tools can help in modeling and simulation of digital circuits.

Q.4a) Explain the design and testing of circuits using Boolean algebra's.
b) What is Automatic test pattern generation? Explain using stuck at fault in a combinational circuits.

Q.5a) Explain the D-algorithm for test generation. Also explain in the working of D-algorithm using an example.
b) Explain the testing of sequential circuits as iterative combinational circuits.

Q.6a) Describe full and partial scan design for sequential circuits.
b) Explain Ad-hoc testable design techniques.

Q.7a) Describe IDDQ testing method to detect fabrication defects.
b) Explain BIST? Describe logic BIST random and weighted random pattern testability.

Q.8 Write short notes on any four
a) Delay modeling
b) Event driven simulation
c) Gate level modeling
d) Fault collapsing
e) Controllability and observability
f) State table verification

----------XXX----------