EI - 602

B.E. VI Semester

Examination, June 2015

VLSI Technology

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each questions are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

1. a) Write and explain the x-ray lithography techniques. Also give its advantages and Disadvantages.
   b) What are steps involved in twin-tub process?
   c) Explain p-well process.
   d) Explain the crystal growing approach by czochralski process.

   OR

   Explain the wafer sort and masking.

2. a) Give the basic process of IC fabrication.
   b) What are the various silicon wafer preparation?
   c) Explain different types of oxidation.
   d) What is metalization? Explain briefly and what kind of material is best suited for metalization?

   OR

   Explain chemical vapour deposition techniques used for deposition of poly silicon.

3. a) Explain channeling in ion implantation.
   b) What is solid state diffusion?
   c) Explain doping mechanism.
   d) Explain any one non-optical lithographic techniques used in silicon processing.

   OR

   Explain oxidation process in detail.

4. a) What is the objective of layout rules? Define Lambda rules.
   b) What are various colour coding used in stick diagram?
   c) Explain EDA tools.
   d) Design the layout of a logical unit with 2 control lines C_1, C_2 that will perform the logical operations given in table.

C_1	C_2	Function
0	0	AND
0	1	OR
1	0	XOR
1	1	XNOR

   OR

   List and briefly explain the various floor planning solution approaches. Classify each approach as to whether it is constructive or iterative.

5. a) What is latch-up?
   b) What is NVRAM?
   c) Explain carry skip adder?
   d) How can 4-bit ALU architecture be used to implement an adder?

   OR

   How the latchup can be eliminated in CMOS technology?