Total No. of Questions :8] [Total No. of Printed Pages :3

Roll No ..0191CS12MT03.

MCSE - 103

M.E./M.Tech., I Semester

Examination, June 2013

Advanced Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note: Total number of questions eight. Attempt any five questions (including all parts). Assume missing data, if any, suitably.

1. a) Describe the characteristic of the SIMD array processor. Explain masking and data routing mechanism with suitable example.

   b) For the following sequence of instructions

   i) S1 : A = B+C

   ii) S2 : B = A+E

   iii) S3 : D = A*F

   iv) S4 : G = I/F+A

   v) S5 : H = B-D

   vi) S6 if D = 3

   vii) S7 K = G * 2+I

   Form the dependence graph and apply Bernstein's condition to show the sets of instructions which can be executed in parallel.

2. a) Describe pipelined vector processing methods. Explain each of them in detail.

b) Answer the following associated with multiprocessor architecture :

i) Banyan Network and its construction.

ii) Delta network and its construction.

iii) Tightly coupled multiprocessors.

3. a) Explain the parallel bubble sort algorithm using interconnection network. Also give its time complexity to sort the elements.

b) What is instruction and arithmetic pipelining? How the following expression will be evaluated using arithmetic pipelining.

$V = B + (A*2) + A/2$.

4. a) What is a systolic array? Give primary characteristics of a systolic array.

b) What do understand by pipeline chaining and vector loops? Explain.

5. a) What are the different weak consistency models? Compare the performance of sequential consistency and weak consistency memory.

b) How can air-traffic simulation be done on a multicomputer system, using decomposition technique?

6. a) What are direct-mapping and associative caches? Discuss various cache performance issues. What is the requirement of memory interleaving? Differentiate low-order and high-order interleaving.

b) i) How many legitimate states are there in a 4x4 switch module, including both broadcast and permutations? Justify.

ii) Construct a 64-input omega network using 4x4 switch modules in multiple stages.

7. a) What are the types of operating systems used for parallel processing? How they are different from the normal OS.

b) Compute the speedup in execution of the following computation : $A \times B+C$ with chaining and without chaining, on a vector processor with two pipeline functional units, one for floating point multiply and the other for add, which are seven stages and six stages long respectively. Let us suppose that A, B and C are three vectors each of 64 elements.

8. Write short notes on any three :

a) Dynamic Interconnections

b) Bitonic merge sort

c) Data and control hazards

d) Remote procedure call

e) MIMD multiprocessor