Total No. of Questions: 10] [Total No. of Printed Pages: 5

Roll No.

CS/EC/IT-401(N)

B. E. (Fourth Semester) EXAMINATION, Dec., 2010

(New Scheme)

(Common for CS, EC & IT Engg. Branch)

COMPUTER SYSTEM ORGANIZATION

Time: Three Hours

Maximum Marks: 100

Minimum Pass Marks: 35

Note: The question paper is divided into five Units. Each Unit carries an internal choice. Attempt any one question from each Unit. Thus attempt five questions in all. All questions carry equal marks. Assume suitable data whenever necessary.

Unit-I

- 1. (i) Explain with an example, how effective address is calculated in different types of addressing modes. 6
 - (ii) Describe the major hardware functional unit of 8085 microprocessor with a neat complete functional diagram.
 - (iii) What is the difference between the two's complement representation of a number and the two's complement of a number?

P. T. O.

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- 2. (i) A machine support 16-bit instruction format. The size of address field is 4-bit. The computer uses expanding opcode technique. Calculate:
 - (a) The number of two-address instructions supported by this machine if it has n zero-address instruction and m one-address instruction.
 - (b) The number of zero-address instructions supported by this machine if it has n two-address instruction and m one-address instruction.
 - (ii) Write a program to evaluate the arithmetic statement:

$$P = \frac{(x - y + z) * (m * n - o)}{O + R * S}$$

by using:

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- (a) Two-address instructions
- (b) One-address instructions
- (c) Zero-address instructions

Unit-II

- 3. (i) Explain Booth's multiplication algorithm. Show the step-by-step multiplication process using Booth's algorithm to multiply the number (+15) and (-13) in binary.
 - (ii) What is the need of a control unit in a computer?
 What is a hardwired control unit? What are its advantages and disadvantages?

Or

4. (i) Give the flowchart for add and subtract operation of two signed 2's complement data. Explain the logic of each operation.

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(ii)	Draw and explain the circuit	t diagram of 4	-bit by 3-bit
	array multiplier.		5
(iii)	With a neat block diagr	am, explain tl	he working
	principle of micro program	sequencer.	5

Unit-III

- 5. (i) List various commands that an interface may receive from control line of the Bus.
 - (ii) Explain the process of handling an interrupt that occurs during the execution of a program, with the help of an example.
 - (iii) A DMA controller transfers 16-bits words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much the CPU be slowed down because of the DMA transfer?

Or

6. (i) Define the following:

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- (a) I/O versus Memory Bus
- (b) I/O interface
- (c) Parallel versus Serial data transfer
- (ii) Explain the different techniques used for interfacing I/O devices with 8085 processor. State the merits and demerits of each.

Unit-IV

- 7. (i) A digital computer has a memory unit of 64 K × 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words: 6
 - (a) How many bits are there in tag, index, block and word fields of the address format?

- (b) How many bits are there in each word of cache and how are they divided in to functions? Include a valid bit.
- (c) How many blocks does the cache accommodate?
- (ii) What is associative memory? Explain the concept of match-logic for associative memories.
- (iii) A computer uses RAM chips of 1024 × 1 capacity: 4
 - (a) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?
 - (b) How many chips are needed to provide a memory capacity of 16 K bytes? Explain in words how the chips are to be connected to the address bus.

Or

- 8. (i) A CPU has 32 bit memory address and 256 KB cache memory. The cache is organized as 4-way set associative cache with cache block size of 16 bytes: 10
 - (a) What is the number of sets in the cache?
 - (b) What is the size of the tag field per cache block?
 - (c) How many address bits are required to find the byte offset within a cache block?
 - (d) What is the total amount of extra memory (in bytes) required for the tag bits?
 - (ii) A virtual memory system has 6 K words of address space and 3 K words of memory space. Page references are made by CPU in the following sequence: 10

3, 2, 0, 3, 4, 1, 2, 2, 0

Find out the pages that are available at the end if the replacement algorithm used is (a) LRU (b) FIFO.

Assume the page and block size of 1 K words.

Unit-V

The same task can be processed in a six-segment pipeline with a clock cycle of 20 ns. Determine the speedup ratio of the pipeline for 200 tasks. What is the maximum speedup that can be achieved?

10 Explain various dynamic and static interconnection networks which interconnect multiprocessor systems.

A non-pipelined system takes 100 ns to process a task.

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Discuss all factors which affect the performance	of
pipelining processor based systems.	10
Explain the operation of a multiprocessor system wi	tŀ
multiport memory.	5
Explain any one vector processing method wi	th
suitable illustration.	5