RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA BHOPAL
Credit Based Grading System
Electronics & Communication Engineering, VI-Semester
EC- 6004 VLSI circuits and systems

Unit I
Introduction
Introduction to CMOS VLSI circuit, VLSI design flow, Design strategies ,Hierarachy, regularity, modularity, locality, MOS Transistor as a Switches, CMOS Logic, Combinational circuit, latches and register, Introduction of CAD Tool , Design entry, synthesis, functional simulation.

Unit II
Specification of sequential systems
Characterizing equation & definition of synchronous sequential machines. Realization of state diagram and state table from verbal description, Mealy and Moore model machines state table and transition diagram. Minimization of the state table of completely and incompletely specified sequential machines.

Unit III
Asynchronous Sequential Machine
Introduction to asynchronous sequential machine, Fundamental mode and Pulse mode asynchronous sequential machine, Secondary state assignments in asynchronous sequential machine, races and hazards.

Unit IV
State Machine
Algorithmic state machine and fundamental concept of hardware/ firmware algorithms. Controllers and data system designing.

Unit V
Fault Detection in combinational circuit

Types of faults, Fault detection using Boolean Difference and path sensitization method.
Concept of PROM, PLA, PAL, CPLD and FPGA, PALASM software applications.

Refrences:

1. Neil Weste: Principle of CMOS VLSI Design, TMH.
2. Kohavi: Switching & Finite Automata Theory, TMH.
3. Lee: Digital Circuits and Logic Design, PHI Learning..
4. Roth Jr.: Fundamentals of Logic Design, Jaico Publishing House.
5. Parag K. Lala: Fault Tolerant and Fault Testable Hardware Design, BS Publication.

LIST OF EXPERIMENTS

1. Write a Verilog/VHDL Code to implement a 4X1 MUX.- (a)Using If-Else Statement (b)Using case statement (c)Using conditional assignment statement

2. Write a Verilog/VHDL code to implement a 2-bit wide 8X1 MUX-(a) Using If-Else Statement

(b) Using case statement (C) Using conditional assignment statement

3. Write Verilog/VHDL code to implement 6-bit comparator

Write a Verilog/VHDL Code to implement a 4Bit Synchronous counter.

4. Write Verilog/VHDL programs to implement an Up/Down counter

5. Write a Verilog/VHDL Code to implement D flip-flop, using positive level triggering.

6. Write a Verilog/VHDL Code to implement D flip-flop, using negative edge triggering.

7. Write a Verilog/VHDL Code to implement JK flip-flop, using negative edge triggering.

8. Write a Verilog/VHDL Code to implement, synthesize and simulate a 4 bit shift register.

9. Write a Verilog/VHDL Code to implement 1011 non-overlapping sequence detector.

10. Write a Verilog/VHDL Code to implement 1010 overlapping sequence detector.