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Roll No

EC-6004 (CBGS)**B.E. VI Semester**

Examination, May 2018

Choice Based Grading System (CBGS)**VLSI Circuits and Systems***Time : Three Hours**Maximum Marks : 70*

- Note:** i) Attempt any five questions.
 ii) All questions carry equal marks.
 iii) Assume any missing data.

1. a) Implement 2×1 MUX using 4 CMOS transistor. 7
 b) Implement 3-inputs CMOS NAND gates and explain its operations. 7

2. a) Design a modulo-8 binary counter. Use T flip flops in your realization. 7
 b) A sequential circuit has four flip flops A, B, C, D and input x. It is described by the following state equations.

$$A(t+1) = A'B'CDx + A'B'Cx + ACDx' + AC'D'x'$$

$$B(t+1) = A$$

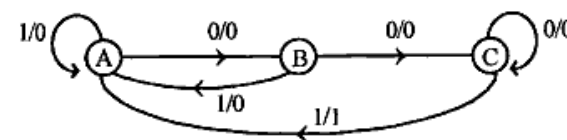
$$C(t+1) = B$$

$$D(t+1) = C$$

Design the sequential circuit described by the above state equation using J-K flip flop. 7

[2]

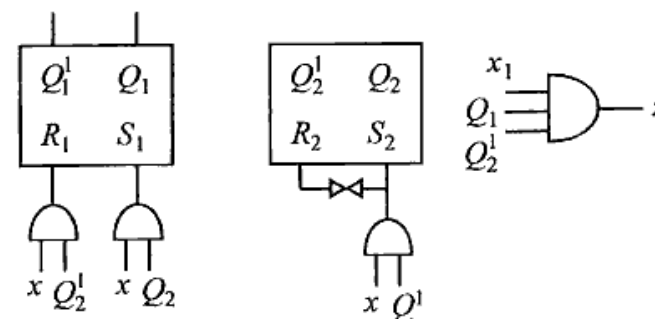
3. a) Construct the state diagram for a MOORE circuit from the following MERLY circuit. 7



- b) The function
 $f(w, x, y, z) = w'x'z' + wx'z + w'yz + wyz'$
 Can be decomposed to form $F[g(w, z), x, y]$.
 Determine the functions F and g. 7

4. a) What do you understand by minimization of incompletely specified machines. 7
 b) Describe second state assignments in sequential machine. 7

5. a) What are various ways to assign the binary values to the state variable. 7
 b) Construct a flow table for the following network. 7



[3]

6. a) Find the hazard free realization of the following function
 $F(A, B, C, D) = \Sigma_m(0, 2, 6, 7, 8, 10, 12, 13)$ 7
- b) What is the fundamental concept of hardware/firmware algorithm? Explain. 7
7. a) Draw the ASM chart for 7
- i) AND Gate
- ii) SR flip-flop
- b) Implement the following Boolean functions using a suitable PAL 7
- i) $w(A, B, C, D) = \Sigma_m(1, 3, 4, 6, 9, 11, 12, 14)$
- ii) $z(A, B, C, D) = \Sigma_m(2, 3, 8, 9, 12, 13)$
8. Write short notes on: 14
- a) GAL
- b) Fault diagnosis
- c) PLA
