Total No. of Questions : 10] [Total No. : [redacted]

Roll No. .....

MCA–104

M. C. A. (First Semester) EXAMINATION, June, 2008

COMPUTER ORGANIZATION AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : [redacted]

[redacted]

Note : Attempt one question from each unit. [redacted] carry equal marks.

[redacted]

1. (a) Define Computer [illegible] Computer Architecture. State difference [illegible] both of them. 5

(b) The state of a 12-cell register [illegible] 010011011011.

What is its content if it represent 5

(i) Three decimal digits in BCD

(ii) Three decimal digits in excess-3 code

(iii) Three decimal digits in 2, 4, 2, 1 code

(c) Explain MOD-10 counter with suitable example. 5

(d) Simplify the Boolean function F together with the don't care-conditions *d* in : 5

(i) sum-of-products

(ii) product-of-sums form

$F(w, x, y, z) = \Sigma(0, 1, 2, 3, 7, 8, 10)$

$d(w, x, y, z) = \Sigma(5, 6, 11, 15)$

P. T. O.

2. (a) What is NAND gates ? Discuss different types of gates. Also give truth table of each. 5

(b) Use the duality theorem to derive another boolean relation from . 5

$$A + \bar{A}B = A + B$$

(c) Why are applications for the half-adder limited ? What does the full adder do which makes it more useful than the half adder and what can be done with a full adder as a result of this feature ? 5

(d) Construct a 16-to-1-line multiplexer with 8-to-1-line multiplexers and one 2-to-1 multiplexer. Use block diagrams for the multiplexers

Unit – II

3. (a) What is three-state gate ? Draw and explain a bus system with the help of three-state buffers and a decoder instead of the multiplexers. 10

(b) Starting from an initial value of P. = 11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. 5

(c) Design a 4-bit combinational circuit decrementer using four full-adder circuits. 5

4. (a) Draw and explain bus system for four registers using multiplexers. 10

(b) Draw a circuit diagram and explain arithmetic logic unit (ALU) perform a micro-operations. 10

Unit – III

5. (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is : 10

   (i) direct

   (ii) immediate

   (iii) relative

   (iv) register indirect

   (v) index with R1 as the index register

   (b) Explain Execution of Instruction cycle with suitable flowchart and examples. 10

6. (a) Explain the following types of control organization : 5

   (i) Hardwired control

   (ii) Microprogrammed control

   (b) Why does DMA have priority over the CPU when both request a memory transfer ? 5

   (c) State the differences between synchronous and asynchronous serial transfer. 5

   (d) Explain the Input-Output configuration. 5

Unit – IV

7. (a) Explain the concept of segmented memory. What are its advantages ? 10

   (b) Write an assembly language program for the addition of two 3 × 3 matrices. Store the result of addition in the third list. 10

8. (a) Draw and discuss the Internal block diagram of 8086. 10

(b) Write an assembly language program to perform a one-byte BCD addition. 10

Unit – V

9. (a) An address space is specified by 24 bits and the corresponding memory space by 16 bits. 10

(i) How many words are there in the address space ?

(ii) How many words are there in the memory space ?

(iii) If a page consists of 2k words, how many pages and blocks are there in the system ?

(b) Explain how memory (RAM and ROM chips) connection is to be performed to CPU. 10

10. (a) Describe in words and by means of a block diagram how multiple matched words can be read out from an associative memory ? 10

(b) Explain the following terms into cache memory : 10

(i) Writing into cache

(ii) Write-through

(iii) Write-back

(iv) Cache initialization

Total No. of Questions : 8] [Total No. of Printed Pages : 2

MCA–104(N)

M. C. A. (First Semester) EXAMINATION, May/June, 2006

(New Scheme)

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

[MCA – 104 (N)]

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks. Use data sheet for writing opcodes.

1. (a) Implement the following Boolean functions using universal gate. Follow all the steps for final implementation :

$Y = A\overline{B} + \overline{A}B\overline{C} + AC + \overline{A}\,\overline{B}$ and

$Y = \overline{A}B + AB\overline{C}$

(b) Register R1 contents are 10110110 and R2 contents are 11001101. Write final contents of all the registers after performing the following micro operations :

(i) Shift left on R1, R2 then

(ii) Rotate left on R1, R2 then

(iii) R 3 ← R1 + R2 then

(iv) Shift Right R3

3. (a) Design synchronous mode-9 counter.

   (b) Design 4 : 16 Decoder using 2 : 4 Decoders.

4. (a) Draw and explain Register organisation of 8086.

   (b) Explain working of Master-Slave J-K flip-flop. Justify using tuning diagram.

5. (a) Draw and explain Memory Read cycle using timing diagram.

   (b) Differentiate between standard I/O and memory mapped I/O devices.

5 (a) Draw and explain Instruction format.

   (b) Write an ALD for adding first 10 odd numbers.

6. (a) Write an ALP to arrange 10 numbers in ascending order.

   (b) What do you understand by segmentation ? Write advantages of segmentation.

7. (a) Total size of Memory (RAM) is 16 KB and size of each chip is 2 K × 4. Map it with 8086.

   (b) Explain Set Associative mapping.

8. Write short notes on any *four* of the following :

   (a) Virtual Memory

   (b) Memory Refreshing

   (c) Hamming Code

   (d) Floating Point numbers

   (e) Shift left and Right Registers

   (f) Addressing Modes

Total No. of Questions : 8] [Total No. of Printed Pages : 3

MCA–104

M. C. A. (First Semester) EXAMINATION. June, 2005

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Write the difference between a combinational circuit and sequential circuit. Design a combinational circuit which performs three bit addition. 8

   (b) Prove using boolean algebra that : 6

   $$AB + BC + \overline{A}C = AB + C\overline{A}$$

   (c) Perform the operation of the following : 6

   (i) $(110011)_2 - (100)_2$

   (ii) $(38AC)_{16} = (?)_8$

2. (a) Convert the following Gray code to Binary code 100101101. 4

   (b) Impelement the following Boolean function using a multiplexer of suitable size : 8

   $$f = \Sigma m\,(3, 4, 5, 9, 10, 11, 14)$$

(c) How a ROM is specified ? Specify the number of AND and OR Gates required to realize 64 × 5 ROM. 8

3. (a) What is micro-operations ? Show the block diagram including the logic gates that implements the statement :

$$xy' T_0 + T_1 + x' y T_2 : A \leftarrow A + 1$$

here A represent Accumulator, x and y are control signals. 10

(b) Draw and explain the block diagram of a bus organized system. 5

(c) Write the sequence of micro-operations required for instruction fetch cycle. 5

4. (a) What is the meaning of the term interrupt ? What are sequence of steps taken by the system when interrupt occures ? 8

(b) Draw and explain the block diagram of a typical I/O processor. 6

(c) Explain the general format for an instruction. 6

5. (a) Draw and explain the match logic for one word of associative memory. 8

(b) What is the difference between Horizontal and Vertical microinstructions ? 4

(c) Write and briefly explain the different page replacement policies. 8

6. (a) Explain the different addressing modes of 8086. 10

(b) Find the overflow, direction, interrupt, trap sign, zero, parity and carry flags after the execution of the following instructions : 10

MOV AH, OF H
SAHF

7. (a) Write a 8086 assembly language program to add two 16-bit numbers in CX and DX and store the result in location 0500H addressed by DI. 10

(b) Write an 8086 ALP to compute :

$$\sum_{i=1}^{100} X_i \, Y_i$$

where X_i and Y_i are signed 8-bit numbers. Assume DS is already initialized and X_i and Y_i are already stored in memory. Assume no overflow. 10

8. Write short notes on any *two* of the following : 10 each

(a) Static and Dynamic RAM

(b) Error detection and error correction codes

(c) Counters

Total No. of Questions : 8] [Total No. of Printed Pages : 6

MCA–104(N)

M. C. A. (First Semester) EXAMINATION, Dec., 2005

(New Scheme)

COMPUTER ORGANIZATION AND ASSEMBLY LANGUAGE PROGRAMMING

[MCA–104(N)]

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Perform the following conversions on unsigned numbers :
   (i) 1101 1110 0100 binary to decimal
   (ii) 0111 1001 1000 1111 binary to hexadecimal
   (iii) 3DC1 hexadecimal to decimal
   (iv) 376 decimal to hexadecimal
   (v) 413 decimal to binary

   (b) Explain with examples the following :
   (i) Floating point representation
   (ii) Floating point addition and subtraction

   (c) A digital system is to store binary numbers in a 16 bit regi r. Assuming five bits reserved for exponent and

donor-receiver pair and will output 1 if the transfusion is permissible by these rules.

To get started, note that 2 bits are needed to be able to uniquely identify each of the four blood types. Use the following table to define the blood types :

0	0	O
0	1	B
1	0	A
1	1	AB

(i) Construct a truth table for the transfusion function that represents each possible donor-receiver pair (table should have four inputs and one output).

(ii) Construct a Karnaugh map for the truth table in part (i). Make sure the Karnaugh map is clearly labelled.

(iii) Write a minimal sum-of-products expression for the function.

(iv) Draw a circuit to implement the expression from part (iii).

(b) Describe the error detecting and correcting codes giving *one* example of each.

4. Describe in detail the operation of a controlled buffer, which register, which uses D flip-flops.

5. (a) Describe in detail the internal architecture of 8086 with suitable diagram.

) What would be the contents of the register affected if each of the following instructions were executed ? Express your answers in hexadecimal.

```
mov ax, bz
mov bl, fz + 2
mov si, word ptr cz + 3
mov bh, byte ptr dz + 1
mov dl, byte ptr dz + 4
mov di, bz + 8
```

) The following data is found in an 80 × 86 assembly language program :

```
Data                    Segment
    az      db      3 dup (3)
    bz      dw      0A32Eh, 3Fh, 1000
    cz      db      'HELLO'
    dz      dd      0FA3672B0h
    ez      dw      -2
    fz      db      4, 2, 3 Ah, 11110000b, 23, 95
data        ends
```

Show exactly what is stored in each byte of this data segment. The contents of each byte should be expressed in hexadecimal. The best way to do this is to fill in the blanks of the following diagram (which represents what DEBUG would display if a memory dump were done) :

xxxx : 0000 .....

xxxx : 0000 .....

(b) Assume that the 8086 registers contain the following data :

AX = 19 (decimal), CX = 2, BH = 10 (decimal), BL = −3

What will be contents of any register changed by each of the instructions given below ? Express your answers in hex.

If the zero flag, the carry flag, the parity flag, the sign flag, and/or the overflow flag are affected by the instruction, give the new status (1 or 0) after execution. Each instruction is independent. In other words, the registers always contain the same initial values given above before execution of each instruction :

(i) ADD AX, 127

(ii) CMP CX, 3

(iii) SHR, BH, CL

(iv) SUB BH, 10

(v) TEST AL, 0Fh

(vi) XOR BH, AL

(vii) MUL CL

(viii) IDIV BL

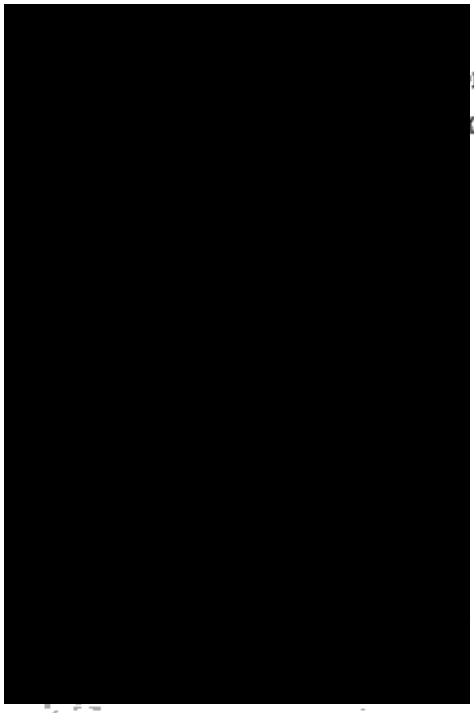
7. (a) Explain in detail the following :

(i) Microprogramming approach to generate control word

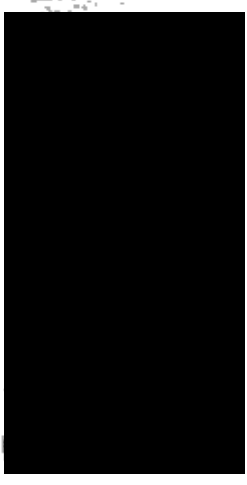
(ii) Multiplexer

(iii) Assembler directives

(b) Write an assembly program that writes the string "Hi, my name is X Y. This is my first assembly program". to the screen. Here, X is your first name, Y your last.



rinting the string, the
of the next line on the



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Total No. of Questions : 8] [Total No. of Printed Pages : 3

MCA-104(O)

M. C. A. (First Semester) EXAMINATION, Dec., 2005

(Old Scheme)

COMPUTER ORGANIZATION AND ASSEMBLY LANGUAGE PROGRAMMING

[MCA–104(O)]

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Convert the following decimal numbers to the bases indicated : 6

   (i) 7562 to octal

   (ii) 1938 to hexadecimal

   (iii) 175 to binary

   (b) Show the value of all bits of 12-bit register that hold the number equivalent to decimal 215 in (i) binary (ii) binary coded octal (iii) binary coded hexadecimal and (iv) binary coded decimal. 8

   (c) Explain multiplexers. Draw 4 to 1 line multiplexer and explain it. 6

2. (a) Explain the following terms : 10

   (i) Parity bit

P. T. O.

(ii) Parity checker

(iii) Parity generator

Derive circuits for 3-bit parity generator and 4-bit parity checker using an odd parity bit.

(b) Explain register transfer languages. Show the block diagram of hardware that implements the following register transfer statement : 10

$$T_2 : R2 \leftarrow R1, R1 \leftarrow R2$$

3. (a) The following transfer statements specify memory. Explain the memory operation in each case : 10

(i) R2 ← M [AR]

(ii) M [AR] ← R3

(iii) R5 ← M [R5]

(b) Explain the digital circuits of the following : 10

(i) Binary adder

(ii) Binary adder-subtractor

4. (a) Explain the following addressing modes with examples : 10

(i) Direct

(ii) Indirect

(iii) Relative

(iv) Indexed addressing

(v) Base register addressing mode

(b) An instruction is stored at location 300 with its address field at locations 301. The address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct

(ii) immediate (iii) relative (iv) register indirec
(v) index with R1 as index register. 1(

5. (a) Give block diagrams of typical RAM and ROM chip and explain it. 1(

(b) Describe in words and by means of block diagram how matched word can be read out from an associative memory. 10

6. (a) Explain the term interrupt. What are the sequences of steps taken by the system when interrupt occurs ? 10

(b) Explain briefly the different page replacement policies. 10

7. (a) In how many types the instruction set of 8086 can be categorised. Explain them. 10

(b) Write an 8086 Assembly language program to find the larger of two numbers. 10

8. Write short notes on any *three* of the following : 20

(i) Dynamic RAM

(ii) Gray code

(iii) Microinstructions

(iv) Virtual memory

Total No. of Questions : 8] [Total No. of Printed Pages : 3

MCA–104

M. C. A. (First Semester) EXAMINATION, Dec., 2004

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Answer any *five* questions. All questions carry equal marks. Attempt all parts of the question at one place.

1. (a) Explain 1's compliment and 2's compliment. Write an algorithm to subtract numbers using 1's compliment and 2's compliment. Also give reason which compliment is better ? 5

   (b) Generate an even parity hamming code for digits 0 to 9. 5

   (c) Simplify the following expression in (i) sum of a product and (ii) product of sum giving logic diagram in each case : 10

   $$F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$$

2. (a) What is don't care conditions in boolean functions/algebra ? Simplify the boolean function F using dont care conditions d, in sum of product :

   $$F = A'B'D' + A'CD + A'B'C'$$

   $$d = A'BC'D + ACD + AB'C'$$

P. T. O.

Also give logic diagram using NAND and NOR gates only. 10

(b) Explain the working of RS and D-flip-flops. 10

3. (a) Using truth table show that : 6

P = (P AND Q) OR (P AND (NOT Q))

(b) Explain the working of decoders and encoders with suitable block diagram. 10

(c) Explain the difference between fixed point and floating point number representation. 4

4. (a) Explain the working of data transfer between registers and memory using bus. Illustrate with a block diagram. 8

(b) Describe the working of 4-bit binary adder along with carry bit. 6

(c) Explain the different phases of instruction cycle. 6

5. (a) Explain the different types of addressing modes used in instruction set. 8

(b) Give the architecture of 8086 microprocessor. 8

(c) Explain the difference between RISC and CISC. 4

6. (a) Write an assembly language program to add two numbers and give the output to the printer (use interrupt). 10

(b) What is an interrupt ? Differentiate between interrupts and subroutine call. 5

(c) Explain the difference between FAR and NEAR procedure in assembly language programming. 5

7. (a) Define the following for a disk system : 10

(i) Seek time

(ii) Number of bits per sector

(iii) Capacity of track in bits

(iv) Latency time

Consider the disk system having 110 tracks per surface, 512 byte per sector and 96 sector per track. Find out the storage capacity of the above media for single surface and double surface.

(b) Explain the hierarchy of memory in computer system. 5

(c) What is the transfer rate for magnetic tape having 9 tracks, whose tape speed is 120 inches/sec. and tape density is 1600 bits per inch. 5

8. Write short notes on any *four* of the following : 20

(i) Isolated *vs* Memory mapped Input/Output

(ii) Direct Memory Access (DMA)

(iii) Virtual Memory

(iv) Control Unit

(v) Segment registers in 8086

(vi) Multiplexers

Total No. of Questions : 8] [Total No. of Printed Pages : 3

MCA–104

M. C. A. (First Semester) EXAMINATION, June, 2004

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks. Answers should be brief and to the point.

1. (a) Compare and contrast the following : 5, 5
   (i) Error correction code and Error detection code
   (ii) BCD number and Binary number
   (b) Formulate AND, OR, NOT, X-OR and X-NOR Gates using NOR Gates only. 10

2. (a) Reduce the following Boolean expression X using either K map or quinn McClauskey method in SOP form and draw circuit diagram using NAND-NAND logic : 10
   $X = (A + B + C + D)(A' + B' + C')(A + B)(A + B' + C')$
   (b) Design modulo seven (mod-7) ripple counter using T flip-flops. 10

3. (a) Design a micro-operation circuit with two selection variables S_0 and S_1 and two n bit data input (A and B)

P. T. O.

and one n bit output (D). Circuit gene
following six micro-operations in conjunc
input carry input (C_{in}). Draw the logic di
first two stages :

S_0	S_1	C_{in}	
0	0	X	D = Ashr A (Arithm Right)
0	1	0	D = A − B (Subtract
0	1	1	D = A + B (Additio
1	0	0	D = A and B (AND)
1	0	1	D = A or B (OR)
1	1	X	D = A (Transfer)

(b) Write the advantage of Bus Transfer over Direct Transfer. 6

4. (a) For making a program reallocable which addressing modes are suitable. Explain why. Support your answer with an example. 10

(b) Compare and contrast memory mapped I/O and Isolated I/O with special emphasis on complexity and cost issues. 10

5. (a) Explain the importance of cache memory and virtual memory. How cache memory can be actualized physically ? Explain in detail. 10

(b) What is the purpose of Interrupt cycle ? How interrupt plays an important role in systems performance ? 10

6. A computer employs RAM chips of 256 × 4 and ROM chips of 512 × 8. The computer system needs 2 k words and 2 k words of ROM and Eight interface units each with

sixteen registers. A memory mapped I/O configuration is used. Computer system is having 16 bit data bus and 16 bit addresss bus. Two highest order bits of address bus are assigned 00 for ROM, 01 for RAM and 11 for interface registers.

(a) How many RAM and ROM chips are needed ? 3, 3

(b) Draw memory address map of the system. 6

(c) Give the address Ranges in Hexadecimal for ROM, RAM and interfaces. 8

Circuit diagram not required to be drawn.

7. (a) Write 8085 Assembly language program for solving a quardetic equation in the form of $ax^2 + bx + c = 0$ consider the cases of real roots only. 15

(b) Explain the function of 'LOOPNE' instruction of 8086 assembly language with suitable example. 5

8. Write short notes on any *four* of the following : 20

(i) Decoders

(ii) Flip-flops

(iii) Instruction set

(iv) Programmed I/O transfer

(v) Basic cell of static RAM

Total No. of Questions : 8] [Total No. of Printed Pages : 4

MCA – 104

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Answer any *five* questions. All questions carry equal marks.

1. (a) Verify the De Morgan's theorem by means of truth table. Discuss the advantages and limitations of Karnaugh Map. 10

   (b) Simplify the following Boolean function in product-of-sums form by means of a four variable map. Draw the logic diagram with : 10

   (i) OR-AND gates

   (ii) NAND gates

2. (a) Explain the method to convert JK flip-flop into a D flip-flop. 6

   (b) Construct a 16-to-1 line multiplexer within two 8-to-1 line multiplexers and one 2-to-1 line multiplexer. Use block diagrams for the three multiplexers. 8

P. T. O.

(c) What is the difference between RAM and ROM ? What functions does each serve in a micro-computer system ? 6

3. (a) Derive the circuits for a 3-bit parity generator and 4-bit parity checker using an even-parity bit. 6

(b) Design a digital circuit that performs the four logic operations of exclusive-OR exclusive – NOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage. 6

(c) Starting from an initial value of R = 11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. 8

4. (a) A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts : an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. 10

(i) How many bits are there in the operation code, the register code part and address part ?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory ?

(b) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R_1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is : 10

(i) direct

(ii) immediate

(iii) relative

(iv) register indirect

(v) index

with R_1 as the index register

5 (a) What is difference between isolated I/O and memory mapped I/O ? What are the advantages and disadvantages of each ? 8

(b) What is Interrupt ? Explain the difference between software interrupt and subroutine call. 6

(c) Write a program to evaluate the arithmetic statement :

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

using a general register computer with two address instructions. 6

6. (a) What is associative memory ? Explain how is it used in address mapping in Cache memory system. 6

(b) Explain the need of auxilliary memory devices. How are they different from main memory and other peripheral devices ? 6

(c) A computer uses RAM chips of 1024 × 1 capacity.

(i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes ?

(ii) How many chips are needed to provide a memory capacity of 16 K bytes ? Explain in words how the chips are to be connected to the address bus. 8

7 (a) Give the classification of 8086 instructions. Discuss any *one* in brief. 8

P.

(b) Discuss about the active flags of a 16 bit flag register in 8086/8088. 4

(c) Write an assembly language program to multiply two 16 bit numbers in the memory. 8

8. Write short notes on any *four* of the following : 20

(a) Integer and floating point representation

(b) Counters

(c) Virtual memory

(d) Sequential circuits

(e) Address space and Memory space

(f) Registers in 8086/8088

Total No. of Questions : 8] [Total No. of Printed Pages : 3

MCA – 104

M. C. A. (First Semester) EXAMINATION, June, 2003

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks. Answers should be brief and to the point.

1. (a) Compare and contrast :
   (i) Floating point representation and fixed point representation of real numbers
   (ii) ASCII and EBCDIC
   (b) Formulate AND, OR, NOT, X-OR, X-NOR Gates using NAND Gates only.

2. (a) Reduce the following Boolean expression X using K-map in POS form and draw circuit diagram using NOR-NOR logic :

$$X = A' B' C' + ABCD + AB'CD + A' B$$

   (b) Design modulo five (mod 5) Synchronous Counter using J-K flip-flops.

P. T. O.

3. Consider Four Register (A, B, C, D) (of two bits each) Parallel Bus Transfer system with four control inputs S_0, S_1, S_2, S_3 as per the following table. Draw its circuit implementation : 6

S_0	S_1	S_2	S_3	Transfer operation	S_0	S_1	S_2	S_3	Transfer operation
0	0	0	0	A → C	1	0	0	0	B → C
0	0	0	1	C → C	1	0	0	1	D → C
0	0	1	0	A → D	1	0	1	0	B → D
0	0	1	1	C → D	1	0	1	1	D → D
0	1	0	0	A → A	1	1	0	0	B → A
0	1	0	1	C → A	1	1	0	1	D → A
0	1	1	0	A → B	1	1	1	0	B → B
0	1	1	1	C → B	1	1	1	1	D → B

(b) Describe arithmetic shift micro-operation with its overflow condition using suitable example.

4. In which particular circumstances base register mode and indexed register mode of addressing should be used ? Explain with suitable example.

(b) Explain with the help of an example, how an interrupt initiated I/O works.

5. (a) "After completion of execution cycle, fetch cycle for next instruction should be started." How this phenomenon can be controlled ? Discuss any *one* technique in detail.

(b) What is content addressable memory ? Where is it used ? Explain its uses with suitable example.

6. (a) A virtual memory system has an address space of 16 K words, a memory space of 8 K words and page and

block size of 1 K word. The following page reference changes occur during a given time interval : 15

6–9–8–3–4–12–8–12–9–10–12–8–6–14–9–14–6–3–2–12–1–10–8–9–6–13–4–9–6–2

Determine the eight pages that are resident in main memory after each Page reference change. Use either FIFO or LRU Page Replacement Algorithm.

(b) Write short note on 'Secondary Memories'. 5

7. (a) Write an 8086 assembly language program for identifying a number whether it is member of Fibonacci sequence or not. When Fibonacci sequence can be defined as :

$$x(n) = x(n-1) + x(n-2) \quad \begin{vmatrix} n > 2 \\ x(1) = 1 \\ x(2) = 1 \end{vmatrix}$$

(b) Explain the function of 'CMP' instruction of 8086 assembly language with suitable example.

8. Write short notes on any *four* of the following :

(i) Multiplexers

(ii) Registers

(iii) Instruction format

(iv) DMA transfer

(v) Basic cell of dynamic RAM

MCA–104

M. C. A. (First Semester) EXAMINATION, Dec., 2002

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) How are floating point numbers represented internally in computer ? Can it handle zero ? 6

   (b) Explain the purpose of Boolean Algebra. Simplify the following Boolean expression using Boolean Algebra rules and draw the logic diagram : 9

   $$A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + \overline{A}\,\overline{B}\,C$$

   (c) Define Parity and describe how is it used to detect an error in transmitted data. 5

2. (a) Simplify the following Boolean function in product-of-sums form by means of a four variable map. Draw the logic diagram with : 10

   (i) OR-AND gates

   (ii) NOR gates

   $$F(w, x, y, z) = \Sigma\,(2, 3, 4, 5, 6, 7, 11, 14, 15)$$

P. T. O.

(b) Design a 2-bit count-down counter. This is a sequential circuit with flip-flops and one input n. When $n = 0$, the state of flip-flops does not change. When $n = 1$, the state sequence is 11, 10, 01, 00, 11 and repeat. 6

(c) What is the difference between sequential circuits and combinational circuits ? 4

3. (a) How many 128×8 memory chips are needed to provide a memory capacity of 4096×16 ? 3

(b) What is difference between serial and parallel transfer ? Using a shift register with parallel load, explain how to convert serial input data to parallel output and parallel input data to serial output. 10

(c) Discuss various character codes. 7

4. (a) Bring out the need of having logic micro-operations in a computer system. Illustrate their use for performing following operations on the bits of a 4-bit binary register : 10

(i) Selective set

(ii) Selective clear

(iii) Selective masking

(iv) Compare and insert

(b) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. 6

(i) How many selection inputs are there in each multiplexer ?

(ii) What size of multiplexers are needed ?

(iii) How many multiplexers are there in the bus ?

(c) Represent the following conditional control statement by two register transfer statements with control functions : 4

If (P = 1) then ($R_1 \leftarrow R_2$) else if (Q = 1) then ($R_1 \leftarrow R_3$)

5. (a) Explain the following addressing modes : 8

(i) Direct addressing

(ii) Immediate addressing

(iii) Indirect addressing

(iv) Register addressing

(b) Draw a block diagram to demonstrate the interrupt cycle. What is the difference between the BSA instruction and the interrupt cycle ? Explain why the BSA instruction cannot fulfil the function of the Interrupt cycle ? 8

(c) What is the difference between I/O program controlled Transfer and DMA transfer ? 4

6. (a) Differentiate between Cache memory and Virtual memory. 6

(b) Describe in words and by means of a block diagram, how multiple matched words can be read out from an associated memory ? 8

(c) (i) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes ? 2

(ii) How many lines of the address must be used to access 2048 bytes of memory ? How many of these lines will be common to all chips ? 4

7. (a) Draw the pin diagram of 8086 microprocessor. 6

P. T. O.

(b) Explain the following instructions in assembl language programming with examples :

(i) STA

(ii) JMP

(iii) CMA

(iv) JNC

(c) Write a program in assembly language to fin maximum in a given series of data. 10

8. Write short notes on any *four* of the following . 20

(a) Decoders

(b) Types of interrupts

(c) JK master-slave flip-flop

(d) Segment register for 8086

(e) Memory Hierarchy

(f) Micro-instructions

Total No. of Questions : 8] [Total No. of Printed Pages : 4

MCA – 104

M. C. A. (First Semester) EXAMINATION, June, 2002

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA – 104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Answer any *five* questions. Parts of same question should be answered together and in the same sequence.

1. (a) Derive the circuits for a 3-bit parity generator. 8
   (b) Draw the block diagram of a dual 4-to-1-line multiplexers and explain its operation by means of function table. 4, 4
   (c) Explain ASCII and EBCDIC codes. 2, 2

2. (a) Simplify the following Boolean function in Product-of-sums forms by means of four variable map. Also draw logic diagram with (i) OR-AND gates (ii) NOR gates : 4, 3, 3

   $F(w, x, y, t) = \Sigma(2, 3, 4, 5, 6, 7, 11, 14, 15)$

   (b) Design a 2-bit count-down counter. It is a sequential circuit with two flip-flops and one input x. When $x = 0$, the state of the flip-flops does not change. When

$x = 1$, the state sequence is 11, 10, 01, 00, 11 and repeat. 10

3. (a) Starting from an initial value of R = 11011101, find the sequence of binary values in R after a logical shift-left, followed by circular shift-right, followed by a logical shift-right and a circular shift-left. 8

   (b) Following transfer statements specify a memory. Explain the memory operation in each case : 6

   (i) $R_2 \leftarrow M[AR]$

   (ii) $M[AR] \leftarrow R_3$

   (iii) $R_5 \leftarrow M[R_5]$

   (c) Show the block diagram of the hardware that implement the following register transfer statements : 6

[redacted]

4. (a) A memory unit has a capacity of 65536 words of 25-bit each. It is used in conjunction with a general purpose computer. The instruction is divided into 4 parts : an indirect mode bit, operation code, two bit specifying a processor register, and an address part. Give :

   (i) Maximum number of operations that can be incorporated in the computer if an instruction is stored in one memory word.

   (ii) The instruction format indicating the number of bits and the function of each part.

   (iii) The number of processor registers present and number of bits in each register

   (iv) Number bits in MAR, MBR and PR. 3 each

   (b) An output program resides in memory starting from address 2300. It is executed after the computer

recognise an interrupt when FGO become a 1 (while IEN = 1). 8

(i) What instruction must be placed at address 1 ?

(ii) What must be the last two instructions of the output program ?

5. (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is : 2 each

(i) direct

(ii) immediate

(iii) relative

(iv) register indirect

(v) index with R1 as index register

(b) Explain working and action of DMA interface in detail assuming suitable hardware configuration and instruction format. 10

6. (a) Explain the concept of cache memory. Discuss the various techniques for mapping data from the main memory to the cache memory. 10

(b) A digital computer has a memory unit of 64 K × 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words.

(i) How many bits are there in the tag, index, block and word fields of the address format ? 6

(ii) How many bits are there in each word of cache, and how they are divided into functions ? Include a valid bit. 3

(iii) How many block can the cache accommodate ? 1

P. T. O.

7. (a) Explain internal architecture of 8086 microprocessor. 10

   (b) Write an assembly language program to compute the average of 4 numbers stored in an array in the memory. 10

8. Discuss any *four* of the following in brief :

   (i) Associative memory

   (ii) Shift registers

   (iii) Addressing modes

   (iv) Random-Access Memory

   (v) Logic microoperations

   (vi) Handshaking

Total No. of Questions : 8] [Total No. of Printed Pages : 4

MCA–104

M. C. A. (First Semester) EXAMINATION, Dec., 2001

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE PROGRAMMING

(MCA—104)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

Note : Attempt any *five* questions out of eight. All questions carry equal marks. Attempt all parts of a question at one place.

1. (a) What is the purpose of r's compliment and $(r-1)$'s compliment ? Write an algorithm for subtraction of unsigned numbers using r's and $(r-1)$'s compliment. 5

   (b) Consider the operation of a machine in which loading the ALU input registers takes 5 n sec, running the ALU takes 10 n sec, and storing the result back in register scratch pad takes 5 n sec. What is the maximum number of millions instruction per second (MIPS) machine is capable of performing in the absence of pipelining . 5

   (c) Simplify the following expression in : 10

   (i) sum of a product

   (ii) product of sum form giving logic circuit diagram in each case :

   $$F(A, B, C, D) = \sum (2, 3, 4, 5, 6, \ldots 11, 14, 15)$$

P. T. O.

2. (a) The 8-bit registers AR, BR, CR and DR initially have the following values : 8

AR = 1111 0010

BR = 1111 1111

CR = 1011 1001

DR = 1110 1010

Determine the 8-bit values in each register after the execution of the following sequence of micro operations :

AR ← AR + BR

CR ← CR ∧ DR / * AND DR to CR *

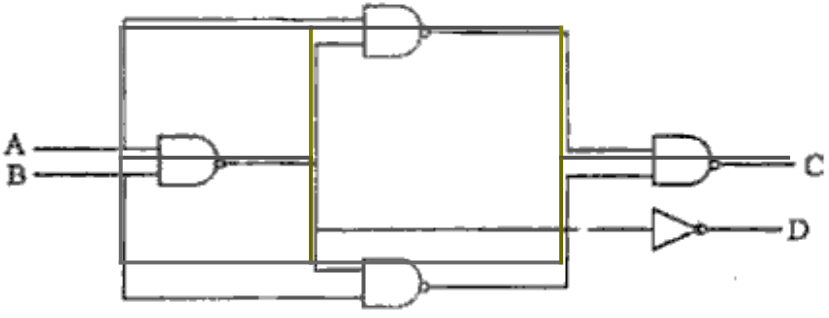
BR ← BR

AR ← AR - CR

AR ← AR ⊕ BR / * BR exclusive OR AR *

(b) Describe one-stage 2-bit hardware implementation of following logic micro-operations AND, OR, XOR and compliment. 8

(c) Explain with truth table output of the following circuit. 4



Explain half-adder and full adder. How a full adder can be converted to full subtractor ? 8

(b) Explain the working of J-K and J-K master-slave flip-flop, giving their applications. 8

(c) The contents of a 4-bits shift register is initially 1101. The register is shifted six times to the right with the serial input being 1C1101. What is the content of the register after each shift ? 4

4. (a) Explain the different types of addressing modes used in instructions. 6

(b) Give the architecture of 8086 microprocessor. What are the different types of registers and flag registers are used ? 8

(c) Write one address, two address and three address instructions to evaluate the arithmetic statement : 6

[redacted]

5. (a) Write the sequence of events and data flow when the instruction code 0110 1010 (5 A) stored in memory location 2105 h is fetched by the microprocessor. 6

(b) Explain the function of following data types :
DB, DW, DD and EQU. 6

(c) Write an assembly language program to add five numbers, 25 h, 12 h, 15 h, 1 Fh, and 2 Bh and take the average of them. 8

6. (a) Describe the hierarchy of memory in computer system. 6

(b) Explain the difference between RISC and CISC. 6

(c) Suppose a CPU has a level 1 cache and level 2 cache, with access time of 5 n sec. and 10 n sec respectively. The main memory access time is 50 n sec. If 20% of the accesses are level 1 cache hit and 60% are level 2 cache hit, what is the average access time ? 8

7. (a) Explain the concept of virtual memory. 8

(b) What are interrupts ? Explain the functions of INT 10 h, INT 21 h, and INT 33 h. 8

(c) Explain the difference between static and dynamic RAM. 4

P. T. O.

8. Write short notes on any *four* of the following : 20

(i) Error correction and detection codes

(ii) Sequential and combinational circuit

(iii) Ripple counter

(iv) Different loop instructions of assembly language

(v) Fixed point and floating point numbers

(vi) Direct Memory Access (DMA)