Total No. of Questions : 8] *[Total No. of Printed Pages : 4*

Roll No .....

CS-6001 (CBGS)

B.E. VI Semester

Examination, May 2018

Choice Based Grading System (CBGS)

Advance Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note: i) Answer any five questions, each question carries equal marks.

ii) Assume suitable data if missing.

1. a) Analyze the data dependencies among the following statements: 10

S1 : Load R1, 1024 / R1 ← 1024 /

S2 : Load R2, M(10) / R2 ← Memory(10) /

S3 : Add R1, R2 / R1 ← (R1) + (R2) /

S4 : Store M(1024), R1 / Memory(1024) ← (R1) /

S5 : Store M((R2)), 1024 / Memory(64) ← 1024 /

Note that (Ri) means that the content of register Ri and Memory (10) contains 64 initially.

i) Draw a dependence graph to show all the dependencies.

ii) Are there any resource dependencies if only one copy of each functional unit is available in the CPU?

b) Compare and comment on static and Dynamic interconnection network in terms of node degree, network diameter and bisection width. 4

2. Consider the five stage pipelined processor specified by the following reservation table: 14

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X		
S5	X					X

a) List the set of forbidden latencies and collision vector.

b) Draw a state transition diagram showing all possible initial sequences without causing a collision in the pipeline.

c) List all the simple cycles

d) Identify the greedy cycles

e) What is the MAL of this pipeline?

3. a) With respect to the mechanism for instruction pipelining explain internal data forwarding and hazards between read and write operation. 7

b) Prove that *k*-Stage linear pipeline can be at most *k* times faster than of non-pipelined serial processor. 7

4. a) Define vector processing and its instruction types. Also, explain Gather, Scatter and Masking instructions in Cray Microprocessor. 7

   b) What is Cache Coherence Protocol? Explain Goodman's write once Cache Coherence Protocol. 7

5. a) Write and explain four operational modes used in programming multiprocessor system by giving an example of each. 7

   b) Explain Store-and-forward routing. Wormhole routing and its handshaking protocol associated with message - passing mechanism. 7

6. a) Draw and explain block diagram of Back plane Bus System. Also, describe bus arbitration and control. 7

   b) Explain the temporal locality, spatial locality and sequential locality associated with program/data access in a memory hierarchy. 7

7. a) Distinguish between multiprocessors and multi computers based on their structures, resource sharing and interprocessor communication. 7

   b) What are inclusion property and memory coherence requirements? Distinguish between write through and write back policies. 7

8. Write short notes on following (Any three): 14

   a) VLIW architecture

   b) SIMD Super computer

   c) Snoopy bus Protocol

   d) Tomosulo's algorithm

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