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B. E. (Fourth Semester) EXAMINATION, June, 2009

(New Scheme)

(Common for EC, EI & BM Engg.)

ELECTRONIC CIRCUITS

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt *one* question from each Unit. All questions carry equal marks.

Unit – I

1. (a) The BJT of fig. 1, given below has the parameter :

$h_{ie} = 2000$ ohms

$h_{fe} = 100$

$h_{re} = 5 \times 10^{-4}$

$h_{oe} = 2 \cdot 5 \times 10^{-5}$ mhos

Find the voltage gain and A. C. input impedance.

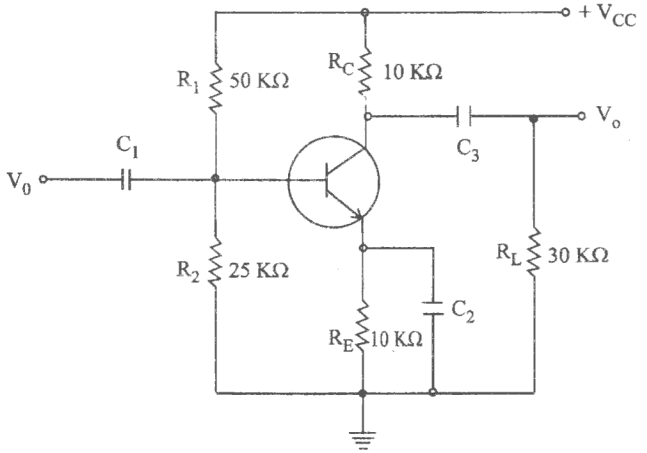

Fig. 1

P. T. O.

(b) Discuss voltage divider biasing (self bias) technique for BJT. Also give its merits and demerits.

Or

2. (a) Give low frequency *h*-parameter model of BJT and derive expressions for voltage and current gain for CE configuration.

(b) Calculate the value of collector current and collector-to-emitter voltage for the d. c. bias circuit shown in fig. 2.

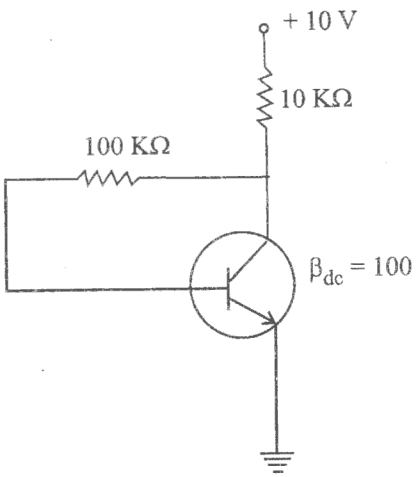

Fig. 2

Also draw the load line and locate Q-point on it. Assume $V_{BE} = 0 \cdot 7$ V.

3. (a) Discuss the principle of Negative Feedback in amplifier with a neat diagram. Derive an expression for the gain and bandwidth.

(b) An amplifier has a mid-frequency gain of 100 and a bandwidth of 200 kHz.

(i) What will be the new bandwidth and gain, if 5% negative feedback is introduced ?

(ii) What should be amount of feedback, if the bandwidth is to be restricted to 1 MHz ?

Or

4. (a) Sketch circuit of a Wien's bridge oscillator. Explain its working. Determine frequency of oscillation. Will oscillation take place, if bridge is balanced ? Explain.

   (b) Design a phase shift oscillator to operate at a frequency of 2 kHz using a JFET. Assume that $\mu = 50, A_v = 40$ and $r_d = 5\,K\,\Omega$ and the phase shift network does not load the amplifier.

   (i) Find the minimum value of R_D to be used in the drain circuit.

   (ii) Find the value of the RC product.

   (iii) Chose reasonable values of R and C to make this oscillator work satisfactory.

5. (a) Show that the maximum conversion efficiency of an idealized Class-B amplifier (push pull configuration) is 78·5%.

   (b) Draw the circuit of a push-pull amplifier stage using two transistors and explain its working.

Or

6. (a) What is meant by term cross-over distortion ? How it is reduced ?

   (b) Explain the following terms for series resonance circuit :

   (i) Q-factor

   (ii) Selectivity and Bandwidth

7. (a) Draw the circuit diagram of Darlington's amplifier. Explain it.

   (b) Write a short note on R. C. coupled amplifier.

Or

8. (a) Write short notes on the following :
   (i) CMRR
   (ii) Slew rate
   (iii) Input offset voltage
   (b) Draw bootstrapped Darlington's circuit and explain how this increases the input resistance.

9. (a) Draw and explain the working of comparator using op-amp.
   (b) Write short note on any *one* of the following :
   (i) Logarithmic amplifier
   (ii) Current-to-voltage converter

Or

10. (a) Sketch the circuit of an Integrator op-amp. and derive the expression for the output voltage, giving its applications.
   (b) Draw the circuit diagram of Schmitt trigger using op-amp. and explain its working in detail.