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Roll No. .....

CS/IT–402(GS)

B. E. (Fourth Semester) EXAMINATION, June, 2012

(Grading System)

(Common for CS & IT Engg. Branch)

COMPUTER SYSTEM ORGANIZATION

Time : Three Hours

Maximum Marks : 70

Minimum Pass Marks : 22 (D Grade)

Note : Attempt all questions. All questions carry equal marks.

1. (a) Describe the Von-Neumann model and explain the functioning of its components.

   (b) Explain and draw a diagram of a bus system that use multiplex k, register of n bits each to produce an n-line common bus.

Or

2. (a) What is instruction cycle ? Explain different phases of instruction cycle and show flow chart for instruction cycle.

   (b) Explain various addressing modes with the help of example.

3. (a) Discuss in brief microprogram control unit and hardwired control unit.

   (b) Draw and explain flowchart for addition and subtraction of floating point number.

P. T. O.

Or

4. (a) Represent the number $(+46 \cdot 5)_{10}$ as a floating point binary number with 24-bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits.

   (b) Define the following :

   (i) Micro-operation

   (ii) Microcode

   (iii) Microinstruction

   (iv) Microprogram

5. (a) Explain with suitable example the working principle of DMA controller.

   (b) What do you mean by interrupt ? Explain the various interrupt handling techniques ?

Or

6. (a) What do you mean by synchronous and asynchronous data transfer ? Explain handshaking method of asynchronous data transfer.

   (b) Explain the use of the following instructions :

   (i) DAA

   (ii) RIM

   (iii) MOV Reg, M

   (iv) PUSH D

7. (a) What is cache coherency ? Why is it necessary ? Explain different approaches for cache coherency.

   (b) Explain associative memory with its hardware organization. Discuss the procedure for reading and writing data in associative memory.

Or

8. (a) Explain in short the following :
   (i) Memory Hierarchy
   (ii) Memory Management Hardware
   (b) What is paging ? Explain how paging can be implemented in CPU to access virtual memory.

9. (a) Formulate a six segment instruction pipeline for a computer. Specify the operation to be performed in each segment.
   (b) Draw and explain the typical functional structure of a SIMD array processor.

Or

10. Explain the following terms :
   (i) Data dependency
   (ii) Pipeline conflicts
   (iii) Interprocessor communication
   (iv) Interconnection structure

Unit – V

9. (a) Solve the recurrence relation,

$$a_r + 7a_{r-1} + 9a_{r-2} = 3$$

give that $a_0 = 0$, $a_1 = 1$.

(b) By the following generating function :

$$Y(t) = \sum_{h=0}^{\infty} y_h \cdot t^h = y_0 + y_1(t) + y_2 t^2 + \ldots\ldots$$

solve $y_{n+1} - y = h$ with $y_0 = 1$.

Or

10. (a) Prove that in distributive lattice, if an element has a complement, then this complement is unique.

(b) Let L = {1, 2, 3, 4, 6, 8, 9, 12, 18, 24} be ordered by the relation '|' where x/y means 'x divides y', show that D_{24} the set of all divisors of the integer 24 of L is a sublattice of the lattice (L, |).