Roll No .....

MEDC-104

M.E./M.Tech. I Semester

Examination, December 2013

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note : 1. *Attempt any five questions.*
2. *All questions carry equal marks.*
3. *Assume and mention suitable missing data if any.*

1. a) Explain the flow for designing of integrated circuit. Discuss different hardware design methodologies.
   b) Derive an equation for drain current I_{DS}. Also explain the channel length modulation effects in MOS transistor and write the equation for I_{DS} with channel-length modulation parameter (λ).

2. a) Calculate the native threshold for an n-transistor at 300°K for a process with a Si substrate with density on carrier in doped semiconductor substrate is 1.50×10^{16} and a SiO_2 gate oxide with thickness 200°A and oxide capacitance of 1.72×10^{-7} farad/cm^2. (Assume $\phi_{ms} = -0.5$v and $\phi_{fc} = 0$).
   b) Discuss the different types of oxide related capacitance in three operating modes of MOS transistor.

3. a) Draw the switching characteristic for CMOS inverter. Also calculate the propagation delay time τ_{PHL} for a CMOS inverter.

   b) Design following logic function using BICMOS logic.
      i) $y = \overline{A(B+C)}$ ii) $y = \overline{A.B}$

4. a) Derive the expression for power delay product.
   b) Explain the working of CMOS domino logic.

5. a) Draw the architecture of field programmable gate arrays (FPGA) and explain the following.
      i) Programmable inter connects
      ii) IOB_s
      iii) CLBS
   b) Summarize the differences between a 50G chip and a standard cell chip. What benefits does each implementation style have?

6. A combinational circuit is to be designed for squaring a given 3 bit number. Implement it using PLA and PROM. Give the truth table also.

7. a) What do you mean by routing of the chip? Explain the global routing.
   b) Explain the term short circuit and open circuit faults, controllability and observability.

8. Write short note on following:
   a) Circuit level simulation
   b) RTL synthesis
   c) Netlist comparison
   d) Logic optimization

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