Roll No .....

CS - 605

B.E. VI Semester

Examination, June 2013

Advance Computer Architecture

Time : Three Hours

Maximum Marks : 70/100

Note: Attempt one question from each unit. All questions carry equal marks.

Unit - I

1. a) Explain how instruction set, compiles technology, CPU implementation and control and cache and memory hierarchy affect the CPU performance and justify the effects in terms of program length, clock rate and effective CPI.

   b) Compare data flow and control flow computers.

2. a) A 400-MHz processor executing an object code with $2x10^6$ instructions. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below.

Instruction type	CPI	instruction mix
Arithmetic & logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

i) Calculate the average CPI when the program is executed on a processor.

ii) Calculate the MIPS rate.

b) Distinguish between medium-grain and fine grain multicomputer in their architectures and programming requirements.

Unit - II

3. a) Explain the difference between superscalar and VLIW architectures in terms of hardware and software requirements.

b) Explain memory capacity planning briefly.

4. a) Describe interleaved memory organisation briefly.

b) Distinguish between scalar RISC and super scalar RISC in terms of instruction issue pipeline architecture and processor performance.

Unit - III

5. a) Consider the execution of a program of 15,000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction has five stages and that one instruction is issued per clock cycle.

i) Calculate the speed factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow through delay.

ii) What are the efficiency and through put of this pipelined processor.

b) Explain multifunctional arithmetic pipelines.

6. Consider the following reservation table for a four stage pipeline with a clockcycle T = 20ns.

	1	2	3	4	5	6
S_1	X					X
S_2		X		X		
S_3			X			
S_4				X	X	

a) What are forbidden latencies and initial collision vector?

b) Draw state transition diagram.

c) Determine greedy cycle and simple cycle.

d) Determine MAL.

Unit - IV

7. a) Explain the message routing schemes in multi computer network.

b) Describe the vector super computer architecture with block diagram.

8. a) Explain cache coherence problem and its solutions briefly.

   b) Discuss the principles of multithreading.

Unit - V

9. a) Explain shared variable and message passing model briefly.

   b) Discuss the features of parallel language.

10. Write short notes on the following :

   a) Software tools and environments.

   b) Parallel compilers.

   c) Object oriented model.

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