Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

EC-8001 (CBGS)

B.E. VIII Semester

Examination, May 2019

Choice Based Grading System (CBGS)

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data, if required.

1. a) Write and explain the classification of integrated circuits by device count.
   b) Explain the microelectronics field. Give the types of major processes used in IC fabrication.

2. a) Draw and explain the block diagram of conventional IC design process.
   b) Explain the operating principle of *n* channel MOSFET with the help of suitable regional diagrams.

3. a) Etching is used in one process step to pattern poly silicon and in a later process step to make contact openings in SiO_2 to gain top contact to residual poly silicon. Why does the contact opening etch not consume the underlying poly silicon.
   b) Explain the chart that explains the approach to device modelling.

4. a) Draw and explain the output characteristic curve for *n* channel MOSFET.
   b) What is the role of parasitic capacitors in MOS transistors for *n* channel device? Explain with suitable diagram.

5. a) Explain the sub threshold operation when MOSFET operating in weak inversion.
   b) Explain the high frequency diode model with suitable examples.

6. a) Derive a relation for quasi static register cells.
   b) What do you mean by micro coded controllers? Explain with suitable circuit diagrams.

7. a) Explain different steps involving in *n* well CMOs process.
   b) Discuss the physical origin of latch up and discuss some latch up prevention techniques.

8. Write short notes (any four)
   a) Hybrid Technology
   b) Passive Component Models
   c) BJT Noise Model
   d) Systollic Array
   e) Twin Tub Process

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