MCSE - 103

M.E./M.Tech., I Semester

Examination, December 2013

Advanced Computer Architecture

Time : Three Hours

Maximum Marks : 70

Note: Attempt one question from each unit.

Unit - I

1. a) Explain how instructions set, compiler technology CPU implementation and control and cache and memory hierarchy affect the CPU performance and justify the effects in terms of program length, clock rate and effective CPI.

   b) Describe the various shared memory multiprocessors.

2. a) Consider the execution of a program of 15,00,000 instructions by a linear pipeline processor with a clock rate of 1000MHz.

      i) Calculate the speed up factor in using pipeline as compared with an equivalent non pipelined processor.

      ii) What are the efficiency and throughout of pipelined processor.

   b) Explain handler's classification of parallel computers.

Unit - II

3. a) Discuss the benefits and limitations of static branch prediction and dynamic branch prediction.
   b) Distinguish between shared memory multiprocessor and message passing multiprocessor.

4. Explain the following terms associated with compound vector processing:
   a) Compound Vector Function.
   b) Vector loops and pipeline chaining
   c) Systolic program graphs
   d) Pipeline network or pipe nets.

Unit - III

5. a) Explain the temporal locality, spatial locality and sequential locality associated with program/data access in a memory hierarchy.
   b) Compare buses, cross has switches and multistage networks for building a multiprocessor system with n processor and n shared memory modules.

6. a) Explain the parallel algorithms for array processors.
   b) Describe in brief the structure of reorder buffer and the functions which it can and cannot perform in the process of exploiting instruction level parallelism.

Unit - IV

7. a) Explain operating system configurations for a multiprocessor computer.
   b) Describe the cache coherence protocol using distributed directories in multiprocessor.

8. a) Explain the protection schemes associated with the multiprocessor system.
   b) Distinguish between stochastic Queuing model and deterministic Queuing model.

Unit -V

9. a) Explain the following terms as applied to communication patterns in a message passing network.
      i) Unicast versus Multicast
      ii) Broadcast versus Conference
      iii) Channel band width
      iv) Communication latency
   b) What is cache coherence? Explain the various protocols of Cache Coherence.

10. Consider the following pipeline reservation table:-
    a) What are the forbidden latencies
    b) Draw the state transition diagram
    c) List all the simple cycles and greedy cycles
    d) Find minimal average latency.

	1	2	3	4
S_1	X			X
S_2		X		
S_3			X	

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