Total No. of Questions : 10] [Total No. of Printed Pages : 3

Roll No. .....

EC–403

B. E. (Fourth Semester) EXAMINATION, June, 2012

(Grading/Non-Grading)

(Electronics & Communication Engg. Branch)

DIGITAL ELECTRONICS

(EC–403)

Time : Three Hours

Maximum Marks : $\begin{cases} GS : 70 \\ NGS : 100 \end{cases}$

Note : Attempt *one* question from each Unit. All questions carry equal marks.

Unit–I

1. (a) Convert the following in the radix shown :

   (i) $(444 \cdot 456)_{10} = (\ )_8$

   (ii) $(101111 \cdot 1101)_2 = (\ )_{10}$

   (b) Express the function $Y = A + \overline{B}\,C$ in (i) canonical SOP and (ii) canonical POS from.

   (c) Simplify the expression :

   $$Y = \Sigma_m (7, 9, 10, 11, 12, 13, 14, 15)$$

   using the K-map method.

Or

2. (a) Add the following BCD numbers :

   (i) 1001 and 0100

   (ii) 00011001 and 00010100

P. T. O.

(b) Realise :

(i) $Y = A + BC\overline{D}$ using NAND gates

(ii) $Y = (A + C)(A + \overline{D})(A + B + \overline{C})$ using NOR gates

Unit – II

3. (a) Discuss the design of BCD adder.

(b) Discuss the use of MUX for generating the function :

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,D + BCD + A\overline{B}\,\overline{C} + AB\overline{C}\,D$$

Or

4. (a) With the help of circuit diagram explain the working of 4 bit parallel adder.

(b) Design a full substractor using logic gates.

Unit – III

5. (a) Design an Astable multivibrator using 555 timer and explain its working.

(b) Design a MOD-8 counter using JK flip-flop.

Or

6. (a) Explain the working of master slave JK flip-flop.

(b) Design a MOD-7 counter using T flip-flop.

Unit – IV

7. Discuss the following memories :

(a) SRAM

(b) PAL

(c) EPROM

Or

8. Discuss the following semiconductor memories :

(a) DRAM

(b) EEPROM

(c) PLA

Unit – V

9. (a) Explain the operation of emitter coupled logic.

   (b) Discuss the operation of n-channel MOS logic circuits.

Or

10. (a) Construct a circuit with TTL as a driver and CMOS as a load and explain.

    (b) Explain with the aid of a circuit diagram the operation of a TTL-3 input NAND gate.