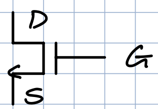
1. General Considerations

1.1 MOSFET as a Switch

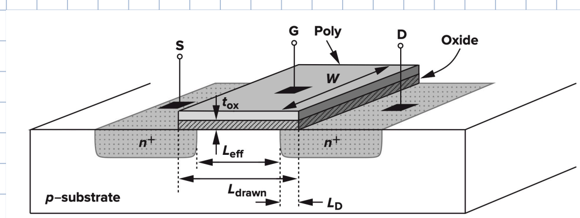


NMOS: Symmetric
S/D are interchangeable.

V_G ⟨ High: source and drain are connected. ("ON")
Low: S/D isolated ("OFF")

1. For what V_G does the NMOS turn on?
2. What is the resistance between source and drain when the NMOS is on / off?
3. How does the resistance depend on terminal voltages?

1.2 MOSFET Structure

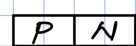


NMOS

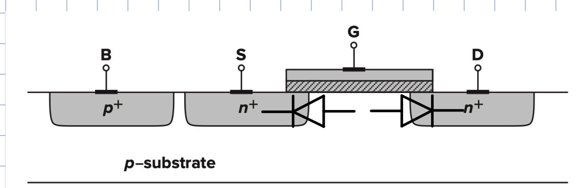
Polysilicon (poly):
Amorphous (non-crystal) silicon

Source: Provides charge carriers (electrons or holes)
Drain: Collects charge carriers

In typical operation, the S/D junction diodes must be reverse biased.



→



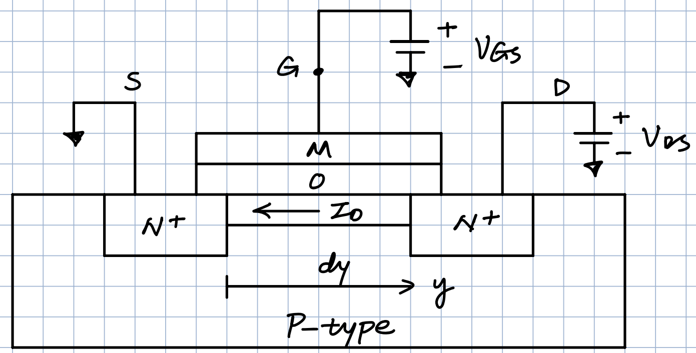
Anode —▷|— Cathode.
Reverse biase: $V_A < V_C$
Depletion region widens

→ Substrate of an NMOS is connected to the most negative supply

→ Actual connection is provided through an ohmic p^+ region

2. MOSFET I/V Characteristics

2.1 Derivation

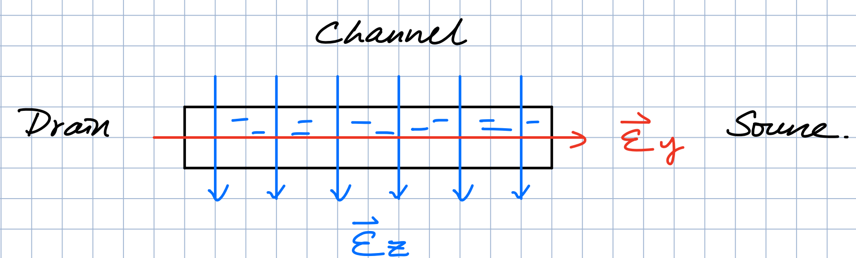


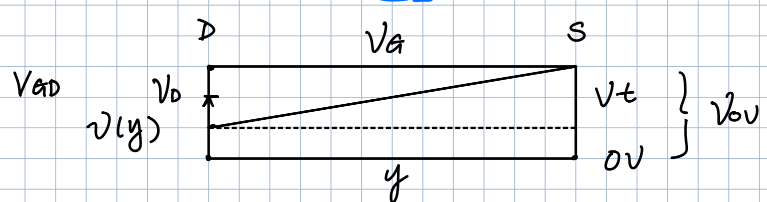
The biasing conditions are shown in the figure.

If $V_{GS} < V_t$:
→ No inversion layer (channel) exists under the gate
→ $I_{DS} = 0$

If $V_{GS} > V_t$:
→ A channel is created.
If $V_{DS} = 0$:
→ The horizontal $\mathcal{E}$ field is 0
→ $I_{DS} = 0$.

V_{GS} controls the vertical $\mathcal{E}$ field while V_{DS} controls the horizontal $\mathcal{E}$ field.
→ Field effect transistors.



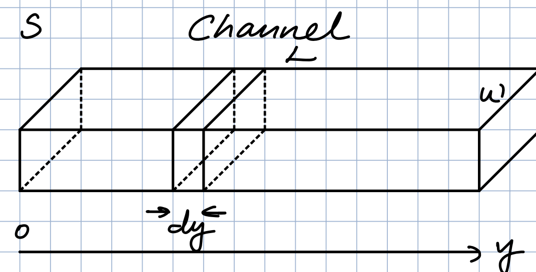


We want to find an expression for I_D.

$$I_D = \frac{dQ}{dt}$$

dQ: incremental channel charge at a distance y from the source in an incremental length dy of the channel

dt: the time needed for dQ to cross length dy.



$$dQ = Q_I \cdot W \cdot dy$$

Q_I: charge per area in the channel

Let $V(y)$ be the voltage in the channel

$$Q_I = C_{ox} \cdot [V_{GS} - V(y) - V_t]$$

Let $v_d(y)$ be the electron drift velocity.

$v_d(y) = \mu_n \cdot E(y)$ if $E(y)$, the horizontal electric field induced by V_{DS} is small.

$$dy = v_d(y)\,dt = \mu_n E(y)\,dt = \mu_n \frac{dV}{dy}\,dt.$$

$$\frac{1}{dt} = \frac{\mu_n \cdot dV}{dy^2}$$

$$I_D = \frac{dQ}{dt} = C_{ox}[V_{GS} - V(y) - V_t] \cdot W \cdot dy \cdot \frac{\mu_n \cdot dV}{dy^2}$$

$$I_D\,dy = C_{ox}[V_{GS} - V(y) - V_t] \cdot W \cdot \mu_n\,dV$$

$$\int_0^L I_D\,dy = \int_0^{V_{DS}} C_{ox}[V_{GS} - V(y) - V_t] \cdot W \cdot \mu_n\,dV$$

$$I_D \cdot L = \mu_n C_{ox} W \left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$\boxed{I_D = \mu_n C_{ox} \cdot \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]}$$

If $V_{DS} \geq V_{GS} - V_t$

→ $V_{DS} = V_{GS} + V_{DG} \geq V_{GS} - V_t$, $V_{DG} \geq -V_t$, $V_{GD} \leq V_t$

→ No inversion occurs at the drain.

→ Channel pinch-off

→ I_D becomes independent* of V_{DS}.

→ Voltage drop across the channel is $V_{GS} - V_t$.

→ MOSFE is saturated.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t)(V_{GS} - V_t) - \frac{1}{2}(V_{GS} - V_t)^2 \right]$$

$$= \boxed{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \cdot (V_{GS} - V_t)^2}$$

$V_{GS} < V_{th}$: Cutoff

$V_{GS} \geq V_{th}$: ① $V_{DS} \ll 2(V_{GS} - V_{th})$,

$$I_D \approx \mu_n C_{ox} \cdot \frac{W}{L} (V_{GS} - V_{th}) \cdot V_{DS}$$

(since $\frac{1}{2} V_{DS}^2 \ll (V_{GS} - V_{th}) \cdot V_{DS}$)

I_D is a linear function of V_{DS}

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} (V_{GS} - V_{th})} \cdot \frac{L}{W}$$

Deep triode region; MOSFET operates as a resistor

② $V_{DS} < V_{GS} - V_{th}$: Triode

③ $V_{DS} \geq V_{GS} - V_{th}$: Saturation

2.2 Transconductance (G_m)

In general. $G_m = \frac{I}{V}$ $\left(S = 1/\Omega = \frac{A}{V}\right)$

How does I_{DS} change with respect to V_{gs}, V_{DS}, V_{BS} ?

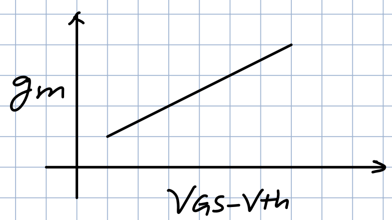
1. Gate transconductance.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2 \leftarrow \text{Saturation}$$

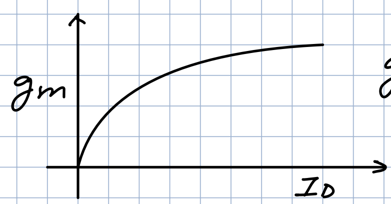
$$\boxed{g_m = \frac{\partial I_D}{\partial V_{GS}} = \left[\mu_n C_{ox}\frac{W}{L}\right](V_{GS}-V_{th}) = \frac{2I_D}{V_{GS}-V_{th}}}$$

Also, $2\mu_n C_{ox}\cdot\frac{W}{L}I_D = (\mu_n C_{ox})^2\left(\frac{W}{L}\right)^2(V_{GS}-V_{th})^2$

$$g_m = \sqrt{2\mu_n C_{ox}\cdot\frac{W}{L}\cdot I_D}$$



Constant W/L



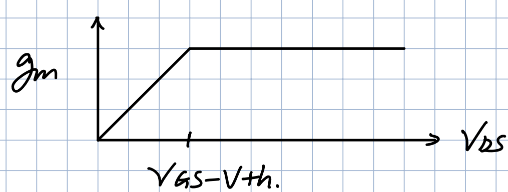
Constant W/L

Constant I_D

* $g_m = 2I_D/V_{ov}$ may be deceiving since I_D is dependent on V_{ov}.

g_m in triode region:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(2(V_{GS}-V_{th})V_{DS} - V_{DS}^2\right)\right)$$
$$= \mu_n C_{ox}\frac{W}{L}V_{DS}$$



g_m drops in the triode region
→ For amplication MOSFETs are usually kept in saturation.

2. Body transconductance

* $\beta = \mu_n C_{ox} \cdot \frac{W}{L}$

V_{th} is a function of V_{SB}

$$I_D = \frac{\beta}{2}(V_{GS} - V_{th})^2$$

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{SB}}\right)\Delta V_{SB}$$

$$\frac{\partial I_D}{\partial V_{SB}} = -\beta\left(V_{GS} - \underline{V_{th}(V_{SB})}\right)\left(\frac{\partial V_{th}}{\partial V_{SB}}\right)$$

Let $\partial V_{th} / \partial V_{SB} \equiv \eta$

$$\frac{\partial I_D}{\partial V_{SB}} = -g_m \cdot \eta = -g_{mb}$$

$$\Delta I_D = -g_{mb}\Delta V_{SB} = g_{mb}\Delta V_{BS}$$

3. Drain/source transconductance

With CLM: $I_D = \frac{1}{2}\beta(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$.

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}\beta(V_{GS} - V_{th})^2\lambda = \boxed{I_D\lambda = \frac{1}{r_o} = g_{ds}.}$$

Ideally $g_{ds} = 0$. and $r_o \propto L$.

2.3 Second-Order Effects

Channel Length Modulation (CLM)

Increasing V_{DS} in NMOS

→ Increases the width of the depletion region around the drain

→ Reduces the effective channel length in saturation

→ Causes I_{DS} to increase (since $R \propto \frac{L}{W}$ and $I = \frac{V}{R}$)

→ $\Delta I_D = \frac{\partial I_D}{\partial V_{DS}} \Delta V_{DS}$

$$\frac{\Delta V_{DS}}{\Delta I_D} = \frac{V_A}{I_D} = \frac{1}{\lambda I_D} = r_o$$, V_A: Early voltage.

Body Effect

For NMOS, if $V_B < V_S$:

→ More holes are attracted to the substrate connection

→ Creates a larger negative charge

→ Depletion region widens

→ V_{th} increases because the gate charge must mirror depletion area charge first

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - 2\sqrt{|2\phi_F|}\right)$$

The body effect can occur even when V_B is constant as V_S varies.

Subthreshold Conduction

For NMOS, if $V_D >$ ~100mV

→ For $V_{GS} < V_{th}$, some I_D still flows from drain to source.

→ I_D exhibits an exponential dependence on V_{GS}

→ $I_D = I_0 \exp\left(\frac{V_{GS}}{\xi \cdot V_T}\right)$.

$I_0 \propto \frac{W}{L}$; $\xi > 1$ (nonideality factor), $V_T = \frac{kT}{q}$

→ Weak inversion region (as opposed to $V_{GS} > V_{th}$ / strong inversion)

→ $g_m = \frac{I_D}{\xi \cdot V_T}$

→ $\frac{I_D}{\xi \cdot V_T} = \frac{2I_D}{V_{ov}}$, $V_{ov} = 2\xi V_T \approx 80mV$ if $\xi \approx 1.5$

→ Large device widths or low I_D are necessary