TSN40LPSROM

TSMC 40nm Low Power
VIA Programmable High Density
Read-Only Memory Compiler
Databook

Version 20071100_210A

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Chapter 1 : Compiler General Description

Low power VLSI technology becomes increasingly important in the growing area of electronic industry. In order to provide the solution of low power application, TSMC 40nm Low-Power VIA Programmable High Density Read-Only Memory with BIST Interface compiler is provided.

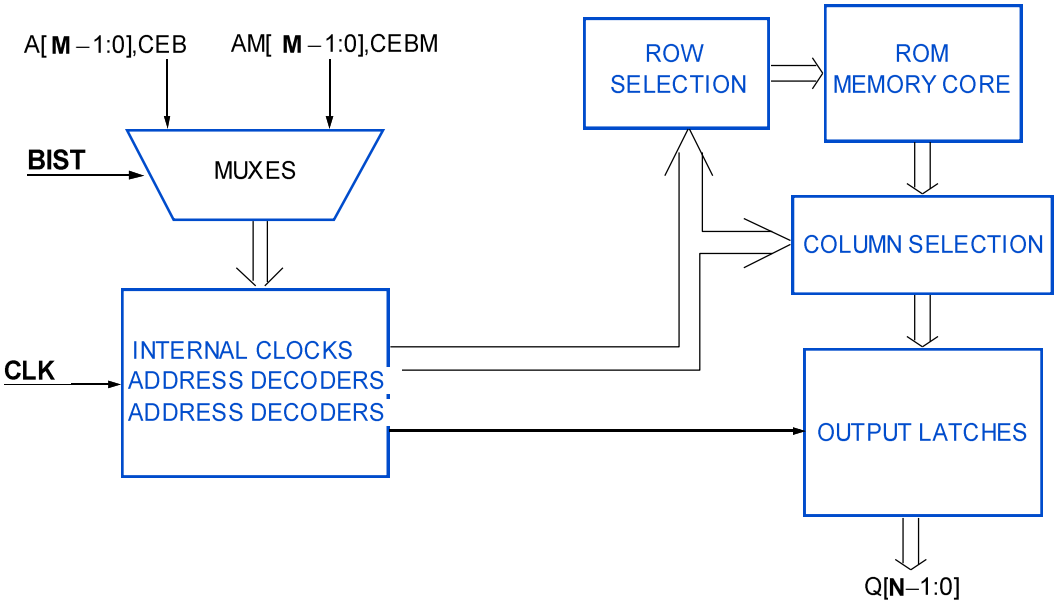
TSMC 40nm Low-Power VIA Programmable High Density Read-Only Memory with BIST Interface compiler is high performance, low power, and fabricated in TSMC CLN40LP (1.1V) CMOS low power technology. This Low Power VIA Programmable High Density ROM operates at a voltage of 1.1V +/- 10% and a junction temperature range of -40°C to 125°C. The **VIA-1** Programmable High- Density ROM can be configured up to 4096 Words by 64 Bits, 8192 Words by 32 Bits, 16384 Words by 16 Bits or 32768 Words by 8 Bits as shown in Figure 4.1. The compiled ROM file is divided into 4 groups according to their column-selected numbers (Mux=8, Mux=16, Mux=32, Mux=64). The “word depth” is defined as the number of words and the “word width” is defined as the number of bits per word.

Chapter 2 : Features

TSMC 40nm Low-Power VIA Programmable High Density Read-Only Memory with BIST Interface compiler has the following features:

- Fully synchronous
- Single-clock operation
- Low standby power
- Full address decoding
- Single mask level programmable (VIA-1)
- Near-Zero Hold Time (address, and control inputs)
- Chip Enable mode active low (CEB)
- Segmented Memory architecture for reduced power consumption
- 4 column mux options: 8, 16, 32, 64
- Up to 32768 Words and 144 Output Bits (can be configured up to 4096 Words by 64 Bits, 8192 Words by 32 Bits, 16384 Words by 16 Bits or 32768 Words by 8 Bits)
- BIST mux interface (optional)
- TSMC 1P10M 40nm CLN40LP (1.1V) CMOS process
- Standard-Vt high density design
- Support power mesh by metal 4 pins
- Route over SROM with metal 5 and above
- Limited porosity on metal 4
- Power down mode is low leakage mode to reduce leakage power by switching off part of periphery circuit.

Chapter 3 : Block Diagram



Chapter 4 : Compiler Supporting Range

40nm low-power ROM compiler is a parameterized static read-only memory function supported by automatic physical generation software. The physical layout data of the 40nm low-power ROM compiler is implemented as a custom, pitch-matched array of cells that is very area efficient.

40nm low-power ROM compiler can be customized by its number of words, **W**, and the number of bits per word, **N**. The number of address bits, **M**, is explicitly determined by the number of words. The column multiplexing (**CM**) is based on the number of words, **W**, and the number of bits per word, **N**. The number of rows is **W/CM**. The number of columns is **N*CM**. Valid and fully supported limits for the values of the configuration parameters are specified in the following table. This table is for general configuration information of word size and bits.

Mux Options	**Word Size (Address locations)**	**Bits (Number of Outputs)**
CM	**W**	**N**
8	32,64,96...4K	2,3,4...144
16	64,128,192...8k	2,3,4...72
32	128,256,384...16k	2,3,4...36
64	256,512,768...32k	2,3,4...18

Figure 4.1

According to silicon result, the following ROM configurations can **NOT** be supported in this compiler.
(1) ROM instances (**W*N**) greater than (>) 256K-bit are **NOT** supported.
(2) ROM instances (**W*N**) less than or equal to (<=) 256K-bit with the number of rows (**W/CM**) greater than or equal to (>=) 256 (rows) **and** the number of columns (**N*CM**) greater than (>) 512 (columns) are **NOT** supported.

Example of 8kx32 ROM instance, 8kx32m16 (**W/CM** > 256 & **N*CM** = 512) is **supported**, but 8kx32m32 (**W/CM** = 256 & **N*CM** > 512) is **not** supported.

- Compiler and instance naming

  ts3n40lpa{**W**}x{**N**}m{**CM**}_{version} or User defined library name: i.e. SROM

For example:

SROM cell: ts3 is designated for ROM compiler

Naming	W	N	CM	Revision
ts3n40lpa256x72m8_210a	256	72	8	210a
ts3n40lpa8192x32m16_210a	8192	32	16	210a

Chapter 5 : Pin Descriptions and Logic Truth Table

Pin Description

Pin	Type	Description
A[**M**-1:0]	Input	**Address Inputs**
CEB	Input	**Chip Enable (Active-Low)**
CLK	Input	**Clock**
AM[**M**-1:0]	Input	**BIST Address Inputs**
CEBM	Input	**BIST Chip Enable (Active-Low)**
BIST	Input	**BIST Interface Enable**
PD	Input	**Power Down (Active High)**
Q[**N**-1]	Output	**Data Outputs**

Netlist Order

Inputs: A[**M**-1:0], CEB, CLK, PD, AM[**M**-1:0], CEBM, BIST
Outputs: Q[**N**-1:0]

Logic Truth Table:

Power Down Mode

Mode	PD	Q
Power Down	**1**	**0 (tPD must be met)**
Normal	**0**	**Q (tWK must be met)**

BIST Mode

Mode	BIST	Clock	Chip Select	Address
Normal	Low	CLK	CEB	A
BIST	High	CLK	CEBM	AM

Functional

Function	CLK	CEB/CEBM	A/AM	Q[i]
Deselect	↑	High	**X**	no change
Read	↑	Low	**a**	mem[**a**][**i**]
Standby	Low	High	**Low**	no change

Note:
In a non-fully decoded array, a read cycle to a nonexistent address location causes the outputs to become unknown.

Chapter 6 : Timing Specifications

Input Timing Requirements

Symbol	Parameter	From	To
tas	Address Setup Before CLK↑	A[**M**-1:0]	CLK
tah	Address Hold After CLK↑	A[**M**-1:0]	CLK
tcs	CEB Setup Before CLK↑	CEB	CLK
tch	CEB Hold After CLK↑	CEB	CLK
tams	Address M Setup Before CLK↑	AM[**M**-1:0]	CLK
tamh	Address M Hold After CLK↑	AM[**M**-1:0]	CLK
tcms	CEBM Setup Before CLK↑	CEBM	CLK
tcmh	CEBM Hold After CLK↑	CEBM	CLK
tbists	BIST Setup Before CLK↑	BIST	CLK
tbisth	BIST Hold After CLK↑	BIST	CLK
tkh	Minimum CLK Pulse High	CLK ↑	CLK ↓
tkl	Minimum CLK Pulse Low	CLK ↓	CLK ↑
tcyc	Minimum Cycle Time	CLK ↑	CLK ↑

Switching Characteristics

Symbol	Parameter	From Input	To Output
tcd	CLK to Valid Q	CLK ↑	Q[**N**-1:0]
thold	CLK to Invalid Q	CLK ↑	Q[**N**-1:0]

Timing Diagram

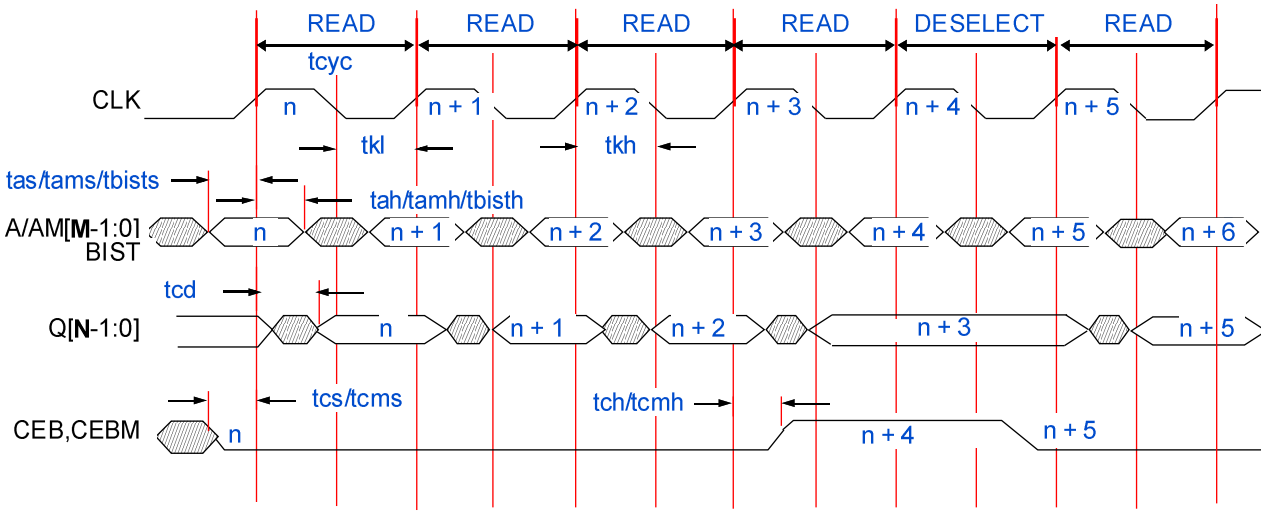


Figure 7.1 Timing Diagram

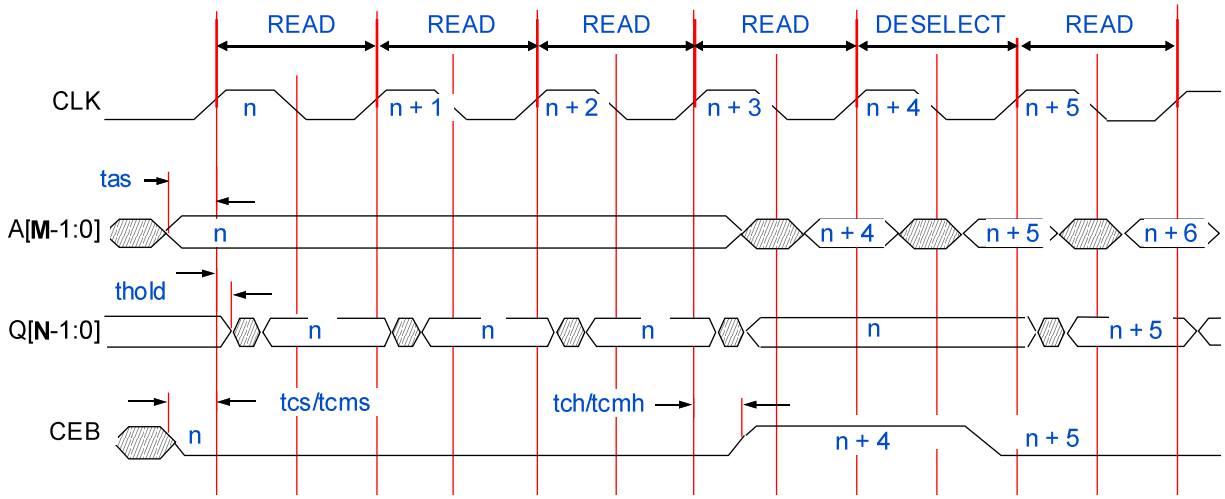


Figure 7.2 Timing Diagram

* Even if the address does not change, the output may go to an unknown state on the rising clock edge (see Figure 7.2 above). If it is desired to keep the same output data from previous cycle, regardless of the address changing or not, the Chip Enable (CEB) should go high (Standby Mode) before the rising clock edge (see Figure 7.2).

Chapter 7 : Process Voltage and Temperature (PVT) Characterization Conditions

PVT	Process	Voltage (V)	Temperature (C)	
SS0P99V125C	SS	0.99	125	Vdd-10%
SS0P99VM40C	SS	0.99	-40	Vdd-10%
SS0P99V0C	SS	0.99	0	Vdd-10%
TT1P1V125C	TT	1.10	125	Vdd
TT1P1V25C	TT	1.10	25	Vdd
FF1P21V0C	FF	1.21	0	Vdd+10%
FF1P21VM40C	FF	1.21	-40	Vdd+10%
FF1P21V125C	FF	1.21	125	Vdd+10%

Note

1. Permanent damage could occur if the operation exceeds the table listing above

Chapter 8 : Power/Ground Connection Guideline

In chip design level, users must guarantee to meet the Vccmin spec(>= Vdd-10%) at the SRAM IP boundary to avoid performance impact from voltage drop of system power.

In order to have better IR drop and EM management, please follow the power/ground connection guidelines below.

- Route M5 power lines over the SRAM instances and cover as much area as possible.
- Connect M4 VDD/VSS power lines thru via as much as possible.
- M5 power/signal lines must be placed perpendicularly to M4 and drop VIAs in full of any cross-area of two metals.

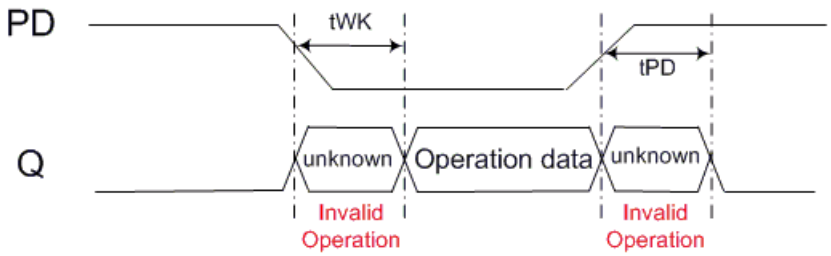
Chapter 9 : Power Down Requirements

The Power Down pin (PD) is a low leakage mode by switching off partial of periphery circuit. No read cycle may take place while PD is asserted. Also, the Q outputs will be forced to logic 0.

Also, the PD input assists in situations where it is desirable to power-down the memory entirely. If PD is held high while VDD is removed from the memory macro, the Q outputs will be held to 0 rather than allowed to float.

There are two timing constraints that need to be followed for the power down mode.

tWK : ROM wake up time. This time window defines the time to charge all the powered down power nets to the vdd level. The tWK is equivalent to eight ROM cycles. ROM operation is invalid in this time window.
tPD : Idle time. During this time window, the output Q will become unknown until after tPD, which will be pulled to logic 0. ROM operation is invalid in this time window.



- The ROM data output (Q) is logic 0 when PD is activated.
- When the values of data output (Q) changes from 0 (power down mode) to unknown-X (normal stand-by mode), there is no high-Z on output Q.

Chapter 10 : Scramble Table

There are 4 column muxes in the ROM: 8, 16, 32 and 64
The maximum number of physical rows is 1024, which requires 10 addresses.

For column mux = 8 which A0:A2 are column addresses and A3:A12 are row addresses.

For column mux = 16 which A0:A3 are column addresses and A4:A13 are row addresses.

For column mux = 32 which A0:A4 are column addresses and A5:A14 are row addresses.

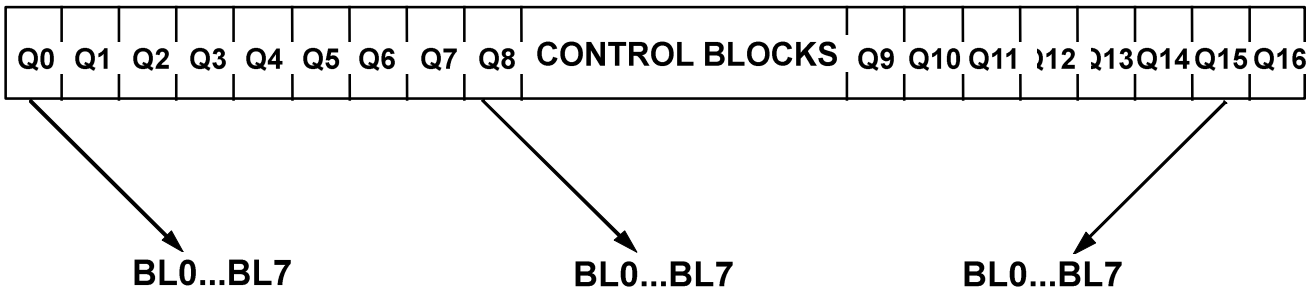
For column mux = 64 which A0:A5 are column addresses and A6:A15 are row addresses.

The column decoder is not scramble.

For the row decoder, every 8 wordlines or rows, the first 4 rows is not scramble and the next 4 rows are flipped.

The Q outputs are counted from left to right (Q0, Q1 ...Q [N-1])

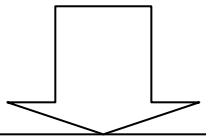
Below is the example of 17 Bits (Q [0:16]) ROM with column mux 8 ([A0:A2] are column addresses).



Physical column = 8 * n + Column address +1, n is the output number
The physical column is counted from left to right (from Q0) and start with 1
For example Q8 with column address 3 (A2=0, A1=1 & A0=1).
Physical column = 8 * 8 +3 +1 = column 68

Word line scramble

1111111100	WL1020
1111111101	WL1021
1111111110	WL1022
1111111111	WL1023
1111111011	WL1019
1111111010	WL1018
1111111001	WL1017
1111111000	WL1016
●	●
●	●
●	●
●	●
0000001100	WL12
0000001101	WL13
0000001110	WL14
0000001111	WL15
0000001011	WL11
0000001010	WL10
0000001001	WL9
0000001000	WL8
0000000100	WL4
0000000101	WL5
0000000110	WL6
0000000111	WL7
0000000011	WL3
0000000010	WL2
0000000001	WL1
0000000000	WL0



A12…….A3 for column mux 8
A13…….A4 for column mux 16
A14…….A5 for column mux 32
A15…….A6 for column mux 64

Test

The recommended test strategy in the absence of BIST circuit is to read and verify every word in the 40nm low-power ROM compiler.

Chip Enable

When Chip Enable (CEB) is low, the internal clocking is activated and the 40nm low-power ROM compiler is accessed. When CEB is high, the power is greatly reduced and the data outputs are unaffected (the data output stays the same as previous cycle).

ROM Coding

- Program “don’t care” or unused locations with “0” to save power.
- Users need to prepare intended **Intel hex** ROM code to be inputted to ROM compiler for back-end kits generation.
- A utility of ROM code generation and verification is packed with compiler.
  - Documents:
    - N40_ROM_Code_Generation_flow
    - N40_ROM_Code_Verification_flow
  - Scripts:
    - hex2intel.pl: convert hex code or verilog code to Intel hex code format
    - chk_rom_code.pl: rom code verification between spice net-list file and intended ROM code file

Chapter 12 : Quick Reference Table

Symbol	Description
Size	Memory configuration
Column	Mux number
Width	Layout width
Height	Layout height
Power	AC current
IDDQ	Standby current
tcd	Access time
tckh	Clock high
tckl	Clock low
tcyc	Cycle time
tas	Address setup time
tah	Address hold time

The timing data is based on output load 0.00156pf and the input slew for each condition is shown as below table.

Voltage	Input slew
1.21V	0.0048ns
1.1V	0.0064ns
0.99V	0.0080ns

Please reference the file: tsn40lpsrom_20071100_210a_Quick_Reference_Table.pdf