TSN40LPD242SPSRAM

TSMC 40nm Low Power Single Port
SRAM Compiler Databook

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Chapter 1 : Compiler General Description

Low power VLSI technology becomes increasingly important in the growing area of electronic industry. In order to provide the solution of low power application, TSMC 40nm low power SRAM compiler is provided.

TSMC 40nm Low Power Synchronous Single Port SRAM (LPSSP) compiler is a high performance, low power, and fabricated in TSMC CLN40LP (1.1V) CMOS low power technology. This SRAM operates at a voltage of 1.1V +/- 10% and a junction temperature range of -40°C to 125°C. The available SRAM size is configured from 1K bits to 1M bits as shown in Fig 3.1. The compiled SRAMs are divided into 3 groups according to their column-selected numbers (Mux=4, Mux=8 and Mux16). The “word depth” is defined as the number of words and the “word width” is defined as the number of bits per word.

Chapter 2 : Features

TSMC 40nm LPSSP SRAM compiler has the following features:

- TSMC 1P10M 40nm CLN40LP (1.1V) CMOS process
- Synchronous operation
- Three column-mux options can be chosen, such as 4, 8 and 16.
- High density 6T SRAM bit cell 0.36 X 0.83 = 0.299um^2 (drawing dimension) and the physical SRAM bit cell area is 0.324 X 0.747 = 0.242um^2
  MT form: HD; cell imp mask: 112(VTC_N) and 199(VTC_P)
- Over SRAM routing for metal 4 and above
- Support global EDA models and precise timing characterization data
- Near-Zero Hold Time (data, address, and control inputs)
- Bit-write (BWEB) option with each data input
- AWT (Asynchronous Write Through) pin which can be turned on or off
- Power down mode to achieve lower leakage
- BIST interface for data, address, and control inputs

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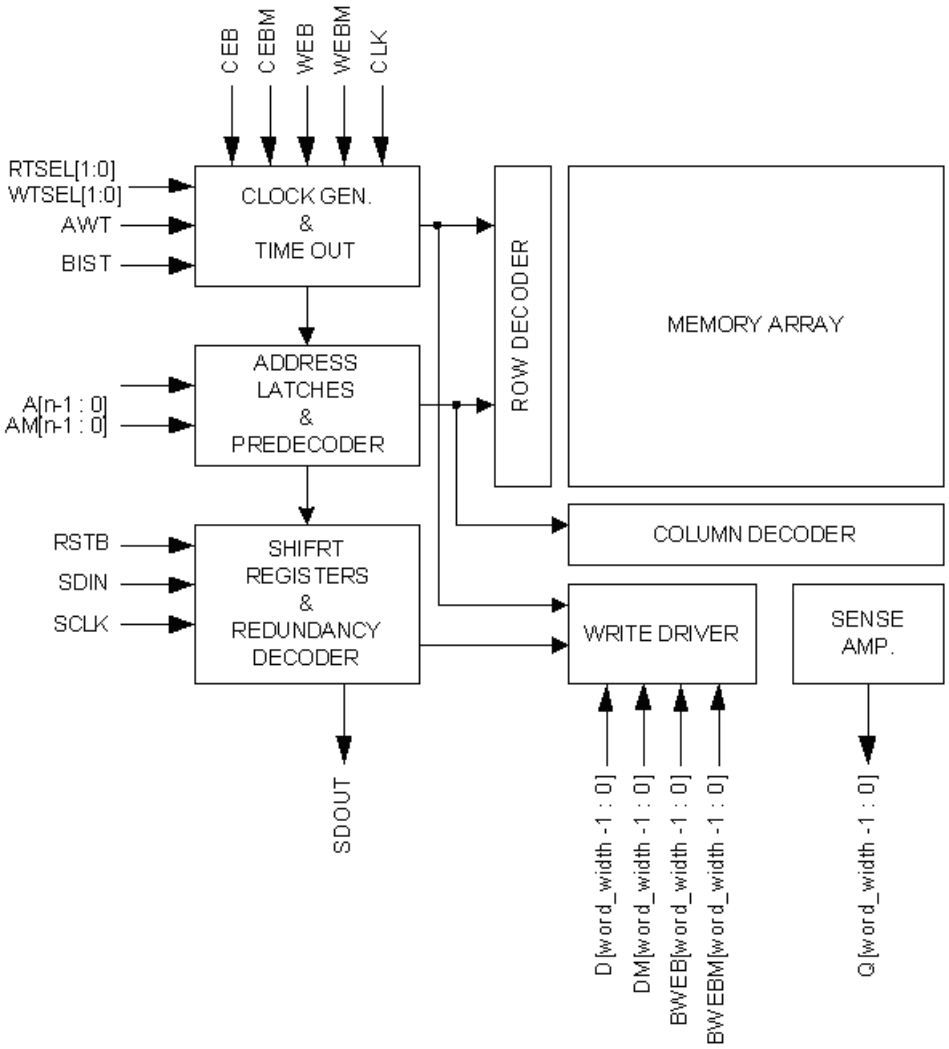

Figure2.1 block diagram (redundancy is removed in 260a release)

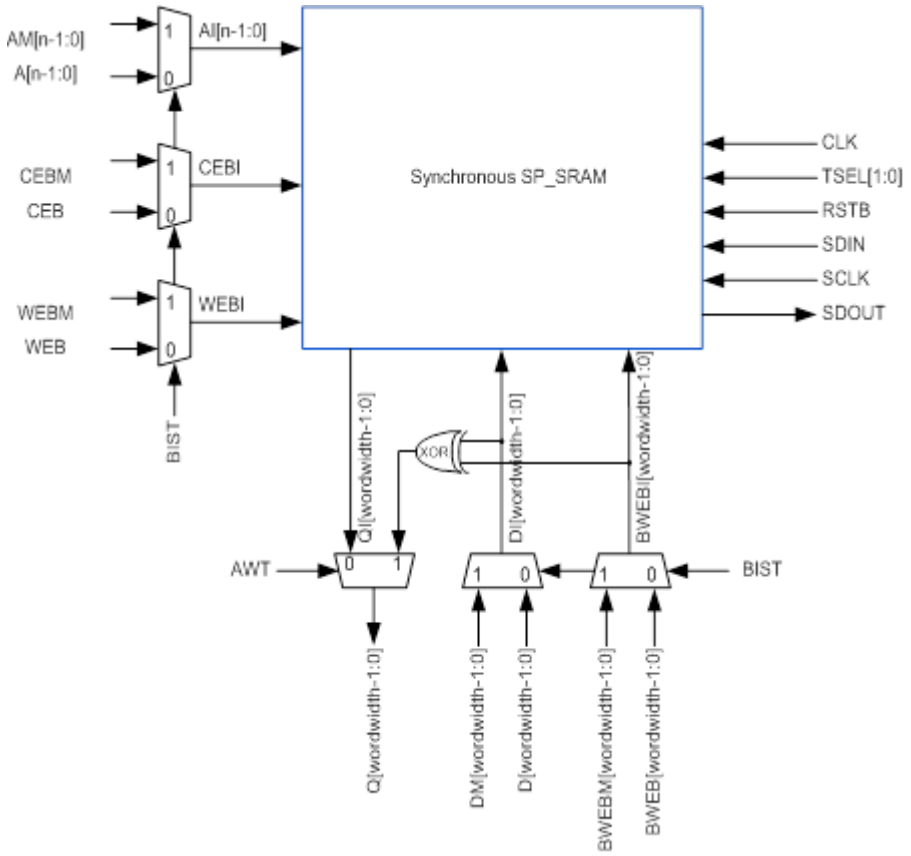

Figure2.2 BIST and AWT function block

The single port SRAM is synchronized and triggered by a rising edge clock, CLK. Input address A, input data D, chip enable CEB, and write enable WEB are latched by the rising edge of the clock. The following explains operation of the single port synchronous SRAM.

Read operation: The chip enable, CEB must be low and WEB stays high when triggered by CLK rising edge. Data is read and then transmitted to output bus Q [k-1:0] from memory location specified by A [n-1:0].

Write operation: The chip-enable, CEB and write-enable, WEB must be low when triggered by CLK rising edge. Data latched on D [k-1:0] that enters memory location specified by address A [n-1:0]. The bit-write feature is controlled by BWEB [k-1:0].

Normal / BIST mode: The Normal / BIST mode operation is controlled by BIST. In normal mode, BIST must be low. In BIST mode, BIST must be high.

AWT function: The AWT (Asynchronous Write Through) mode is enabled by AWT pin. In AWT mode, the output pins receive the value from input pins in specified time delay (regardless of clock). Use AWT option to get better test coverage.

Chapter 3 : Compiler Supporting Range

This compiler can be customized by segment option **SEG**, column mux option **CM**, number of words, **W**, and number of bits per word, **N**. The valid range for these parameters is specified in the following table:

SPWOR

Segment Option	Mux Options	Word Size (Address locations)	Bits (Number of I/Os)
SEG	**CM**	**W**	**N**
F (Fast)	4	128,136,144...2048	8,9,10...144
M (Medium)	4 8 16	256,264,272...4096 512,528,544...8192 1024,1056,1088…16384	8,9,10...144 4,5,6...72 2,3,4…39
S (High Density)	4 8	520,528,536...8192 1040,1056,1072...16384	8,9,10...144 4,5,6...72

. Figure 3.1: Available SP SRAM Compiler Configurations

- Compiler and instance naming
  ts1n40lpb{**W**}x{**N**}m{**CM**}{**SEG**}{**wba**}_{version} or user defined library name

For example:

SRAM cell: ts1n is designated for SP SRAM compiler

Naming	W	N	CM	SEG	BWEB	BIST	AWT	Version
ts1n40lpb256x144m4f_260a	256	144	4	F	No	No	No	260a
ts1n40lpb512x72m8m_260a	512	72	8	M	No	No	No	260a
ts1n40lpb16384x72m8swb_260a	16384	72	8	S	Yes	Yes	No	260a
ts1n40lpb16384x72m8swba_260a	16384	72	8	S	Yes	Yes	Yes	260a

NOTE: nonBWEB cannot be in-pair with AWT option

Chapter 4 : Pin Descriptions

SRAM macro: ts1n40lpb{word_depth}x{word_width}m{mux}{seg}wba_260a; Word_depth = 2^n

Pin	**Type**	Description
VDD	Supply	Power bus
VSS/GND	Supply	Ground bus
A[0]~A[n-1]	Input	Address input
AM[0]~AM[n-1]	Input	Address input for BIST
D[0]~D[word_width - 1]	Input	Data input
DM[0]~DM[word_width – 1]	Input	Data input for BIST
CLK	Input	CLK input
CEB	Input	Chip enable, active low for SRAM operation; active high for fuse data setting
CEBM	Input	Chip enable for BIST, active low for SRAM operation; active high for fuse data setting
WEB	Input	Write enable, active low
WEBM	Input	Write enable for BIST, active low
BWEB[0]~BWEB[word_width - 1]	Input	Bit write enable, active low
BWEBM[0]~BWEBM[word_width -1]	Input	Bit write enable, active low
Q[0]~Q[word_width – 1]	Output	Data output
RTSEL[1:0]	Input	Read margin setting pins
WTSEL[1:0]	Input	Write margin setting pins
BIST	Input	BIST enable
AWT	Input	Asynchronous write through
PD	Input	Power down mode

Note:

The timing data is characterized based on the setting of RTSEL [1]=0, RTSEL [0]=1 and WTSEL [1]=0 , WTSEL [0]=1.

User must connect these two pins to the correct logic value (RTSEL [1], RTSEL [0])=(0,1) and (WTSEL [1], WTSEL [0])=(0,1).

(RTSEL[1],RTSEL[0])=(0,0) : Aggressive read margin setting, used for debugging purpose.

(RTSEL[1],RTSEL[0])=(0,1) : Please use this setting.

Recommended setting with the optimized design margin

(RTSEL[1],RTSEL[0])=(1,0) : Relax read margin setting, used for debugging purpose.

(RTSEL[1],RTSEL[0])=(1,1) : Most relax read margin setting, used for debugging purpose.

(WTSEL[1],WTSEL[0])=(0,0) : Aggressive write margin setting, used for debugging purpose.

(WTSEL[1],WTSEL[0])=(0,1) : Please use this setting.

Recommended setting with the optimized design margin

(WTSEL[1],WTSEL[0])=(1,0) : Relax write margin setting, used for debugging purpose.

(WTSEL[1],WTSEL[0])=(1,1) : Most relax write margin setting, used for debugging purpose.

Chapter 5 Logic Truth Table

BIST Mode

Mode	BIST	Chip Select	Read/Write	Bit-write mask	Address	Data in
Normal	Low	CEB	WEB	BWEB	A	D
BIST	High	CEBM	WEBM	BWEBM	AM	DM

SRAM Function

Stage	PD	CLK	CEB	WEB	BWEB	D	A	Q	Memory contents
Standby	Low	H->H	High	-	-	-	-	No change	No change
Standby	Low	L->L	High	-	-	-	-	No change	No change
Power down	High	-	High	-	-	-	-	Low	No change
Write bit[i]	Low	L->H	Low	Low	Low	d[i]	a	No change	Mem[a][i]=d[i]
Read	Low	L->H	Low	High	-	-	a	Mem[a][i]	No change
Write bit[i] mask	Low	L->H	Low	Low	bit[i]=High	-	a	No change	No change in mem[a][i]

Asynchronous Write Through

AWT	D	BWEB	Q
High	d[i]	b[i]	b[i] (xor) d[i]
High	d[i]	b[i]	Low

NOTE: AWT MUST be in-pair with BWEB

Note:

1. The verilog model doesn't support the control enable, data, and address signals transition at positive clock edge. Please have some timing delays between control/data/address and clock signals to ensure the correct behavior.
2. In a non-fully decoded array, a write cycle to a nonexistent address location does not change the memory array contents and output remains the same.
3. In a non-fully decoded array, a read cycle to a nonexistent address location does not change the memory array contents but the output becomes unknown.
4. In the verilog model, the behavior of unknown clock will corrupt the memory data and make output unknown regardless of CEB signal. But in the silicon, the unknown clock at CEB high, the memory and output data will be held. The verilog model behavior is more conservative in this condition.
5. Rising and falling signals are measured at 50% of VDD.
6. Rising and falling slews are measured at 10% and 90% of VDD.
7. The verilog model provides UNIT_DELAY mode for the fast function simulation. All timing values in the specification are not checked in the UNIT_DELAY mode simulation. The behaviors still follow the truth table as above.

Memory x/z exception

PD	AWT	BIST	CLK	CEB	WEB	A	BWEB	D	mem	Output Q
x/z	-	-	-	-	-	-	-	-	all x	x
L	x/z	-	-	-	-	-	-	-	hold	x
L	L	x/z	-	-	-	-	-	-	all x	x
L	L	L	x/z	-	-	-	-	-	all x	x
L	L	L	L->H	x/z	-	-	-	-	all x	x
L	L	L	L->H	H	-	-	-	-	hold	hold
L	L	L	L->H	L	x/z	-	-	-	all x	x
L	L	L	L->H	L	H	x/z	-	-	hold	x
L	L	L	L->H	L	L	x/z	-	-	all x	hold
L	L	L	L->H	L	H	valid	x/z	-	hold	data-out
L	L	L	L->H	L	L	valid	x/z	-	mem[A] = x	hold
L	L	L	L->H	L	H	valid	valid	x/z	hold	data-out
L	L	L	L->H	L	L	valid	valid	x/z	mem[A][i] = x	hold

Used term for truth table

Condition:

L: low

H: high

x/z: unknown or high impedance

-: don't care, no matter with this pin

valid: address, data-in, BWEB only. It means stable (L or H); in fixed condition

L->H: clock only, rising edge

H->L: clock only, falling edge

L->L: clock only

H->H: clock only

Change: signal transient

Output buffer-in:

hold : keep previous state

x : unknown

data-out: normal read function case

mem:

Data-in (except BWEB): normal write function case except BWEBn=1

hold: keep previous state

x: store unknown to specified memory address

all x: store unknown to all memory address

all x (except BWEB): store unknown to all memory address except BWEBn=1

Chapter 6 : Timing Specifications

- Input Timing Requirements (please refer to **Quick Reference Table**)

SRAM read/write

Symbol	Parameter	From	To
tcd	Access time	CLK ↑	Q
thold	CLK to invalid Q	CLK ↑	Invalid Q
tos	Output slew time	Q	Q
tcs	Chip enable setup	CEB	CLK ↑
tch	Chip enable hold	CLK ↑	CEB
tas	Address setup time	A	CLK ↑
tah	Address hold time	CLK ↑	A
tws	Write enable setup	WEB	CLK ↑
twh	Write enable hold	CLK ↑	WEB
tbws	Bit-write enable setup	BWEB	CLK ↑
tbwh	Bit-write enable hold	CLK ↑	BWEB
tds	Data setup	D	CLK ↑
tdh	Data hold	CLK ↑	D
tcms	BIST Chip enable setup	CEBM	CLK ↑
tcmh	BIST Chip enable hold	CLK ↑	CEBM
tams	BIST Address setup time	AM	CLK ↑
tamh	BIST Address hold time	CLK ↑	AM
twms	BIST Write enable setup	WEBM	CLK ↑
twmh	BIST Write enable hold	CLK ↑	WEBM
tbwms	BIST Bit-write enable setup	BWEBM	CLK ↑
tbwmh	BIST Bit-write enable hold	CLK ↑	BWEBM
tdms	BIST Data setup	DM	CLK ↑
tdmh	BIST Data hold	CLK ↑	DM
tbists	BIST enable setup	BIST	CLK ↑
tbisth	BIST enable hold	CLK ↑	BIST
tcyc	Minimum CLK cycle	CLK ↑	CLK ↑
tckh	Minimum CLK Pulse High	CLK ↑	CLK ↓
tckl	Minimum CLK Pulse Low	CLK ↓	CLK ↑

Output Switching from AWT

Parameter	Symbol	From	To
tawtq	AWT to valid Q	AWT	Q
tbwq	BWEB to valid Q	BWEB	Q
tdq	D to valid Q	D	Q
tawtqh	AWT to invalid Q	AWT	Invalid Q
tbwqh	BWEB to invalid Q	BWEB	Invalid Q
tdqh	D to invalid Q	D	Invalid Q

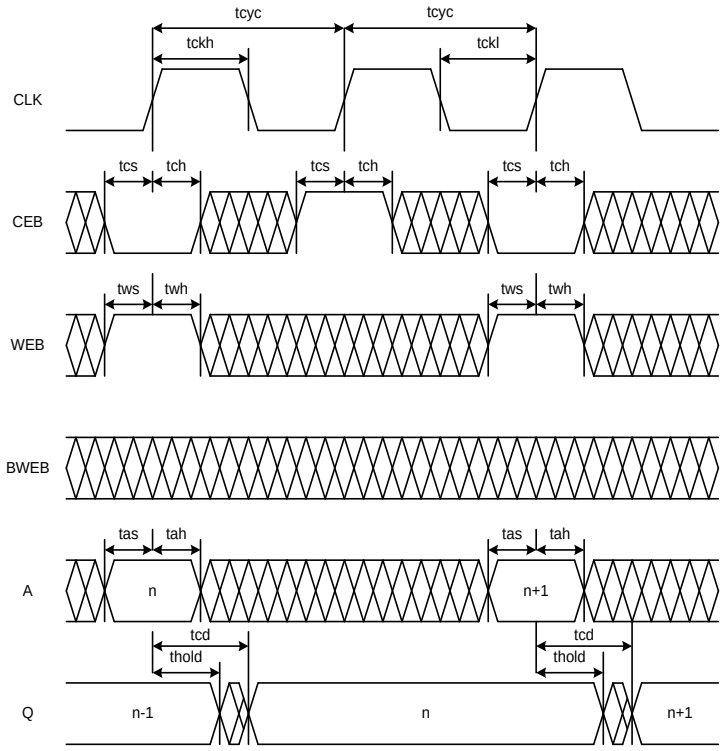

Figure 6.1 Timing waveform of Normal Mode READ cycle (BIST low)

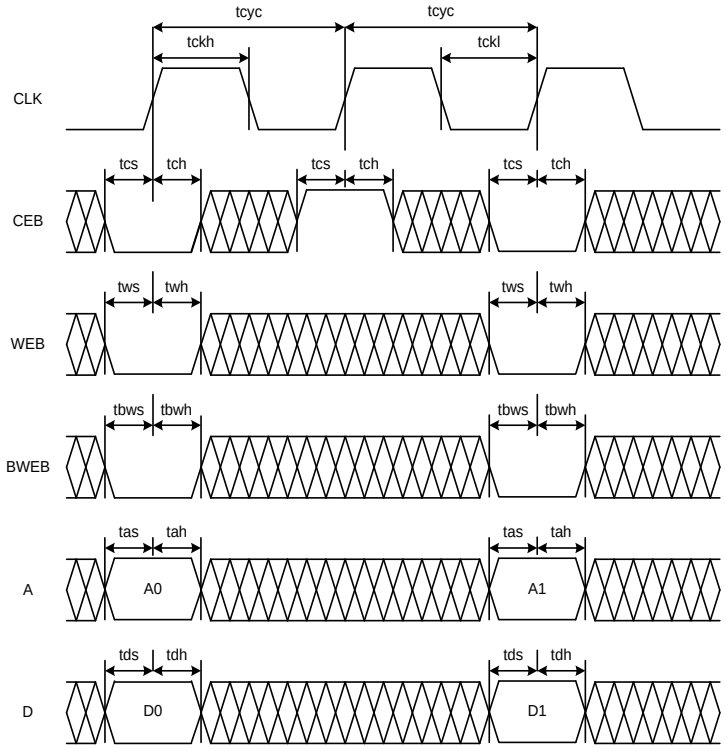

Figure 6.2 Timing waveform of Normal Mode WRITE cycle with bit-write mask

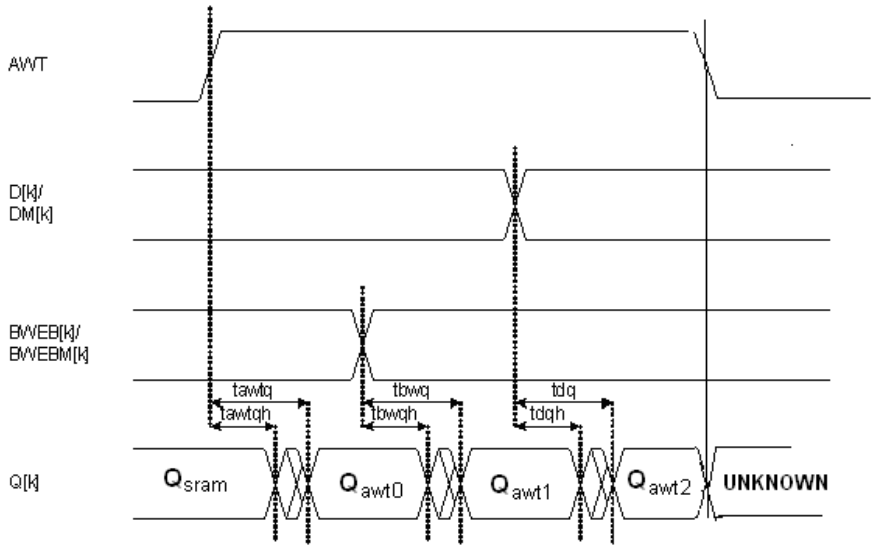

Figure 6.3 Asynchronous Write-through

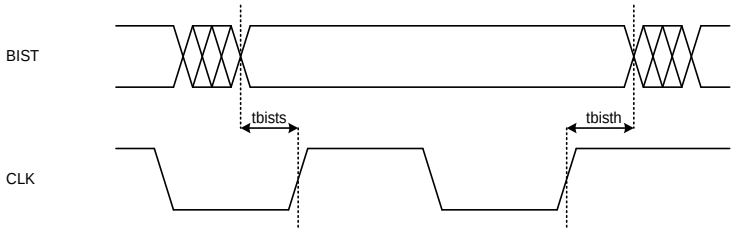

Figure 6.4 Timing waveform of BIST operation

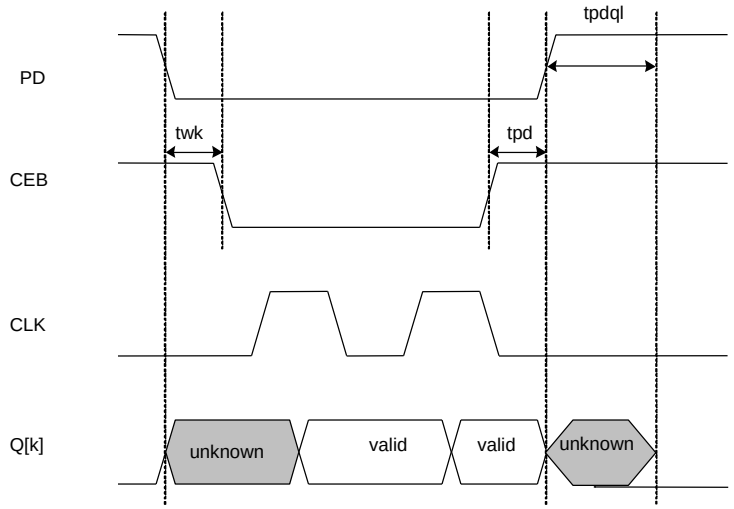

Figure 6.5 Timing waveform of Power down operation

Power Down Function

- Power Saving
  - Save stand-by leakage power by shutting down the peripheries circuits
- Behavior
  - Active high (1'b1 = power saving)
  - Power down mode works as an asynchronous control pin
  - Power down mode works when chip is disabled (CEB = 1'b1)
  - **All input pins cannot be floating or unknown during power down mode (PD =1'b1)**
  - There is a SRAM data output wake up time from power-saving mode to normal stand-by mode (twk). Wake up time must be sufficiently guaranteed for instance to have healthy power supply
  - The SRAM data output (Q) is logic low when PD is activated (PD =1'b1)
  - When the values of data output (Q) changes from 0 (power-saving mode) to unknown-X (normal stand-by mode), there is no high-Z on output Q.

Symbol	Parameter	From	To	Note
twk	Wake up time leaving PD mode	PD	CEB	Around 8 X SRAM minimum CLK cycle time.
tpd	Idle time entering PD mode	CEB	PD	Around 1 X SRAM minimum CLK cycle time
tpdql	Delay from PD to Q held low	PD	Q	-

Special Note:

- tpdql is not specified in Verilog model for the “unknown” status. In Verilog model, the output Q is changed to “L” directly after tpd = “H”. tpdql is 8 CLK cycles time

Chapter 7 : Process Voltage and Temperature (PVT) Characterization Conditions

PVT	Process	Voltage (V)	Temperature (C)
SS0P99VM40C	SS	0.99	-40
SS0P99V0C	SS	0.99	0
SS0P99V125C	SS	0.99	125
TT1P1V25C	TT	1.1	25
TT1P1V125C	TT	1.1	125
FF1P21VM40C	FF	1.21	-40
FF1P21V0C	FF	1.21	0
FF1P21V125C	FF	1.21	125
FFG1P21V125C	**FFG**	**1.21**	**125**

Note:

1. Permanent damage could occur if the operation exceeds the table listing above.
2. FFG/1.21V/125C corner is for Iddq leakage sign-off only, there is no timing data in this corner.

Chapter 8 : Power/Ground Connection Guideline

In chip design level, users must guarantee to meet the Vccmin spec(>= Vdd-10%) at the SRAM IP boundary to avoid performance impact from voltage drop of system power.

In order to have better IR drop and EM management, please follow the power/ground connection guideline below:

- All power and ground pins **MUST** be connected to VDD and VSS, respectively.
- Route M5 power lines over the SRAM instances and cover as much area as possible.
- M5 power/signal lines must be placed perpendicularly to M4 and drop VIAs in full of any cross-area of two metals.
- Fully populate the intersections of power rails and power pins with VIAs.
- Special attention should be made to the power connections close to the bottom of the memory array to power the IO buffers.
- Multiple connections along each power pin is recommended to further reduce IR drop.

Chapter 9 : Scramble Diagram

BL[i] and BLB[i] mean the bit-line and the complement of bit line. When write cycle, if the D[0]=1;row address =1 and column address A[2:0]=001, then the WL[1] is active and the pair of BL[1] and BLB[1] is selected. BL[1] keeps high and BLB[1] discharges to logic 0, the selected bit cell stores logic 1.

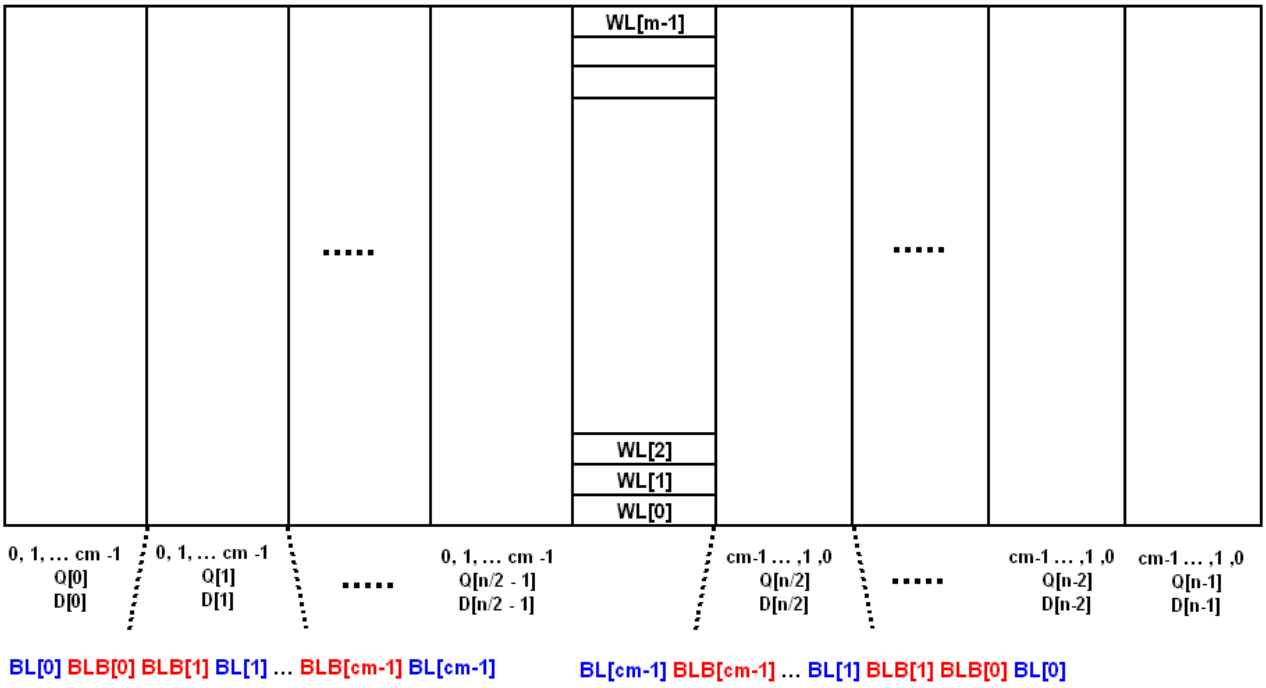

Figure9.1 scramble table

Note:
cm : the number of column-mux;
m : the number of row;
n : the number of word width(bits).
If n is equal to even number, all IO(bits) will be allocated evenly into left and right bank, namely each bank has the same number of IO(bits), whereas, if n is equal to odd number, left bank always has one more IO(bit) than right bank.

Example-1: For word-depth=16384, Mux = 8: WL number = 16384/8 = 2048 = 2^{11}

Column Mux Decode	A[2:0]
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Word line Decode	A[13:3]
WL[1]	0000,0000,001
WL[5]	0000,0000,101

Example-2: For word-depth=2048, Mux = 4: WL number = 2048/4 = 512 = 2^9

Column Mux Decode	A[1:0]
0	00
1	01
2	10
3	11

Word line Decode	A[10:2]
WL[0]	00,0000,000
WL[7]	00,0000,111

Chapter 10 : Quick Reference Table

Symbol	**Description**
Word	Word depth
IO	IO number
SEG	Row number of one segment
Mux	Mux number
Area	Layout area
Access_time	Access time
Cycle_time	Cycle time
Adr_setup	Address setup time
Adr_hold	Address hold time
Data_setup	Data setup time
Data_hold	Data hold time
Read_power	Read current (not including pin transition)
Write_power	Write current (not including pin transition)
Leakage	Standby current
Leakage_pd	Standby current in power down mode
Leakage_ffg	Standby current in FFG/1.21V/125C

The timing data is based on output load 0.002pf and the input slew for each condition is shown as below table.

Voltage	Input slew
1.21V	0.0048ns
1.1V	0.0064ns
0.99V	0.0080ns

Please reference the file: tsn40lpd242spsram_20100400_260a_Quick_Reference_Table.pdf