TSN40LP2PRF

TSMC 40nm Low Power Two-Port Register File Compiler Databook

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Chapter 1: Compiler General Description

Low power VLSI technology becomes increasingly important in the growing area of electronic industry. In order to provide the solution of low power application, TSMC 40nm low power SRAM compiler is provided.

TSMC 40nm Low Power Synchronous Two Port Register File with BIST interface compiler is high performance, low power, and fabricated in TSMC CLN40LP (1.1V) CMOS low power technology. This register file operates at a voltage of 1.1V +/- 10% and a junction temperature range of -40°C to 125°C. The available register file size is configured from 16 bits to 72K bits as shown in Figure 4.1. The compiled register file is divided into 4 groups according to their column-selected numbers (Mux=2, 4, 8, or 16). There are three kinds of segmentation selections available for different speed applications (fast, medium, small). The "word depth" is defined as the number of words, and the "word width" is defined as the number of bits per word.

Chapter 2: Features

TSMC 40nm LP 2P Register File compiler has the following features:

- TSMC 1P10M 40nm CLN40LP (1.1V) CMOS process
- Synchronous operation
- Parameterized selectable configurations
- Four column-selected options can be chosen (2, 4, 8, or 16)
- High current with TSMC's d562/d455 (pre-shrink/ post-shrink) 8TTP SRAM bit cell; MT form: 8TTP (HP), cell imp mask:11N(VTC_N2) and 11P(VTC_P2)
- Support power mesh by metal 4 pins
- Limited porosity on metal 4
- Support global EDA models and precise timing characterization data
- Near-Zero Hold Time (data, address, and control inputs)
- Bit-write function with each data input
- BIST mux interface (optional)
- Power down mode is low leakage mode to reduce leakage power by switching off part of periphery circuit

Chapter 3: Block Diagrams

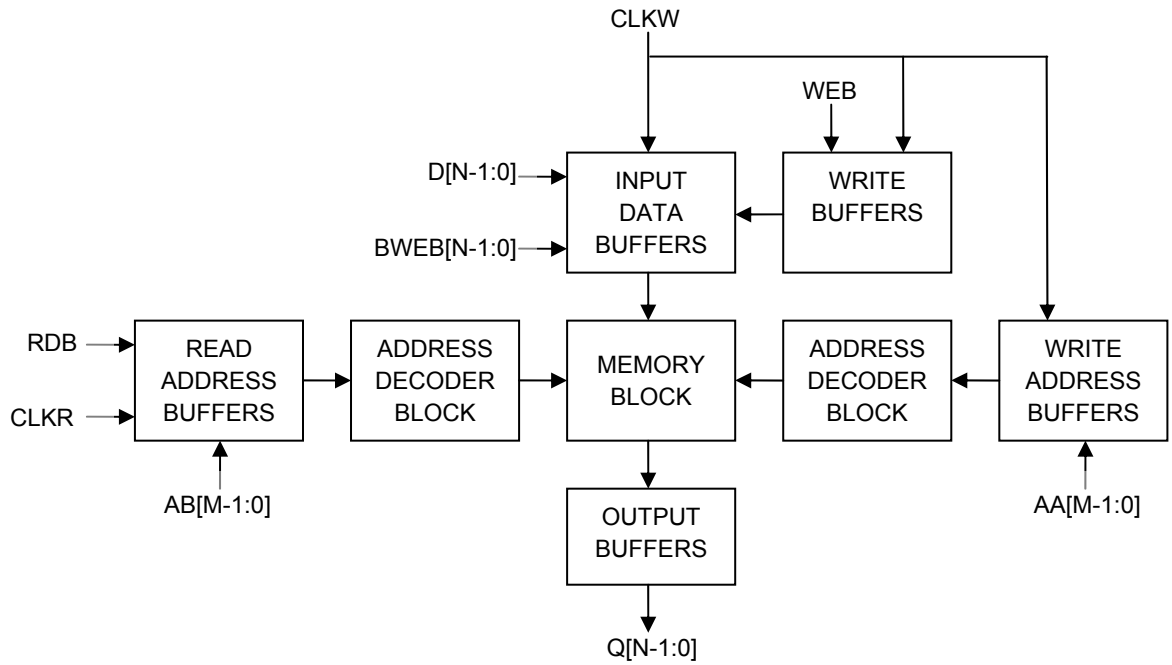


Figure 3.1: Without BIST Interface

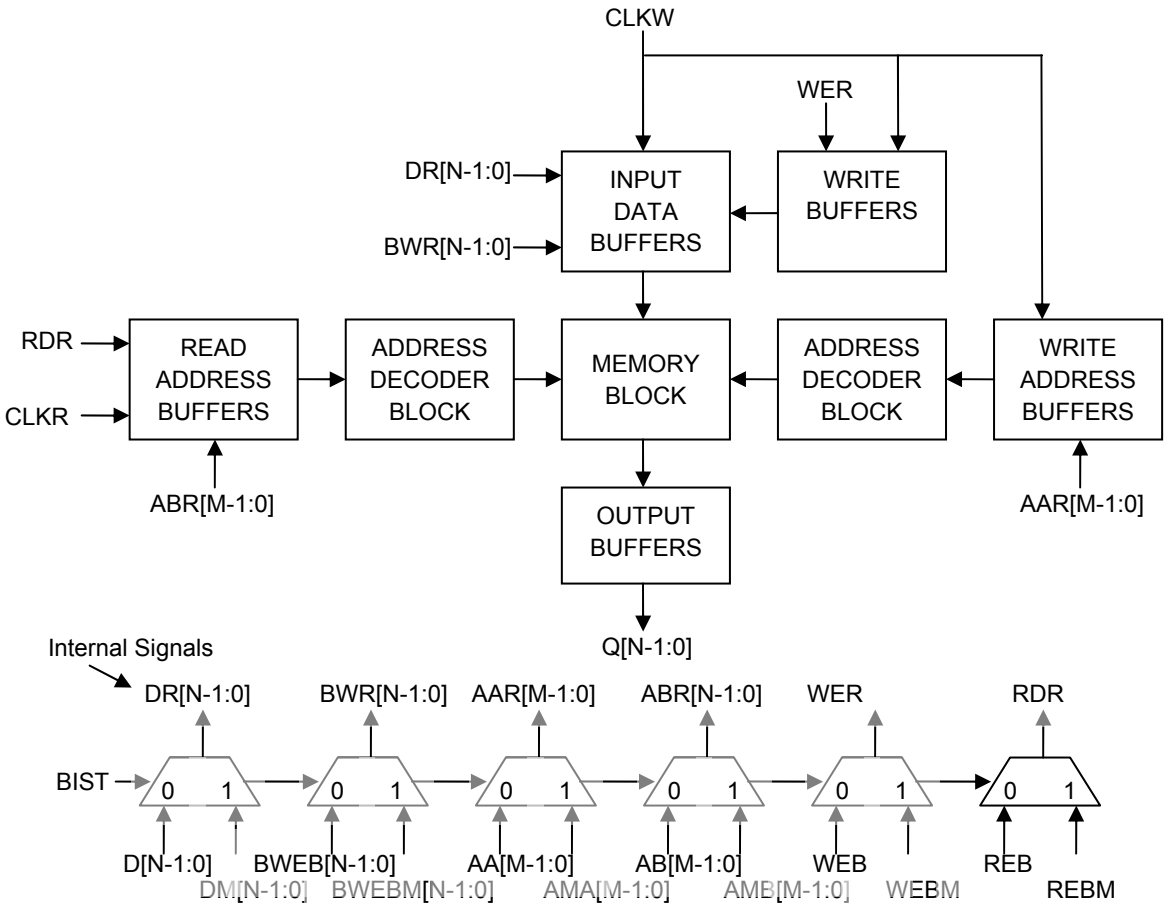


Figure 3.2: With BIST Interface

Chapter 4: Compiler Supporting Range

The 2P RF compiler can be customized by segment option **SEG**, column mux option **CM**, number of words, **W**, and number of bits per word, **N**. The valid range for these parameters is specified in the following table:

Segment Option	Mux Options	Word Size (Address locations)	Bits (Number of IOs)
SEG	**CM**	**W**	**N**
F (Fast)	2 4 8 16	8,16,24...256 16,32,48...512 32,64,96...1k 64,128,192...2k	2,3,4...72 2,3,4...36 2,3,4...18 2,3,4...9
M (Medium)	2 4 8 16	40,48,56....512 80,96,112...1k 160,192,224...2k 320,384,448...4k	2,3,4...72 2,3,4...36 2,3,4...18 2,3,4...9
S (High Density)	2 4 8 16	72,80,88...1k 144,160,176...2k 288,320,352...4k 576,640,704...8k	2,3,4...72 2,3,4...36 2,3,4...18 2,3,4...9

Figure 4.1: Available Register File Configurations

- Compiler and instance naming
  ts6n40lpa{**W**}x{**N**}m{**CM**}{**SEG**}_{version} or
  user defined library name : i.e. 2PRF

For example:

SRAM cell: ts6 is designated for 2P RF compiler

Naming	**W**	**N**	**CM**	**SEG**	**Revision**
ts6n40lpa256x36m4f_130a	256	36	4	F	130a
ts6n40lpa4096x16m8s_130a	4096	16	8	S	130a

Chapter 5: Pin Descriptions

Pin	Type	Description
VDD	Supply	Power bus
VSS	Supply	Ground bus
AA[**M**-1:0]	Input	Address Bits on Port A (Write)
D[**N**-1:0]	Input	Data Inputs
BWEB[**N**-1:0]	Input	Bit-write Enable Bar Inputs (Active-Low)
WEB	Input	Write Enable Bar (Active-Low)
AB[**M**-1:0]	Input	Address Bits on Port B (Read)
CLKW	Input	Write Clock (Active-High)
CLKR	Input	Read Clock (Active-High)
REB	Input	Latch Read Address Enable (Active-Low)
AMA[**M**-1:0]	Input	BIST Address Bits on Port A (Write)
DM[**N**-1:0]	Input	BIST Data Input
BWEBM[**N**-1:0]	Input	BIST Bit-write Enable Bar Inputs (Active-Low)
WEBM	Input	BIST Write Enable Bar Input (Active-Low)
AMB[**M**-1:0]	Input	BIST Address Bits on Port B (Read)
REBM	Input	BIST Latch Read Address Enable (Active-Low)
BIST	Input	BIST Interface Enable
PD	Input	Power Down
Q[**N**-1:0]	Output	Data Outputs

Chapter 6: Logic Truth Table

Power Down Mode:

Mode	PD	CLKR/ CLKW	REB/ WEB	REBM/ WEBM	BWEB/ BWEBM	D/ DM	AA/ AAM	AB/ ABM	BIST	Q	Memory contents
Power Down	H	-	H	-	-	-	-	-	L	L	Hold
Power Down	H	-	-	H	-	-	-	-	H	L	Hold

Logic Truth Table - Normal or BIST Mode:

Mode	BIST	Clock	Read Enable	Write Enable	Address	Data-In
Normal	L	CLKR/CLKW	REB	WEB	AA/AB	D
BIST	H	CLKR/CLKW	REBM	WEBM	AMA/AMB	DM

Logic Truth Table – Active Pins:

Function	CLKR	CLKW	REB/ REBM	WEB/ WEBM	BWEB/ BWEBM	D/ DM	AA/ AMA	AB/ AMB	Q[i]	Memory Contents
Standby	L	L	-	-	-	-	-	-	no change	no change
Deselect	↑	↑	H	H	-	-	-	-	no change	no change
Read	↑	↑	L	H	-	-	-	b	mem[b]	no change
Write bit [i]	↑	↑	H	L	L	d[i]	a	-	no change	mem[**a**][i]=d[i]
Write bit [i] Mask	↑	↑	H	L	b[i]=H	-	a	-	no change	no change on mem[**a**][i]
Write and Read a!=b	↑	↑	L	L	L	d[i]	a	b	mem[b]	mem[**a**][i]=d[i]
Write and Read a==b	↑	↑	L	L	L	d[i]	a	b	X	mem[**a**][i]=d[i]

Note:

1. The verilog model doesn't support the control enable, data, and address signals transition at positive clock edge. Please have some timing delays between control/data/address and clock signals to ensure the correct behavior.
2. In a non-fully decoded array, a write cycle to a nonexistent address location does not change the memory array contents and output remains the same.
3. In a non-fully decoded array, a read cycle to a nonexistent address location does not change the memory array contents but the output becomes unknown.
4. In the verilog model, the behavior of unknown clock will corrupt the memory data and make output unknown regardless of CEB signal. But in the silicon, the

unknown clock at CEB high, the memory and output data will be held. The verilog model behavior is more conservative in this condition.

5. Rising and falling signals are measured at 50% of VDD.
6. Rising and falling slews are measured at 10% and 90% of VDD.
7. There is a read/write port contention issue when read port and write port operate with the same address. Please check the critical contention timings, trwcc and twrcc, for the correct usage.
8. The verilog model provides UNIT_DELAY mode for the fast function simulation. All timing values in the specification are not checked in the UNIT_DELAY mode simulation. The behaviors still follow the truth table as above.
9. The critical contention timings, trwcc and twrcc, are not checked in the UNIT_DELAY mode simulation. If addresses of read and write operations are the same and the real time of the positive edge of CLKW and CLKR are the same, it will be treated as a read/write port contention and followed the logic truth table as above.

Memory x/z exception

PD	BIST	CLKR	REB	AB	CLKW	WEB	AA	BWEB[i]	D[i]	mem	Output Q
x/z	-	-	-	-	-	-	-	-	-	all x	x
H	-	-	-	-	-	-	-	-	-	hold	L
L	x/z	-	-	-	-	-	-	-	-	all x	x
L	-	x/z	-	-	-	-	-	-	-	hold	x
L	L	L->H	x/z	-	-	-	-	-	-	hold	x
L	L	L->H	H	-	-	-	-	-	-	hold	hold
L	L	L->H	L	x/z	-	-	-	-	-	hold	x
L	-	-	-	-	x/z	-	-	-	-	all x	hold
L	L	-	-	-	L->H	x/z	-	-	-	all x	hold
L	L	-	-	-	L->H	L	x/z	-	-	all x	hold
L	L	-	-	-	L->H	L	valid	x/z	-	mem[AA][i] = x	hold
L	L	-	-	-	L->H	L	valid	L	x/z	mem[AA][i] = x	hold

Note: above hazard condition is for functional definition. Input pin high impedance might cause high leakage issue.

Used term for truth table

Condition:

L: logic low

H: logic high

x/z: unknown or high impedance

-: Logic low, logic high or Unknown. Not include high impedance

valid: Address and BWEB only. It means stable (0 or 1) in fixed condition

L->H: clock only, rising edge

Output Q:

hold: keep previous state

x: unknown

mem:

mem[AA][i] = x: memory content is unknown at the specific memory address **and** specific **IO**

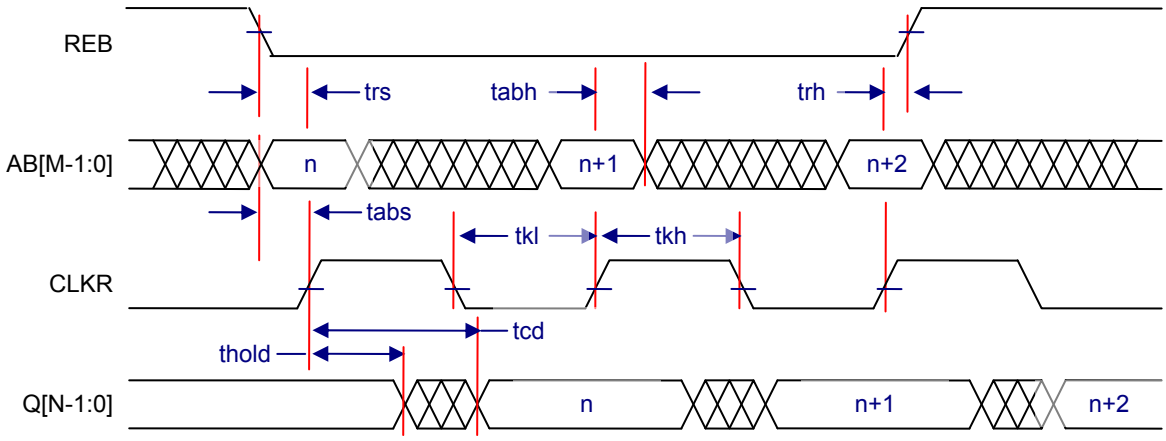
hold: keep previous state

all x: store unknown to all memory address

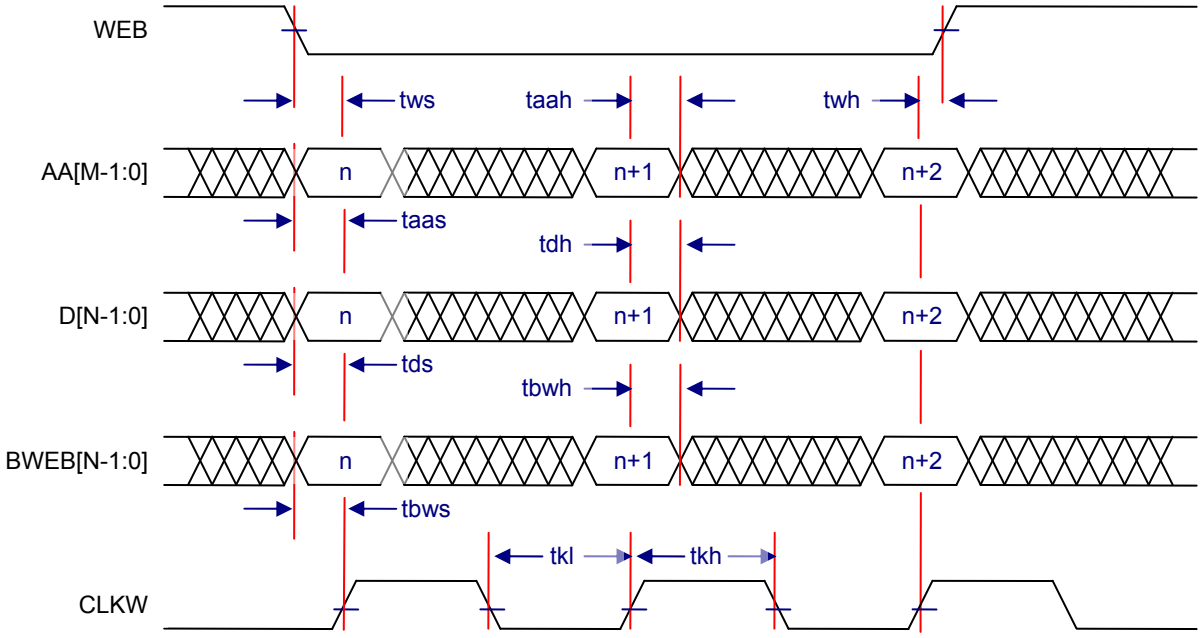
Chapter 7: Timing Specifications

Symbol	Parameter	From	To
tws	WEB Setup Before CLKW↑	WEB	CLKW↑
twh	WEB Hold After CLKW↑	WEB	CLKW↑
twms	WEBM Setup Before CLKW↑	WEBM	CLKW↑
twmh	WEBM Hold After CLKW↑	WEBM	CLKW↑
taas	AA Setup Before CLKW↑	AA[**M**-1:0]	CLKW↑
taah	AA Hold After CLKW↑	AA[**M**-1:0]	CLKW↑
tamas	AMA Setup Before CLKW↑	AMA[**M**-1:0]	CLKW↑
tamah	AMA Hold After CLKW↑	AMA[**M**-1:0]	CLKW↑
tds	Data Setup Before CLKW↑	D[**N**-1:0]	CLKW↑
tdh	Data Hold After CLKW↑	D[**N**-1:0]	CLKW↑
tdms	DM Setup Before CLKW↑	DM[**N**-1:0]	CLKW↑
tdmh	DM Hold After CLKW↑	DM[**N**-1:0]	CLKW↑
tbws	BWEB Setup Before CLKW↑	BWEB[**N**-1:0]	CLKW↑
tbwh	BWEB Hold After CLKW↑	BWEB[**N**-1:0]	CLKW↑
tbwms	BWEBM Setup Before CLKW↑	BWEBM[**N**-1:0]	CLKW↑
tbwmh	BWEBM Hold After CLKW↑	BWEBM[**N**-1:0]	CLKW↑
tbists	BIST Setup Before CK↑	BIST	CLKW↑CLKR↑
tbisth	BIST Hold After CK↑	BIST	CLKW↑CLKR↑
trs	REB Setup Before CLKR↑	REB	CLKR↑
trh	REB Hold After CLKR↑	REB	CLKR↑
trms	REBM Setup Before CLKR↑	REBM	CLKR↑
trmh	REBM Hold After CLKR↑	REBM	CLKR↑
tabs	AB Setup Before CLKR↑	AB[**M**-1:0]	CLKR↑
tabh	AB Hold After CLKR↑	AB[**M**-1:0]	CLKR↑
tambs	AMB Setup Before CLKR↑	AMB[**M**-1:0]	CLKR↑
tambh	AMB Hold After CLKR↑	AMB[**M**-1:0]	CLKR↑
tkh	Minimum CK Pulse High	CLKW↑CLKR↑	CLKW↓CLKR↓
tkl	Minimum CK Pulse Low	CLKW↓CLKR↓	CLKW↑CLKR↑
twcyc	Minimum CLKW Cycle Time	CLKW↑	CLKW↑
trcyc	Minimum CLKR Cycle Time	CLKR↑	CLKR↑
trwcc	Minimum Read Write Clock Separation	CLKR↑	CLKW↑
twrcc	Minimum Write Read Clock Separation	CLKW↑	CLKR↑
tcd	Clock to Valid Q	CLKR↑	Q[**N**-1:0]
thold	Clock to Invalid Q	CLKR↑	Q[**N**-1:0]

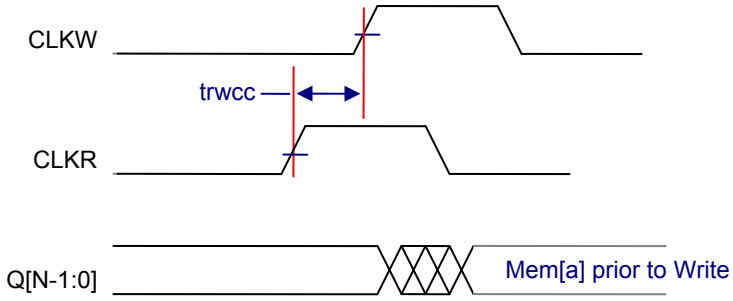
Read Operation with CLKR Pulse



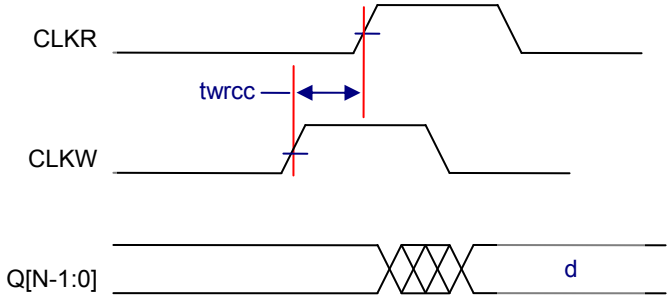
Write Operation with CLKW Pulse



Port Contention Timing Diagram Read then Write (AA=AB=a, D=d)

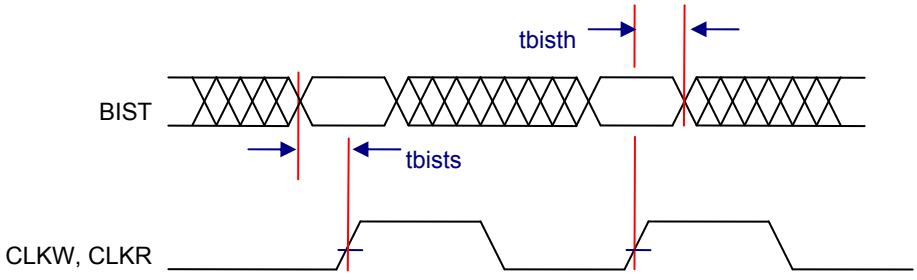


Port Contention Timing Diagram Write then Read (AA=AB=a, D=d)



BIST Timing Diagram

Note: BIST timing can be violated (BIST toggling while one of the clocks is high).There is no assurance that all data in the memory will remain unchanged. Once back in functional mode, normal operation can resume.



Chapter 8: Process Voltage and Temperature (PVT) Characterization Conditions

PVT	Process	Voltage (V)	Temperature (C)	
SS0P99VM40C	SS	0.99	-40	Vdd-10%
SS0P99V0C	SS	0.99	0	Vdd-10%
SS0P99V125C	SS	0.99	125	Vdd-10%
TT1P1V25C	TT	1.1	25	Vdd
TT1P1V125C	TT	1.1	125	Vdd
FF1P21VM40C	FF	1.21	-40	Vdd+10%
FF1P21V0C	FF	1.21	0	Vdd+10%
FF1P21V125C	FF	1.21	125	Vdd+10%
FFG1P21V125C	FFG	1.21	125	Vdd+10%

Note: FFG/1.21v/125C corner is supported as one extra pvt corner in NLDM and only leakage data is provided.

Chapter 9: Power/Ground Connection Guideline

In chip design level, users must guarantee to meet the Vccmin spec(>= Vdd-10%) at the SRAM IP boundary to avoid performance impact from voltage drop of system power.

In order to have better IR drop and EM management, please follow the power/ground connection guidelines below:

- All power and ground pins MUST be connected to VDD and VSS, respectively.
- M5 power/signal lines must be placed perpendicularly to M4 and drop VIAs in full of any cross-area of two metals as much as possible.
- Route M5 power lines over the SRAM instances and cover as much area as possible.
- Special attention should be made to the power connections close to the bottom of the memory array to power the IO buffers.

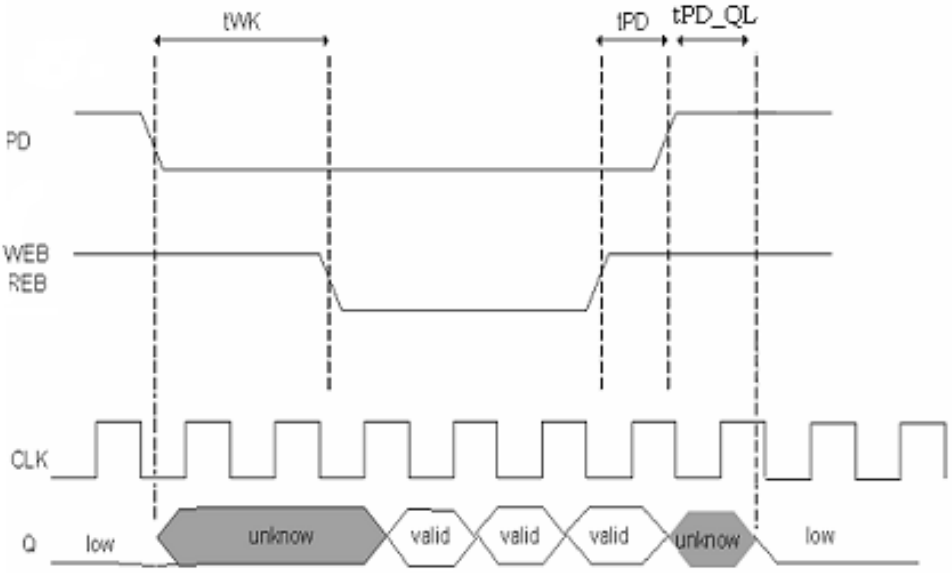
Chapter 10: Power Down Requirements

The Power Down pin (PD) is a low leakage mode by periphery power partially switch off, an active-high input which may be used to reduce leakage power on a memory during periods of time when it is not being used. No read or write cycles may take place while PD is asserted, but data will still be retained in the memory cells. Also, the Q outputs will be forced to 0.

Also, the PD input assists in situations where it is desirable to power-down the memory entirely. If PD is held high while VDD is removed from the memory macro, the Q outputs will be held to 0 rather than allowed to float.

It is required that the memory have one inactive cycle (rising edge of either CLK with the associated CEB input high, or inactive), and no intervening read or write cycles on either port, before PD is asserted.

After PD is de-asserted, it is required that the memory have eight inactive cycles on either port, with no intervening read or write cycles on any port, before the first active (read or write) cycle.



Symbol	Parameter	From	To	Note
tWK	Wake up time leaving PD mode	PD	WEB/REB	8 times SRAM minimum clock cycles time
tPD	Idle time entering PD mode	WEB/REB	PD	1 SRAM minimum clock cycles time
tPD_QL	Delay from PD to Q held low	PD	Q	unknown

Chapter 11: Scramble Tables

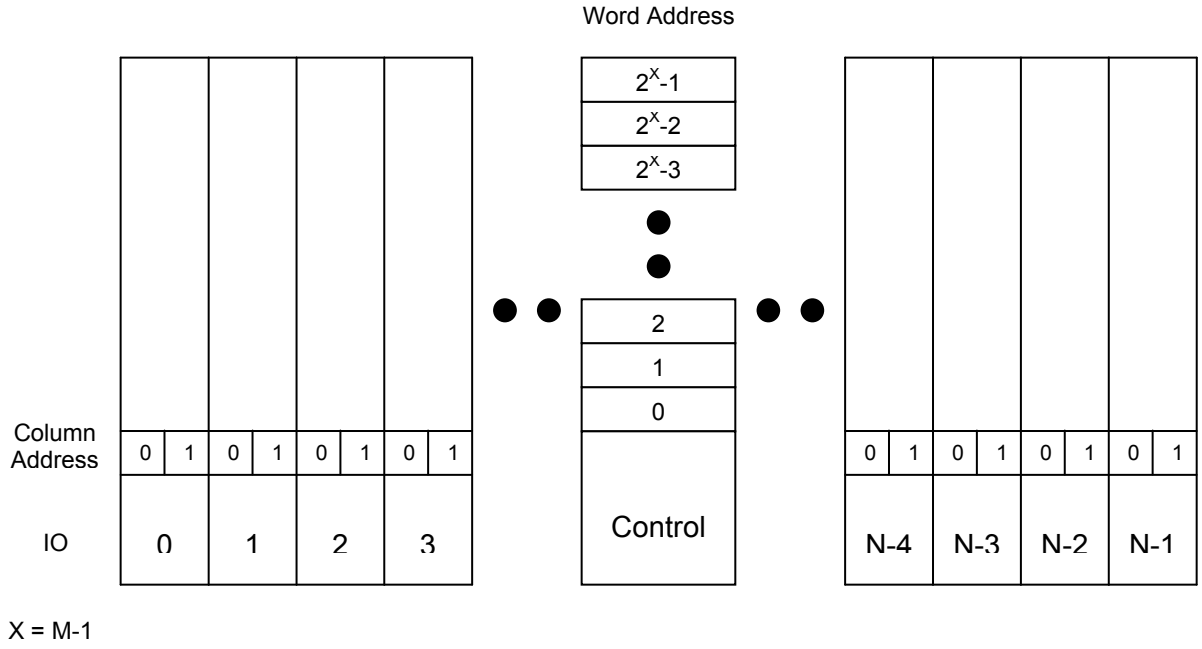


Figure 10.1: Scramble Table CM=2

Column address

A0
Y0

Row address

A1	A2	. . .	A[M-1]
X0	X1	. . .	X[J-1]

Y0 are used for bit line selection. X0~X[J-1] are used for word line decoding.

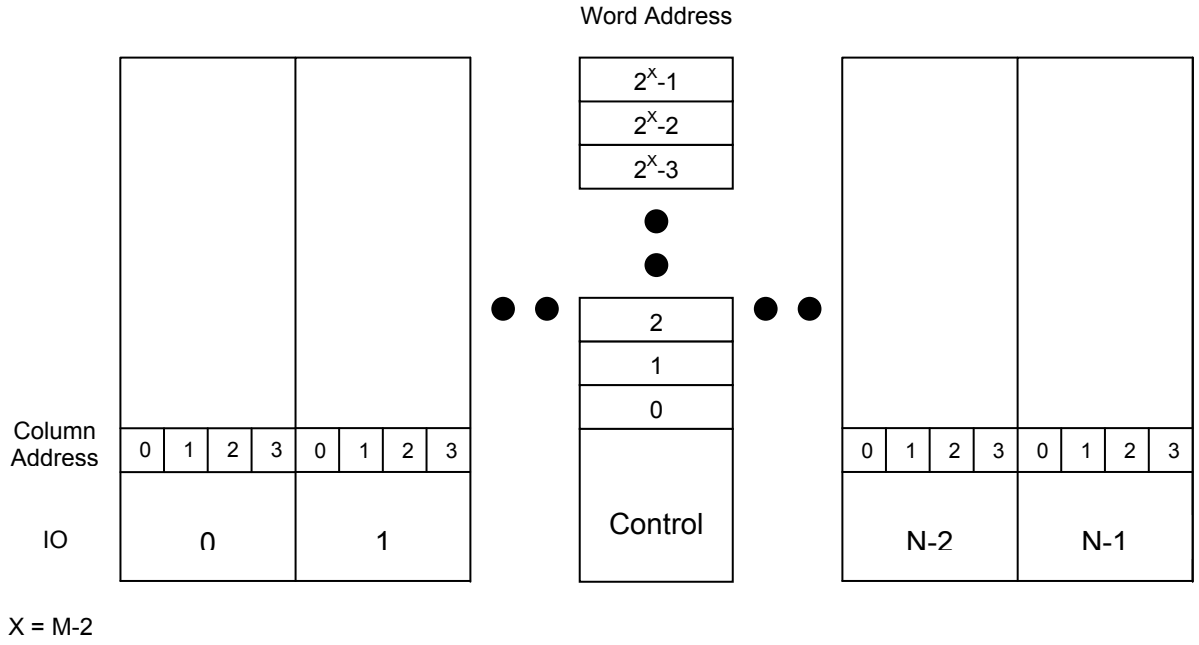


Figure 10.2: Scramble Table CM=4

Column address

A0	A1
Y0	Y1

Row address

A2	A3	. . .	A[M-1]
X0	X1	. . .	X[J-1]

Y0~Y1 are used for bit line selection. X0~X[J-1] are used for word line decoding.

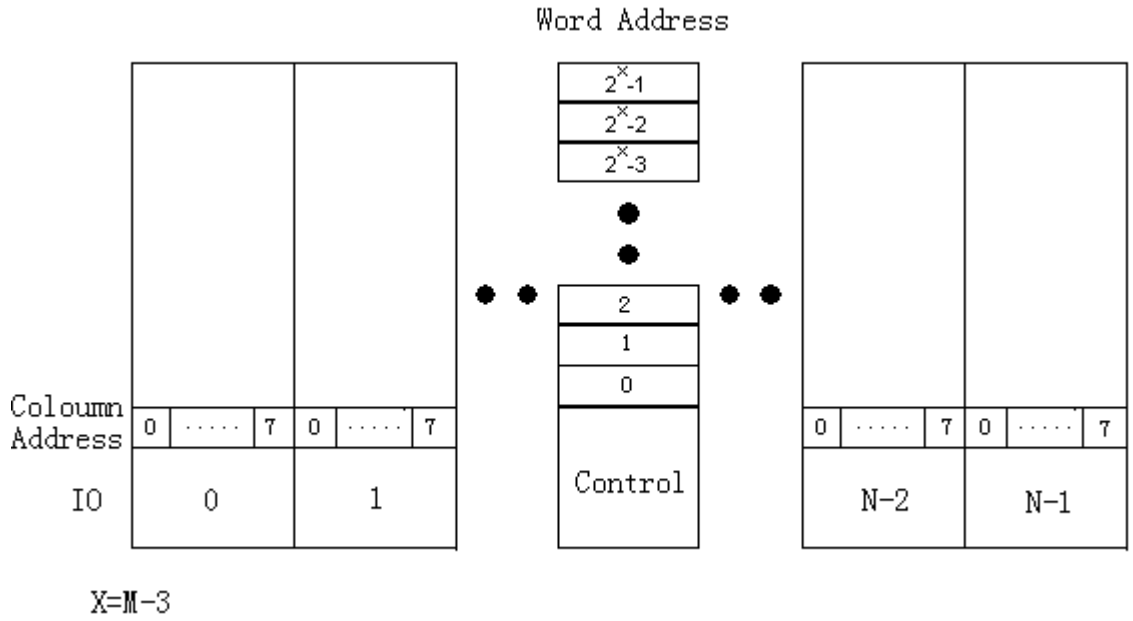


Figure 10.3: Scramble Table CM=8

Column address

A0	A1	A2
Y0	Y1	Y2

Row address

A3	A4	. . .	A[M-1]
X0	X1	. . .	X[J-1]

Y0~Y2 are used for bit line selection. X0~X[J-1] are used for word line decoding.

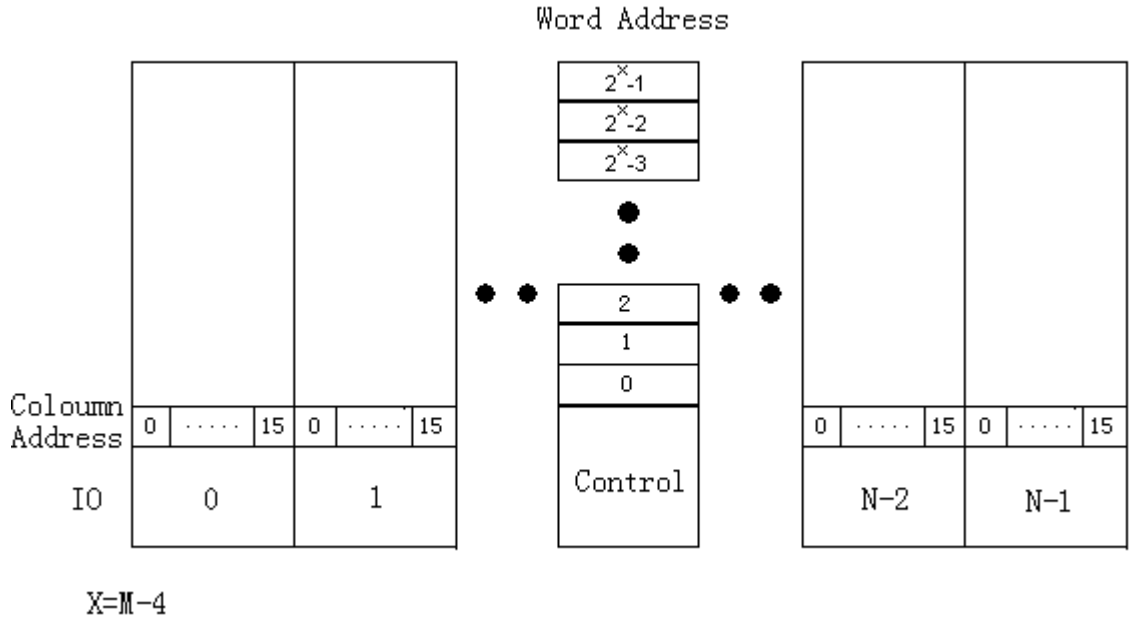


Figure 10.4: Scramble Table CM=16

Column address

A0	A1	A2	A3
Y0	Y1	Y2	Y3

Row address

A4	A5	. . .	A[M-1]
X0	X1	. . .	X[J-1]

Y0~Y3 are used for bit line selection. X0~X[J-1] are used for word line decoding.

Chapter 12: Application Notes

Interfacing

The 2P RF is designed for synchronous operation with positive edge-triggered flip-flops driving the addresses, data inputs, and controls. Data output delay, tcd, is measured from clock to the latest arriving Q output. Data output hold time, thold, is measured from clock to the first changing Q output.

Address Contention in General
Since CLKW and CLKR are independent clocks whose edges may not be related to each other, address contentions between ports A and B are not resolved. Address contention is defined as the same address being latched during a write and read operation where insufficient clock separation occurs (trwcc or twrcc). If an address contention occurs, indeterminate results are read from the array. Timing specifications trwcc, and twrcc relate the minimum time required between CLKW and CLKR in order for same address operations to occur without indeterminate results. If the same external signal drives CLKW and CLKR, indeterminate results will occur if the addresses match during a simultaneous write and read operation.

Address Contention with Write Operation Followed by Read Operation
twrcc (measured from both clocks rising) is the minimum separation time required for a write to complete before a successful read of the same address can occur. This guarantees that the data is written to the array before the data is accessed for a read operation. If twrcc is violated during a write followed by read operation, then the read output is indeterminate.

Address Contention with Read Operation Followed by Write Operation
trwcc (measured from both clocks rising) is the minimum separation time required for a successful read to complete before a write of the same address can occur. This guarantees that the data is read from the array before the data is overwritten by the write operation. If trwcc is violated during a read followed by write operation, then the read output is indeterminate.

Chapter 13: Quick Reference Table

Symbol	Description
word	Word depth
io	IO number
mux	Mux number
seg	Segment
drawing dimension area	Layout area
access_time	Access time
rcycle_time	Read Cycle time
wcycle_time	Write Cycle time
adr_setup	Address setup time
adr_hold	Address hold time
data_setup	Data setup time
data_hold	Data hold time
readc	Read current, excludes pin current
writec	Write current, excludes pin current
leakage	Static current
leakage_pd	Static power in power down mode
leakage_ffg	Static power in FF global corner
total Kbits	(word * io) / 1024

The timing data is based on output load 0.00156pf and the input slew for each condition is shown as below table.

Process	Input slew
FF	0.0048ns
TT	0.0064ns
SS	0.0080ns

Please refer to the file: TSN40LP2PRF_20071100_130A_Quick_Reference_Table.xls