TSN40LPHS1PRF

TSMC 40nm Low Power High Performance

One-Port Register File SRAM Compiler

Databook

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Chapter 1: Compiler General Description

Low power VLSI technology becomes increasingly important in the growing area of electronic industry. In order to provide the solution of low power application, TSMC 40nm low power high performance one-port register file SRAM compiler is provided.

TSMC 40nm low power high performance one-port register file SRAM compiler is a high performance synchronous one-port register file memory designed with TSMC 6T SRAM bit cell in TSMC's ten-metal-layer, 40nm CLN40LP (1.1V) CMOS process. The TSMC one-port register file operates at a voltage of 1.1V ± 10% and a junction temperature range of -40℃ to +125℃.

The available SRAM size is configured from 32 bits to 36K bits as shown in Figure 4.1. The compiled SRAMs are divided into 4 groups according to their column-selected numbers (Mux=2, 4, 8, 16). The "word depth" is defined as the number of words and the "word width" is defined as the number of bits per word.

Chapter 2: Features

TSMC 40nm low power high performance one-port register file SRAM compiler has the following features.

- TSMC 1P10M 40nm CLN40LP (1.1V) CMOS process
- Synchronous operation
- Segmented memory array and 4 kinds of column-mux option
- High Performance with 6T SRAM bit cell 1.04X0.36=0.374um^2 (pre- shrink)/ 0.303um^2 (post-shrink)
- Over SRAM routing for metal 4 and above
- Support global EDA models and precise timing characterization data
- Near-Zero Hold Time (data, address, and control inputs)
- Bit-write function with each data input
- Power down mode is low leakage mode to reduce leakage power by switching-off part of periphery circuit

Chapter 3: Block Diagram

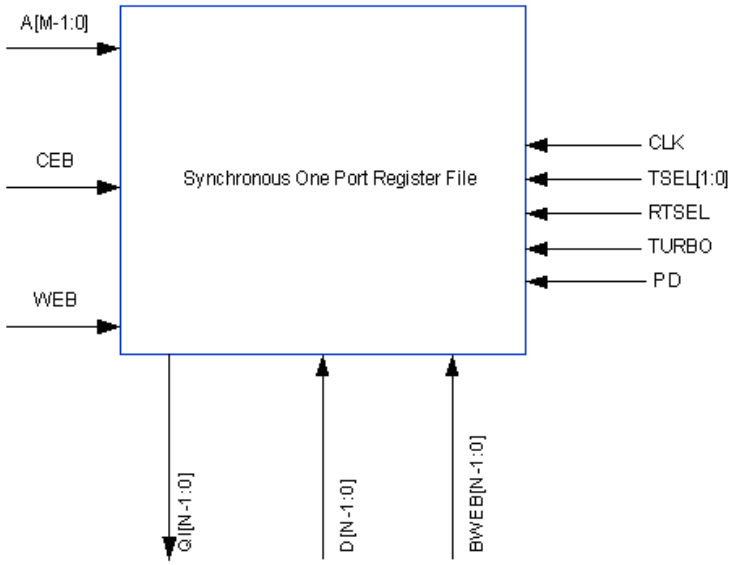


Figure 3.1 block diagram

The one-port register file is synchronized and triggered by the rising edge clocks, CLK. Input address A, input data D, chip enable CEB, and write enable WEB are latched by the rising edge of the clock. The following explains operation of the one port register file.

Read operation: The chip enable, CEB must be low and WEB stays high when triggered by CLK rising edge. Data is read and then transmitted to output bus Q[N-1:0] from memory location specified by A[M-1:0].

Write operation: The chip-enable, CEB and write-enable, WEB must be low when triggered by CLK rising edge. Data latched on D[N-1:0] that enters memory location specified by address A[M-1:0]. The bit-write feature is controlled by BWEB[N-1:0].

Chapter 4: Compiler Supporting Range

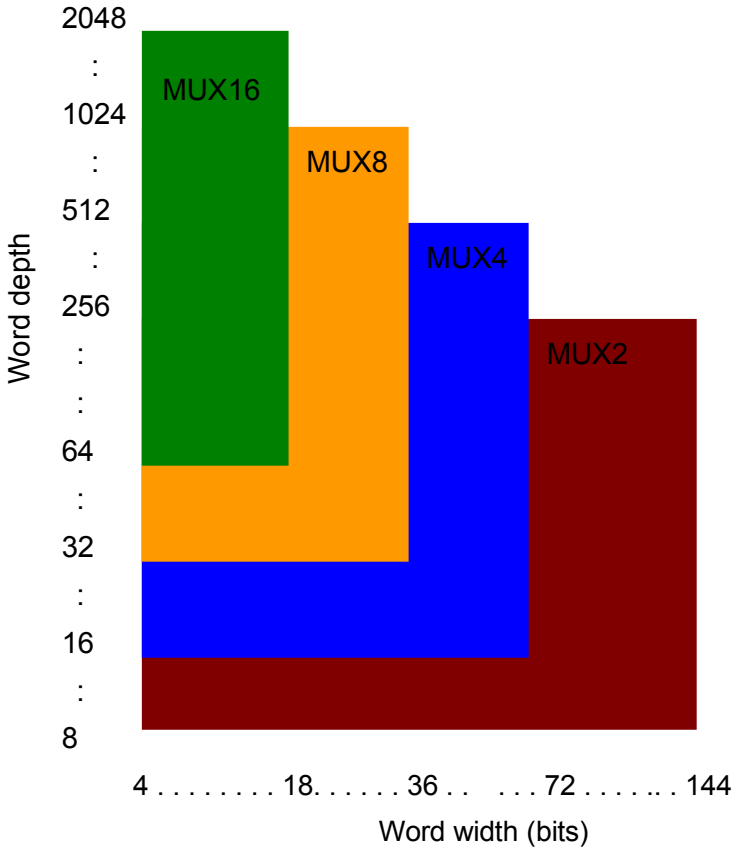


Figure 4.1 Available SRAM Configurations

This SRAM compiler provides wide range of embedded SRAM instances with very friendly environment. The variety range of SRAM configurations are described in Table 4.1 and Table_4.2.

Total Mux16(63x15) + Mux8(63x33) + Mux4(63x69) + Mux2(63x141) = 16,254 kinds of configuration are supported in this SRAM compiler.

One-port register file can be customized by column-mux option CM, number of words, W, number of bits per word, N and number of rows per segment, SEG. The valid range for these parameters is specified in the following table.

Table 4.1 SRAM Compiler Configuration Range for SVT

SEG option	Mux Option	Word Size	Bits
		(Address Locations)	(Number of I/Os)
SEG	CM	W	N
S	2	20,24…256	4,5,6…144
	4	40,48,56…512	4,5,6…72
	8	80,96,112…1024	4,5,6…36
	16	160,192,224…2048	4,5,6…18

Table 4.2 SRAM Compiler Configuration Range for LVT

SEG option	Mux Option	Word Size	Bits
		(Address Locations)	(Number of I/Os)
SEG	CM	W	N
S	2	8,12,16…256	4,5,6…144
	4	16,24,32…512	4,5,6…72
	8	32,48,64…1024	4,5,6…36
	16	64,96,128…2048	4,5,6…18

Note:

Compiler SEG option was changed to S only against to v120a and the supporting range remains the same. That of using “S”-segment type brings smaller area and the speed performance is comparable to “F”-segment instances as well; thus “F”-segment option is removed from v120b release.

Compiler and instance naming

SRAM cell:

SVT periphery: ts5n40lphsa{word_depth}x{word_width}m{mux}{seg}_{version}

LVT periphery: ts5n40lphslvta{word_depth}x{word_width}m{mux}{seg}_{version}

For example

SRAM cell: ts5n is designated for 1PRF SRAM compiler

Naming	W	N	CM	SEG	Version
ts5n40lphsa256x144m2s_200a	256	144	2	s	200a
ts5n40lphsa512x72m4s_200a	512	72	4	s	200a

Chapter 5: Pin Descriptions and Logic Truth Table

Pin Description

Pin	Type	Description
VDD	Power Supply	Power bus
VSS/GND	Power Supply	Ground bus
A[M-1:0]	Input	Address input
D[N-1:0]	Input	Data input
CLK	Input	Clock input
CEB	Input	Chip enable, active low
WEB	Input	Write enable, active low
BWEB[N-1:0]	Input	Bit write enable, active low
PD	Input	Power down enable, active high
TSEL[1:0]	Input	Timing adjustment for debug purpose
RTSEL	Input	Read timing setting for debug purpose
TURBO	Input	Read timing setting for debug purpose
Q[N-1:0]	Output	Data output

Note

User must connect the following two pins to the correct logic value

1. TURBO= High
2. RTSEL= Low

Logic Truth Table

Delay Control

Delay Mode	TSEL[1]	TSEL[0]	Purpose
Normal Use	L	H	Default mode of operation
Fast	L	L	Internal timings accelerated for high performance screen
Slow1	H	L	Internal timings slowed for diagnostics
Slow2	H	H	Internal timings slower than Slow1 for diagnostics

Note

1. TSEL[1:0] default setting is “01”
2. The other settings are for debugging purpose only

SRAM Function

Stage	CLK	CEB	WEB	BWEB	D	A	Q	Memory contents
Standby	L	H	-	-	-	-	No change	No change
Deselect	↑	H	-	-	-	-	No change	No change
Write bit[i]	↑	L	L	L	d[i]	a	No change	mem[**a**][i]=d[i]
Read	↑	L	H	-	-	a	mem[a][i]	No change
Write bit[i] mask	↑	L	L	bit[i]=H	-	a	No change	No change in mem[**a**][i]

Power Down Mode

Mode	PD	CLK	CEB	BWEB	D	A	Q	Memory contents
Power Down	H	-	H	-	-	-	L	No change

Note

1. The verilog model doesn't support the control enable, data, and address signals transition at positive clock edge. Please have some timing delays between control/data/address and clock signals to ensure the correct behavior.
2. In a non-fully decoded array, a write cycle to a nonexistent address location does not change the memory array contents and output remains the same.
3. In a non-fully decoded array, a read cycle to a nonexistent address location does not change the memory array contents but the output becomes unknown.
4. In the verilog model, the behavior of unknown clock will corrupt the memory data and make output unknown regardless of CEB signal. But in the silicon, the unknown clock at CEB high, the memory and output data will be held. The verilog model behavior is more conservative in this condition.
5. Rising and falling signals are measured at 50% of VDD.
6. Rising and falling slews are measured at 10% and 90% of VDD.

7. The verilog model provides UNIT_DELAY mode for the fast function simulation. All timing values in the specification are not checked in the UNIT_DELAY mode simulation. The behaviors still follow the truth table as above.

Memory x/z exception

PD	CLK	CEB	WEB	A	BWEB	D	Memory contents	Output Q
x/z	-	-	-	-	-	-	all x	x
L	x/z	-	-	-	-	-	all x	x
L	L->H	x/z	-	-	-	-	all x	x
L	L->H	L	x/z	-	-	-	all x	x
L	L->H	L	H	x/z	-	-	hold	x
L	L->H	L	L	x/z	-	-	all x	hold
L	L->H	L	H	valid	x/z	-	hold	data-out
L	L->H	L	L	valid	x/z	-	mem[A] = x	hold
L	L->H	L	H	valid	valid	x/z	hold	data-out
L	L->H	L	L	valid	valid	x/z	mem[A][i] = x	hold

Used term for truth table

Condition:

L: logic low

H: logic high

x/z: unknown or high impedance

-: Logic low, logic high or Unknown. Not include high impedance

valid: Address and BWEB only. It means stable(0 or 1); in fixed condition

L->H: clock only, rising edge

Output Q:

hold : keep previous state

x : unknown (either logic low or logic high)

L : logic low

data-out: Output of normal read function

Memory contents:

mem[A] = x: memory content is unknown at the specific memory address

mem[A][i] = x: memory content is unknown at the specific memory address and specific IO

hold: keep previous state

all x: store unknown to all memory address

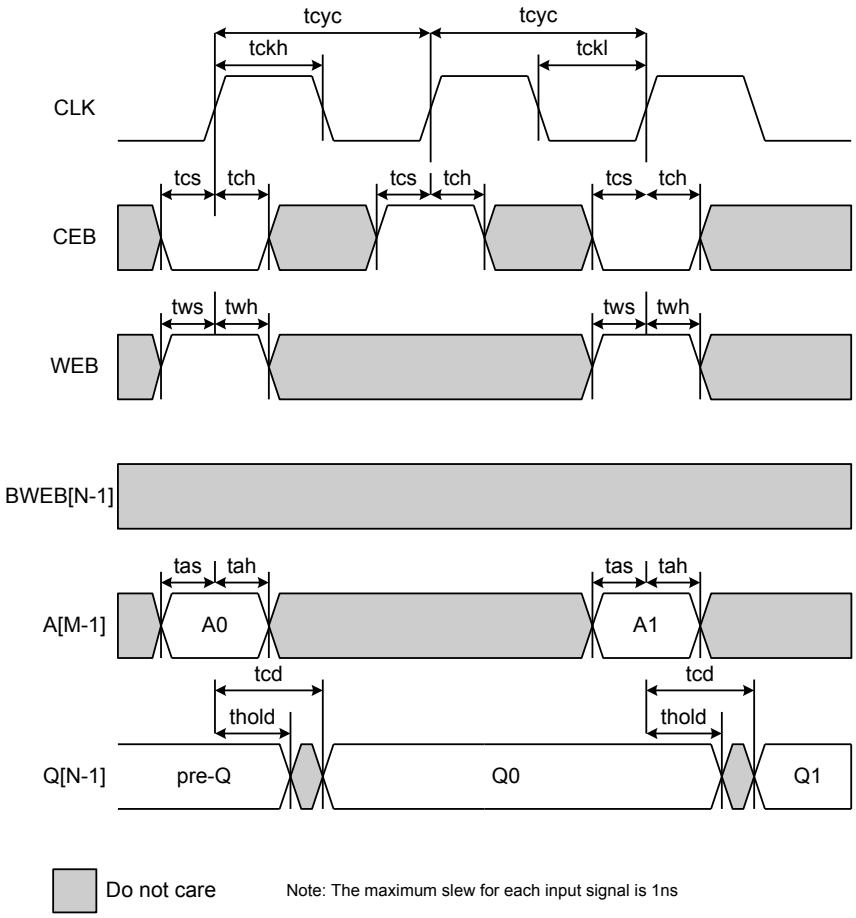
Chapter 6: Timing Specifications

Input Timing Requirements (please refer to Quick Reference Table)

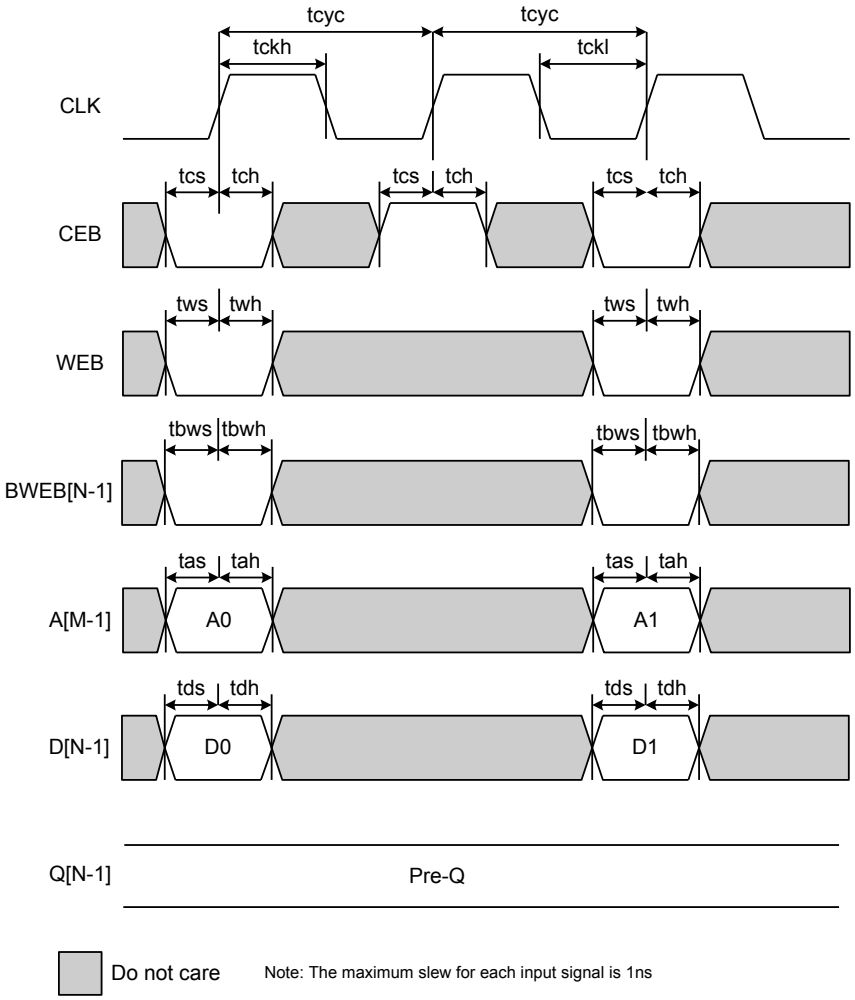
Normal Mode

Symbol	Parameter	From	To
tcyc	Minimum Cycle time	CLK ↑	CLK ↑
tcd	CLK to valid Q	CLK ↑	Q
thold	CLK to invalid Q	CLK ↑	Invalid Q
tas	Address setup	A	CLK ↑
tah	Address hold	CLK ↑	A
tcs	Chip enable setup	CEB	CLK ↑
tch	Chip enable hold	CLK ↑	CEB
tws	Write enable setup	WEB	CLK ↑
twh	Write enable hold	CLK ↑	WEB
tbws	Bit-write enable setup	BWEB	CLK ↑
tbwh	Bit-write enable hold	CLK ↑	BWEB
tds	Data setup	D	CLK ↑
tdh	Data hold	CLK ↑	D
tckh	Clock high	CLK ↑	CLK ↓
tckl	Clock low	CLK ↓	CLK ↑

Timing waveform of Normal Mode Read Cycle with bit-write mask



Timing waveform of Normal mode Write cycle with bit-write mask



Chapter 7: Process Voltage and Temperature (PVT) Characterization Conditions

PVT	Process	Voltage (V)	Temperature (C)	Note
FF1P21V0C	FF	1.21	0	Vdd+10%
FF1P21VM40C	FF	1.21	-40	Vdd+10%
FF1P21V125C	FF	1.21	125	Vdd+10%
TT1P1V25C	TT	1.1	25	Vdd
SS0P99V125C	SS	0.99	125	Vdd-10%
SS0P99VM40C	SS	0.99	-40	Vdd-10%
SS0P99V0C	SS	0.99	0	Vdd-10%
FFG1P21V125C	FFG	1.21	125	Vdd+10%

Note

1. FFG/1.21V/125C corner is supported as one extra pvt corner in NLDM and only leakage data is provided
2. The MLG corner is for leakage estimation only and cannot be used for timing and active power sign off
3. Permanent damage could occur if the operation exceeds the table listing above

Chapter 8: Power/Ground Connection Guideline

In chip design level, users must guarantee to meet the Vccmin spec(>= Vdd-10%) at the SRAM IP boundary to avoid performance impact from voltage drop of system power.

In order to have better IR drop and EM management, please follow the power/ground connection guideline below.

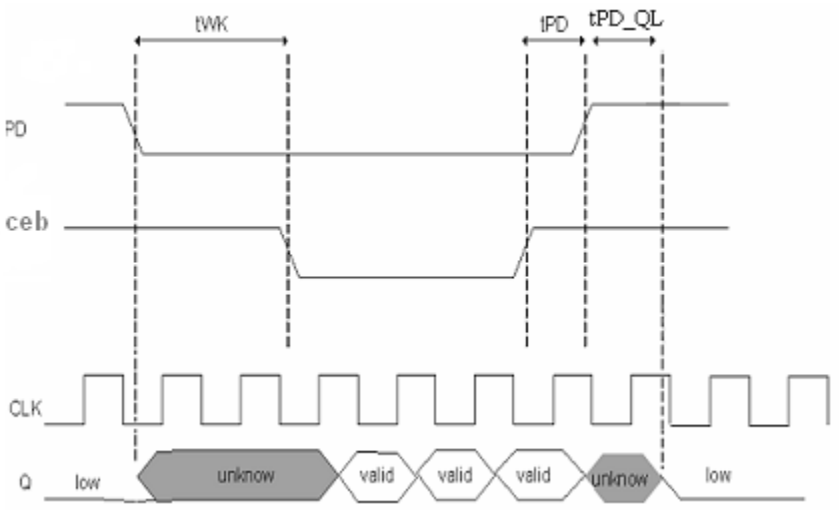
- All power and ground pins **MUST** be connected to VDD and VSS, respectively
- Route M5 power lines over the SRAM instances and cover as much area as possible
- Connect M4 VDD/VSS power lines thru via as much as possible
- M5 power/signal lines must be placed perpendicularly to M4 and drop VIAs
- Multiple connections along each power pin is recommended to further reduce IR drop

Chapter 9: Power Saving Mode and Power Down Requirements

The Power Down(PD) pin is a low leakage mode by periphery power partially switch off, an active-high input which may be used to reduce leakage power on a memory during periods of time when sram is not being used. No read or write cycles may take place while PD is asserted, but data will still be retained in the memory cells. Also, the output Q will be forced to logic low rather than allowed to be floating.

It is required that the memory have one inactive cycle (rising edge of either CLK with the associated CEB input high, or inactive), and no intervening read or write cycle before PD is asserted.

After PD is de-asserted, it is required that the memory has eight inactive cycles, with no intervening read or write cycles, before the first active (read or write) cycle.



Symbol	Parameter	From	To
tWK	Wake up time (from leaving PD mode)	PD	CEB
tPD	Idle time (to enter PD mode)	CEB	PD
tPD_QL	Delay time (from PD to Q held low)	PD	Q

Chapter 10: Scramble Diagram

BL[i] and BLB[i] mean the bit-line and the complement of bit line. When write cycle, if the D[0]=1;row address =1 and column address A[2:0]=001, then the WL[1] is active and the pair of BL[1] and BLB[1] is selected. BL[1] keeps high and BLB[1] discharges to logic 0, the selected bit cell stores logic 1.

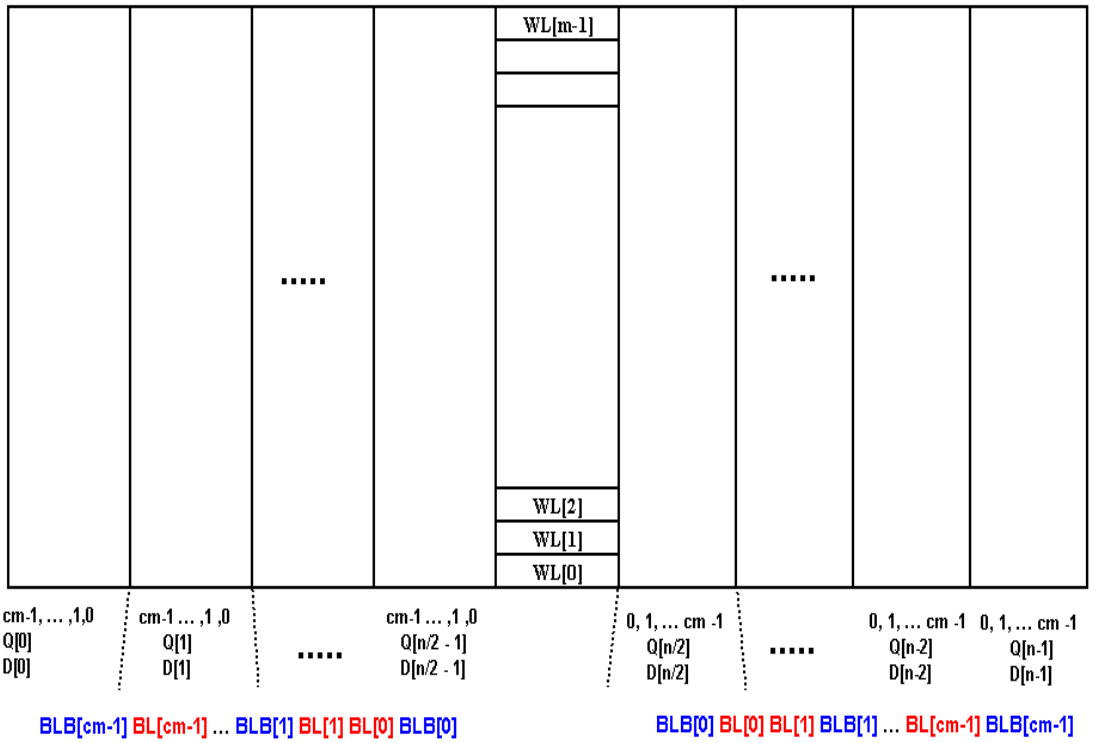


Figure 10.1 scramble table

Note:
cm : the number of column-mux
m : the number of row
n : the number of word width(bits)

If n is equal to even number, all IO(bits) will be allocated evenly into left and right bank, namely each bank has the same number of IO(bits), whereas, if n is equal to odd number, left bank always has one more IO(bit) than right bank.

Example 1: For word-depth=1024, Mux = 8, WL number = 1024/8 = 128 = 2^7

Column Mux Decode	A[2:0]
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Word line Decode	A[9:3]
WL[1]	0000,001
WL[5]	0000,101

Example 2: For word-depth=256, Mux = 4, WL number = 256/4 = 64 = 2^6

Column Mux Decode	A[1:0]
0	00
1	01
2	10
3	11

Word line Decode	A[7:2]
WL[0]	000,000
WL[7]	000,111

Chapter 11: Quick Reference Table

Symbol	Description
type	Compiler type
word	Word depth
io	Word width (Bit number)
mux	Column mux
seg	Segment type (bit-line partition)
drawing dimension area	Macro size in GDS layout
access_time	Access_time (CLK to output Q)
cycle_time	Cycle_time
adr_setup	Address setup time
adr_hold	Address hold time
data_setup	Data setup time
data_hold	Data hold time
readc	Read current, excludes pin power
writec	Write current, excludes pin power
leakage	Static current
leakage_pd	Static power in power down mode
leakage_ffg	Static power in FF global corner
Total (k)bits	(word * io) / 1024

The timing data is based on output load 0.002pf and the input slew for each condition

Voltage	Input slew
1.21V	0.0048ns
1.1V	0.0064ns
0.99V	0.0080ns

Please also refer to the following file for details.
“tsn40lphs1prf_20100400_200a_Quick_Reference_Table.pdf”