TSN40LPHSD242SPSRAM

TSMC 40nm Low Power High Performance
Single Port SRAM Compiler Databook

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Chapter 1 : Compiler General Description

Low power VLSI technology becomes increasingly important in the growing area of electronic industry. In order to provide the solution of low power application, TSMC 40nm low power high performance SRAM compiler is provided.

TSMC 40nm Low Power Synchronous Single Port SRAM (LPSSP) compiler is high performance, low power, and fabricated in TSMC CLN40LP (1.1V) CMOS low power technology. This SRAM operates at a voltage of 1.1V +/- 10% and a junction temperature range of -40°C to 125°C. The available SRAM size is configured from 1K bits to 312K bits as shown in Fig 3.1. The compiled SRAMs are divided into 3 groups according to their column-selected numbers (Mux=4, Mux=8 and Mux16). The “word depth” is defined as the number of words and the “word width” is defined as the number of bits per word.

Chapter 2 : Features

TSMC 40nm LP SPSRAM compiler has the following features:

- TSMC 1P10M 40nm CLN40LP (1.1V) CMOS process
- Synchronous operation
- Three column-mux options can be chosen, such as 4, 8 and 16.
- High density 6T SRAM bit cell 0.36 X 0.83 = 0.299um^2 (drawing dimension) and the physical SRAM bit cell area is 0.324 X 0.747 = 0.242um^2
  MT form: HD; cell imp mask: 112(VTC_N) and 199(VTC_P)
- Over SRAM routing for metal 4 and above
- Support global EDA models and precise timing characterization data
- Near-Zero Hold Time (data, address, and control inputs)
- Bit-write function (BWEB) option with each data input
- Power down mode to achieve lower leakage
- AWT (Asynchronous Write Through) pin which can be turned on or off.
- BIST interface for data, address, and control inputs

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Block Diagram:

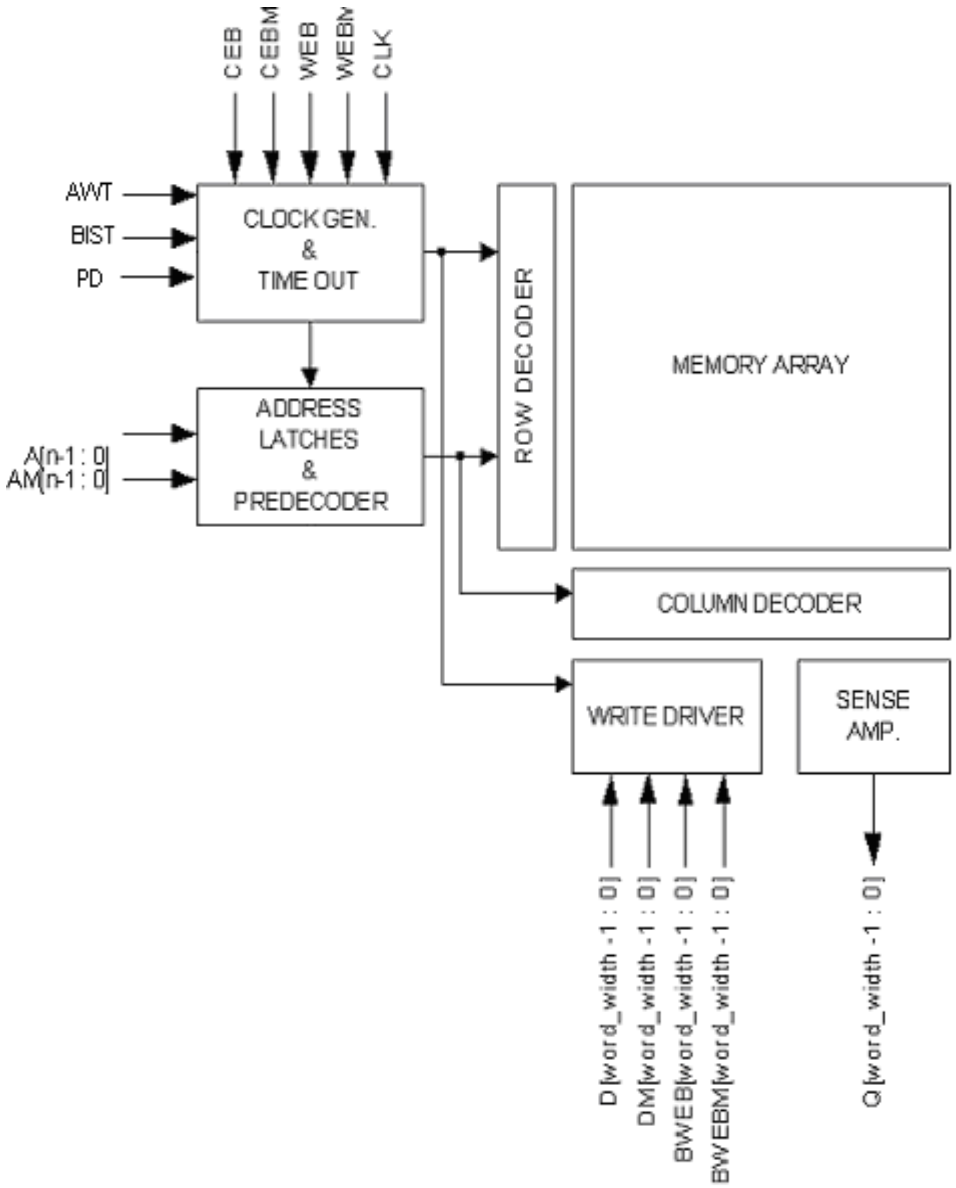

Figure2.1 Function Block

The single port SRAM is synchronized and triggered by a rising edge clock, CLK. Input address A, input data D, chip enable CEB, and write enable WEB are latched by the rising edge of the clock. The following explains operation of the single port synchronous SRAM.

Read operation: The chip enable, CEB must be low and WEB stays high when triggered by CLK rising edge. Data is read and then transmitted to output bus Q [k-1:0] from memory location specified by A [n-1:0].

Write operation: The chip-enable, CEB and write-enable, WEB must be low when triggered by CLK rising edge. Data latched on D [k-1:0] that enters memory location specified by address A [n-1:0]. The bit-write feature is controlled by BWEB [k-1:0].

Normal / BIST mode: The Normal / BIST mode operation is controlled by BIST. In normal mode, BIST must be low. In BIST mode, BIST must be high.

AWT function: The AWT (Asynchronous Write Through) mode is enabled by AWT pin. In AWT mode, the output pins receive the value from input pins in specified time delay (regardless of clock). Use AWT option to get better test coverage.

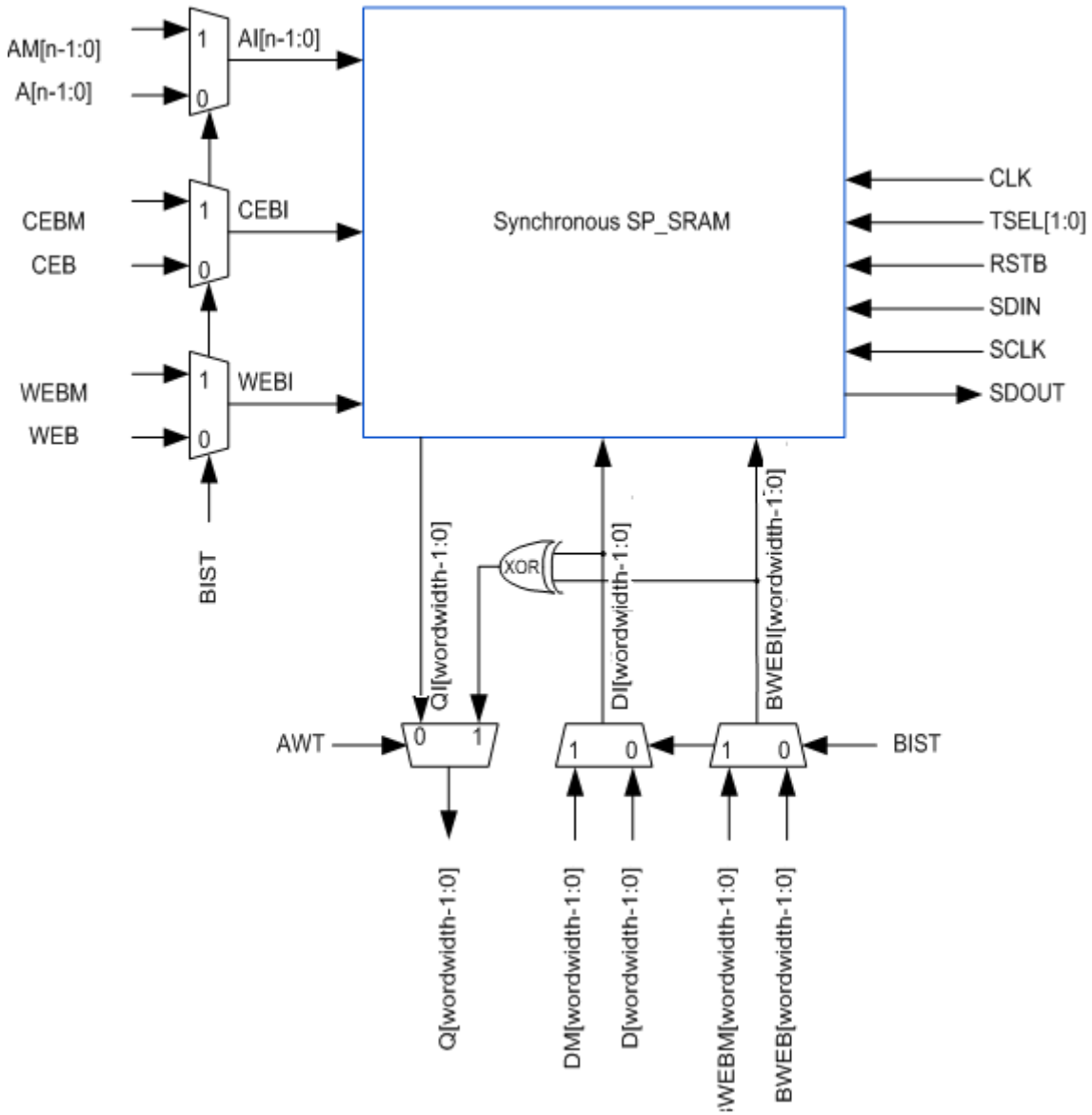

Figure2.2 BIST and AWT function block

Note: Non-Segment structure has no AWT function

Chapter 3 : Compiler Supporting Range

This compiler can be customized by column mux option **CM**, number of words **W**, and number of bits per word **N**. and number of rows per segment, **SEG.**

This compiler provides two kinds of design architecture:

1. Non-Segment design (Single Bank):

Compiler and instance naming convention:

SVT periphery: ts1n40lphs**sb**svtb{**W**}x{**N**}m{**CM**}{wb}_{version} or user defined library name

LVT periphery: ts1n40lphs**sb**lvtb{**W**}x{**N**}m{**CM**}{wb}_{version} or user defined library name

The supporting range is as follows: increment of Word Depth = CM*2

Mux Options	Word Depth (Address locations)	Bits (Number of I/Os)
CM	W	N
4	128,136,144...2048	8,9,10...144
8	256,272,288…4096	4,5,6...72
16	512,544…8192	2,3,4…39

Figure 3.1: Available SP SRAM Compiler Configurations for non-Segment

2. Segment design (Multi Bank):

SVT periphery: ts1n40lphs**mb**svtb{**W**}x{**N**}m{**CM**}{**SEG**}{wba}_{version} or user defined library name

LVT periphery: ts1n40lphs**mb**lvtb{**W**}x{**N**}m{**CM**}{**SEG**}{wba}_{version} or user defined library name

The supporting range is as follows: increment of Word Depth = CM*2

SEG option	Mux Option	Word Depth (Address Locations)	Bits (Number of I/Os)
SEG	CM	W	N
F	4	128,136,144...2048	8,9,10…144
	8	256,272,288...4096	4,5,6…72
	16	512, 544, 576…8192	2,3,4…39
S	4	1024,1032,1040...8192	8,9,10…144
	8	2048,2064,2080...16384	4,5,6…72
	16	4096,4128,4160…32768	2,3,4…39

Figure 3.2: Available SP SRAM Compiler Configurations for Segment

For example: ts1n represents SP SRAM, “b” stands for d242 cell

Naming	W	N	CM	SEG	VT	BWEB	BIST	AWT	Version
ts1n40lphssbsvtb256x144m4_250a	256	144	4	no	svt	No	No	No	250a
ts1n40lphssblvtb512x72m8_250a	512	72	8	no	lvt	No	No	No	250a
ts1n40lphsmbsvtb8192x144m4swba_250a	8192	144	4	s	svt	Yes	Yes	Yes	250a
ts1n40lphsmblvtb4096x72m8fwba_250a	4096	72	8	f	lvt	Yes	Yes	Yes	250a

Chapter 4 : Pin Descriptions

SRAM macro: ts1n40lphs{vt}b{word_depth}x{word_width}m{mux}{seg}{wba}_250a;

Word_depth = 2^n

Pin	Type	Description
VDD	Supply	Power bus
VSS/GND	Supply	Ground bus
A[0]~A[n-1]	Input	Address input
AM[0]~AM[n-1]	Input	Address input for BIST
D[0]~D[word_width - 1]	Input	Data input
DM[0]~DM[word_width – 1]	Input	Data input for BIST
CLK	Input	CLK input
CEB	Input	Chip enable, active low for SRAM operation; active high for fuse data setting
CEBM	Input	Chip enable for BIST, active low for SRAM operation; active high for fuse data setting
WEB	Input	Write enable, active low
WEBM	Input	Write enable for BIST, active low
BWEB[0]~BWEB[word_width - 1]	Input	Bit write enable, active low
BWEBM[0]~BWEBM[word_width -1]	Input	Bit write enable, active low
Q[0]~Q[word_width – 1]	Output	Data output
BIST	Input	BIST enable
PD	Input	Power down mode
AWT*	Input	Asynchronous write through

NOTE: *Non-Segment design has no AWT pin

nonBWEB cannot be in-pair with AWT option

Chapter 5 : Logic Truth Table

BIST Mode

Mode	BIST	Chip Select	Read/Write	Bit-write mask	Address	Data in
Normal	Low	CEB	WEB	BWEB	A	D
BIST	High	CEBM	WEBM	BWEBM	AM	DM

SRAM Function

Stage	PD	CLK	CEB	WEB	BWEB	D	A	Q	Memory contents
Standby	Low	High	High	-	-	-	-	No change	No change
Standby	Low	Low	High	-	-	-	-	No change	No change
Power down	High	-	High	-	-	-	-	Low	No change
Write bit[i]	Low	↑	Low	Low	Low	d[i]	a	**No change**	Mem[a][i]=d[i]
Read	Low	↑	Low	High	-	-	a	Mem[a][i]	No change
Write bit[i] mask	Low	↑	Low	Low	bit[i]=High	-	a	No change	No change in mem**[a][i]**

Asynchronous Write Through

AWT	D	BWEB	Q
High	d[i]	b[i]	b[i] (xor) d[i]

NOTE: AWT must be in-pair with BWEB option

Note:

1. The verilog model doesn't support the control enable, data, and address signals transition at positive clock edge. Please have some timing delays between control/data/address and clock signals to ensure the correct behavior.
2. In a non-fully decoded array, a write cycle to a nonexistent address location does not change the memory array contents and output remains the same.
3. In a non-fully decoded array, a read cycle to a nonexistent address location does not change the memory array contents but the output becomes unknown.
4. In the verilog model, the behavior of unknown clock will corrupt the memory data and make output unknown regardless of CEB signal. But in the silicon, the unknown clock at CEB high, the memory and output data will be held. The verilog model behavior is more conservative in this condition.
5. Rising and falling signals are measured at 50% of VDD.
6. Rising and falling slews are measured at 10% and 90% of VDD.
7. The verilog model provides UNIT_DELAY mode for the fast function simulation. All timing values in the specification are not checked in the UNIT_DELAY mode simulation. The behaviors still follow the truth table as above.
8. Non-Segment structure has no AWT function.

Memory x/z exception

PD	BIST	AWT	CLK	CEB	WEB	A	BWEB[i]	D[i]	mem	Output Q
x/z	-	-	-	-	-	-	-	-	all x	x
L	x/z	-	-	-	-	-	-	-	all x	x
L	L	x/z	-	-	-	-	-	-	hold	x
L	L	L	x/z	-	-	-	-	-	all x	x
L	L	L	↑	x/z	-	-	-	-	all x	x
L	L	L	↑	H	-	-	-	-	hold	hold
L	L	L	↑	L	x/z	-	-	-	all x	x
L	L	L	↑	L	H	x/z	-	-	hold	x
L	L	L	↑	L	L	x/z	-	-	all x	hold
L	L	L	↑	L	H	valid	x/z	-	hold	data-out
L	L	L	↑	L	L	valid	x/z	-	mem[A][i] = x	hold
L	L	L	↑	L	H	valid	L	x/z	hold	data-out
L	L	L	↑	L	L	valid	L	x/z	mem[A][i] = x	hold

Note: Non-Segment structure has no AWT function.

Used term for truth table

Condition:

L: logic low

H: logic high

x/z: unknown or high impedance

-: Logic low, logic high or Unknown. Not include high impedance

valid: Address and BWEB only. It means stable (0 or 1) in fixed condition

↑ Signal rising edge

Output Q:

hold: keep previous state

x: unknown

L: logic low

mem:

mem[A][i] = x: memory content is unknown at the specific memory address **and** specific **IO**

hold: keep previous state

all x: store unknown to all memory address

Chapter 6 : Timing Specifications

- Input Timing Requirements (please refer to **Quick Reference Table**)

SRAM read/write

Symbol	Parameter	From	To
tcd	Access time	CLK ↑	Q
thold	CLK to invalid Q	CLK ↑	Invalid Q
tos	Output slew time	Q	Q
tcs	Chip enable setup	CEB	CLK ↑
tch	Chip enable hold	CLK ↑	CEB
tas	Address setup time	A	CLK ↑
tah	Address hold time	CLK ↑	A
tws	Write enable setup	WEB	CLK ↑
twh	Write enable hold	CLK ↑	WEB
tbws	Bit-write enable setup	BWEB	CLK ↑
tbwh	Bit-write enable hold	CLK ↑	BWEB
tds	Data setup	D	CLK ↑
tdh	Data hold	CLK ↑	D
tcms	BIST Chip enable setup	CEBM	CLK ↑
tcmh	BIST Chip enable hold	CLK ↑	CEBM
tams	BIST Address setup time	AM	CLK ↑
tamh	BIST Address hold time	CLK ↑	AM
twms	BIST Write enable setup	WEBM	CLK ↑
twmh	BIST Write enable hold	CLK ↑	WEBM
tbwms	BIST Bit-write enable setup	BWEBM	CLK ↑
tbwmh	BIST Bit-write enable hold	CLK ↑	BWEBM
tdms	BIST Data setup	DM	CLK ↑
tdmh	BIST Data hold	CLK ↑	DM
tbists	BIST enable setup	BIST	CLK ↑
tbisth	BIST enable hold	CLK ↑	BIST
tcyc	Minimum CLK cycle	CLK ↑	CLK ↑
tckh	Minimum CLK Pulse High	CLK ↑	CLK ↓
tckl	Minimum CLK Pulse Low	CLK ↓	CLK ↑

Output Switching from AWT

Parameter	Symbol	From	To
tawtq	AWT to valid Q	AWT	Q
tbwq	BWEB to valid Q	BWEB	Q
tdq	D to valid Q	D	Q
tawtqh	AWT to invalid Q	AWT	Invalid Q
tbwqh	BWEB to invalid Q	BWEB	Invalid Q
tdqh	D to invalid Q	D	Invalid Q

Note: Non-Segment structure has no AWT function.

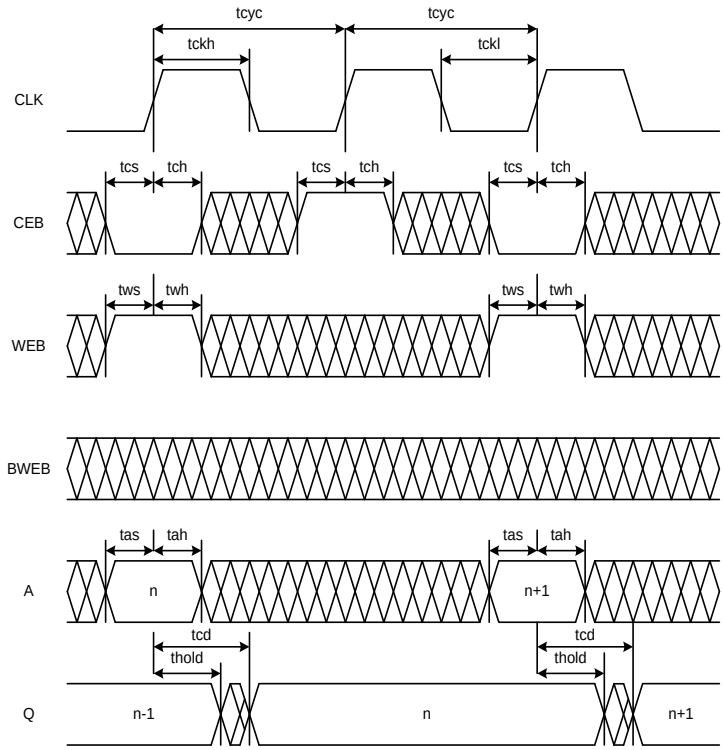

Figure 6.1 Timing waveform of Normal Mode READ cycle (BIST low)

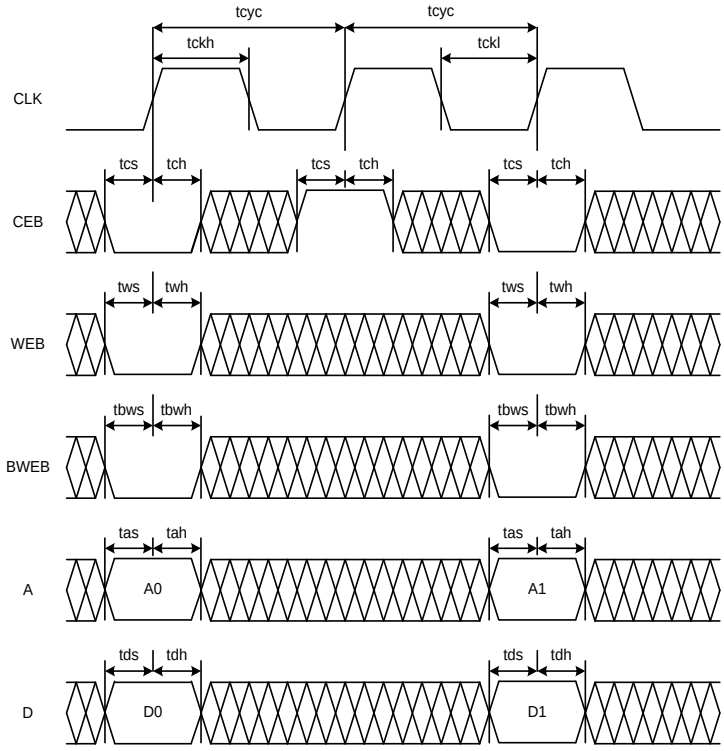

Figure 6.2 Timing waveform of Normal Mode WRITE cycle with bit-write mask

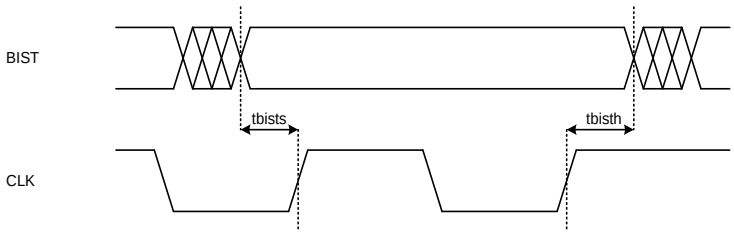

Figure 6.3 Timing waveform of BIST operation

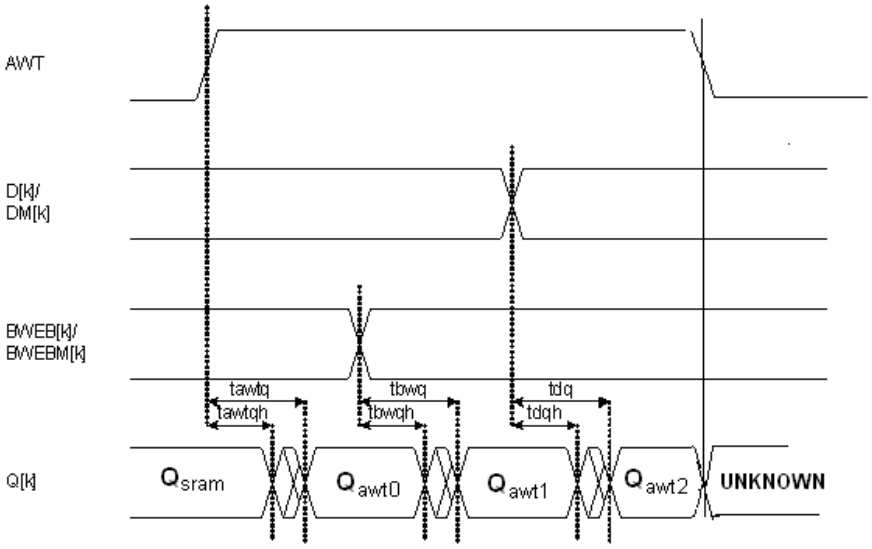

Figure 6.4 Asynchronous Write-through

Note: Non-Segment structure has no AWT function.

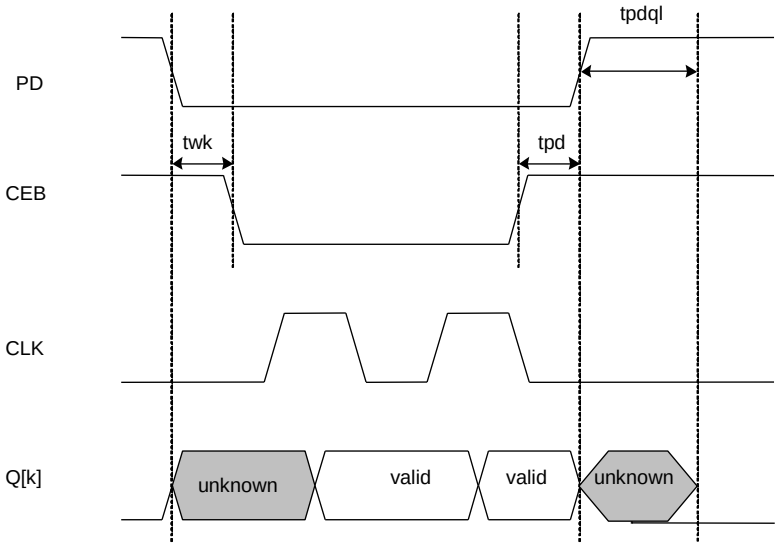

Figure 6.5 Timing waveform of Power down operation

Power Down Function

- Power Saving
  Save stand-by leakage power by switching off partial of the periphery circuit
- Behavior
  - PD pin is an asynchronous control input pin
  - PD pin is active high (1'b1 = power saving)
  - Chip enable signal should be disabled (CEB = 1'b1 or CEBM = 1'b1 as BIST mode)
  - **All input pins cannot be floating or unknown during power down mode (PD =1'b1)**
  - There is a SRAM data output wake up time from power-saving mode to normal stand-by mode (twk). Wake up time must be sufficiently guaranteed for instance to have healthy power supply
  - The SRAM data output (Q) is logic low when PD is activated (PD =1'b1)
  - When the values of data output (Q) changes from 0 (power-saving mode) to unknown-X (normal stand-by mode), there is no high-Z on output Q

Special Note:

Symbol	Parameter	From	To	Note
twk	Wake up time leaving PD mode	PD	CEB	Around 8 X SRAM minimum CLK cycle time.
tpd	Idle time entering PD mode	CEB	PD	Around 1 X SRAM minimum CLK cycle time
tpdql	Delay from PD to Q held low	PD	Q	-

Chapter 7 : Process Voltage and Temperature (PVT) Characterization Conditions

PVT	Process	Voltage (V)	Temperature (C)
SS0P99VM40C	SS	0.99	-40
SS0P99V0C	SS	0.99	0
SS0P99V125C	SS	0.99	125
TT1P1V25C	TT	1.1	25
FF1P21VM40C	FF	1.21	-40
FF1P21V0C	FF	1.21	0
FF1P21V125C	FF	1.21	125
FFG1P21V125C	FFG	1.21	125

Note:

1. **FFG1P21V125C corner is supported as one extra pvt corner in NLDM and only leakage data is provided.**
2. **Permanent damage could occur if the operation exceeds the table listing above.**

Chapter 8 : Power/Ground Connection Guideline

In chip design level, users must guarantee to meet the Vccmin spec(>= Vdd-10%) at the SRAM IP boundary to avoid performance impact from voltage drop of system power.

In order to have better IR drop and EM management, please follow the power/ground connection guideline below:

- All power and ground pins **MUST** be connected to VDD and VSS, respectively.
- Route M5 power lines over the SRAM instances and cover as much area as possible.
- M5 power/signal lines must be placed perpendicularly to M4 and drop VIAs in full of any cross-area of two metals.
- Fully populate the intersections of power rails and power pins with VIAs.
- Special attention should be made to the power connections close to the bottom of the memory array to power the IO buffers.
- Multiple connections along each power pin is recommended to further reduce IR drop.

Chapter 9 : Scramble Diagram

BL[i] and BLB[i] mean the bit-line and the complement of bit line. When write cycle, if the D[0]=1;row address =1 and column address A[2:0]=001, then the WL[1] is active and the pair of BL[1] and BLB[1] is selected. BL[1] keeps high and BLB[1] discharges to logic 0, the selected bit cell stores logic 1.

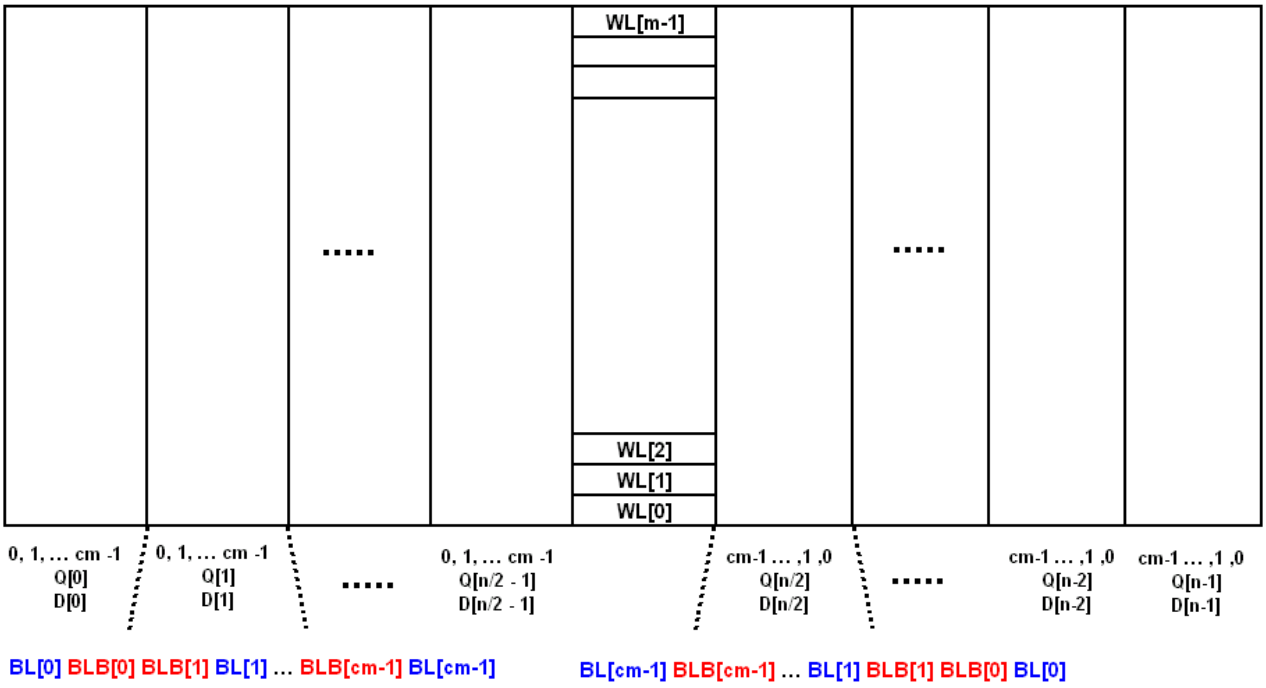

Figure9.1 scramble table

Note:
cm : the number of column-mux;
m : the number of row;
n : the number of word width(bits).
If n is equal to even number, all IO(bits) will be allocated evenly into left and right bank, namely each bank has the same number of IO(bits), whereas, if n is equal to odd number, left bank always has one more IO(bit) than right bank.

Example: For word-depth=2048, Mux = 4: WL number = 2048/4 = 512 = 2^9

Column Mux Decode	A[1:0]
0	00
1	01
2	10
3	11

Word line Decode	A[10:2]
WL[0]	00,0000,000
WL[7]	00,0000,111

Chapter 10 : Quick Reference Table

Symbol	Description
type	Compiler type
word	Word depth
io	I/O number
mux	Column mux
drawing dimension area	Macro area
access_time	Access time
cycle_time	Cycle time
adr_setup	Address setup time
adr_hold	Address hold time
data_setup	Data setup time
data_hold	Data hold time
readc	Read current, excludes pin power
writec	Write current, excludes pin power
leakage	Static power
leakage_pd	Static power in power down mode
leakage_ffg	Static power in FF global corner

The timing data is based on output load 0.00156 pf and the input slew for each condition is shown as below table.

Process	Input slew
FF	0.0048ns
TT	0.0064ns
SS	0.0080ns

Please reference the QRT pdf file:

TSN40LPHSD242SPSRAM_20100400_250A_Quick_Reference_Table.pdf