Project 4:
Pipelined Control Unit

Due: 4/6/2021
Points: 50

1 The Objective

The principle objective here is to demonstrate that you understand the basic operation of the construction of a pipelined control unit for a simple instruction set. At your discretion, you can work on this project in teams of $2-4$ individuals. It is solely your responsibility to form a team. I am not responsible for any team members performance issues, including a member's withdrawl from the class.

2 The Task

Design a pipelined control unit to implement the instruction set of the course processor specification from Project 3. Your design must include a pipelined solution that contains at least three pipeline stages. The three stages are: (i) instruction fetch, (ii) register operand fetch and effective address computation, and (iii) execute. You are free to develop a deeper pipeline structure with a different decomposition. **Your design needs to be setup to properly satisfy data and control (including exception) hazards.** Stalling is an acceptable solution but it will not get you optimization points. You are to design the data path, the control unit signaling, and the state machine to implement a hardwired control unit. You do not have to complete a gate level implementation of this design.

In addition to solving this problem, you are expected to deliver documentation to your solution that is well-organized, modular, and thoroughly described. You cannot simply turn in a complex design solution and expect credit. Part of your challenge is to discover a method to deliver a documented solution that is easy to study, digest, and understand. You will lose points if you do not develop a suitable presentation for your design solution.

3 Constraints

1. There are no hard constraints on the data path. You can have point-to-point connections, multiple buses, etc. You can have additional increment/decrement units as necessary. I only ask that you try to make reasonable decisions in this matter. Remember, you should add only what you really need and will use extensively. This is an optimization problem; additional structures work against you for optimization.

2. You can assume a memory model that has separate instruction and data ports. Thus, you can issue an instruction read simultaneously with a data read/write. You can assume that the memory operation will complete in one clock cycle (or at least it will appear to your control unit that way).

3. You can assume that you have a register file with 3 read ports and 2 write port that can all be accessed simultaneously.

4 The Report

Your report must clearly document your design solution. The documentation should include informal descriptions of the various components in your solution.

There are no limits on the length of the report. Good luck.