64Mbit IoT RAM

64Mbit SQPI PSRAM Introduction

Version 0.1

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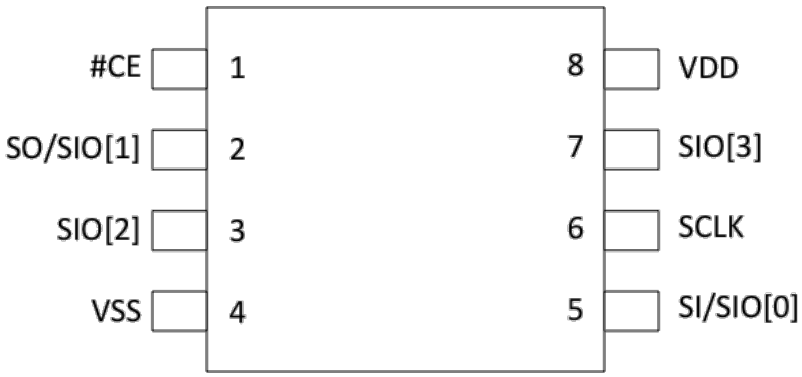
2 Introduction

This document defines "64Mbit IoT RAM", which is 64 Mbit of SPI/QPI (serial/quad parallel interface) Pseudo−SRAM device. This RAM is configurable as 1 bit Input and Output separate or 4 bit I/O common interface. The Linear Burst can cross page boundary within tCEM(max.). 32 bytes wrap burst mode is also available.

IoT RAM specification is standardized and IoT RAM technology is provided by AP Memory Technology. IPUS IoT RAM product is fully compliant with this IoT RAM specification.

3 Package Information

SOP 8(150mil) pin order



4 Ordering Information

Table 1 : Ordering information

Ordering Part number	Operational Voltage	Maximum Frequency	Temperature Range	Minimum Order Quantity
IPS6404L-SQ-SPN	2.7V ~ 3.6V	104Mhz	-25°C to +85°C	4Kunits
IPS6404L-SQL-SPN	1.62V ~ 1.98V	133Mhz		

5 Signal description

Table 2 : Signal description

Symbol	Signal Type	SPI Mode	QPI Mode
VDD	Power	Core Power Supply	
VSS	Ground	Core Supply Ground	
CE#	Input	Chip select signal, Active Low. When CE# input is High, memory will be in Standby state	
CLK	Input	Clock Signal	
SI/SIO[0]	I/O	Serial Input	I/O[0]
SO/SIO[1]	I/O	Serial Output	I/O[1]
SIO[3:2]	I/O	(I/O[3:2]*)	I/O[3:2]

*: Fast read Quad access and Quad Write access in SPI Mode use SIO[3:2]. Recommend to pull down to GND if no use of SIO[3:2] in SPI mode.

6 Basic Function Description

6.1 Address Space

SPI/QPI PSRAM device is byte−addressable. 64M device is addressed with A[22:0].

6.2 Page Length

The page size is 1K Bytes. Read and write operations are always linear address space. The Linear Burst can cross page boundary under following conditions.

- Operative Clock frequency ≤ 84Mhz
- CE# low pulse width ≤ tCEM(max.)

The wrap 32 burst mode can be set by “Burst mode toggle commend” optionally. There is no page boundary crossing function supported on wrap 32 burst mode.

6.3 Command/Address Latching Truth

The device recognizes the following commands specified by the various input methods

Table 3 : Command Table

		SPI Mode				QPI Mode			
Command	Code	Cmd	Addr	Wait Cycle	DIO	Cmd	Addr	Wait Cycle	DIO
Read	0x03	S	S	0	S	N.A.			
Fast Read	0x0B	S	S	8	S	N.A.			
Fast Read Quad	0xEB	S	Q	6	Q	Q	Q	6	Q
Write	0x02	S	S	0	S	Q	Q	0	Q
Quad Write	0x38	S	Q	0	Q	same as 0x02			
Enter Quad Mode	0x35	S	-	-	-	N.A.			
Exit Quad Mode	0xF5	N.A.				Q	-	-	-
Reset Enable	0x66	S	-	-	-	Q	-	-	-
Reset	0x99	S	-	-	-	Q	-	-	-
Burst mode toggle	0xC0	S	-	-	-	Q	-	-	-
Read ID	0x9F	S	S	0	S	N/A			

Remark: S = Serial IO, Q = Quad IO

*Note: 84Mhz is maximum operative clock frequency allows to cross the page boundary.

7 Waveform examples

7.1 SPI Read waveform example

The read data will be available t_{ACLK} after the falling edge of CLK.

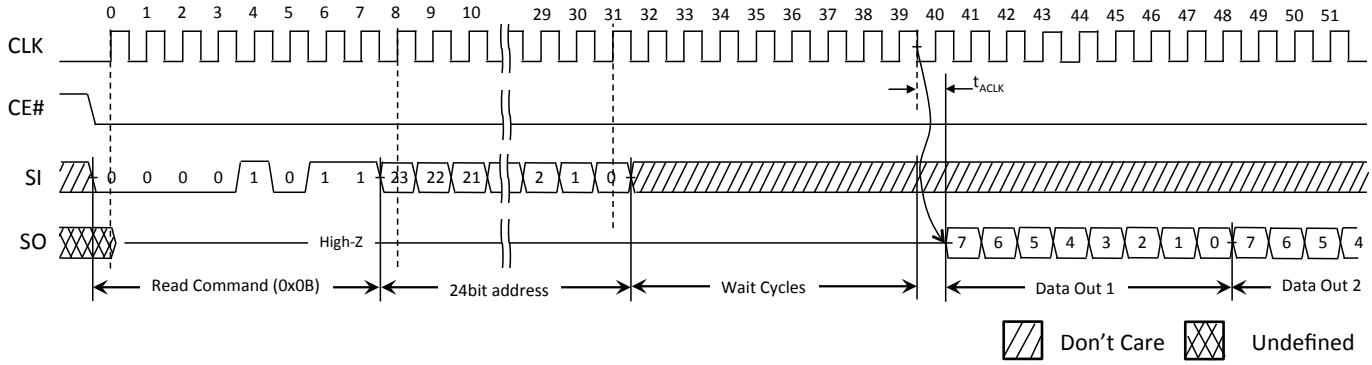


Figure 1 : SPI Read 0x0B (High frequency)

7.2 SPI Write wave form example

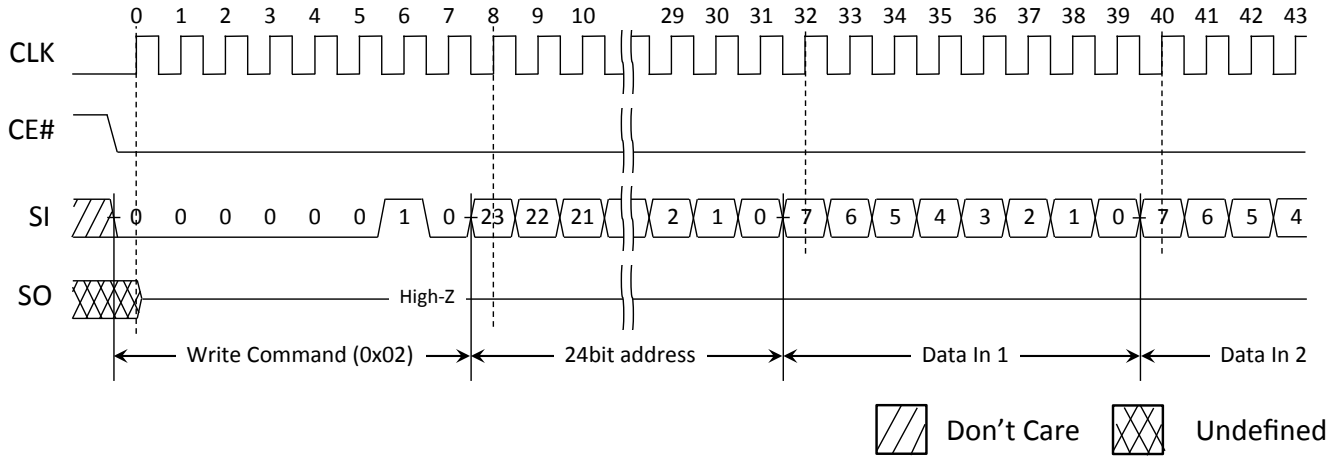


Figure 2 : SPI Write 0x02(High frequency)

7.3 QPI Read wave form example

The read data will be available t_{ACLK} after the falling edge of CLK.

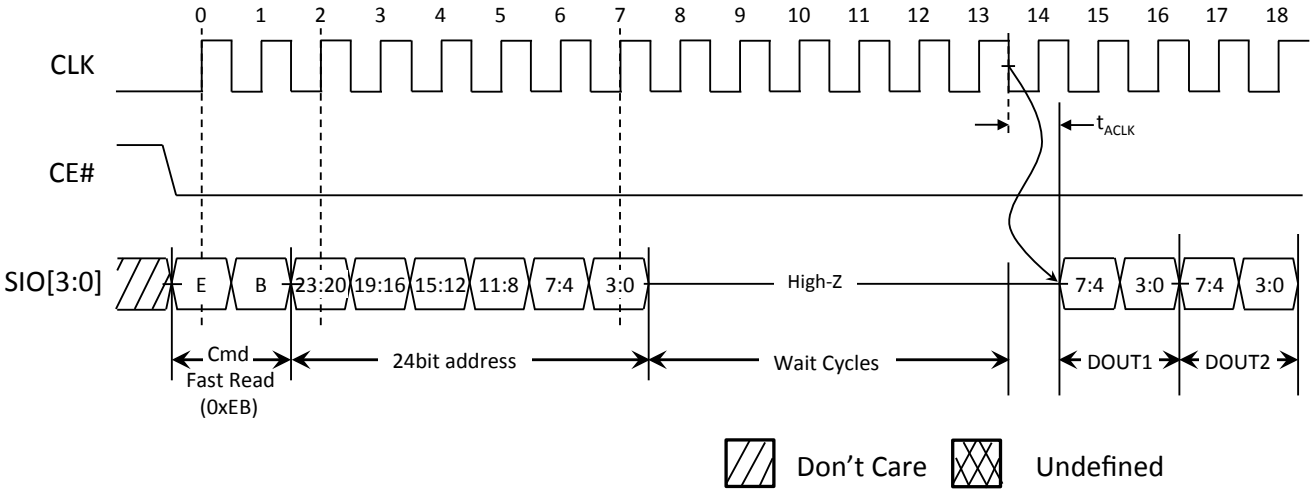


Figure 3: QPI Read (High frequency)

7.4 QPI Write wave form example

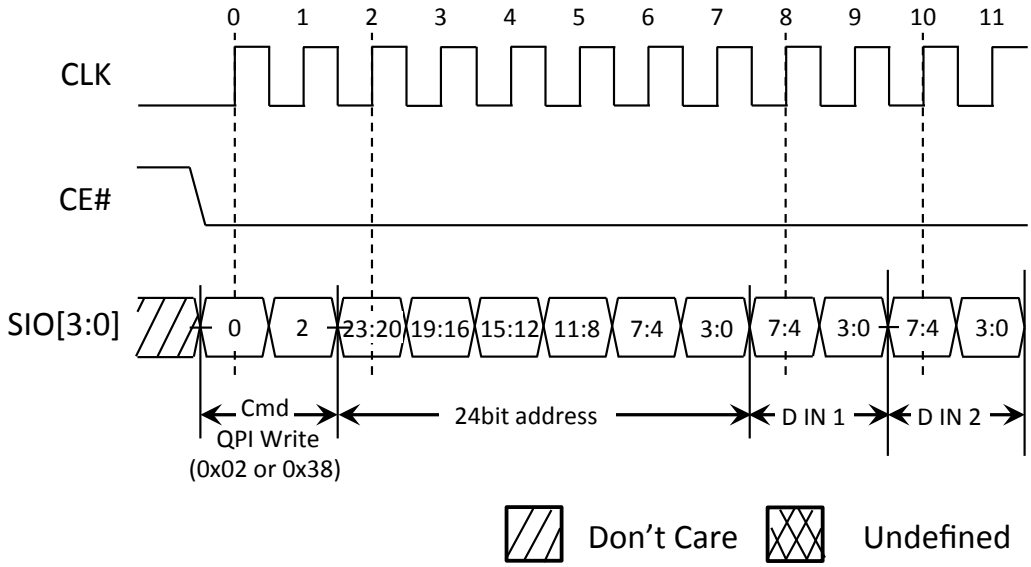


Figure 4 : QPI Write

This product introduction sheet is introducing fundamental features
For any further detail parameter inquiry, please contact IPUS Limited for data sheet.

8 Version History

Version 0.1	July17th, 2017	Initial Version