2 3 4 5

## **BOARD CHARACTERISTICS**

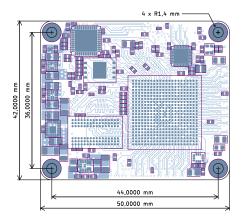
Copper Layer Count: 8 Board Thickness: 1,2396 mm

Board overall dimensions:  $50,0000 \text{ mm } \times 42,0000 \text{ mm}$ 

Min track/spacing: 0,0900 mm / 0,0900 mm Min hole diameter: 0,2000 mm

Copper Finish: ENIG Impedance Control: Yes Castellated pads: No Plated Board Edge: No

Edge card connectors: No



## Layer Stack Legend

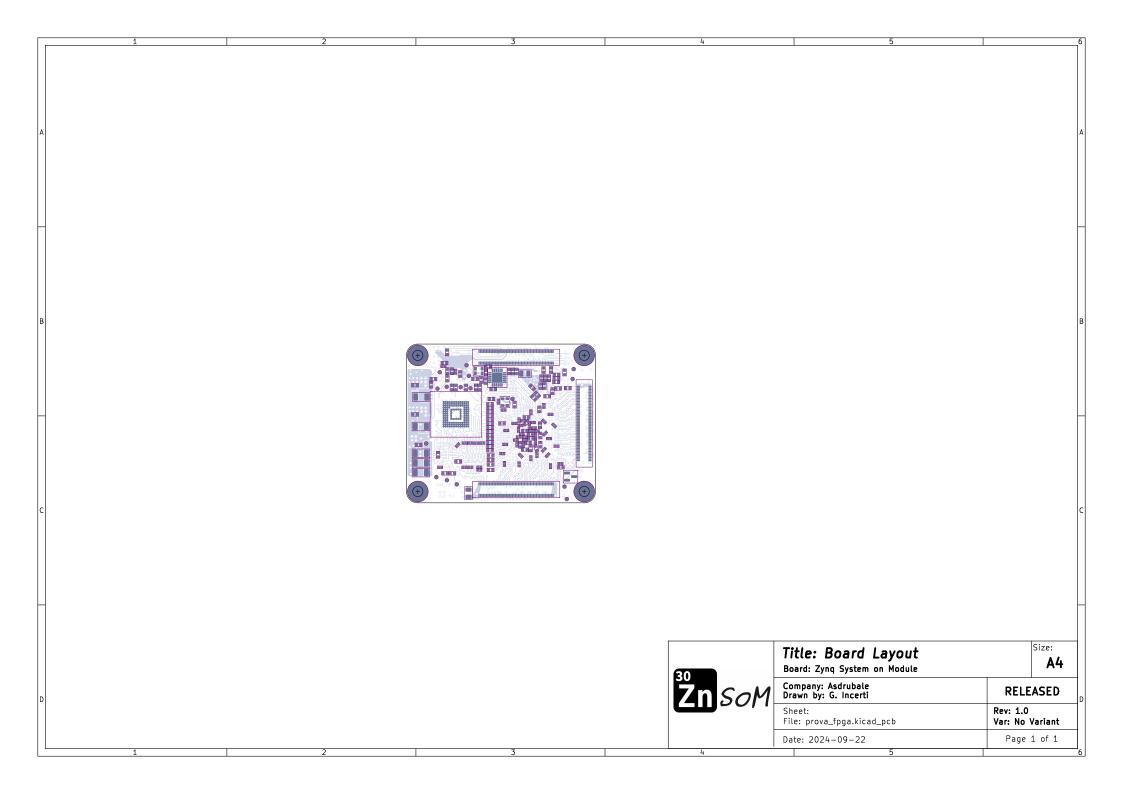
		Material	Layer	Thickness	Dielectric Material	Epsilon	Туре	Gerber
			B.Paste				Paste Mask	GTP
			B.Silkscreen				Legend	GT0
			B.Mask		Solder Resist		Solder Mask	GTS
		Copper	L1 (Sig)	0.035mm (1oz)			Signal	GTL
111111	///////////////////////////////////////	Prepreg		0.0764 mm	1080 RC67%	3.91	Dielectric	
=		Copper	L2 (GND)	0.0152mm (0.5oz)			Internal Plane	G2
1111.		Core		0.2 mm	FR-4	4.36	Dielectric	
		Copper	L3 (PWR)	0.0152mm (0.5oz)			Plane	G3
111111	///////////////////////////////////////	Prepreg		0.1528 mm	1080 RC67%	3.91	Dielectric	
-		Copper	L4 (Sig+Pwr)	0.0152mm (0.5oz)			Signal	G4
1111;		Core		0.2 mm	FR-4	4.36	Dielectric	
-		Copper	L5 (GND)	0.152mm (0.5oz)			Internal Plane	G5
111111		Prepreg		0.1528 mm	1080 RC67%	3.91	Dielectric	
-		Copper	L6 (Sig+Pwr)	0.0152mm (0.5oz)			Signal	G6
1111;		Core		0.2 mm	FR-4	4.36	Dielectric	
_		Copper	L7 (GND)	0.0152mm (0.5oz)			Internal Plane	G7
111111	///////////////////////////////////////	Prepreg		0.0764 mm	1080 RC67%	3.91	Dielectric	
		Copper	L8 (Sig)	0.035mm (1oz)			Signal	GBL
			B.Mask		Solder Resist		Solder Mask	GBS
			B.Silkscreen				Legend	GBO
			B.Paste				Paste Mask	GBP

## Impedance specification

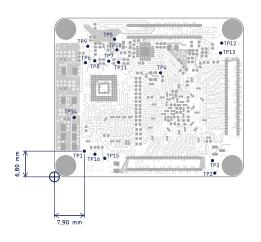
Copper	Layers	Impedance (Ohm)	Width (mm)	Spacing (mm)	Ref. Layers
Microstrip	L1 (L8)	50	0.120		L2 (L7)
Microstrip	L1 (L8)	90	0.1146	0.15	L2 (L7)
Microstrip	L1 (L8)	100	0.1	0.2	L2 (L7)
Microstrip	L1 (L8)	100	0.104	0.250	L2 (L7)
Stripline	L4 (L6)	52.7	0.135		L3,L5 (L5,L7)
Stripline	L4 (L6)	100	0.102	0.125	L3,L5 (L5,L7)

20	<b>Title: Board Layout</b> Board: Zynq System on Module	Size: A4	
Žn SoM	Company: Asdrubale Drawn by: G. Incerti	RELEASED	
	Sheet: File: prova_fpga.kicad_pcb	Rev: 1.0 Var: No Variant	
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1 2 3 4 5



SIGNAL X (mm) Y (mm) TP1 ZYNQ\_PL\_PROGB 7.9 6.8 TP3 ZYNQ\_PL\_DONE 41.8 4.3 TP16 +0V675\_REF 10.71 5.98 TP15 +1V35 4.9 TP8 30.7 QSPI\_D1/BM1 10.65 TP5 ZYNQ\_PS\_SRST 15.9 36.4 34.55 TP9 ZYNQ\_BMODE\_2 8.8 TP14 +100 5.22 15.7 TP6 QSPI\_CS 8.2 30.2 TP7 QSPI\_D0/BM3 14.35 30.6 TP2 ZYNQ\_PL\_INITB 42.4 1 TP12 44.23 35.38 CLK\_25MHz TP13 1V0\_ETH 43.93 32.77 TP10 ZYNQ\_BMODE\_0 16.5 33.6 TP4 PS\_CLK\_33MHz 27.5 28.05 TP11 16.95 30.3 QSPI\_CLK



30	
Žn SoM	,

Title: Board Layout Board: Zynq System on Module		Size: <b>A4</b>
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