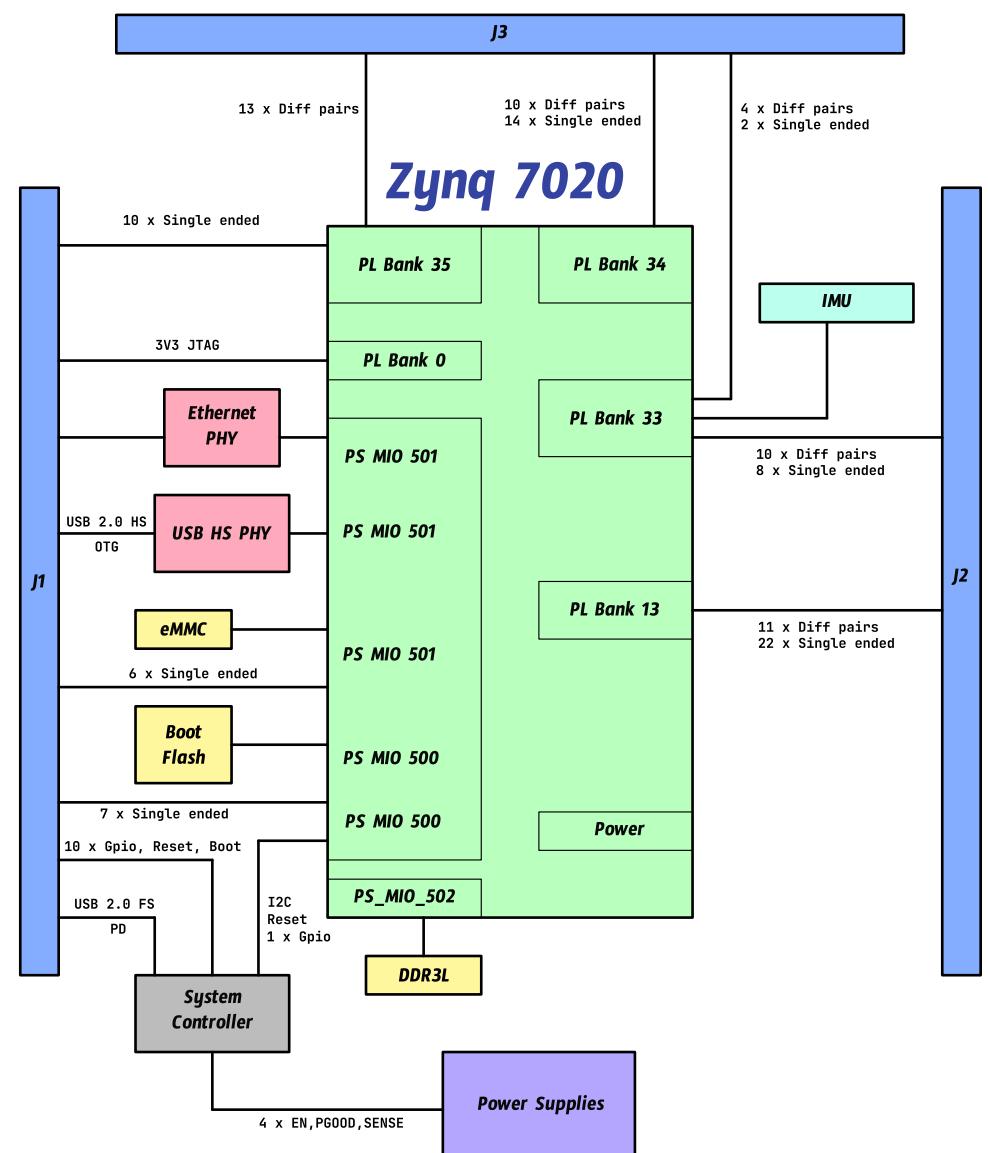


Zynq System on Module

Variant: No Variant
Revision: 1.0

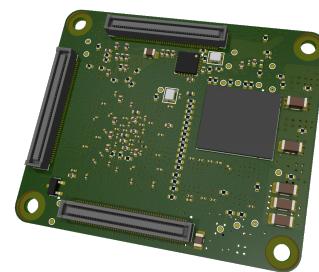
2024-10-14



TOP VIEW



BOTTOM VIEW



NOTES

- PL - Programmable Logic (FPGA fabric)
- PS - Processing System (Dual Core ARM A9)
- MIO - Multiplexed I/O
- Bank - Group of I/O pins that share common resources (e.g. power supply)
- PD - USB Power Delivery

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for layout notes.

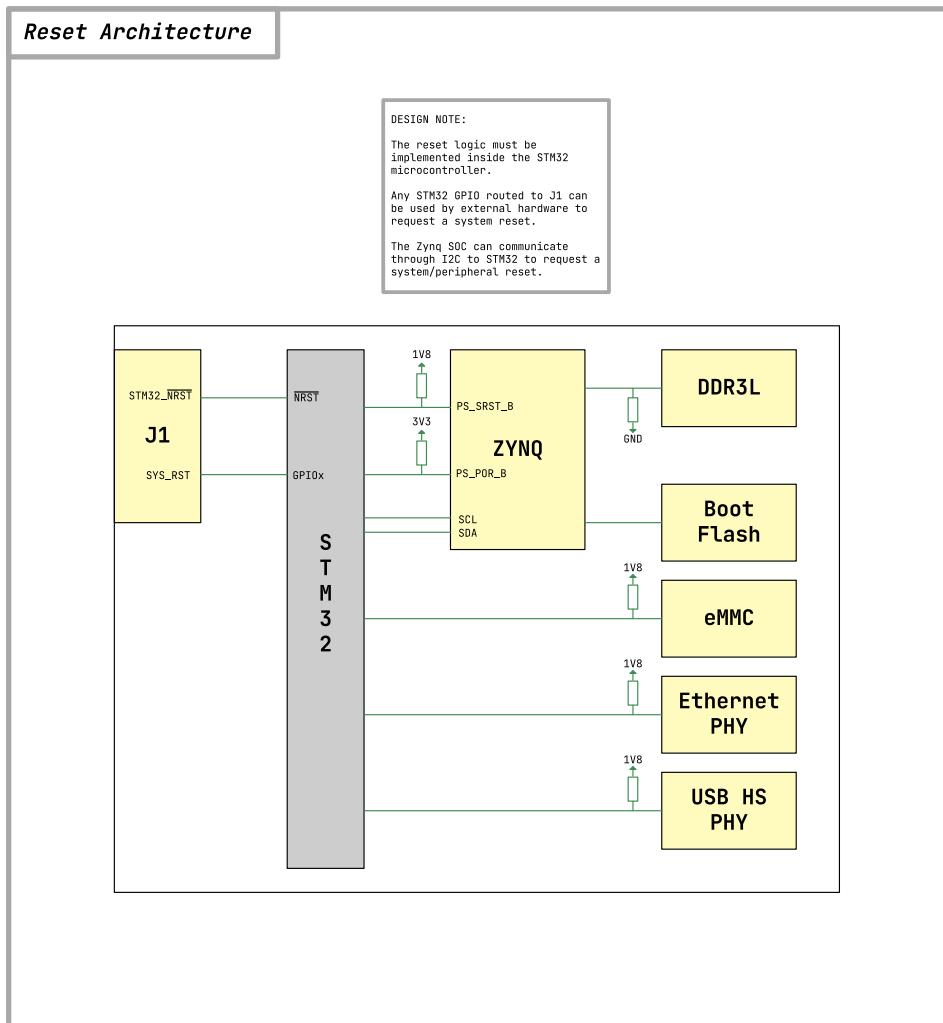
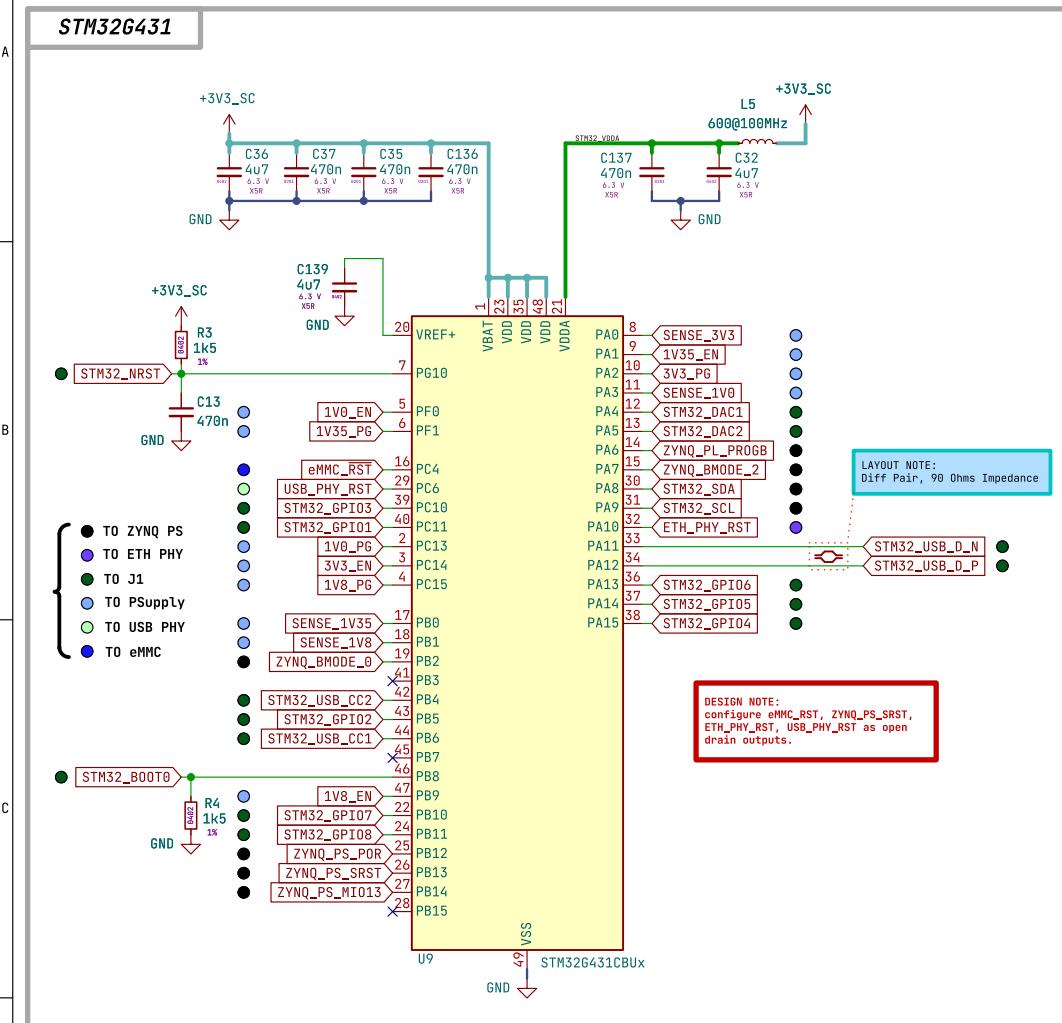
SCHEMATIC STATUS NOTES

DRAFT, PRELIMINARY, CHECKED, RELEASED

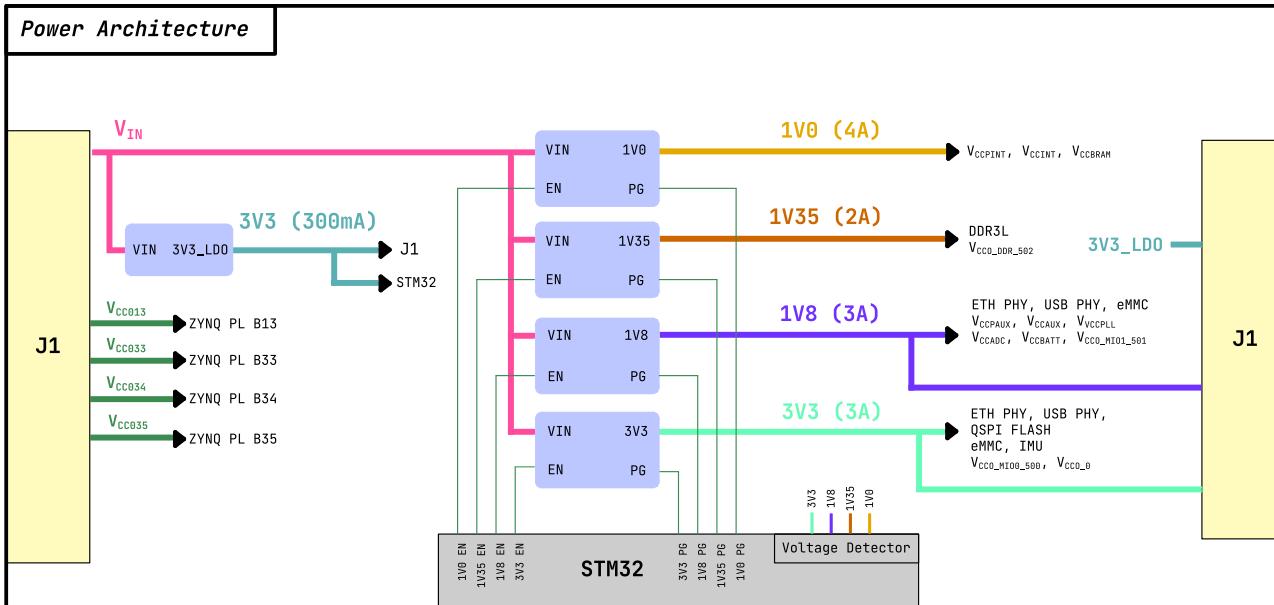
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Board: Zynq System on Module		
Company: Drawn by: G. Incerti	RELEASED	
Sheet: / File: Zynq_SoM.kicad_sch	Rev: 1.0 Var: No Variant	
Date: 2024-09-22	Page 1 of 16	

30
ZnSoM

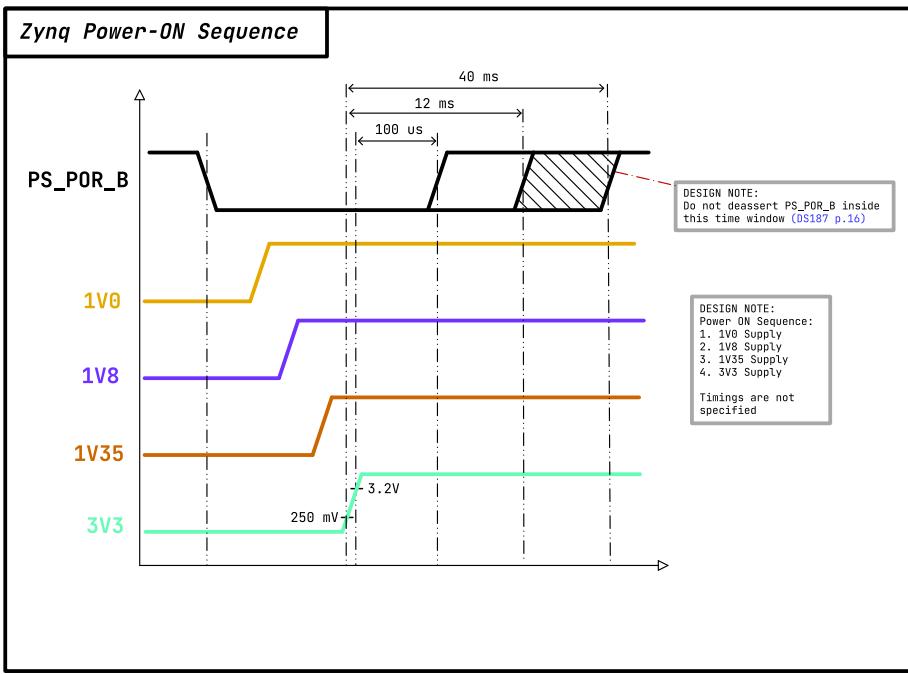
System Controller (STM32)



Title: System Controller		Size: A4
Board: Zynq System on Module		
Company: Drawn by: G. Incerti		RELEASED
Sheet: /System Controller/ File: system_controller.kicad_sch		Rev: 1.0 Var: No Variant
Date: 2024-09-22		Page 2 of 16



		Voltage	I _{MAX}	Note
I_N	V _{IN}	4.2-5V	3.7A	Mandatory
	V _{CCI013}	1.2-3.3V	1.2A	
	V _{CCI033}	1.2-3.3V	1.2A	
	V _{CCI034}	1.2-3.3V	0.9A	used for PUDC
	V _{CCI035}	1.2-3.3V	1.2A	used for ETH_PHY_INT
O_UT	1V8	1V8	0.9A	
	3V3	3V3	1.2A	
	3V3_LDO	3V3	100mA	



Block
Diagram

30
ZnSOM

Title: Power Architecture

Board: Zynq System on Module

Size:
A4

Company:
Drawn by: G. Incerti

RELEASED

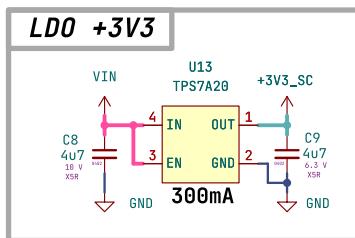
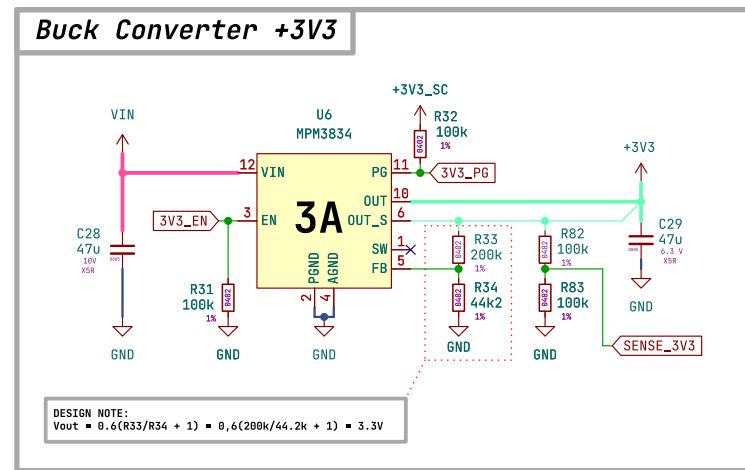
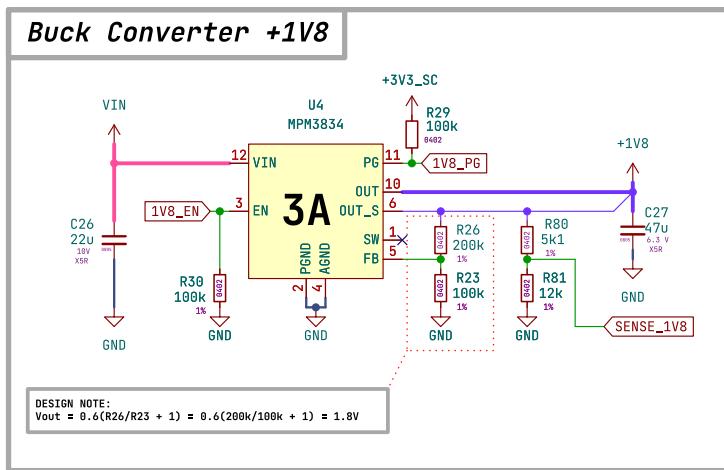
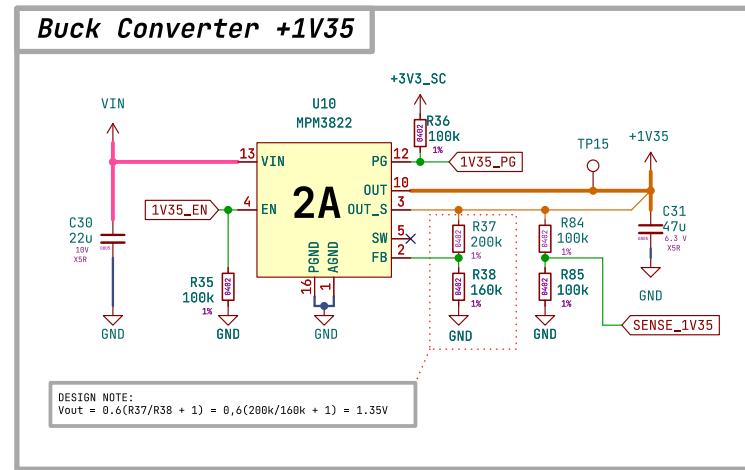
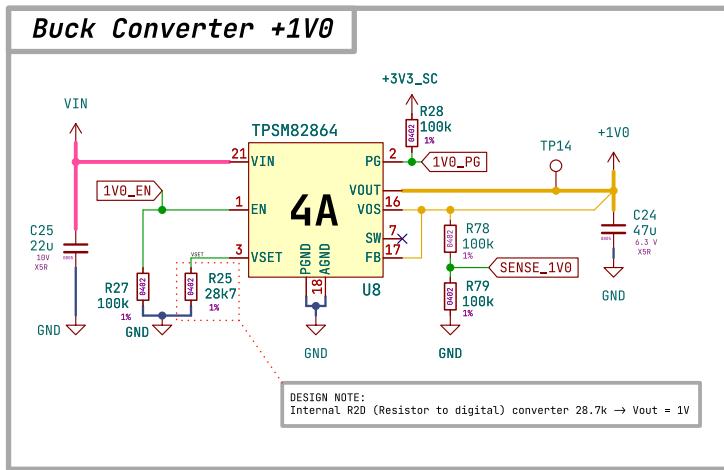
Sheet: /Power architecture/
File: power_architecture.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

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Power Supplies



Block
Diagram
30
ZnSOM

Title: Power Supplies

Board: Zynq System on Module

Size:
A4

Company:
Drawn by: G. Incerti

RELEASED

Sheet: /Power/
File: Power.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

Page 4 of 16

Zynq Power

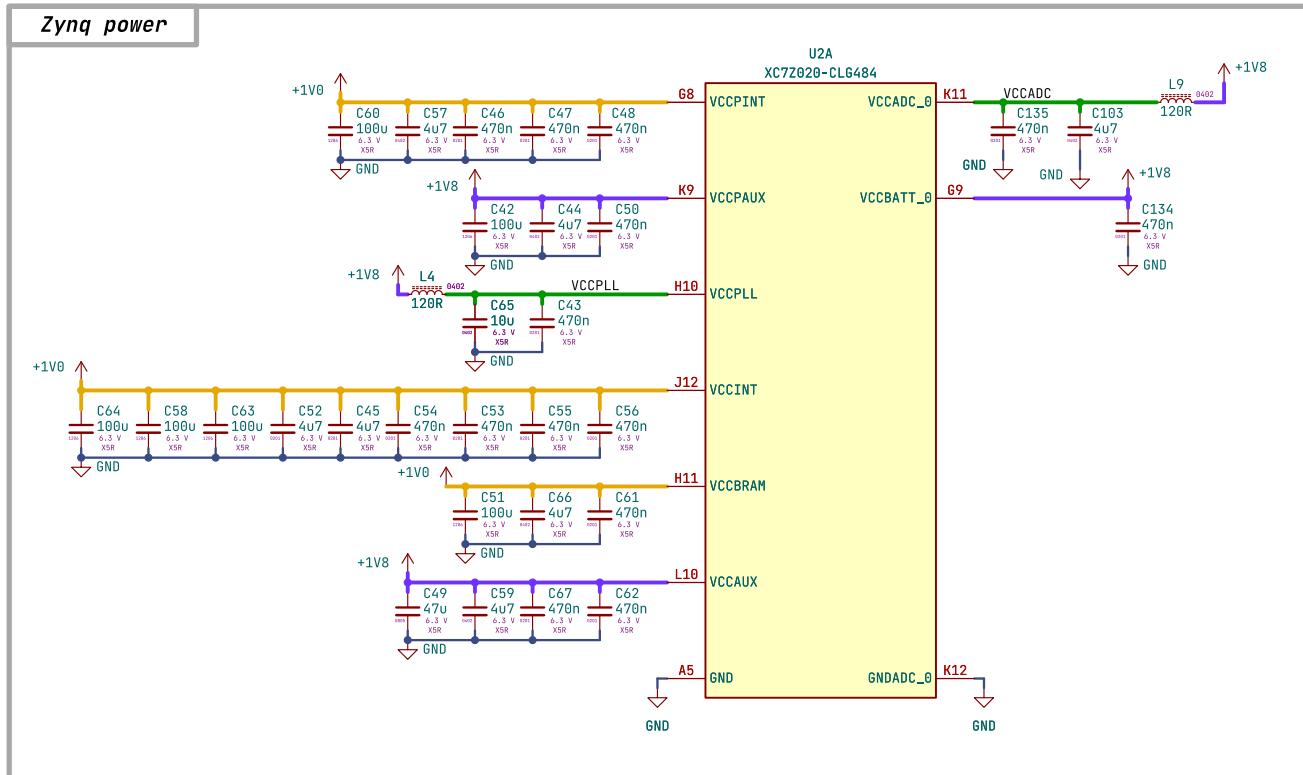


Table 3-2: Required PCB Capacitor Quantities per Device (PS) (Cont'd)

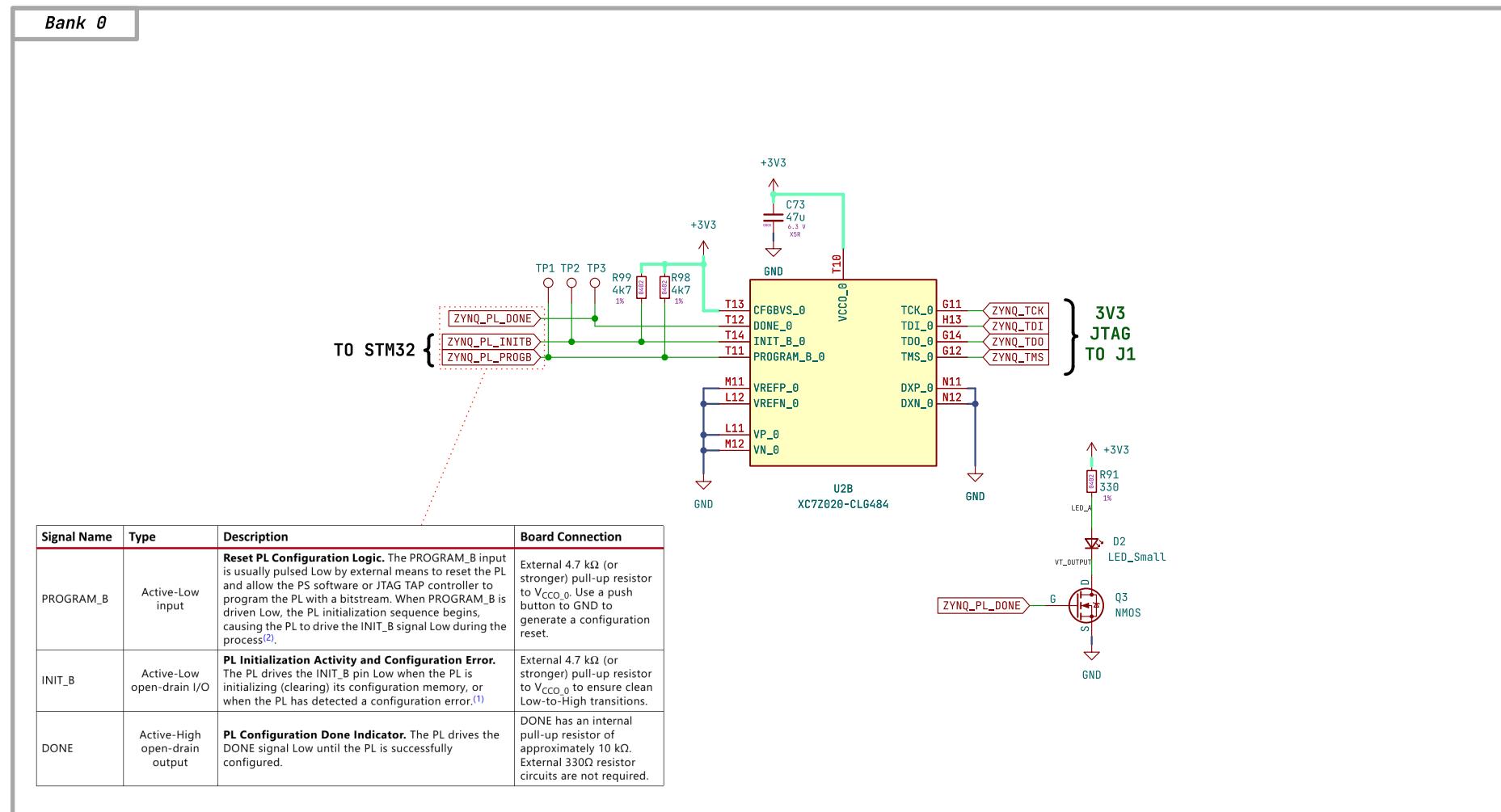
Package	Device	V _{CCPINT}		V _{CCPAUX} ⁽¹⁾		V _{CCO_DDR}		V _{CCO_MIO0}		V _{CCO_MIO1}		V _{CCPLL} ⁽²⁾⁽³⁾	
		100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F
CLG484	Z-7020	1	1	3	1	1	1	1	1	4	1	1	1

Table 3-1: Required PCB Capacitor Quantities per Device (PL)

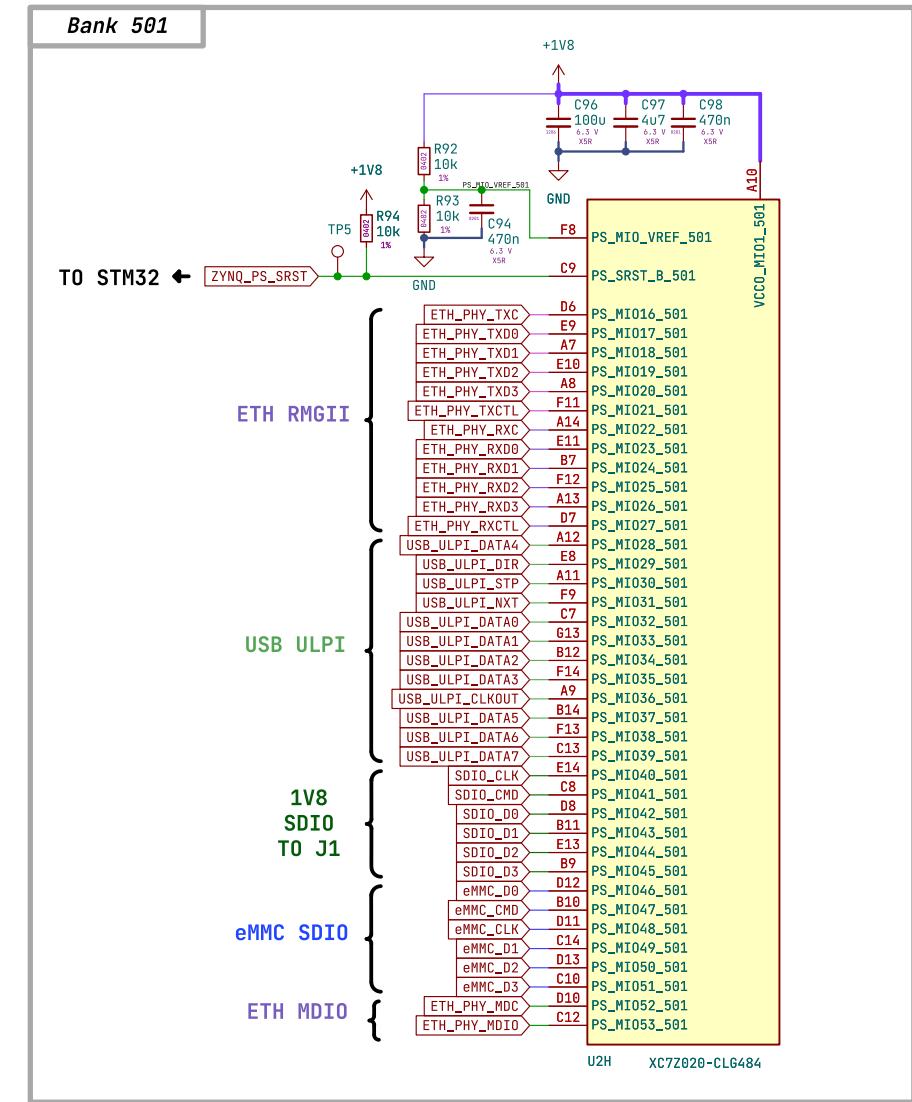
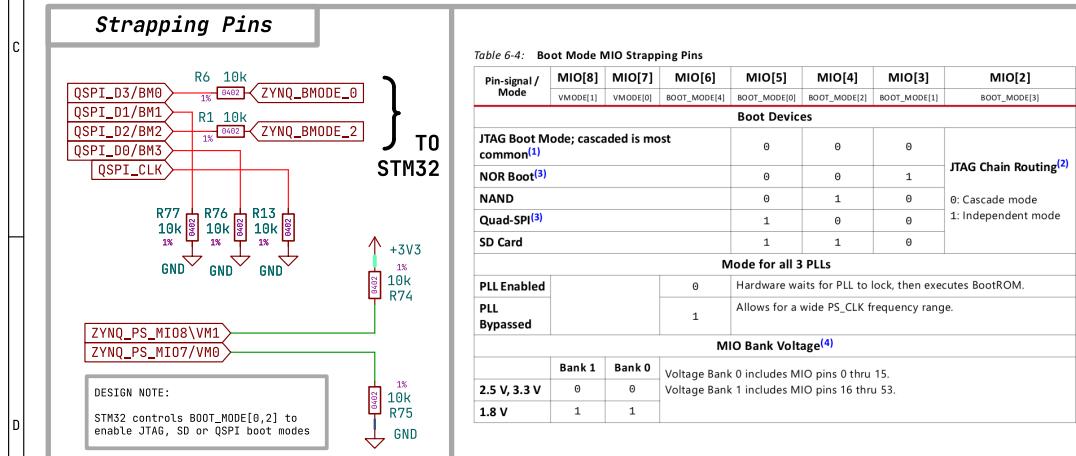
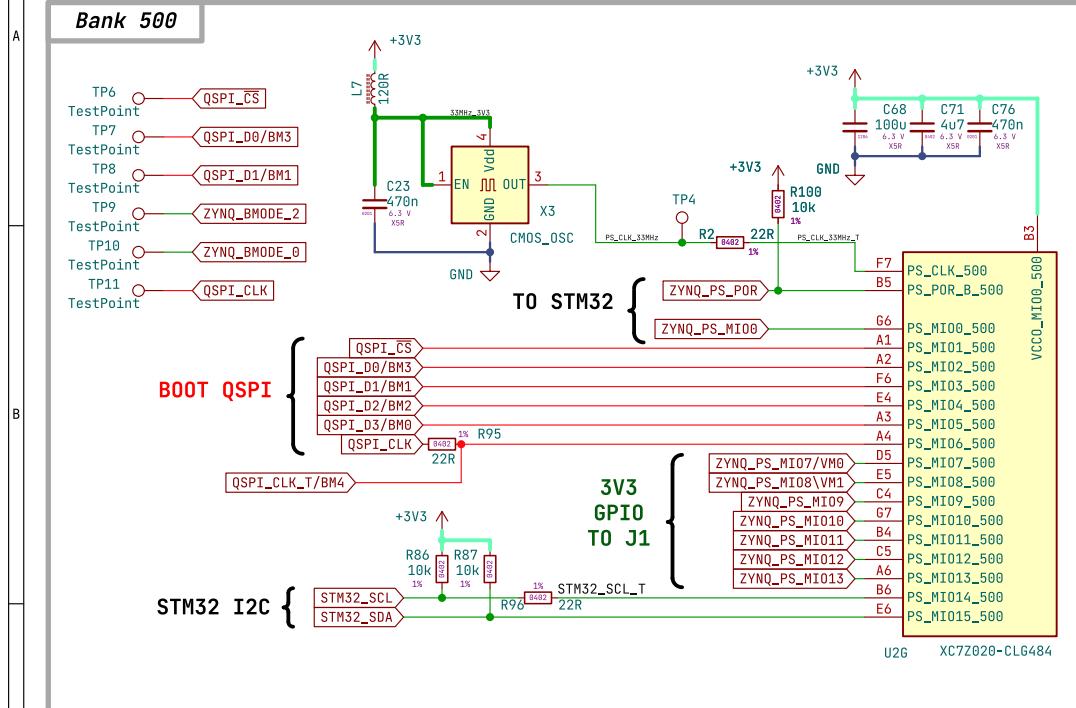
Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}		V _{CCAUX_J0}		V _{CCO} per Bank ⁽³⁾⁽⁴⁾	Bank 0		
		680 μ F	330 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F or 100 μ F	4.7 μ F	0.47 μ F	47 μ F
CLG484	Z-7020	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1

Block Diagram	30 Zn SOM	Title: Zynq Power	
		Board: Zynq System on Module	Size: A4
		Company: Drawn by: G. Incerti	RELEASED
		Sheet: /Zynq Power/ File: zynq_power.kicad_sch	Rev: 1.0 Var: No Variant
Date: 2024-09-22		Page 5 of 16	

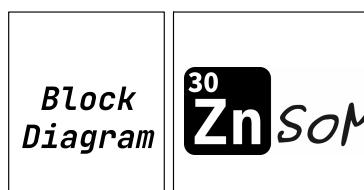
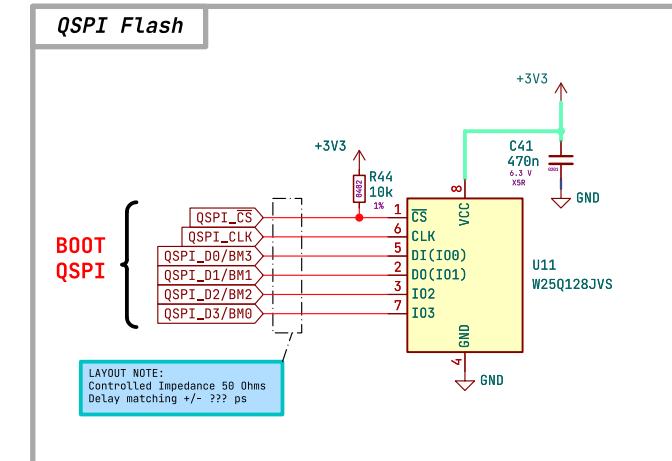
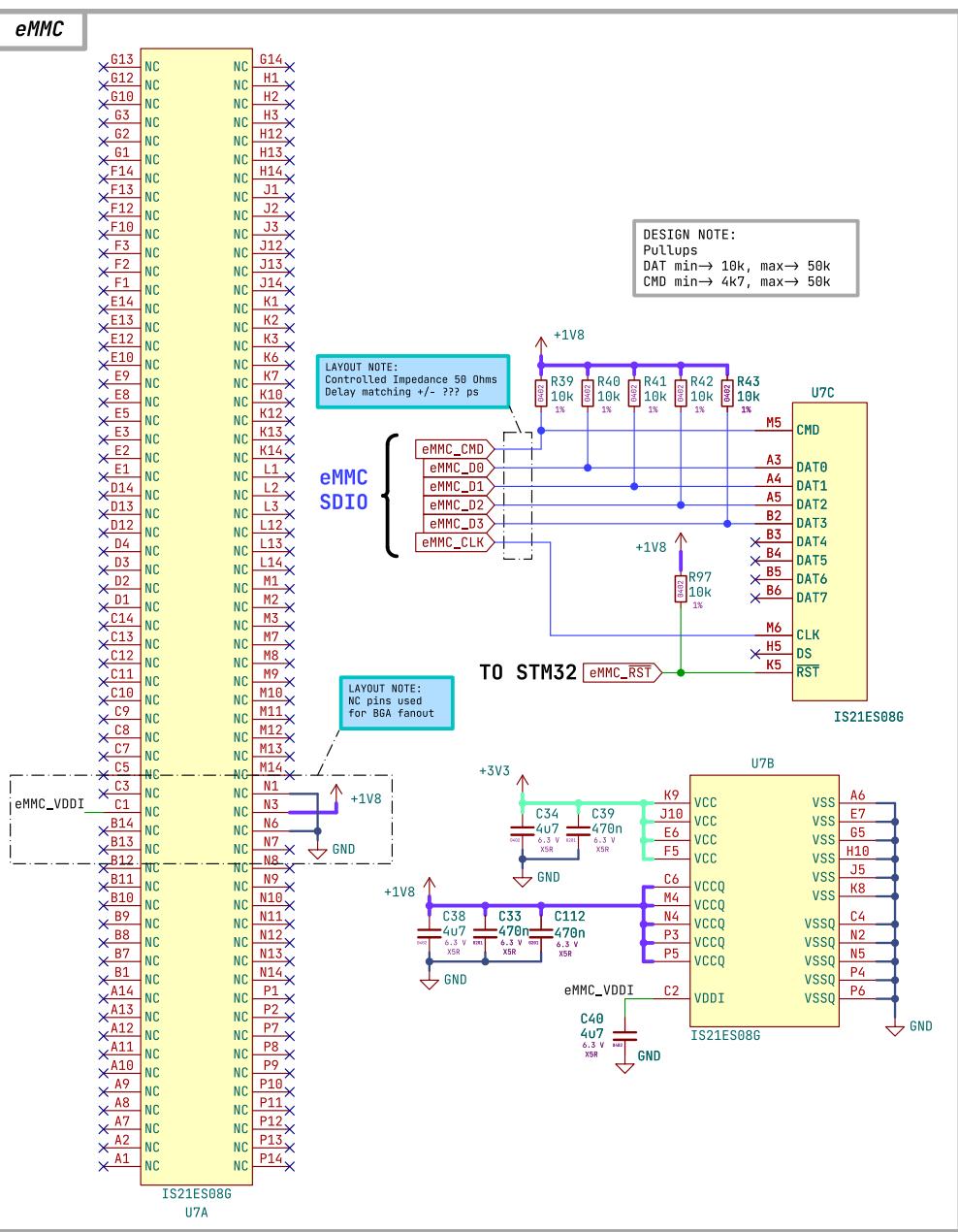
Zynq Bank 0



Zynq PS Banks



Flash Memories



Title: Flash Memories

Size: A4

Board: Zynq System on Module

RELEASED

Company:
Drawn by: G. Incerti

Rev: 1.0

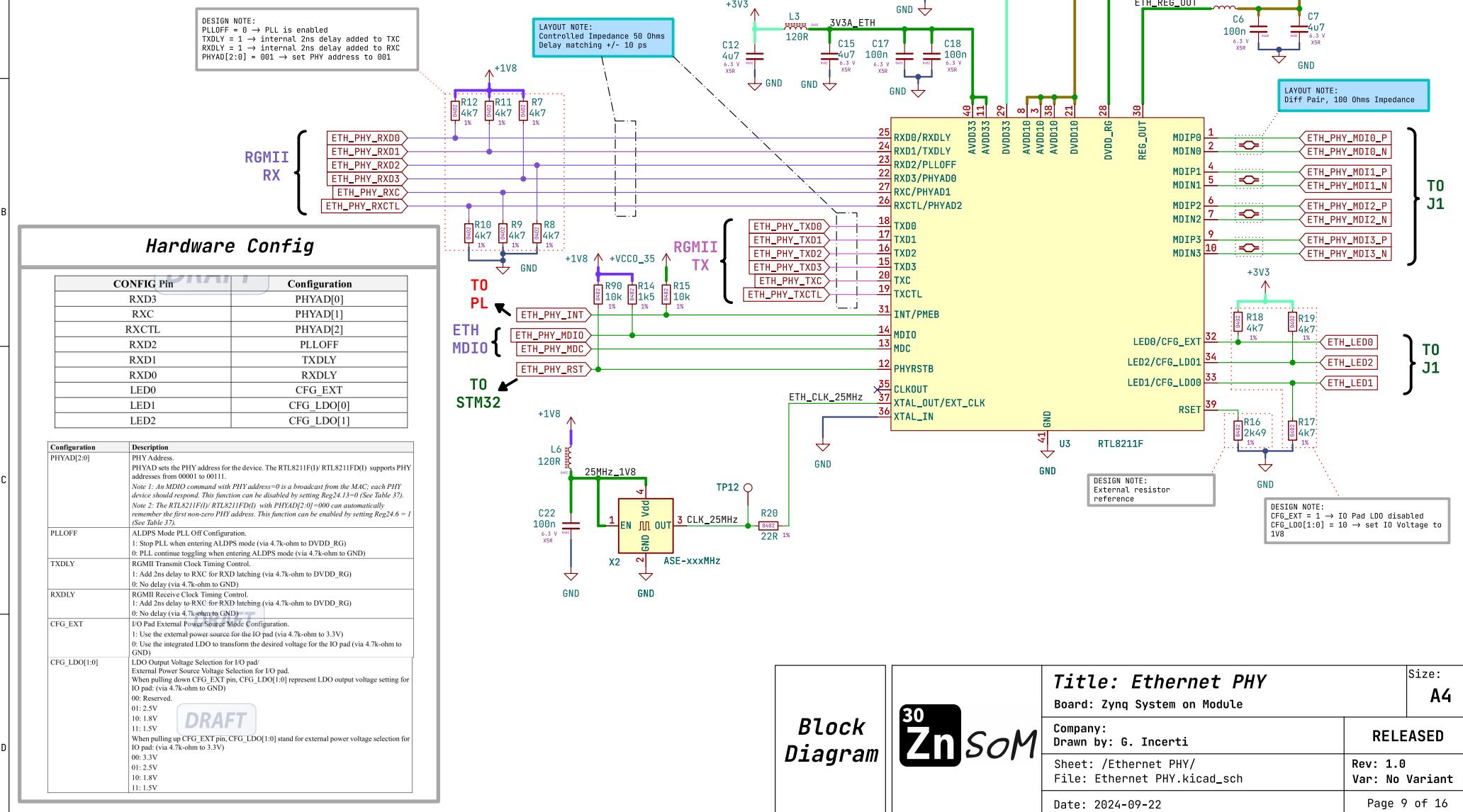
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File: emmc.kicad_sch

Var: No Variant

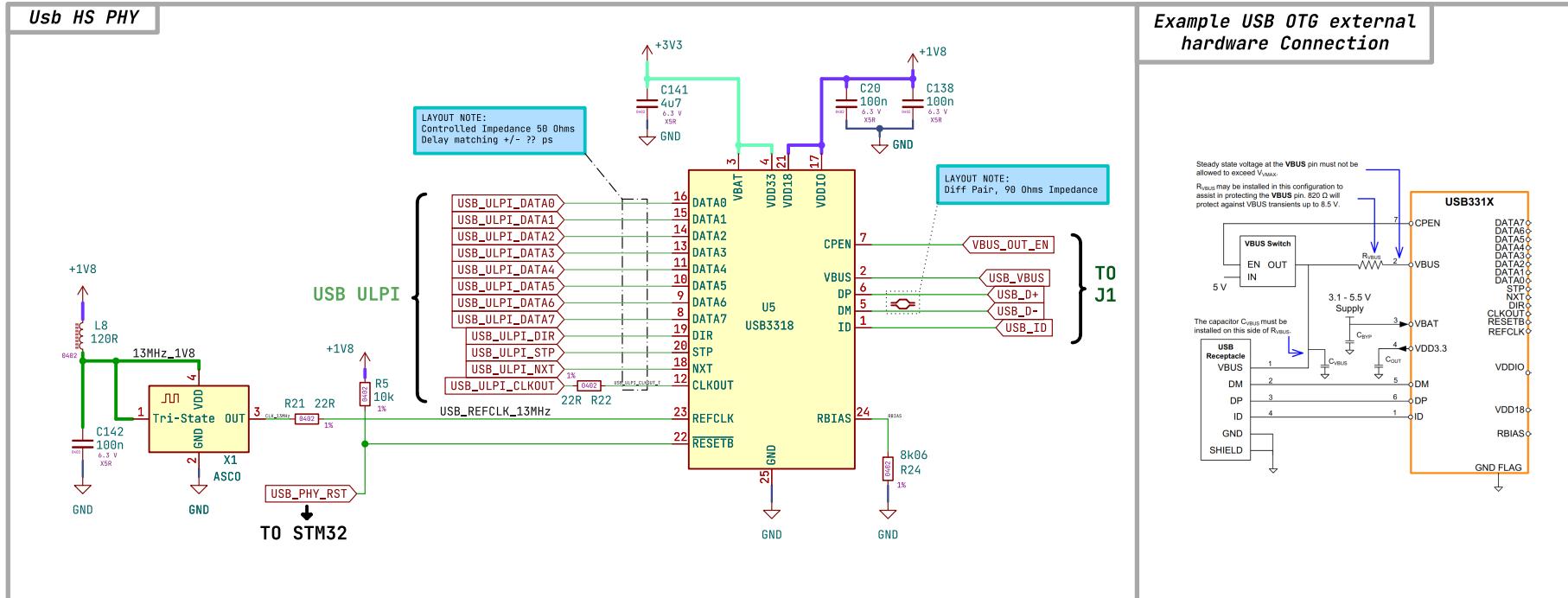
Date: 2024-09-22

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Gigabit Ethernet



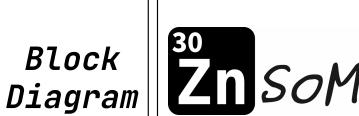
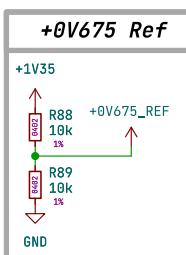
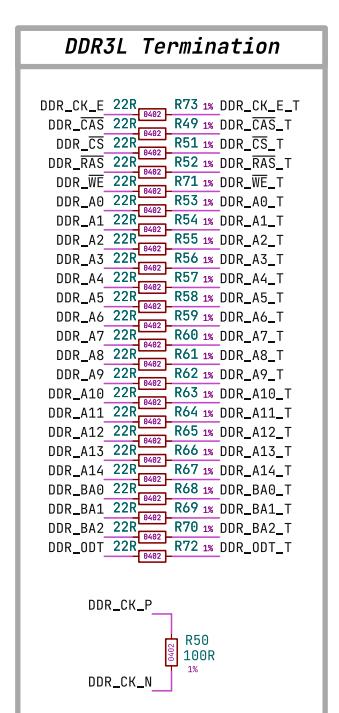
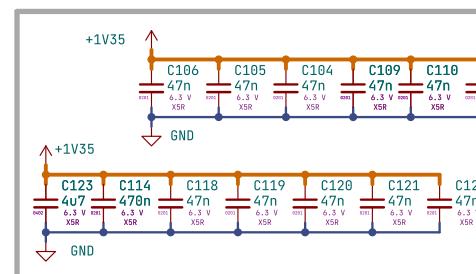
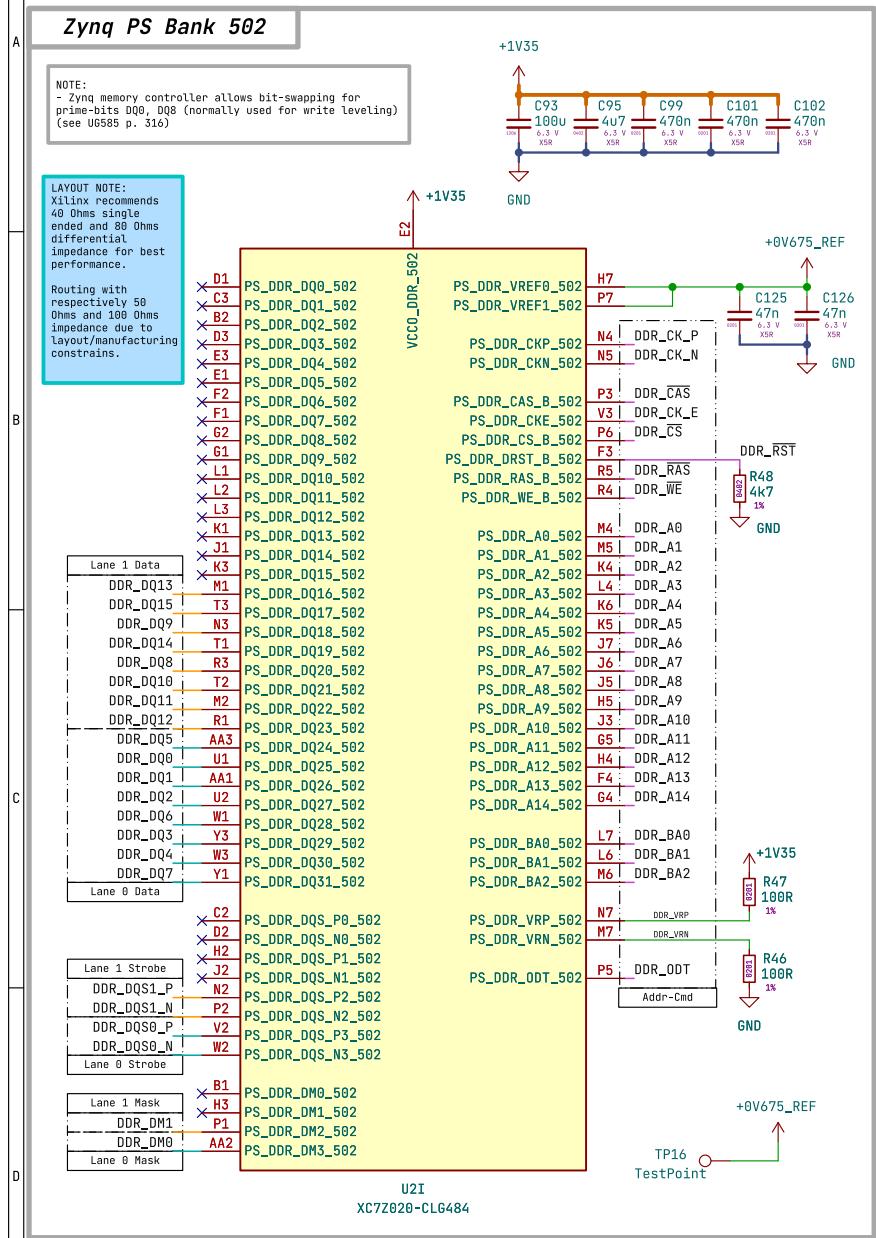
USB HS PHY



Block Diagram | ³⁰**Zn** *SOM*

<i>Block Diagram</i>	 ZnSOM 30	Title: <i>USB HS PHY</i>	Size: A4
		Board: Zynq System on Module	
		Company: Drawn by: G. Incerti	RELEASED
		Sheet: /USB HS PHY/ File: usb_hs_phy.kicad_sch	Rev: 1.0 Var: No Variant
		Date: 2024-09-22	Page 10 of 16

DDR Memory



Title: Zvng B502 & DDR3L

Board: Zynq System-on-Module

Company:

Drawn by: G. Incerti

Sheet: /2ylnq_B502
File: DDR3L.kicad

Size

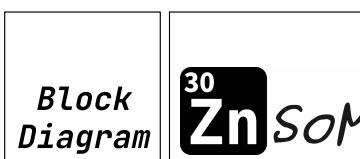
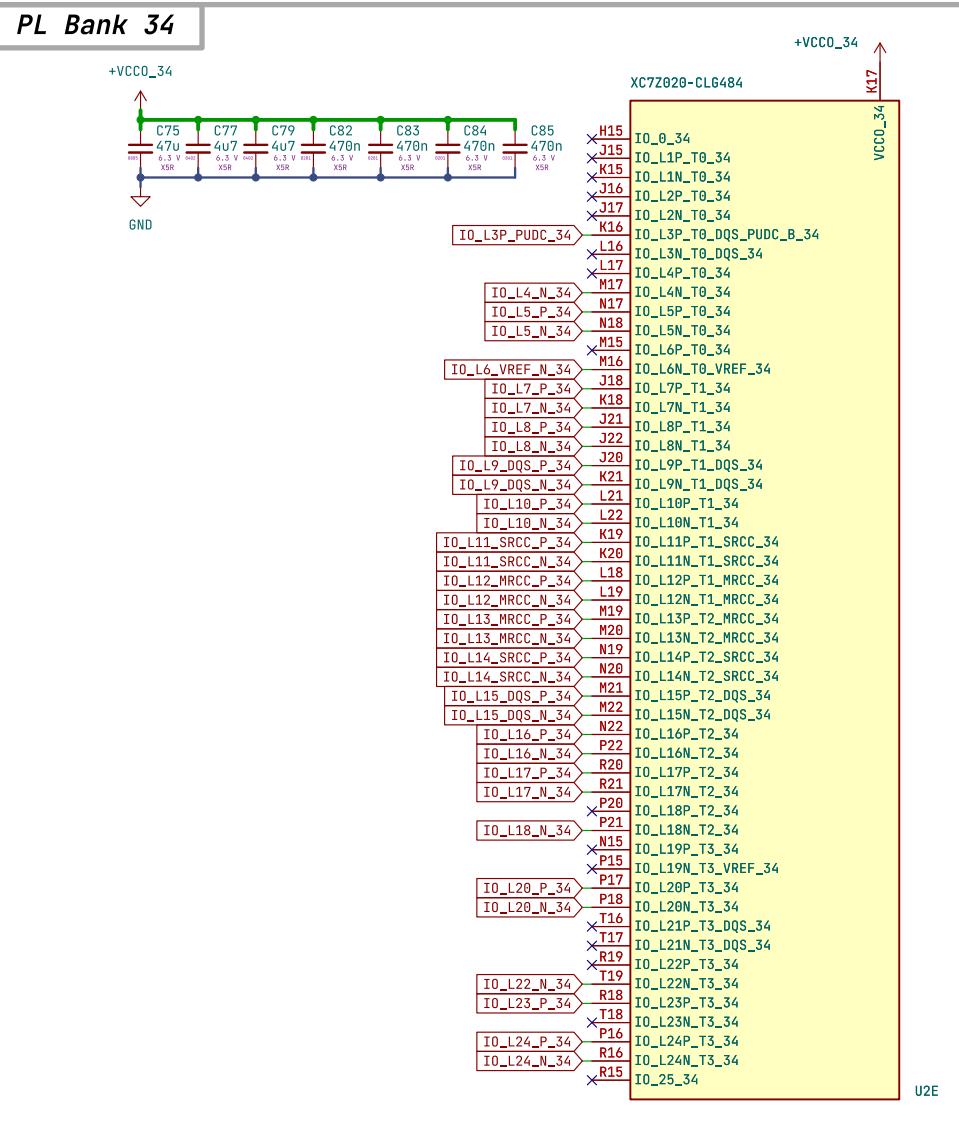
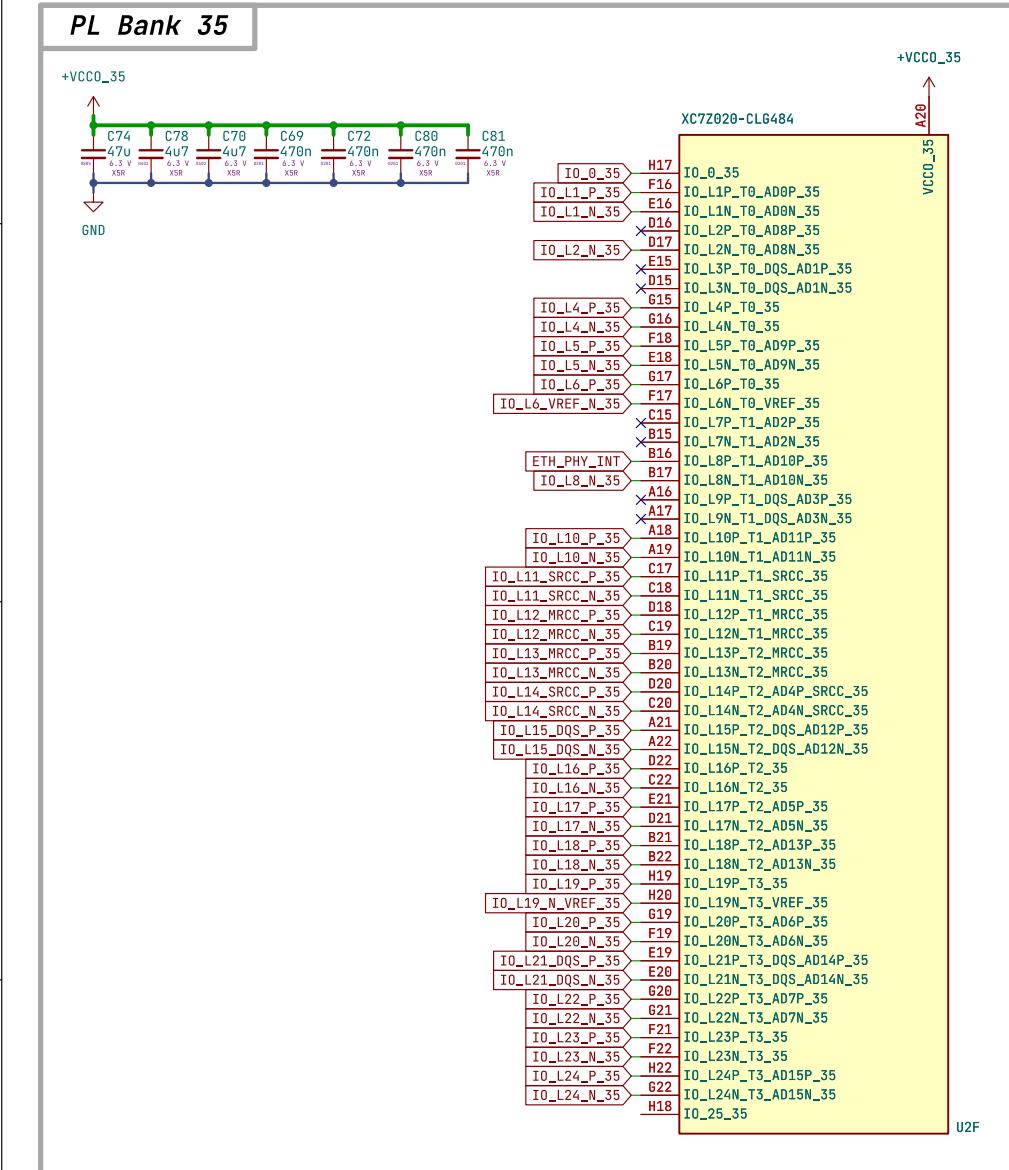
A4

RELEASED

[View Details](#)

c: No Variant

Zynq PL Banks 34 & 35



Title: Zynq PL B34 & B35

Size: A4

Board: Zynq System on Module

RELEASED

Company:
Drawn by: G. Incerti

Rev: 1.0

Sheet: /Zynq B33 B34 B35/
File: zynq_b33_b34_b35.kicad_sch

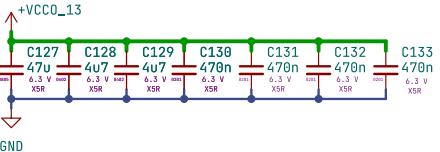
Var: No Variant

Date: 2024-09-22

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Zynq PL Banks 13 & 33

PL Bank 13



+VCCO_13
AA10
VCCO_13

IO_L1P_13
IO_L1N_T0_13
V9
IO_L2P_T0_13
W8
IO_L2_N_13
W11
IO_L3P_T0_DQS_13
W10
IO_L3N_T0_DQS_13
V12
IO_L4P_T0_13
W12
IO_L4N_T0_13
U12
IO_L5P_T0_13
U11
IO_L5N_T0_13
U10
IO_L6P_T0_13
U9
IO_L6N_T0_VREF_13
AA12
IO_L7P_T1_13
AB12
IO_L7N_T1_13
AA11
IO_L8P_T1_13
AB11
IO_L8N_T1_13
AB10
IO_L9P_T1_DQS_13
AB9
IO_L9N_T1_DQS_13
Y11
IO_L10P_T1_13
Y10
IO_L10N_T1_13
AA9
IO_L11P_T1_SRCC_13
AA8
IO_L11N_T1_SRCC_13
V9
IO_L12P_T1_MRCC_13
Y8
IO_L12N_T1_MRCC_13
Y6
IO_L13P_T2_MRCC_13
Y5
IO_L13N_T2_MRCC_13
AA7
IO_L14P_T2_SRCC_13
AA6
IO_L14N_T2_SRCC_13
AB2
IO_L15P_T2_DQS_13
AB1
IO_L15N_T2_DQS_13
AB5
IO_L16P_T2_13
AB4
IO_L16N_T2_13
AB7
IO_L17P_T2_13
AB6
IO_L17N_T2_13
Y4
IO_L18P_T2_13
AA4
IO_L18N_T2_13
R6
IO_L19P_T3_13
T6
IO_L19N_T3_VREF_13
T4
IO_L20P_T3_13
U4
IO_L20N_T3_13
V5
IO_L21P_T3_DQS_13
V4
IO_L21N_T3_DQS_13
U6
IO_L22P_T3_13
U5
IO_L22N_T3_13
V7
IO_L23P_T3_13
W7
IO_L23N_T3_13
W6
IO_L24P_T3_13
W5
IO_L24N_T3_13
U7
IO_25_13

XC7Z020-CLG484

PL Bank 33

+VCCO_33

stitching, close to IO_L19_VREF_N_33 and IO_L1P_13

GND

+VCCO_33

AA29
VCCO_33

U19	IO_0_33
T21	IO_L1P_T0_33
IO_L1N_T0_33	
T22	IO_L2P_T0_33
IO_L2N_T0_33	
U22	IO_L3P_T0_33
IO_L3_DQS_P_33	W22
IO_L3_DQS_N_33	W20
U20	IO_L4P_T0_33
IO_L4_N_33	
W21	IO_L5P_T0_33
IO_L5_N_33	
V20	IO_L6P_T0_33
IO_L6_P_33	
V18	IO_L6N_T0_VREF_33
AA22	IO_L7P_T1_33
IO_L7N_T1_33	
AA21	IO_L8P_T1_33
IO_L8_P_33	
Y20	IO_L9P_T1_DQS_33
IO_L9_DQS_P_33	Y21
IO_L9_DQS_N_33	Y20
AB19	IO_L10P_T1_33
IO_L10_N_33	
AB20	IO_L10N_T1_33
Y19	IO_L11P_T1_SRCC_33
IO_L11_SRCC_P_33	AA19
IO_L11_SRCC_N_33	IO_L11N_T1_SRCC_33
IO_L12_MRCC_P_33	Y18
IO_L12_MRCC_N_33	AA18
W17	IO_L13P_T2_MRCC_33
IO_L13P_T2_13	W18
IO_L13N_T2_MRCC_13	IO_L13N_T2_MRCC_33
W16	IO_L14P_T2_SRCC_33
IO_L14_SRCC_P_33	Y16
IO_L14_SRCC_N_33	IO_L14N_T2_SRCC_33
U15	IO_L15P_T2_DQS_33
IO_L15_VREF_N_33	U16
IO_L15_N_33	IO_L15N_T2_DQS_33
V17	IO_L16P_T2_33
IO_L16N_T2_33	
AA17	IO_L17P_T2_33
IO_L17N_T2_33	
AB17	IO_L18P_T2_33
IO_L18_N_33	
AA16	IO_L18N_T2_33
IO_L19P_T3_13	
V14	IO_L19N_T3_33
IO_L15_P_33	
V15	IO_L19N_T3_VREF_33
IO_L20P_T3_13	
W13	IO_L20N_T3_33
IO_L21_DQS_P_33	
W15	IO_L21P_T3_DQS_33
IO_L21_DQS_N_33	
Y15	IO_L21N_T3_DQS_33
Y14	IO_L22P_T3_33
IO_L22_N_33	
AA14	IO_L22N_T3_33
IO_L23_P_33	
Y13	IO_L23P_T3_33
IO_L23_N_33	
AA13	IO_L23N_T3_33
AB14	IO_L24P_T3_33
IO_L24_P_33	
AB15	IO_L24N_T3_33
U14	IO_25_33

XC7Z020-CLG484

Title: Zynq PL B13 & B33

Size: A4

Board: Zynq System on Module

RELEASED

Company:

Drawn by: G. Incerti

Sheet: /Zynq PL (B13)/

File: zynq_PL_b13.kicad_sch

Rev: 1.0

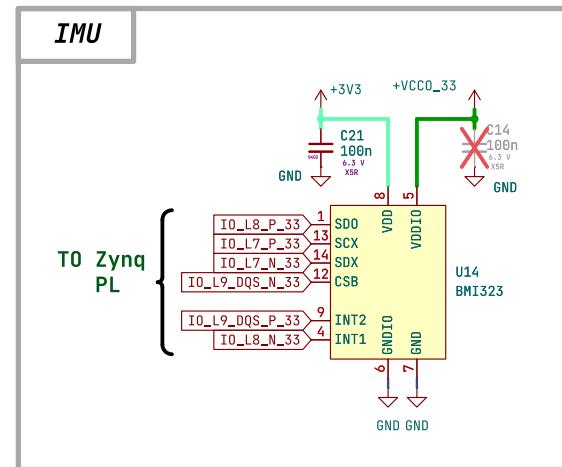
Var: No Variant

Date: 2024-09-22

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30
ZnSOM

Inertial Measurement Unit



Block
Diagram

30
ZnSOM

Title: IMU

Board: Zynq System on Module

Size:
A4

Company:

Drawn by: G. Incerti

RELEASED

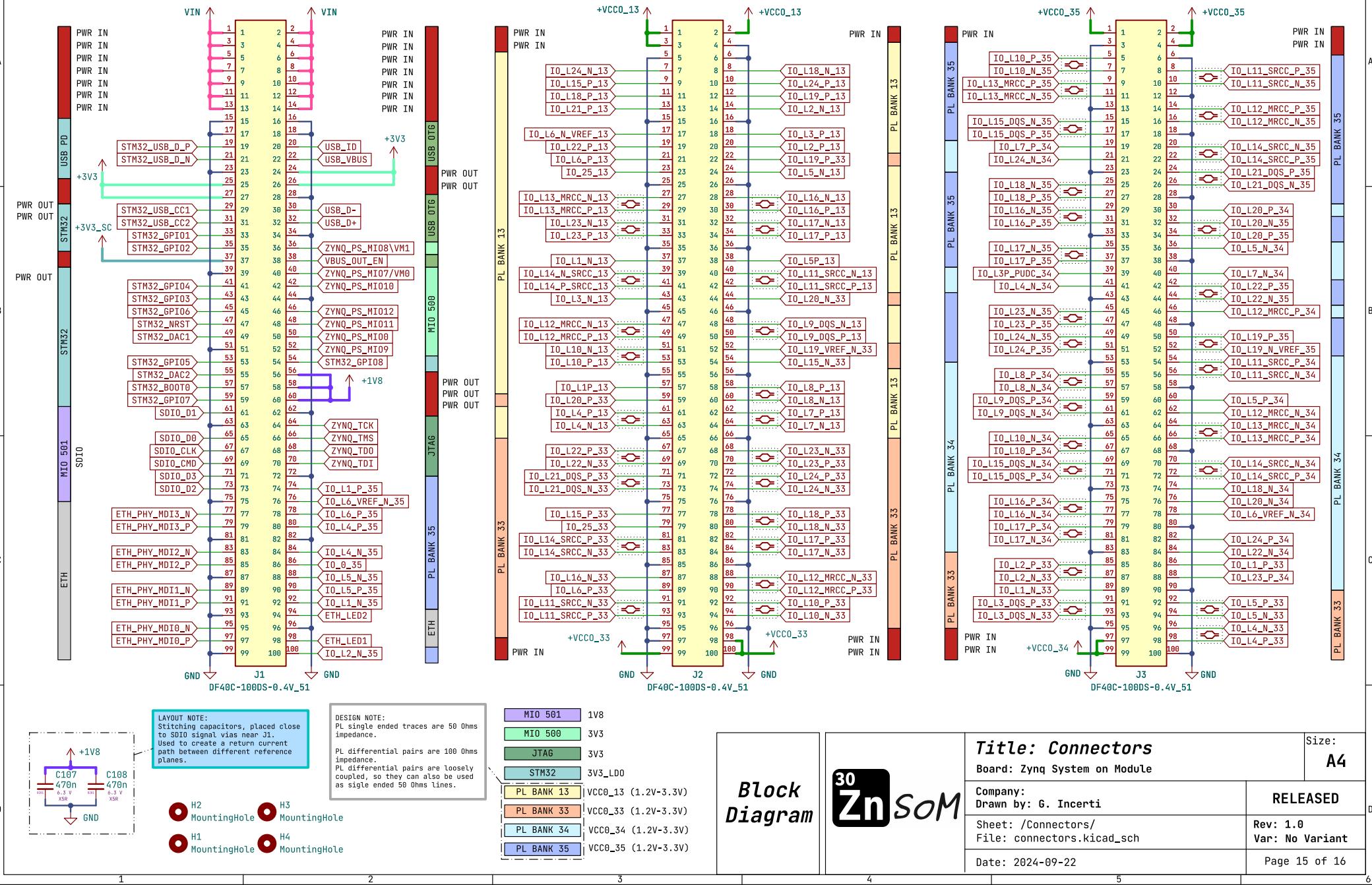
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File: Sensors.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

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Connectors



A

A

<i>REV</i>	<i>Description</i>	
1.0	Initial revision	

B

B

C

C

D

D

30 ZnSoM	Title: Revision History	Size:
Board: Zynq System on Module		A4
Company: Drawn by: G. Incerti	RELEASED	
Sheet: /Revisions changes/ File: revision_changes.kicad_sch	Rev: 1.0	Var: No Variant
Date: 2024-09-22	Page 16 of 16	