

BOARD CHARACTERISTICS

Copper Layer Count: 8

Board overall dimensions: 50,0000 mm x 42,0000 mm

Min track/spacing: 0,0900 mm / 0,0900 mm

Copper Finish: ENIG

Castellated pads: No

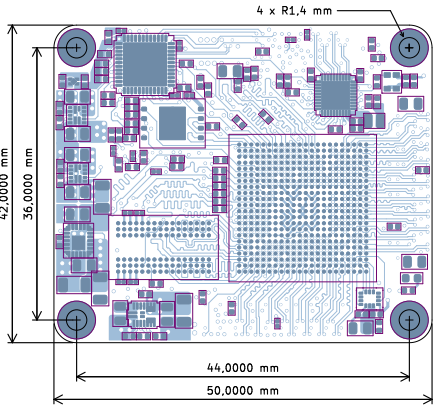
Edge card connectors: No

Board Thickness: 1,2396 mm

Min hole diameter: 0,2000 mm

Impedance Control: Yes

Plated Board Edge: No



Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Epsilon	Type	Gerber
	B.Paste					Paste Mask	GTP
	B.Silkscreen					Legend	GTO
	B.Mask					Solder Mask	GTS
	Copper	L1 (Sig)	0.035mm (1oz)			Signal	6TL
	Prepreg		0.0764 mm	1080 RC67%	3.91	Dielectric	
	Copper	L2 (GND)	0.0152mm (0.5oz)			Internal Plane	G2
	Core		0.2 mm	FR-4	4.36	Dielectric	
	Copper	L3 (PWR)	0.0152mm (0.5oz)			Plane	G3
	Prepreg		0.1528 mm	1080 RC67%	3.91	Dielectric	
	Copper	L4 (Sig+Pwr)	0.0152mm (0.5oz)			Signal	G4
	Core		0.2 mm	FR-4	4.36	Dielectric	
	Copper	L5 (GND)	0.152mm (0.5oz)			Internal Plane	G5
	Prepreg		0.1528 mm	1080 RC67%	3.91	Dielectric	
	Copper	L6 (Sig+Pwr)	0.0152mm (0.5oz)			Signal	G6
	Core		0.2 mm	FR-4	4.36	Dielectric	
	Copper	L7 (GND)	0.0152mm (0.5oz)			Internal Plane	G7
	Prepreg		0.0764 mm	1080 RC67%	3.91	Dielectric	
	Copper	L8 (Sig)	0.035mm (1oz)			Signal	G8L
	B.Mask					Solder Mask	G8S
	B.Silkscreen					Legend	G8O
	B.Paste					Paste Mask	G8P

Impedance specification

Copper	Layers	Impedance (Ohm)	Width (mm)	Spacing (mm)	Ref. Layers
Microstrip	L1 (L8)	50	0.120		L2 (L7)
Microstrip	L1 (L8)	90	0.1146	0.15	L2 (L7)
Microstrip	L1 (L8)	100	0.1	0.2	L2 (L7)
Microstrip	L1 (L8)	100	0.104	0.250	L2 (L7)
Stripline	L4 (L6)	52.7	0.135		L3,L5 (L5,L7)
Stripline	L4 (L6)	100	0.102	0.125	L3,L5 (L5,L7)

30

Zn

SOM

Title: Board Layout

Board: Zynq System on Module

Company: Asdrubale

Drawn by: G. Incerti

Sheet:

File: prova_fpga.kicad_pcb

Date: 2024-09-22

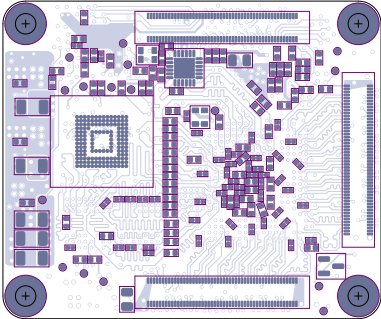
Size: A4

RELEASED

Rev: 1.0

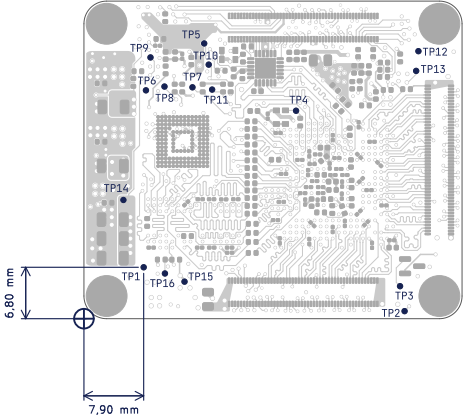
Var: No Variant

Page 1 of 1

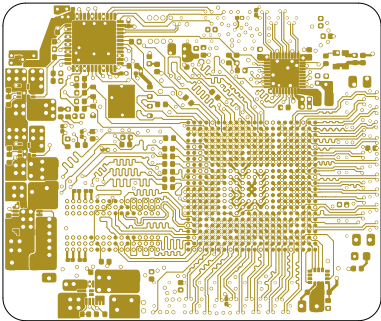


<div>30</div> <div>Zn</div> <div>SoM</div>	Title: Board Layout		Size:
	Board: Zynq System on Module		A4
	Company: Asdrubale Drawn by: G. Incerti		RELEASED
	Sheet: File: prova_fpga.kicad_pcb		Rev: 1.0 Var: No Variant
	Date: 2024-09-22		Page 1 of 1

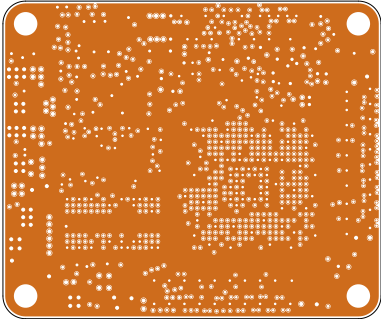
	SIGNAL	X (mm)	Y (mm)
TP1	ZYNQ_PL_PROGB	7.9	6.8
TP3	ZYNQ_PL_DONE	41.8	4.3
TP16	+0V675_REF	10.71	5.98
TP15	+1V35	13.3	4.9
TP8	QSPI_D0/BM1	10.65	30.7
TP5	ZYNQ_PS_SRSST	15.9	36.4
TP9	ZYNQ_BMODE_2	8.8	34.55
TP14	+1V0	5.22	15.7
TP6	QSPI_CS	8.2	30.2
TP7	QSPI_D0/BM3	14.35	30.6
TP2	ZYNQ_PL_INITB	42.4	1
TP12	CLK_25MHz	44.23	35.38
TP13	1V0_ETH	43.93	32.77
TP10	ZYNQ_BMODE_0	16.5	33.6
TP4	PS_CLK_33MHz	28.05	27.5
TP11	QSPI_CLK	16.95	30.3



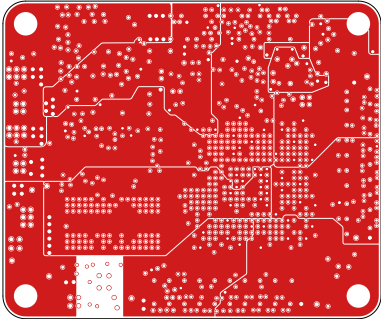
<div>30</div> <div>Zn</div> <div>SoM</div>	<div>Title: Board Layout</div> <div>Board: Zynq System on Module</div>		<div>Size:</div> <div>A4</div>
	<div>Company: Asdrubale</div> <div>Drawn by: G. Incerti</div>		RELEASED
	<div>Sheet:</div> <div>File: prova_fpga.kicad_pcb</div>		<div>Rev: 1.0</div> <div>Var: No Variant</div>
	<div>Date: 2024-09-22</div>		Page 1 of 1



<div>30</div> <div>Zn</div> <div>SoM</div>	Title: Board Layout		Size:
	Board: Zynq System on Module		A4
	Company: Asdrubale Drawn by: G. Incerti		RELEASED
	Sheet: File: prova_fpga.kicad_pcb		Rev: 1.0 Var: No Variant
	Date: 2024-09-22		Page 1 of 1



<div>30</div> <div>Zn</div> <div>SOM</div>	Title: Board Layout		Size:
	Board: Zynq System on Module		A4
	Company: Asdrubale Drawn by: G. Incerti		RELEASED
	Sheet: File: prova_fpga.kicad_pcb		Rev: 1.0 Var: No Variant
	Date: 2024-09-22		Page 1 of 1



Title: Board Layout

Board: Zynq System on Module

Company: Asdrubale
Drawn by: G. Incerti

Sheet:
File: prova_fpga.kicad_pcb

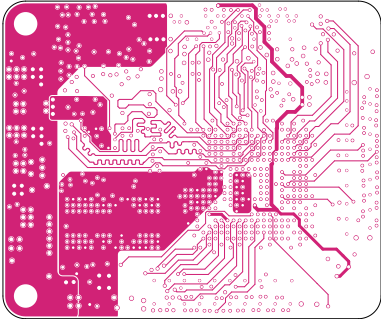
Date: 2024-09-22

RELEASED

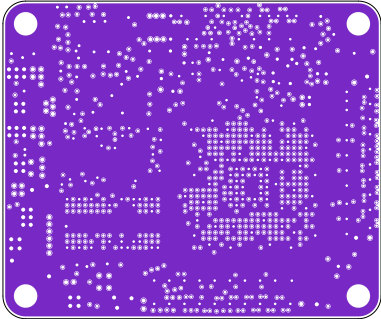
Rev: 1.0
Var: No Variant

Page 1 of 1

Size:
A4



<div>30</div> <div>Zn</div> <div>SoM</div>	Title: Board Layout		Size:
	Board: Zynq System on Module		A4
	Company: Asdrubale Drawn by: G. Incerti		RELEASED
	Sheet: File: prova_fpga.kicad_pcb		Rev: 1.0 Var: No Variant
	Date: 2024-09-22		Page 1 of 1



Title: Board Layout
Board: Zynq System on Module

Size:
A4

Company: Asdrubale
Drawn by: G. Incerti

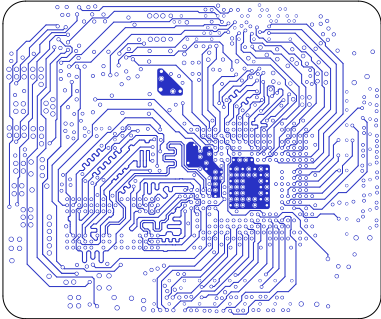
RELEASED

Sheet:
File: prova_fpga.kicad_pcb

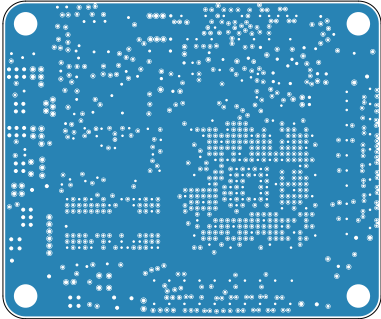
Rev: 1.0
Var: No Variant


Date: 2024-09-22

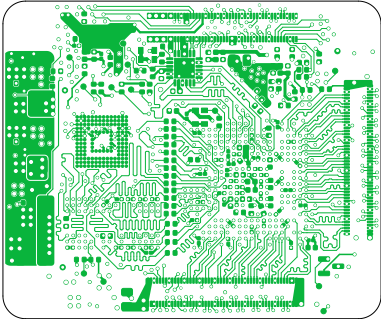
Page 1 of 1




<div>30</div> <div>Zn</div> <div>SoM</div>	Title: Board Layout		Size:
	Board: Zynq System on Module		A4
	Company: Asdrubale Drawn by: G. Incerti		RELEASED
	Sheet: File: prova_fpga.kicad_pcb		Rev: 1.0 Var: No Variant
	Date: 2024-09-22		Page 1 of 1



	Title: Board Layout		Size: A4
	Board: Zynq System on Module		
	Company: Asdrubale Drawn by: G. Incerti		RELEASED
	Sheet: File: prova_fpga.kicad_pcb		Rev: 1.0 Var: No Variant
	Date: 2024-09-22		Page 1 of 1



	Title: Board Layout		Size: A4
	Board: Zynq System on Module		
	Company: Asdrubale Drawn by: G. Incerti	RELEASED	
	Sheet: File: prova_fpga.kicad_pcb	Rev: 1.0 Var: No Variant	
	Date: 2024-09-22	Page 1 of 1	