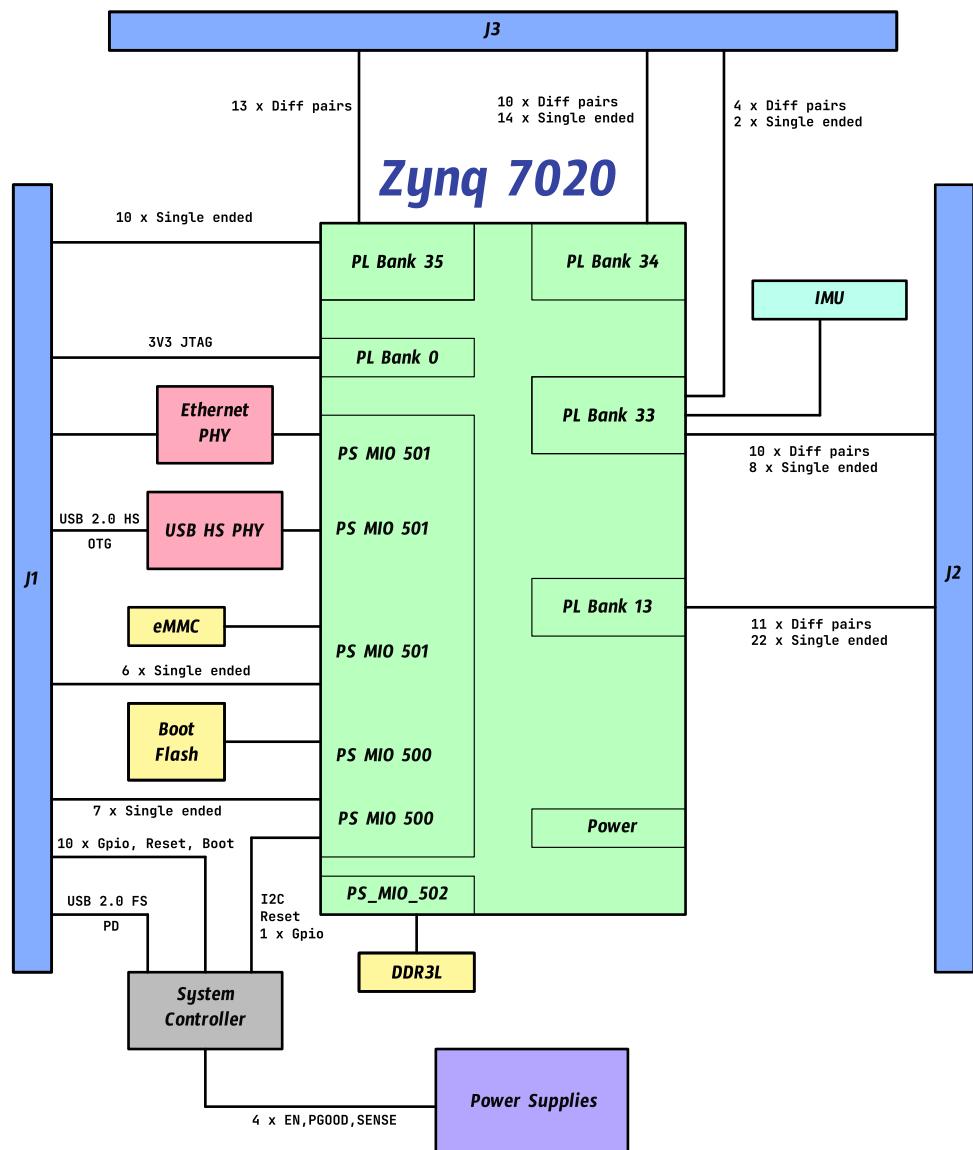


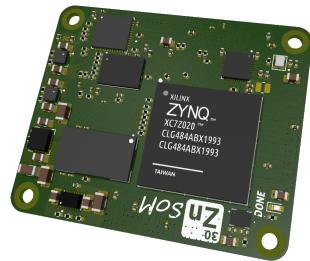
Zynq System on Module

Variant: No Variant
Revision: 1.0

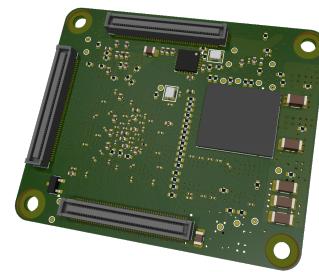
2025-03-29



TOP VIEW



BOTTOM VIEW



NOTES

- PL - Programmable Logic (FPGA fabric)
- PS - Processing System (Dual Core ARM A9)
- MIO - Multiplexed I/O
- Bank - Group of I/O pins that share common resources (e.g. power supply)
- PD - USB Power Delivery

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

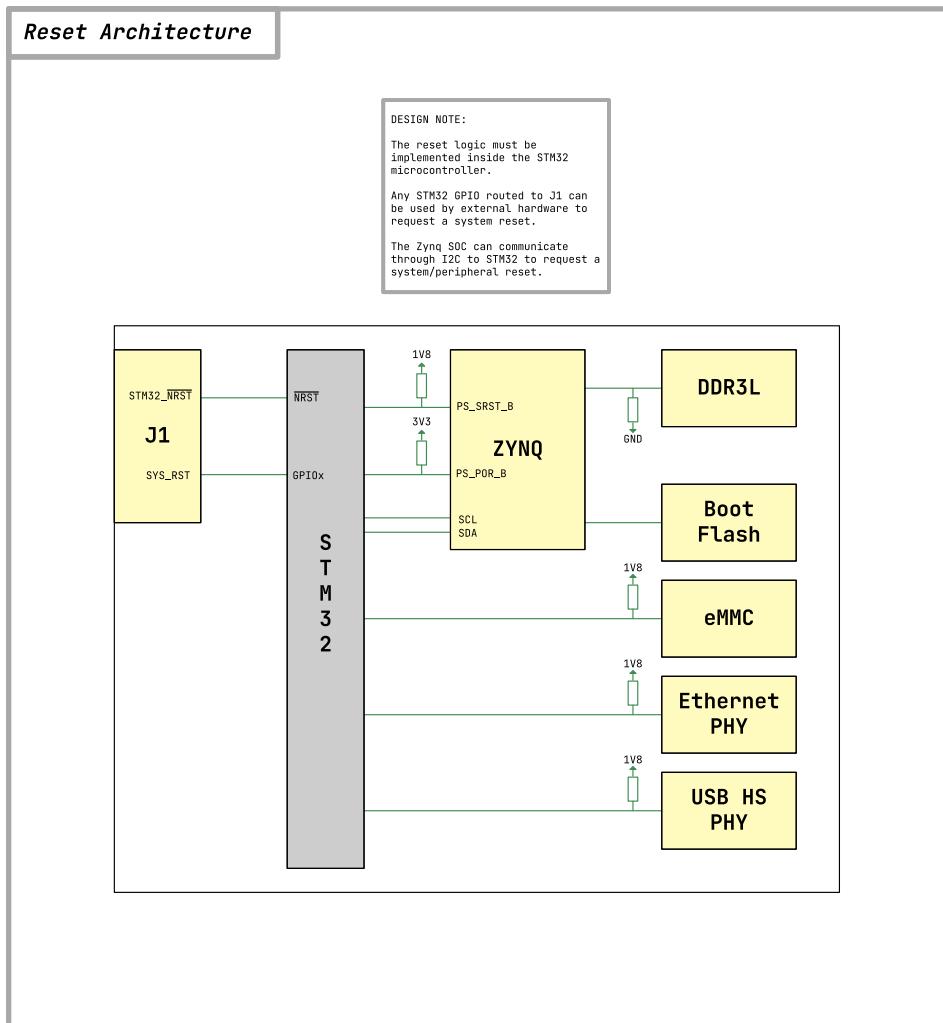
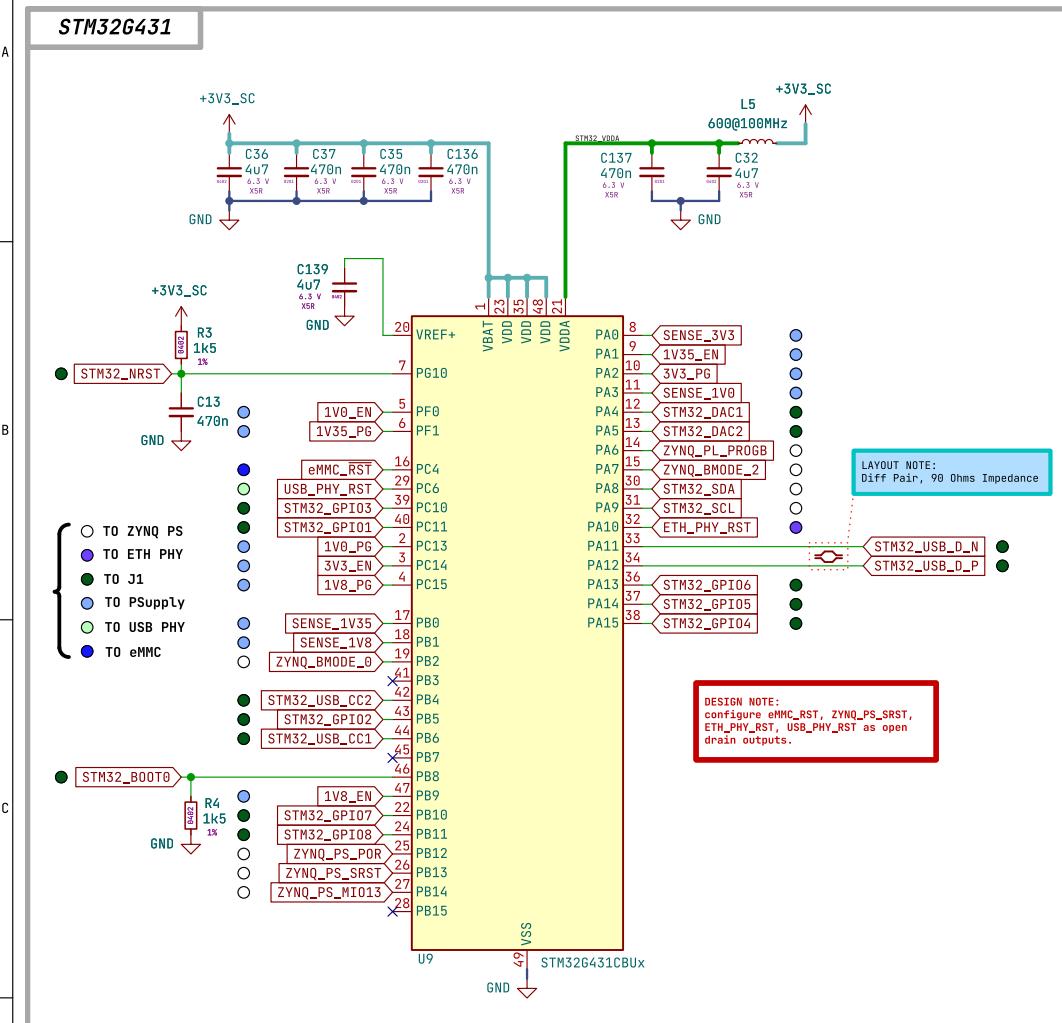
LAYOUT NOTE:
Example text for layout notes.

SCHEMATIC STATUS NOTES

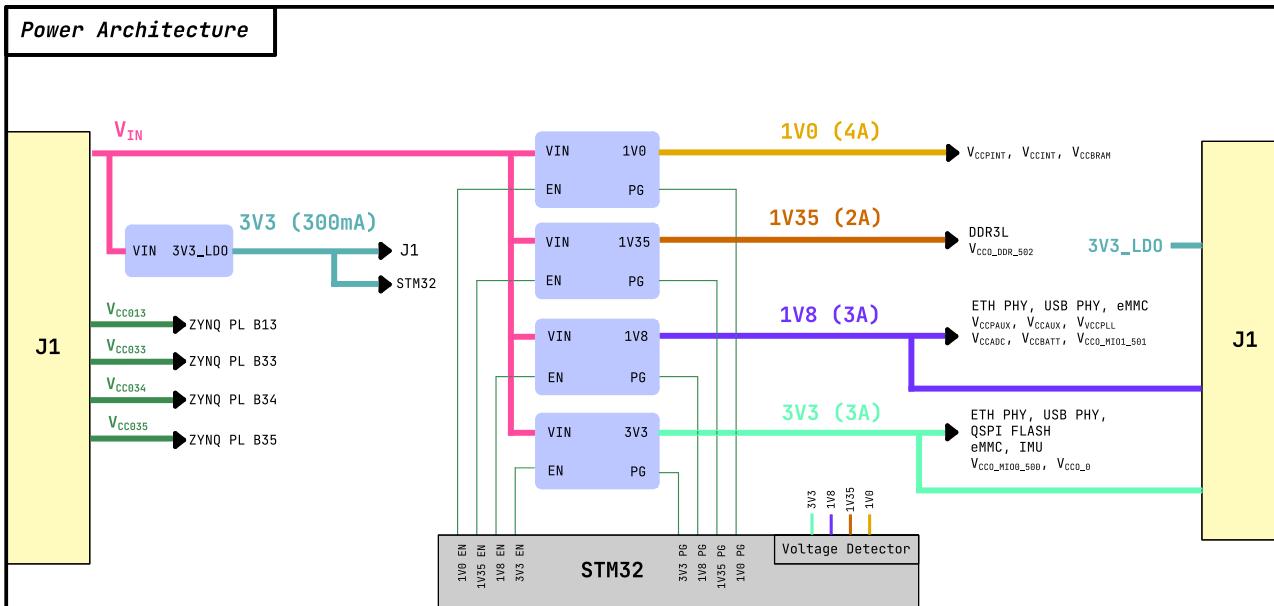
DRAFT, PRELIMINARY, CHECKED, RELEASED

	Title: Block Diagram		Size: A4
	Board: Zynq System on Module		
	Company: Drawn by: G. Incerti	RELEASED	
	Sheet: / File: Zynq_SoM.kicad_sch	Rev: 1.0 Var: No Variant	
Date: 2024-09-22		Page 1 of 16	

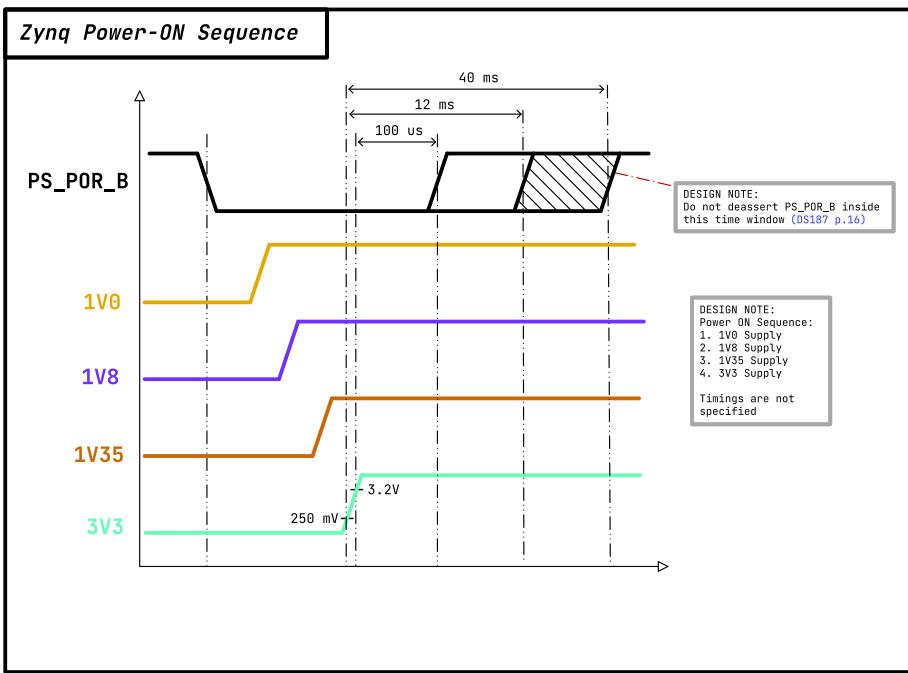
System Controller (STM32)



Title: System Controller		Size: A4
Board: Zynq System on Module		
Company: Drawn by: G. Incerti		RELEASED
Sheet: /System Controller/ File: system_controller.kicad_sch		Rev: 1.0 Var: No Variant
Date: 2024-09-22		Page 2 of 16



	V_{IN}	Voltage	I_{MAX}	Note
I N	V_{IN}	4.2-5V	3.7A	Mandatory
	V_{CCI013}	1.2-3.3V	1.2A	
	V_{CCI033}	1.2-3.3V	1.2A	
	V_{CCI034}	1.2-3.3V	0.9A	used for PUDC
	V_{CCI035}	1.2-3.3V	1.2A	used for ETH_PHY_INT
O U T	$1V8$	$1V8$	0.9A	
	$3V3$	$3V3$	1.2A	
	$3V3_LDO$	$3V3$	100mA	



Block
Diagram

30
ZnSOM

Title: Power Architecture

Size:
A4

Board: Zynq System on Module

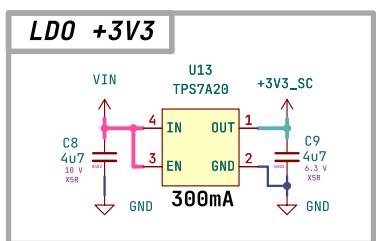
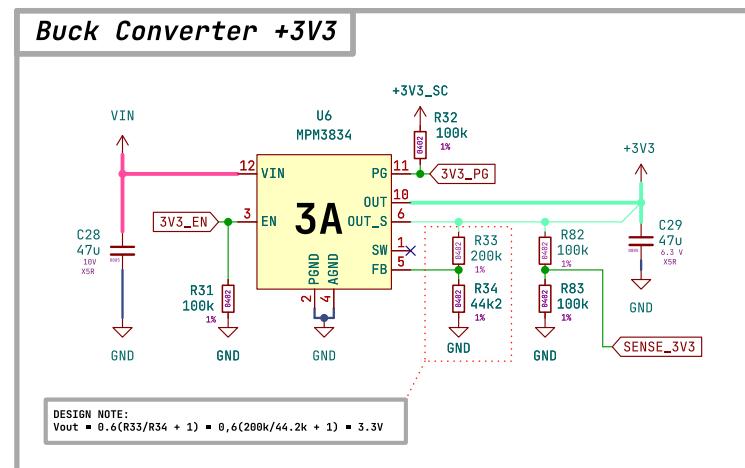
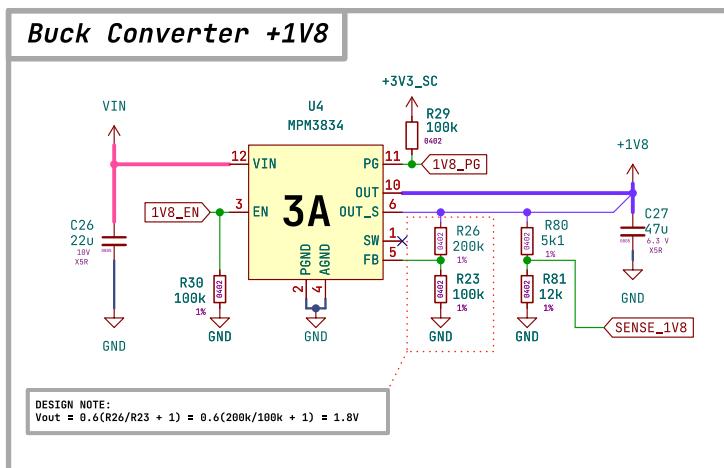
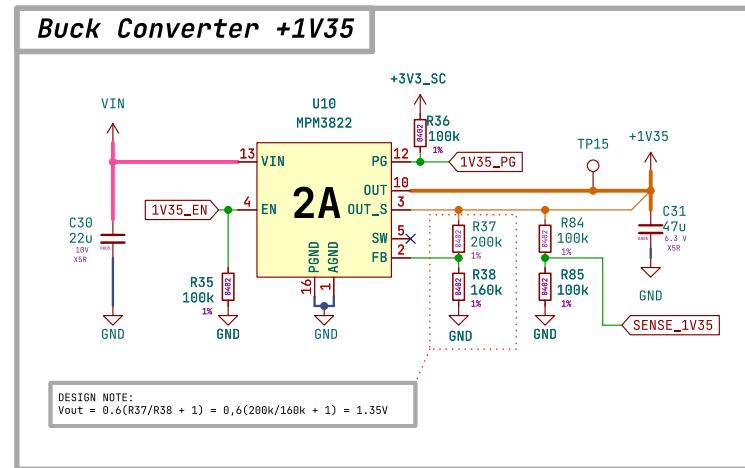
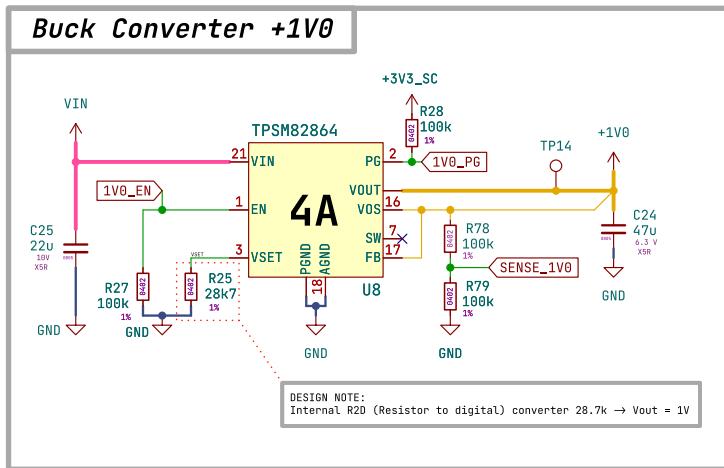
RELEASED

Company:
Drawn by: G. Incerti

Sheet: /Power architecture/
File: power_architecture.kicad_sch
Date: 2024-09-22

Rev: 1.0
Var: No Variant
Page 3 of 16

Power Supplies



Block Diagram

30
ZnSoM

Title: Power Supplies

Board: Zynq System on Module

Size:
A4

Company:
Drawn by: G. Incerti

RELEASED

Sheet: /Power/
File: Power.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

Page 4 of 16

Zynq Power

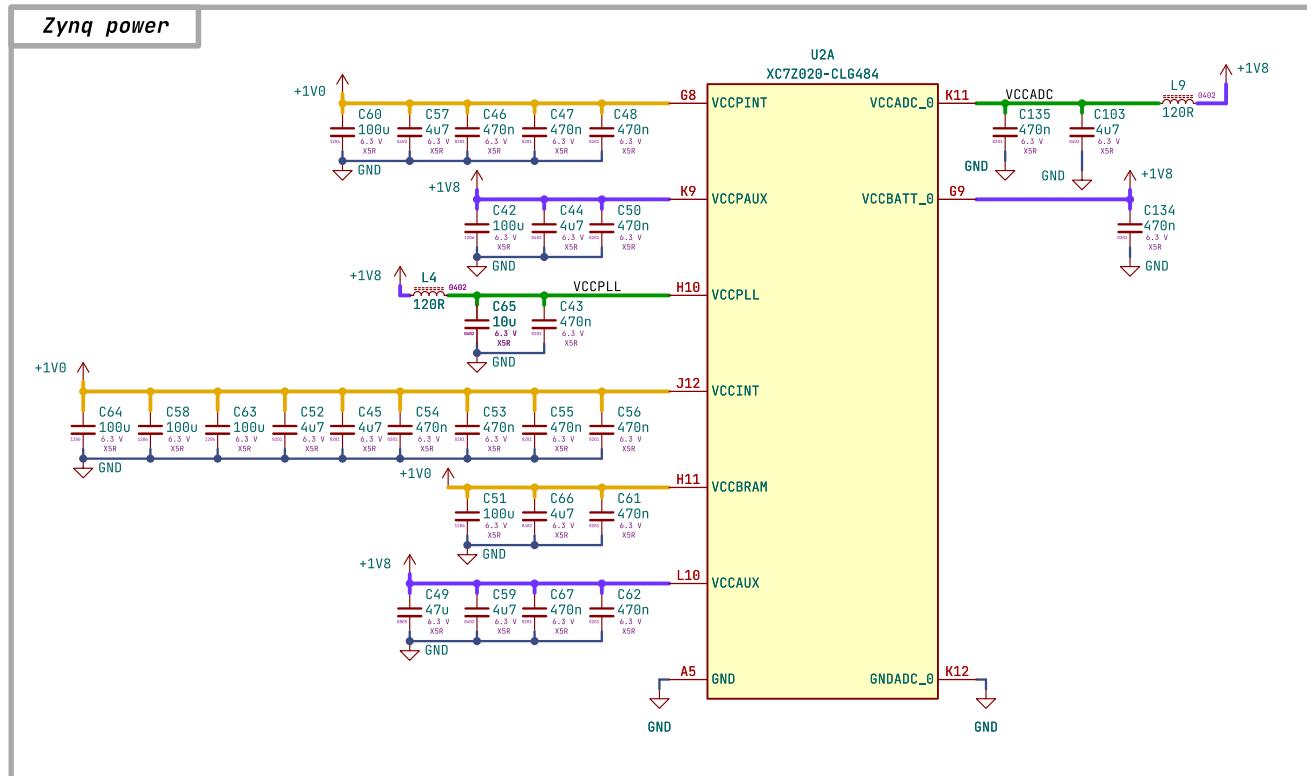


Table 3-2: Required PCB Capacitor Quantities per Device (PS) (Cont'd)

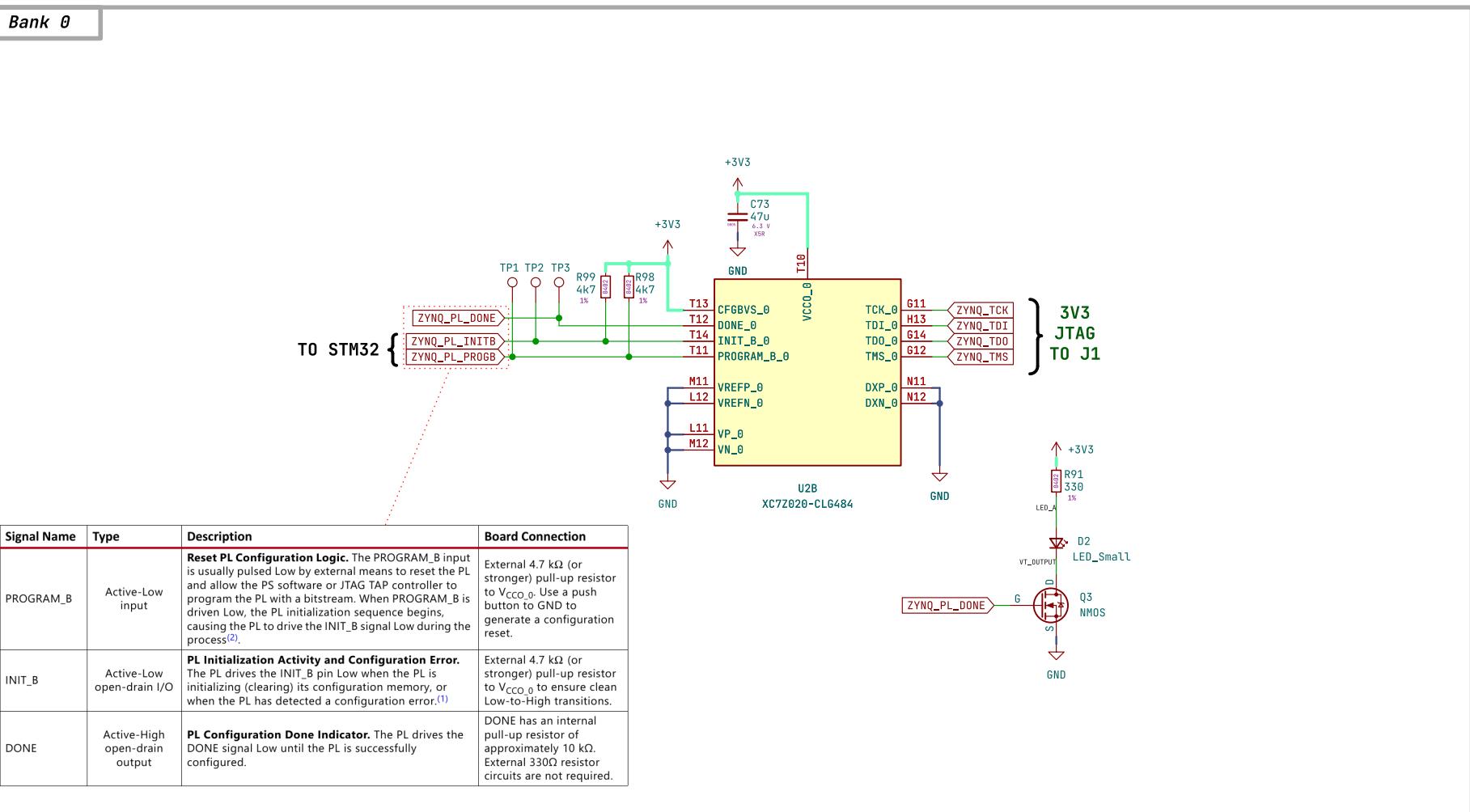
Package	Device	V _{CCPINT}		V _{CCPAUX} ⁽¹⁾		V _{CCO_DDR}		V _{CCO_MIO0}		V _{CCO_MIO1}		V _{CCPLL} ⁽²⁾⁽³⁾	
		100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF
CLG484	Z-7020	1	1	3	1	1	1	1	1	4	1	1	1

Table 3-1: Required PCB Capacitor Quantities per Device (PL)

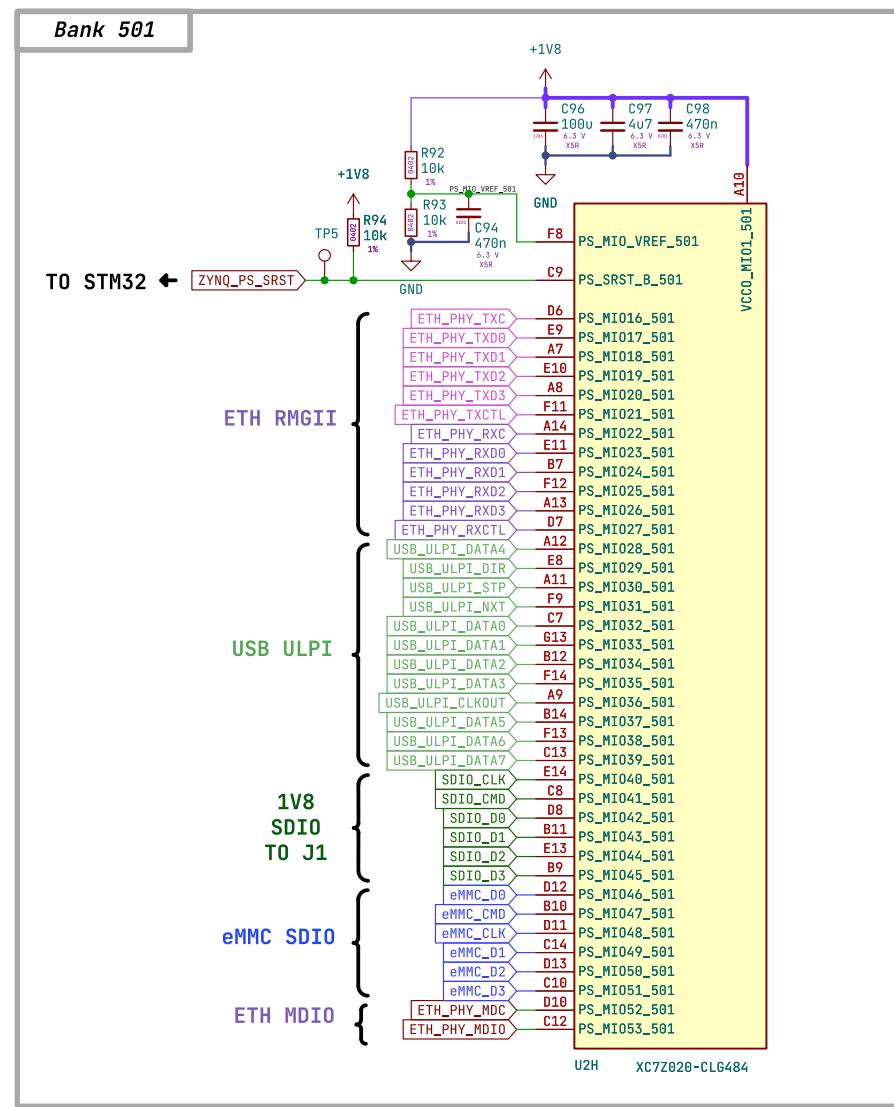
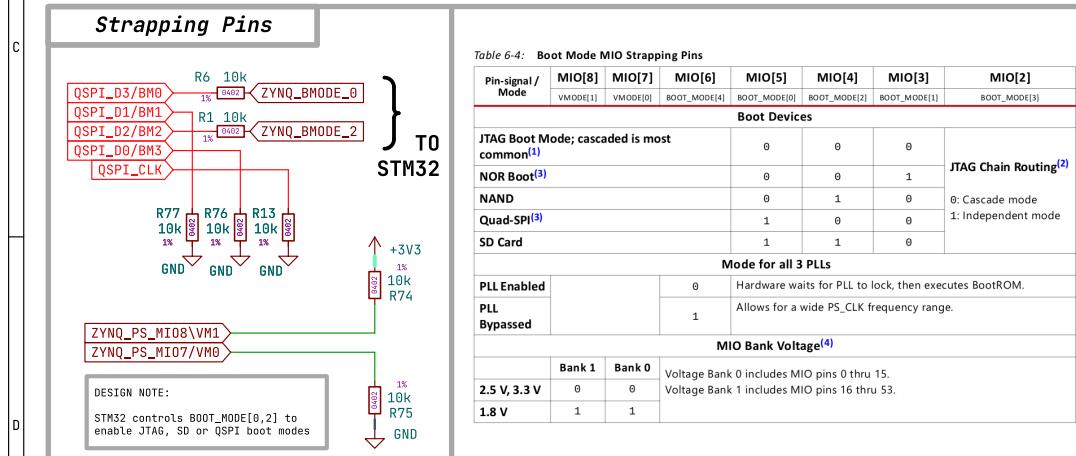
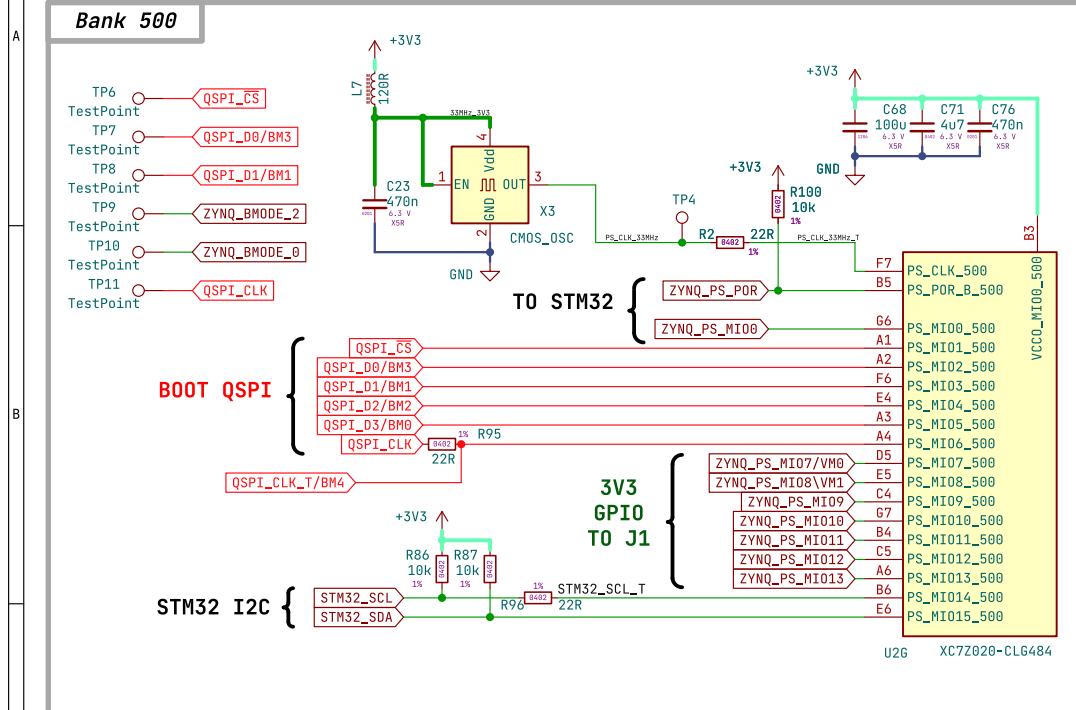
Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}		V _{CCAUX_J0}		V _{CCO} per Bank ⁽³⁾⁽⁴⁾	Bank 0					
		680 μF	330 μF	100 μF	4.7 μF	0.47 μF	100 μF	47 μF	4.7 μF	0.47 μF	47 μF	4.7 μF	0.47 μF	47 μF or 100 μF	4.7 μF	0.47 μF	47 μF			
CLG484	Z-7020	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	1

Block Diagram	30 Zn SOM	Title: Zynq Power	Size: A4
		Board: Zynq System on Module	
Company: Drawn by: G. Incerti	RELEASED		
Sheet: /Zynq Power/ File: zynq_power.kicad_sch	Rev: 1.0 Var: No Variant		
Date: 2024-09-22	Page 5 of 16		

Zynq Bank 0



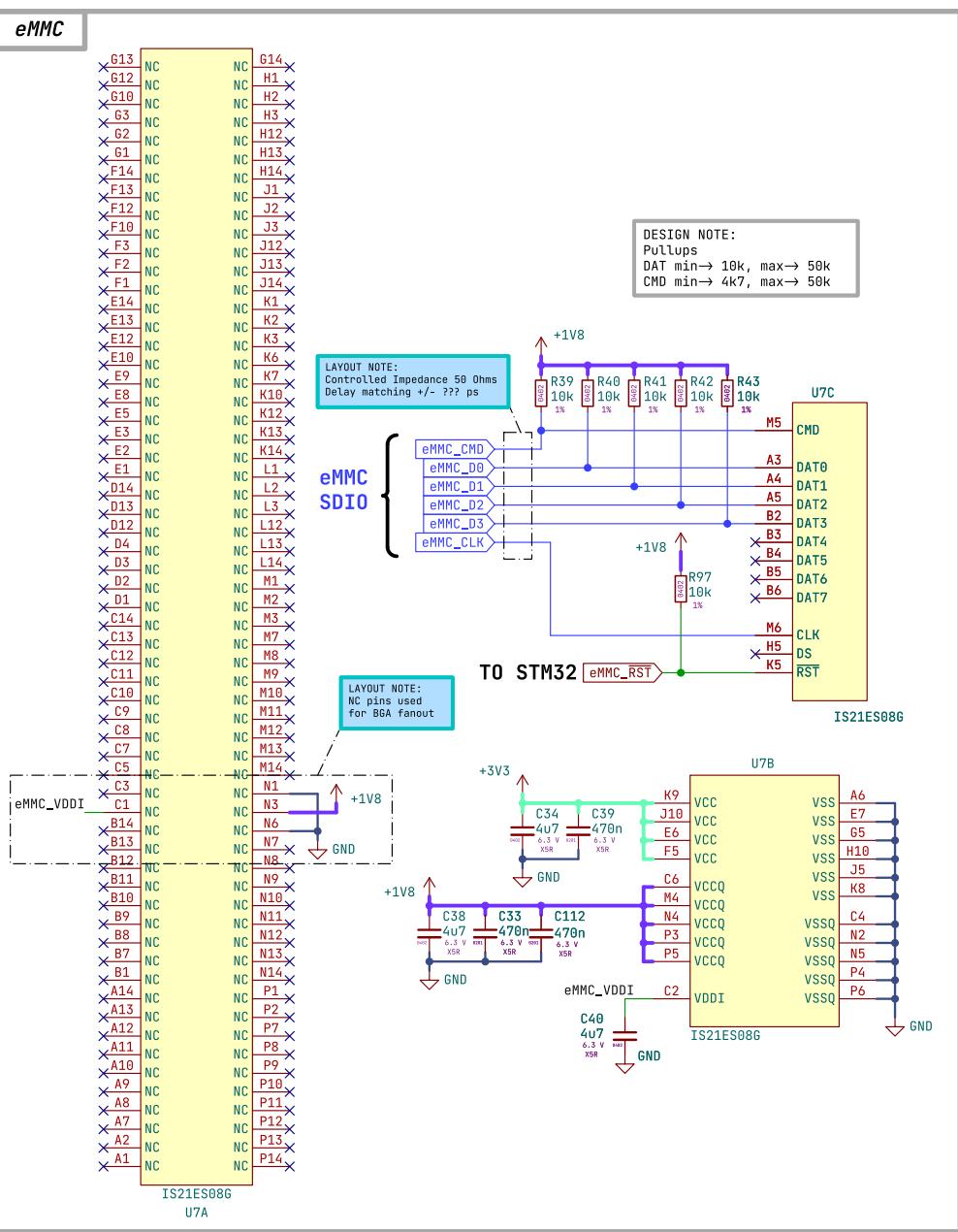
Zynq PS Banks



Title: Zynq PS B500 & B501		Size: A4
Board: Zynq System on Module		
Company:	Drawn by: G. Incerti	RELEASED
Sheet: /Zynq B500-B501/		Rev: 1.0
File: zynq_PS_b500_b501.kicad_sch		Var: No Variant
Date: 2024-09-22		Page 7 of 16

Block Diagram
30 Zn SOM

Flash Memories



Gigabit Ethernet

DESIGN NOTE:
 PLLOFF = 0 → PLL is enabled
 TXDLY = 1 → internal 2ns delay added to TXC
 RXDLY = 1 → internal 2ns delay added to RXC
 PHYAD[2:0] = 001 → set PHY address to 001

LAYOUT NOTE:
 Controlled Impedance 50 Ohms
 Delay matching +/- 10 ps

RGMII
RX

Hardware Config

CONFIG Pin	Configuration
RXD3	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD2	PLLOFF
RXD1	TXDLY
RXD0	RXDLY
LED0	CFG_EXT
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]

Configuration	Description
PHYAD[2:0]	PHY Address. PHYAD sets the PHY address for the device. The RTL8211F(J)/RTL8211FD(J) supports PHY addresses from 00001 to 00111.
Note 1:	An MDIO command with PHYAddress=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Reg24.13=0 (See Table 37).
Note 2:	The RTL8211F(J)/RTL8211FD(J) with PHYAD[2:0]=000 can automatically remember the first non-zero PHY address. This function can be enabled by setting Reg24.6 = 1 (See Table 37).

PLLOFF
ALDPS Mode PLL Off Configuration.
1: Stop PLL when entering ALDPS mode (via 4.7k-ohm to DVDD_RG)
0: PLL continue toggling when entering ALDPS mode (via 4.7k-ohm to GND)

TXDLY
RGMII Transmit Clock Timing Control.

1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG)

0: No delay (via 4.7k-ohm to GND)

RXDLY
RGMII Receive Clock Timing Control.

1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG)

0: No delay (via 4.7k-ohm to GND)

CFG_EXT
I/O Pad External Power Source Mode Configuration

1: Use the external power source for the IO pad (via 4.7k-ohm to 3.3V)

0: Use the integrated LDO to transform the desired voltage for the IO pad (via 4.7k-ohm to GND)

CFG_LDO[1:0]
LDO Output Voltage Selection for I/O pad

External Power Source Voltage Selection for I/O pad.

When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: (via 4.7k-ohm to GND)

00: Reserved.

01: 2.5V

10: 1.8V

11: 1.5V

DRAFT
When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for external power voltage selection for IO pad: (via 4.7k-ohm to 3.3V)

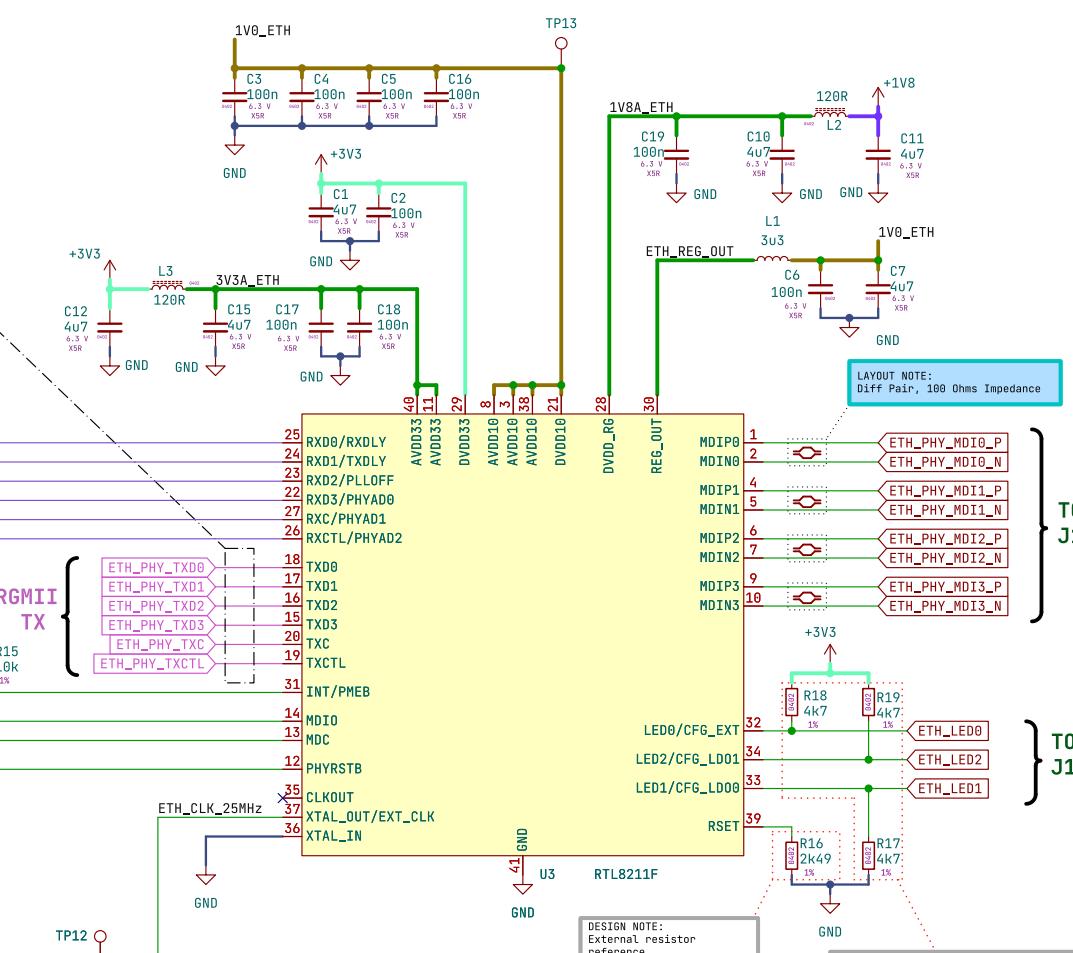
00: 3.3V

01: 2.5V

10: 1.8V

11: 1.5V

DRAFT



Block
Diagram

30
ZnSom

Title: Ethernet PHY

Size: A4

Board: Zynq System on Module

RELEASED

Company: Drawn by: G. Incerti

Rev: 1.0

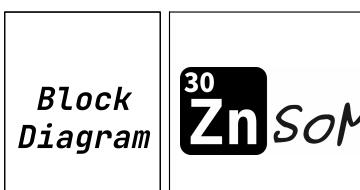
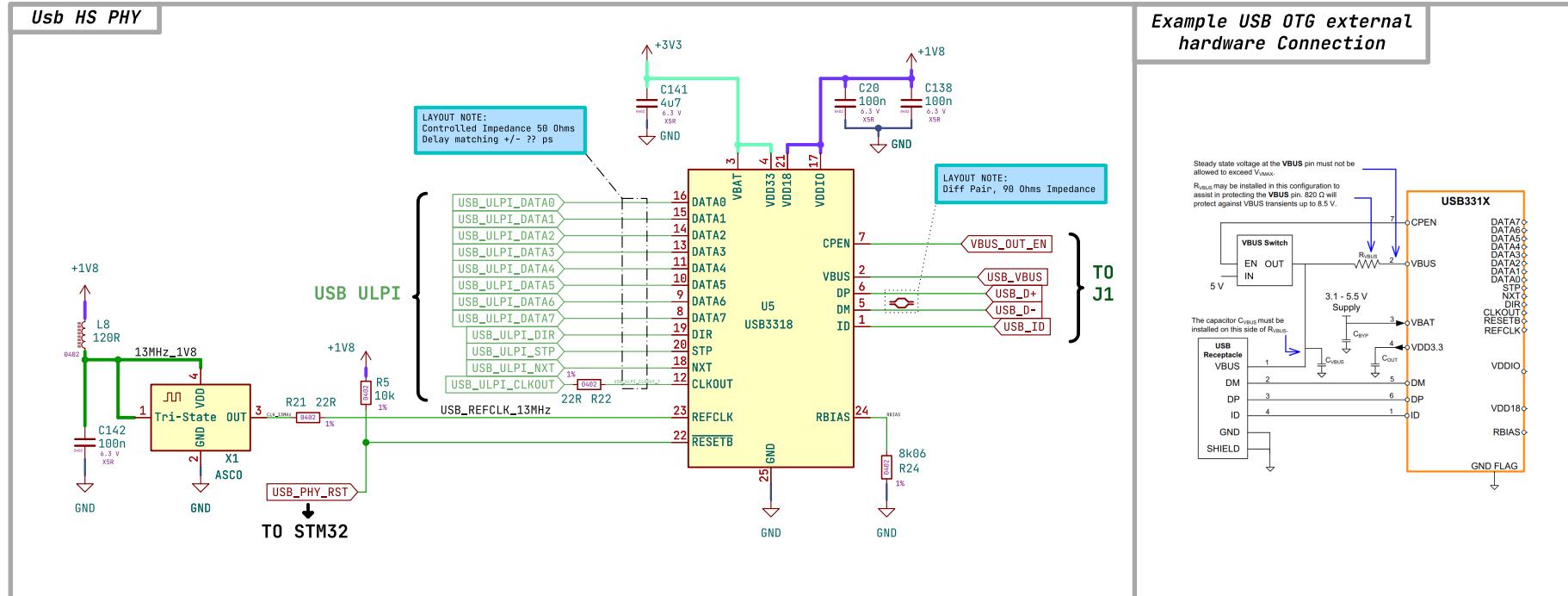
Sheet: /Ethernet PHY/
File: Ethernet PHY.kicad_sch

Var: No Variant

Date: 2024-09-22

Page 9 of 16

USB HS PHY



Title: USB HS PHY

Board: Zynq System on Module

Size: A4

Company:
Drawn by: G. Incerti

RELEASED

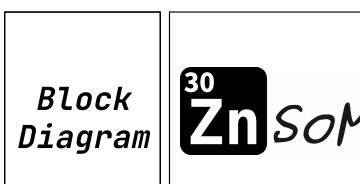
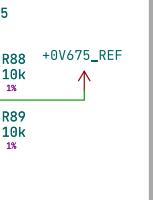
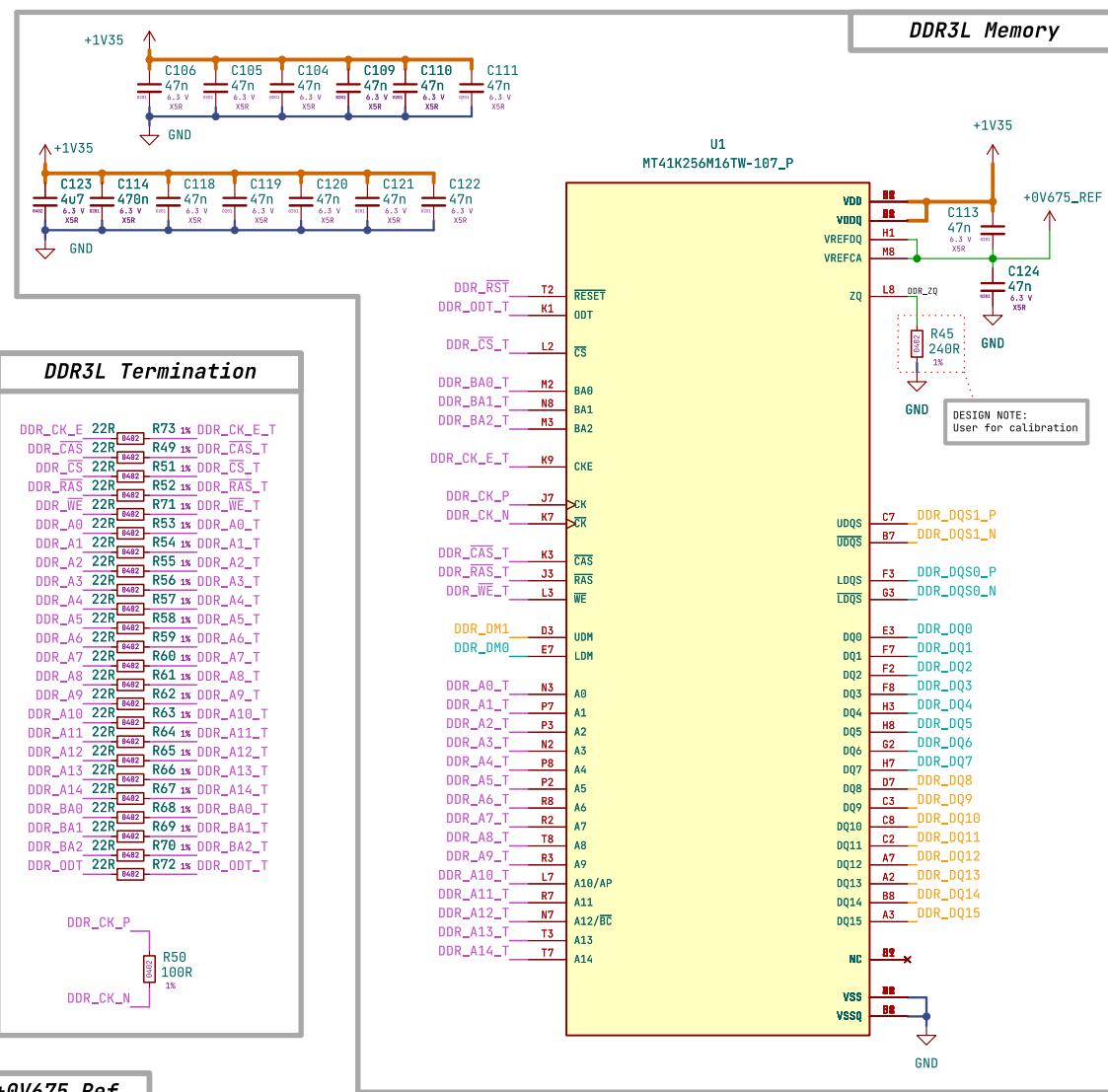
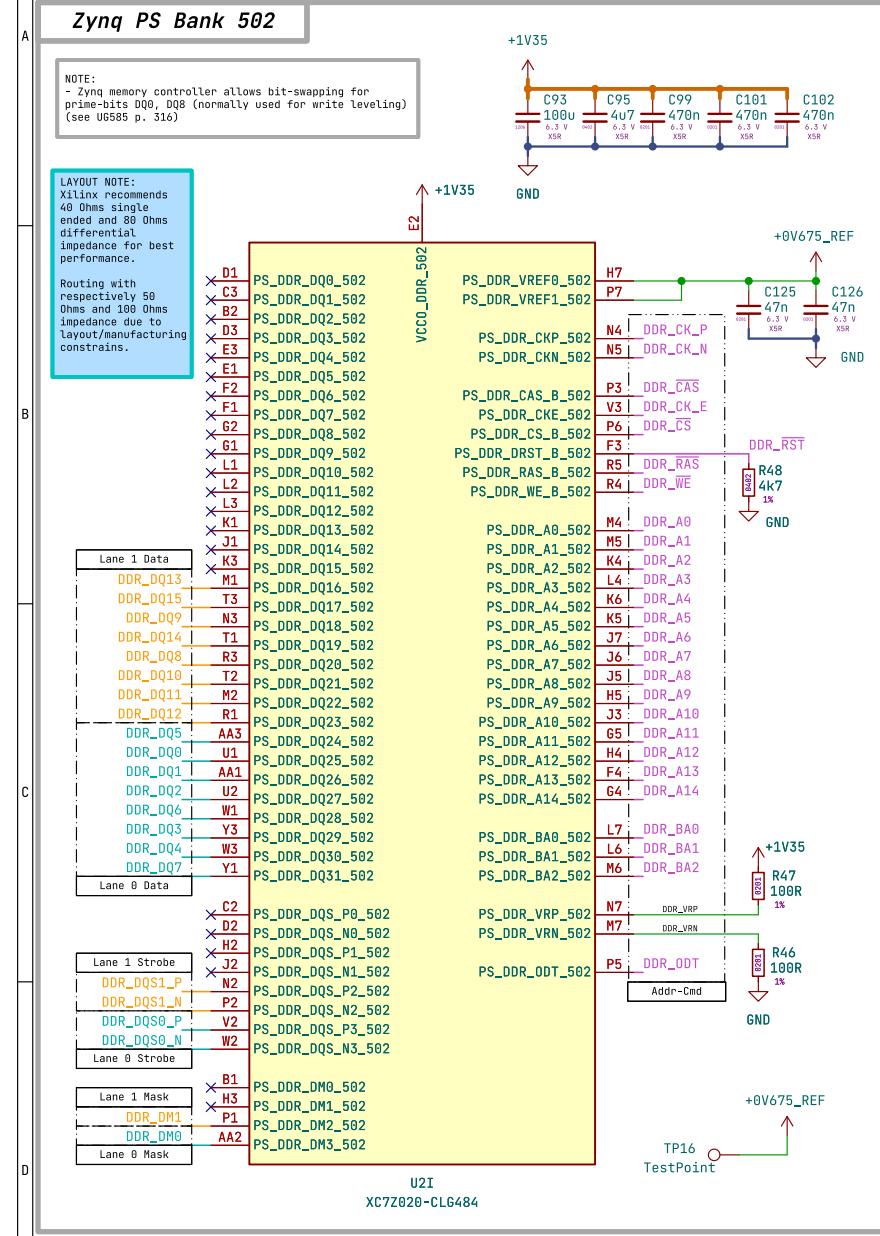
Sheet: /USB HS PHY/
File: usb_hs_phy.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

Page 10 of 16

DDR Memory



Title: Zynq B502 & DDR3L

Board: Zynq System on Module

Size: **A4**

Company:
Drawn by: G. Incerti

RELEASED

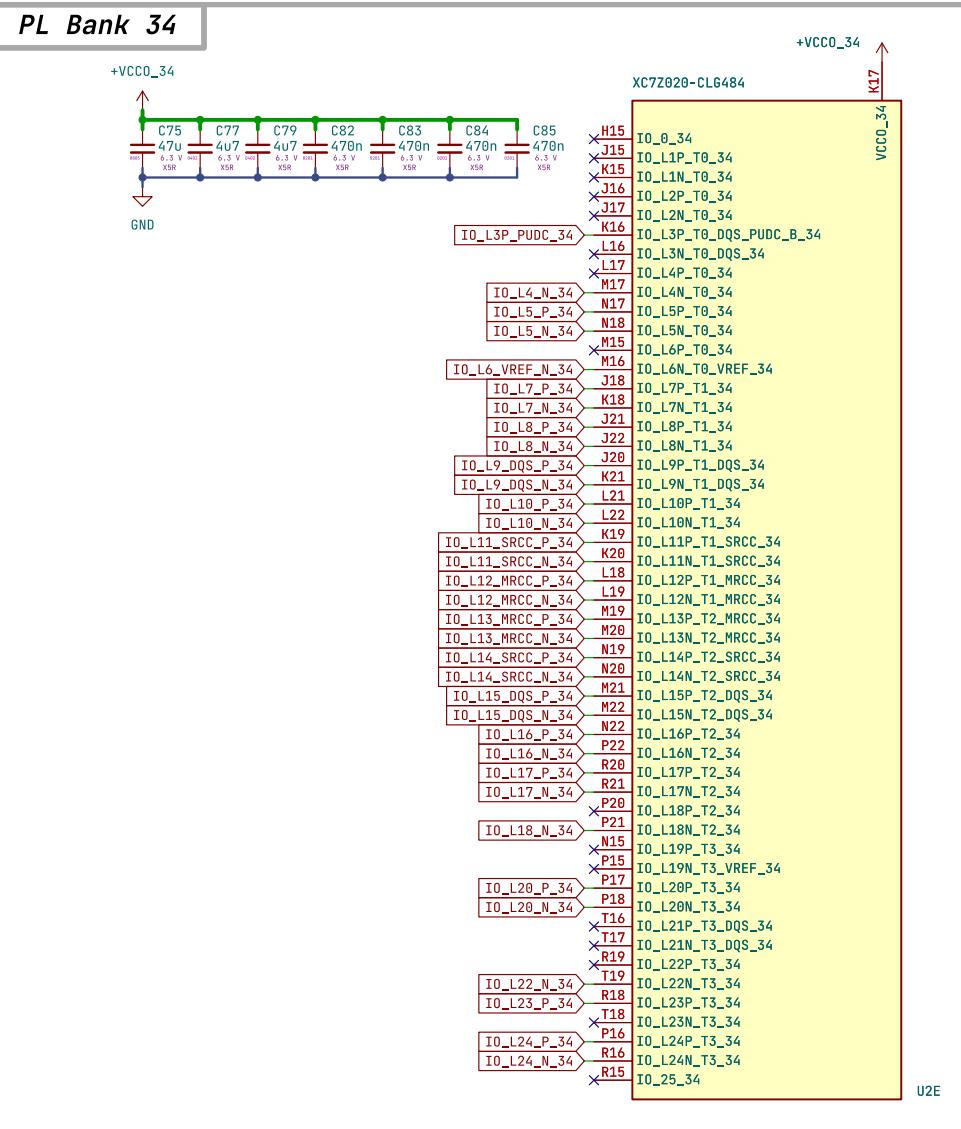
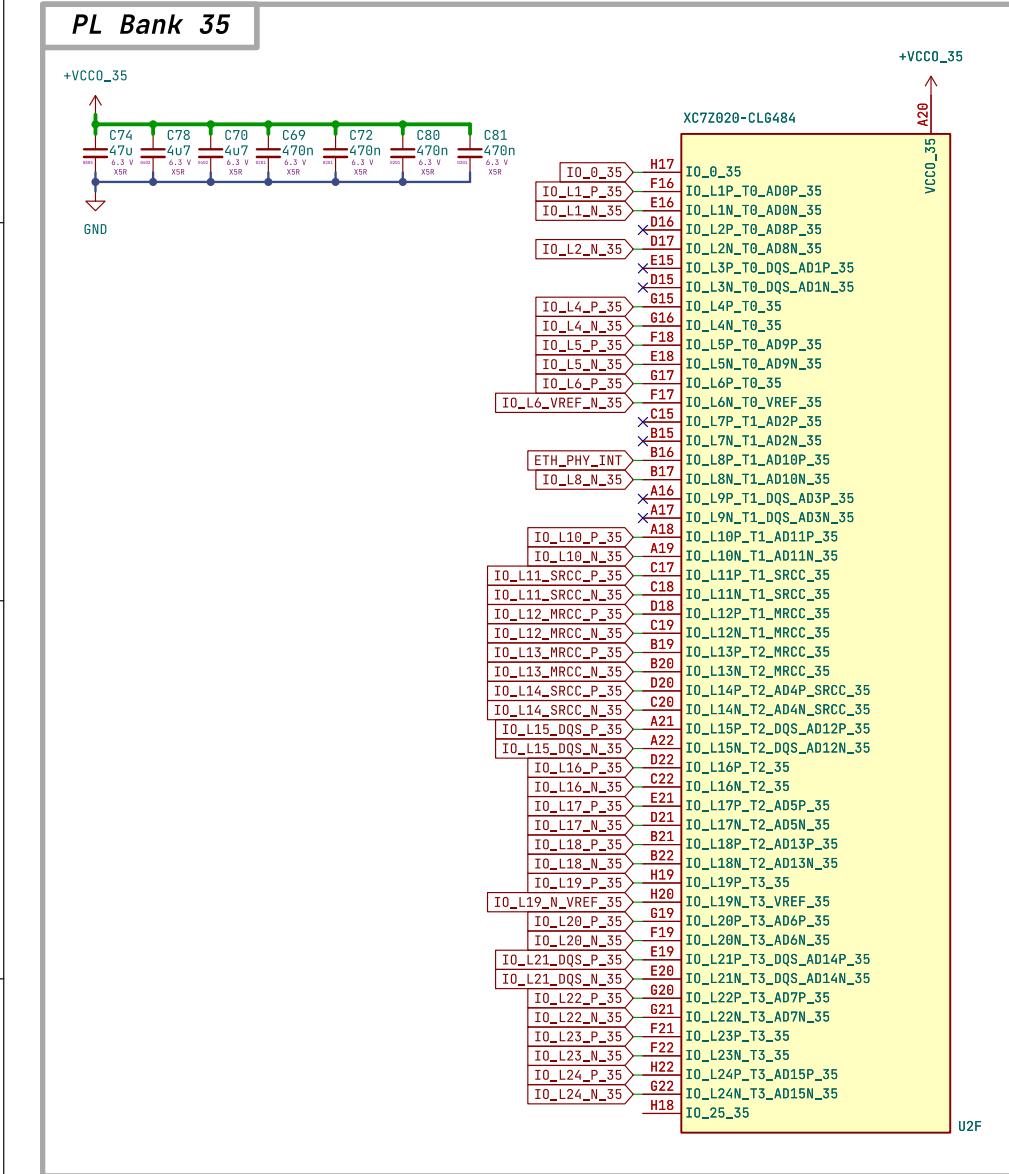
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File: DDR3L.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

Page 11 of 16

Zynq PL Banks 34 & 35



Block
Diagram

30
ZnSOM

Title: Zynq PL B34 & B35

Size:
A4

Board: Zynq System on Module

RELEASED

Company:

Drawn by: G. Incerti

Rev: 1.0

Var: No Variant

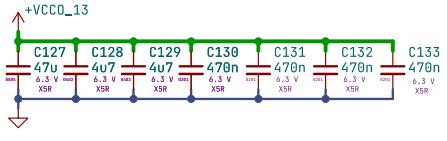
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File: zynq_b33_b34_b35.kicad_sch

Date: 2024-09-22

Page 12 of 16

Zynq PL Banks 13 & 33

PL Bank 13



+VCCO_13
AA10
GND

IO_L1P_13
IO_L1N_T0_13
V9
IO_L2P_T0_13
W8
IO_L2_N_13
W11
IO_L3_P_13
W10
IO_L3N_T0_DQS_13
V12
IO_L4_P_13
W12
IO_L4N_T0_13
U12
IO_L5P_T0_13
U11
IO_L5N_T0_13
U10
IO_L6P_T0_13
U9
IO_L6N_T0_VREF_13
AA12
IO_L7_P_13
AB12
IO_L7N_T1_13
AA11
IO_L8P_T1_13
AB11
IO_L8N_T1_13
AB10
IO_L9P_T1_DQS_13
AB9
IO_L9N_T1_DQS_13
Y11
IO_L10_P_13
Y10
IO_L10_N_13
AA9
IO_L11_SRCC_P_13
AA8
IO_L11_SRCC_N_13
V9
IO_L12_MRCC_P_13
Y8
IO_L12_MRCC_N_13
Y6
IO_L13_MRCC_P_13
Y5
IO_L13_MRCC_N_13
AA7
IO_L14_P_SRCC_13
AA6
IO_L14_N_SRCC_13
AB2
IO_L15_P_13
AB1
IO_L16_P_13
AB4
IO_L16_N_13
AB7
IO_L17_P_13
AB6
IO_L17N_T2_13
Y4
IO_L18_P_13
AA4
IO_L18N_T2_13
R6
IO_L19P_T3_13
T6
IO_L19N_T3_VREF_13
T4
IO_L20P_T3_13
U4
IO_L20N_T3_13
V5
IO_L21P_T3_DQS_13
U6
IO_L22P_T3_13
U5
IO_L22N_T3_13
V7
IO_L23P_T3_13
W7
IO_L23N_T3_13
W6
IO_L24P_T3_13
W5
IO_L24N_T3_13
U7
IO_25_13

XC7Z020-CLG484

PL Bank 33

+VCCO_33

stitching, close to IO_L19_VREF_N_33 and IO_L1P_13

GND

+VCCO_33

AA29
VCCO_33

U19	IO_0_33
T21	IO_L1P_T0_33
IO_L1N_T0_33	
T22	IO_L2P_T0_33
IO_L2N_T0_33	
U22	IO_L3P_T0_33
IO_L3_DQS_P_33	W22
IO_L3_DQS_N_33	W20
U20	IO_L4P_T0_33
IO_L4_N_33	
V20	IO_L5P_T0_33
IO_L5_N_33	
V18	IO_L6P_T0_33
IO_L6_N_VREF_33	
V19	IO_L6N_T0_VREF_33
AA22	IO_L7P_T1_33
IO_L7_N_33	
AA22	IO_L7N_T1_33
IO_L8_P_33	AB22
IO_L8_N_33	AB21
Y20	IO_L9P_T1_DQS_33
IO_L9_DQS_P_33	Y21
IO_L9_DQS_N_33	AB19
AB20	IO_L10P_T1_33
IO_L10_N_33	
Y19	IO_L10N_T1_33
IO_L11_SRCC_P_33	AA19
IO_L11_SRCC_N_33	IO_L11N_T1_SRCC_33
IO_L12_MRCC_P_33	Y18
IO_L12_MRCC_N_33	AA18
W17	IO_L13P_T2_MRCC_33
IO_L13P_T2_MRCC_13	
W18	IO_L13N_T2_MRCC_33
IO_L14_SRCC_P_33	Y16
IO_L14_SRCC_N_33	IO_L14N_T2_SRCC_33
U15	IO_L15P_T2_DQS_33
IO_L15_VREF_N_33	U16
IO_L15_N_33	IO_L15N_T2_DQS_33
V17	IO_L16P_T2_33
IO_L16_N_33	
AA17	IO_L17P_T2_33
IO_L17_N_33	
AB17	IO_L17N_T2_33
IO_L18_P_33	AA16
IO_L18_N_33	AB16
IO_L19_P_33	Y14
IO_L19N_T3_VREF_33	Y15
IO_L15_P_33	V13
IO_L20_P_33	W13
IO_L20_N_33	IO_L20N_T3_33
W15	IO_L21P_T3_DQS_33
IO_L21_DQS_P_33	Y15
IO_L21_DQS_N_33	IO_L21N_T3_DQS_33
Y14	IO_L22P_T3_33
IO_L22_P_33	AA14
IO_L22_N_33	IO_L22N_T3_33
Y13	IO_L23P_T3_33
IO_L23_N_33	AA13
AB14	IO_L23N_T3_33
IO_L24_P_33	AB15
IO_L24_N_33	IO_L24N_T3_33
U14	IO_25_33

XC7Z020-CLG484

Block
Diagram

30
Zn
Som

Title: Zynq PL B13 & B33

Size:
A4

Board: Zynq System on Module

RELEASED

Company:
Drawn by: G. Incerti

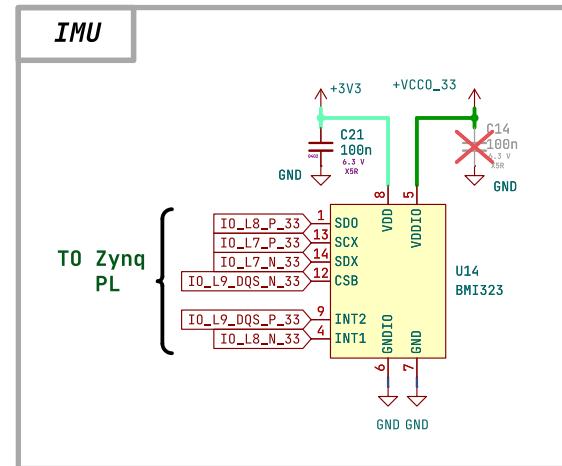
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File: zynq_PL_b13.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

Page 13 of 16

Inertial Measurement Unit



Block
Diagram

30
ZnSOM

Title: IMU

Board: Zynq System on Module

Size:
A4

Company:
Drawn by: G. Incerti

RELEASED

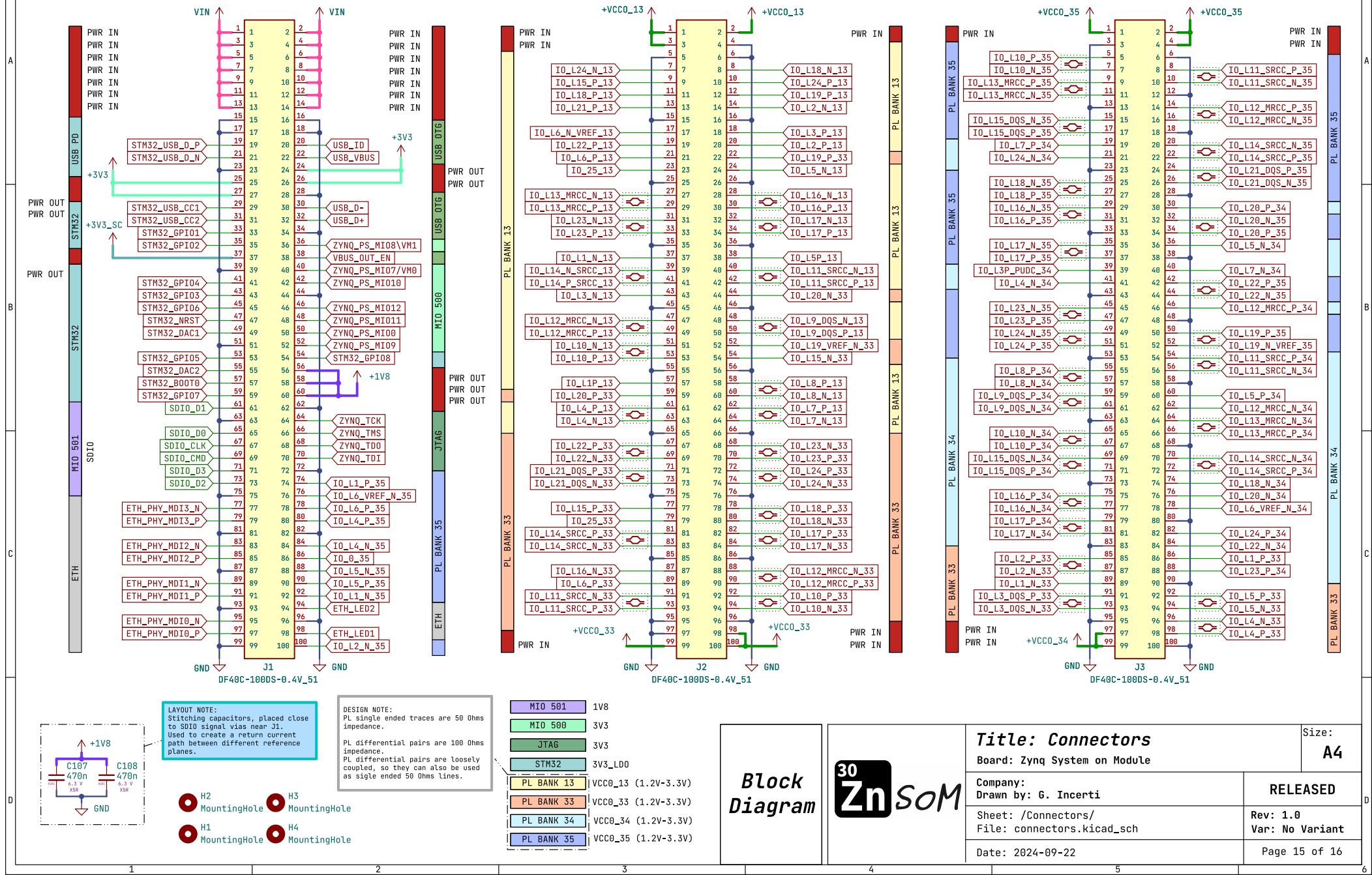
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File: Sensors.kicad_sch

Rev: 1.0
Var: No Variant

Date: 2024-09-22

Page 14 of 16

Connectors



A

A

<i>REV</i>	<i>Description</i>	
1.0	Initial revision	

B

B

C

C

D

D

**Title: Revision History**Size:
A4

Board: Zynq System on Module

Company:
Drawn by: G. Incerti**RELEASED**Sheet: /Revisions changes/
File: revision_changes.kicad_schRev: 1.0
Var: No Variant

Date: 2024-09-22

Page 16 of 16