# Lab 7: Matrix Multiplication Circuit Design


National Chiao Tung University
Chun-Jen Tsai
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# Lab 7: Matrix Multiplication

- In this lab, you will design a circuit to do 4×4 matrix multiplications.
  - The user press BTN1 to start the circuit
  - The circuit reads two 4×4 matrices from a file on the SD card, perform the multiplication, and print the output matrix through the UART to a terminal window
- The deadline of the lab is on 11/28

# Design Constraint of Lab6

- You must use no more than 16 multipliers to implement your circuit
  - Each Atrix-7 35T FPGA on the Arty board has 90 20×18-bit multipliers
- Your grade will be based on correctness and logic usage; the smaller the logic, the better the grade
  - The “size” of the logic is calculated by the number of physical multipliers, LUTs, Flip-flops (FFs), and BRAMs

# The Input Matrix Format

- Each input matrix has 16 unsigned 8-bit elements of values between 0 ~ 255 in column-major format

32 numbers for two 4×4 matrices

```
MATX_TAG↵
E1↵
6B↵
D7↵
1D↵
B6↵

…

6E↵
BC↵
02↵
D3↵
```

- The output matrix has 16 unsigned 18-bit elements

# The Output Format

- After the multiplication, your circuit must prints the following messages to the UART:

```
The result is:↵
[ 11CE9, 18749, 0EE26, 16F64 ]↵
[ 0ED5B, 1091D, 04768, 06376 ]↵
[ 167B9, 1BF8A, 0E496, 1504F ]↵
[ 09901, 0F404, 08F23, 0C4A5 ]↵
↵
```