CS2115-1819A FINAL EXAM

Computer Organization (City University of Hong Kong)

CITY UNIVERSITY OF HONG KONG

Course code & title : CS2115 Computer Organization

Session : Semester A 2018/19

Time allowed : Two hours

This paper has 20 pages (including this cover page).

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1. This paper consists of 4 questions.
2. Answer ALL questions.
3. Write your answers in the space provided.

Student Name: _____

Student ID: _____

Seat number: _____

1	2	3	4	Total

*This is a **closed-book** examination.*

No materials or aids are allowed during the whole examination. If any unauthorized materials or aids are found on a candidate during the examination, the candidate will be subject to disciplinary action.

NOT TO BE TAKEN AWAY

Problem 1 (20 marks)

a) For the decimal number $(12.625)_{10}$, convert it to the **binary** and **hexadecimal** forms, respectively. For the binary number $(11010.011)_2$, convert it to the **decimal** form. (6 marks)

b) Design a finite state machine (FSM) that can detect the input pattern '101'. The input to the machine is a string of bits, and the system will detect whether the three most recent input bits up to now is '101'. If it is, then the output is '1', otherwise, the output is '0'. For example, for the input string '0010101001010', the system will output '0000101000010'. **i) Draw the state transition diagram of this FSM, clearly label the state, input, and output in the diagram. ii) Write down the state table.** (14 marks)

Hint: You can define 3 (or 4) states: s_0 for the states that last input is 0, s_1 for the states that last input is 1, and s_2 for the state that last two inputs are 10, (or s_3 for the state that last three inputs are 101).

Problem 2 (25 marks + 6 bonus marks)

We have a logic expression $Y = \bar{A}B + BC$ with 3 variables.

a) Write the truth table of the function Y. (7 marks)

b) Write the function F in the canonical SOP and POS form. (7 marks)

c) Draw the circuit of the function $Y = \bar{A}B + BC$. (7 marks)

d) The neural network can also be used to compute a logic function. It consists of several layers of neurons to do the computing. For example, the following structure in Fig. 1 is to compute the function $F = g(a_1 + a_2A + a_3B)$ (note that here it is the arithmetic operation), where the function $g(x)$ is shown in Fig. 2 with the property that $g(x) \approx 0$ for $x \leq -10$ and $g(x) \approx 1$ for $x \geq 10$. In this case, we can use this simple neural network to do the logic AND or OR operations by giving appropriate values to a_1, a_2, and a_3. For example, by setting $a_1 = -30$, $a_2 = a_3 = 20$, we have $F = g(-30) \approx 0$ for $A = B = 0$, $F = g(-10) \approx 0$ for $A = 1, B = 0$, or $A = 0, B = 1$, and $F = g(10) \approx 1$ for $A = 1, B = 1$. This is a realization of the AND gate. As another example, by setting $a_1 = -10$, $a_2 = a_3 = 20$, we have $F = g(-10) \approx 0$ for $A = B = 0$, $F = g(10) \approx 1$ for $A = 1, B = 0$, or $A = 0, B = 1$, and $F = g(30) \approx 1$ for $A = 1, B = 1$. This is a realization of the OR gate.

Using this analysis method, **write down the expression of the logic function G with inputs A and B shown in Fig. 3.** (4 marks) Hint: Draw the truth table.

e) **(Bonus point question) Can you design a neural network to compute the logic $Y = \bar{A}B + BC$? Draw your neural network,** clearly label the neurons and the edges connecting them, and justify your answer. (6 bonus marks, however, you cannot get above 100 points for this exam.)

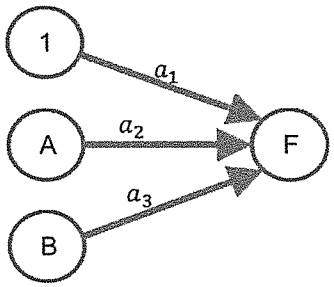


Figure 1: Neuron illustration

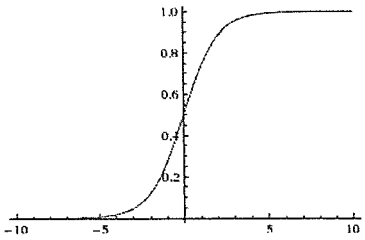


Figure 2: $g(x)$ function.

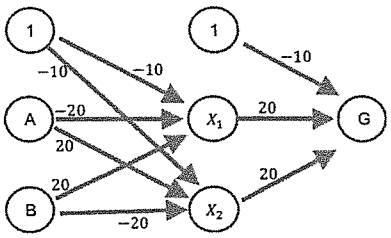


Figure 3: Calculating G.

Problem 3 (30 marks)

In class, we have learned the binary half adder and the binary full adder in CPU. In a 2's complement number system, we can use the adder and 2's complement calculation to do the subtraction. Now in this problem, we use similar ideas to design the system with only subtractors.

a) Design a binary half subtractor and a binary full subtractor. Given two binary inputs X, Y and the borrow in B_{in}, the binary half subtractor will perform $X - Y$ and output a difference D with a borrow out B_{out}, and the binary full subtractor will perform $X - Y - B_{in}$ and output a difference D with a borrow out B_{out}. The truth tables are given in Figs. 4 and 6 and their representation diagrams are shown in Figs. 5 and 7. **Write down the logic expressions of D and B_{out} for both the half subtractor and the full subtractor. Draw the circuits of the half subtractor and the full subtractor.** (10 marks)

b) Use two half subtractors together with some of the basic gates AND, OR, NOT, or XOR to construct a full subtractor. (6 marks)

c) Design a 4-bit subtractor using full subtractors, i.e., calculate $X_3X_2X_1X_0 - Y_3Y_2Y_1Y_0$ to get a difference $D_3D_2D_1D_0$ and a 1-bit borrow out B_{out}, where $X_3X_2X_1X_0$, $Y_3Y_2Y_1Y_0$, and $D_3D_2D_1D_0$ represent 4-bit binary numbers. **Draw the circuit.** You can use the full subtractor representation in Fig. 7. Clearly label the necessary input/output names. How can you determine if there is an overflow for the subtraction of two signed numbers in their 2's complement form? Write down the logic expression for V, where $V = 1$ indicates there is an overflow, and $V = 0$ otherwise. (8 marks)

d) Design a 4-bit adder of two signed numbers in their 2's complement form using full subtractors together with some of the basic gates AND, OR, NOT, or XOR. **Draw your circuit.** You can use the full subtractor representation in Fig. 7. (6 marks)

Hint: $A + B = A - (-B)$.

Note: You can either simply the logic expressions and circuits or not, as long as it is correct. You do not need to draw the overflow detection part in questions c) and d).

Inputs		Outputs	
X	Y	D	B_{out}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure 4: Truth table of the half substractor.

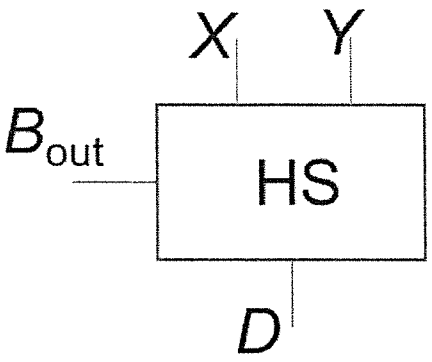


Figure 5: Half subtractor diagram.

Inputs			Outputs	
X	Y	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Figure 6: Truth table of the full substractor.

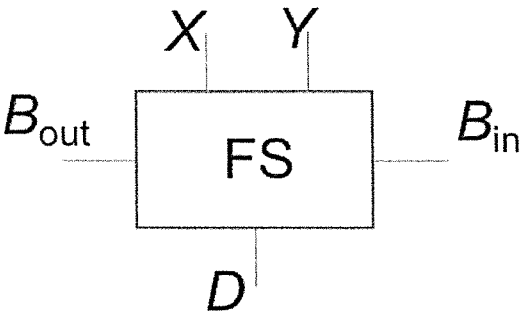
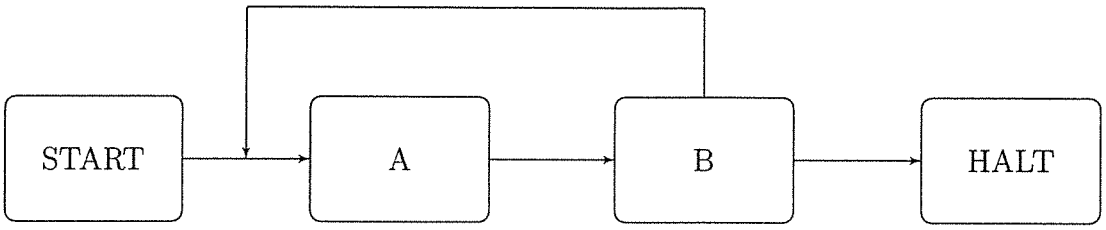


Figure 7: Full subtractor diagram.

Problem 4 (25 marks)

a) The diagram below is about instruction cycle, **what phases are A and B represent for? Identify which operation belongs to A, and which operation belongs to B.** (9 marks)



(a) CPU fetches an instruction from memory location pointed to by PC

(b) Store moving data from CPU to memory

(c) Program Counter (PC) holds the address of next instruction to fetch

(d) Add the immediate number X to the number in register R7

b) Why do we use the cache memory in computer systems? Do we usually use DRAM or SRAM for the cache memory? What are the differences between DRAM and SRAM? (8 marks)

c) Give an example of the RISC architecture and an example of the CISC architecture. What are the key differences between these two architectures? Which one is more suitable for pipelining and why? (8 marks)