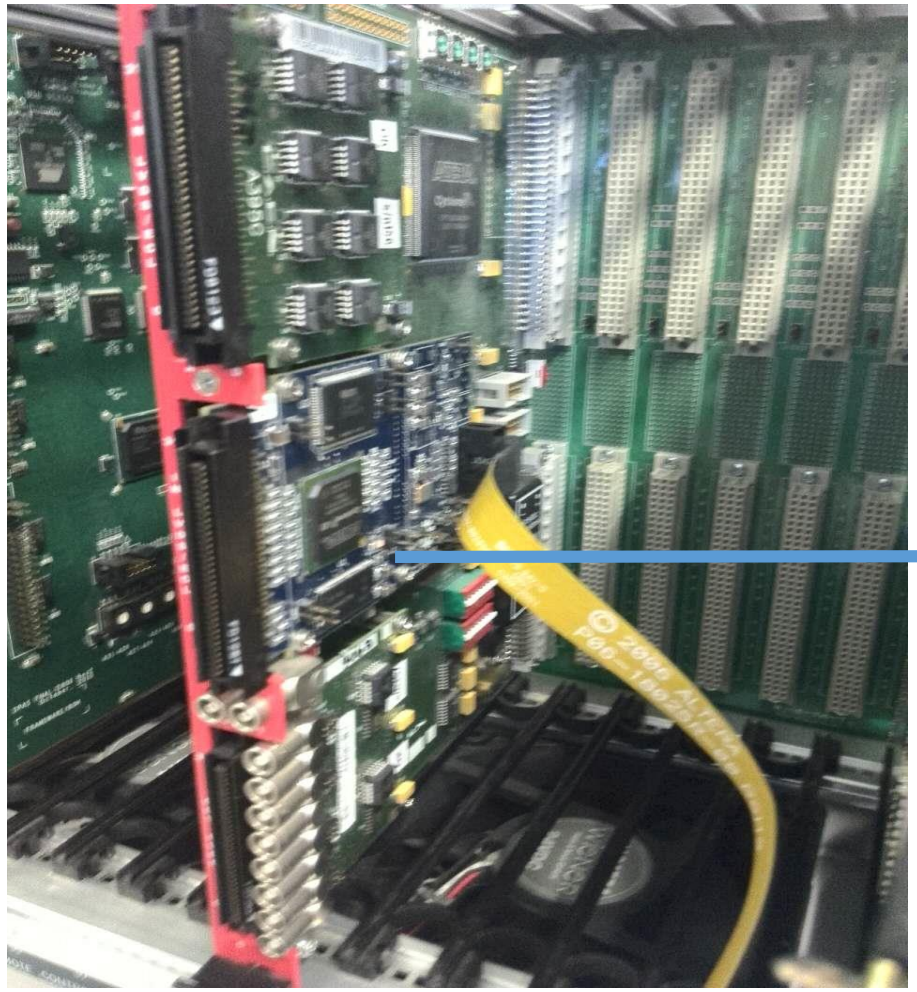
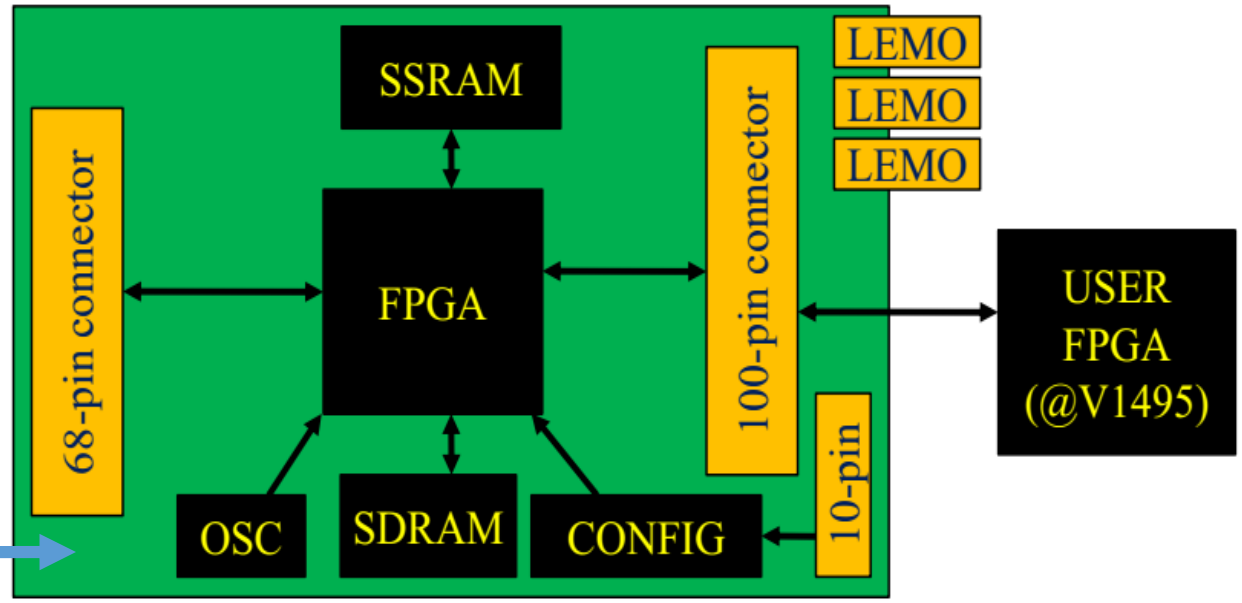
FPGA Design on V1495&Daughter Card





32-MB SDRAM, 2MB SSRAM and FPGA used as interface and memory controller

V1495

Lv0 for pulser test

Lv1 for TDC readout during beam-off & trigger decision

A/B/D port as data input (32*3 chns)

C port as data output -> Lv2

E/F port free

Daughter Card

- **FPGA** CycloneIII EP3C16F484C8
- **2MB SSRAM (not used)**
- **32-MB SDRAM** **4 Meg *16 *4 banks**

  Row addr. A[12..0] (8K)

  Col addr. A[8..0] (512)

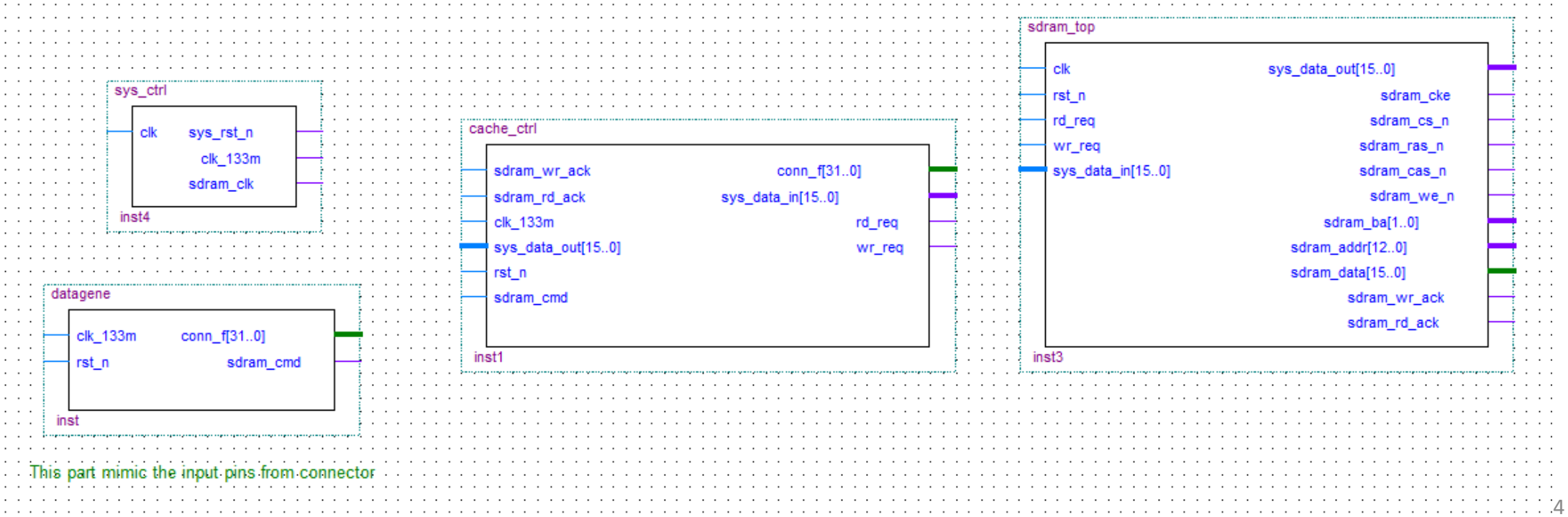
  Bank addr. BA[1..0] (4)

256*16bits/event => A total of 2 * 8K * 4 = 64K words

FPGA Design on the Daughter Card

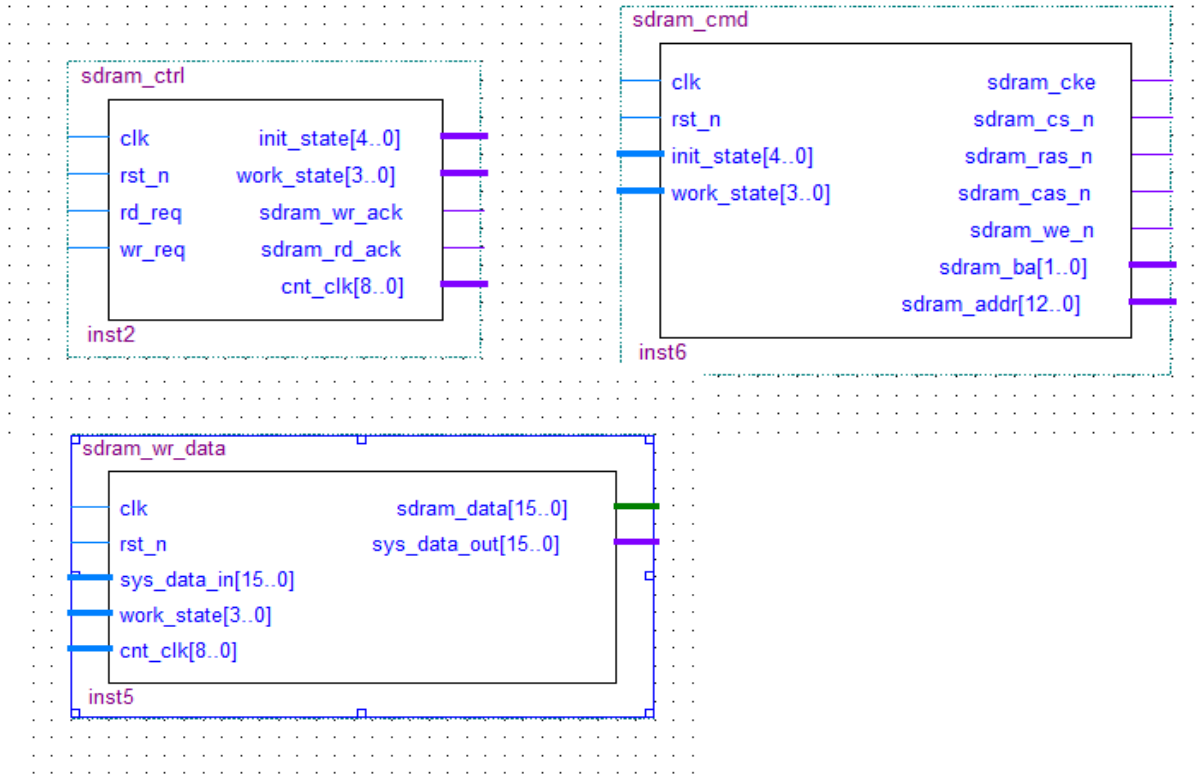
Daughter Card Design Modules

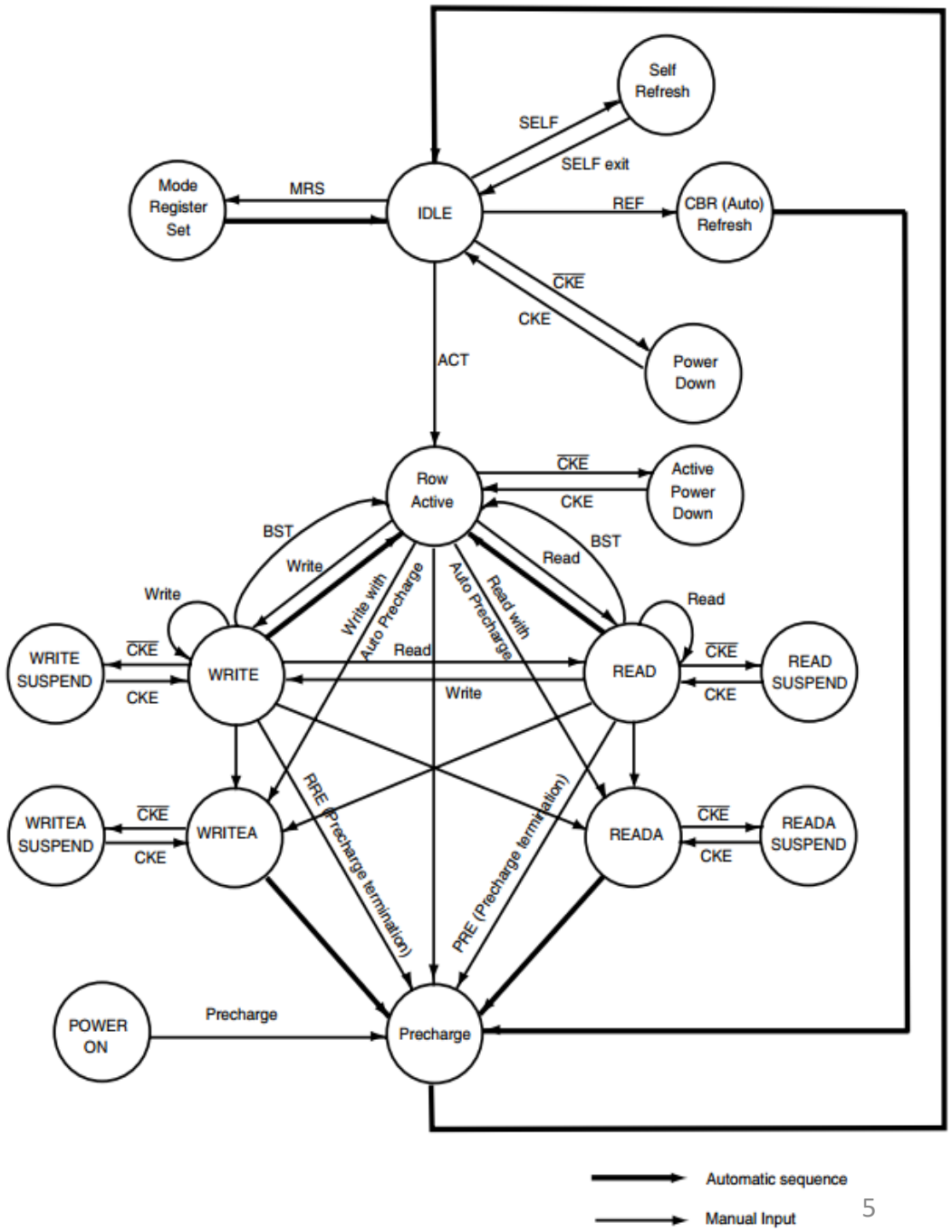
- **sys_ctrl:** Clock input from V1495, use PLL to provide clocks with phase shift, provide global reset
- **datagene:** For stand-alone simulation purpose, mimic the E/F[31:0], /OEF input from V1495
- **cache_ctrl:** FIFO as buffer, send/receive read/write request ⇔ SDRAM controller
- **sdram**: SDRAM controler



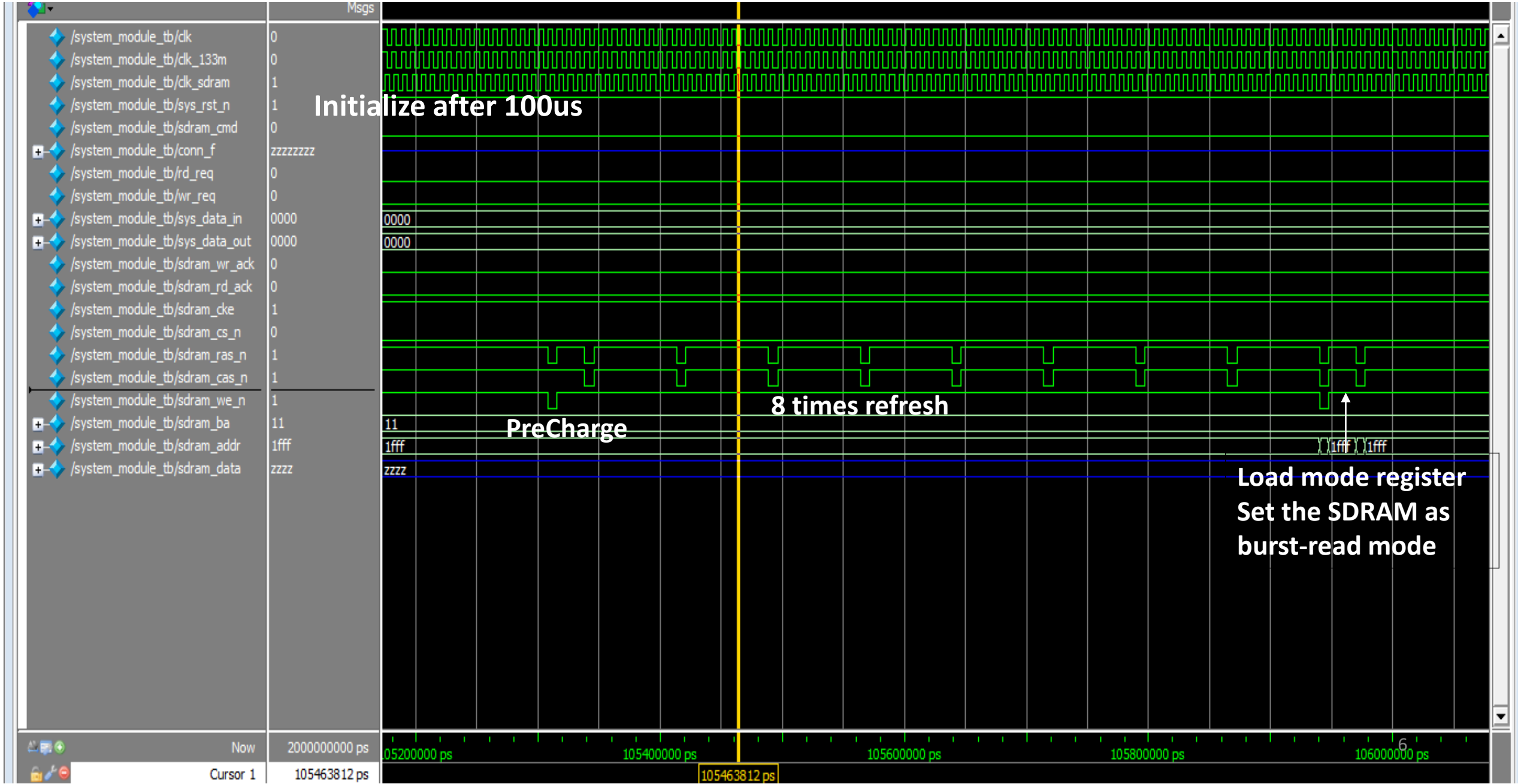
SDRAM Controller

- **sdram_ctrl:**
  SDRAM state machine for Init, Refresh, Write/Read
- **sdram_cmd:**
  Assign the command to SDRAM for each state
- **sdram_wr_data:**
  Write/Read ⇔SDRAM data bus

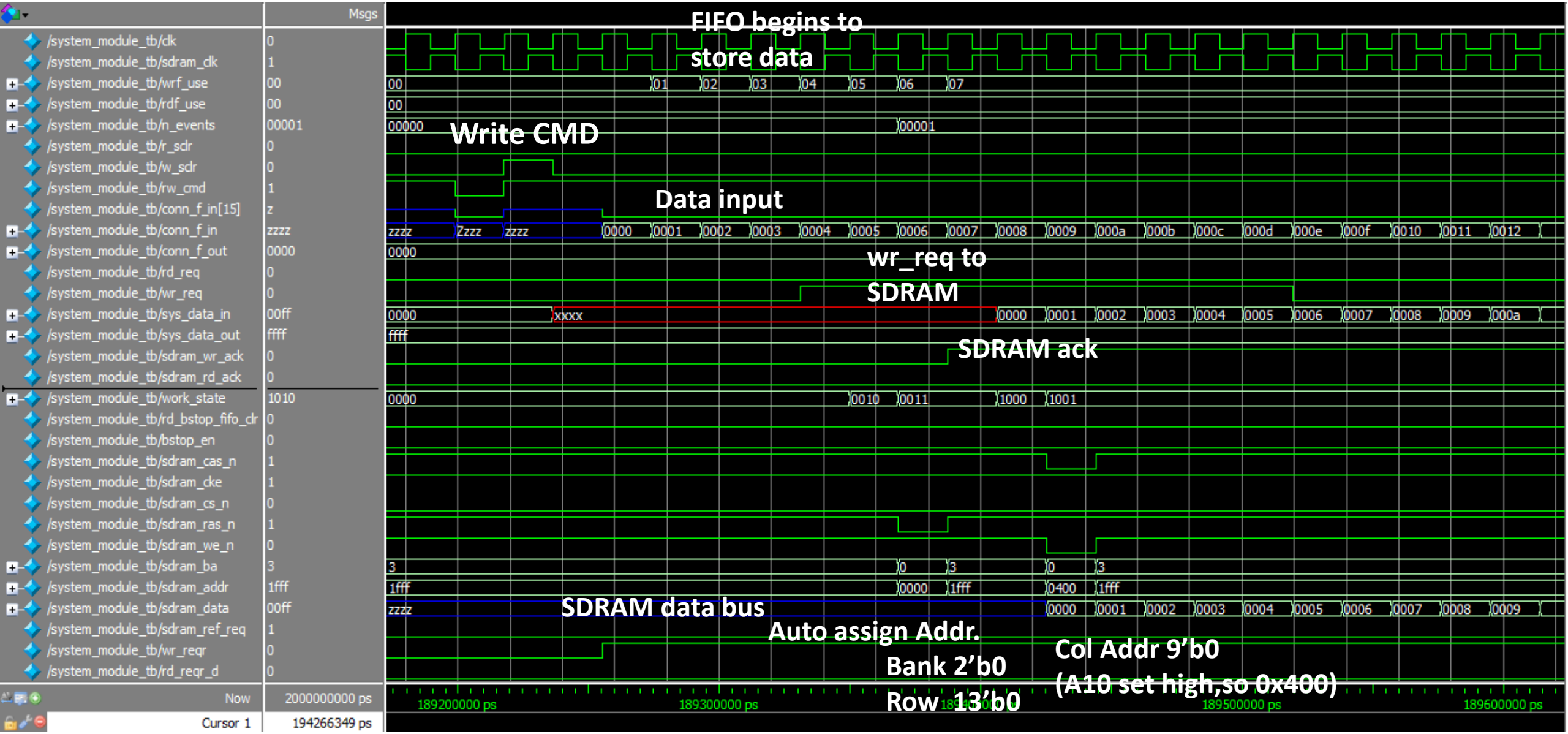




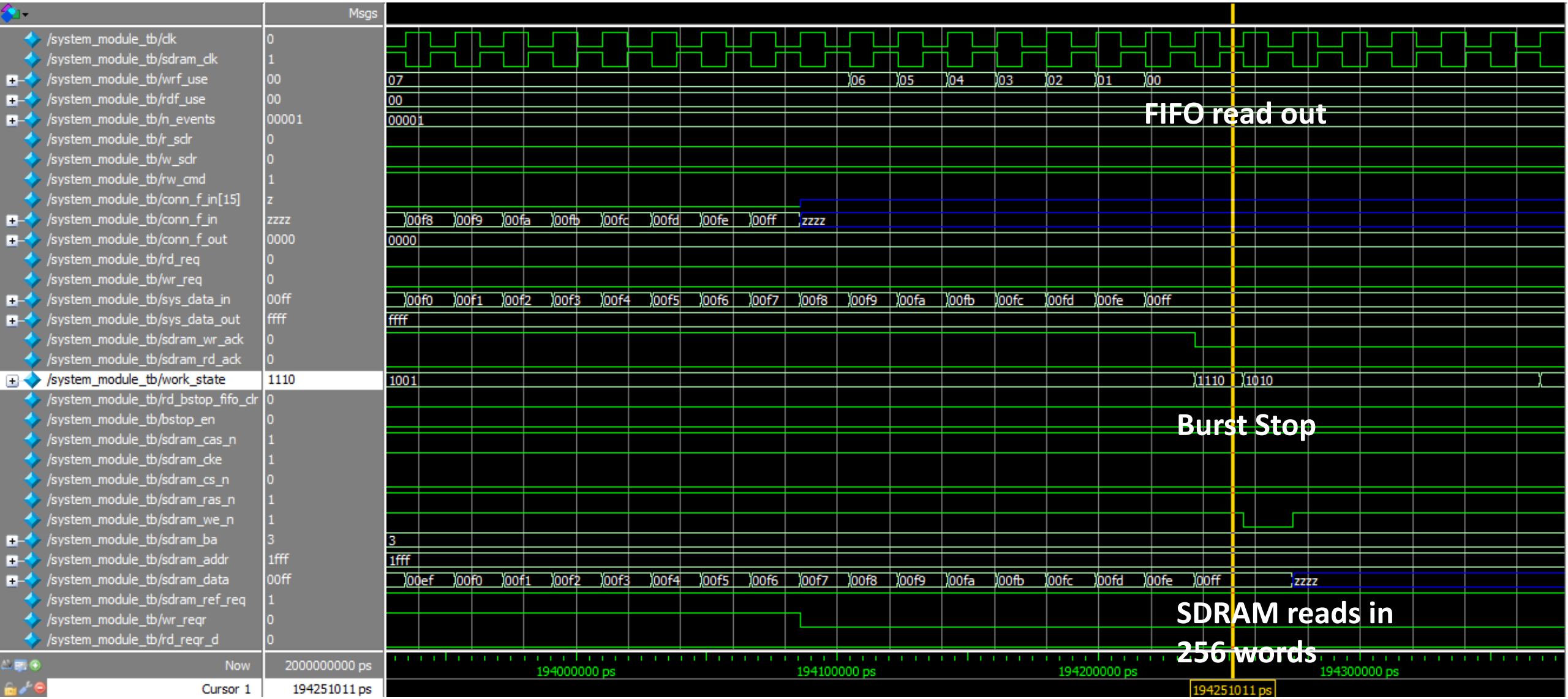
Simulation -- Initialization



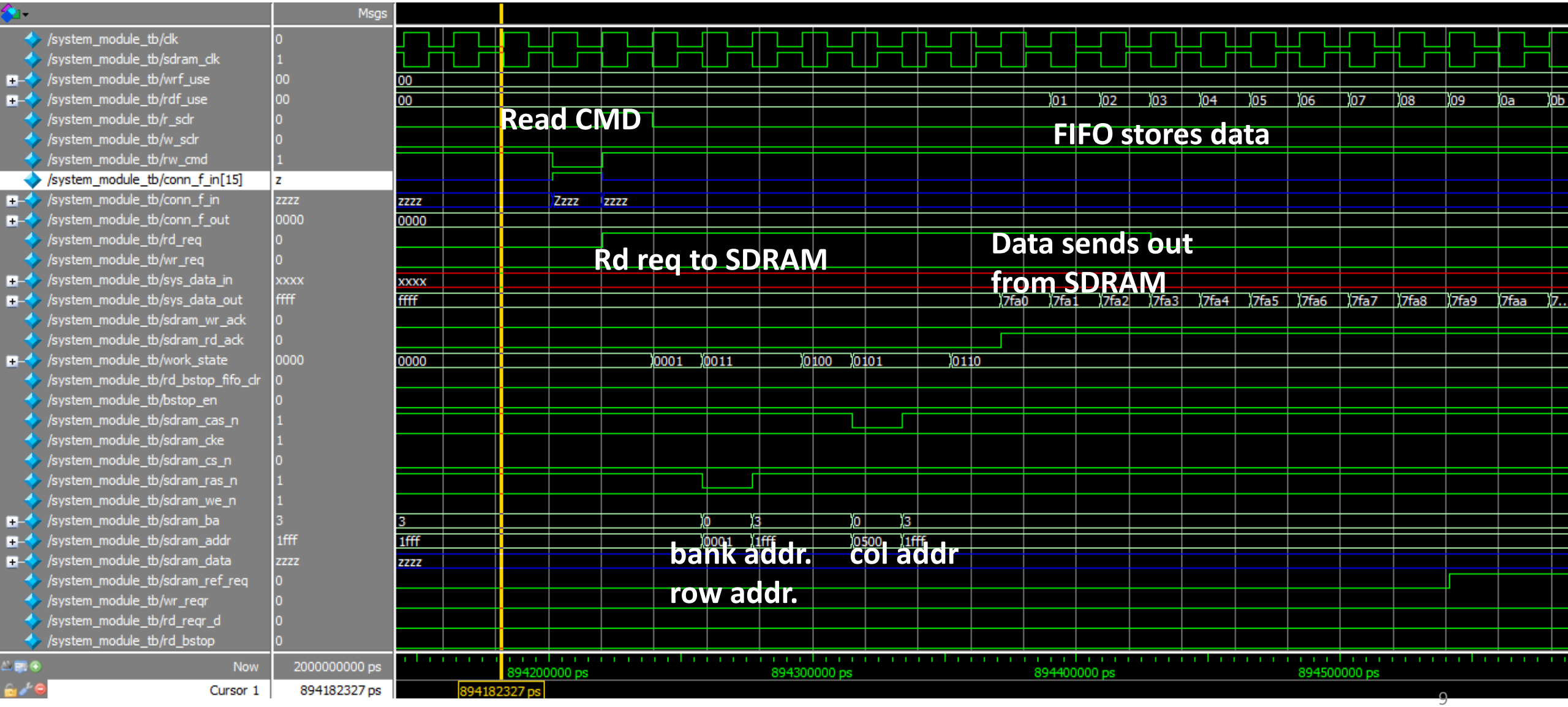
Simulation – Writing to SDRAM



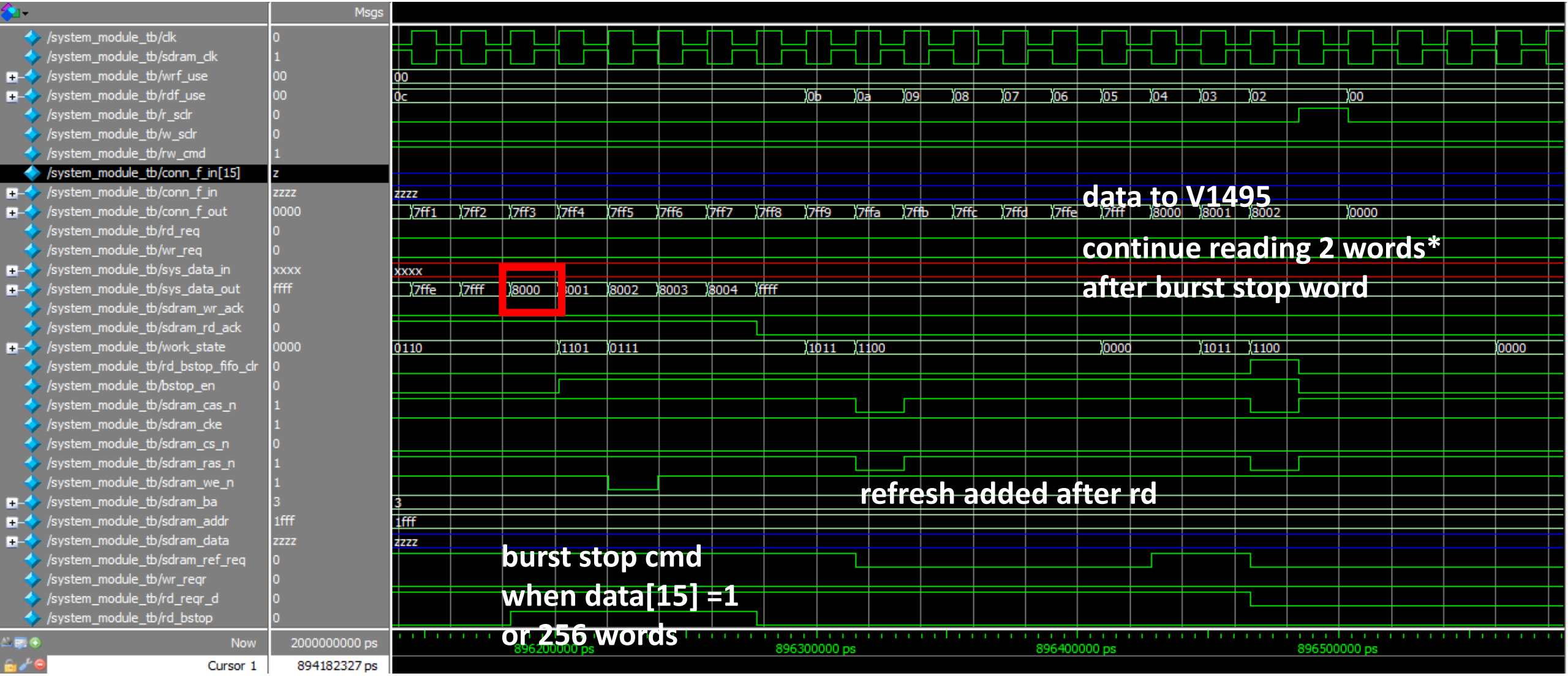
Simulation – Writing to SDRAM



Simulation – Reading from SDRAM



Simulation – Reading from SDRAM



*reserved for EVENT ID

FPGA Design on the V1495

- **BOS** Enable receiving physics trigger

- **Physics Trigger** Stop the pipeline and reads out the pipeline (unchanged)
  Fill in buffer with valid hits, header (0x8***(#no. words)), event ID
  Sending data in the buffer to the Daughter Card
  CommonStop word read (stored in ROC)
  Restarting pipeline operation

Dead time estimation:

- Pipeline readout(64 ns time window) 96(channel)*4(time slot)*20 ns ~ 8 us
- CommonStop word readout through VME bus:
  1.5 us * 2 (loop)* 2 (boards) ~ 6 us
- Restart pipeline operation: 256*20 ns ~ 5 us
- Write the EVENT ID from registers: ~ 3 us

* writing and reading one word through VME bus ~1.5us

- **EOS**

  Disable receiving physics trigger
  Read data from Daughter card into a 2048 words buffer
  (buffer is cleared before reading)
  Read next event when data[15]=1 till exactly 7 events

- **Flush Events**

  Total of ~9000 flush events
  CODA Readout from VME
  Continue Reading data from Daughter card till all events readout

Test with CODA

Test 1 Read in – Read out

Data generated @1495 FPGA -> buffer -> daughter card SDRAM-> V1495 buffer ->VME

Read in : zz01 – zzff
Read out: zz01- zzff

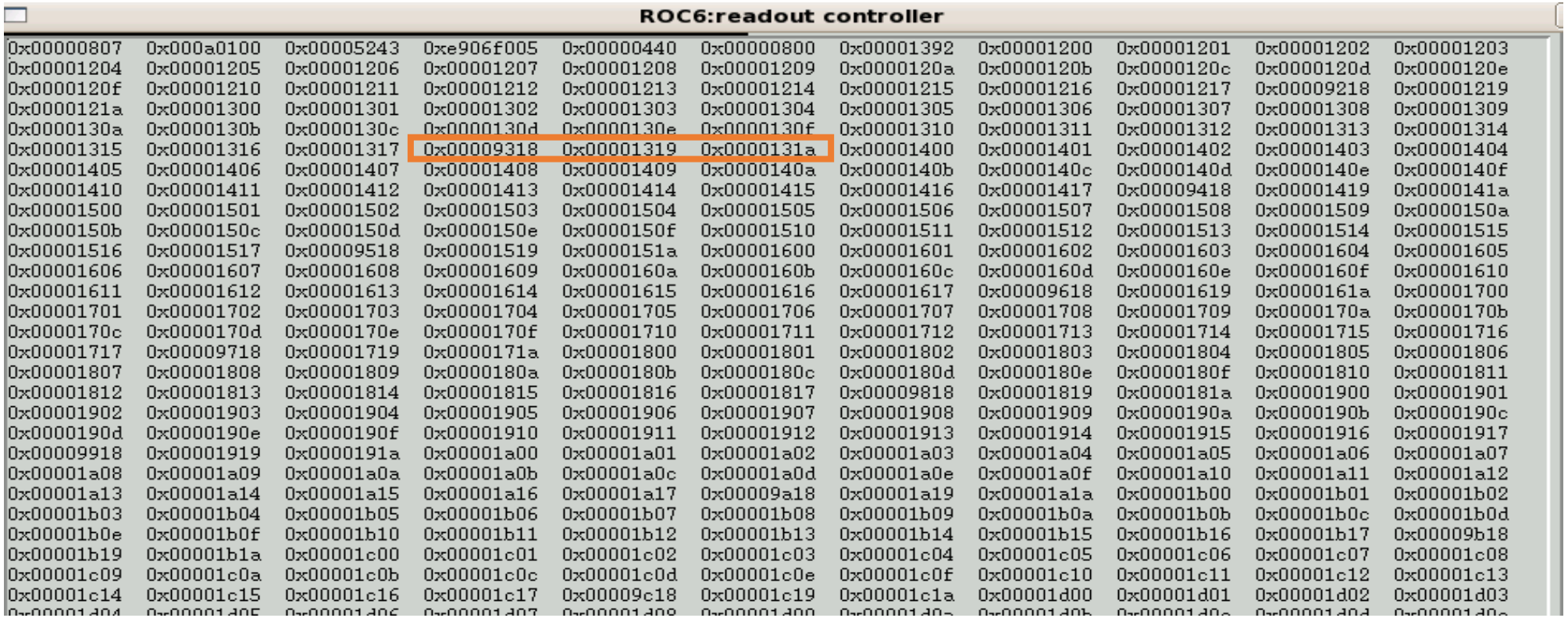
```
f0301200:  0100 0101 0102 0103 0104 0105 0106 0107   *................*
f0301210:  0108 0109 010a 010b 010c 010d 010e 010f   *................*
f0301220:  0110 0111 0112 0113 0114 0115 0116 0117   *................*
f0301230:  8118 0119 011a 011b 011c 011d 011e 011f   *................*
f0301240:  0120 0121 0122 0123 0124 0125 0126 0127   *. .!."#.$.%.&.'*
f0301250:  0128 0129 012a 012b 012c 012d 012e 012f   *.(.).*.+.,.-.../*
f0301260:  0130 0131 0132 0133 0134 0135 0136 0137   *.0.1.2.3.4.5.6.7*
f0301270:  0138 0139 013a 013b 013c 013d 013e 013f   *.8.9.:.;.<.=.>.?*
f0301280:  0140 0141 0142 0143 0144 0145 0146 0147   *.@.A.B.C.D.E.F.G*
f0301290:  0148 0149 014a 014b 014c 014d 014e 014f   *.H.I.J.K.L.M.N.O*
f03012a0:  0150 0151 0152 0153 0154 0155 0156 0157   *.P.Q.R.S.T.U.V.W*
f03012b0:  0158 0159 015a 015b 015c 015d 015e 015f   *.X.Y.Z.[.\.].^._*
f03012c0:  0160 0161 0162 0163 0164 0165 0166 0167   *.`.a.b.c.d.e.f.g*
f03012d0:  0168 0169 016a 016b 016c 016d 016e 016f   *.h.i.j.k.l.m.n.o*
f03012e0:  0170 0171 0172 0173 0174 0175 0176 0177   *.p.q.r.s.t.u.v.w*
f03012f0:  0178 0179 017a 017b 017c 017d 017e 017f   *.x.y.z.{.|.}.~..*
f0301300:  0180 0181 0182 0183 0184 0185 0186 0187   *................*
f0301310:  0188 0189 018a 018b 018c 018d 018e 018f   *................*
f0301320:  0190 0191 0192 0193 0194 0195 0196 0197   *................*
f0301330:  0198 0199 019a 019b 019c 019d 019e 019f   *................*
f0301340:  01a0 01a1 01a2 01a3 01a4 01a5 01a6 01a7   *................*
f0301350:  01a8 01a9 01aa 01ab 01ac 01ad 01ae 01af   *................*
f0301360:  01b0 01b1 01b2 01b3 01b4 01b5 01b6 01b7   *................*
f0301370:  01b8 01b9 01ba 01bb 01bc 01bd 01be 01bf   *................*
f0301380:  01c0 01c1 01c2 01c3 01c4 01c5 01c6 01c7   *................*
f0301390:  01c8 01c9 01ca 01cb 01cc 01cd 01ce 01cf   *................*
f03013a0:  01d0 01d1 01d2 01d3 01d4 01d5 01d6 01d7   *................*
f03013b0:  01d8 01d9 01da 01db 01dc 01dd 01de 01df   *................*
f03013c0:  01e0 01e1 01e2 01e3 01e4 01e5 01e6 01e7   *................*
f03013d0:  01e8 01e9 01ea 01eb 01ec 01ed 01ee 01ef   *................*
f03013e0:  01f0 01f1 01f2 01f3 01f4 01f5 01f6 01f7   *................*
f03013f0:  01f8 01f9 01fa 01fb 01fc 01fd 01fe 01ff   *................*
value = 21 = 0x15
```

Test 2 Read in – Read out

Data generate @1495 FPGA -> buffer -> daughter card SDRAM-> v1495 buffer ->VME ->CODA

Read in : zz01 – zzff zz18 highest bit set as 1

Read out: Continue reading two words(reserved for event ID) and read next event



Test 3 Production test

Data from v1495 pulser-> buffer -> daughter card SDRAM-> v1495 buffer ->VME ->CODA

→ VME ->CODA (For compare)

Read during spill(old way)

ROC6:readout controller

0x00000105	0x00020100	0x000b77b3	0xe906f005	0x00000440	0x000040ff	0x000040ef
0x000041ed	0x000040df	0x000021ca	0x000023c9	0x000025ca	0x000027c9	0x000029c9
0x00002bc9	0x00002dc8	0x00002fc7	0x000031c9	0x000033c8	0x000035c8	0x000037c8
0x000039ca	0x00003bc8	0x00003dc9	0x00003fc9	0x000040cf	0x00008115	0x00000000
0x00000000	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115
0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115	0x00008115

Read during beam-off(now)

ROC6:readout controller

0x00000805	0x000a0100	0x000b7b12	0xe906f005	0x00000440	0x000040ff	0x000040ef
0x000041ed	0x000040df	0x000021ca	0x000023c9	0x000025ca	0x000027c9	0x000029c9
0x00002bc9	0x00002dc8	0x00002fc7	0x000031c9	0x000033c8	0x000035c8	0x000037c8
0x000039ca	0x00003bc8	0x00003dc9	0x00003fc9	0x000040cf	0x00008115	0x00000000
0x00000000	0x000040ff	0x000040ef	0x000041e7	0x000040df	0x000021c4	0x000023c3
0x000025c4	0x000027c3	0x000029c3	0x00002bc3	0x00002dc2	0x00002fc1	0x000031c3
0x000033c2	0x000035c2	0x000037c2	0x000039c4	0x00003bc2	0x00003dc3	0x00003fc3
0x000040cf	0x00008115	0x00000000	0x00000001	0x000040ff	0x000040ef	0x000041e7
0x000040df	0x000021c4	0x000023c4	0x000025c4	0x000027c3	0x000029c3	0x00002bc4
0x00002dc2	0x00002fc1	0x000031c3	0x000033c3	0x000035c3	0x000037c2	0x000039c4
0x00003bc3	0x00003dc4	0x00003fc4	0x000040cf	0x00008115	0x00000000	0x00000002
0x000040ff	0x000040ef	0x000041ed	0x000040df	0x000021ca	0x000023c9	0x000025ca
0x000027c9	0x000029c9	0x00002bc9	0x00002dc8	0x00002fc7	0x000031c9	0x000033c8
0x000035c8	0x000037c8	0x000039ca	0x00003bc8	0x00003dc9	0x00003fc9	0x000040cf
0x00008115	0x00000000	0x00000003	0x000040ff	0x000040ef	0x000040df	0x000041df
0x000040cf	0x00008105	0x00000000	0x00000004	0x000040ff	0x000040ef	0x000040df
0x000041df	0x000040cf	0x00008105	0x00000000	0x00000005	0x000040ff	0x000040ef
0x000041eb	0x000040df	0x000021c9	0x000023c8	0x000025c9	0x000027c8	0x000029c8
0x00002bc8	0x00002dc7	0x00002fc6	0x000031c8	0x000033c7	0x000035c7	0x000037c7
0x000039c8	0x00003bc7	0x00003dc8	0x00003fc8	0x000040cf	0x00008115	0x00000000
0x00000006	0x000040ff	0x000040ef	0x000041e6	0x000040df	0x000021c3	0x000023c2
0x000025c3	0x000027c2	0x000029c2	0x00002bc2	0x00002dc1	0x00002fc0	0x000031c2
0x000033c1	0x000035c1	0x000037c1	0x000039c3	0x00003bc1	0x00003dc2	0x00003fc2

Test 4 Production test

Data from v1495 pulser-> buffer -> daughter card SDRAM-> v1495 buffer ->VME ->CODA

Read exactly 7 words per flush event
Trigger delay to SIS3610 set as 10us.

ROC6:readout controller

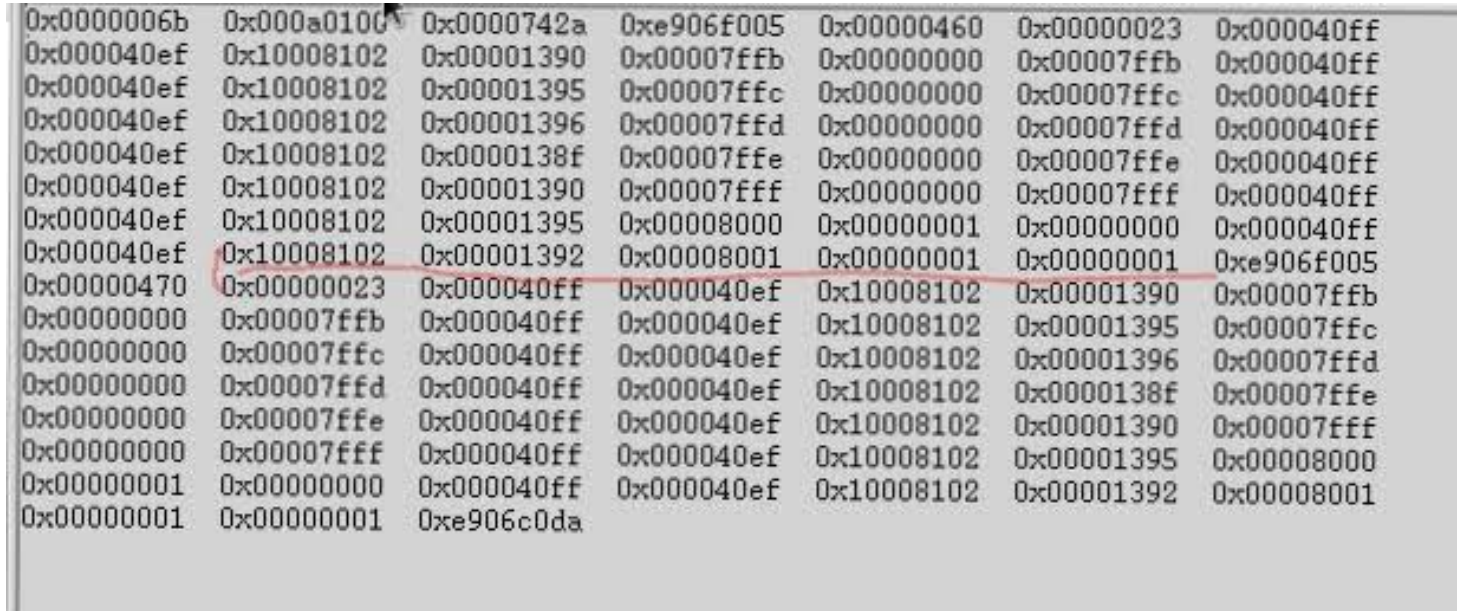
```
0x0000017b 0x000a0100 0x000c3950 0xe906f005 0x00000440 0x00000175 0x000040ff 0x000040ef 0x000041ea 0x000031da
0x000033d9 0x000035da 0x000037da 0x000039d9 0x00003bd9 0x00003dd9 0x00003fd9 0x000040df 0x000043d9 0x000045da
0x000047d7 0x000049da 0x00004bda 0x00004dda 0x00004fd9 0x000051d9 0x000053d8 0x000055d8 0x000057d8 0x000059d9
0x00005bd8 0x00005dda 0x00005fd8 0x000030c9 0x000031c1 0x000032c3 0x000033c0 0x000034c3 0x000035c1 0x000036c4
0x000037c1 0x000038c3 0x000039c0 0x00003ac2 0x00003bc0 0x00003cc3 0x00003dc0 0x00003ec4 0x00003fc0 0x000040cf
0x000042c3 0x000043c1 0x000044c1 0x000045c1 0x000046c1 0x000048c4 0x000049c1 0x00004ac3 0x00004bc1 0x00004cc3
0x00004dc1 0x00004ec2 0x00004fc0 0x000051c0 0x000052c3 0x000053c0 0x000054c3 0x000055c0 0x000056c3 0x000058c1
0x000059c0 0x00005ac5 0x00005cc4 0x00005dc1 0x00005ec2 0x00008145 0x00000000 0x00000000 0x000040ff 0x000040ef
0x000041e7 0x000030d7 0x000031d7 0x000033d7 0x000035d8 0x000037d8 0x000039d6 0x00003bd6 0x00003dd6 0x00003fd6
0x000040df 0x000043d7 0x000045d7 0x000047d4 0x000049d7 0x00004bd7 0x00004dd7 0x00004fd6 0x000051d6 0x000053d6
0x000055d6 0x000057d5 0x000059d6 0x00005bd5 0x00005dd7 0x00005fd5 0x000030c6 0x000032c1 0x000034c1 0x000036c2
0x000038c1 0x00003ac0 0x00003cc1 0x00003ec1 0x000040cf 0x000042c0 0x000048c1 0x00004ac0 0x00004cc0 0x000052c0
0x000054c1 0x000056c1 0x00005ac2 0x00005cc1 0x0000812e 0x00000000 0x00000001 0x000040ff 0x000040ef 0x000030d8
0x000040df 0x000041df 0x000031cf 0x000033ce 0x000035cf 0x000037cf 0x000039ce 0x00003bce 0x00003dce 0x00003fce
0x000040cf 0x000043cf 0x000045cf 0x000047cc 0x000049cf 0x00004bcf 0x00004dcf 0x00004fce 0x000051ce 0x000053cd
0x000055ce 0x000057cd 0x000059cd 0x00005bcd 0x00005dcf 0x00005fcd 0x0000811d 0x00000000 0x00000002 0x000040ff
0x000040ef 0x000041e6 0x000030df 0x000031d6 0x000033d6 0x000035d7 0x000037d7 0x000039d5 0x00003bd5 0x00003dd5
0x00003fd5 0x000040df 0x000043d6 0x000045d6 0x000047d3 0x000049d6 0x00004bd6 0x00004dd6 0x00004fd5 0x000051d5
0x000053d5 0x000055d5 0x000057d4 0x000059d5 0x00005bd4 0x00005dd6 0x00005fd5 0x000030c5 0x000032c0 0x000034c0
0x000036c1 0x000038c0 0x00003cc0 0x00003ec0 0x000040cf 0x000048c1 0x000054c0 0x000056c0 0x00005ac1 0x00005cc0
0x00008129 0x00000000 0x00000003 0x000040ff 0x000040ef 0x000030d8 0x000031d0 0x000035d0 0x000037d0 0x000040df
0x000041df 0x000049d0 0x000033cf 0x000039cf 0x00003bcf 0x00003dce 0x00003fcf 0x000040cf 0x000043cf 0x000045cf
0x000047cd 0x00004bcf 0x00004dcf 0x00004fcf 0x000051cf 0x000053ce 0x000055ce 0x000057ce 0x000059ce 0x00005bcd
0x00005dcf 0x00005fce 0x0000811d 0x00000000 0x00000004 0x000040ff 0x000040ef 0x000041e9 0x000031d9 0x000033d9
0x000035da 0x000037da 0x000039d9 0x00003bd8 0x00003dd8 0x00003fd8 0x000040df 0x000043d9 0x000045d9 0x000047d7
0x000049d9 0x00004bd9 0x00004dd9 0x00004fd8 0x000051d8 0x000053d8 0x000055d8 0x000057d7 0x000059d8 0x00005bd7
0x00005dd9 0x00005fd8 0x000030c9 0x000031c1 0x000032c3 0x000033c0 0x000034c3 0x000035c1 0x000036c4 0x000037c1
0x000038c3 0x000039c0 0x00003ac2 0x00003bc0 0x00003cc3 0x00003ec3 0x00003fc0 0x000040cf 0x000042c3 0x000043c0
0x000044c1 0x000045c1 0x000046c0 0x000048c4 0x000049c1 0x00004ac2 0x00004bc0 0x00004cc2 0x00004dc0 0x00004ec1
0x00004fc0 0x000051c0 0x000052c2 0x000054c3 0x000056c3 0x000058c1 0x00005ac4 0x00005cc3 0x00005dc1 0x00005ec1
0x00008141 0x00000000 0x00000005 0x000040ff 0x000040ef 0x000041eb 0x000031dc 0x000033db 0x000035dc 0x000037dc
0x000039db 0x00003bdb 0x00003dda 0x00003fdb 0x000040df 0x000043db 0x000045db 0x000047d9 0x000049dc 0x00004bdc
0x00004ddc 0x00004fdb 0x000051db 0x000053da 0x000055da 0x000057da 0x000059da 0x00005bd9 0x00005ddc 0x00005fda
0x000030cb 0x000031c3 0x000032c5 0x000033c2 0x000034c5 0x000035c3 0x000036c6 0x000037c3 0x000038c5 0x000039c2
0x00003ac4 0x00003bc2 0x00003cc5 0x00003dc2 0x00003ec6 0x00003fc2 0x000040cf 0x000042c5 0x000043c3 0x000044c3
0x000045c3 0x000046c3 0x000047c0 0x000048c6 0x000049c3 0x00004ac4 0x00004bc3 0x00004cc5 0x00004dc3 0x00004ec4
0x00004fc2 0x000051c2 0x000052c5 0x000053c1 0x000054c5 0x000055c1 0x000056c5 0x000057c1 0x000058c3 0x000059c1
0x00005ac7 0x00005bc1 0x00005cc6 0x00005dc3 0x00005ec4 0x00005fc1 0x00008149 0x00000000 0x00000006
0xe906c0da
```

Test 5 Production test

@SeaQuest
Installed at V1495 LV1 460 470
Dead time within 28us

Data Format:

0x0460	boardID
0x0023	#words in the FPGA buffer
0x40ff 0x40ef	hits
0x10008102	header
0x1392	common stop word (from CPU)
0x8001	eventID (from CPU)
0x0001	eventID higher 15 bits (from FPGA)
0x0001	eventID lower 15 bits (from FPGA)



0x0000006b	0x000a0100	0x0000742a	0xe906f005	0x00000460	0x00000023	0x000040ff
0x000040ef	0x10008102	0x00001390	0x00007ffb	0x00000000	0x00007ffb	0x000040ff
0x000040ef	0x10008102	0x00001395	0x00007ffc	0x00000000	0x00007ffc	0x000040ff
0x000040ef	0x10008102	0x00001396	0x00007ffd	0x00000000	0x00007ffd	0x000040ff
0x000040ef	0x10008102	0x0000138f	0x00007ffe	0x00000000	0x00007ffe	0x000040ff
0x000040ef	0x10008102	0x00001390	0x00007fff	0x00000000	0x00007fff	0x000040ff
0x000040ef	0x10008102	0x00001395	0x00008000	0x00000001	0x00000000	0x000040ff
0x000040ef	0x10008102	0x00001392	0x00008001	0x00000001	0x00000001	0xe906f005
0x00000470	0x00000023	0x000040ff	0x000040ef	0x10008102	0x00001390	0x00007ffb
0x00000000	0x00007ffb	0x000040ff	0x000040ef	0x10008102	0x00001395	0x00007ffc
0x00000000	0x00007ffc	0x000040ff	0x000040ef	0x10008102	0x00001396	0x00007ffd
0x00000000	0x00007ffd	0x000040ff	0x000040ef	0x10008102	0x0000138f	0x00007ffe
0x00000000	0x00007ffe	0x000040ff	0x000040ef	0x10008102	0x00001390	0x00007fff
0x00000000	0x00007fff	0x000040ff	0x000040ef	0x10008102	0x00001395	0x00008000
0x00000001	0x00000000	0x000040ff	0x000040ef	0x10008102	0x00001392	0x00008001
0x00000001	0x00000001	0xe906c0da				