

SSD1306

Advance Information

**128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CONTENTS

1 GENERAL DESCRIPTION	6
2 FEATURES.....	6
3 ORDERING INFORMATION	6
4 BLOCK DIAGRAM	7
5 DIE PAD FLOOR PLAN	8
6 PIN ARRANGEMENT.....	11
6.1 SSD1306TR1 PIN ASSIGNMENT.....	11
7 PIN DESCRIPTION	13
8 FUNCTIONAL BLOCK DESCRIPTIONS.....	15
8.1 MCU INTERFACE SELECTION.....	15
8.1.1 MCU Parallel 6800-series Interface.....	15
8.1.2 MCU Parallel 8080-series Interface.....	16
8.1.3 MCU Serial Interface (4-wire SPI).....	17
8.1.4 MCU Serial Interface (3-wire SPI).....	18
8.1.5 MCU I ² C Interface.....	19
8.2 COMMAND DECODER	22
8.3 OSCILLATOR CIRCUIT AND DISPLAY TIME GENERATOR.....	22
8.4 FR SYNCHRONIZATION	23
8.5 RESET CIRCUIT	23
8.6 SEGMENT DRIVERS / COMMON DRIVERS	24
8.7 GRAPHIC DISPLAY DATA RAM (GDDRAM).....	25
8.8 SEG/COM DRIVING BLOCK	26
8.9 POWER ON AND OFF SEQUENCE	27
9 COMMAND TABLE	28
9.1 DATA READ / WRITE	33
10 COMMAND DESCRIPTIONS	34
10.1 FUNDAMENTAL COMMAND	34
10.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)	34
10.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~1Fh)	34
10.1.3 Set Memory Addressing Mode (20h).....	34
10.1.4 Set Column Address (21h)	35
10.1.5 Set Page Address (22h).....	36
10.1.6 Set Display Start Line (40h~7Fh)	36
10.1.7 Set Contrast Control for BANK0 (81h).....	36
10.1.8 Set Segment Re-map (A0h/A1h)	36
10.1.9 Entire Display ON (A4h/A5h).....	37
10.1.10 Set Normal/Inverse Display (A6h/A7h).....	37
10.1.11 Set Multiplex Ratio (A8h).....	37
10.1.12 Set Display ON/OFF (AEh/AFh)	37
10.1.13 Set Page Start Address for Page Addressing Mode (B0h~B7h).....	37
10.1.14 Set COM Output Scan Direction (C0h/C8h).....	37
10.1.15 Set Display Offset (D3h)	37
10.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h).....	40
10.1.17 Set Pre-charge Period (D9h)	40
10.1.18 Set COM Pins Hardware Configuration (DAh)	40
10.1.19 Set V _{COMH} Deselect Level (DBh)	43

10.1.20	<i>NOP (E3h)</i>	43
10.1.21	<i>Status register Read</i>	43
10.2	GRAPHIC ACCELERATION COMMAND.....	44
10.2.1	<i>Horizontal Scroll Setup (26h/27h)</i>	44
10.2.2	<i>Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)</i>	45
10.2.3	<i>Deactivate Scroll (2Eh)</i>	46
10.2.4	<i>Activate Scroll (2Fh)</i>	46
10.2.5	<i>Set Vertical Scroll Area(A3h)</i>	46
11	MAXIMUM RATINGS.....	47
12	DC CHARACTERISTICS.....	48
13	AC CHARACTERISTICS.....	49
14	APPLICATION EXAMPLE.....	55
15	PACKAGE INFORMATION.....	56
15.1	SSD1306TR1 DETAIL DIMENSION	56
15.2	SSD1306Z DIE TRAY INFORMATION.....	58

TABLES

TABLE 5-1 : SSD1306Z BUMP DIE PAD COORDINATES.....	10
TABLE 6-1 : SSD1306TR1 PIN ASSIGNMENT TABLE.....	12
TABLE 7-1 : MCU BUS INTERFACE PIN SELECTION.....	14
TABLE 8-1 : MCU INTERFACE ASSIGNMENT UNDER DIFFERENT BUS INTERFACE MODE	15
TABLE 8-2 : CONTROL PINS OF 6800 INTERFACE.....	15
TABLE 8-3 : CONTROL PINS OF 8080 INTERFACE.....	17
TABLE 8-4 : CONTROL PINS OF 4-WIRE SERIAL INTERFACE.....	17
TABLE 8-5 : CONTROL PINS OF 3-WIRE SERIAL INTERFACE.....	18
TABLE 9-1: COMMAND TABLE	28
TABLE 9-2 : READ COMMAND TABLE.....	33
TABLE 9-3 : ADDRESS INCREMENT TABLE (AUTOMATIC)	33
TABLE 10-1 : EXAMPLE OF SET DISPLAY OFFSET AND DISPLAY START LINE WITH NO REMAP.....	38
TABLE 10-2 :EXAMPLE OF SET DISPLAY OFFSET AND DISPLAY START LINE WITH REMAP	39
TABLE 10-3 : COM PINS HARDWARE CONFIGURATION	40
TABLE 11-1 : MAXIMUM RATINGS (VOLTAGE REFERENCED TO VSS).....	47
TABLE 12-1 : DC CHARACTERISTICS.....	48
TABLE 13-1 : AC CHARACTERISTICS.....	49
TABLE 13-2 : 6800-SERIES MCU PARALLEL INTERFACE TIMING CHARACTERISTICS.....	50
TABLE 13-3 : 8080-SERIES MCU PARALLEL INTERFACE TIMING CHARACTERISTICS.....	51
TABLE 13-4 : 4-WIRE SERIAL INTERFACE TIMING CHARACTERISTICS	52
TABLE 13-5 : 3-WIRE SERIAL INTERFACE TIMING CHARACTERISTICS	53
TABLE 13-6 :I ² C INTERFACE TIMING CHARACTERISTICS.....	54

FIGURES

FIGURE 4-1 SSD1306 BLOCK DIAGRAM	7
FIGURE 5-1 : SSD1306Z DIE DRAWING	8
FIGURE 5-2 : SSD1306Z ALIGNMENT MARK DIMENSIONS	9
FIGURE 6-1 : SSD1306TR1 PIN ASSIGNMENT	11
FIGURE 7-1 PIN DESCRIPTION	13
FIGURE 8-1 : DATA READ BACK PROCEDURE - INSERTION OF DUMMY READ	16
FIGURE 8-2 : EXAMPLE OF WRITE PROCEDURE IN 8080 PARALLEL INTERFACE MODE.....	16
FIGURE 8-3 : EXAMPLE OF READ PROCEDURE IN 8080 PARALLEL INTERFACE MODE	16
FIGURE 8-4 : DISPLAY DATA READ BACK PROCEDURE - INSERTION OF DUMMY READ	17
FIGURE 8-5 : WRITE PROCEDURE IN 4-WIRE SERIAL INTERFACE MODE.....	18
FIGURE 8-6 : WRITE PROCEDURE IN 3-WIRE SERIAL INTERFACE MODE.....	18
FIGURE 8-7 : I^2C -BUS DATA FORMAT	20
FIGURE 8-8 : DEFINITION OF THE START AND STOP CONDITION	21
FIGURE 8-9 : DEFINITION OF THE ACKNOWLEDGEMENT CONDITION	21
FIGURE 8-10 : DEFINITION OF THE DATA TRANSFER CONDITION	21
FIGURE 8-11 : OSCILLATOR CIRCUIT AND DISPLAY TIME GENERATOR	22
FIGURE 8-12 : SEGMENT OUTPUT WAVEFORM IN THREE PHASES	24
FIGURE 8-13 : GDDRAM PAGES STRUCTURE OF SSD1306.....	25
FIGURE 8-14 : ENLARGEMENT OF GDDRAM (NO ROW RE-MAPPING AND COLUMN-REMAPPING).....	25
FIGURE 8-15 : I_{REF} CURRENT SETTING BY RESISTOR VALUE	26
FIGURE 8-16 : THE POWER ON SEQUENCE.....	27
FIGURE 8-17 : THE POWER OFF SEQUENCE	27
FIGURE 10-1 : ADDRESS POINTER MOVEMENT OF PAGE ADDRESSING MODE	34
FIGURE 10-2 : EXAMPLE OF GDDRAM ACCESS POINTER SETTING IN PAGE ADDRESSING MODE (NO ROW AND COLUMN-REMAPPING)	34
FIGURE 10-3 : ADDRESS POINTER MOVEMENT OF HORIZONTAL ADDRESSING MODE	35
FIGURE 10-4 : ADDRESS POINTER MOVEMENT OF VERTICAL ADDRESSING MODE	35
FIGURE 10-5 : EXAMPLE OF COLUMN AND ROW ADDRESS POINTER MOVEMENT	36
FIGURE 10-6 : TRANSITION BETWEEN DIFFERENT MODES	37
FIGURE 10-7 : HORIZONTAL SCROLL EXAMPLE: SCROLL RIGHT BY 1 COLUMN.....	44
FIGURE 10-8 : HORIZONTAL SCROLL EXAMPLE: SCROLL LEFT BY 1 COLUMN	44
FIGURE 10-9 : HORIZONTAL SCROLLING SETUP EXAMPLE.....	44
FIGURE 10-10 : CONTINUOUS VERTICAL AND HORIZONTAL SCROLLING SETUP EXAMPLE.....	45
FIGURE 13-1 : 6800-SERIES MCU PARALLEL INTERFACE CHARACTERISTICS.....	50
FIGURE 13-2 : 8080-SERIES PARALLEL INTERFACE CHARACTERISTICS.....	51
FIGURE 13-3 : 4-WIRE SERIAL INTERFACE CHARACTERISTICS.....	52
FIGURE 13-4 : 3-WIRE SERIAL INTERFACE CHARACTERISTICS.....	53
FIGURE 13-5 : I^2C INTERFACE TIMING CHARACTERISTICS.....	54
FIGURE 14-1 : APPLICATION EXAMPLE OF SSD1306Z	55
FIGURE 15-1 SSD1306TR1 DETAIL DIMENSION	56
FIGURE 15-2 : SSD1306Z DIE TRAY INFORMATION	58

1 GENERAL DESCRIPTION

SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1306 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface, I²C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
 - V_{DD} = 1.65V to 3.3V for IC logic
 - V_{CC} = 7V to 15V for Panel driving
- For matrix display
 - OLED driving output voltage, 15V maximum
 - Segment maximum source current: 100uA
 - Common maximum sink current: 15mA
 - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
 - 8-bit 6800/8080-series parallel interface
 - 3 /4 wire Serial Peripheral Interface
 - I²C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG & COF
- Wide range of operating temperature: -40°C to 85°C

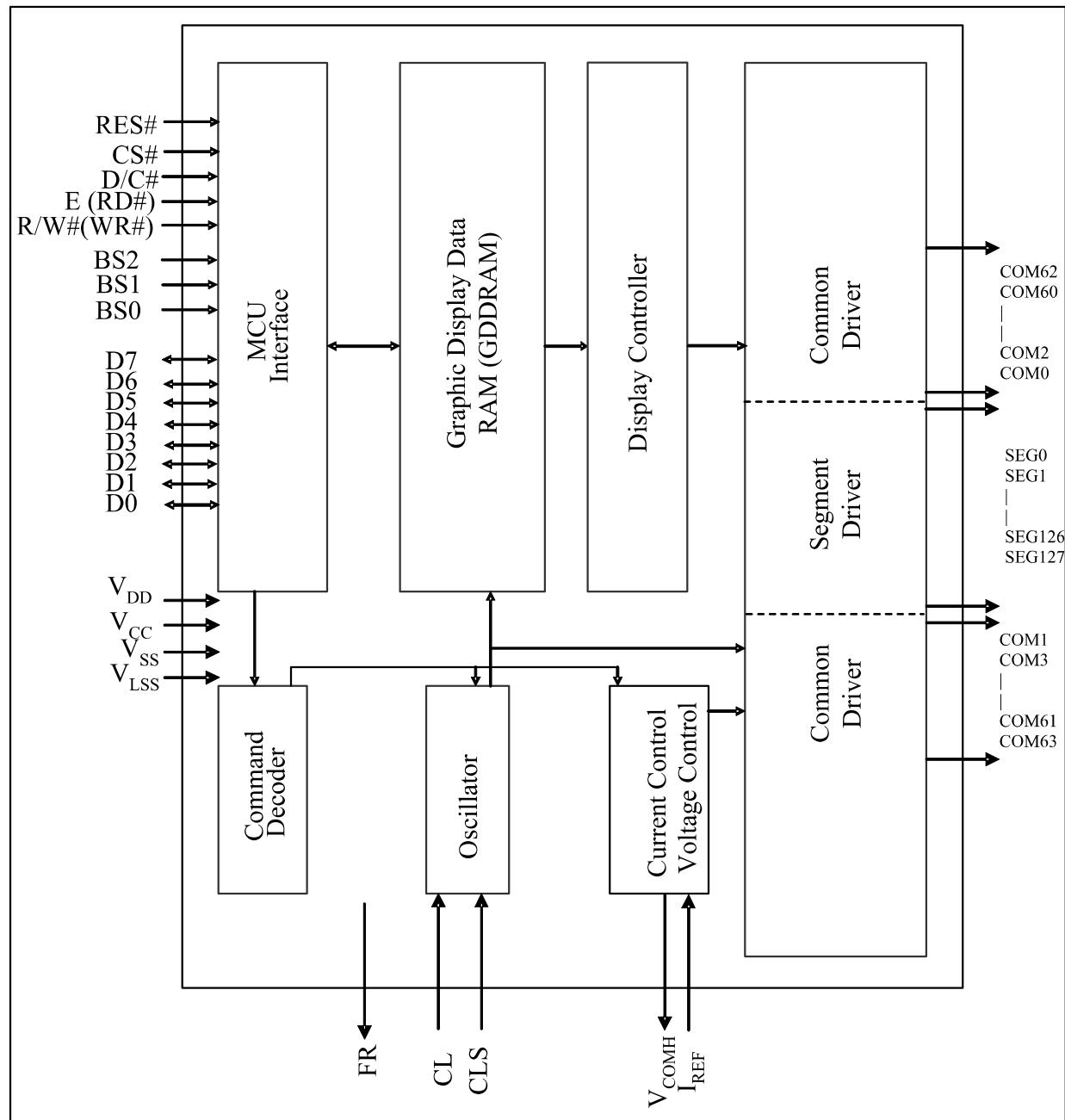
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1306Z	128	64	COG	8	<ul style="list-style-type: none">○ Min SEG pad pitch : 47um○ Min COM pad pitch : 40um○ Die thickness: 300 +/- 25um
SSD1306TR1	104	48	TAB	11, 56	<ul style="list-style-type: none">○ 35mm film, 4 sprocket hole, Folding TAB○ 8-bit 80 / 8-bit 68 / SPI / I²C interface○ SEG, COM lead pitch 0.1mm x 0.997 =0.0997mm○ Die thickness: 457 +/- 25um

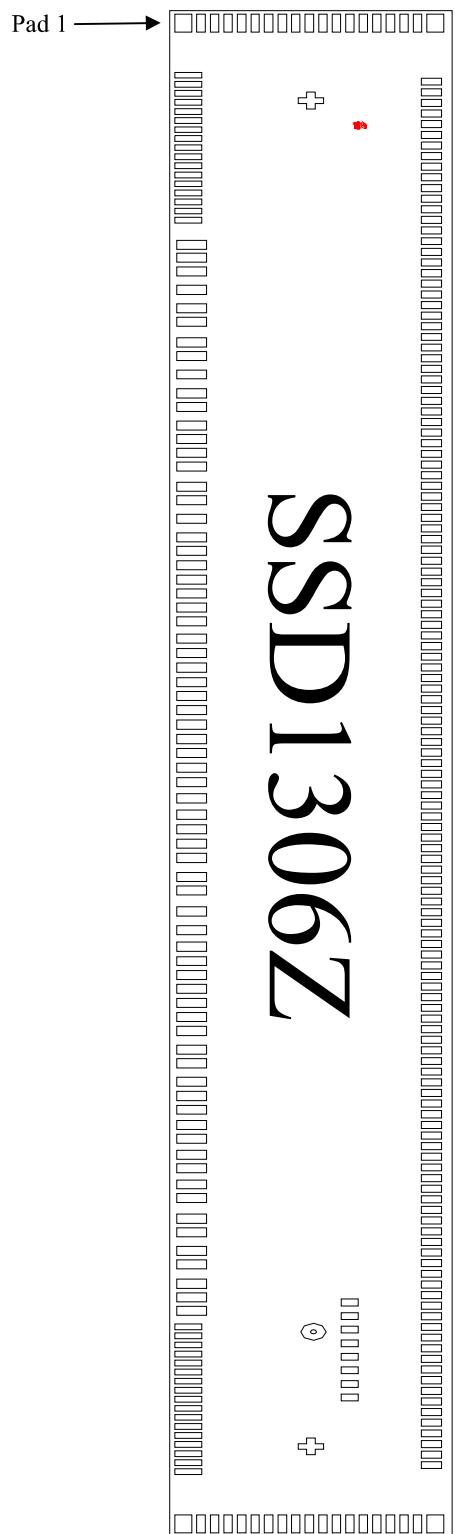
4 BLOCK DIAGRAM

Figure 4-1 SSD1306 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1306Z Die Drawing



Die size	6.76mm x 0.86mm
Die thickness	300 +/- 25um
Min I/O pad pitch	60um
Min SEG pad pitch	47um
Min COM pad pitch	40um
Bump height	Nominal 15um

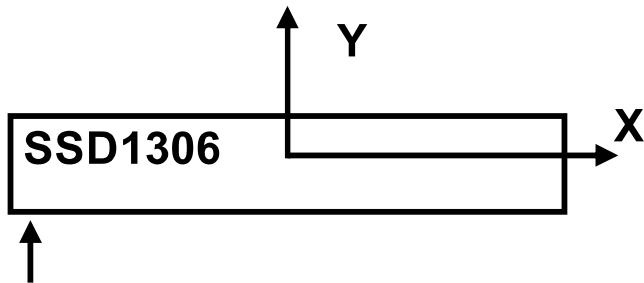
Bump size	
Pad 1, 106, 124, 256	80um x 50um
Pad 2-18, 89-105, 107-123, 257-273	25um x 80um
Pad 19-88	40um x 89um
Pad 125-255	31um x 59um
Pad 274-281 (TR pads)	30um x 50um

Alignment mark	Position	Size
+	(-2973, 0)	75um x 75um
+	(2973, 0)	75um x 75um
Circle	(2466.665, 7.575)	R37.5um, inner 18um
SSL Logo	(-2862.35, 144.82)	-

(For details dimension please see p.9)

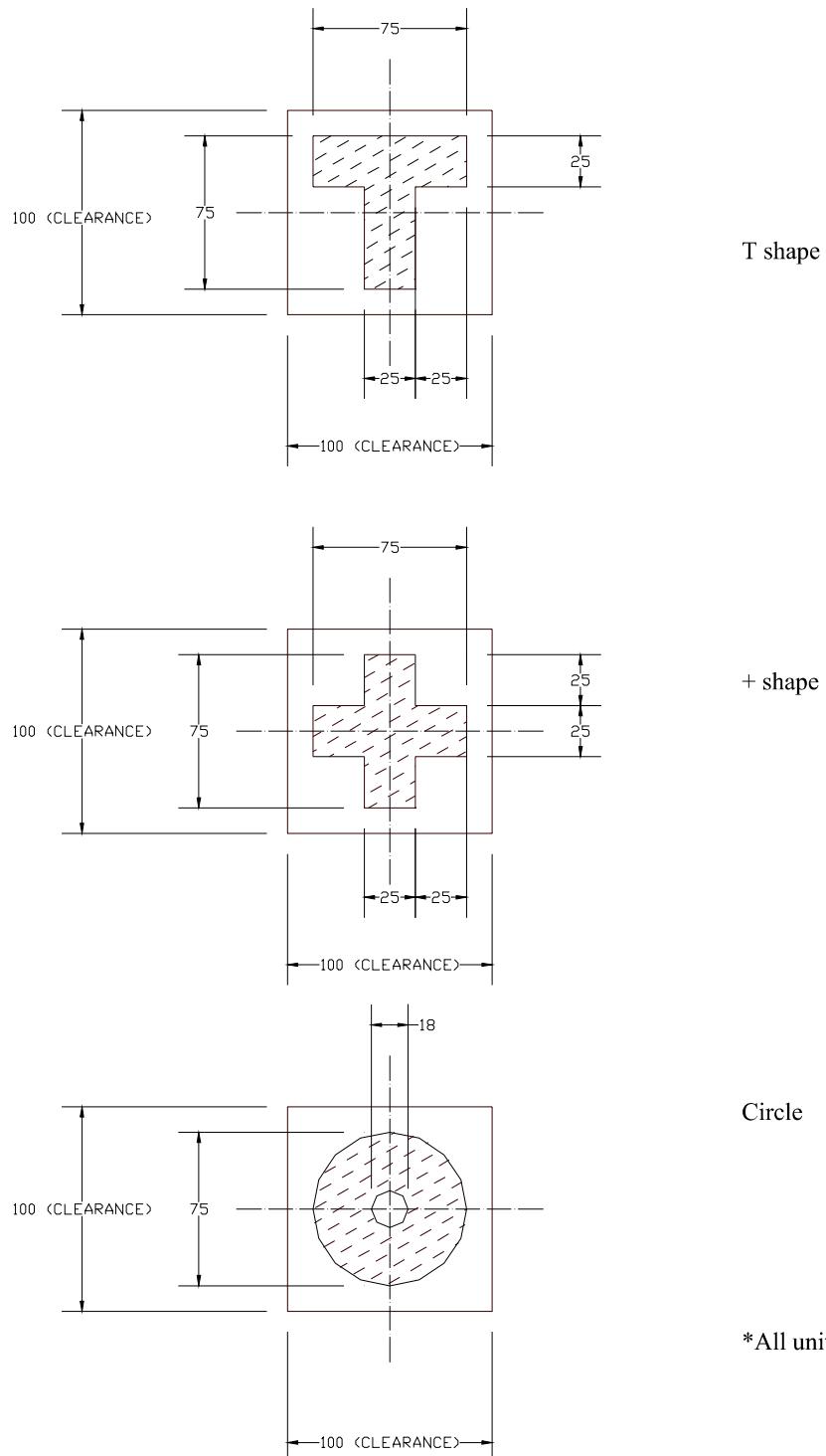
Note

- ⁽¹⁾ Diagram showing the Gold bumps face up.
- ⁽²⁾ Coordinates are referenced to center of the chip.
- ⁽³⁾ Coordinate units and size of all alignment marks are in um.
- ⁽⁴⁾ All alignment keys do not contain gold



Pad 1,2,3,...>281
Gold Bumps face up

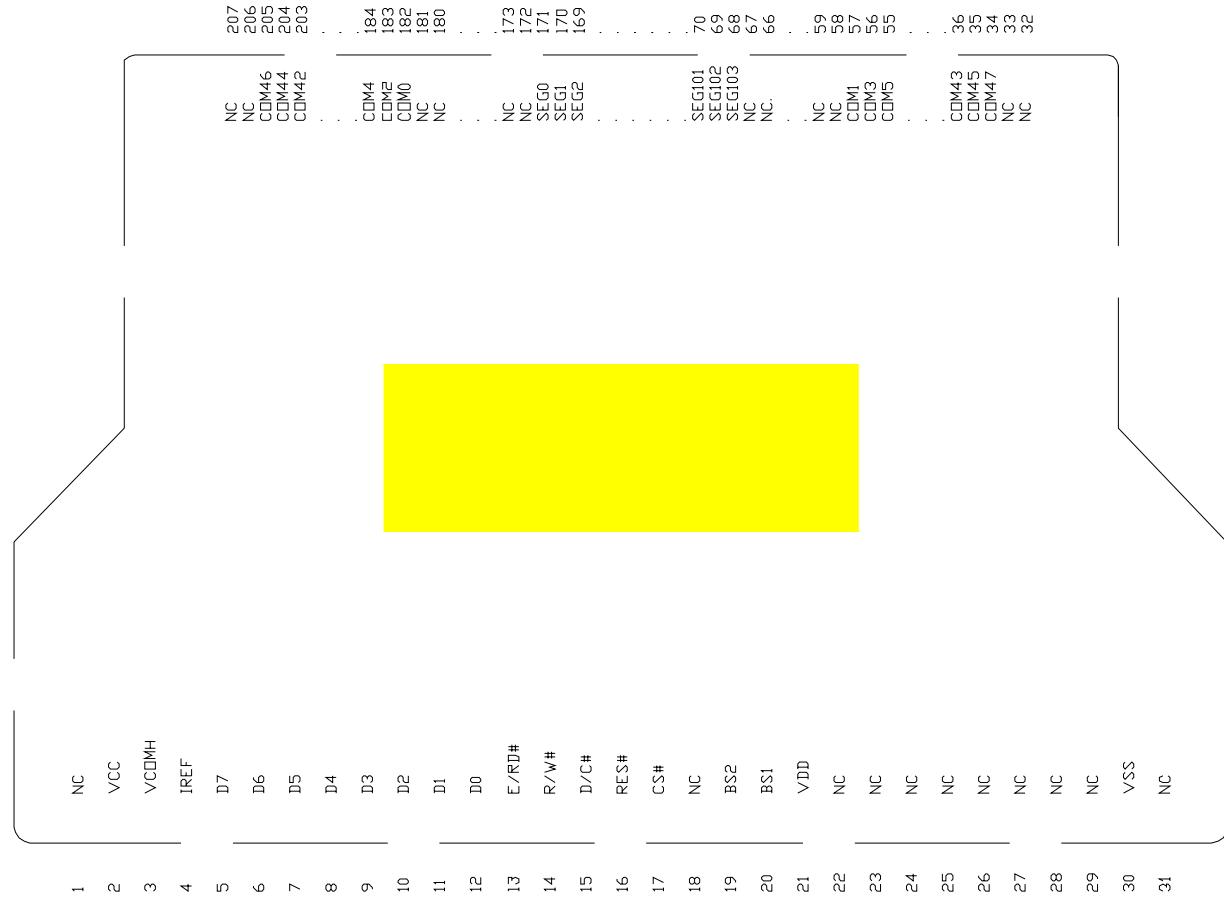
Figure 5-2 : SSD1306Z alignment mark dimensions



6 PIN ARRANGEMENT

6.1 SSD1306TR1 pin assignment

Figure 6-1 : SSD1306TR1 Pin Assignment



Note:

⁽¹⁾ COM sequence (Split) is under command setting: DAh, 12h

Table 6-1 : SSD1306TR1 Pin Assignment Table

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	81	SEG90	161	SEG10
2	VCC	82	SEG89	162	SEG9
3	VCOMH	83	SEG88	163	SEG8
4	IREF	84	SEG87	164	SEG7
5	D7	85	SEG86	165	SEG6
6	D6	86	SEG85	166	SEG5
7	D5	87	SEG84	167	SEG4
8	D4	88	SEG83	168	SEG3
9	D3	89	SEG82	169	SEG2
10	D2	90	SEG81	170	SEG1
11	D1	91	SEG80	171	SEG0
12	D0	92	SEG79	172	NC
13	E/RD#	93	SEG78	173	NC
14	R/W#	94	SEG77	174	NC
15	D/C#	95	SEG76	175	NC
16	RES#	96	SEG75	176	NC
17	CS#	97	SEG74	177	NC
18	NC	98	SEG73	178	NC
19	BS2	99	SEG72	179	NC
20	BS1	100	SEG71	180	NC
21	VDD	101	SEG70	181	NC
22	NC	102	SEG69	182	COM0
23	NC	103	SEG68	183	COM2
24	NC	104	SEG67	184	COM4
25	NC	105	SEG66	185	COM6
26	NC	106	SEG65	186	COM8
27	NC	107	SEG64	187	COM10
28	NC	108	SEG63	188	COM12
29	NC	109	SEG62	189	COM14
30	VSS	110	SEG61	190	COM16
31	NC	111	SEG60	191	COM18
32	NC	112	SEG59	192	COM20
33	NC	113	SEG58	193	COM22
34	COM47	114	SEG57	194	COM24
35	COM45	115	SEG56	195	COM26
36	COM43	116	SEG55	196	COM28
37	COM41	117	SEG54	197	COM30
38	COM39	118	SEG53	198	COM32
39	COM37	119	SEG52	199	COM34
40	COM35	120	SEG51	200	COM36
41	COM33	121	SEG50	201	COM38
42	COM31	122	SEG49	202	COM40
43	COM29	123	SEG48	203	COM42
44	COM27	124	SEG47	204	COM44
45	COM25	125	SEG46	205	COM46
46	COM23	126	SEG45	206	NC
47	COM21	127	SEG44	207	NC
48	COM19	128	SEG43		
49	COM17	129	SEG42		
50	COM15	130	SEG41		
51	COM13	131	SEG40		
52	COM11	132	SEG39		
53	COM9	133	SEG38		
54	COM7	134	SEG37		
55	COM5	135	SEG36		
56	COM3	136	SEG35		
57	COM1	137	SEG34		
58	NC	138	SEG33		
59	NC	139	SEG32		
60	NC	140	SEG31		
61	NC	141	SEG30		
62	NC	142	SEG29		
63	NC	143	SEG28		
64	NC	144	SEG27		
65	NC	145	SEG26		
66	NC	146	SEG25		
67	NC	147	SEG24		
68	SEG103	148	SEG23		
69	SEG102	149	SEG22		
70	SEG101	150	SEG21		
71	SEG100	151	SEG20		
72	SEG99	152	SEG19		
73	SEG98	153	SEG18		
74	SEG97	154	SEG17		
75	SEG96	155	SEG16		
76	SEG95	156	SEG15		
77	SEG94	157	SEG14		
78	SEG93	158	SEG13		
79	SEG92	159	SEG12		
80	SEG91	160	SEG11		

7 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O = Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V _{DD}
P = Power pin	

Figure 7-1 Pin Description

Pin Name	Type	Description
V _{DD}	P	Power supply pin for core logic operation.
V _{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V _{SS}	P	This is a ground pin.
V _{LSS}	P	This is an analog ground pin. It should be connected to V _{SS} externally.
V _{COMH}	O	The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and V _{SS} .
V _{BAT}	P	Reserved pin. It should be connected to V _{DD} .
BGGND	P	Reserved pin. It should be connected to ground.
C1P/C1N C2P/C2N	I	Reserved pin. It should be kept NC.
V _{BREF}	P	Reserved pin. It should be kept NC.
BS[2:0]	I	MCU bus interface selection pins. Please refer to Table 7-1 for the details of setting.
I _{REF}	I	This is segment output current reference pin. A resistor should be connected between this pin and V _{SS} to maintain the I _{REF} current at 12.5 uA. Please refer to Figure 8-15 for the details of resistor value.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Please refer to Section 8.4 for details usage.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V _{SS} . When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V _{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V _{DD}) during normal operation.
CS#	I	This pin is the chip select input. (active LOW).

Pin Name	Type	Description
D/C#	I	<p>This is Data/Command control pin. When it is pulled HIGH (i.e. connect to V_{DD}), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register.</p> <p>In I²C mode, this pin acts as SA0 for slave address selection.</p> <p>When 3-wire serial interface is selected, this pin must be connected to V_{SS}.</p> <p>For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams: Figure 13-1 to Figure 13-5.</p>
E (RD#)	I	<p>When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V_{DD}) and the chip is selected.</p> <p>When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.</p> <p>When serial or I²C interface is selected, this pin must be connected to V_{SS}.</p>
R/W#(WR#)	I	<p>This is read / write control input pin connecting to the MCU interface.</p> <p>When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V_{DD}) and write mode when LOW.</p> <p>When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.</p> <p>When serial or I²C interface is selected, this pin must be connected to V_{SS}.</p>
D[7:0]	IO	<p>These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.</p> <p>When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.</p> <p>When I²C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.</p>
TR0-TR6	-	Testing reserved pins. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide Segment switch signals to OLED panel. These pins are V _{SS} state when display is OFF.
COM0 ~ COM63	O	These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.
NC	-	This is dummy pin. Do not group or short NC pins together.

Table 7-1 : MCU Bus Interface Pin Selection

SSD1306 Pin Name	I ² C Interface	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0	0	0	1
BS1	1	0	1	0	0
BS2	0	1	1	0	0

Note

⁽¹⁾ 0 is connected to V_{SS}

⁽²⁾ 1 is connected to V_{DD}

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface selection

SSD1306 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-1 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW		NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW		RES#		
4-wire SPI	Tie LOW		NC	SDIN	SCLK	Tie LOW		CS#	D/C#		RES#		
I ² C	Tie LOW		SDA _{OUT}	SDA _{IN}	SCL	Tie LOW			SA0		RES#		

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 8-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note

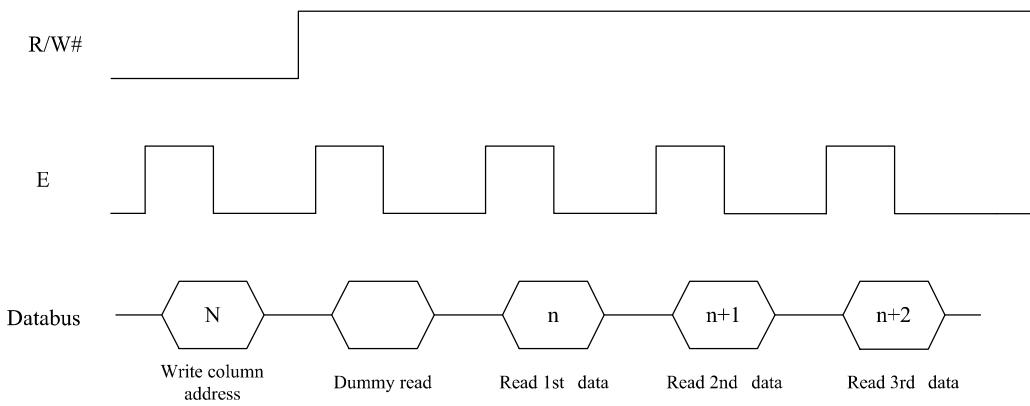
⁽¹⁾ ↓ stands for falling edge of signal

H stands for HIGH in signal

L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

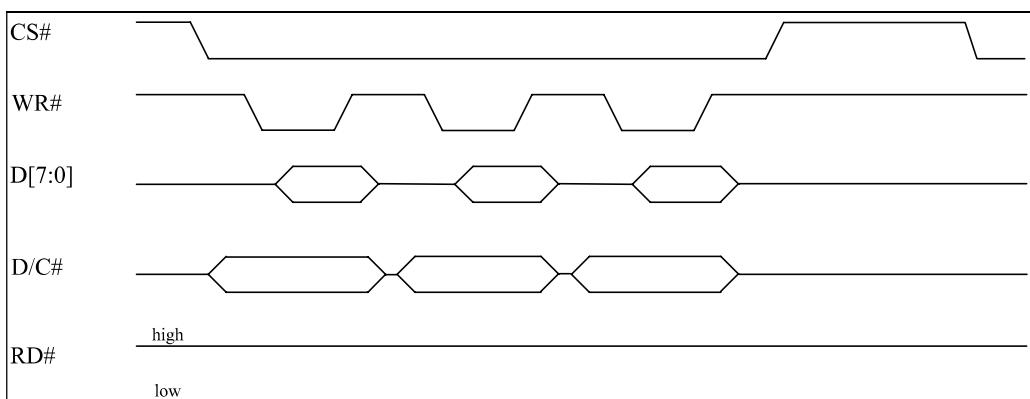


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

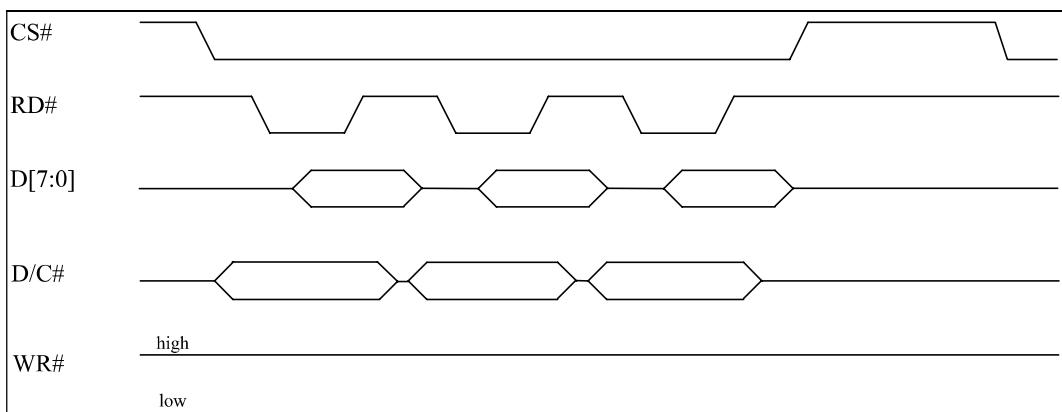


Table 8-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note

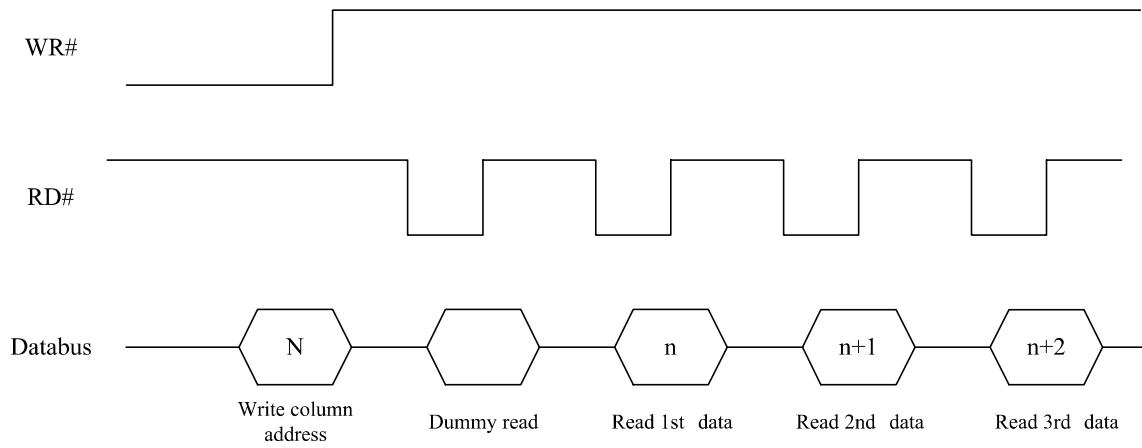
⁽¹⁾ ↑ stands for rising edge of signal

⁽²⁾ H stands for HIGH in signal

⁽³⁾ L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W#(WR#)# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note

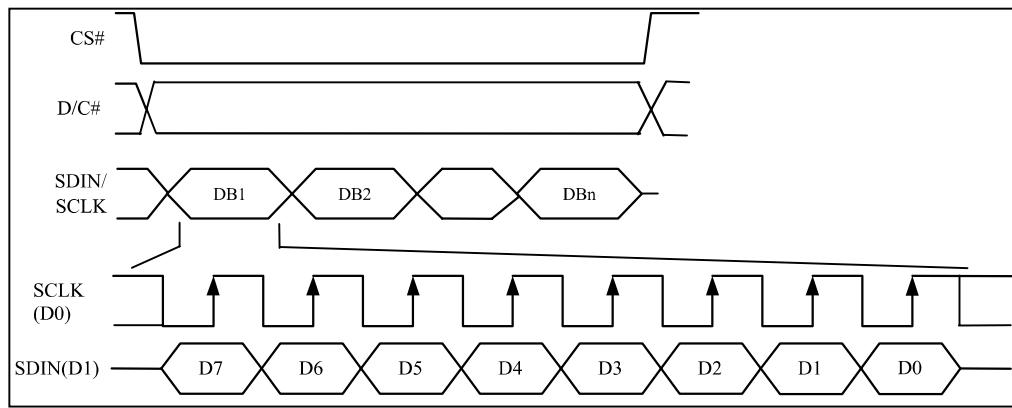
⁽¹⁾ H stands for HIGH in signal

⁽²⁾ L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

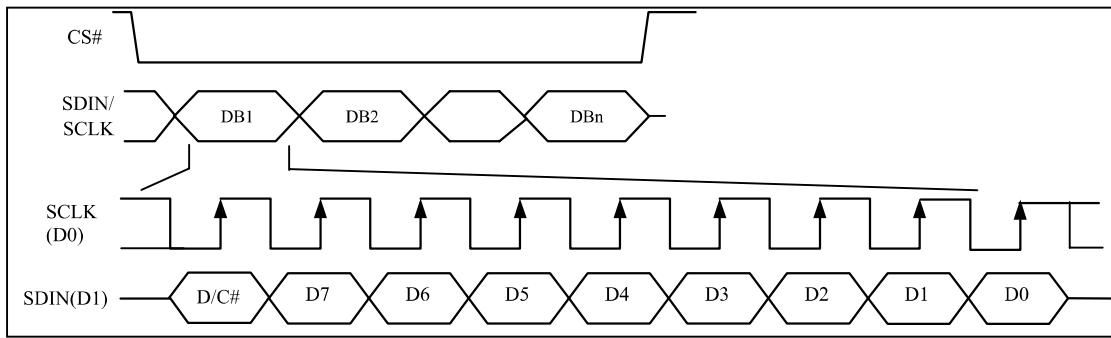
The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#) #, E and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0	Note
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑	(¹) L stands for LOW in signal
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑	

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D₂ for output and SDA_{IN}/D₁ for input) and I²C-bus clock signal SCL (D₀). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)

SSD1306 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

b₇ b₆ b₅ b₄ b₃ b₂ b₁ b₀
0 1 1 1 1 0 SA0 R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, can be selected as the slave address of SSD1306. D/C# pin acts as SA0 for slave address selection.

“R/W#” bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.

“SDA_{IN}” and “SDA_{OUT}” are tied together and serve as SDA. The “SDA_{IN}” pin must be connected to act as SDA. The “SDA_{OUT}” pin may be disconnected. When “SDA_{OUT}” pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

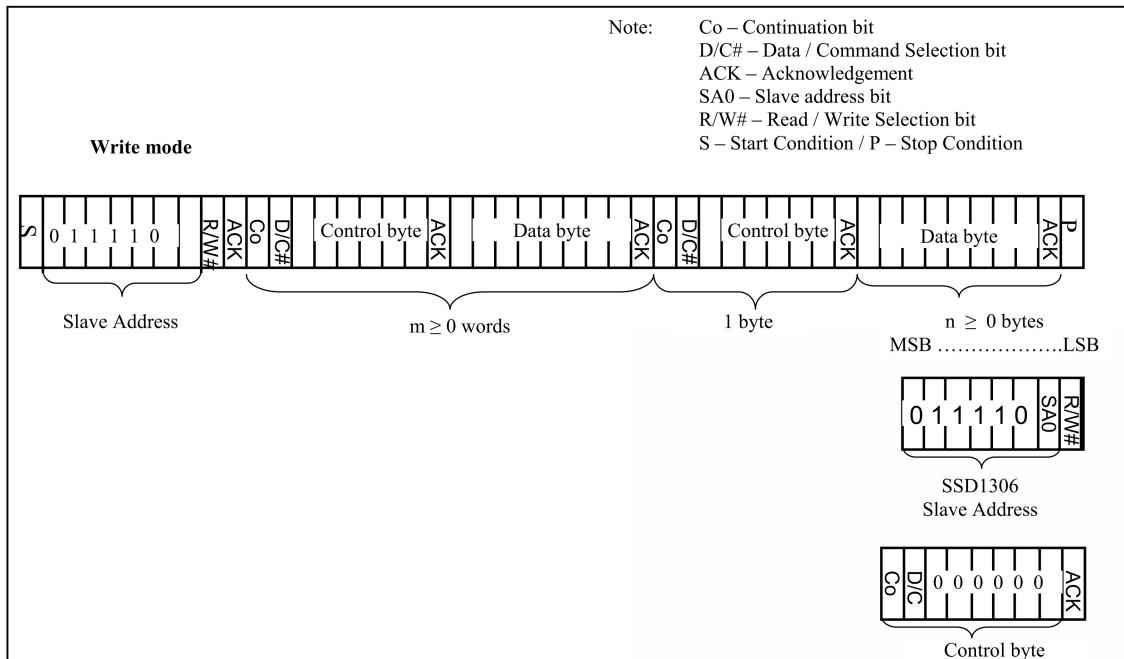
c) I²C-bus clock signal (SCL)

The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I²C-bus in chronological order.

Figure 8-7 : I²C-bus data format



8.1.5.2 Write mode for I²C

- 1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
- 2) The slave address is following the start condition for recognition use. For the SSD1306, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
- 3) The write mode is established by setting the R/W# bit to logic “0”.
- 4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
- 5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
 - a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
 - b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
- 6) Acknowledge bit will be generated after receiving each control byte or data byte.
- 7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 8-8 : Definition of the Start and Stop Condition

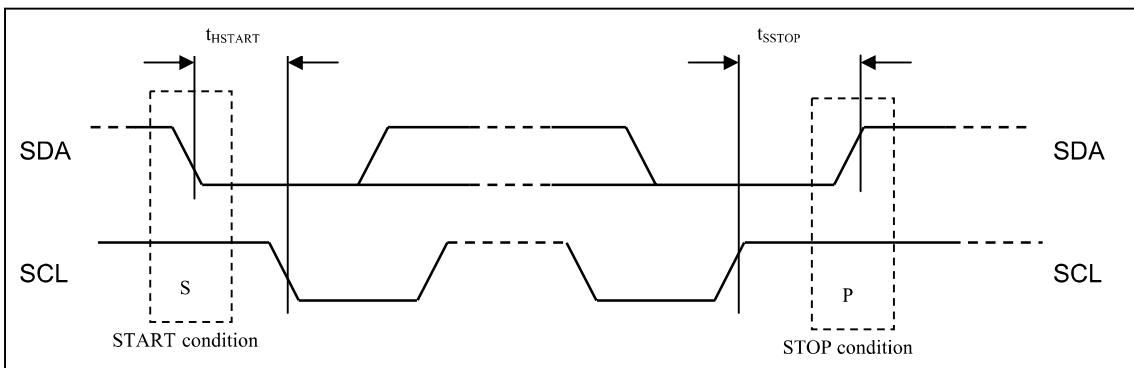
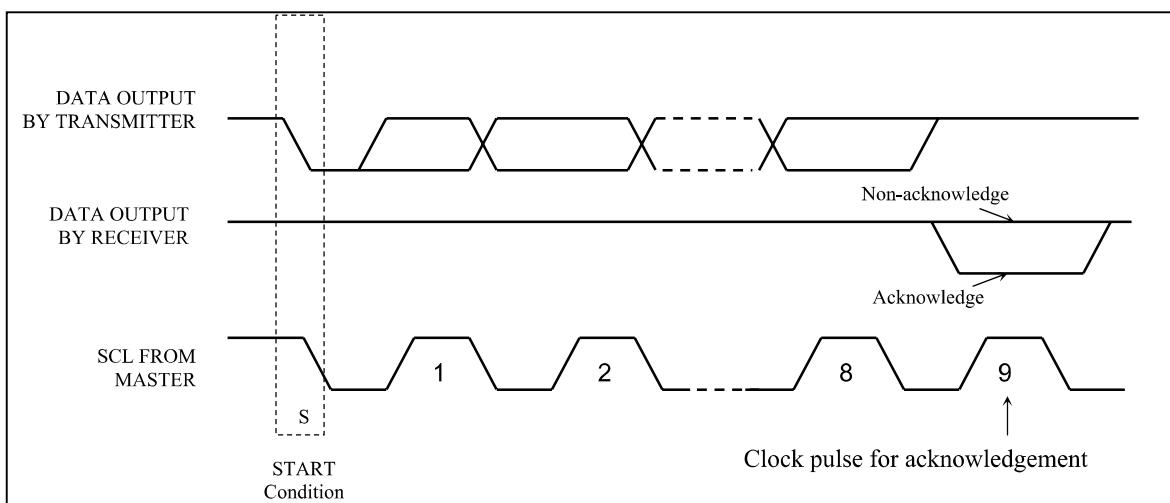


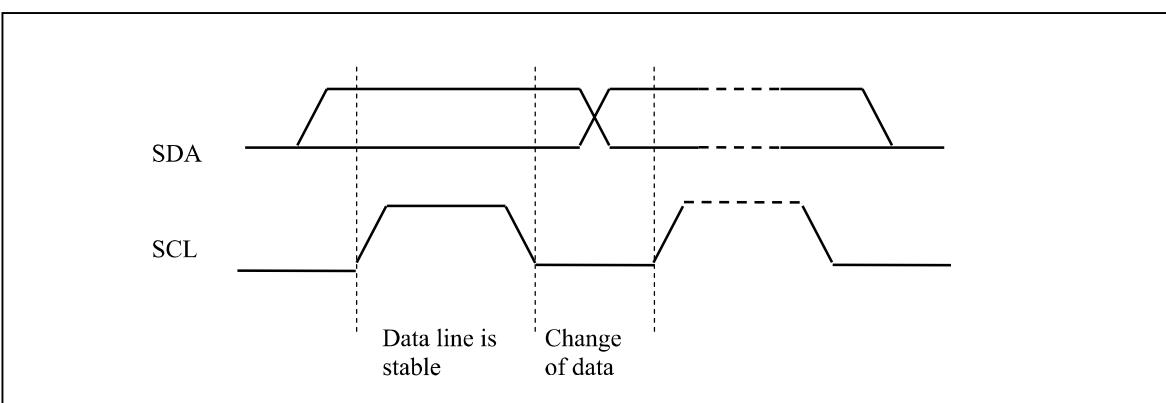
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8-10 : Definition of the data transfer condition



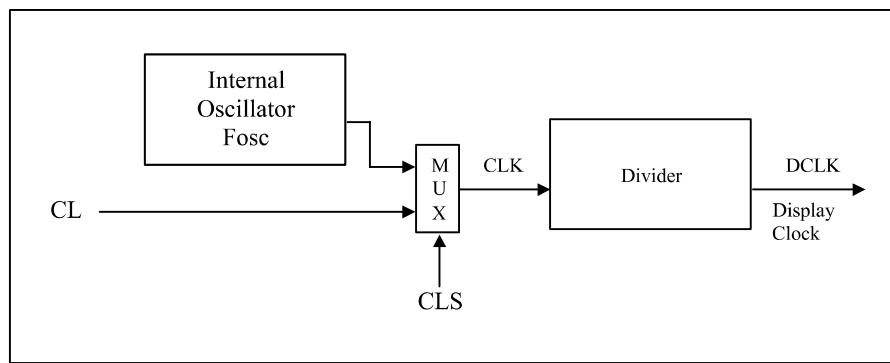
8.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be left open. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

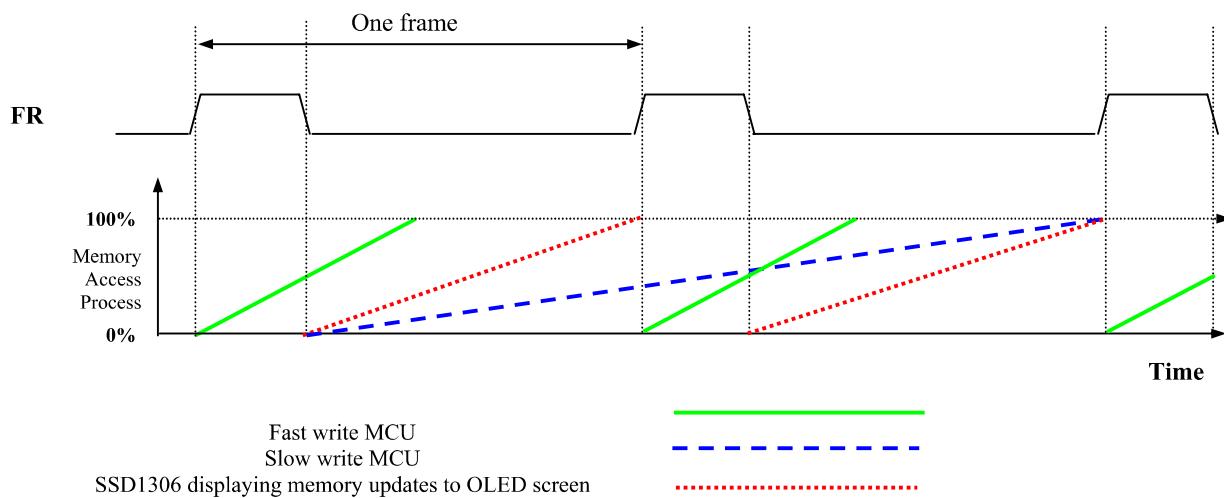
- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by

$$K = \text{Phase 1 period} + \text{Phase 2 period} + \text{BANK0 pulse width}$$

$$= 2 + 2 + 50 = 54 \text{ at power on reset}$$
 (Please refer to Section 8.6 “Segment Drivers / Common Drivers” for the details of the “Phase”)
- Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64MUX).
- Fosc is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

8.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

8.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

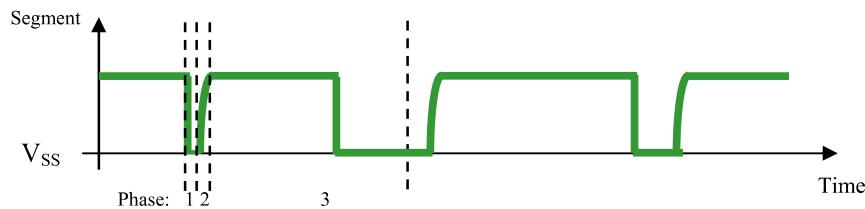
8.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 100uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS} . The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 8-12 : Segment Output Waveform in three phases



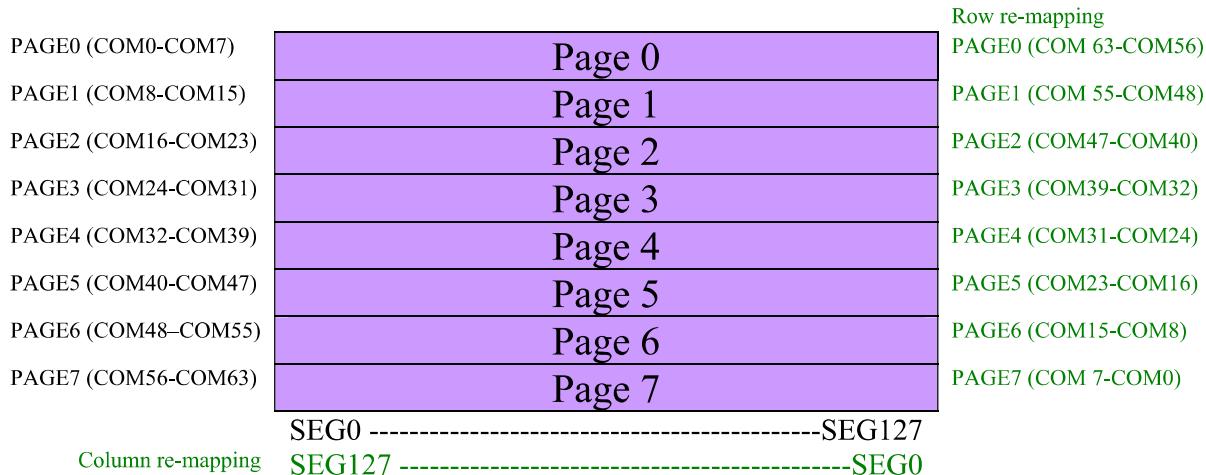
After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 50, after finishing 50 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

8.7 Graphic Display Data RAM (GDDRAM)

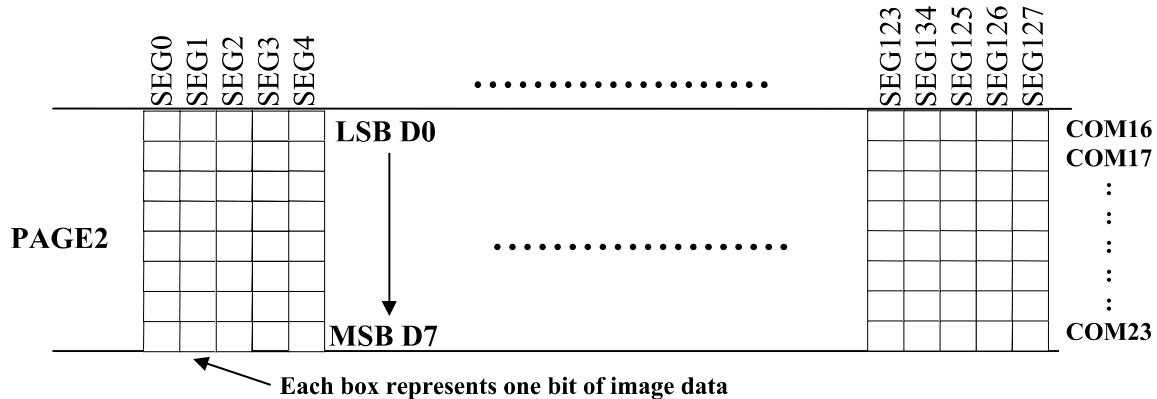
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Figure 8-13 : GDDRAM pages structure of SSD1306



When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

8.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG} . The relationship between reference current and segment current of a color is:

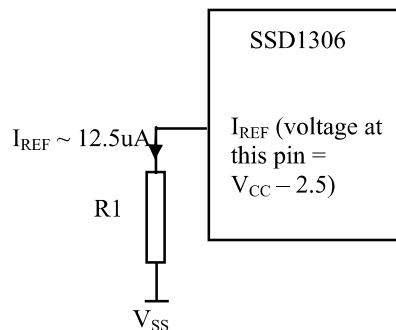
$$I_{SEG} = \text{Contrast} / 256 \times I_{REF} \times \text{scale factor}$$

in which

the contrast (0~255) is set by Set Contrast command 81h; and
the scale factor is 8 by default.

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 8-15. It is recommended to set I_{REF} to $12.5 \pm 2\mu A$ so as to achieve $I_{SEG} = 100\mu A$ at maximum contrast 255.

Figure 8-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is $V_{CC} - 2.5V$, the value of resistor R1 can be found as below:

For $I_{REF} = 12.5\mu A$, $V_{CC} = 12V$:

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &= (12 - 2.5) / 12.5\mu A \\ &= 760K\Omega \end{aligned}$$

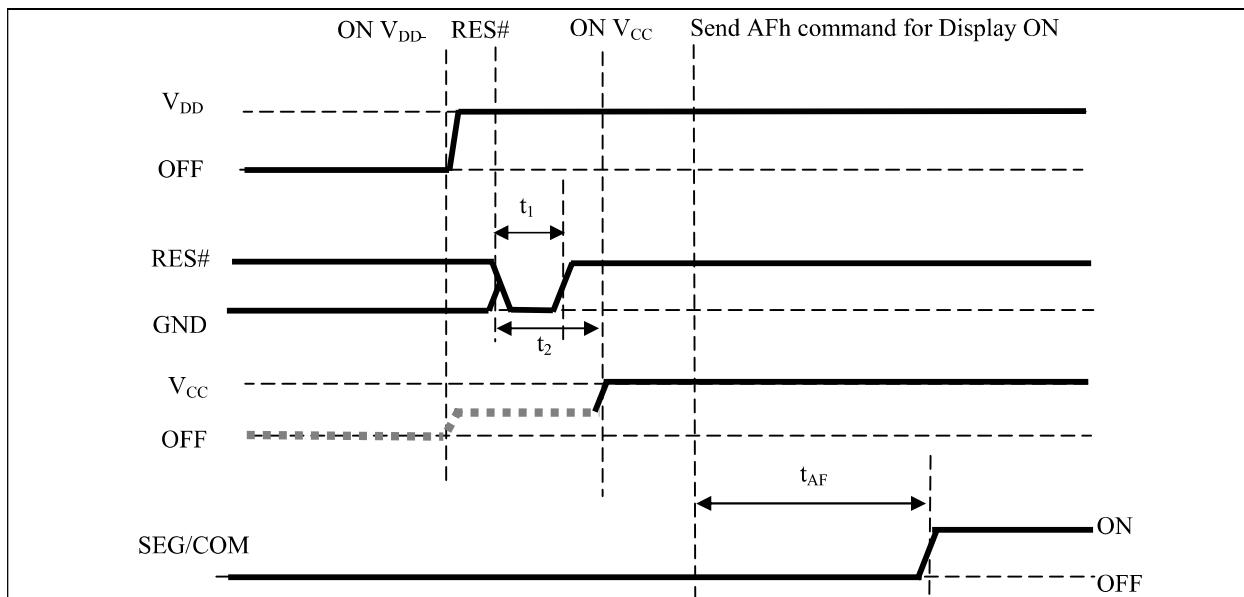
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1306

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) ⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

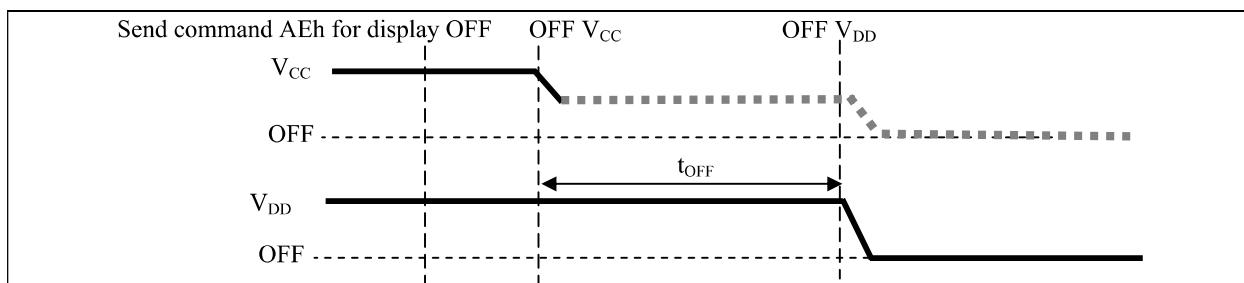
Figure 8-16 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.^{(1), (2), (3)}
3. Power OFF V_{DD} after t_{OFF} .⁽⁵⁾ (Typical $t_{OFF}=100ms$)

Figure 8-17 : The Power OFF sequence



Note:

- (1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-16 and Figure 8-17.
- (2) V_{CC} should be kept float (i.e. disable) when it is OFF.
- (3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
- (4) The register values are reset after t_1 .
- (5) V_{DD} should not be Power OFF before V_{CC} Power OFF.

9 COMMAND TABLE

Table 9-1: Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	81	1	0	0	0	0	0	0	1	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	A4/A5	1	0	1	0	0	1	0	X ₀	Entire Display ON	A4h, X ₀ =0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X ₀ =1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X ₀	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X ₀	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X ₀	Continuous Horizontal Scroll	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll
0	A[7:0]	0	0	0	0	0	0	0	0	Horizontal Scroll	(Horizontal scroll by 1 column)
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀	Setup	A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀		000b – PAGE0 011b – PAGE3 110b – PAGE6
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀		001b – PAGE1 100b – PAGE4 111b – PAGE7
0	E[7:0]	0	0	0	0	0	0	0	0		010b – PAGE2 101b – PAGE5
0	F[7:0]	1	1	1	1	1	1	1	1		C[2:0] : Set time interval between each scroll step in terms of frame frequency
											000b – 5 frames 100b – 3 frames
											001b – 64 frames 101b – 4 frames
											010b – 128 frames 110b – 25 frame
											011b – 256 frames 111b – 2 frame
											D[2:0] : Define end page address
											000b – PAGE0 011b – PAGE3 110b – PAGE6
											001b – PAGE1 100b – PAGE4 111b – PAGE7
											010b – PAGE2 101b – PAGE5
											The value of D[2:0] must be larger or equal to B[2:0]
											E[7:0] : Dummy byte (Set as 00h)
											F[7:0] : Dummy byte (Set as FFh)

2. Scrolling Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	29/2A	0	0	1	0	1	0	X ₁	X ₀	Continuous Vertical and Right Horizontal Scroll	29h, X ₁ X ₀ =01b : Vertical and Right Horizontal Scroll 2Ah, X ₁ X ₀ =10b : Vertical and Left Horizontal Scroll
0	A[2:0]	0	0	0	0	0	0	0	0	Vertical and Horizontal Scroll	(Horizontal scroll by 1 column)
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀	Horizontal Scroll	A[7:0] : Dummy byte
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀	Setup	
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀		
0	E[5:0]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀	B[2:0] : Define start page address	000b – PAGE0 011b – PAGE3 110b – PAGE6 001b – PAGE1 100b – PAGE4 111b – PAGE7 010b – PAGE2 101b – PAGE5
										C[2:0] : Set time interval between each scroll step in terms of frame frequency	000b – 5 frames 100b – 3 frames 001b – 64 frames 101b – 4 frames 010b – 128 frames 110b – 25 frame 011b – 256 frames 111b – 2 frame
										D[2:0] : Define end page address	000b – PAGE0 011b – PAGE3 110b – PAGE6 001b – PAGE1 100b – PAGE4 111b – PAGE7 010b – PAGE2 101b – PAGE5
										The value of D[2:0] must be larger or equal to B[2:0]	
										E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows	
										Note ⁽¹⁾ No continuous vertical scrolling is available.	
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. Note ⁽¹⁾ After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A3	1	0	1	0	0	0	1	1	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0]
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		

Note

- (¹) A[5:0]+B[6:0] <= MUX ratio
- (²) B[6:0] <= MUX ratio
- (^{3a}) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0]
- (^{3b}) Set Display Start Line (X₅X₄X₃X₂X₁X₀ of 40h~7Fh) < B[6:0]
- (⁴) The last row of the scroll area shifts to the first row of the scroll area.
- (⁵) For 64d MUX display
A[5:0] = 0, B[6:0]=64 : whole area scrolls
A[5:0]= 0, B[6:0] < 64 : top area scrolls
A[5:0] + B[6:0] < 64 : central area scrolls
A[5:0] + B[6:0] = 64 : bottom area scrolls

3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	20	0	0	1	0	0	0	0	0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0	A[1:0]	*	*	*	*	*	*	*	A ₁	A ₀	
0											
0	21	0	0	1	0	0	0	0	1	Set Column Address	Setup column start and end address
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[6:0] : Column start address, range : 0-127d, (RESET=0d)
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		B[6:0]: Column end address, range : 0-127d, (RESET =127d)

Note

- (¹) This command is only for horizontal or vertical addressing mode.

3. Addressing Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	22	0	0	1	0	0	0	1	0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	A[2:0]	*	*	*	*	*	A ₂	A ₁	A ₀		
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀		
										Note	⁽¹⁾ This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X ₂	X ₁	X ₀	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].
										Note	⁽¹⁾ This command is only for page addressing mode

4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	40~7F	0	1	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₅ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X ₀	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET=111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	C0/C8	1	1	0	0	X ₃	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0	D3	1	1	0	1	A ₃	0	A ₂	1	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	DA	1	1	0	1	A ₄	1	0	1	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration
0	A[5:4]	0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D5 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, Fosc. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0	D9 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0	DB A[6:4]	1 0	1 A ₆	0 A ₅	1 A ₄	1 0	0 0	1 0	1 0	Set V _{COMH} Deselect Level	A[6:4] Hex code V _{COMH} deselect level 000b 00h ~ 0.65 x V _{CC} 010b 20h ~ 0.77 x V _{CC} (RESET) 011b 30h ~ 0.83 x V _{CC}
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

Note

(1) “*” stands for “Don’t care”.

Table 9-2 : Read Command Table

Bit Pattern	Command	Description
D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Status Register Read	D[7] : Reserved D[6] : “1” for display OFF / “0” for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note

⁽¹⁾ Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

9.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 9-3 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

10 COMMAND DESCRIPTIONS

10.1 Fundamental Command

10.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

10.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~1Fh)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section Table 9-1 and Section 10.1.3 for details.

10.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1306: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, "COL" means the graphic display data RAM column.

Page addressing mode (A[1:0]=10xb)

In page addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 10-1.

Figure 10-1 : Address Pointer Movement of Page addressing mode

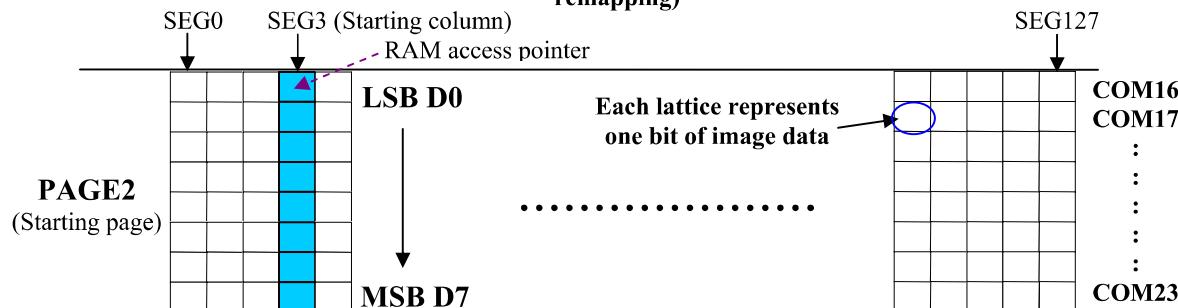
	COL0	COL 1	COL 126	COL 127
PAGE0	→				
PAGE1	→				
:	:	:	:	:	:
PAGE6	→				
PAGE7	→				

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B7h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~1Fh.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 10-2. The input data byte will be written into RAM position of column 3.

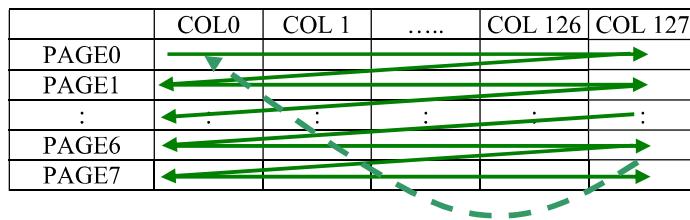
Figure 10-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



Horizontal addressing mode (A[1:0]=00b)

In horizontal addressing mode, after the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 10-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-3.)

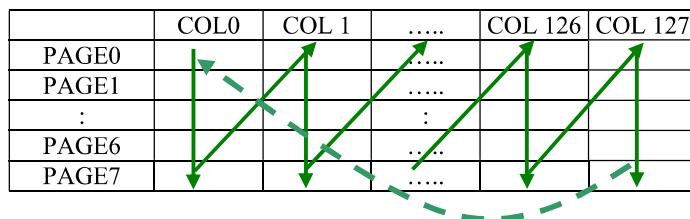
Figure 10-3 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (A[1:0]=01b)

In vertical addressing mode, after the display RAM is read/written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 10-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 10-4.)

Figure 10-4 : Address Pointer Movement of Vertical addressing mode



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 10-5.

10.1.4 Set Column Address (21h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 125, page start address is set to 1 and page end address is set to 6; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from page 1 to page 6 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line* in Figure 10-5). Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and page address is automatically increased by 1 (*solid line* in Figure 10-5). While the end page 6 and end column 125 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line* in Figure 10-5).

Figure 10-5 : Example of Column and Row Address Pointer Movement

	Col 0	Col 1	Col 2	Col 125	Col 126	Col 127
PAGE0								
PAGE1								
:								
PAGE6								
PAGE7								

10.1.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

Refer to Table 10-1 for more illustrations.

10.1.7 Set Contrast Control for BANK0 (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

10.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 9-1.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

10.1.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.

If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.

In other words, A4h command resumes the display from entire display “ON” stage.

A5h command forces the entire display to be “ON”, regardless of the contents of the display data RAM.

10.1.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an “ON” pixel while in inverse display a RAM data of 0 indicates an “ON” pixel.

10.1.11 Set Multiplex Ratio (A8h)

This command switches the default 63 multiplex mode to any multiplex ratio, ranging from 16 to 63. The output pads COM0~COM63 will be switched to the corresponding COM signal.

10.1.12 Set Display ON/OFF (AEh/AFh)

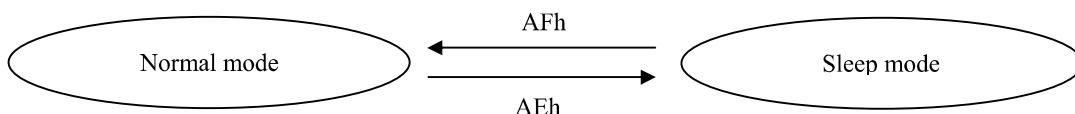
These single byte commands are used to turn the OLED panel display ON or OFF.

When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.

When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 10-6 :Transition between different modes



10.1.13 Set Page Start Address for Page Addressing Mode (B0h~B7h)

This command positions the page start address from 0 to 7 in GDDRAM under Page Addressing Mode. Please refer to Table 9-1 and Section 10.1.3 for details.

10.1.14 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 10-3 for details.

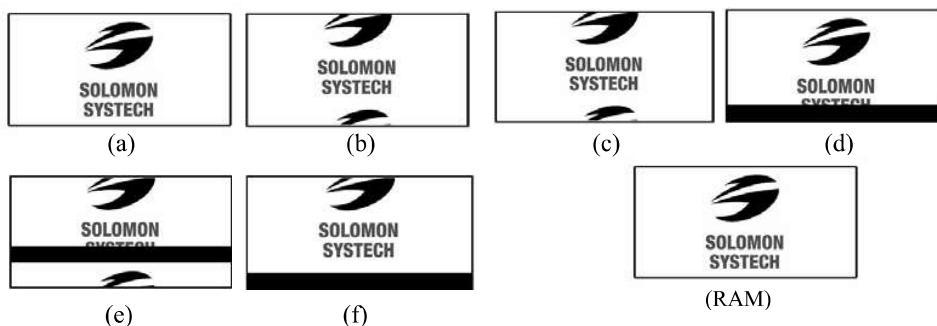
10.1.15 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 – 16, so the second byte would be 100000b. The following two tables (Table 10-1, Table 10-2) show the example of setting the command C0h/C8h and D3h.

Table 10-1 : Example of Set Display Offset and Display Start Line with no Remap

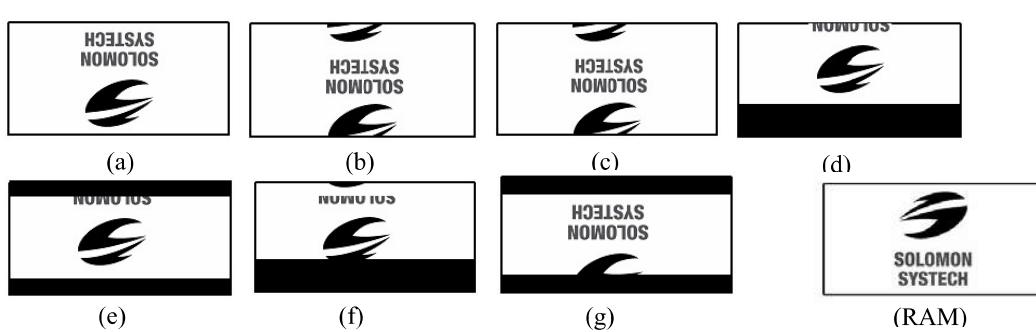
Hardware pin name	Output						Set MUX ratio(A8h) COM Normal / Remapped (C0h / C8h) Display offset (D3h) Display start line (40h - 7Fh)
	64 Normal	64 Normal	64 Normal	56 Normal	56 Normal	56 Normal	
	0	8	0	0	8	0	
	0	0	8	0	0	8	
COM0	Row0 RAM0	Row8 RAM8	Row0 RAM8	Row0 RAM0	Row8 RAM8	Row0 RAM8	
COM1	Row1 RAM1	Row9 RAM9	Row1 RAM9	Row1 RAM1	Row9 RAM9	Row1 RAM9	
COM2	Row2 RAM2	Row10 RAM10	Row2 RAM10	Row2 RAM2	Row10 RAM10	Row2 RAM10	
COM3	Row3 RAM3	Row11 RAM11	Row3 RAM11	Row3 RAM3	Row11 RAM11	Row3 RAM11	
COM4	Row4 RAM4	Row12 RAM12	Row4 RAM12	Row4 RAM4	Row12 RAM12	Row4 RAM12	
COM5	Row5 RAM5	Row13 RAM13	Row5 RAM13	Row5 RAM5	Row13 RAM13	Row5 RAM13	
COM6	Row6 RAM6	Row14 RAM14	Row6 RAM14	Row6 RAM6	Row14 RAM14	Row6 RAM14	
COM7	Row7 RAM7	Row15 RAM15	Row7 RAM15	Row7 RAM7	Row15 RAM15	Row7 RAM15	
COM8	Row8 RAM8	Row16 RAM16	Row8 RAM16	Row8 RAM8	Row16 RAM16	Row8 RAM16	
COM9	Row9 RAM9	Row17 RAM17	Row9 RAM17	Row9 RAM9	Row17 RAM17	Row9 RAM17	
COM10	Row10 RAM10	Row18 RAM18	Row10 RAM18	Row10 RAM10	Row18 RAM18	Row10 RAM18	
COM11	Row11 RAM11	Row19 RAM19	Row11 RAM19	Row11 RAM11	Row19 RAM19	Row11 RAM19	
COM12	Row12 RAM12	Row20 RAM20	Row12 RAM20	Row12 RAM12	Row20 RAM20	Row12 RAM20	
COM13	Row13 RAM13	Row21 RAM21	Row13 RAM21	Row13 RAM13	Row21 RAM21	Row13 RAM21	
COM14	Row14 RAM14	Row22 RAM22	Row14 RAM22	Row14 RAM14	Row22 RAM22	Row14 RAM22	
COM15	Row15 RAM15	Row23 RAM23	Row15 RAM23	Row15 RAM15	Row23 RAM23	Row15 RAM23	
COM16	Row16 RAM16	Row24 RAM24	Row16 RAM24	Row16 RAM16	Row24 RAM24	Row16 RAM24	
COM17	Row17 RAM17	Row25 RAM25	Row17 RAM25	Row17 RAM17	Row25 RAM25	Row17 RAM25	
COM18	Row18 RAM18	Row26 RAM26	Row18 RAM26	Row18 RAM18	Row26 RAM26	Row18 RAM26	
COM19	Row19 RAM19	Row27 RAM27	Row19 RAM27	Row19 RAM19	Row27 RAM27	Row19 RAM27	
COM20	Row20 RAM20	Row28 RAM28	Row20 RAM28	Row20 RAM20	Row28 RAM28	Row20 RAM28	
COM21	Row21 RAM21	Row29 RAM29	Row21 RAM29	Row21 RAM21	Row29 RAM29	Row21 RAM29	
COM22	Row22 RAM22	Row30 RAM30	Row22 RAM30	Row22 RAM22	Row30 RAM30	Row22 RAM30	
COM23	Row23 RAM23	Row31 RAM31	Row23 RAM31	Row23 RAM23	Row31 RAM31	Row23 RAM31	
COM24	Row24 RAM24	Row32 RAM32	Row24 RAM32	Row24 RAM24	Row32 RAM32	Row24 RAM32	
COM25	Row25 RAM25	Row33 RAM33	Row25 RAM33	Row25 RAM25	Row33 RAM33	Row25 RAM33	
COM26	Row26 RAM26	Row34 RAM34	Row26 RAM34	Row26 RAM26	Row34 RAM34	Row26 RAM34	
COM27	Row27 RAM27	Row35 RAM35	Row27 RAM35	Row27 RAM27	Row35 RAM35	Row27 RAM35	
COM28	Row28 RAM28	Row36 RAM36	Row28 RAM36	Row28 RAM28	Row36 RAM36	Row28 RAM36	
COM29	Row29 RAM29	Row37 RAM37	Row29 RAM37	Row29 RAM29	Row37 RAM37	Row29 RAM37	
COM30	Row30 RAM30	Row38 RAM38	Row30 RAM38	Row30 RAM30	Row38 RAM38	Row30 RAM38	
COM31	Row31 RAM31	Row39 RAM39	Row31 RAM39	Row31 RAM31	Row39 RAM39	Row31 RAM39	
COM32	Row32 RAM32	Row40 RAM40	Row32 RAM40	Row32 RAM32	Row40 RAM40	Row32 RAM40	
COM33	Row33 RAM33	Row41 RAM41	Row33 RAM41	Row33 RAM33	Row41 RAM41	Row33 RAM41	
COM34	Row34 RAM34	Row42 RAM42	Row34 RAM42	Row34 RAM34	Row42 RAM42	Row34 RAM42	
COM35	Row35 RAM35	Row43 RAM43	Row35 RAM43	Row35 RAM35	Row43 RAM43	Row35 RAM43	
COM36	Row36 RAM36	Row44 RAM44	Row36 RAM44	Row36 RAM36	Row44 RAM44	Row36 RAM44	
COM37	Row37 RAM37	Row45 RAM45	Row37 RAM45	Row37 RAM37	Row45 RAM45	Row37 RAM45	
COM38	Row38 RAM38	Row46 RAM46	Row38 RAM46	Row38 RAM38	Row46 RAM46	Row38 RAM46	
COM39	Row39 RAM39	Row47 RAM47	Row39 RAM47	Row39 RAM39	Row47 RAM47	Row39 RAM47	
COM40	Row40 RAM40	Row48 RAM48	Row40 RAM48	Row40 RAM40	Row48 RAM48	Row40 RAM48	
COM41	Row41 RAM41	Row49 RAM49	Row41 RAM49	Row41 RAM41	Row49 RAM49	Row41 RAM49	
COM42	Row42 RAM42	Row50 RAM50	Row42 RAM50	Row42 RAM42	Row50 RAM50	Row42 RAM50	
COM43	Row43 RAM43	Row51 RAM51	Row43 RAM51	Row43 RAM43	Row51 RAM51	Row43 RAM51	
COM44	Row44 RAM44	Row52 RAM52	Row44 RAM52	Row44 RAM44	Row52 RAM52	Row44 RAM52	
COM45	Row45 RAM45	Row53 RAM53	Row45 RAM53	Row45 RAM45	Row53 RAM53	Row45 RAM53	
COM46	Row46 RAM46	Row54 RAM54	Row46 RAM54	Row46 RAM46	Row54 RAM54	Row46 RAM54	
COM47	Row47 RAM47	Row55 RAM55	Row47 RAM55	Row47 RAM47	Row55 RAM55	Row47 RAM55	
COM48	Row48 RAM48	Row56 RAM56	Row48 RAM56	Row48 RAM48	-	-	Row48 RAM56
COM49	Row49 RAM49	Row57 RAM57	Row49 RAM57	Row49 RAM49	-	-	Row49 RAM57
COM50	Row50 RAM50	Row58 RAM58	Row50 RAM58	Row50 RAM50	-	-	Row50 RAM58
COM51	Row51 RAM51	Row59 RAM59	Row51 RAM59	Row51 RAM51	-	-	Row51 RAM59
COM52	Row52 RAM52	Row60 RAM60	Row52 RAM60	Row52 RAM52	-	-	Row52 RAM60
COM53	Row53 RAM53	Row61 RAM61	Row53 RAM61	Row53 RAM53	-	-	Row53 RAM61
COM54	Row54 RAM54	Row62 RAM62	Row54 RAM62	Row54 RAM54	-	-	Row54 RAM62
COM55	Row55 RAM55	Row63 RAM63	Row55 RAM63	Row55 RAM55	-	-	Row55 RAM63
COM56	Row56 RAM56	Row64 RAM64	Row56 RAM64	-	-	-	
COM57	Row57 RAM57	Row65 RAM65	Row57 RAM65	-	-	-	
COM58	Row58 RAM58	Row66 RAM66	Row58 RAM66	-	-	-	
COM59	Row59 RAM59	Row67 RAM67	Row59 RAM67	-	-	-	
COM60	Row60 RAM60	Row68 RAM68	Row60 RAM68	-	-	-	
COM61	Row61 RAM61	Row69 RAM69	Row61 RAM69	-	-	-	
COM62	Row62 RAM62	Row70 RAM70	Row62 RAM70	-	-	-	
COM63	Row63 RAM63	Row71 RAM71	Row63 RAM71	-	-	-	
Display examples	(a)	(b)	(c)	(d)	(e)	(f)	



(RAM)

Table 10-2 :Example of Set Display Offset and Display Start Line with Remap

Hardware pin name	Output							Set MUX ratio(A8h) COM Normal / Remapped (C0h / C8h) Display offset (D3h) Display start line (40h - 7fh)
	64 Remap 0 0	64 Remap 8 0	64 Remap 0 8	48 Remap 0 0	48 Remap 8 0	48 Remap 0 8	48 Remap 8 16	
	Row63 RAM63	Row7 RAM7	Row63 RAM7	Row47 RAM47	- -	Row47 RAM55	- -	
	Row62 RAM62	Row6 RAM6	Row62 RAM6	Row46 RAM46	- -	Row46 RAM54	- -	
COM1	Row61 RAM61	Row5 RAM5	Row61 RAM5	Row45 RAM45	- -	Row45 RAM53	- -	
COM2	Row60 RAM60	Row4 RAM4	Row60 RAM4	Row44 RAM44	- -	Row44 RAM52	- -	
COM3	Row59 RAM59	Row3 RAM3	Row59 RAM3	Row43 RAM43	- -	Row43 RAM51	- -	
COM4	Row68 RAM68	Row2 RAM2	Row68 RAM2	Row42 RAM42	- -	Row42 RAM50	- -	
COM5	Row57 RAM57	Row1 RAM1	Row57 RAM1	Row41 RAM41	- -	Row41 RAM49	- -	
COM6	Row66 RAM66	Row0 RAM0	Row66 RAM0	Row40 RAM40	- -	Row40 RAM48	- -	
COM7	Row65 RAM65	Row63 RAM63	Row65 RAM63	Row39 RAM39	Row47 RAM47	Row39 RAM47	Row47 RAM53	
COM8	Row64 RAM64	Row62 RAM62	Row64 RAM62	Row38 RAM38	Row46 RAM46	Row38 RAM46	Row46 RAM52	
COM9	Row53 RAM53	Row61 RAM61	Row53 RAM61	Row37 RAM37	Row45 RAM45	Row37 RAM45	Row45 RAM51	
COM10	Row52 RAM52	Row60 RAM60	Row52 RAM60	Row36 RAM36	Row44 RAM44	Row36 RAM44	Row44 RAM60	
COM11	Row51 RAM51	Row69 RAM69	Row51 RAM69	Row35 RAM35	Row43 RAM43	Row35 RAM43	Row43 RAM59	
COM12	Row50 RAM50	Row68 RAM68	Row50 RAM68	Row34 RAM34	Row42 RAM42	Row34 RAM42	Row42 RAM58	
COM13	Row49 RAM49	Row57 RAM57	Row49 RAM57	Row33 RAM33	Row41 RAM41	Row33 RAM41	Row41 RAM57	
COM14	Row48 RAM48	Row56 RAM56	Row48 RAM56	Row32 RAM32	Row40 RAM40	Row32 RAM40	Row40 RAM56	
COM15	Row47 RAM47	Row55 RAM55	Row47 RAM55	Row31 RAM31	Row39 RAM39	Row31 RAM39	Row39 RAM55	
COM16	Row46 RAM46	Row54 RAM54	Row46 RAM54	Row30 RAM30	Row38 RAM38	Row30 RAM38	Row38 RAM54	
COM17	Row45 RAM45	Row53 RAM53	Row45 RAM53	Row29 RAM29	Row37 RAM37	Row29 RAM37	Row37 RAM53	
COM18	Row44 RAM44	Row52 RAM52	Row44 RAM52	Row28 RAM28	Row36 RAM36	Row28 RAM36	Row36 RAM52	
COM19	Row43 RAM43	Row51 RAM51	Row43 RAM51	Row27 RAM27	Row35 RAM35	Row27 RAM35	Row29 RAM51	
COM20	Row42 RAM42	Row50 RAM50	Row42 RAM50	Row26 RAM26	Row34 RAM34	Row26 RAM34	Row34 RAM50	
COM21	Row41 RAM41	Row49 RAM49	Row41 RAM49	Row25 RAM25	Row33 RAM33	Row25 RAM33	Row33 RAM49	
COM22	Row40 RAM40	Row48 RAM48	Row40 RAM48	Row24 RAM24	Row32 RAM32	Row24 RAM32	Row32 RAM48	
COM23	Row39 RAM39	Row47 RAM47	Row39 RAM47	Row23 RAM23	Row31 RAM31	Row23 RAM31	Row31 RAM47	
COM24	Row38 RAM38	Row46 RAM46	Row38 RAM46	Row22 RAM22	Row30 RAM30	Row22 RAM30	Row30 RAM46	
COM25	Row37 RAM37	Row45 RAM45	Row37 RAM45	Row21 RAM21	Row29 RAM29	Row21 RAM29	Row29 RAM45	
COM26	Row36 RAM36	Row44 RAM44	Row36 RAM44	Row20 RAM20	Row28 RAM28	Row20 RAM28	Row28 RAM44	
COM27	Row35 RAM35	Row43 RAM43	Row35 RAM43	Row19 RAM19	Row27 RAM27	Row19 RAM27	Row27 RAM43	
COM28	Row34 RAM34	Row42 RAM42	Row34 RAM42	Row18 RAM18	Row26 RAM26	Row18 RAM26	Row26 RAM42	
COM29	Row33 RAM33	Row41 RAM41	Row33 RAM41	Row17 RAM17	Row25 RAM25	Row17 RAM25	Row25 RAM41	
COM30	Row32 RAM32	Row40 RAM40	Row32 RAM40	Row16 RAM16	Row24 RAM24	Row16 RAM24	Row24 RAM40	
COM31	Row31 RAM31	Row39 RAM39	Row31 RAM39	Row15 RAM15	Row23 RAM23	Row15 RAM23	Row23 RAM39	
COM32	Row30 RAM30	Row38 RAM38	Row30 RAM38	Row14 RAM14	Row22 RAM22	Row14 RAM22	Row22 RAM38	
COM33	Row29 RAM29	Row37 RAM37	Row29 RAM37	Row13 RAM13	Row21 RAM21	Row13 RAM21	Row21 RAM37	
COM34	Row28 RAM28	Row36 RAM36	Row28 RAM36	Row12 RAM12	Row20 RAM20	Row12 RAM20	Row20 RAM36	
COM35	Row27 RAM27	Row35 RAM35	Row27 RAM35	Row11 RAM11	Row19 RAM19	Row11 RAM19	Row19 RAM35	
COM36	Row26 RAM26	Row34 RAM34	Row26 RAM34	Row10 RAM10	Row18 RAM18	Row10 RAM18	Row18 RAM34	
COM37	Row25 RAM25	Row33 RAM33	Row25 RAM33	Row9 RAM9	Row17 RAM17	Row9 RAM17	Row17 RAM33	
COM38	Row24 RAM24	Row32 RAM32	Row24 RAM32	Row8 RAM8	Row16 RAM16	Row8 RAM16	Row16 RAM32	
COM39	Row23 RAM23	Row31 RAM31	Row23 RAM31	Row7 RAM7	Row15 RAM15	Row7 RAM15	Row15 RAM31	
COM40	Row22 RAM22	Row30 RAM30	Row22 RAM30	Row6 RAM6	Row14 RAM14	Row6 RAM14	Row14 RAM30	
COM41	Row21 RAM21	Row29 RAM29	Row21 RAM29	Row5 RAM5	Row13 RAM13	Row5 RAM13	Row13 RAM29	
COM42	Row20 RAM20	Row28 RAM28	Row20 RAM28	Row4 RAM4	Row12 RAM12	Row4 RAM12	Row12 RAM28	
COM43	Row19 RAM19	Row27 RAM27	Row19 RAM27	Row3 RAM3	Row11 RAM11	Row3 RAM11	Row11 RAM27	
COM44	Row18 RAM18	Row26 RAM26	Row18 RAM26	Row2 RAM2	Row10 RAM10	Row2 RAM10	Row10 RAM26	
COM45	Row17 RAM17	Row25 RAM25	Row17 RAM25	Row1 RAM1	Row9 RAM9	Row1 RAM9	Row9 RAM25	
COM46	Row16 RAM16	Row24 RAM24	Row16 RAM24	Row0 RAM0	Row8 RAM8	Row0 RAM8	Row8 RAM24	
COM47	Row15 RAM15	Row23 RAM23	Row15 RAM23	- -	Row7 RAM7	- -	Row7 RAM23	
COM48	Row14 RAM14	Row22 RAM22	Row14 RAM22	- -	Row6 RAM6	- -	Row6 RAM22	
COM49	Row13 RAM13	Row21 RAM21	Row13 RAM21	- -	Row5 RAM5	- -	Row5 RAM21	
COM50	Row12 RAM12	Row20 RAM20	Row12 RAM20	- -	Row4 RAM4	- -	Row4 RAM20	
COM51	Row11 RAM11	Row19 RAM19	Row11 RAM19	- -	Row3 RAM3	- -	Row3 RAM19	
COM52	Row10 RAM10	Row18 RAM18	Row10 RAM18	- -	Row2 RAM2	- -	Row2 RAM18	
COM53	Row9 RAM9	Row17 RAM17	Row9 RAM17	- -	Row1 RAM1	- -	Row1 RAM17	
COM54	Row8 RAM8	Row16 RAM16	Row8 RAM16	- -	Row0 RAM0	- -	Row0 RAM16	
COM55	Row7 RAM7	Row15 RAM15	Row7 RAM15	- -	- -	- -	- -	
COM56	Row6 RAM6	Row14 RAM14	Row6 RAM14	- -	- -	- -	- -	
COM57	Row5 RAM5	Row13 RAM13	Row5 RAM13	- -	- -	- -	- -	
COM58	Row4 RAM4	Row12 RAM12	Row4 RAM12	- -	- -	- -	- -	
COM59	Row3 RAM3	Row11 RAM11	Row3 RAM11	- -	- -	- -	- -	
COM60	Row2 RAM2	Row10 RAM10	Row2 RAM10	- -	- -	- -	- -	
COM61	Row1 RAM1	Row9 RAM9	Row1 RAM9	- -	- -	- -	- -	
COM62	Row0 RAM0	Row8 RAM8	Row0 RAM8	- -	- -	- -	- -	
COM63	(a)	(b)	(c)	(d)	(e)	(f)	(g)	
Display examples	(a)	(b)	(c)	(d)	(e)	(f)	(g)	



10.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D)(A[3:0])
Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 8.3 for the details relationship of DCLK and CLK.
- Oscillator Frequency (A[7:4])
Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1000b.

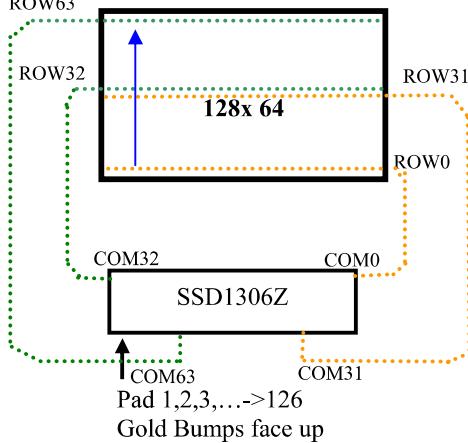
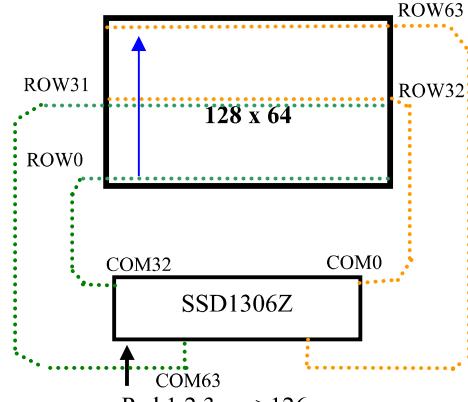
10.1.17 Set Pre-charge Period (D9h)

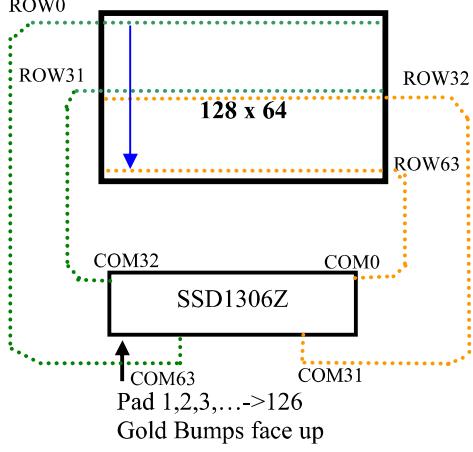
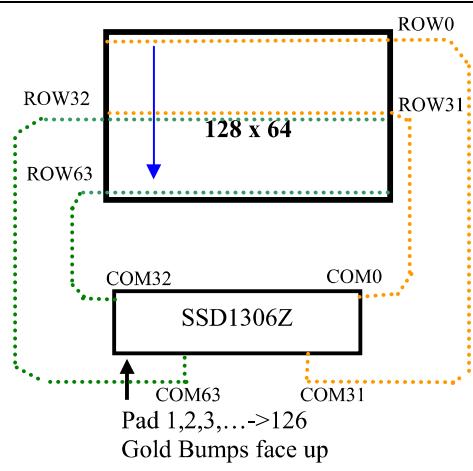
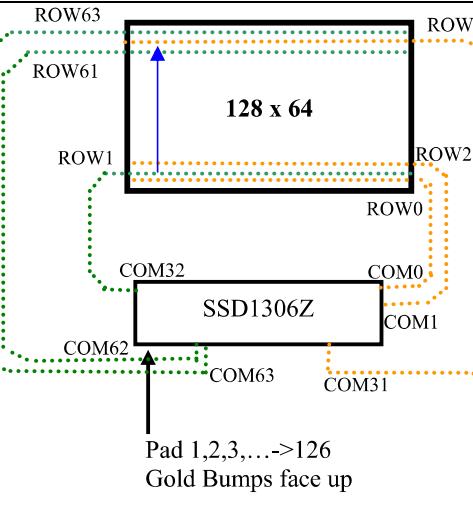
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals 2 DCLKs.

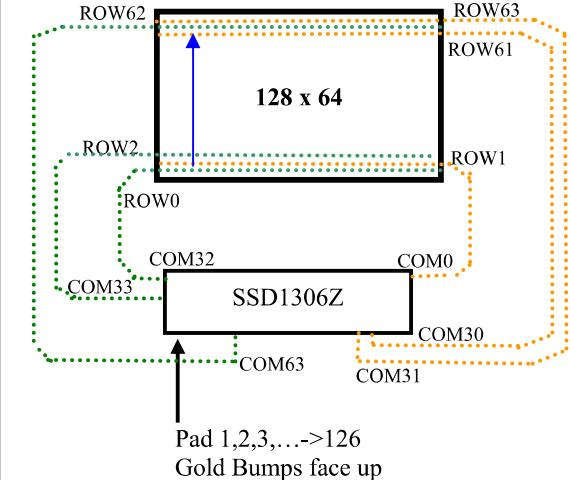
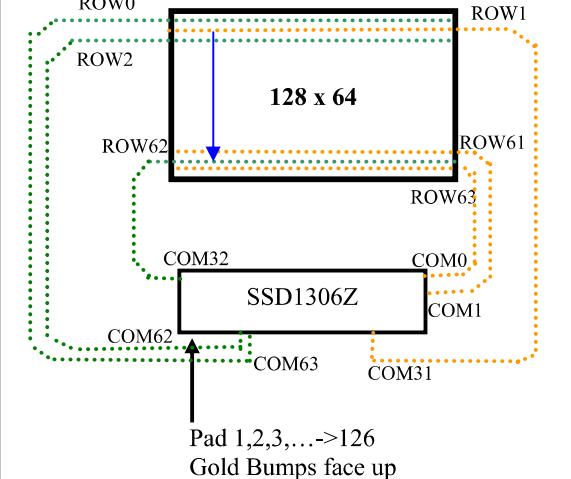
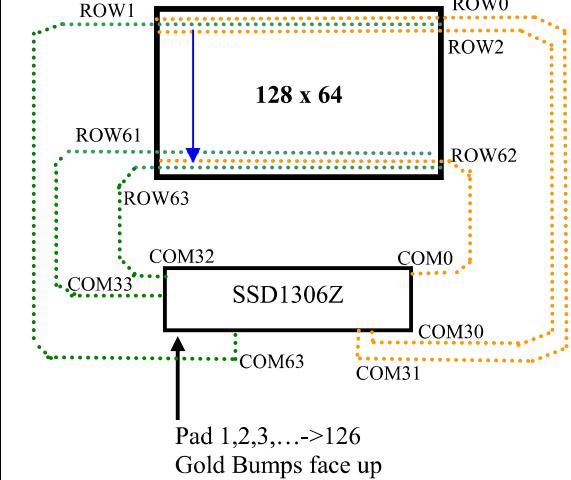
10.1.18 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. The table below shows the COM pin configuration under different conditions (for MUX ratio =64):

Table 10-3 : COM Pins Hardware Configuration

Conditions	COM pins Configurations
1 Sequential COM pin configuration (DAh A[4]=0) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5]=0)	
2 Sequential COM pin configuration (DAh A[4]=0) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5]=1)	

Conditions	COM pins Configurations
3 Sequential COM pin configuration (DAh A[4]=0) COM output Scan direction: from COM63 to COM0 (C8h) Disable COM Left/Right remap (DAh A[5]=0)	 <p>ROW0 ROW31 ROW63 COM32 COM0 SSD1306Z COM63 Pad 1,2,3,...>126 Gold Bumps face up</p>
4 Sequential COM pin configuration (DAh A[4]=0) COM output Scan direction: from COM63 to COM0 (C8h) Enable COM Left/Right remap (DAh A[5]=1)	 <p>ROW0 ROW32 ROW63 ROW31 COM32 COM0 SSD1306Z COM63 Pad 1,2,3,...>126 Gold Bumps face up</p>
5 Alternative COM pin configuration (DAh A[4]=1) COM output Scan direction: from COM0 to COM63 (C0h) Disable COM Left/Right remap (DAh A[5]=0)	 <p>ROW63 ROW61 ROW1 ROW0 COM32 COM0 SSD1306Z COM62 COM63 COM31 Pad 1,2,3,...>126 Gold Bumps face up</p>

Conditions	COM pins Configurations
6 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM0 to COM63 (C0h) Enable COM Left/Right remap (DAh A[5] =1)	 <p>Pad 1,2,3,...>126 Gold Bumps face up</p>
7 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Disable COM Left/Right remap (DAh A[5] =0)	 <p>Pad 1,2,3,...>126 Gold Bumps face up</p>
8 Alternative COM pin configuration (DAh A[4] =1) COM output Scan direction: from COM63 to COM0(C8h) Enable COM Left/Right remap (DAh A[5] =1)	 <p>Pad 1,2,3,...>126 Gold Bumps face up</p>

10.1.19 Set V_{COMH} Deselect Level (DBh)

This command adjusts the V_{COMH} regulator output.

10.1.20 NOP (E3h)

No Operation Command

10.1.21 Status register Read

This command is issued by setting D/C# ON LOW during a data read (See Figure 13-1 to Figure 13-2 for parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

10.2 Graphic Acceleration Command

10.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1306 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 10-7, Figure 10-8, Figure 10-9) show the examples of using the horizontal scroll:

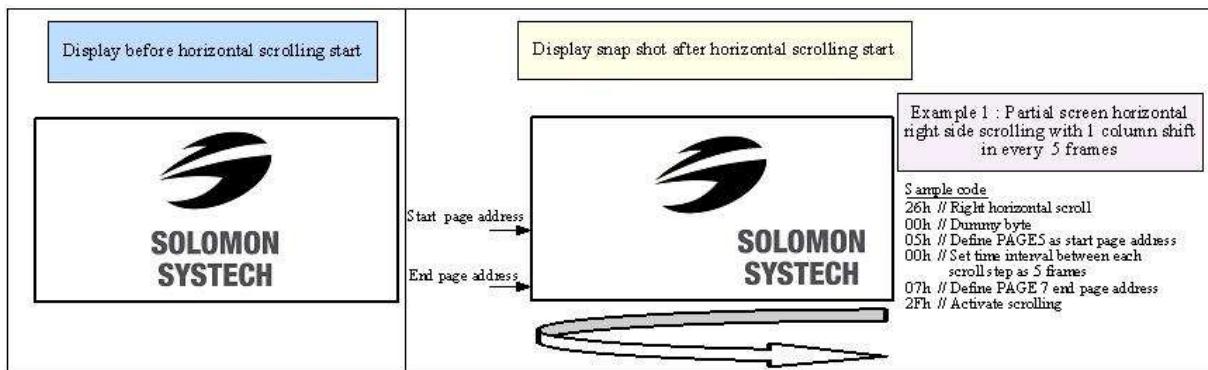
Figure 10-7 : Horizontal scroll example: Scroll RIGHT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5
After one scroll step	SEG127	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16

Figure 10-8 : Horizontal scroll example: Scroll LEFT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
After one scroll step	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG0

Figure 10-9 : Horizontal scrolling setup example



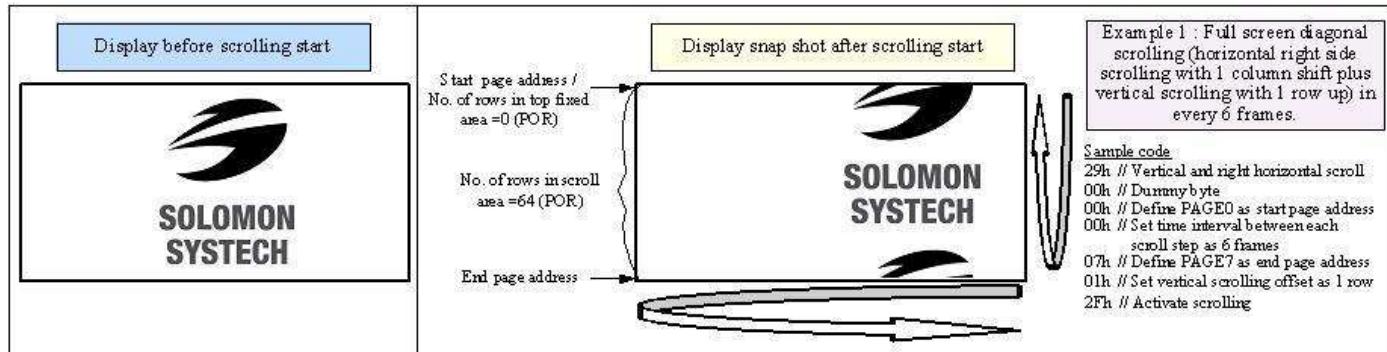
10.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of 6 consecutive bytes to set up the continuous vertical scroll parameters and determines the scrolling start page, end page, scrolling speed and vertical scrolling offset.

The bytes B[2:0], C[2:0] and D[2:0] of command 29h/2Ah are for the setting of the continuous horizontal scrolling. The byte E[5:0] is for the setting of the continuous vertical scrolling offset. All these bytes together are for the setting of continuous diagonal (horizontal + vertical) scrolling. If the vertical scrolling offset byte E[5:0] is set to zero, then only horizontal scrolling is performed (like command 26/27h).

Before issuing this command the scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted. The following figure (Figure 10-10) show the example of using the continuous vertical and horizontal scroll:

Figure 10-10 : Continuous Vertical and Horizontal scrolling setup example



10.2.3 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.4 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands :26h/27h/29h/2Ah . The setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

10.2.5 Set Vertical Scroll Area(A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29/2Ah), the number of rows that in vertical scrolling can be set smaller or equal to the MUX ratio.

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9* V_{CC}	V
V_{in}	Input voltage	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 1.65 to 3.3V

T_A = 25°C

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{CC}	Operating Voltage	-	7	-	15	V
V _{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V _{OH}	High Logic Output Level	I _{OUT} = 100uA, 3.3MHz	0.9 x V _{DD}	-	-	V
V _{OL}	Low Logic Output Level	I _{OUT} = 100uA, 3.3MHz	-	-	0.1 x V _{DD}	V
V _{IH}	High Logic Input Level	-	0.8 x V _{DD}	-	-	V
V _{IL}	Low Logic Input Level	-	-	-	0.2 x V _{DD}	V
I _{CC, SLEEP}	I _{CC} , Sleep mode Current	V _{DD} = 1.65V~3.3V, V _{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
I _{DD, SLEEP}	I _{DD} , Sleep mode Current	V _{DD} = 1.65V~3.3V, V _{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
I _{CC}	V _{CC} Supply Current V _{DD} = 2.8V, V _{CC} = 12V, I _{REF} = 12.5uA No loading, Display ON, All ON	Contrast = FFh	-	430	780	uA
I _{DD}	V _{DD} Supply Current V _{DD} = 2.8V, V _{CC} = 12V, I _{REF} = 12.5uA No loading, Display ON, All ON		-	50	150	uA
I _{SEG}	Segment Output Current V _{DD} =2.8V, V _{CC} =12V, I _{REF} =12.5uA, Display ON.	Contrast=FFh Contrast=AFh Contrast=3Fh	-	100	-	uA
Dev	Segment output current uniformity	Dev = (I _{SEG} - I _{MID}) / I _{MID} I _{MID} = (I _{MAX} + I _{MIN}) / 2 I _{SEG[0:131]} = Segment current at contrast = FFh	-3	-	+3	
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	+2	%

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}

V_{DD}=1.65 to 3.3V

T_A = 25°C

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
FOSC ⁽¹⁾	Oscillation Frequency of Display Timing Generator	V _{DD} = 2.8V	333	370	407	kHz
F _{FRM}	Frame Frequency for 64 MUX Mode	128x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F _{Osc} x 1/(D _x K _x 64) ⁽²⁾	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

⁽¹⁾ FOSC stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

⁽²⁾ D: divide ratio (default value = 1)

K: number of display clocks (default value = 54)

Please refer to Table 9-1 (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 1.65V$ to $3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

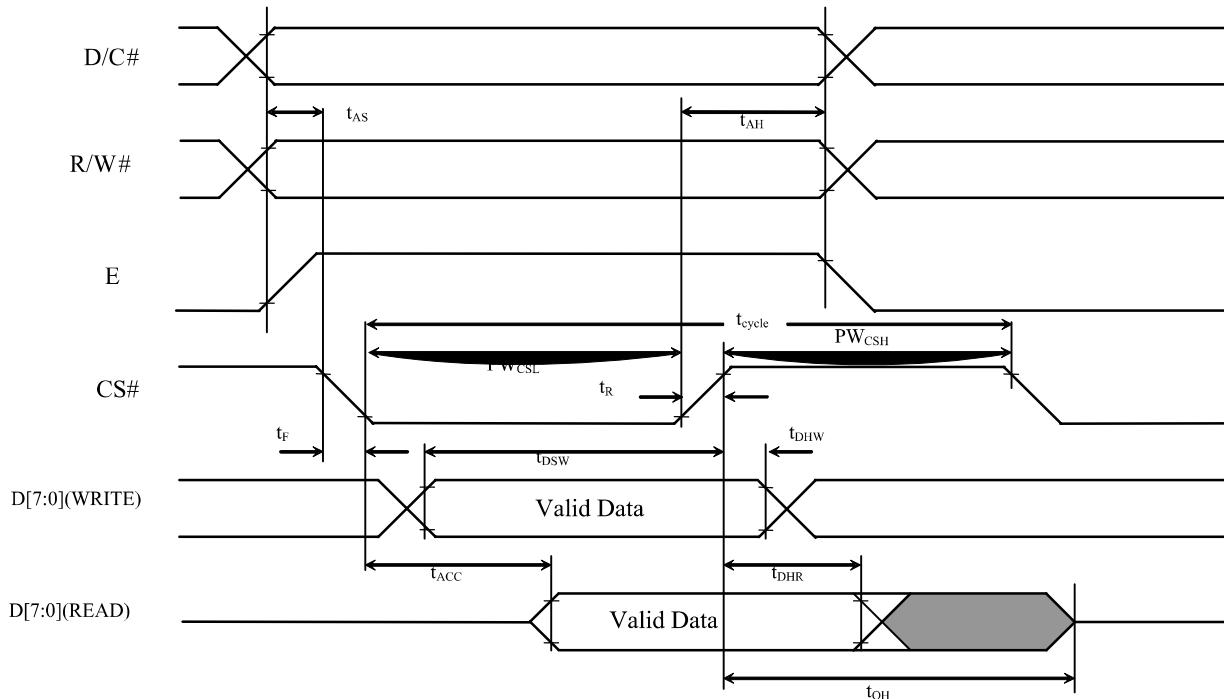


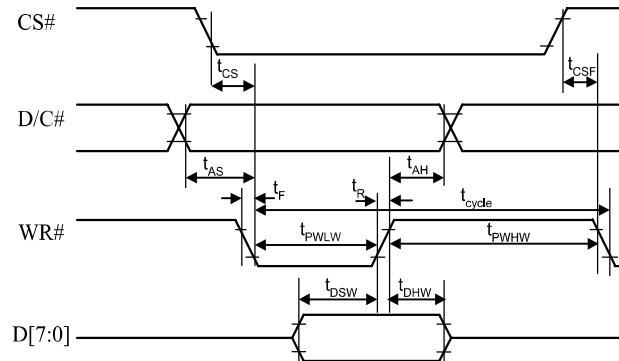
Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 1.65V$ to $3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics

Write Cycle



Read cycle

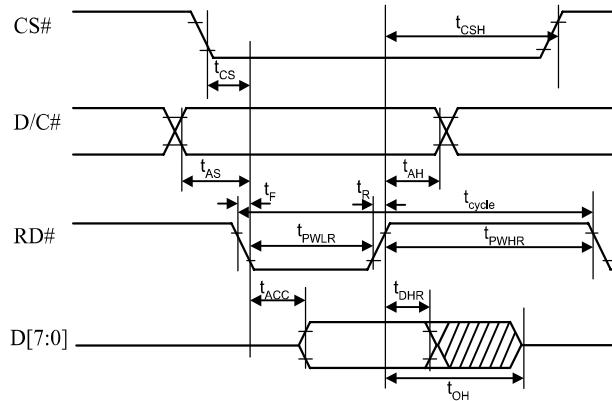


Table 13-4 : 4-wire Serial Interface Timing Characteristics

($V_{DD} - V_{SS} = 1.65V$ to $3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-3 : 4-wire Serial interface characteristics

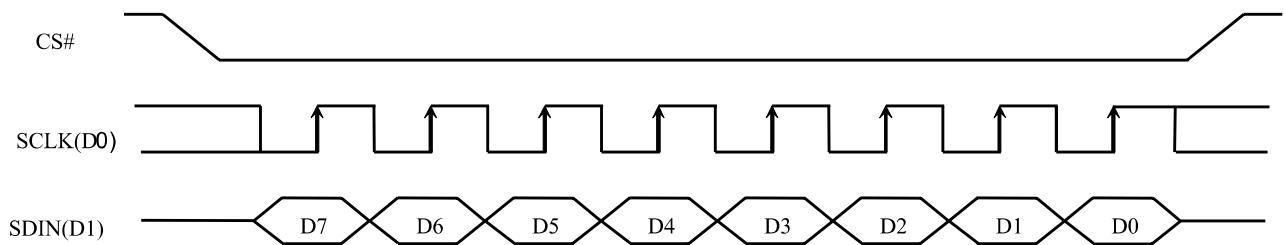
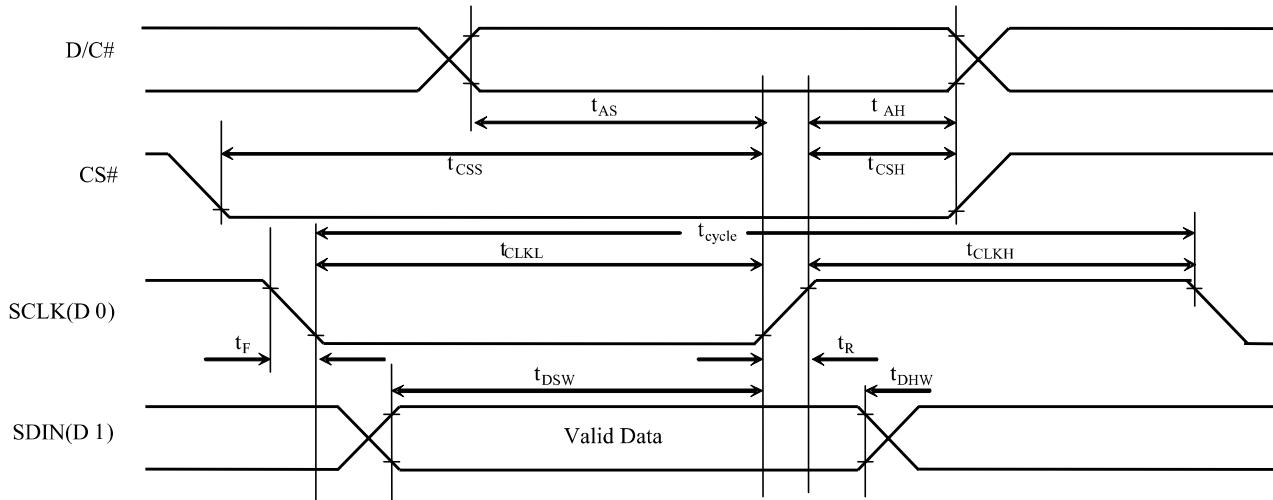
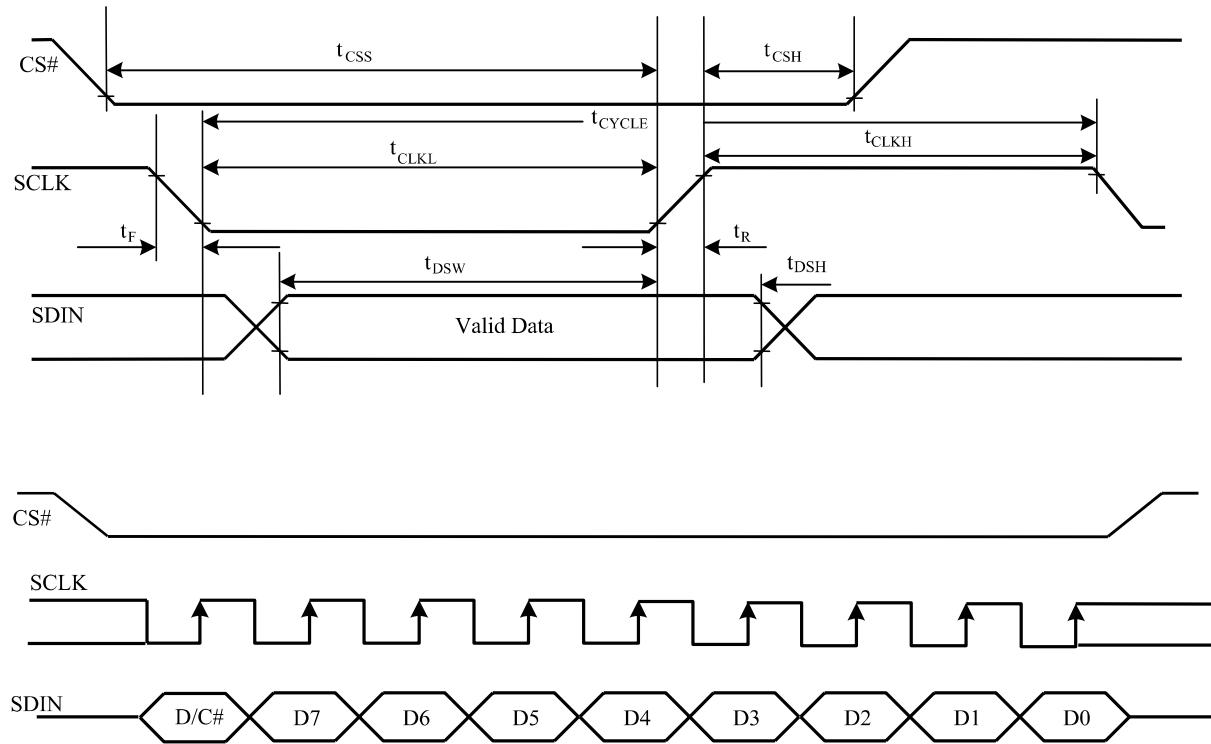


Table 13-5 : 3-wire Serial Interface Timing Characteristics

($V_{DD} - V_{SS} = 1.65V$ to $3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-4 : 3-wire Serial interface characteristics



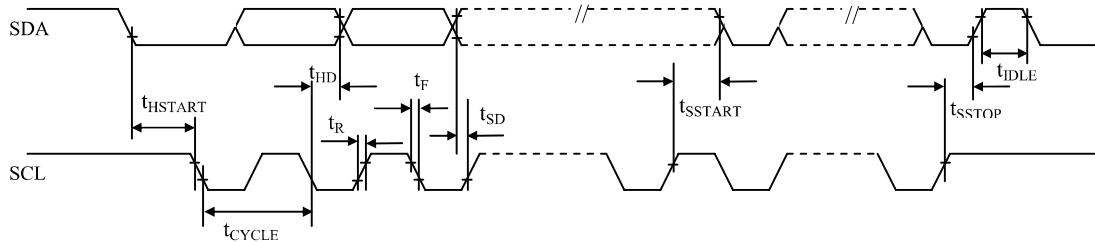
Conditions:

$V_{DD} - V_{SS} = V_{DD} - V_{SS} = 1.65V$ to $3.3V$
 $T_A = 25^\circ C$

Table 13-6 :I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA _{OUT} " pin)	0	-	-	ns
	Data Hold Time (for "SDA _{IN} " pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{STOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

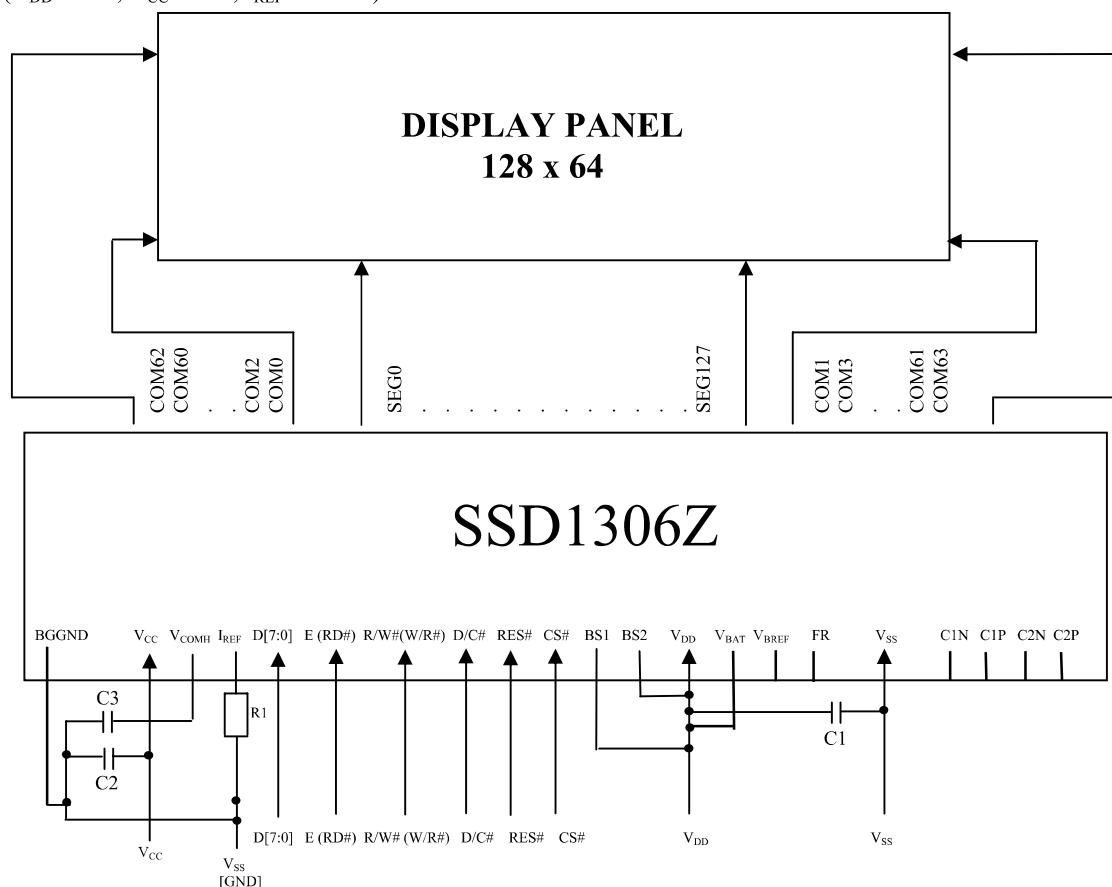
Figure 13-5 : I²C interface Timing characteristics



14 Application Example

Figure 14-1 : Application Example of SSD1306Z

The configuration for 8080-parallel interface mode is shown in the following diagram:
 $(V_{DD}=2.8V, V_{CC}=12V, I_{REF}=12.5\mu A)$



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, CS#, RES#

Pin internally connected to V_{SS}: BS0, CL

Pin internally connected to V_{DD}: CLS

C2P, C2N, C1P, C1N, V_{BREF}, FB should be left open.

C1: 1.0uF ⁽¹⁾

C2: 2.2uF ⁽¹⁾

C3: 2.2uF ⁽¹⁾

Voltage at I_{REF} = V_{CC} - 2.5V. For V_{CC} = 12V, I_{REF} = 12.5uA:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$= (12-2.5) / 12.5\mu A$$

$$= 760K\Omega$$

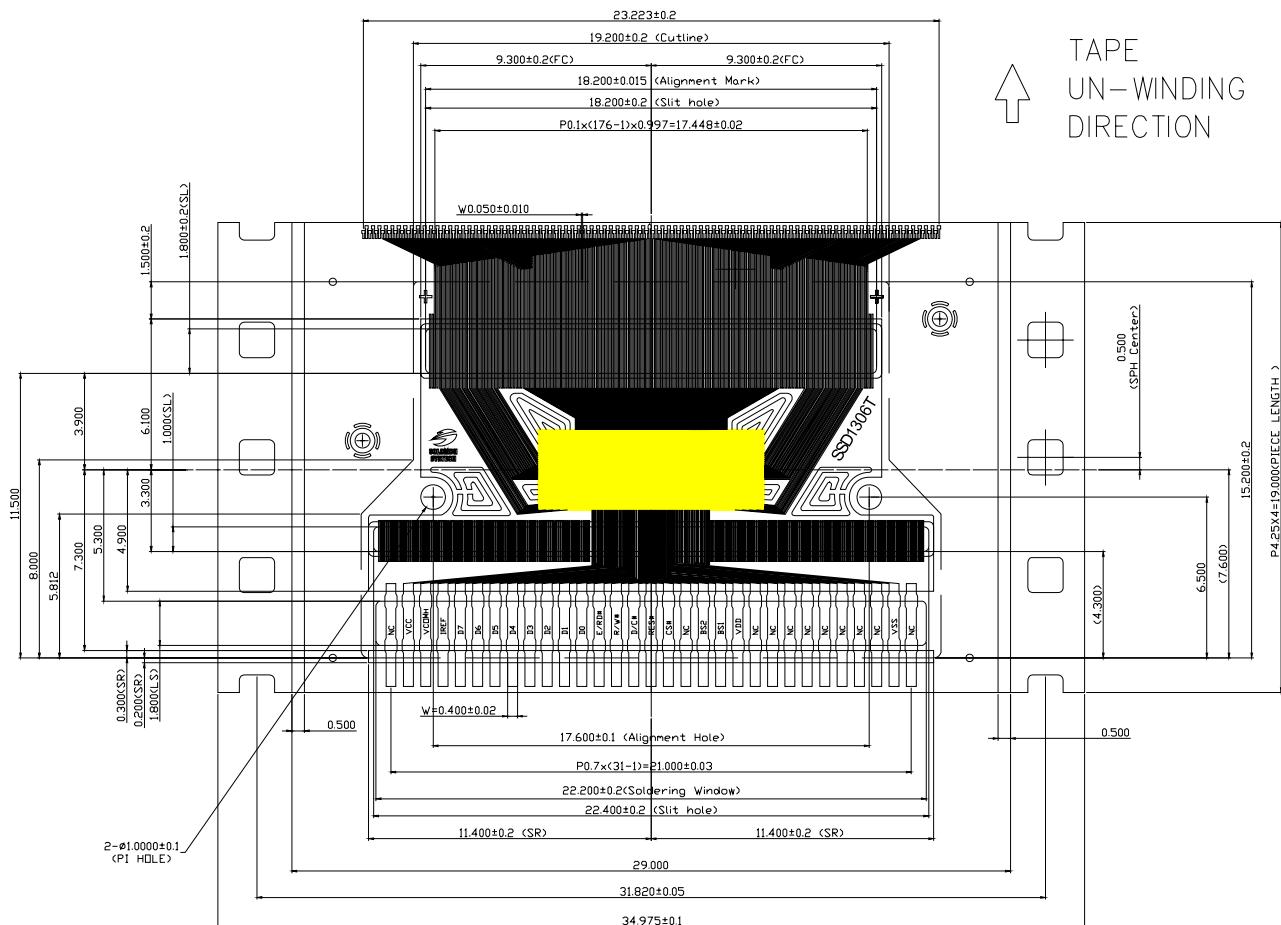
Note

⁽¹⁾The capacitor value is recommended value. Select appropriate value against module application.

15 PACKAGE INFORMATION

15.1 SSD1306TR1 Detail Dimension

Figure 15-1 SSD1306TR1 Detail Dimension



Specification:

1. GENERAL TOLERANCE: ± 0.05 mm

2. MATERIAL

PI: 75 ± 8 μm

CU: 15 ± 3 μm

ADHESIVE: 12 ± 3 μm

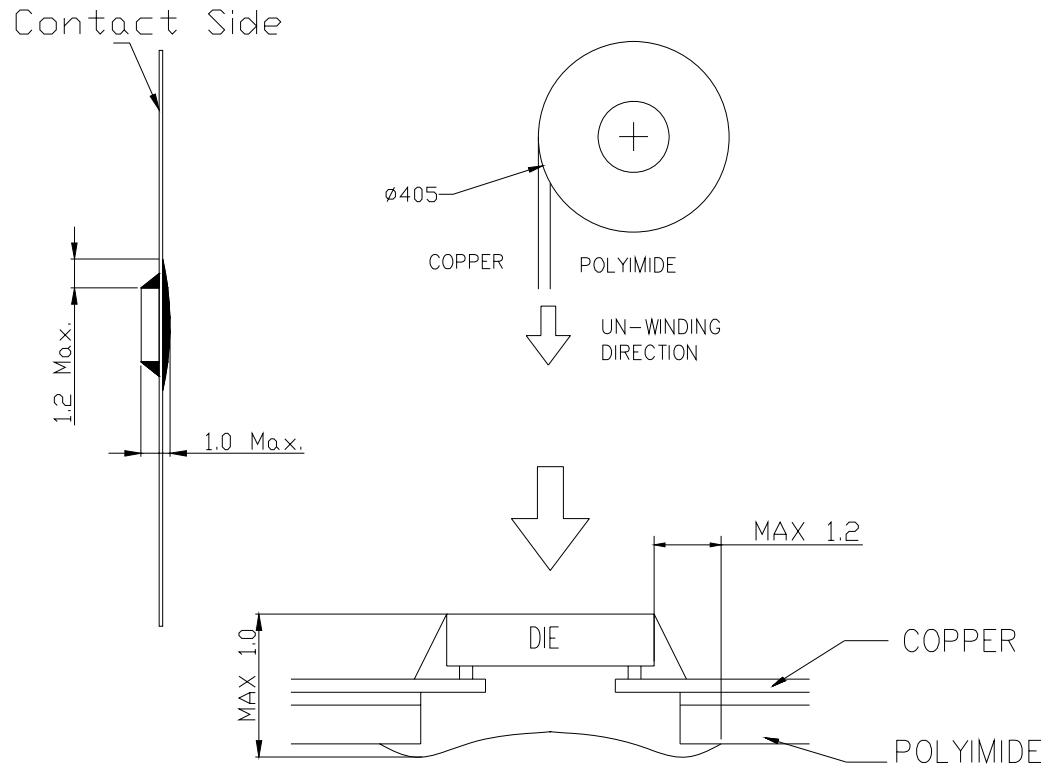
SR: 26 ± 14 μm

TOLERANCE ± 0.200 mm

FLEX COATING: Min 10 μm

3. Plating : Sn 0.20 ± 0.05 μm

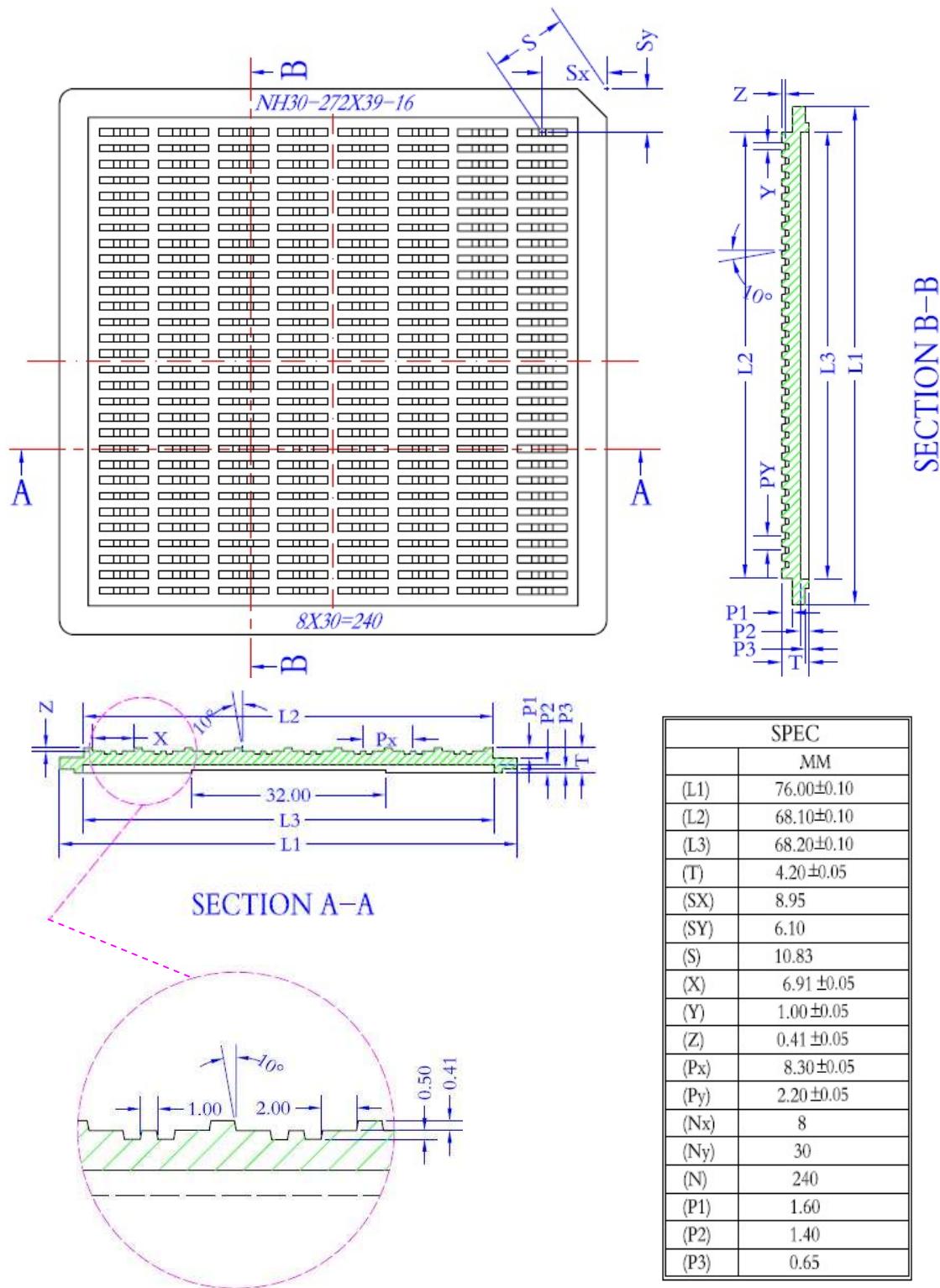
4. TAPESITE: 4 SPH, 19 mm



MIRROR DESIGN

15.2 SSD1306Z Die Tray Information

Figure 15-2 : SSD1306Z die tray information



Solomon Systech reserves the right to make changes without notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any, and all, liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typical" must be validated for each customer application by the customer's technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) "Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)" and China standard "电子信息产品污染控制标识要求 (SJ/T11364-2006)" with control Marking Symbol . Hazardous Substances test report is available upon requested.

<http://www.solomon-systech.com>

SSD1306

Application Note

**128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TABLE OF CONTENTS

1	INTRODUCTION	3
2	CHARGE PUMP REGULATOR	3
2.1	Command Table for Charge Bump Setting	3
3	SOFTWARE CONFIGURATION	5

TABLE OF FIGURES

Figure 1 : Application Example of SSD1306Z with charge bump	4
Figure 2 : Software Initialization Flow Chart	5

Confidential
to
Univision Technology Inc.

1 Introduction

This application note of SSD1306 is written to explain the charge pump regulator function of SSD1306. SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

For the detailed characteristics of the driver IC, please refer to SSD1306 datasheet.

2 Charge Pump Regulator

The internal regulator circuit in SSD1306 accompanying only 2 external capacitors can generate a 7.5V voltage supply, V_{CC} , from a low voltage supply input, V_{BAT} . The V_{CC} is the voltage supply to the OLED driver block. This is a switching capacitor regulator circuit, designed for handheld applications. This regulator can be turned on/off by software command setting.

- Power supply
 - $V_{DD} = 1.65V$ to $3.3V < V_{BAT}$ for IC logic
 - $V_{BAT} = 3.3V$ to $4.2V$ for charge pump regulator circuit
- Pins description for related pins of the charge pump regulator
 - V_{BAT} – Power supply for charge pump regulator circuit.
 - Status Table:

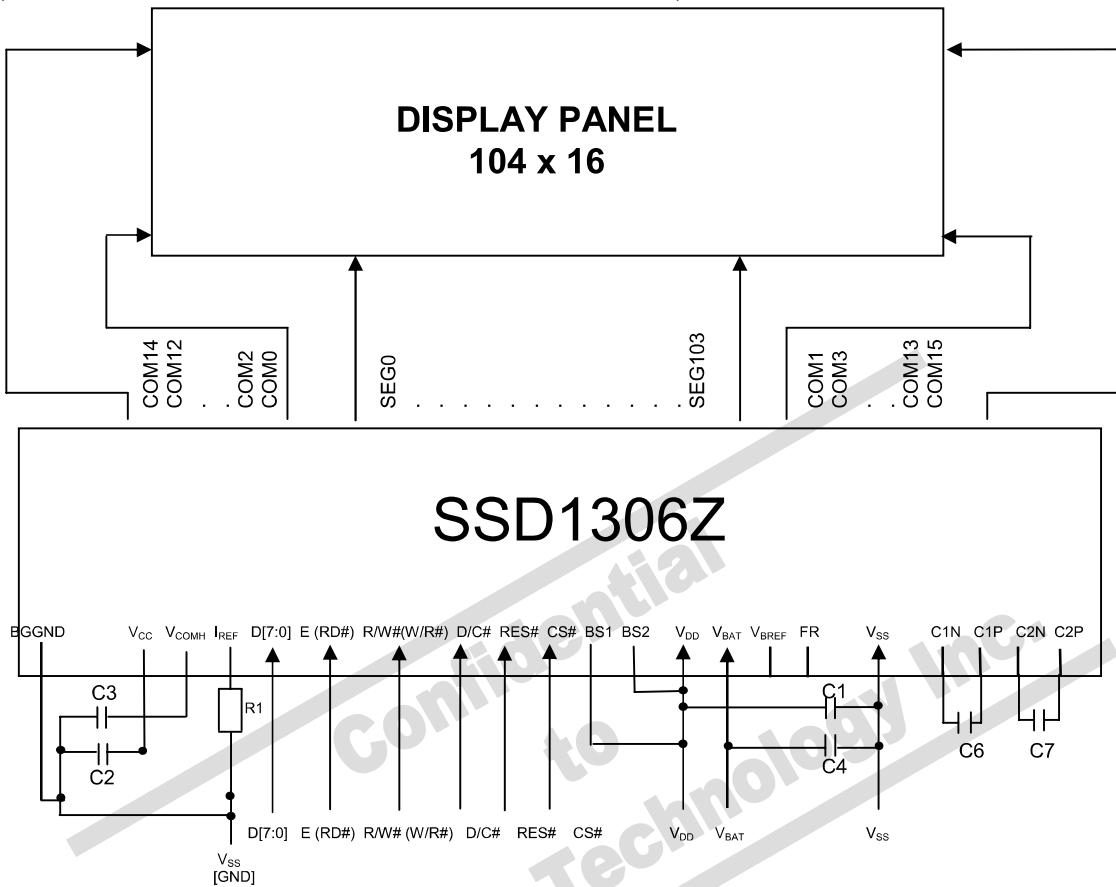
Status	V_{BAT}	V_{DD}	V_{CC}
Enable charge pump	Connect to external V_{BAT} source	Connect to external V_{DD} source	A capacitor should be connected between this pin and V_{SS}
Disable charge pump pin	Connect with V_{DD}	Connect to external V_{DD} source	Connect to external V_{CC} source
 - C1P/C1N – Pin for charge pump capacitor; Connect to each other with a capacitor
 - C2P/C2N – Pin for charge pump capacitor; Connect to each other with a capacitor

2.1 Command Table for Charge Pump Setting

1. Charge Pump Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	8D A[7:0]	1 *	0 *	0 0	0 1	1 0	1 A ₂	0 0	1 0	Charge Pump Setting	A[2] = 0b, Disable charge pump(RESET) A[2] = 1b, Enable charge pump during display on Note ⁽¹⁾ The Charge Pump must be enabled by the following command: 8Dh ; Charge Pump Setting 14h ; Enable Charge Pump AFh; Display ON

Figure 1 : Application Example of SSD1306Z with charge bump

The configuration for 8080-parallel interface mode is shown in the following diagram:
 $(V_{DD} = 1.65V \sim 3.3V, < V_{BAT}, V_{BAT}=3.3V\sim4.2V, I_{REF}=12.5\mu A)$



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, CS#, RES#

Pin internally connected to V_{SS}: BS0, CL

Pin internally connected to V_{DD}: CLS

V_{BREF}, FR should be left open.

C1, C4, C6, C7: 1.0uF ⁽¹⁾

C2, C3: 2.2uF ⁽¹⁾

Voltage at I_{REF} = V_{CC} - 2.5V. For V_{CC} = 7.5V, I_{REF} = 12.5uA:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$= (7.5-2.5) / 12.5\mu A$$

$$= 400K\Omega$$

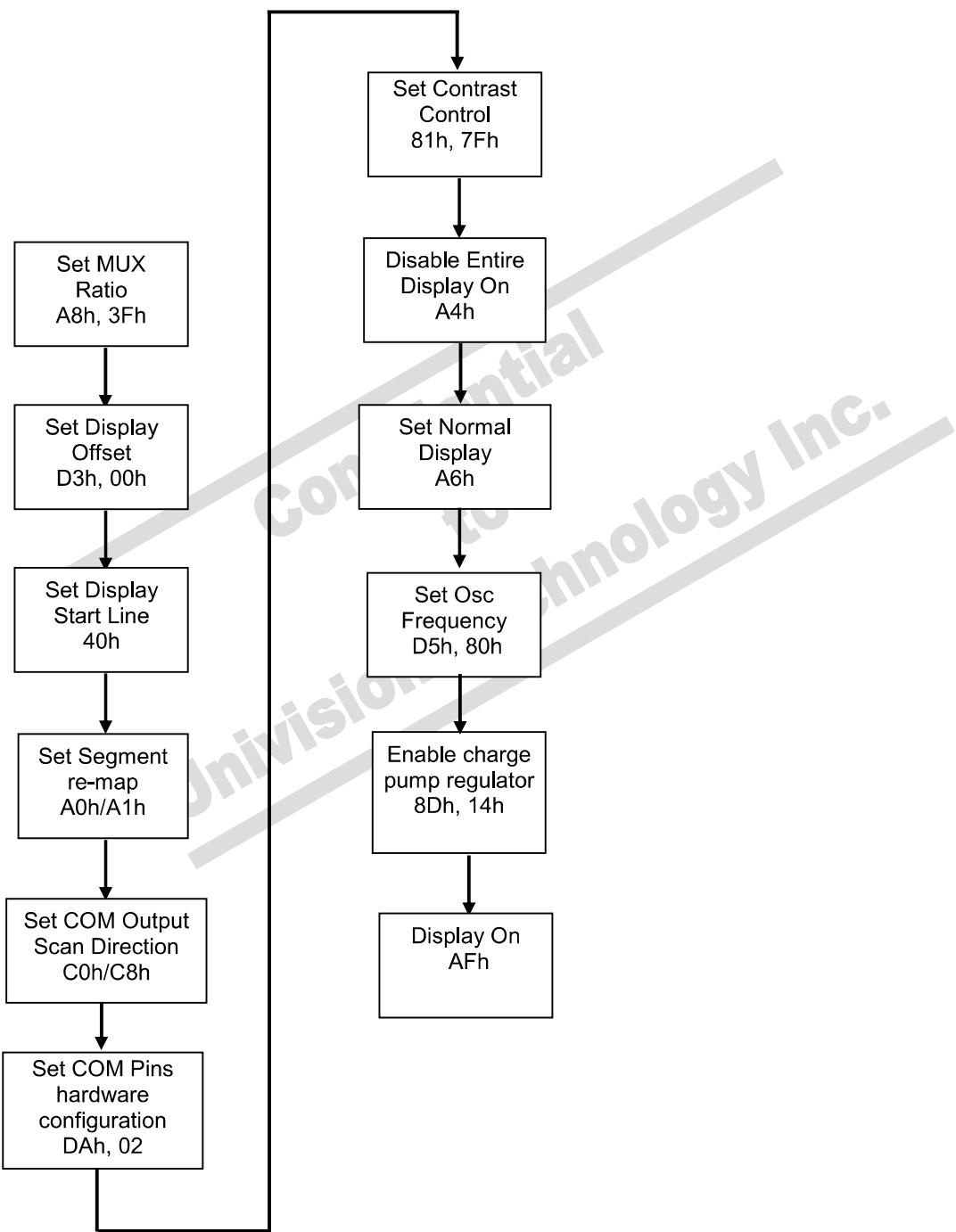
Note

⁽¹⁾ The capacitor value is recommended value. Select appropriate value against module application.

3 Software Configuration

SSD1306 has internal command registers that are used to configure the operations of the driver IC. After reset, the registers should be set with appropriate values in order to function well. The registers can be accessed by MPU interface in either 6800, 8080, SPI type with D/C# pin pull low or using I²C interface. Below is an example of initialization flow of SSD1306. The values of registers depend on different condition and application.

Figure 2 : Software Initialization Flow Chart



Confidential
to **Solomon Systech Inc.**

Solomon Systech reserves the right to make changes without notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any, and all, liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typical" must be validated for each customer application by the customer's technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) "Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)" and China standard "电子信息产品污染控制标识要求 (SJ/T11364-2006)" with control Marking Symbol . Hazardous Substances test report is available upon requested.

<http://www.solomon-systech.com>