

PAT9125EL: Optical Tracking Miniature Chip

General Description

The PAT9125EL is PixArt Imaging's low power optical tracking miniature chip using PixArt's LASER-based optical navigation technology enabling digital surface tracking. It integrates an optical chip with a LASER light source in a single miniature package, providing wide depth of field (DOF) range on glossy surfaces, and design flexibility into highly space constraint devices. This tracking system also does not require code wheel, code strip and any special marking on tracking surface for motion control or tracking purposes. It is recommended for use in hermetic or enclosed mechanical system design and applications. LASER power calibration process is NOT required in the complete system; it was pre-calibrated at chip level which helps to facilitate high volume assembly.

Key Features

- Miniature reflowable SMT package with built-in VCSEL LASER light source in a single package
- Wide DOF range on glossy surfaces, e.g. stainless steel (STS)
- No lens is needed
- Compliance to IEC/EN 60825-1 Eye Safety
 - Class 1 LASER power output level
 - On-chip LASER fault detection circuitry
- Support I²C or 3-wire SPI or interface
- Programmable resolution up to 1,275cpi (on flat STS)
- Motion detection interrupt output
- Efficient low power management with programmable sleep modes & downshift time
- Internal oscillator no external clock input needed

Applications

- Suitable for space-constraint and battery-powered wireless devices
- Devices that requires tracking on surfaces with wide DOF working range
- Devices that require tracking on small diameter of shaft and suitable for wearable and portable devices

Key Parameters

Parameter	Value
Supply Voltage	VDD: 2 connection types type1 $2.1 \sim 3.6V$ type2 $1.7 \sim 1.9V$
	VLD: 2.7 ~ 3.6V
Control Interface	I ² C or 3-wire SPI
Distance to tracking surface (DOF)	1 ~ 30mm (on STS surface)
Max. tracking speed	On flat STS ■ 30 ips @ distance ≥ 3mm ■ 10 ips @ distance 1~3mm On 1.0mm diameter STS shaft ■ 900 rpm @ distance ≥ 3mm
Max Resolution	■ 300 rpm @ distance 1~3mm ~1,275 cpi (on flat STS) or ~630 counts/rev (on 1.0mm diameter STS shaft at 1.0mm distance)
Operating current (Average @ VDD = VLD = 3.3V)	Run : 0.7mA Sleep1/2 : 25μA / 10uA Power down : 5μA
Light Source	VCSEL LASER 850 nm
Package Size LWH	3.5 x 3.2 x 1.0 mm

Ordering Information

Part Number	Interface	Package Type
PAT9125EL-TKIT	I ² C	LGA 8-pin
PAT9125EL-TKMT	SPI	LGA 8-pin









For any additional inquiries, please contact us at http://www.pixart.com/contact.asp

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1.0 Introduction

1.1 Overview

PAT9125EL is a high performance and an ultralow power CMOS-processed optical navigation chip with the integrated digital image process algorithm/circuits and a VCSEL LASER as the light source. It is based on PixArt's optical navigation technology of LASER which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the speed, the direction and the magnitude of motion. The displacement X and Y information are available in registers. A host controller can read and translate the displacement X and Y information from the SPI or I²C serial interface. **Note:** Throughout this document PAT9125EL is referred to as the chip.

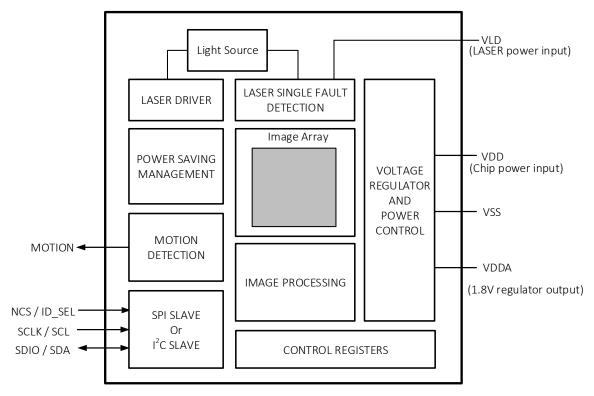


Figure 1. Functional Block Diagram

1.2 Signal Description

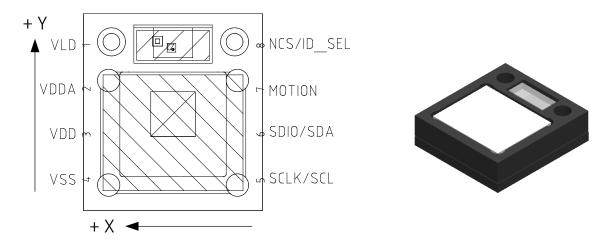


Figure 2. Pin Configuration

Table 1. Signal Pins Description

Dis No	Signal	Signal Name		Description.
Pin No.	SPI	I ² C	Туре	Description
1	VLD	VLD	PWR	Anode of the VCSEL LASER, voltage range: 2.7V ~ 3.3V
2	VDDA	VDDA	PWR	VDD is the main power supply for IC circuits
				High voltage Segment (VDD: 2.1V $^{\sim}$ 3.6V): VDDA is 1.8V regulator output and
3	VDD	VDD	PWR	should connect a 4.7uF capacitor to ground
				Low Voltage Segment (VDD: 1.7V ~ 2.1V): VDDA should connect to VDD directly
4	VSS	VSS	GND	Chip ground
5	SCLK	SCL	IN	SCLK : Clock input for SPI interface
<u> </u>	SCLK	SCL	IIN	SCL : Clock input for I ² C interface
6	SDIO	SDA	I/O	SDIO : Bi-directional I/O for SPI interface
	טוטנ	SDA	1/0	SDA : Bi-directional I/O for I ² C interface
7	MOTION	MOTION	OUT	Motion detection output (active low)
				NCS : Chip select for 3-wire SPI interface (active low)
8	NCS	ID_SEL	IN	ID_SEL : Slave ID (7-bit) Selection for I ² C interface
				High = 0x73, Low=0x75, NC = 0x79
9	TEST	TEST	NC	This pin is located on the back of the chip and is for PixArt testing purpose.
	9 TEST TEST NC		IVC	Please do NOT connect it to any part of the PCB. Please refer to Figure 9.

1.3 Potential Tracking Mechanisms



Figure 3. Tracking on a Moving Surface

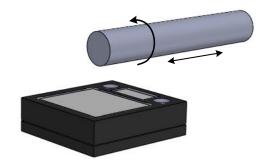


Figure 4. Tracking on the Side of a Rotational Shaft

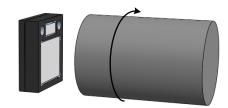


Figure 5. Tracking on the end of a Rotational Shaft



Figure 6. Tracking on a Disk Edge



Figure 7. Tracking on a Rotational Bezel

1.4 Terminologies

Term	Description
ACK	Acknowledge bit of I ² C bus
CPI	Counts per Inch
DOF	Depth of Field
FPS	Frames per Second
I ² C	Inter-Integrated Circuit
IPS	Inches per Second
LD	LASER Diode
LGA	Land Grid Array
LOP	LASER output power, unit: uW (micro-watt)
NA	Not-acknowledge bit of I ² C bus
RPM	Revolutions per Minute
SPI	Serial Peripheral Interface
STS	Stainless Steel
VCSEL	Vertical-Cavity Surface-Emitting LASER

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_{STG}	-40	85	°C	
Power Supply Voltage	V_{DC}	-0.3	3.9	V	
Signal Input Voltage	V _{IN}	-0.3	V_{DC}	V	For all input I/O
Lead Solder Temp	T _{SOL}	-	260	°C	Non-condensing, Non-biased
ESD	V_{HBM}	-	2	1 K\/	All pins, Human Body Model MIL 883 Method 3015

Notes:

- 1. At room temperature.
- 2. Maximum Ratings are those values beyond which damage to the device may occur.
- 3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
- 4. Functional operation should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Тур.	Max.	Unit	Notes
Operating Temperature	T _A	-20	-	60	°C	
	VDD	2.1	-	3.6	V	For chip operated in High Voltage Segment
Power Supply Voltage	VUU	1.7	1.8	1.9	V	For chip operated in Low Voltage Segment
	VLD	2.7	3.0	3.6	V	For LASER Power
Supply Noise	V_{NPP}	-	-	100	mV	Peak to peak voltage within 10kHz – 80 MHz
Distance to Tracking Surface (DOF)	Z	1		30	mm	On STS surface (refer to Notes below)
		-	-	30	ips	Based on flat STS with distance ≧ 3mm
				10	ips	Based on flat STS with distance 1~3mm
Tracking Speed	V_{SP}			900	rpm	Based on 1.0mm diameter STS shaft with distance \geq 3mm
				300	rpm	Based on 1.0mm diameter STS shaft with distance 1~3mm

Notes:

- 1. PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.
- 2. When the distance to tracking surface is < 3mm, the reported CPI resolution could be lower than the CPI value at \geq 3mm. Please refer to Figure 8 below.

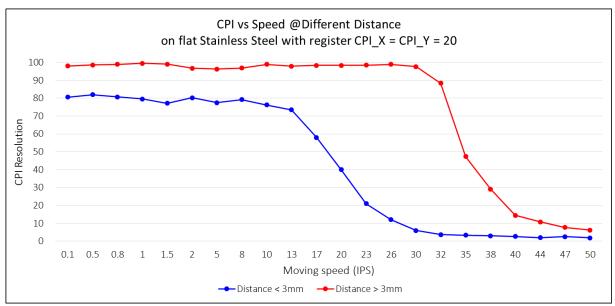


Figure 8. CPI vs Speed @Different Distance

2.3 DC Characteristics

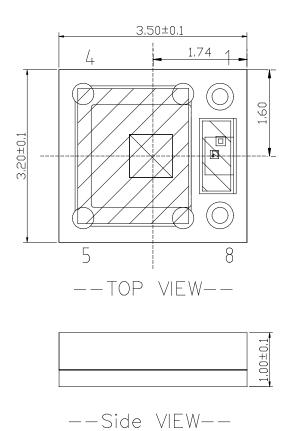
Table 4. DC Electrical Specifications

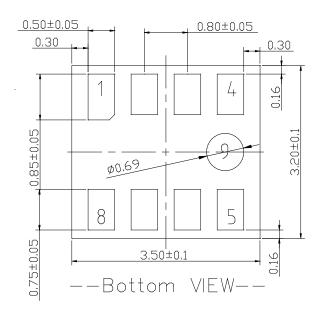
Parameters	Symbol	Min.	Тур.	Max.	Unit	Conditions
Run mode current			0.7		mΛ	Tracking speed dependent
	I _{RUN}	1	0.7	-	mA	@VDD=VLD=3.3V on STS
Class 1 made ourrent			2.5		^	Based on 32ms sampling period
Sleep 1 mode current	I _{SLP1}	-	25	-	μΑ	@VDD=VLD=3.3V on STS
Class 2 manda ayumant	I _{SLP2}	-	10		μΑ	Based on 128ms sampling period
Sleep 2 mode current						@VDD=VLD=3.3V on STS
Power Down current	I _{PD}	-	5	10	μΑ	@VDD=VLD=3.3V
Input Voltage High	V _{IH}	VDD*0.7	-	-	V	
Input Voltage Low	V_{IL}	ı	1	VDD*0.3	V	For NCS, SCLK, SDIO, MOTION pins
Output Voltage High	V _{OH}	VDD-0.4	-	-	V	TOT NCS, SCLK, SDIO, MOTION PINS
Output Voltage Low	V _{OL}	-	-	0.4	V	

Notes: All the parameters are tested under operating conditions: $T_A = 25$ °C

3.0 Mechanical Specifications

3.1 Mechanical Dimension





Note:

1. All dimensions are in mm

Figure 9. Package Outline Diagram

4.0 Reference Schematics

4.1 Schematics for I²C Interface (PAT9125EL-TKIT)

The chip supports standard I²C interface and the SCL clock speed is up to 1MHz. Three different Slave IDs can be selected from the ID_SEL pin (High = 0x73, Low=0x75, NC = 0x79). Notice that $5K\Omega$ of R1 and R2 (SCL/SDA bus pull-high resistors) is just for reference and the resistance might have to be adjusted according to the overall I²C bus loading of user's whole system.

4.1.1 High Voltage Segment (VDD: 2.1V ~ 3.6V)

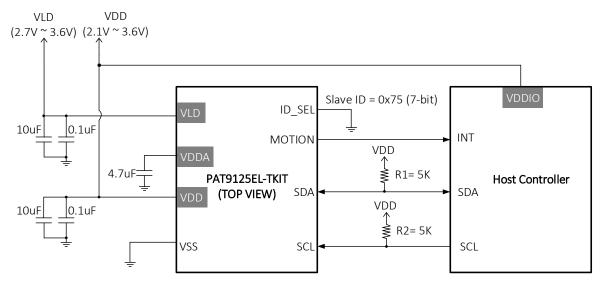


Figure 10. Schematics for High Voltage Segment (I²C Interface)

4.1.2 Low Voltage Segment (VDD : 1.7V ~ 1.9V)

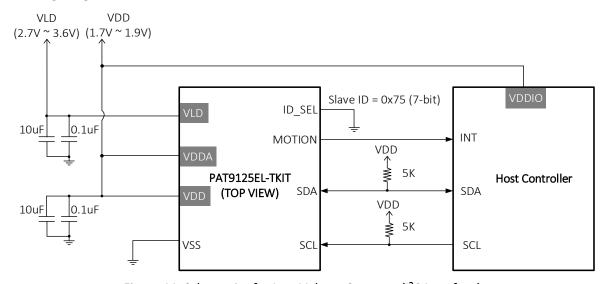


Figure 11. Schematics for Low Voltage Segment (I²C Interface)

4.2 Schematics for SPI Interface (PAT9125EL-TKMT)

The chip only supports simplified 3-wire SPI slave mode, while some host controllers only support standard 4-wire SPI master mode. In this case, users can connect the host controller to the chip using the method shown below to communicate each other. Notice that $3.3K\Omega$ for R1 is just for reference and the resistance might have to be modified according to different I/O capability of different host controllers.

4.2.1 High Voltage Segment (VDD: 2.1V~3.6V)

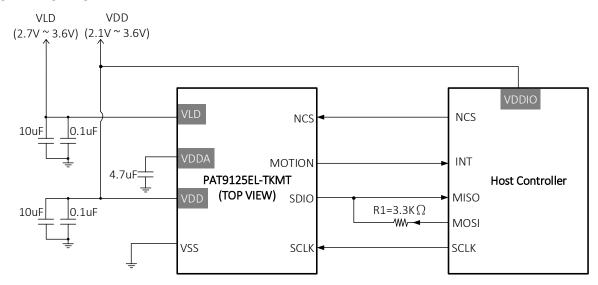


Figure 12. Schematics for High Voltage Segment (SPI Interface)

4.2.2 Low Voltage Segment (VDD: 1.7V ~ 1.9V)

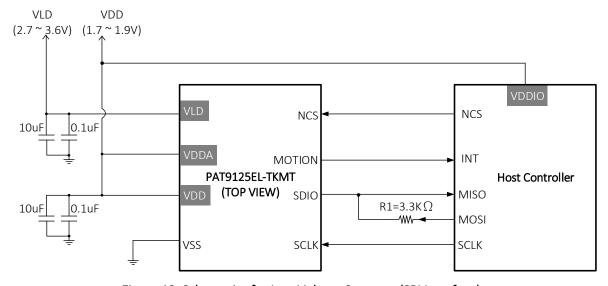


Figure 13. Schematics for Low Voltage Segment (SPI Interface)

5.0 Registers List

Address	Register Name	Access	Reset	Brief Description	
0x00	Product_ID1	RO	0x31	Product Identifier [11:4]	
0x01	Product_ID2	RO	0x91 Upper 4 bits for Product Identifier, PID [3:0] Lower 4 bits for Product Version, VID [3:0]		
0x02	Motion_Status	RO	-	Motion Status information	
0x03	Delta_X_Lo	RO	1	8-bit 2's complement number for X-movement data in 8-bit movement data format X-movement = Delta_X_Lo[7:0]	
0x04	Delta_Y_Lo	RO	-	8-bit 2's complement number for Y-movement data in 8-bit movement data format Y-movement = Delta_Y_Lo[7:0]	
0x05	Operation_Mode	R/W	0xA0	0xA0 Operation mode selection	
0x06	Configuration	R/W	0x17	0x17 Software power down and reset	
0x09	Write_Protect	R/W	0x00	Write Protect to avoid missed-writing registers	
0x0A	Sleep1	R/W	0x77 Sleep1 configuration		
0x0B	Sleep2	R/W	0x10 Sleep2 configuration		
0x0D	RES_X	R/W	0x14	CPI resolution setting for X axis	
0x0E	RES_Y	R/W	0x14	CPI resolution setting for Y axis	
0x12	Delta_XY_Hi	RO	-	High nibble of X-movement and Y-movement for 12-bit 2's complement data format. X-movement = {Delta_XY_Hi[7:4], Delta_X_Lo[7:0]} Y-movement = {Delta_XY_Hi[3:0], Delta_Y_Lo[7:0]}	
0x14	Shutter	RO	-	Index of LASER shutter time	
0x17	Frame_Avg	RO	-	Average brightness of a frame	
0x19	Orientation	R/W	0x04	Chip orientation selection	

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Document Revision History

Revision Number	Date	Description			
1.1	05 Apr 2017	Based on DS v1.1			
1.2	31 May 2017	Based on DS v1.1 1. Widened the spec. of VDD from 2.1V~3.3V to 2.1V~3.6V 2. Widened the spec. of VLD from 2.7V~3.3V to 2.7V~3.6V 3. Added LASER Class 1 Product logo			